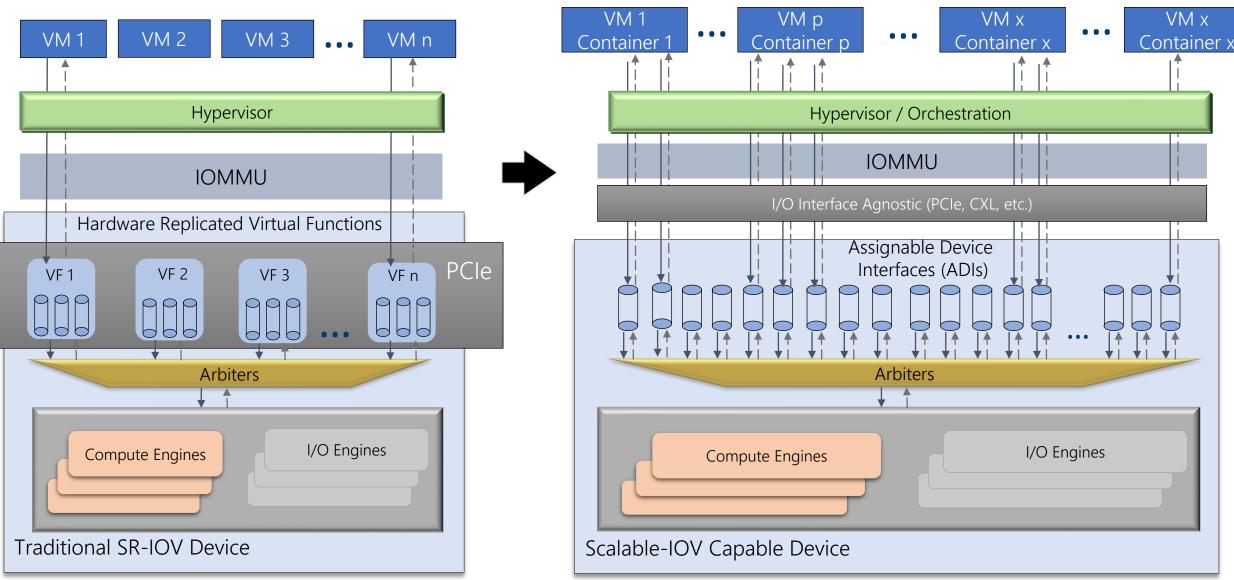
Scalable-IOV Contribution

Tom Stachura, Intel Corporation Rajesh Sankaran, Intel Corporation

OCP: Server Project Meeting, October 27, 2021

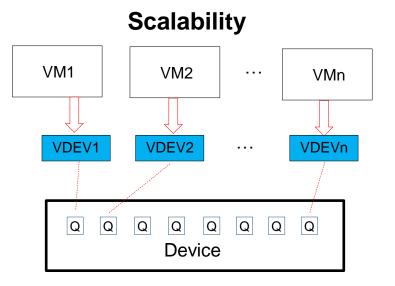
Disclaimer: The current <u>Scalable-IOV specification</u> is posted on the Intel web site with a granted copyright license. Intel is in process of developing the CLA to contribute this to OCP.

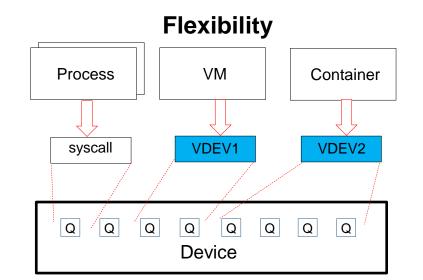
SR-IOV (Single-Root I/O V) → Scalable I/O Virtualization (Scalable-IOV)



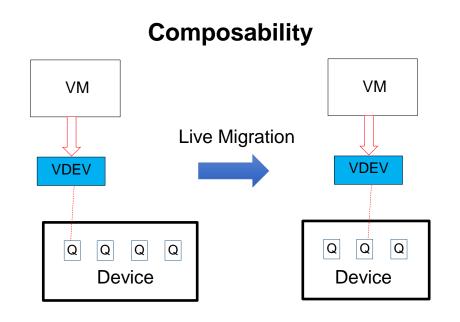
• While SR-IOV maps virtual devices as Virtual Functions (VFs) in HW, S-IOV composes virtual devices through light-weight and scalable Assignable Device Interfaces (ADIs) for fast-path operations and software mediated slow-path operations

Scalable IOV Benefits





Over-provisioning VDEV1 VDEV2 Q Q Q Q Q Q Q Device



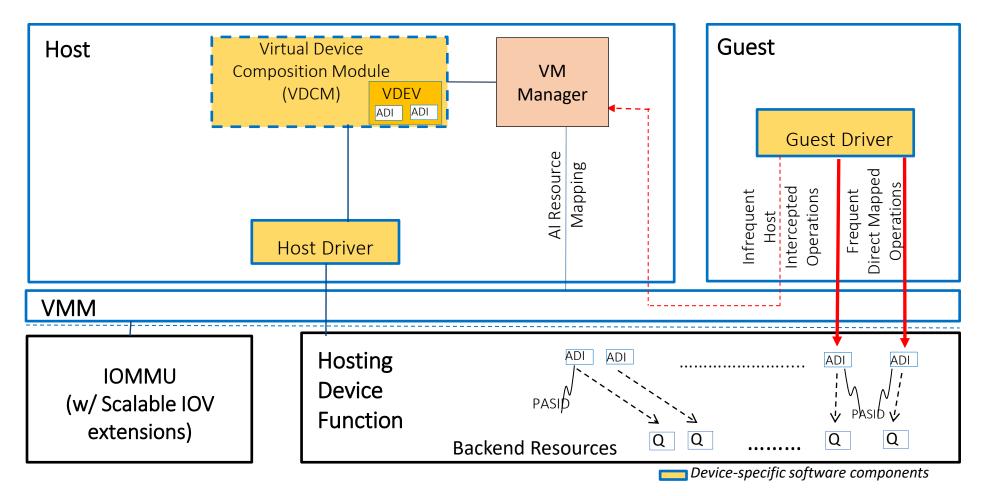
Proposed Scalable I/O Virtualization (S-IOV) Path

- 1. Contribute Scalable-IOV to OCP
 - Intel in process of drafting CLA for <u>Scalable-IOV specification</u> contribution
- 2. Create workstream with interested stakeholders to define next version of Scalable-IOV. Example areas of scope (to be formalized in workstream):
 - Standard method for S-IOV enumeration and ADI identification
 - Standard method for scaling interrupt message storage for ADIs
 - Extensions to support confidential computing (trusted execution) with ADIs
 - Extensions to optimize live migration of virtual devices backed by ADIs
 - Considerations for CXL devices supporting ADIs
 - QoS associations and management for ADIs
 - Enhancements to Address translation services (ATS) for ADIs

Output of the workstream could include ECRs to be submitted for extensions to relevant specifications such as PCI-Express and CXL

BACKUP

Scalable IOV: High Level Software Architecture



Device specific VDCM to decide what to intercept vs direct map

Emulating infrequent operations in VDCM simplifies device without compromising performance