

F20 SIDE PLANE


PCB REV: D

PCBA REV: D3A

FAB: 5

SCH Rev: V01

LAST UPDATE: 2015/12/22

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Yosemite Block Diagram V0.07

OCV V2 40GE Mezz or 10GBASE-KR Mezz with QSFP+ Conn

Adaptor board

Slot1
1S Server Card

Slot2
1S Server Card

Slot3
1S Server Card

Slot4
1S Server Card

BMC (AST1250)

HotSwap
Controllers

Temp
Seosors
(Inlet and Outlet)

FRU

Fan x 2

Power Button
Reset Button
Select Switch
LEDs

Analog
Sensors

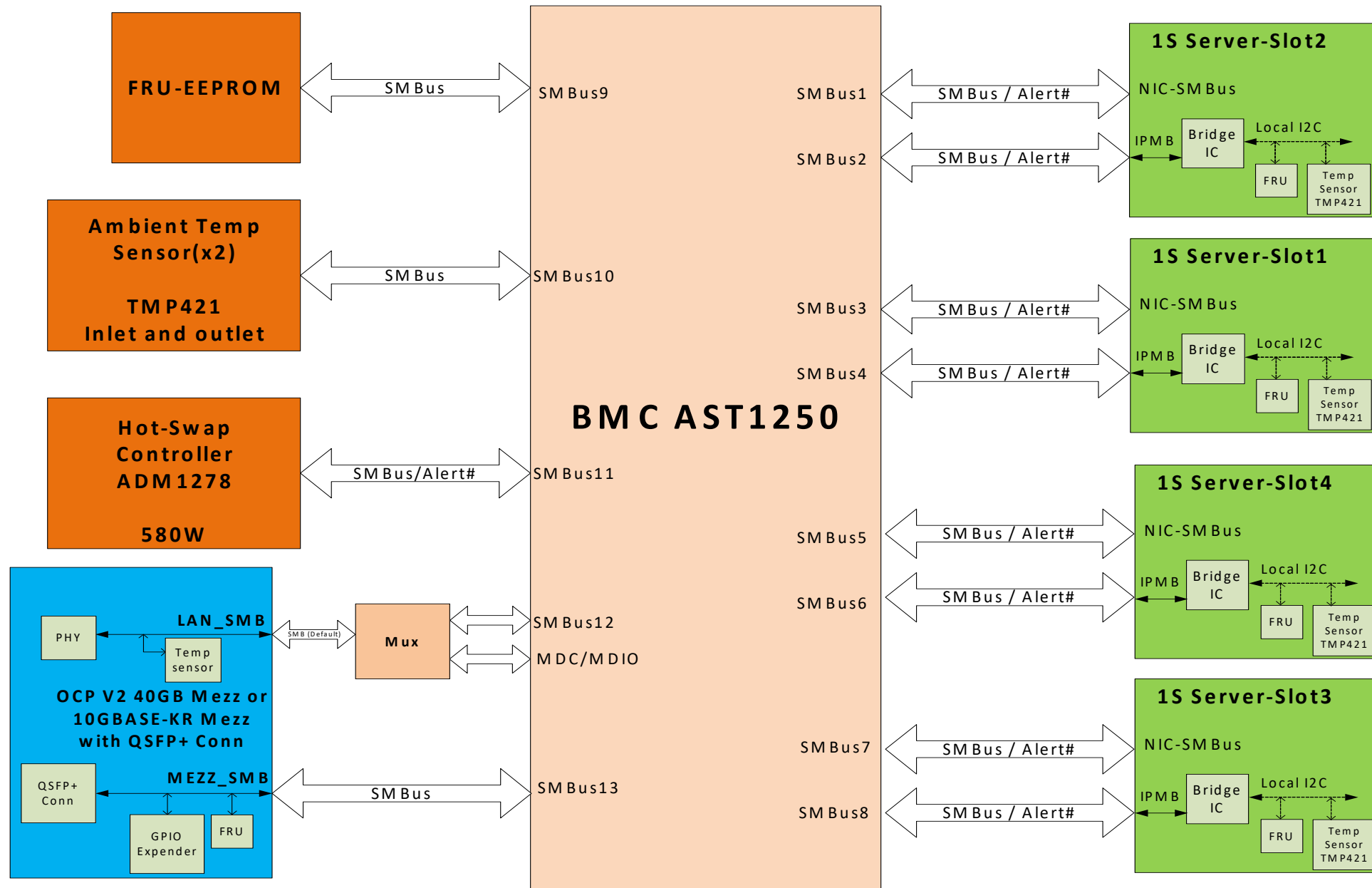
OCV Debug
Card

USB MUX

USB HUB

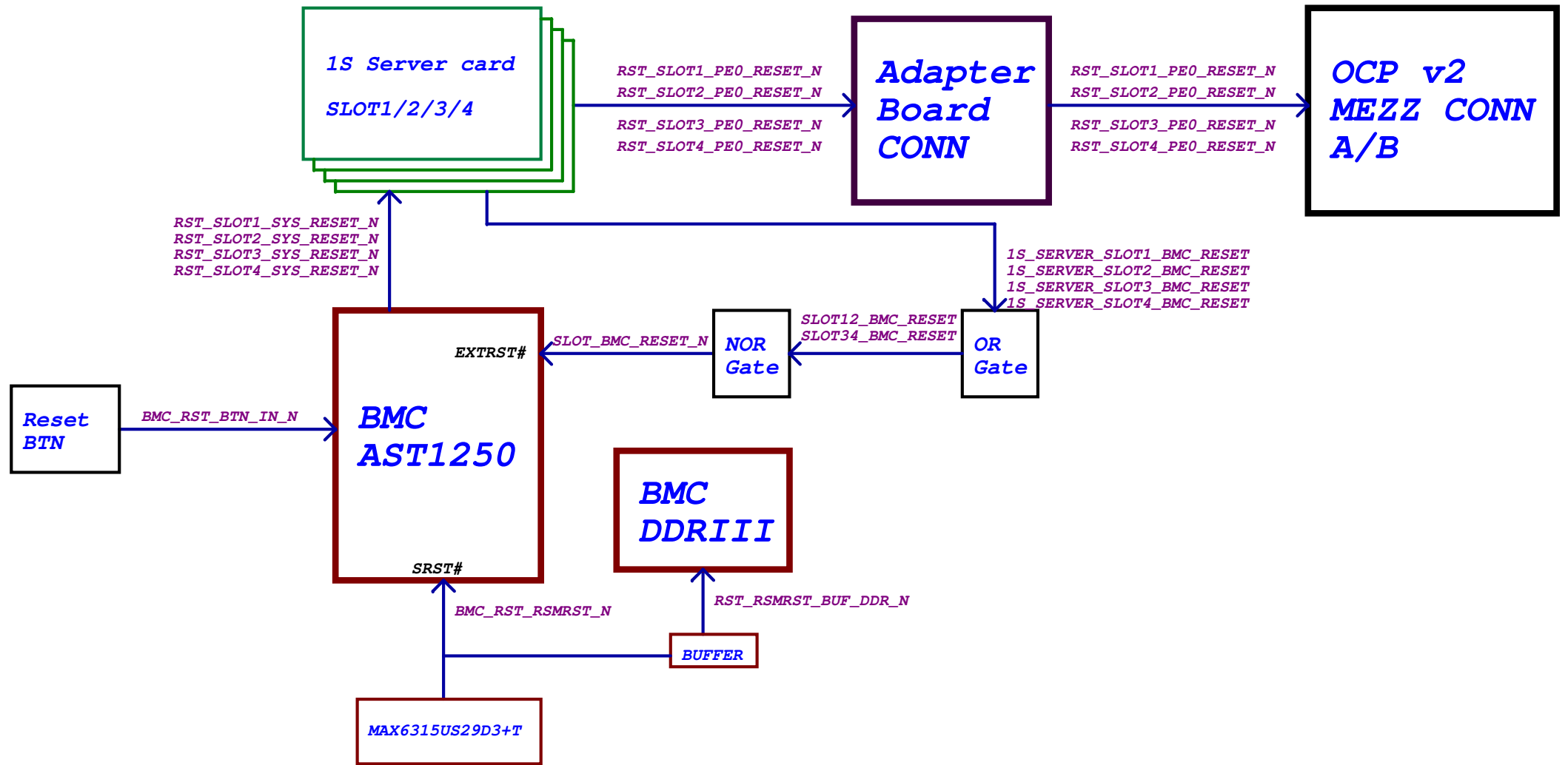
USB Conn

Yosemite SMB Diagram V0.05



SMBus Block Diagram

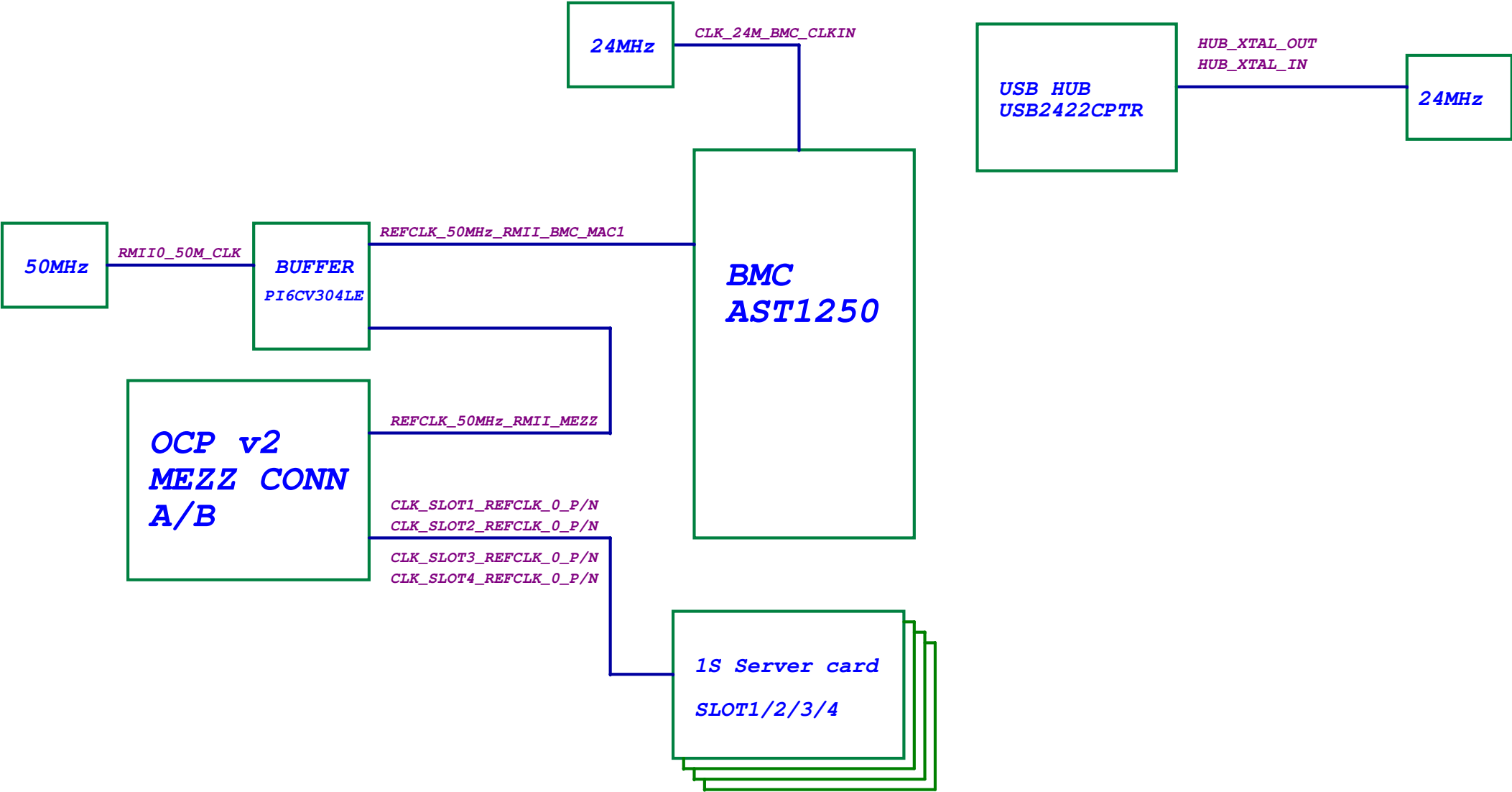
Reset Block Diagram v02



Reset Block Diagram

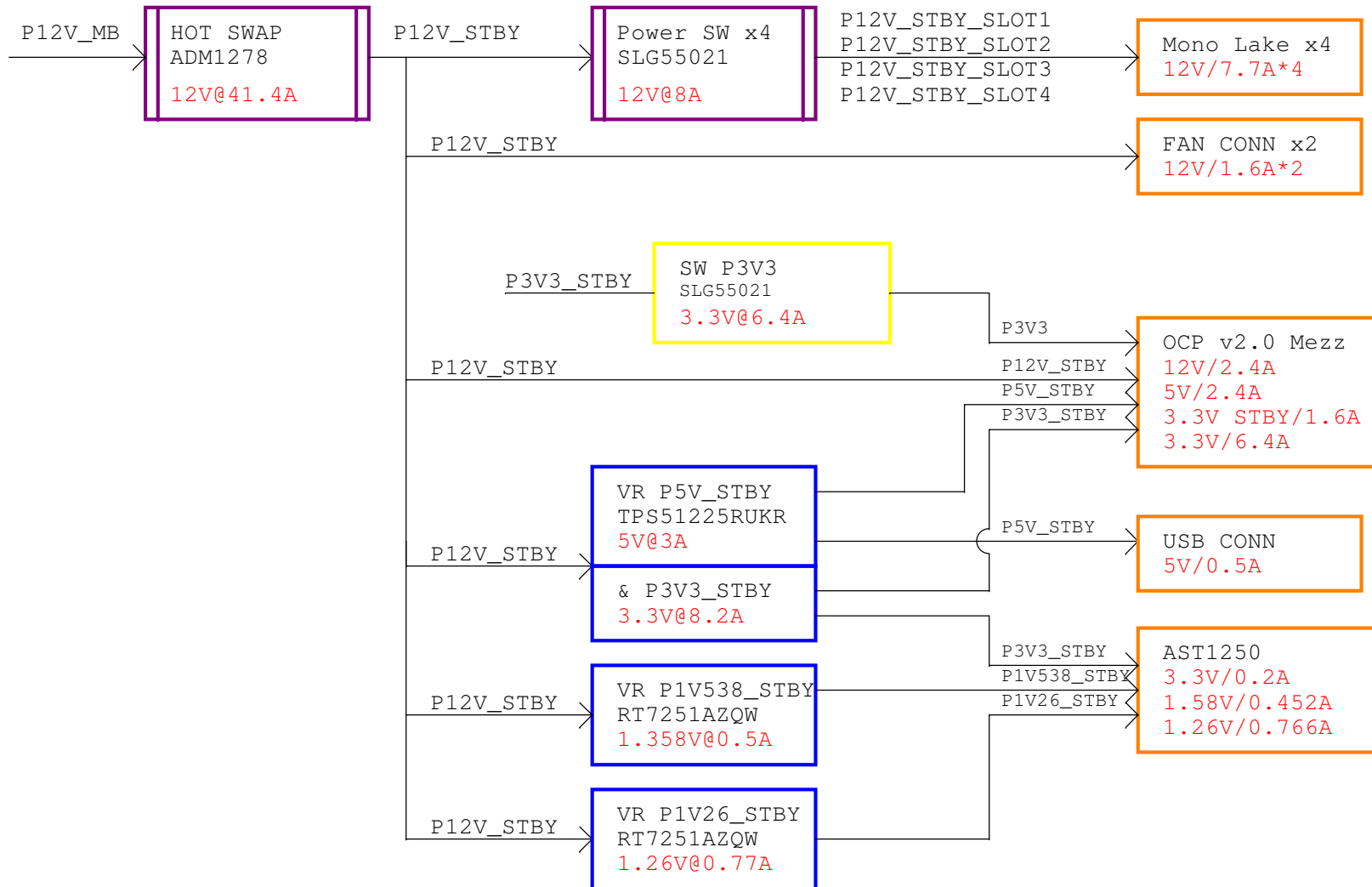
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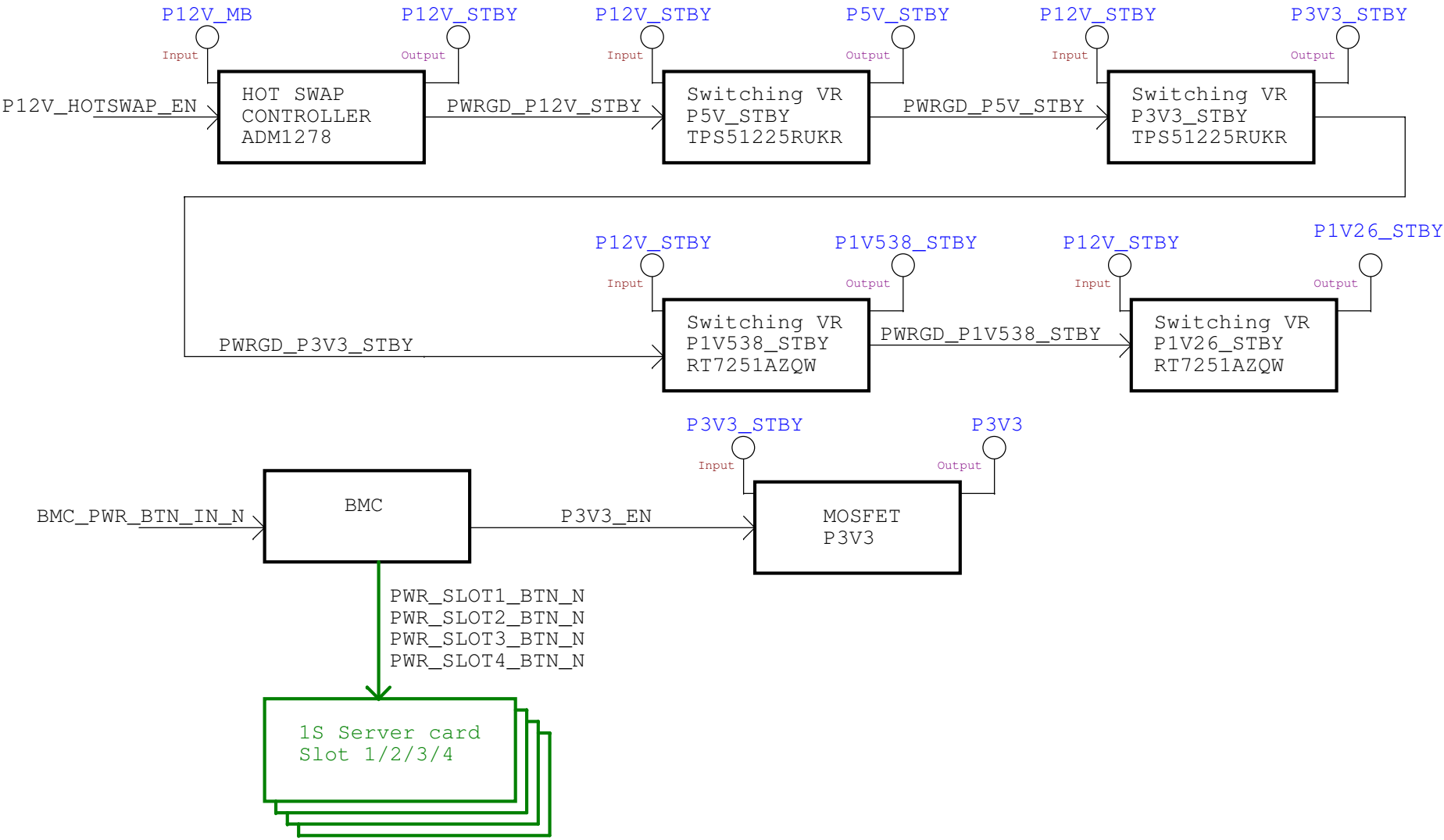


Clock Block Diagram

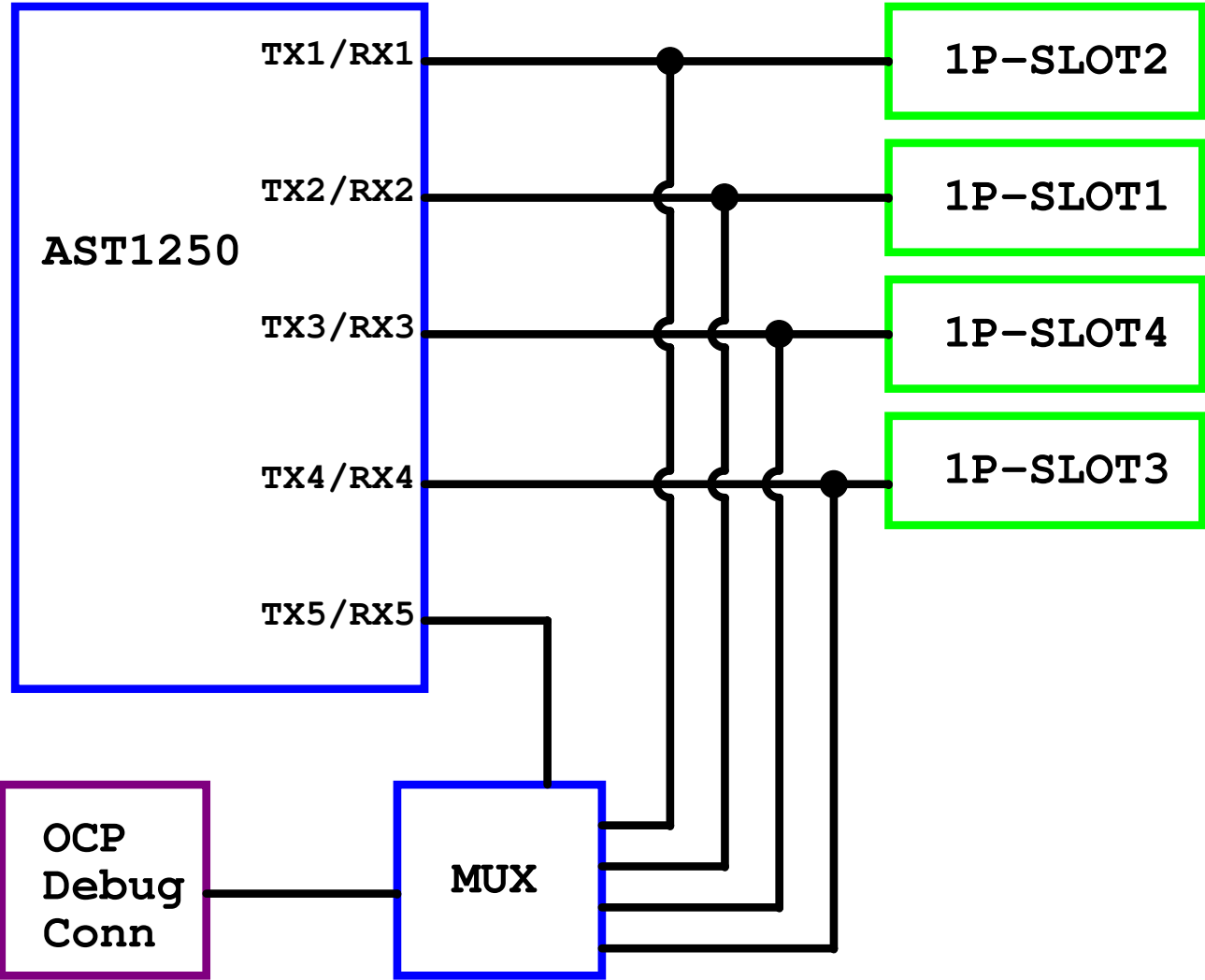
Power Block Diagram v0.4



Power Sequence SYSTEM v0.4



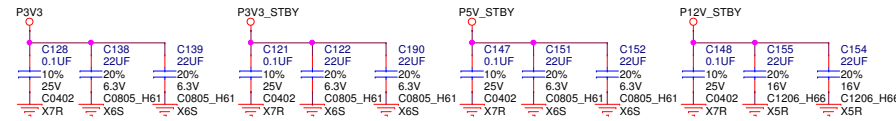
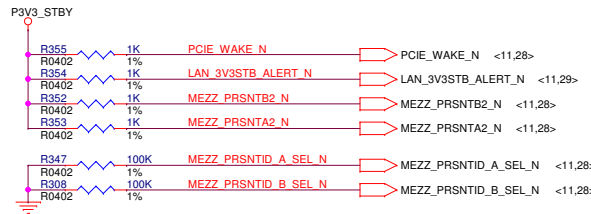
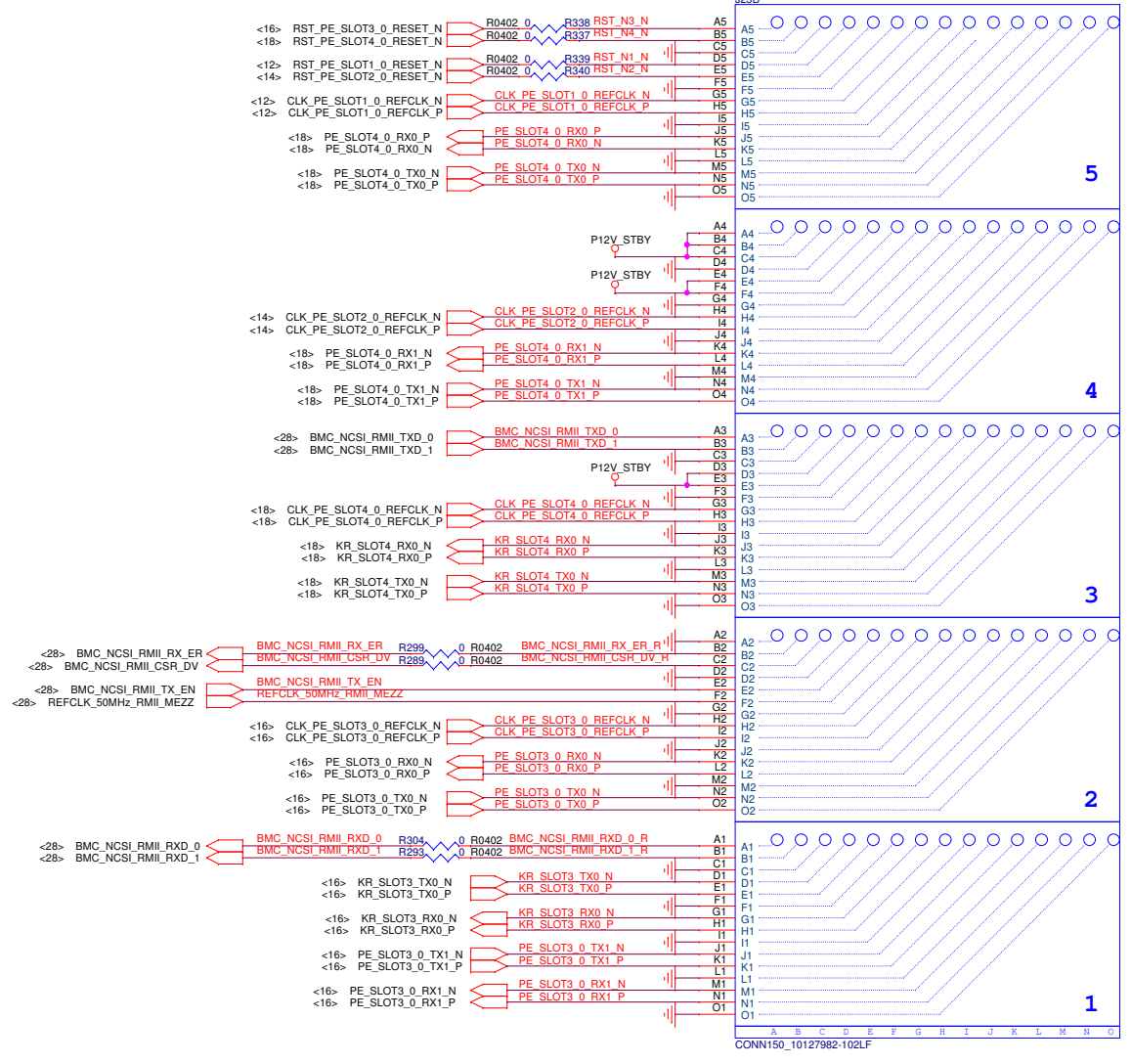
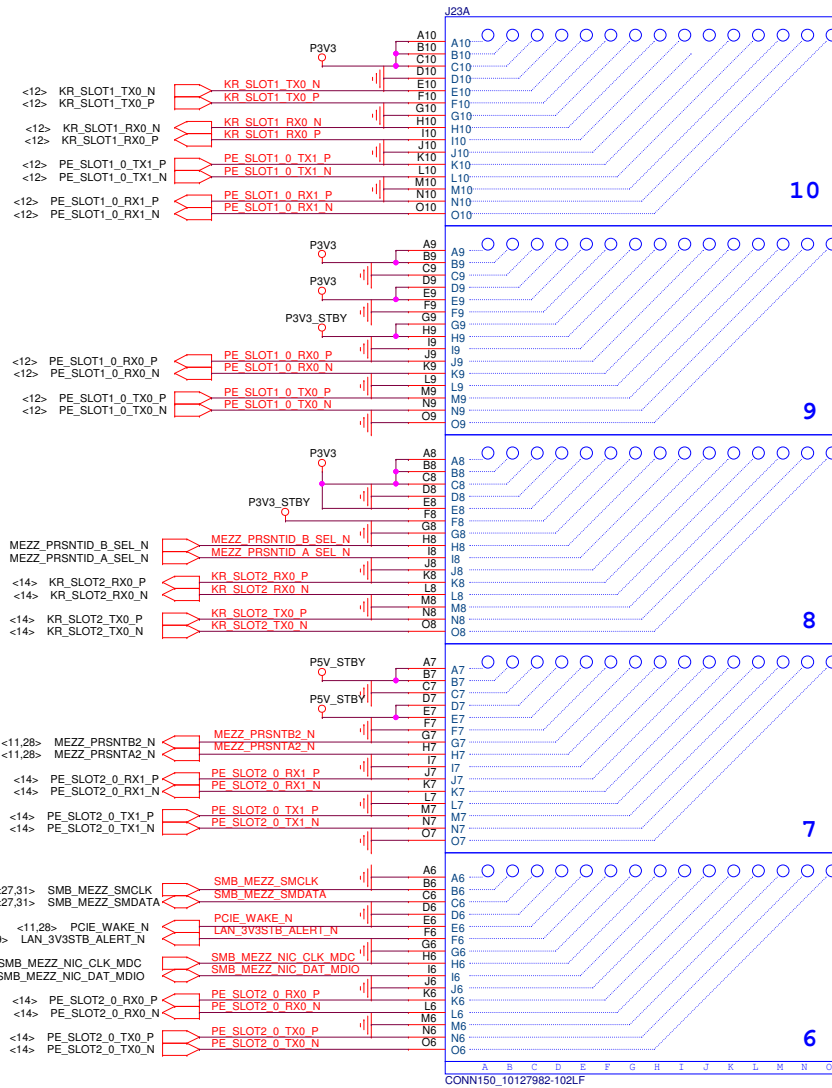
UART Topology v0.2



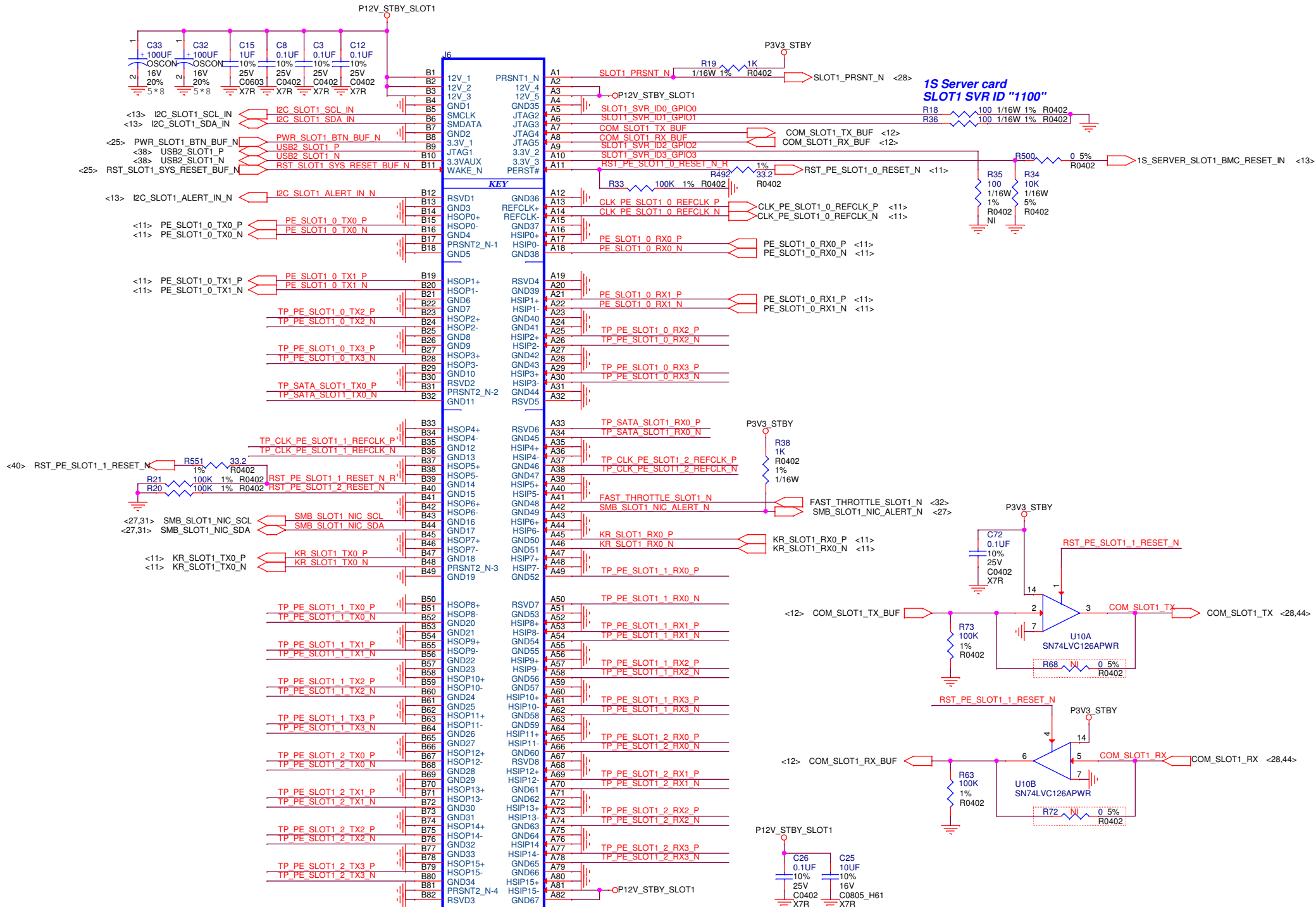
	10	9	8	7	6	5	4	3	2	1
P	No Pin		No Pin		No Pin		No Pin		No Pin	
O	PE_SLOT1_0_RX1_N	GND	KR_SLOT2_TX0_N	GND	PE_SLOT2_0_TX0_N	GND	PE_SLOT4_0_TX1_P	GND	PE_SLOT3_0_TX0_P	GND
N	PE_SLOT1_0_RX1_P	PE_SLOT1_0_TX0_N	KR_SLOT2_TX0_P	PE_SLOT2_0_TX1_N	PE_SLOT2_0_TX0_P	PE_SLOT4_0_TX0_P	PE_SLOT4_0_TX1_N	KR_SLOT4_TX0_P	PE_SLOT3_0_TX0_N	PE_SLOT3_0_RX1_P
M	GND	PE_SLOT1_0_TX0_P	GND	PE_SLOT2_0_TX1_P	GND	PE_SLOT4_0_TX0_N	GND	KR_SLOT4_TX0_N	GND	PE_SLOT3_0_RX1_N
L	PE_SLOT1_0_TX1_N	GND	KR_SLOT2_RX0_N	GND	PE_SLOT2_0_RX0_N	GND	PE_SLOT4_0_RX1_P	GND	PE_SLOT3_0_RX0_P	GND
K	PE_SLOT1_0_TX1_P	PE_SLOT1_0_RX0_N	KR_SLOT2_RX0_P	PE_SLOT2_0_RX1_N	PE_SLOT2_0_RX0_P	PE_SLOT4_0_RX0_N	PE_SLOT4_0_RX1_N	KR_SLOT4_RX0_P	PE_SLOT3_0_RX0_N	PE_SLOT3_0_TX1_P
J	GND	PE_SLOT1_0_RX0_P	GND	PE_SLOT2_0_RX1_P	GND	PE_SLOT4_0_RX0_P	GND	KR_SLOT4_RX0_N	GND	PE_SLOT3_0_TX1_N
I	KR_SLOT1_RX0_P	GND	MEZZ_PRSENTI_D_A_SEL_N	GND	SMB_MEZZ_NI_C_DAT_MDIO	GND	CLK_PE_SLOT2_0_REFCLK_P	GND	CLK_PE_SLOT3_0_REFCLK_P	GND
H	KR_SLOT1_RX0_N	P3V3_STBY	MEZZ_PRSENTI_D_B_SEL_N	MEZZ_PRSENTA2_N	SMB_MEZZ_NI_C_CLK_MDC	CLK_PE_SLOT1_0_REFCLK_P	CLK_PE_SLOT2_0_REFCLK_N	CLK_PE_SLOT4_0_REFCLK_P	CLK_PE_SLOT3_0_REFCLK_N	KR_SLOT3_RX0_P
G	GND	P3V3_STBY	GND	MEZZ_PRSENTB2_N	GND	CLK_PE_SLOT1_0_REFCLK_N	GND	CLK_PE_SLOT4_0_REFCLK_N	GND	KR_SLOT3_RX0_N
F	KR_SLOT1_TX0_P	GND	P3V3_STBY	GND	LAN_3V3STB_ALERT_N	GND	P12V_STBY	GND	BMC_NCSI_RMII_TX_EN	GND
E	KR_SLOT1_TX0_N	P3V3	P3V3	P5V_STBY	PCIE_WAKE_N	RST_N2_N	P12V_STBY	P12V_STBY	REFCLK_50MHz_RMII_MEZZ	KR_SLOT3_TX0_P
D	GND	P3V3	GND	P5V_STBY	GND	RST_N1_N	GND	P12V_STBY	GND	KR_SLOT3_TX0_N
C	P3V3	GND	P3V3	GND	SMB_MEZZ_SMDATA	GND	P12V_STBY	GND	BMC_NCSI_RMII_CSR_DV_R	GND
B	P3V3	P3V3	P3V3	P5V_STBY	SMB_MEZZ_S_MCLK	RST_N4_N	P12V_STBY	BMC_NCSI_RMII_TXD_1	BMC_NCSI_RMII_RX_ER	BMC_NCSI_RMII_RXD_1_R
A	P3V3	P3V3	P3V3	P5V_STBY	GND	RST_N3_N	P12V_STBY	BMC_NCSI_RMII_TXD_0	GND	BMC_NCSI_RMII_RXD_0_R

Adapter Board CONN Pin mapping

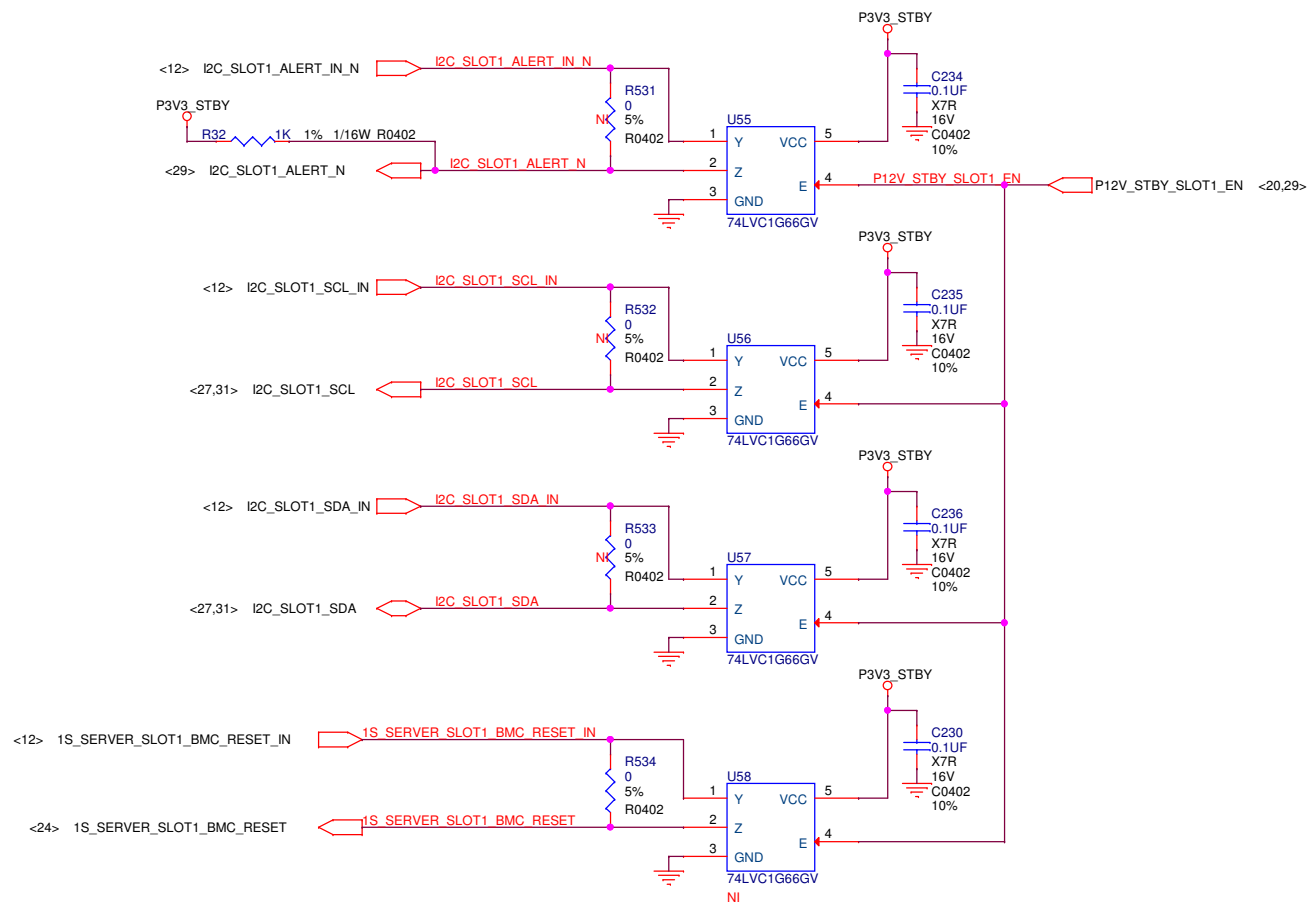
Vertical Air Max conn: FCI# 10127982-102LF



Adapter Board CONN

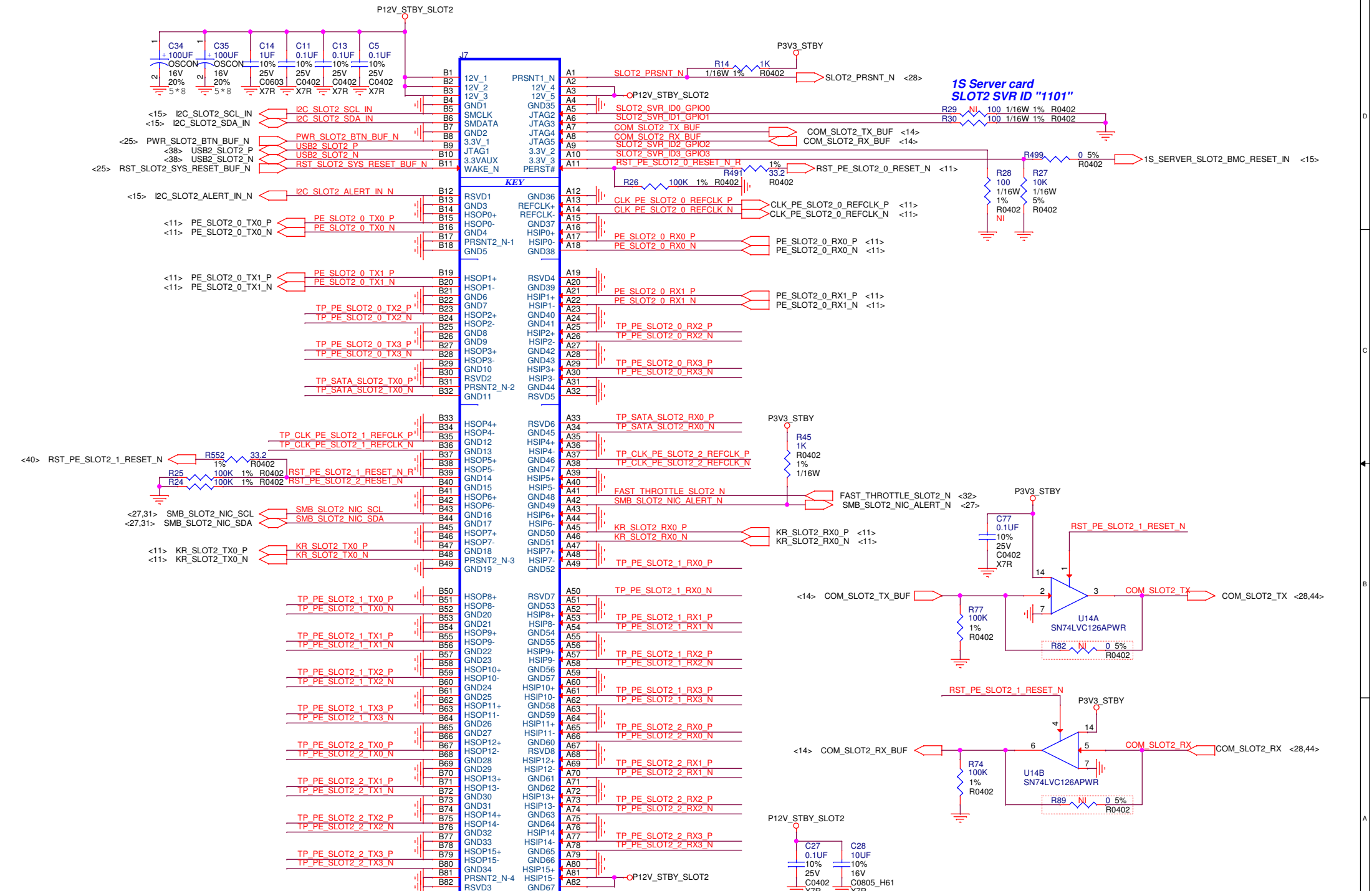


Slot1 x16 conn - Primary



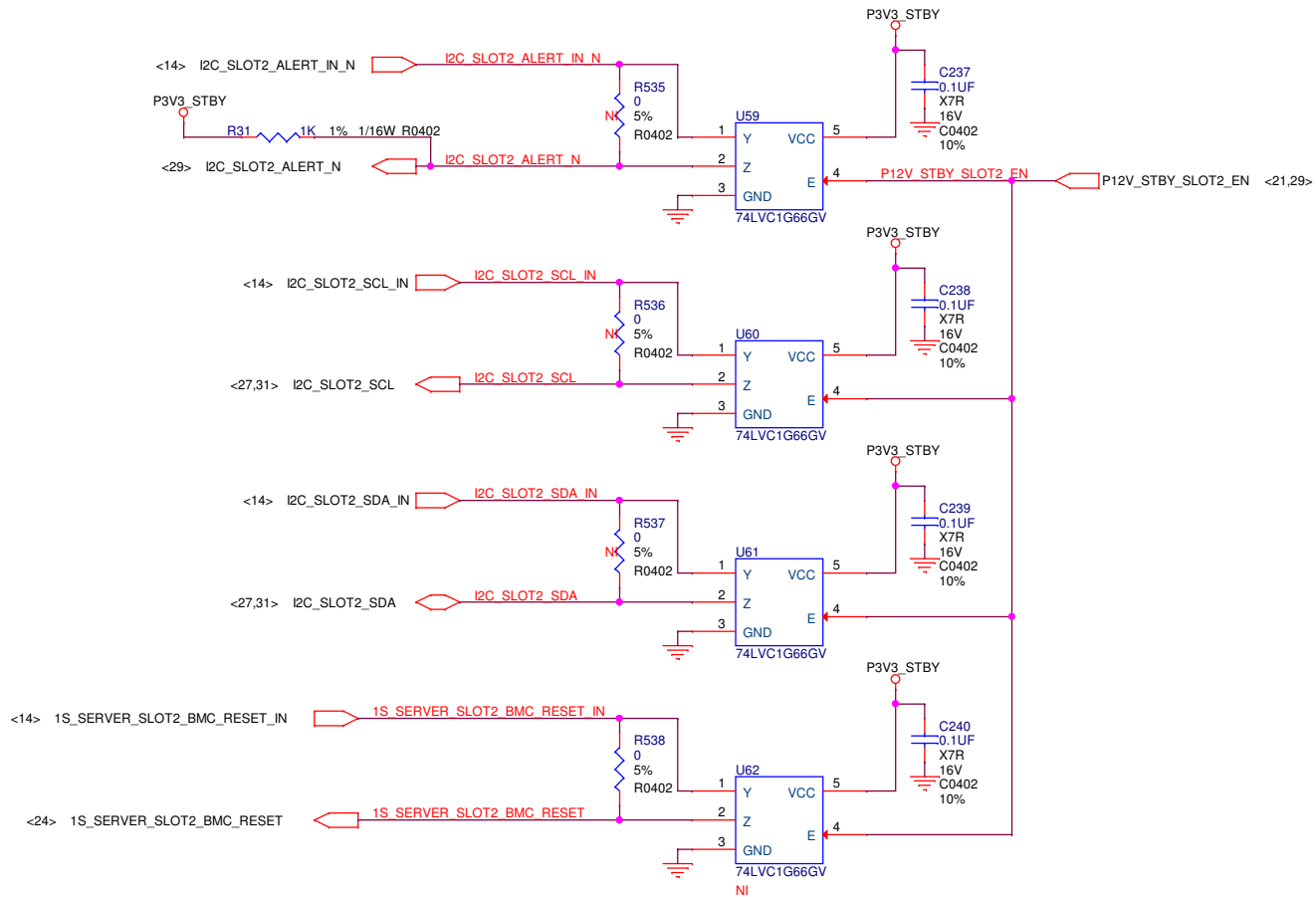
Slot1 Bilateral switch

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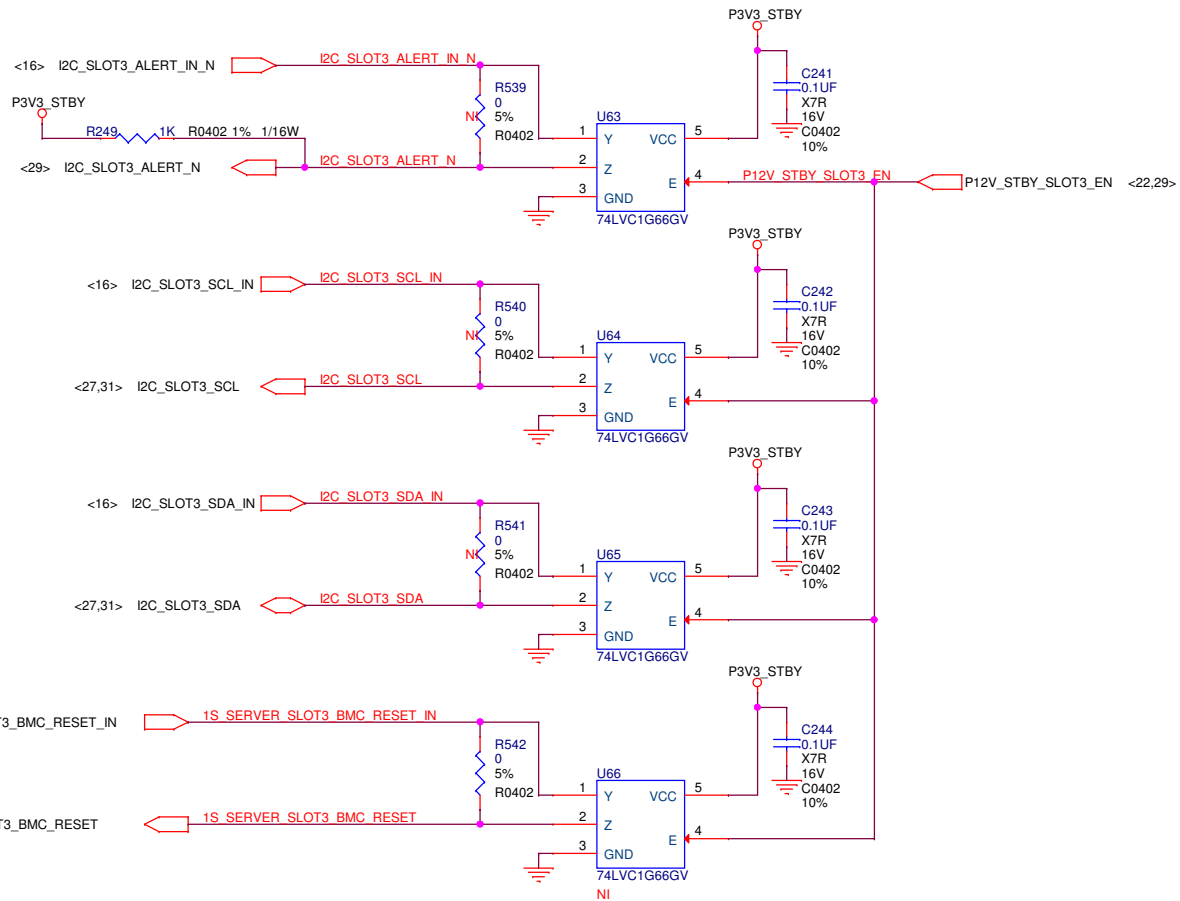
Slot2 x16 conn - Primary

CONN164_AAA-PCF166-R33

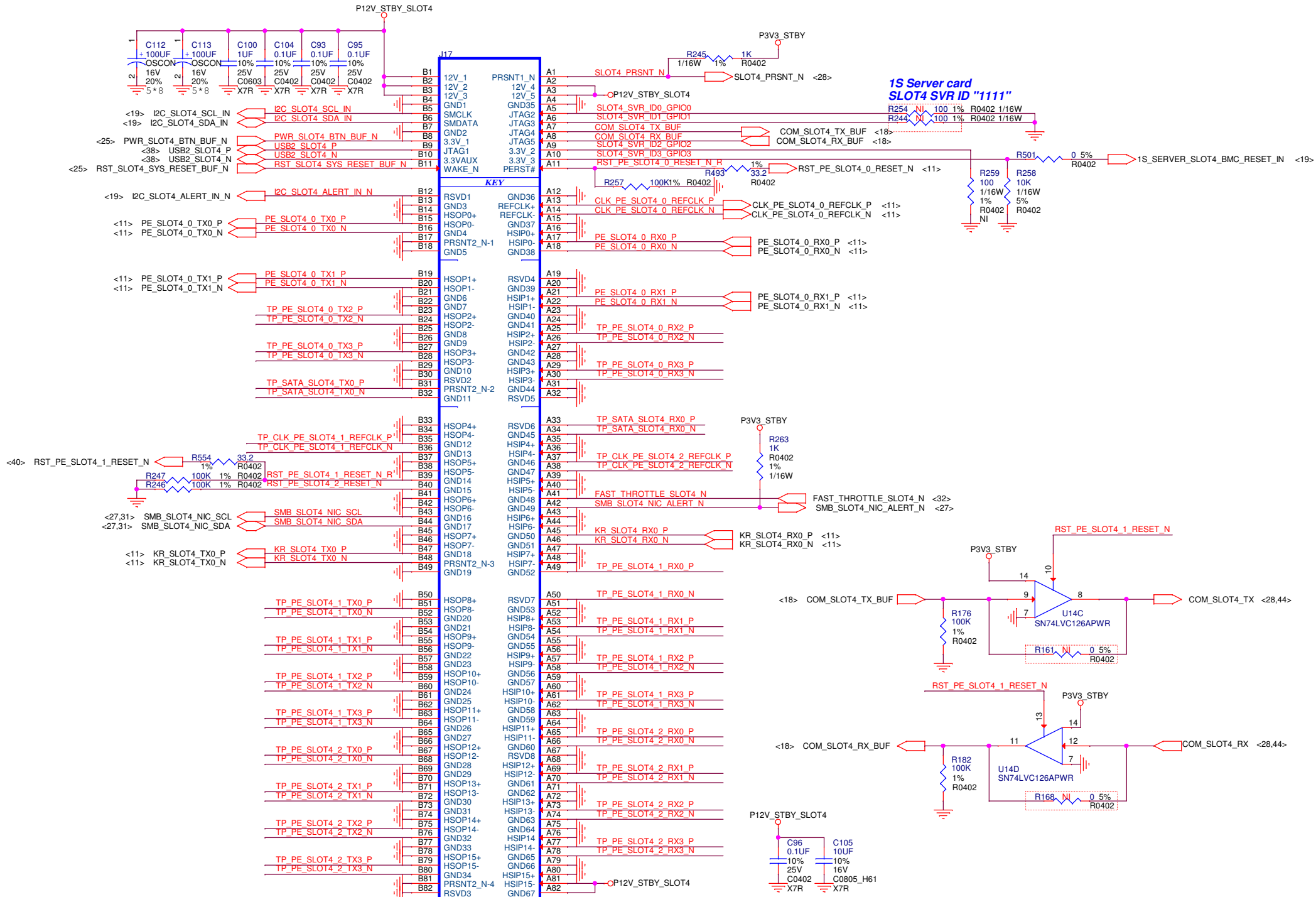


Slot2 x16 conn - Extension

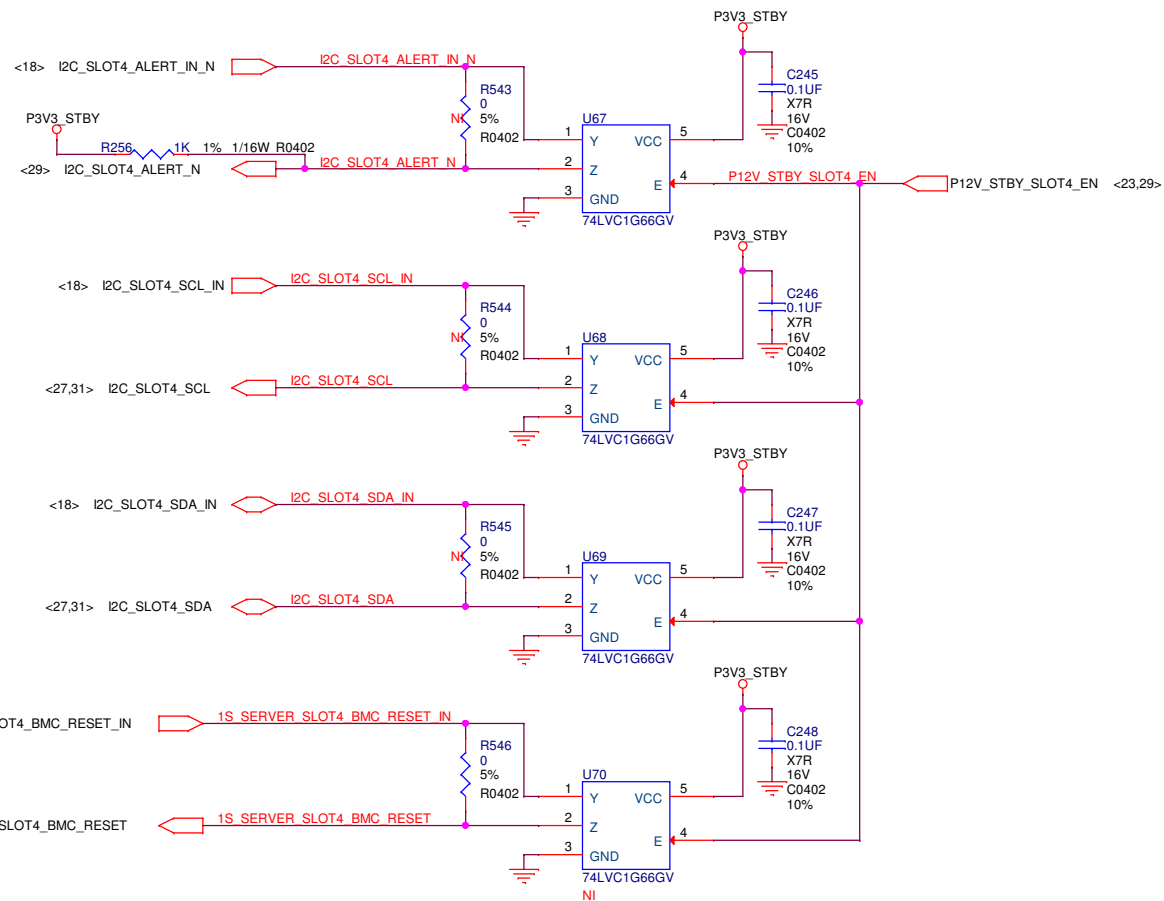
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Slot3 x16 conn - Extension

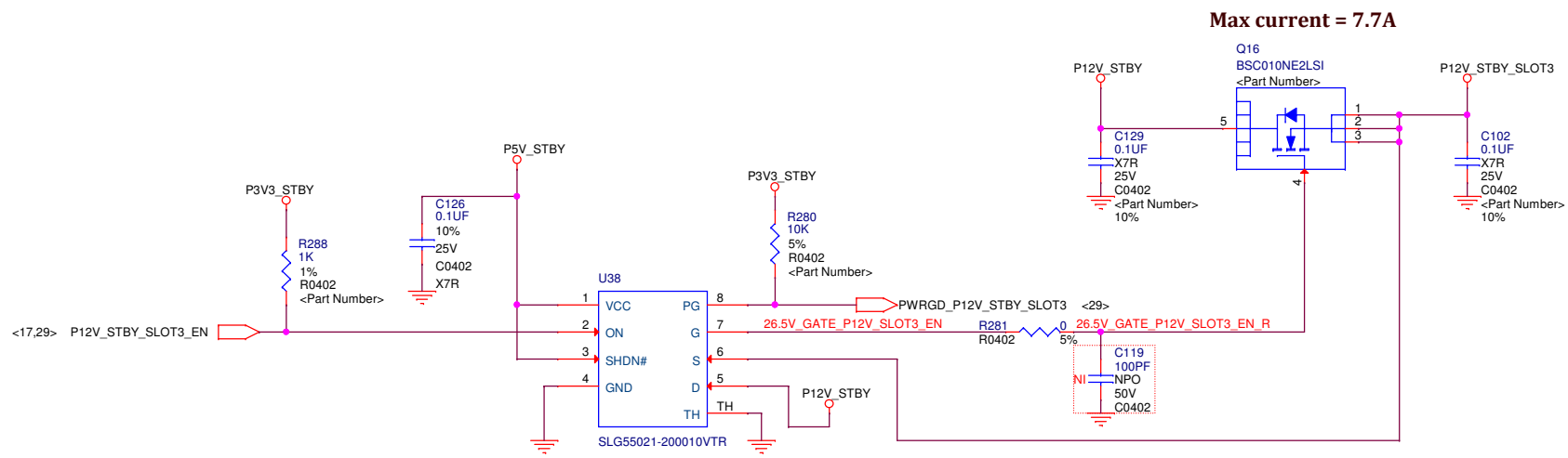


Slot4 x16 conn - Primary



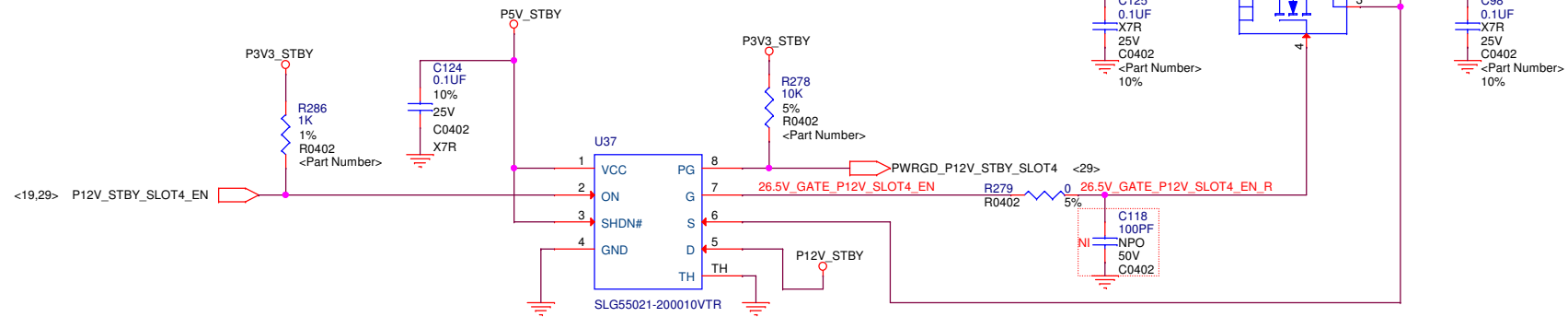
Slot4 x16 conn - Extension

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Slot3 Power Switch

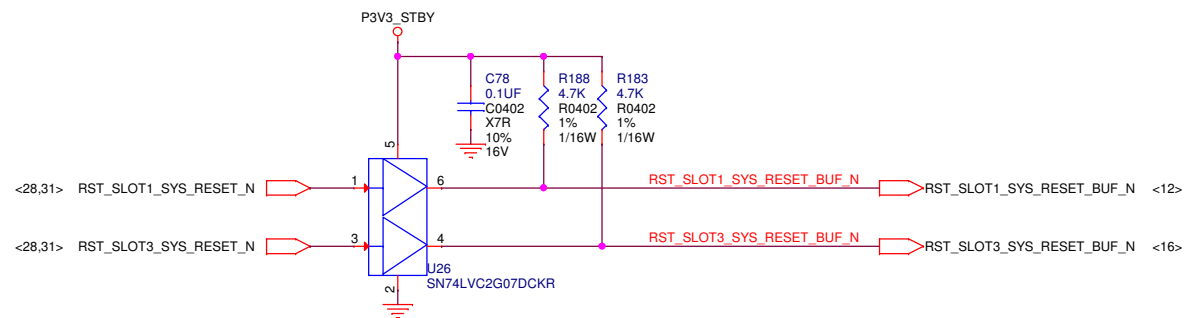
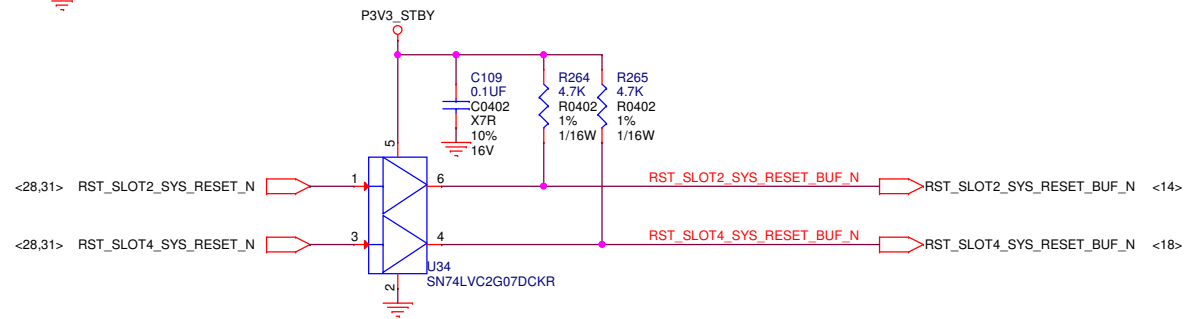
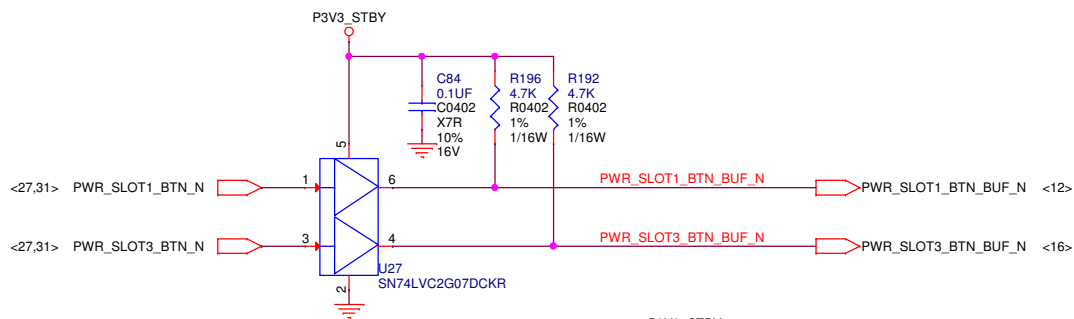
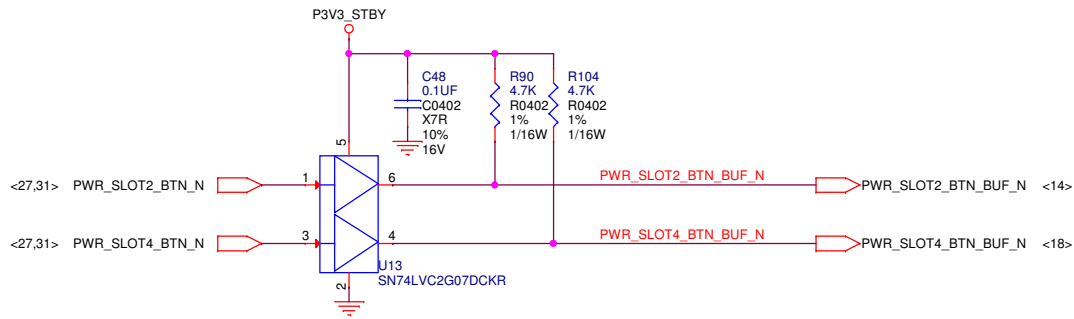
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Slot4 Power Switch

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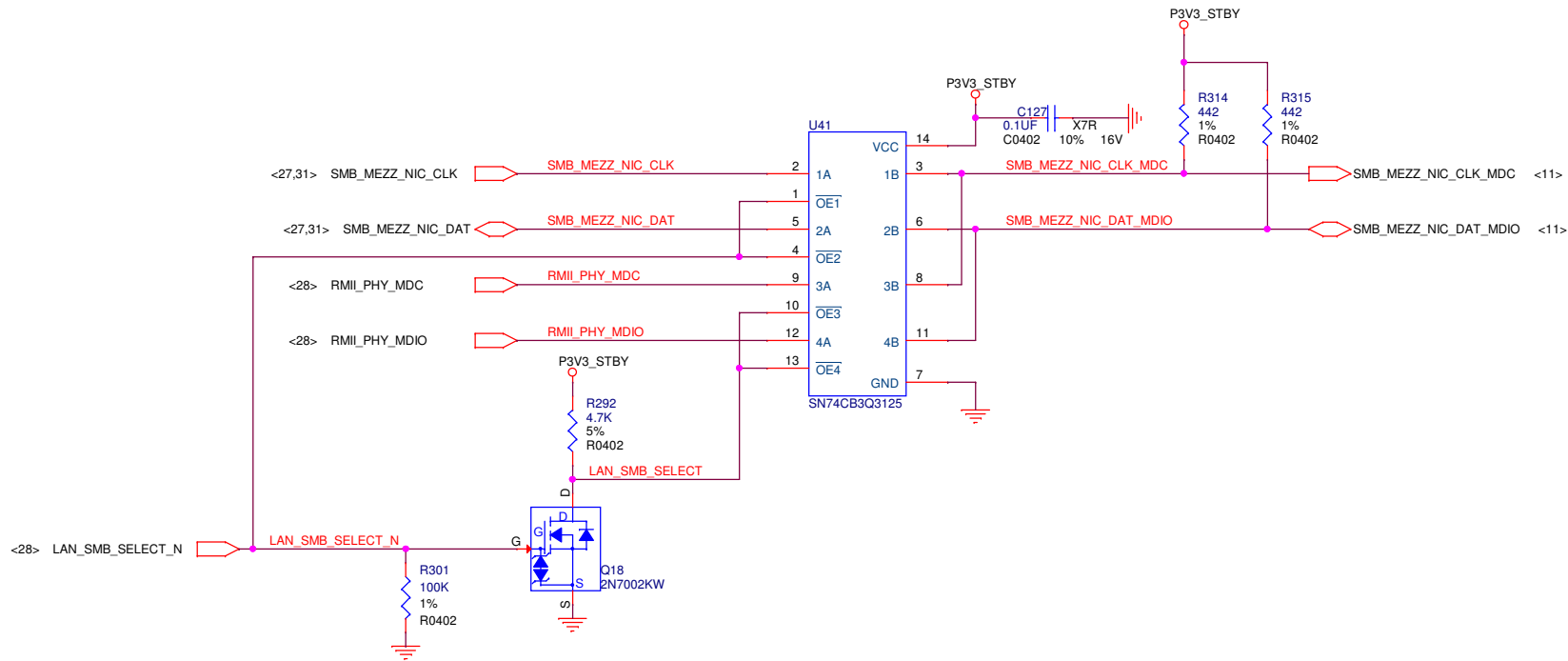




PWR/RST BTN BUFFER

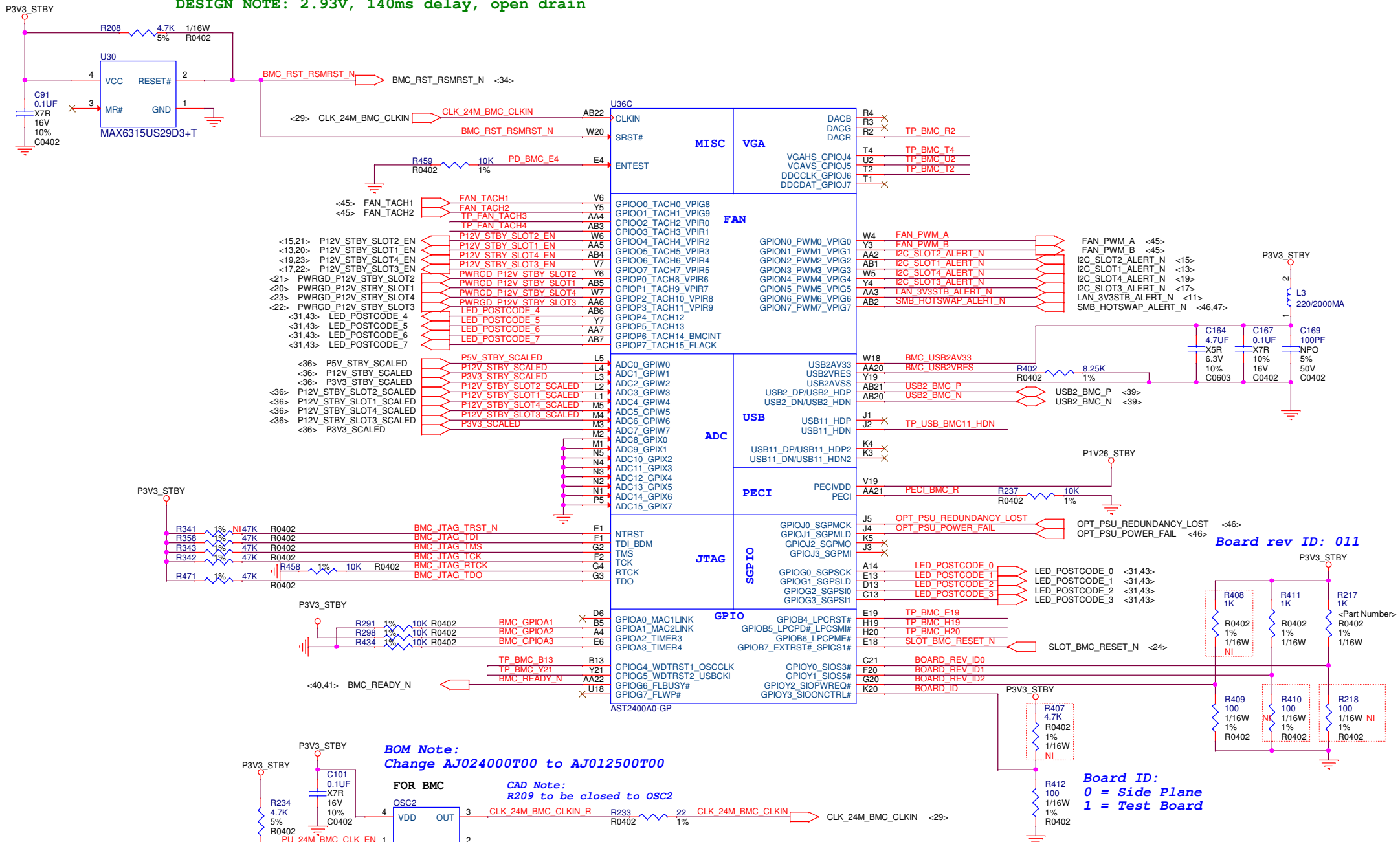
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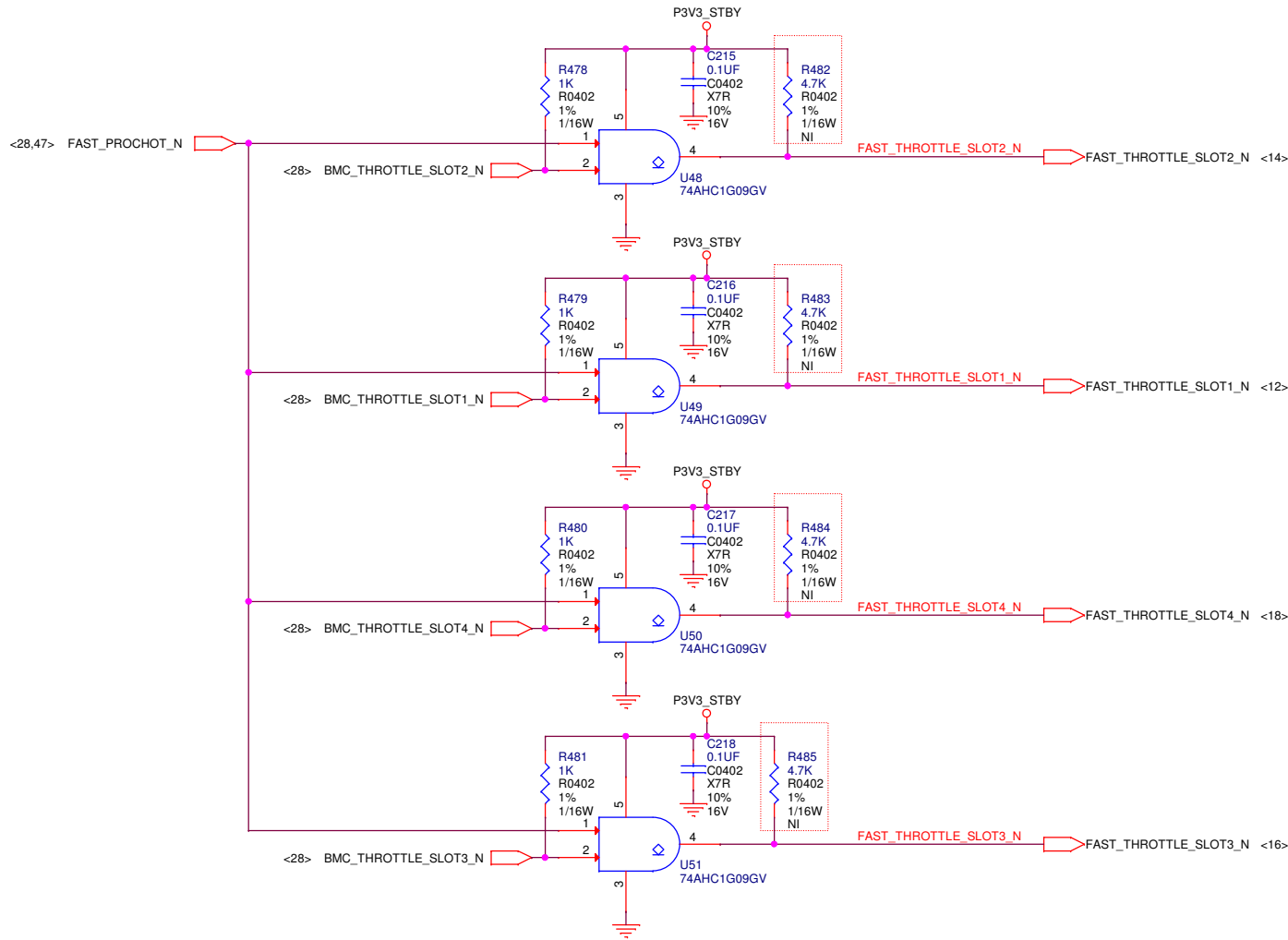


LAN_SMB_SELECT_N
 Low: select SMB_MEZZ_NIC_CLK/DAT (default)
 High: select RMII_PHY_MDC/MDIO

DESIGN NOTE: 2.93V, 140ms delay, open drain

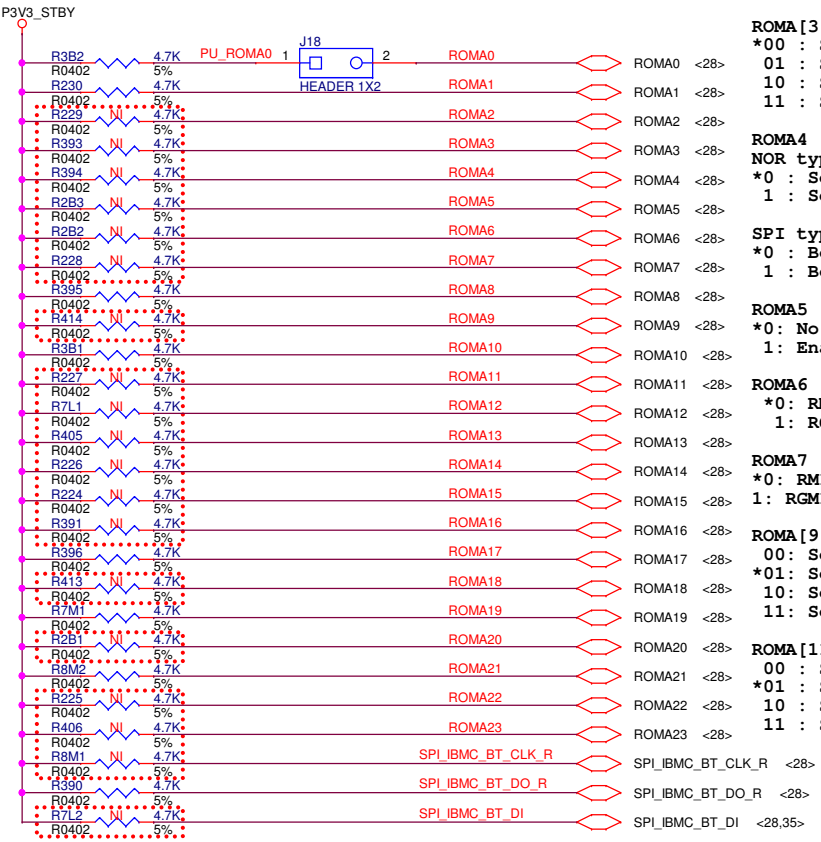


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FAST_THROTTLE_N

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ROMA[1:0] : ARM CPU boot code selection
00 : Boot from NOR flash memory
01 : Boot from NAND flash memory
*10 : Boot from SPI flash memory
11 : Disable ARM CPU operation

ROMA[3:2] : VGA memory size selection
*00 : Select 8 MB VGA memory
01 : Select 16 MB VGA memory
10 : Select 32 MB VGA memory
11 : Select 64 MB VGA memory

ROMA4 : Boot flash memory extended option
NOR type flash: data bus width selection
*0 : Select 8 bits interface
1 : Select 16 bits interface

SPI type flash: boot address mode selection
*0 : Boot with 24 bits address mode
1 : Boot with 32 bits address mode

ROMA5 : Enable VGA BIOS ROM
*0 : No VGA BISO ROM (for on-board applications)
1 : Enable VGA BIOS ROM (for add-on card applications)

ROMA6 : Define MAC#1 interface
*0: RMII/NCSI
1: RGMII

ROMA7 : Define MAC#2 interface
*0: RMII/NCSI
1: RGMII

ROMA[9:8] : H-PLL default clock frequency selection
00: Select 384 MHz
*01: Select 360 MHz
10: Select 336 MHz
11: Select 204 MHz

ROMA[11:10] : CPU/AHB clock frequency ratio selection
00 : Select CPU:AHB = 1:1
*01 : Select CPU:AHB = 2:1
10 : Select CPU:AHB = 4:1
11 : Select CPU:AHB = 3:1

ROMA[13:12] : SPI mode selection
*00 : Disable SPI interface
01 : Enable SPI Master
10 : Enable SPI Master and SPI Slave to AHB Bridge
11 : Enable SPI Bypass

ROMA14 : Enable LPC dedicated reset pin function
*0 : LPC reset is shared with PCI reset pin
1 : LPC reset is located at pin number E19, shared with GPIOB4.

ROMA15 : VGA Class Code selection
*0 : Select the Class Code for video device
1 : Select the Class Code for VGA device

ROMA16 : SuperIO configuration address selection
*0 : Decode 0x2E
1 : Decode 0x4E

ROMA17 : Enable BMC 2nd boot watchdog timer
0 : Disable
*1 : Enable BMC 2nd boot watchdog timer start counting at power up.

ROMA23,ROMA18 : Clock source selection
*00 : 24MHz
01: 48MHz
10 : 25MHz USBCKI = 24MHz
11: 25MHz USBCKI = 48MHz

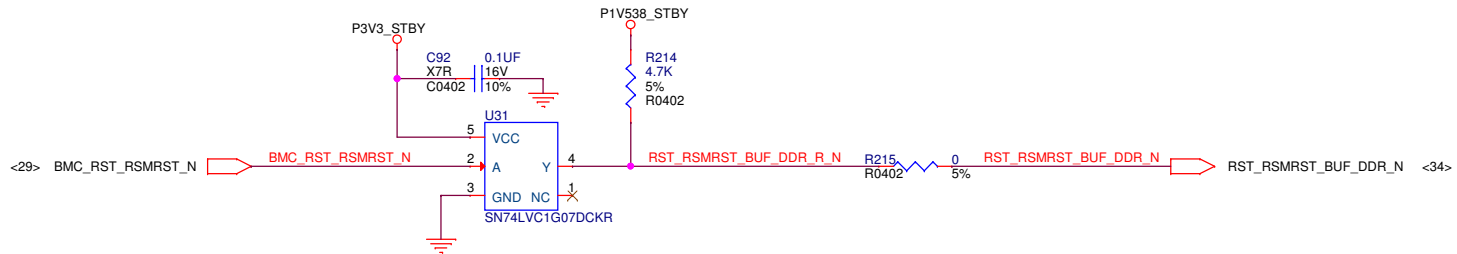
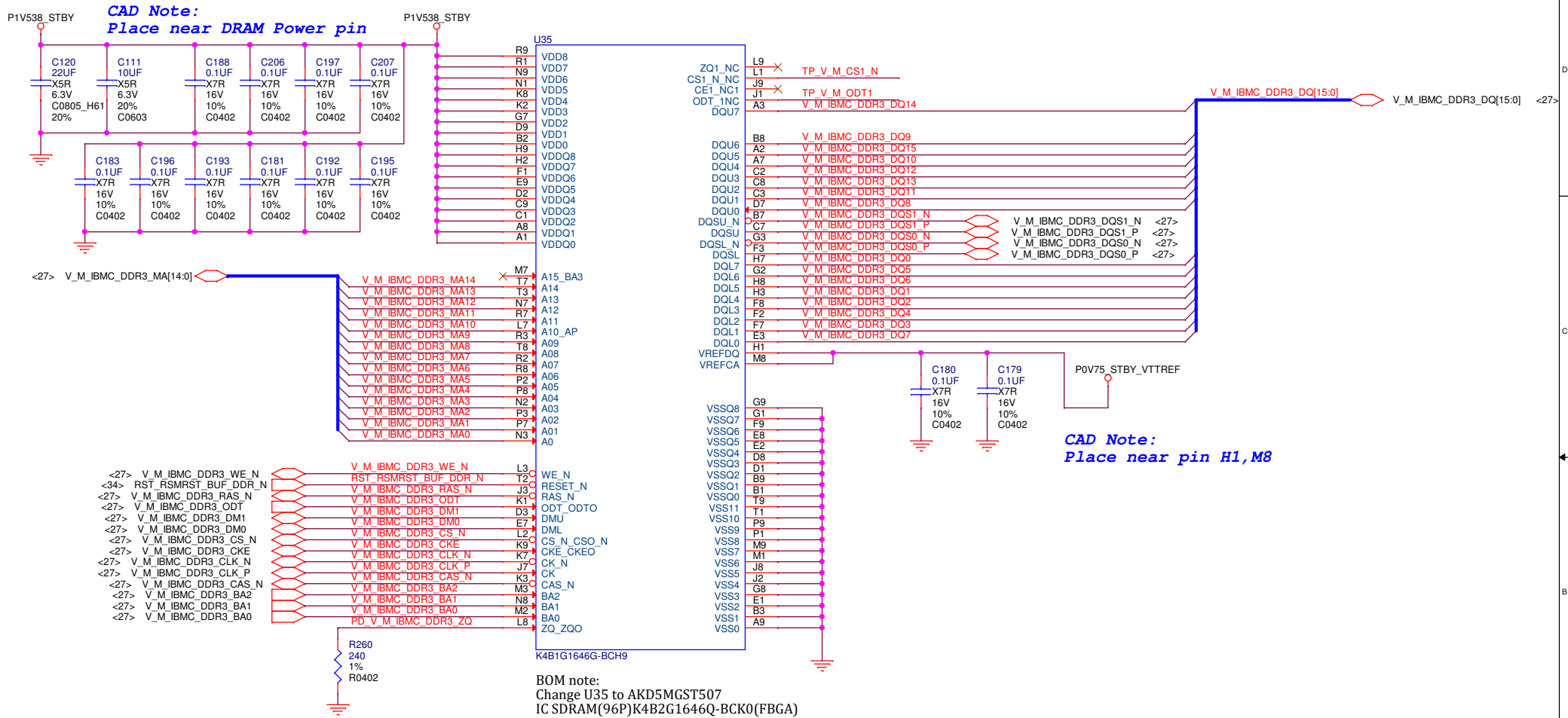
ROMA19 : Disable MSI controller
0 : Enable
*1 : Disable

ROMA20 : DISABLE LPC TO DECODE SUPERIO 0X2E / 0X4E ADDRESS
*0 : Disable, normal reset sequence
1 : Enable

ROMA21 : Enable GPIOD pass-through mode
0 : Disable, pass through can be enabled by SCU8C[11:8].
*1: Enable pass-through at power on.

ROMA22 : Enable GPIOE pass-through mode
*0: Disable, pass through can be enabled by SCU8C[15:12]
1: Enable pass-through at power on.

ROMD[2:0]
DRAM configuration setting
000: DDR3 SDRAM with CL= 5, CWL = 5
*010: DDR3 SDRAM with CL = 6, CWL = 5
100: DDR3 SDRAM with CL = 7, CWL = 6
110: DDR3 SDRAM with CL = 8, CWL = 6
001: DDR2 SDRAM with CL = 4
011: DDR2 SDRAM with CL = 5
101: DDR2 SDRAM with CL = 6
111: DDR2 SDRAM with CL = 7

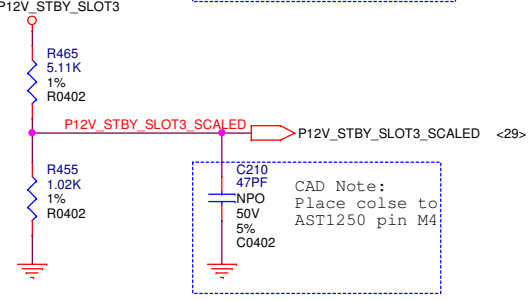
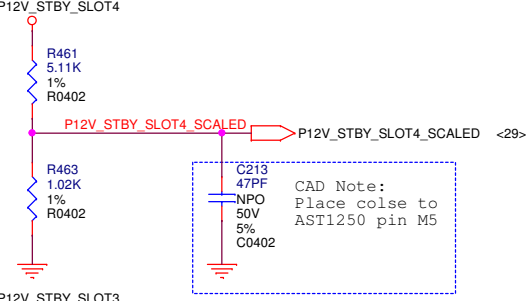
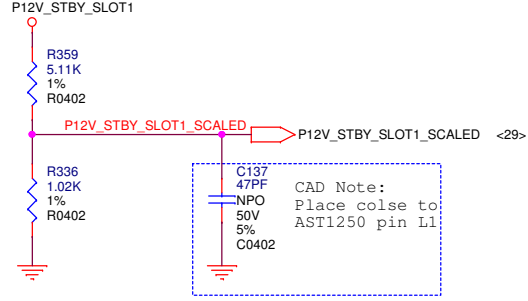
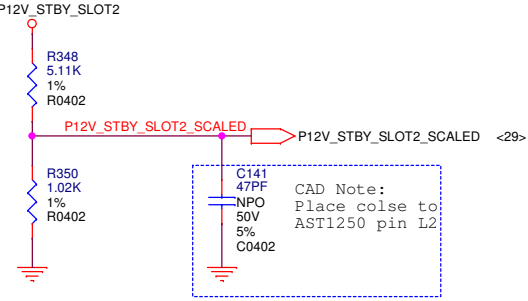
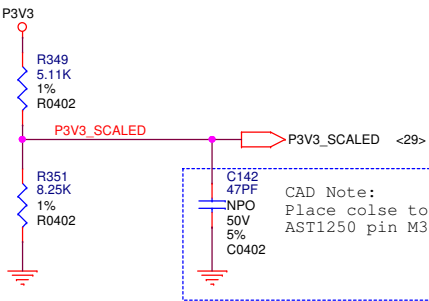
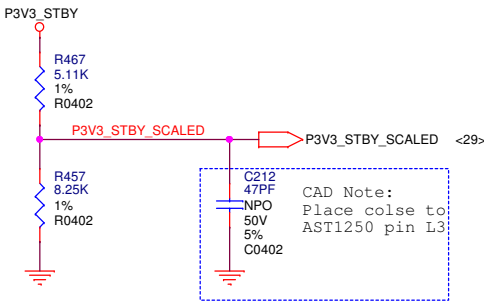
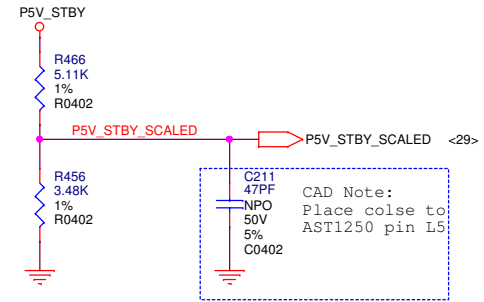
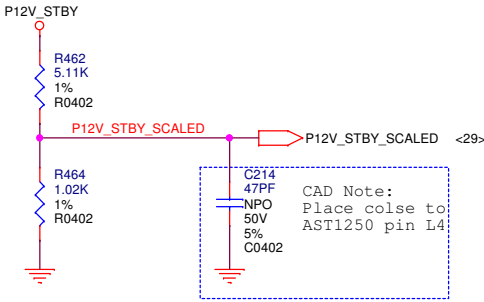


BMC DDRIII SDRAM

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ROUTE ALL ADC NETS AT 6 MILLS WIDE



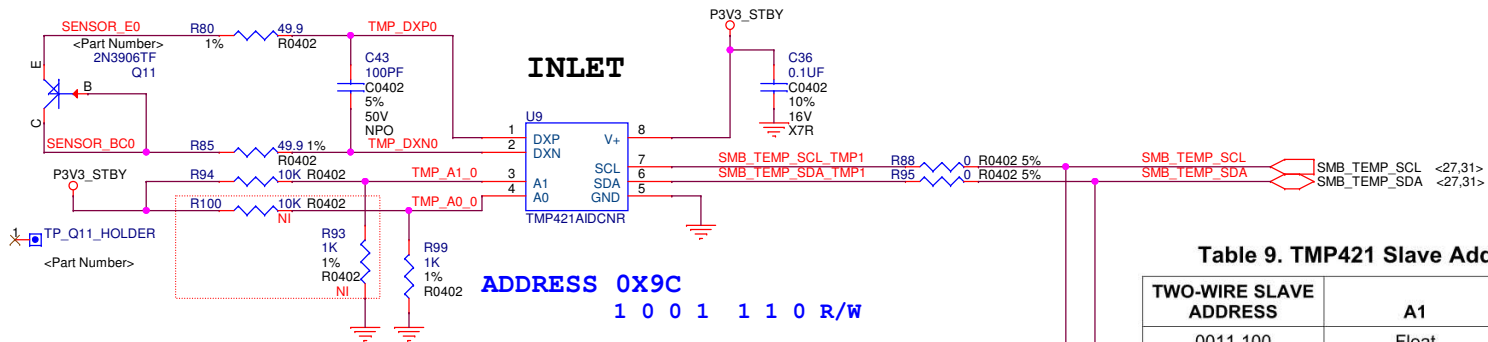


Table 9. TMP421 Slave Address Options

TWO-WIRE SLAVE ADDRESS	A1	A0
0011 100	Float	0
0011 101	Float	1
0011 110	0	Float
0011 111	1	Float
0101 010	Float	Float
1001 100	0	0
1001 101	0	1
1001 110	1	0
1001 111	1	1

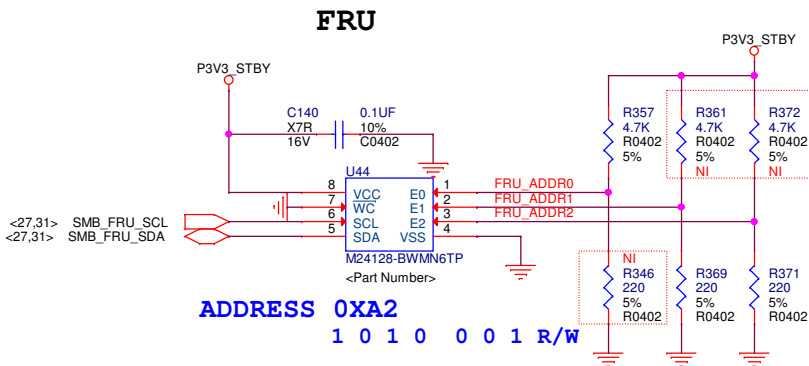
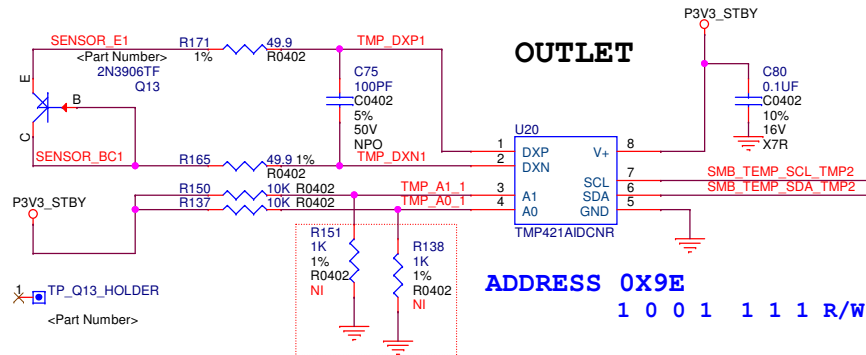


Table 2. Device Select Code

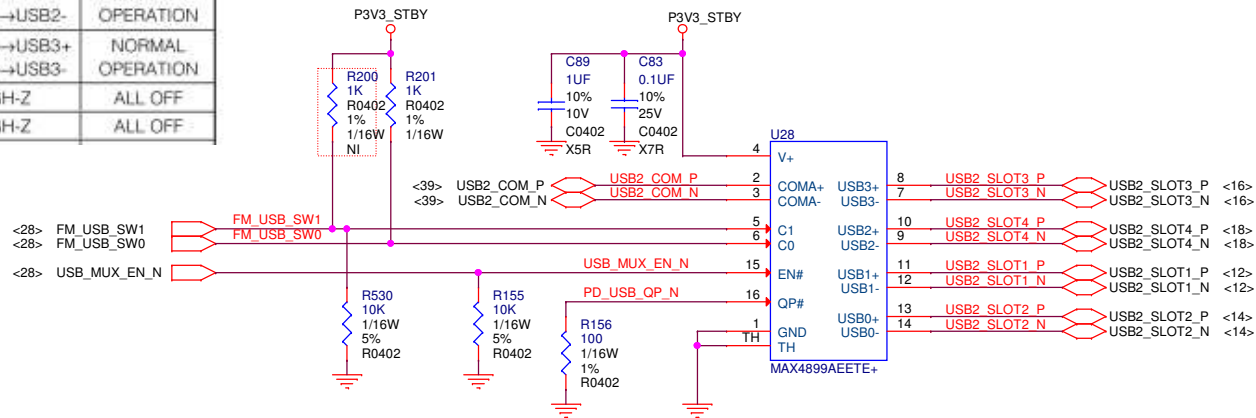
	Device Type Identifier ¹				Chip Enable Address ²			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select Code	1	0	1	0	E2	E1	E0	RW

Note: 1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.

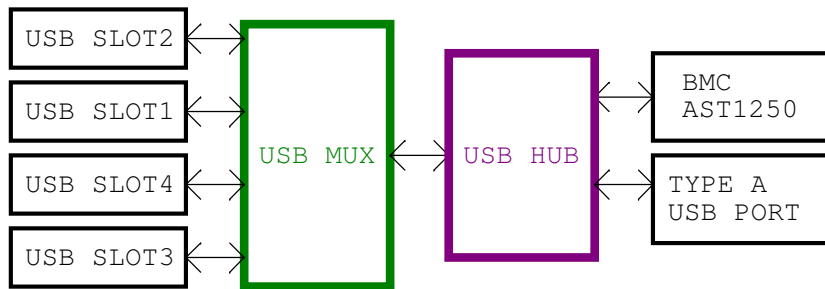
FRU address

TEMP SENSOR / FRU

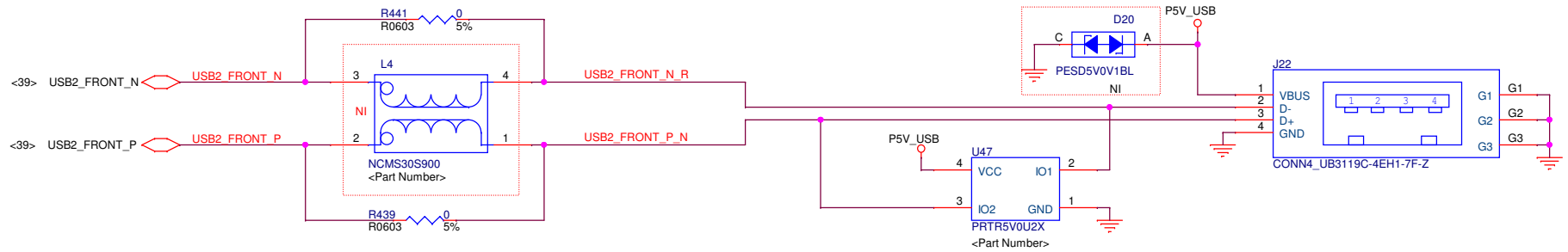
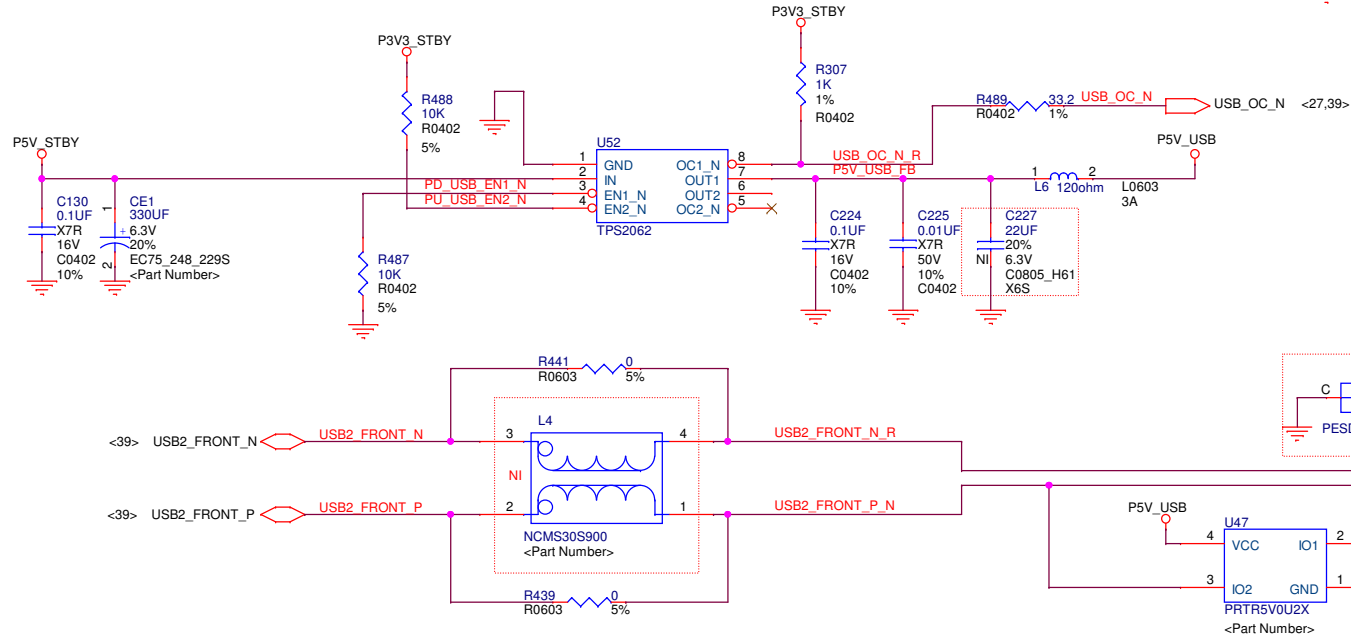
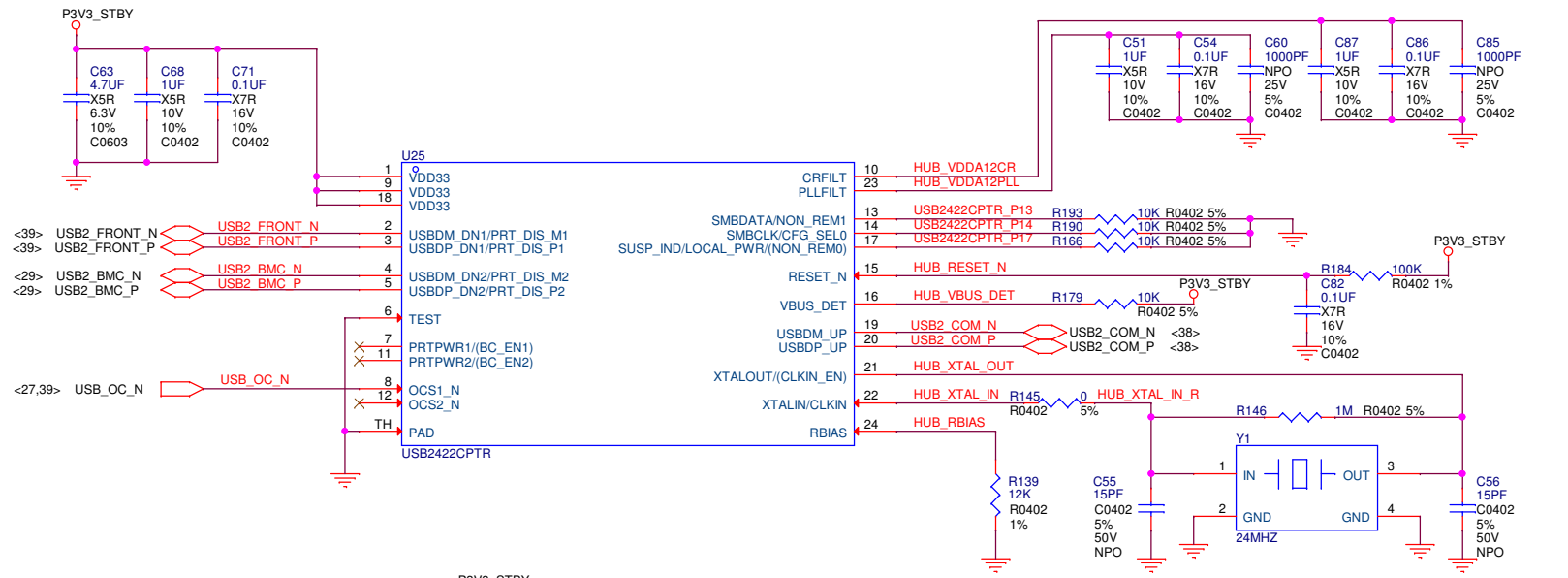
MAX4899AE					
QP	EN	C1	C0	FUNCTION	COMMENT
0	0	0	0	COMA+ →USB0+ COMA- →USB0-	NORMAL OPERATION
0	0	0	1	COMA+ →USB1+ COMA- →USB1-	NORMAL OPERATION
0	0	1	0	COMA+ →USB2+ COMA- →USB2-	NORMAL OPERATION
0	0	1	1	COMA+ →USB3+ COMA- →USB3-	NORMAL OPERATION
0	1	X	X	HIGH-Z	ALL OFF
1	1	X	X	HIGH-Z	ALL OFF



DESIGN NOTE:

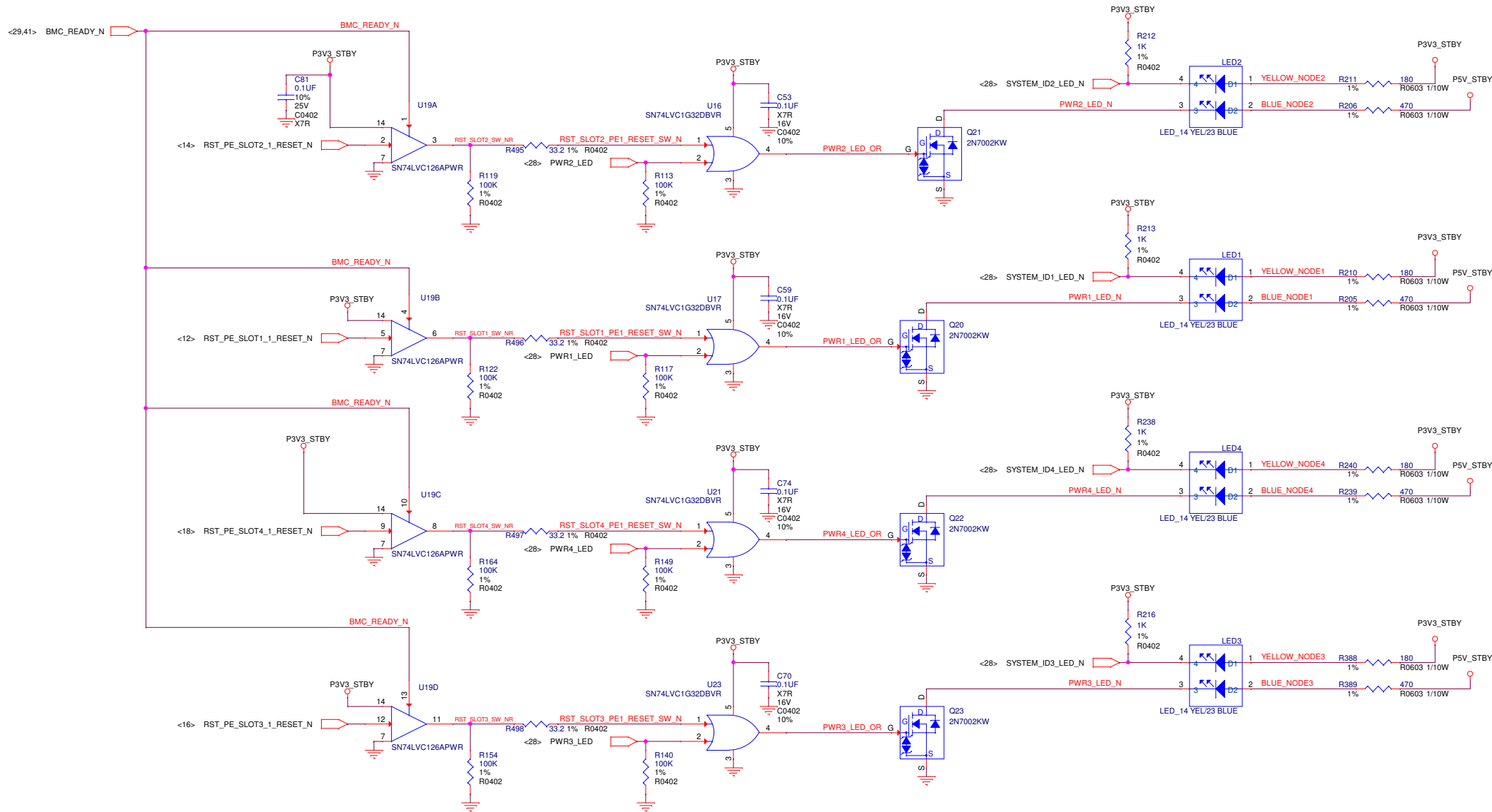


USB MUX



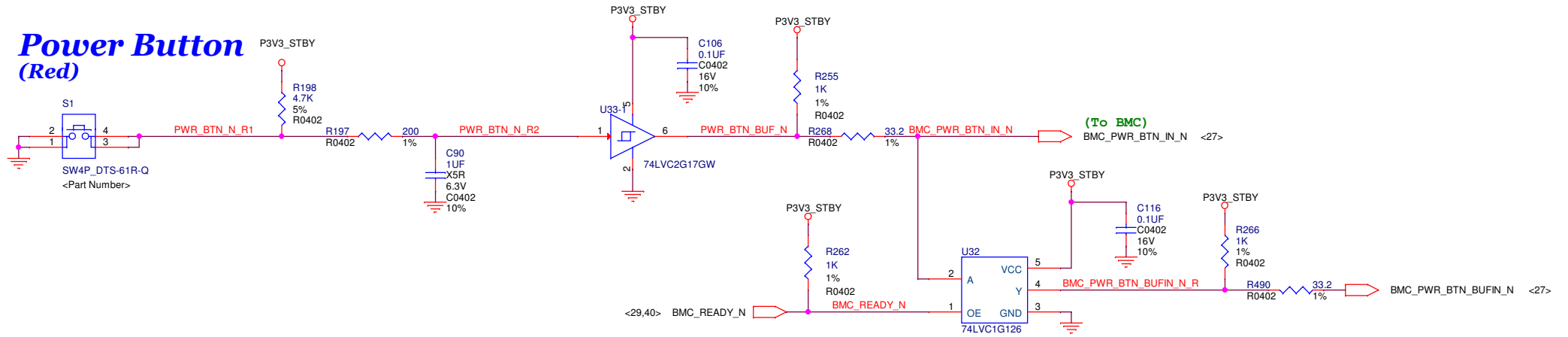
USB HUB

<div> <div>Quanta</div> <div>CCBU</div> </div>	Department	Designer	Project	Doc Number	Rev
	CCBU	<Designer>	F20 Side Plane fab4	<Doc>	V17
	Reviewer	<Reviewer>	Size B	Page Title	Sheet
			Date: Tuesday, January 16, 2018	USB HUB	39 of 53

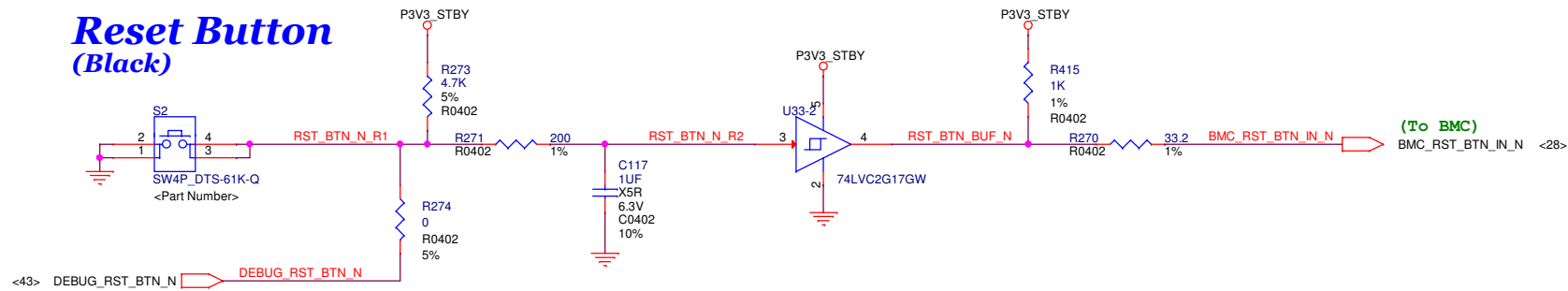


POWER	System Identify	Status	
off	off	X	LED consistently off
off	on	Good	LED blue for 0.1sec, off for 0.9sec, and loop
on	off	Good	LED consistently blue
on	on	Good	LED blue for 0.9sec, off for 0.1sec, and loop
off	on	Bad	LED yellow for 0.1sec, off for 0.9sec, and loop
on	off	Bad	LED consistently yellow
on	on	Bad	LED yellow for 0.9sec, off for 0.1sec, and loop

Power Button (Red)



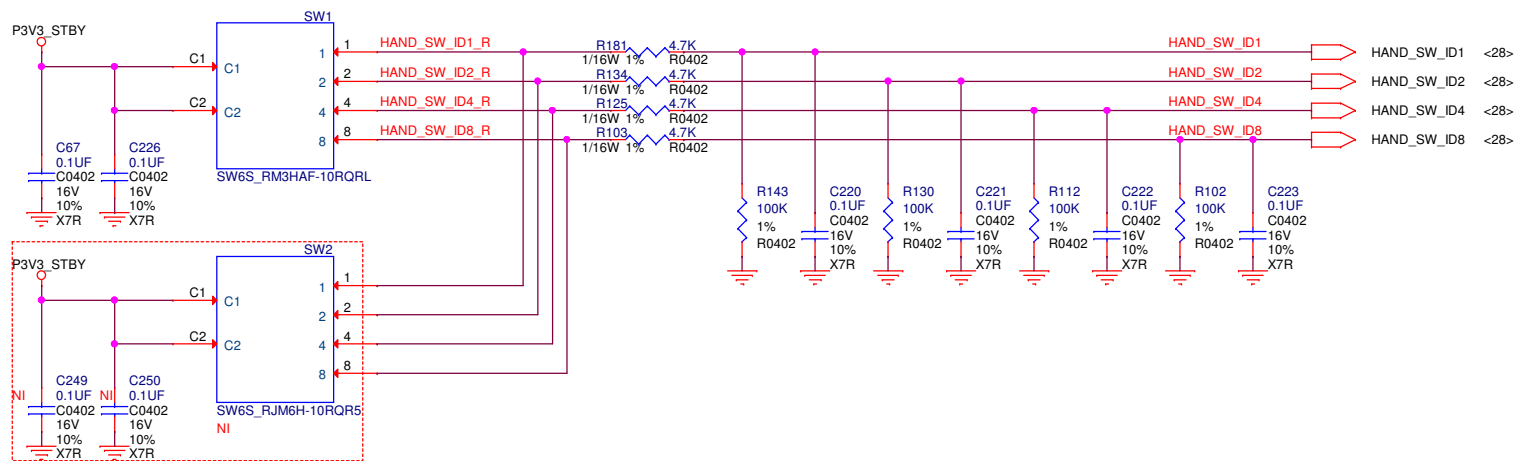
Reset Button (Black)



PWR/RST BUTTON

Quanta

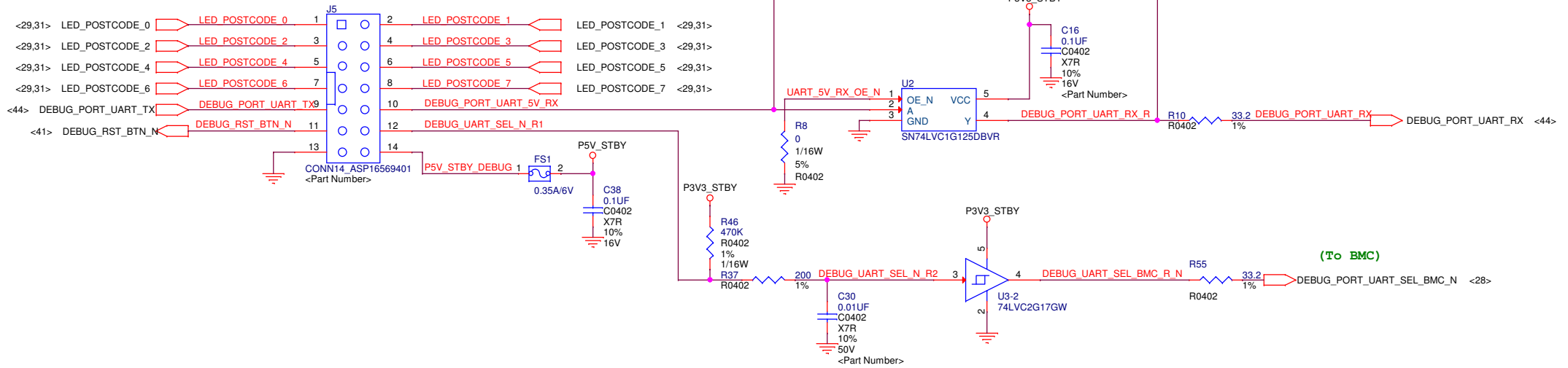
Department	CCBU	Designer	<Designer>	Project	F20 Side Plane fab4	Doc Number	<Doc>	Rev	
Reviewer	<Reviewer>			Size B	Date: Tuesday, January 16, 2018	Page Title	PWR/RST/SELECT BUTTON	Sheet 41	of 53



HAND_SW_ID8	HAND_SW_ID4	HAND_SW_ID2	HAND_SW_ID1	Position	
L	L	L	L	1	1S SERVER SLOT1 SELECT (DEFAULT)
L	L	L	H	2	1S SERVER SLOT2 SELECT
L	L	H	L	3	1S SERVER SLOT3 SELECT
L	L	H	H	4	1S SERVER SLOT4 SELECT
L	H	L	L	5	BMC DEBUG PORT SELECT
L	H	L	H	6	1S SERVER SLOT1 SELECT
L	H	H	L	7	1S SERVER SLOT2 SELECT
L	H	H	H	8	1S SERVER SLOT3 SELECT
H	L	L	L	9	1S SERVER SLOT4 SELECT
H	L	L	H	10	BMC DEBUG PORT SELECT

SELECT SWITCH

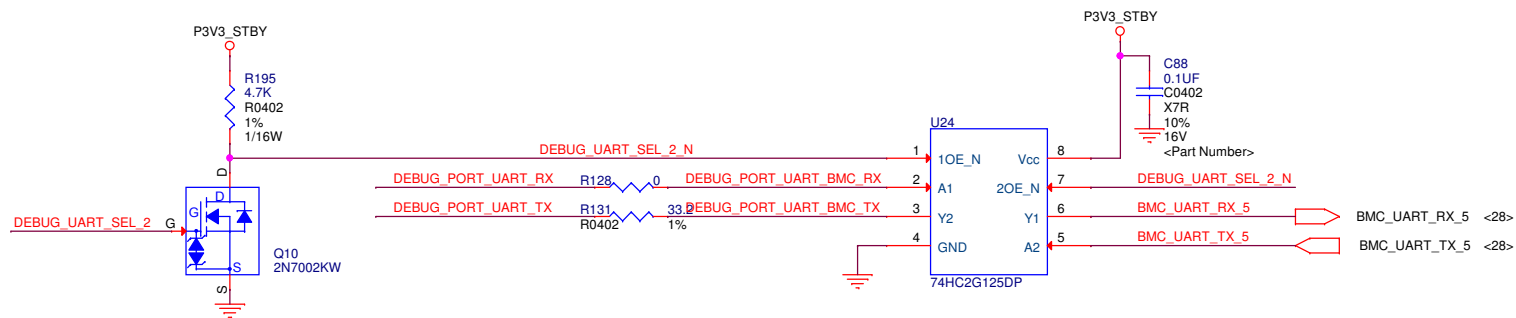
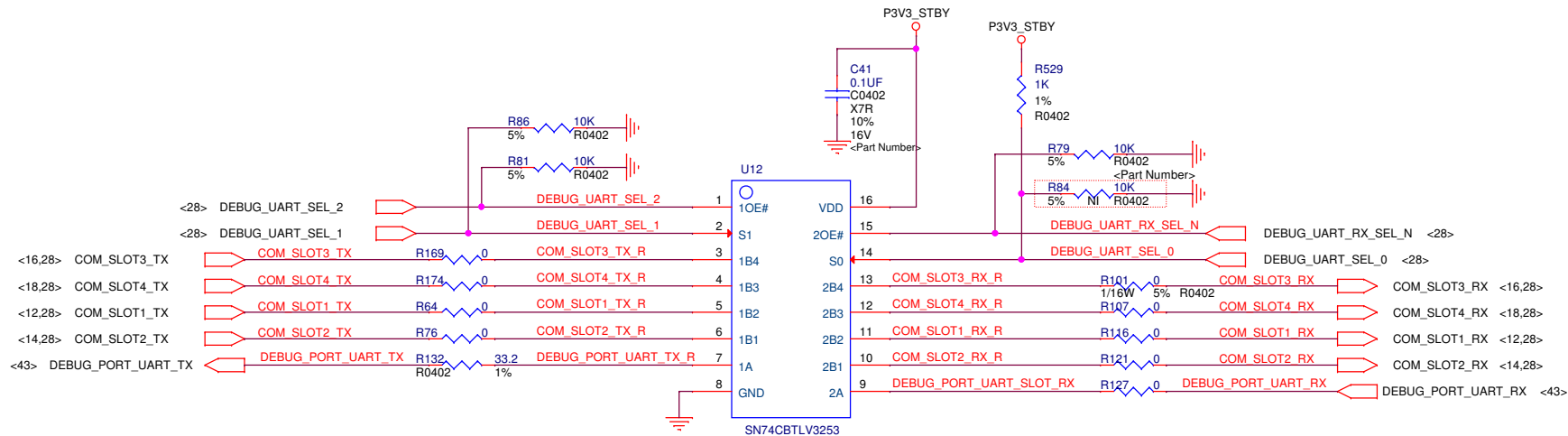
FB Debug Header



DEBUG

Quanta

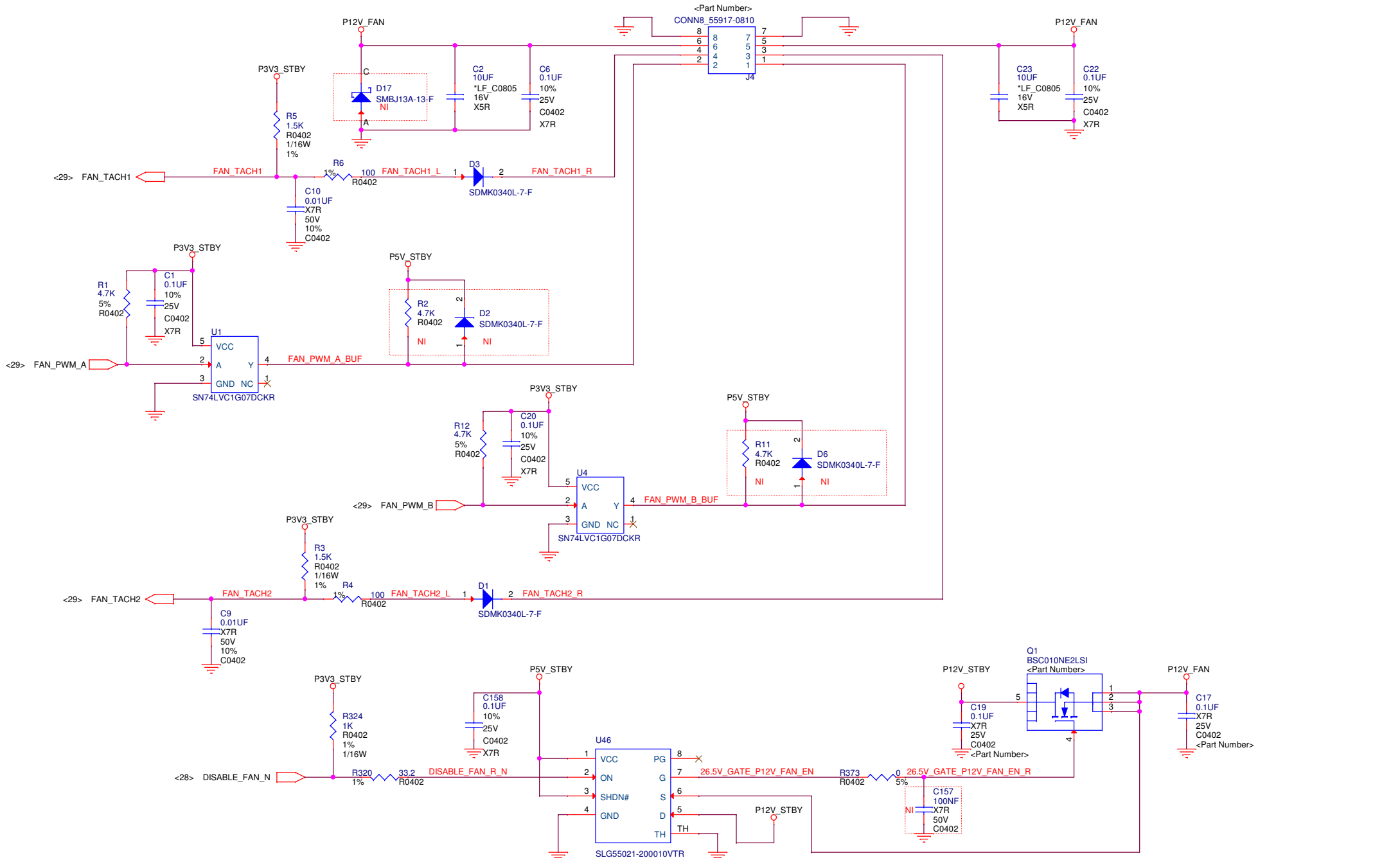
Department	CCBU	Designer	<Designer>	Project	F20 Side Plane fab4	Doc Number	<Doc>	Rev	V17
Reviewer	<Reviewer>	Size B	Date: Tuesday, January 16, 2018	Page Title	DEBUG	Sheet 43	of 53		

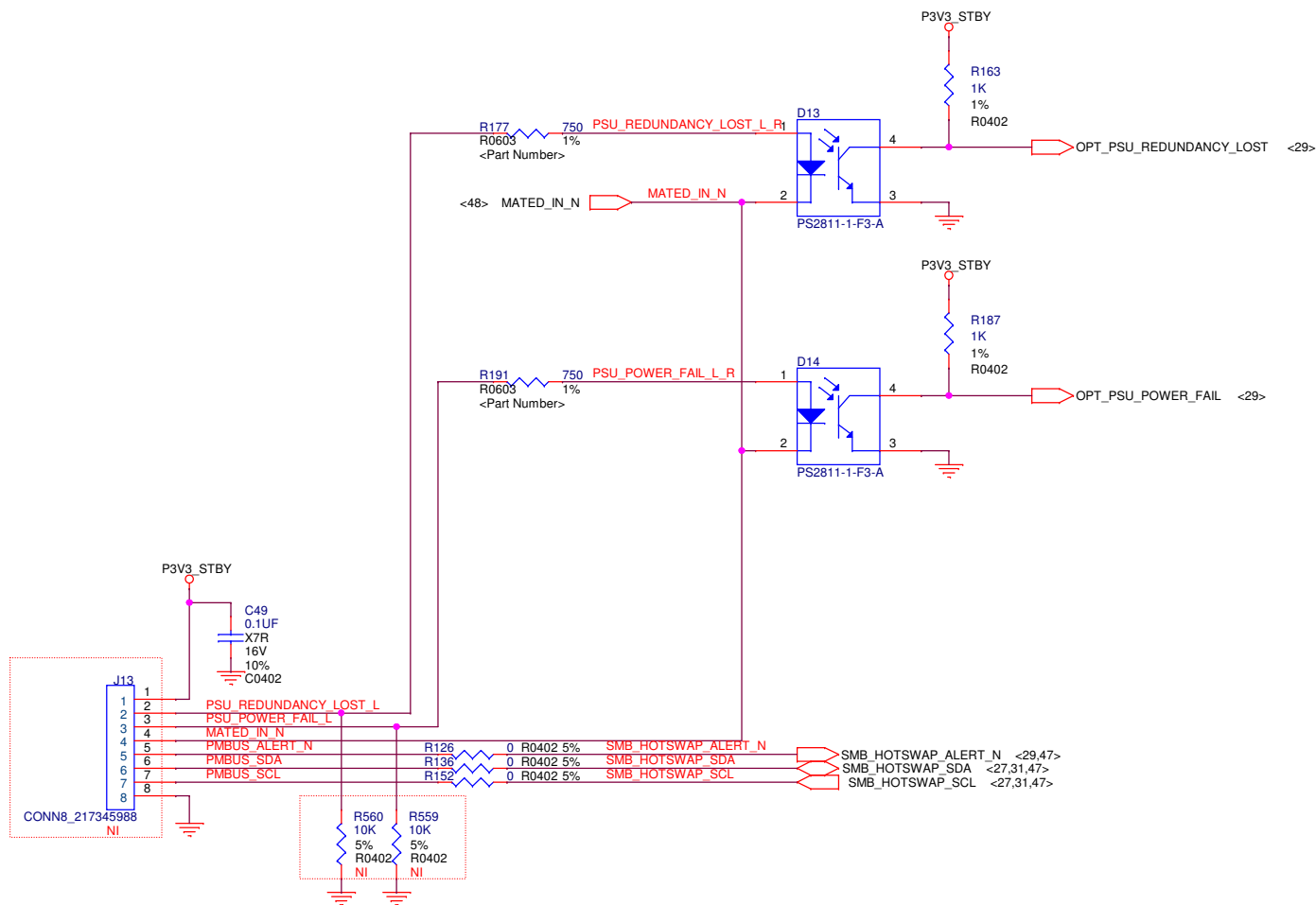


SEL_2	SEL_1	SEL_0	RX_SEL_N	
0	0	0	0	SLOT2
0	0	1	0	SLOT1
0	1	0	0	SLOT4
0	1	1	0	SLOT3
0	X	X	1	SLOT RX Disable
1	0	0	1	BMC Debug

UART select table

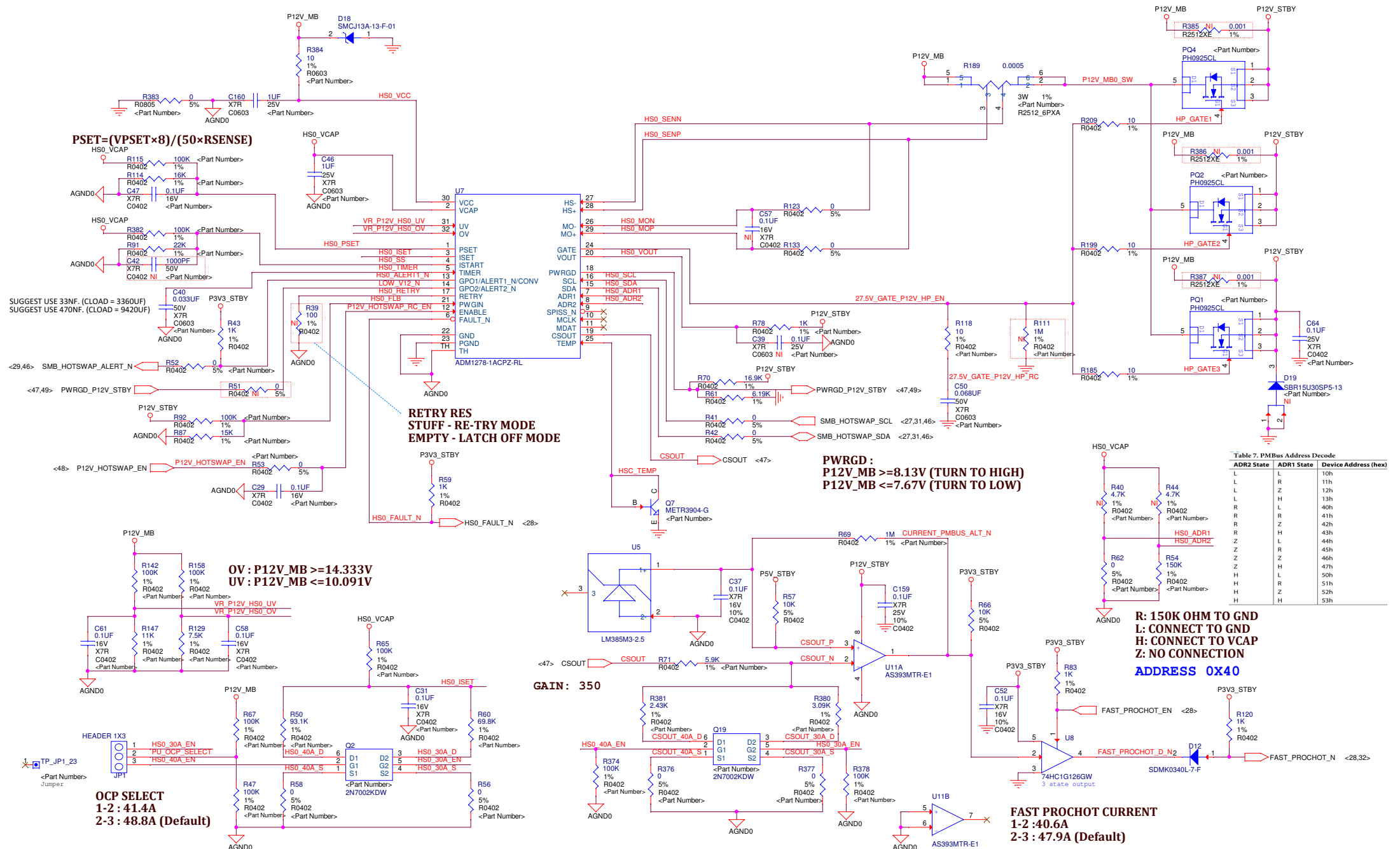
FAN CONN

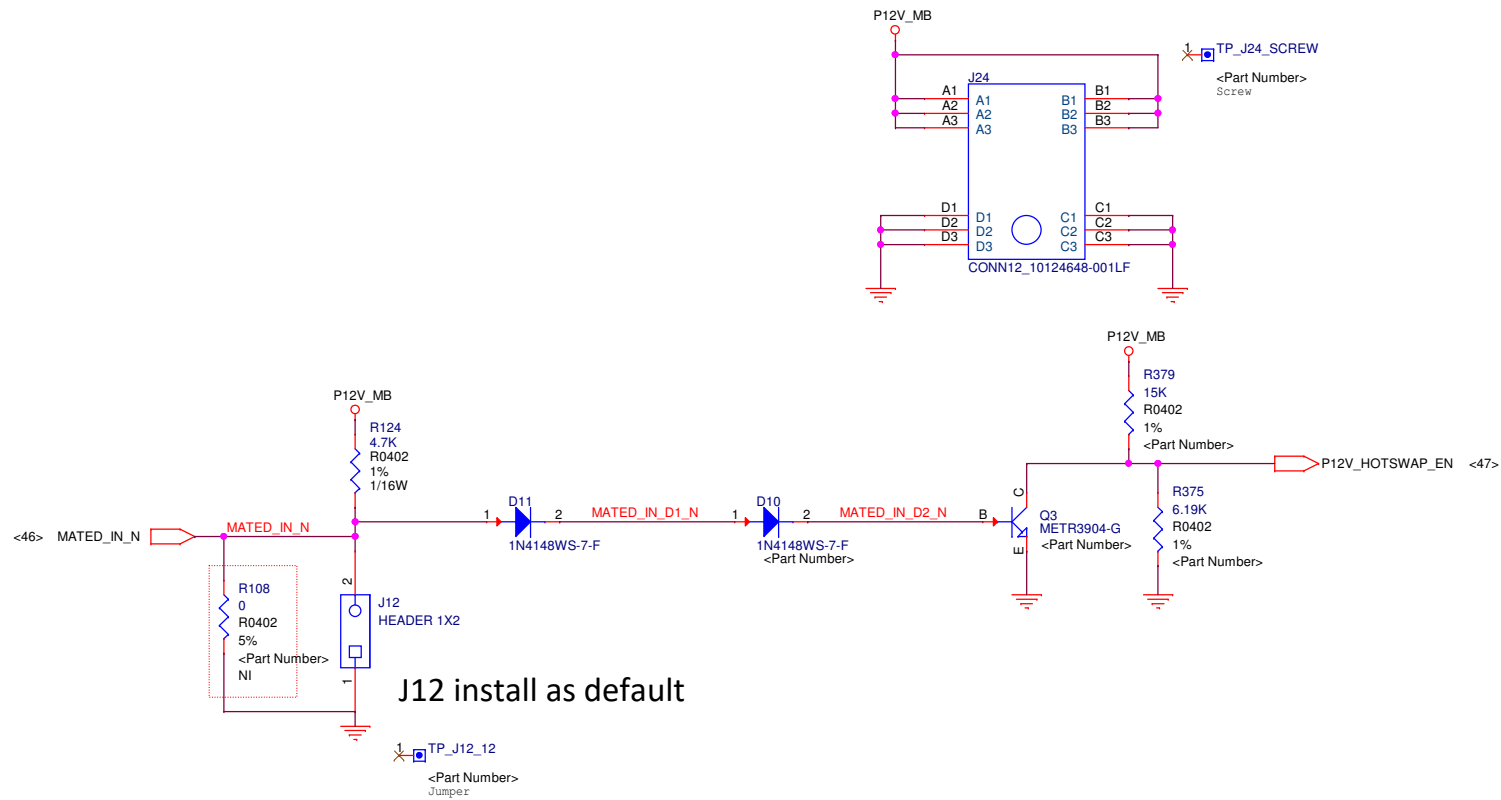




Power Side Band

HOT SWAP CONTROLLER



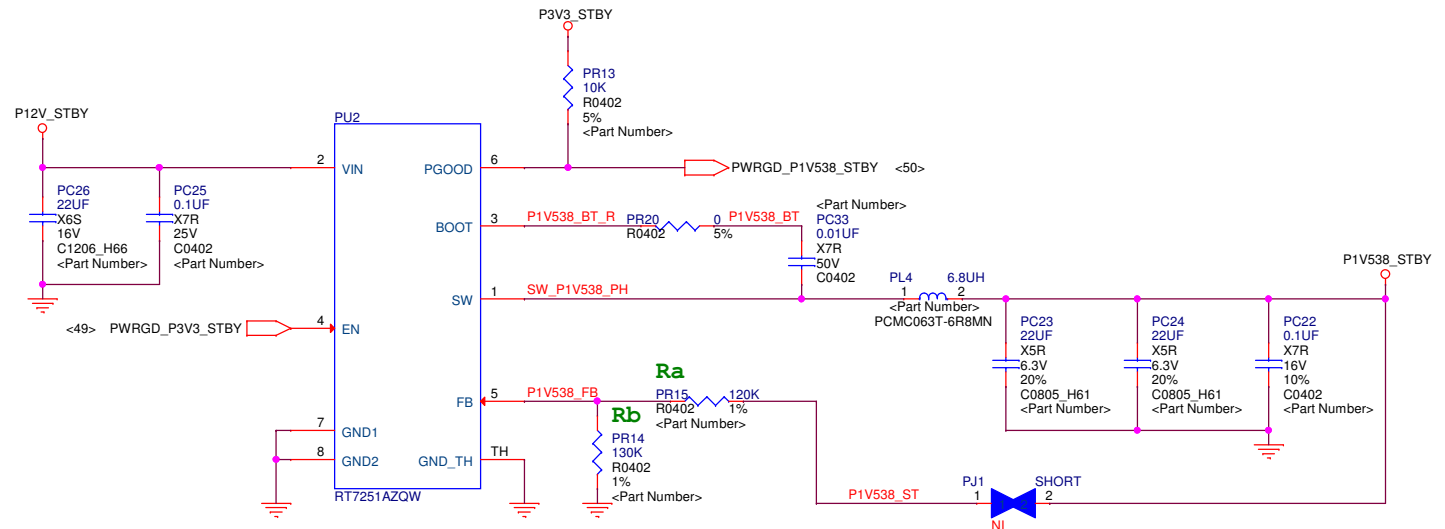


POWER CONN

<div> <div>Quanta</div> <div>CCBU</div> </div>	Department	Designer	Project	Doc Number	Rev
	CCBU	<Designer>	F20 Side Plane fab4	<Doc>	V17
	Reviewer	<Reviewer>	Size B	Page Title	Sheet 48 of 53
			Date: Tuesday, January 16, 2018	POWER CONN	

P1V538_STBY

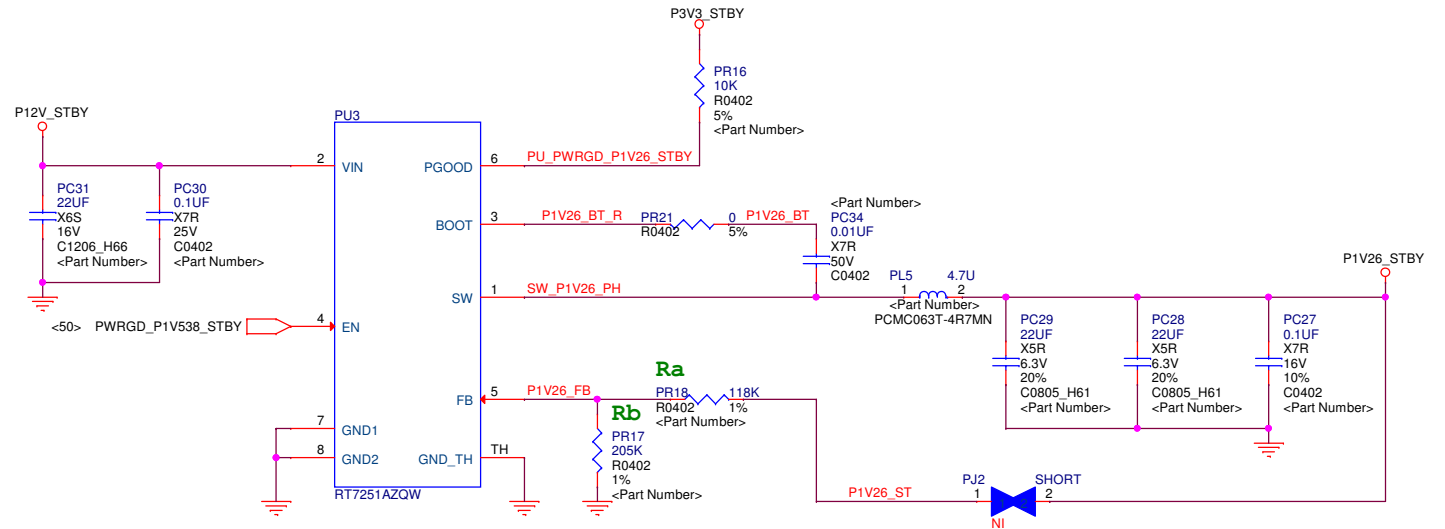
Output Voltage = 1V538±5%
Output Ripple & Noise < 30mV
Transient Tolerance = 155mV
TDC = 1.22A
Max current = 1.22A
Over-Current Protection(Max Rating × 1.5) = 1.83A
Slew Rate = 2.5A/us
Work Frequency = 340kHz
Efficiency > 90% @TDC



$$V_{OUT}=0.8(1+R_a/R_b)=1.538V$$

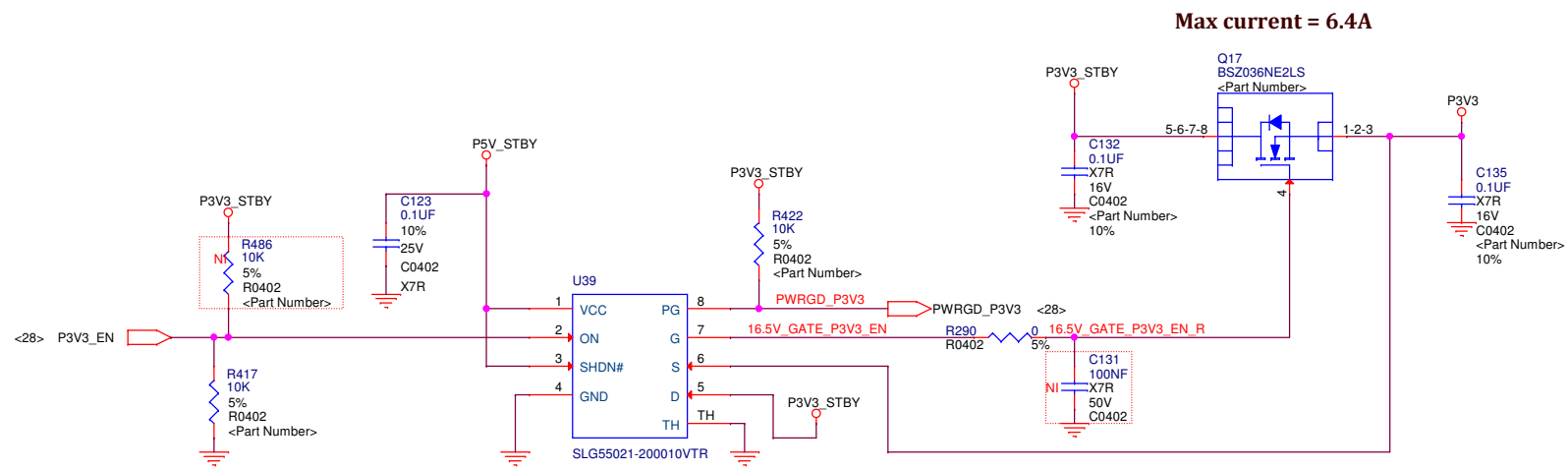
P1V26_STBY

Output Voltage = 1V26±5%
Output Ripple & Noise < 30mV
Transient Tolerance = 126mV
TDC = 0.77A
Max current = 0.77A
Over-Current Protection(Max Rating × 1.5) = 1.16A
Slew Rate = 2.5A/us
Work Frequency = 340kHz
Efficiency > 90% @TDC



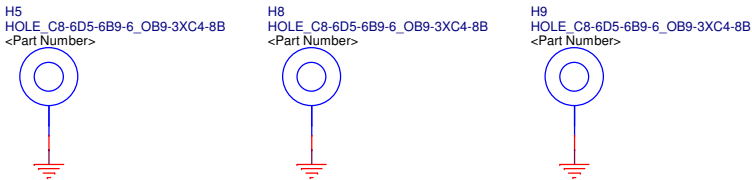
$$V_{OUT}=0.8(1+R_a/R_b)=1.26V$$

VR P1V538_STBY & P1V26_STBY

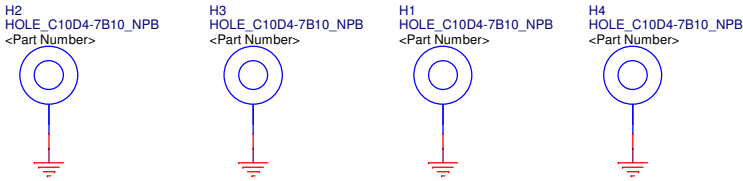


P3V3 Power Switch

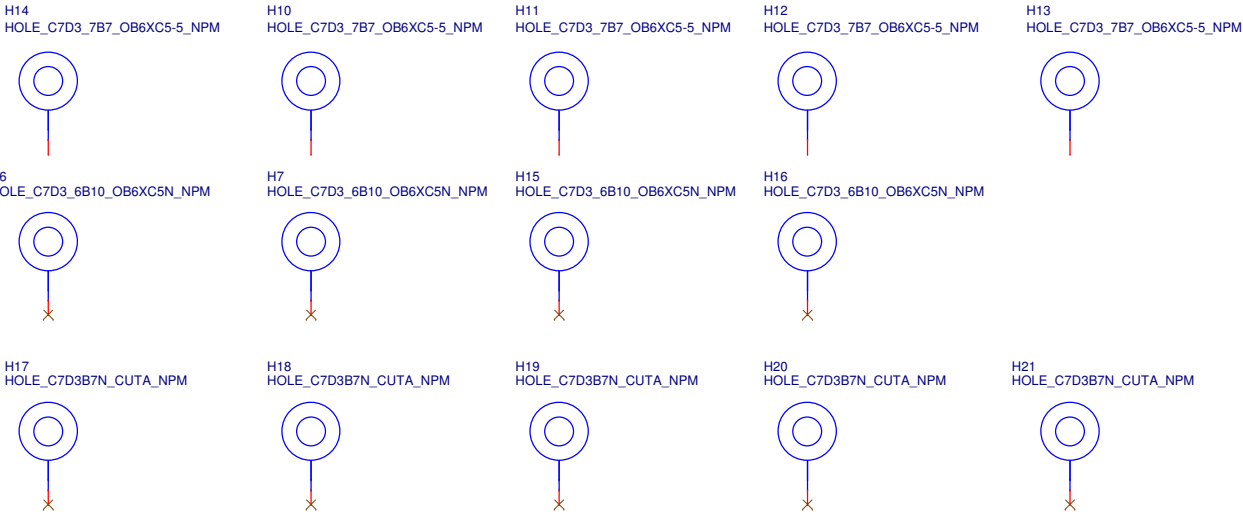
SMT THUMB SCREW * 3pcs



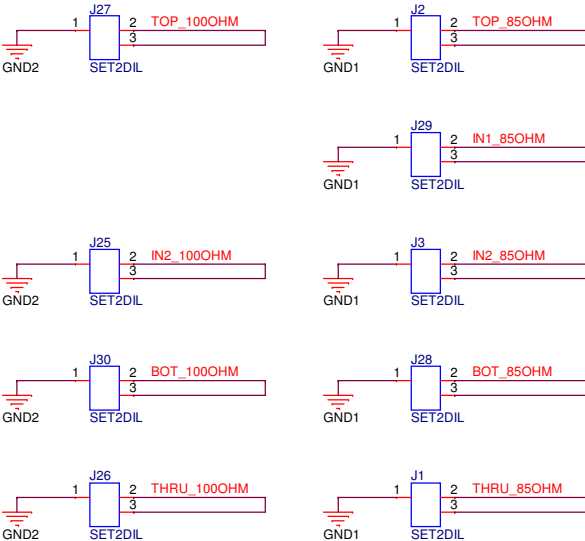
SMT NUT * 4pcs



Key Holes * 14pcs



SET2DIL



Mechanical