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Compute Project

Debug Reference Guide

for Yosemite v0.5 System

Rev. 0.5

Author: <Primary>

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2. Scope

This document defines the technical specifications for the <Yosemite> used in Open Compute Project <Server Project>

Revision History

Revision	Date	Change Summary
0.5	2018/01/18	Preliminary Version Release

CONTENT

LIST OF FIGURES

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1. Yosemite System

1.1 Overview

Yosemite is FB's next generation platform that enables higher performance 1P server cards. It hosts up to 4 OCP compliant 1P server cards. And Yosemite system implements a vertically installed side-plane to hold 1P server card horizontally. The system communicates with external world via an OCP 2.0 40Gb Ethernet mezzanine card, or a 10GBase-KR based 40Gb capable PHY mezzanine card. A Baseband Management Controller is used to manage all 1P servers and the system itself. BMC support both in-band management form 1P server card and out-of-band management through Ethernet NIC's side band.

Yosemite system is single-socket compute system compatible with Open Rack V2.

1.2 Yosemite System

Yosemite contains one primary board as the side-plane to hold all of the connectors and common infrastructure pieces, including the 1P server card connectors, OCP V2 mezzanine card connectors, a 12.5V inlet power connector (from the Cubby chassis). BMC section, fan connectors, and a hot-swap controller.

Yosemite side-plane is installed vertically on the side of a Cubby chassis. OCP complaint 1P server cards with height of 110mm or 160mm can be installed horizontally to the side-plane.
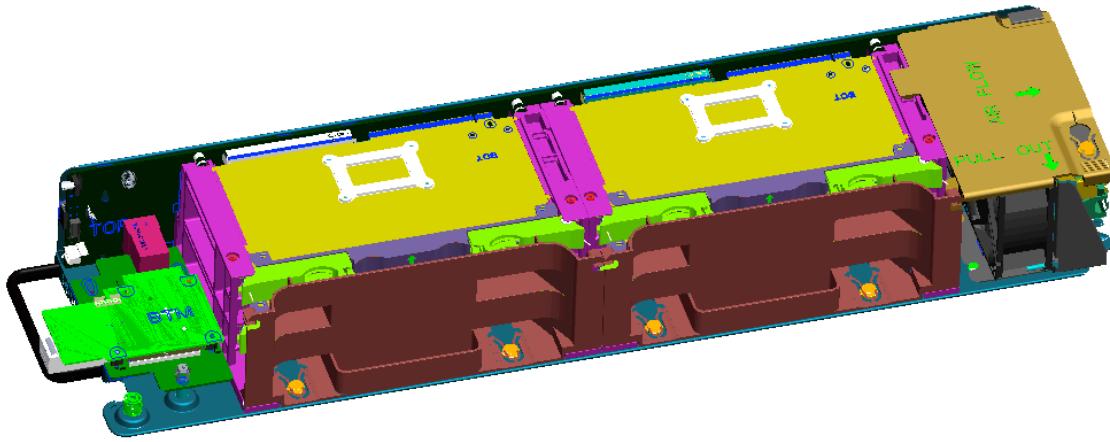
Figure 1   Yosemite System

1.3 Yosemite Functional Block Diagram

High level functional block diagram of Yosemite is shown in

Figure 2

Yosemite Block Diagram V0.08

OCP V2 40GE Mezz or 10GBASE-KR Mezz with QSFP+ Conn

Adaptor board

| Slot1 1S Server Card | Slot2 1S Server Card | Slot3 1S Server Card | Slot4 1S Server Card |

BMC (AST1250)

HotSwap Controllers

Temp Seosors (Inlet and Outlet)

FRU

Fan x 2

Power Button Reset Button Select Switch LEDs

Analog Sensors

OCP Debug Card

USB MUX

USB HUB

USB Conn

Side-plane
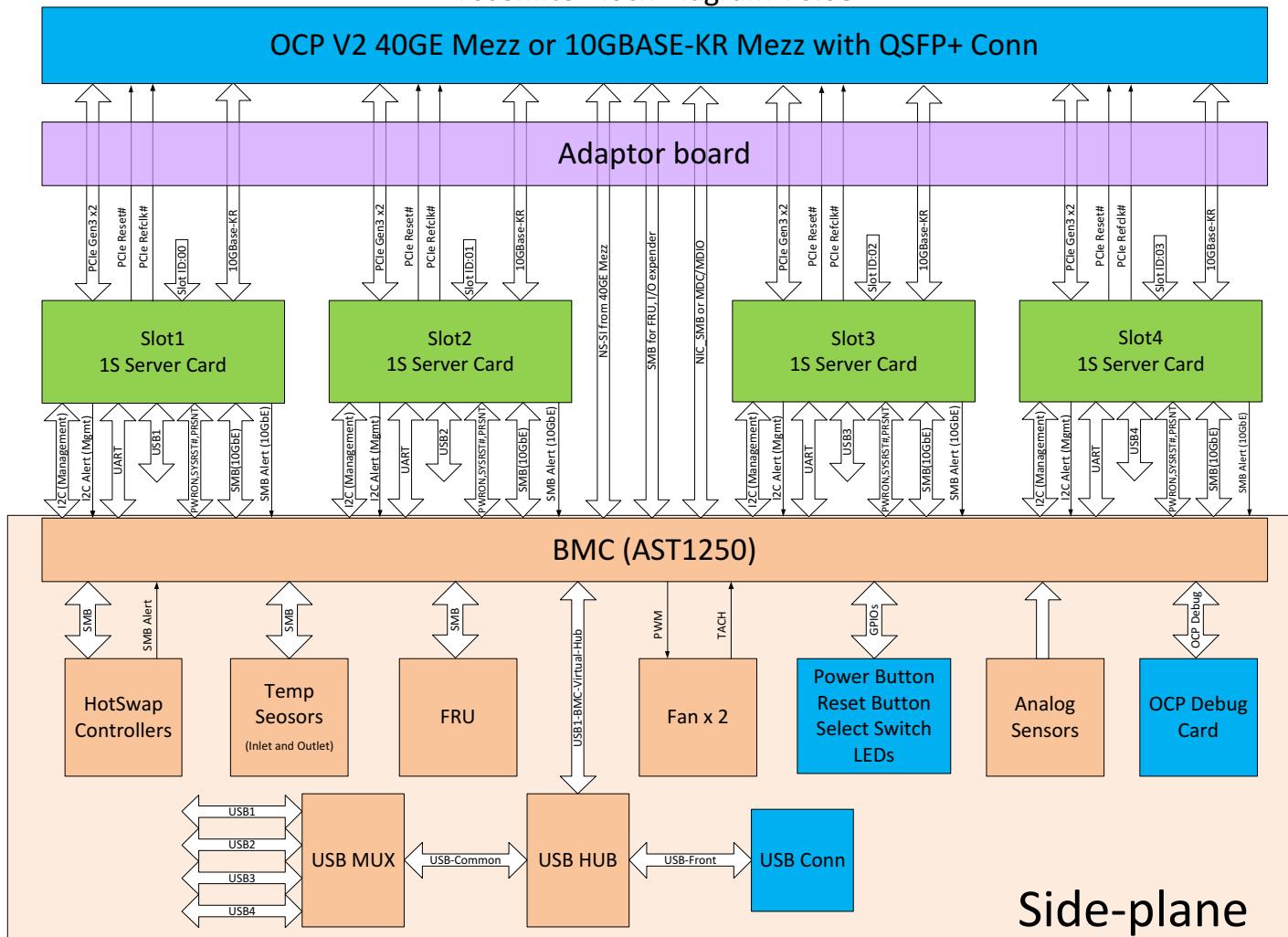
Figure 2   Yosemite Functional Block Diagram

1.4 System I2C Topology
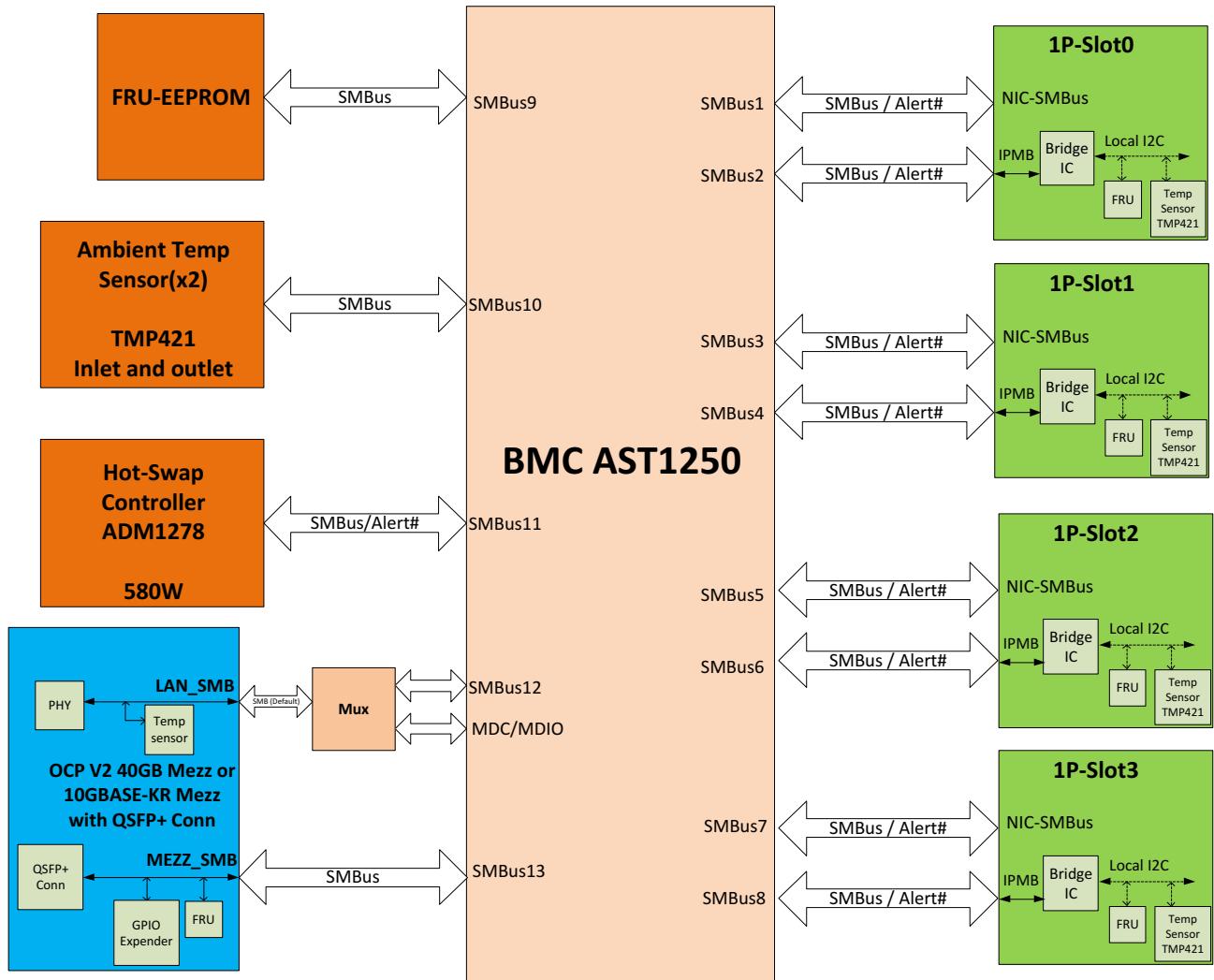
Figure 3   System I2C Topology

1.5 Yosemite system thermal sensors Location
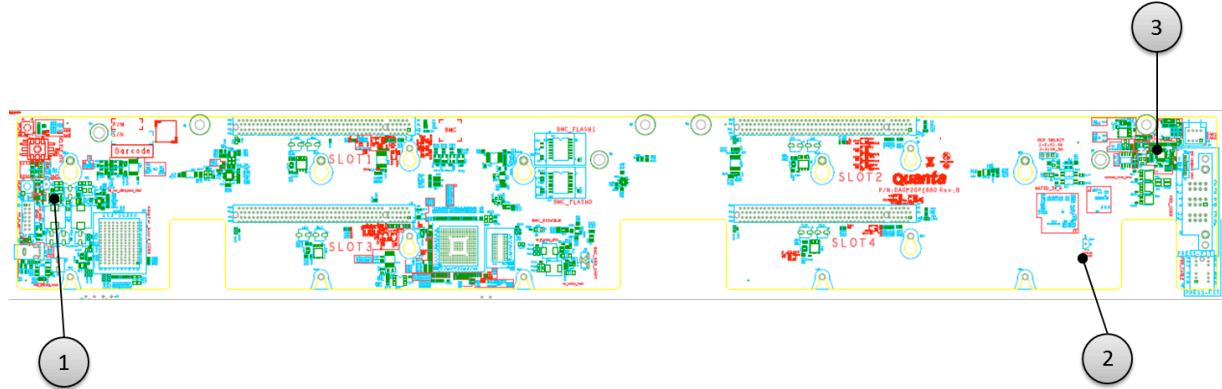
Item	Temp sensor	Location	Note
1	Inlet Temp	Q11	
2	Outlet Temp	Q13	
3	HSC Temp	Q7	

Side-Plane
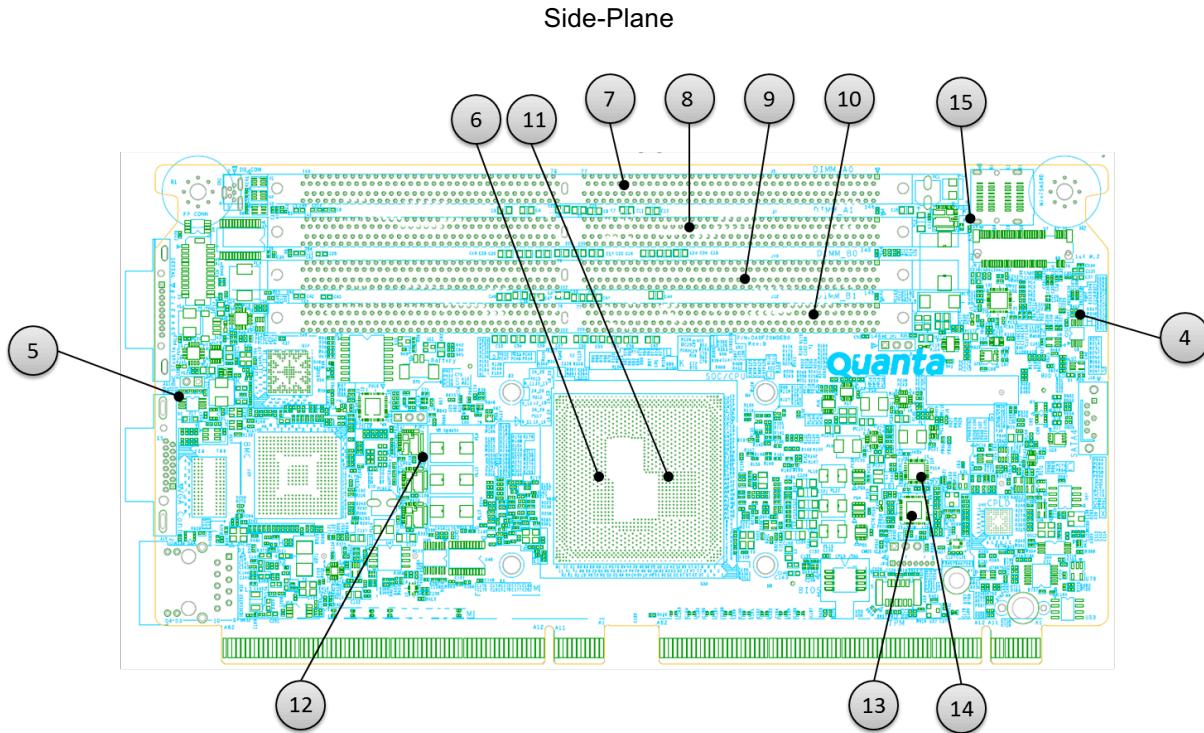
Item	Temp sensor	Location	Note
4	MB Outlet Temp	U8	
5	MB Inlet Temp	U17	
6	SOC Temp	U30	
7	SOC DIMMA0 Temp	J5	

8	SOC DIMMA1 Temp	J7	
9	SOC DIMMB0 Temp	J10	
10	SOC DIMMB1 Temp	J12	
11	PCH Temp	U30	
12	VCCIN VR Temp	PQ2	
13	VCCGBE VR Temp	PU16	
14	1V05PCH VR Temp	PU14	
15	VDDR VR Temp	PQ1	
16	VCCSCSUS VR Temp	PU16	

Mono Lake
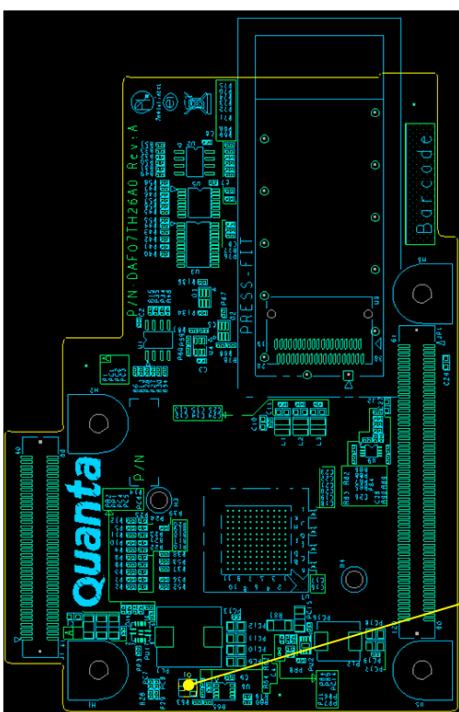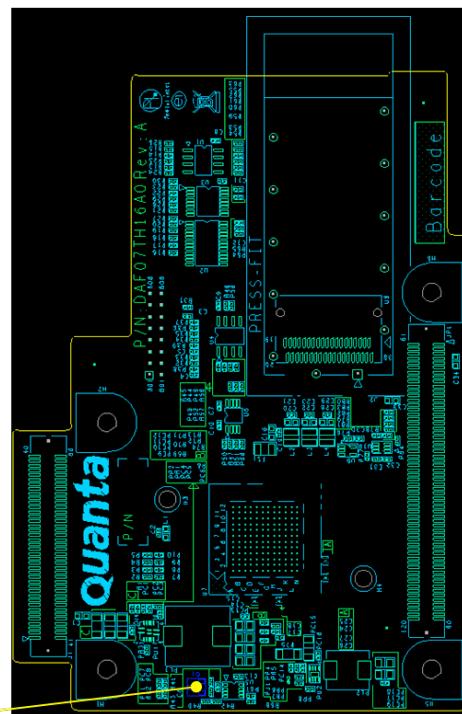
Item	Temp sensor	Location	Note
17	Mezz Temp	Q1	Cortina PHY Mezz
18	Mezz Temp	Q1	Semtech PHY Mezz

KR PHY Mezzanine card

Figure 4   Yosemite system thermal sensors Location

1.6 System Cables

Side Plane board attached with press-fit power cable.

2. MotherBoard (Mono Lake)

Mono Lake is a PCIe card like 1P server, particularly designed for Facebook's Yosemite platform. Mono Lake uses Intel's next-generation Broadwell-DE SOC, which supports 8 Xeon cores, up to 128GB DDR3/DDR4 memory, X24 PCIe Gen3 lanes, X8 PCIe Gen2 lanes, X6 SATA3 ports, 2 10GbE network controllers and other advanced features.

Mono Lake supports 4 DDR4 RDIMMs, 2 RDIMM per memory channel. The maximum memory capacity of Mono Lake is 128GB, 32GB per DIMM. Two M.2 SSD drive are connected to Broadwell-DE though a SATA or PCIe interface as local storage. Minimal capacity of this local drive is 128GB.

A Bridge IC is used to connect BMC and Broadwell-DE together for server management through an I2C interface. The BMC on Yosemite can access FRU and temperature sensors through the Bridge IC.

2.1 Mono Lake outline and placement
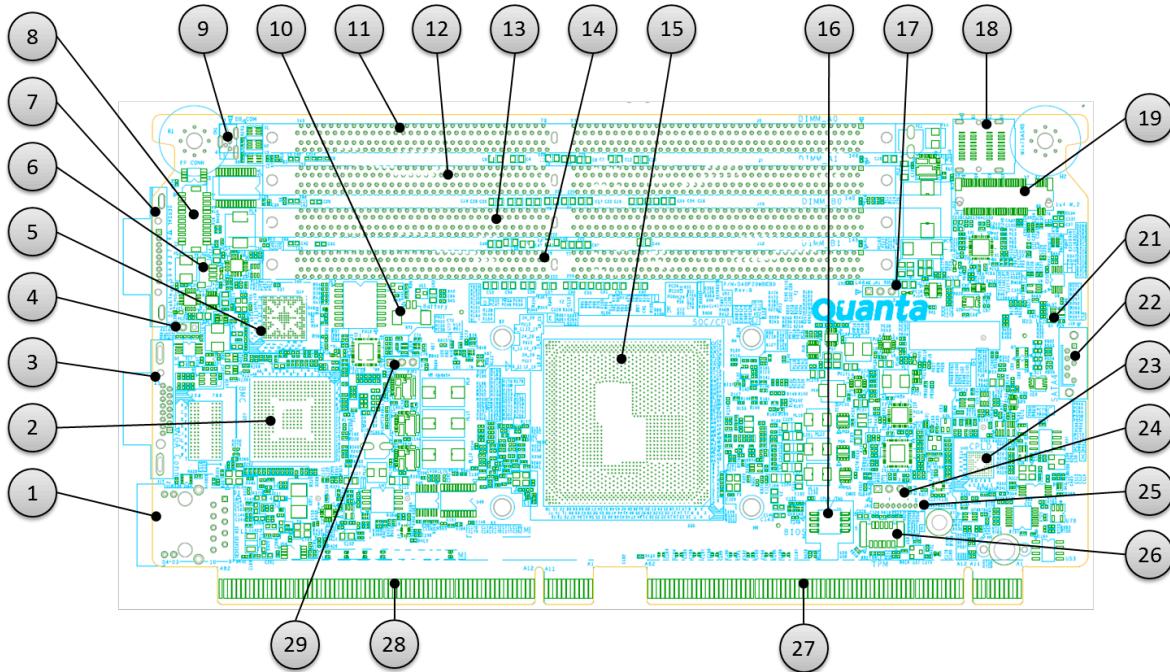
Item	Ref Designator / Silkscreen @PCB	Description	Note
1	**J18 / DEDICATED NIC**	AST2400 Dedicated NIC RJ45 conn	Only support in QCI SKU
2	**U27 / BMC**	BMC AST2400	Only support in QCI SKU
3	**J17 / VGA Conn**	VGA connector	Only support in QCI SKU
4	**J15 / BMC Disable**	BMC / Bridge IC disable header 1-2 Open: Enable 1-2 Short: Disable	
5	**U14**	Bridge IC	Unstuff in QCI SKU
6	**J13 / TI JTAG**	Bridge IC JTAG connector	Unstuff in QCI SKU

7	J11 / SERIAL	COM port connector	Only support in QCI SKU
8	J8 / FP CONN	Front panel connector	Only support in QCI SKU
9	CN1 / DB CONN	Bridge IC debug connector	Unstuff in QCI SKU
10	BT1 / Battery	Battery connector	
11	J5 / DIMM_A0	DDR4 DIMM connector channel 0 DIMM0	
12	J7 / DIMM_A1	DDR4 DIMM connector channel 0 DIMM1	
13	J10 / DIMM_B0	DDR4 DIMM connector channel 1 DIMM0	
14	J12 / DIMM_B1	DDR4 DIMM connector channel 1 DIMM1	
15	U30	Intel Broadwell-DE Processor with heat sink	
16	U56 / BIOS	BIOS flash with socket	Socket may be de-populated when MP
17	JP1 / ME	ME recovery mode jumper 1-2 : Normal (default) 2-3: ME recovery mode	
18	J6 / MiniSASHD	Mini SAS HD connector	Only support in QCI SKU
19	J9 / 1st M.2	M.2 Connector for 1st M.2 SSD drive	
21	D1 / HDD LED	M.2 HDD LED	
22	J16 / SATA4	SATA connector	Only support in QCI SKU
23	U40 / CPLD	Altera CPLD chip	
24	JP2 / CMOS CLEAR	CMOS clear jumper 1-2 : Normal (default) 2-3 : Clear COMS	
25	JP3 / CPLD JTAG	CPLD (Altera) in system programming header	
26	J33	TPM connector	Only support in QCI SKU
27	J25	OCP extension x16 golden finger	
28	J26	OCP primary x16 golden finger	
29	PJP1	VR programming header	**Debug only**

Figure 5   Mono Lake board Top overview
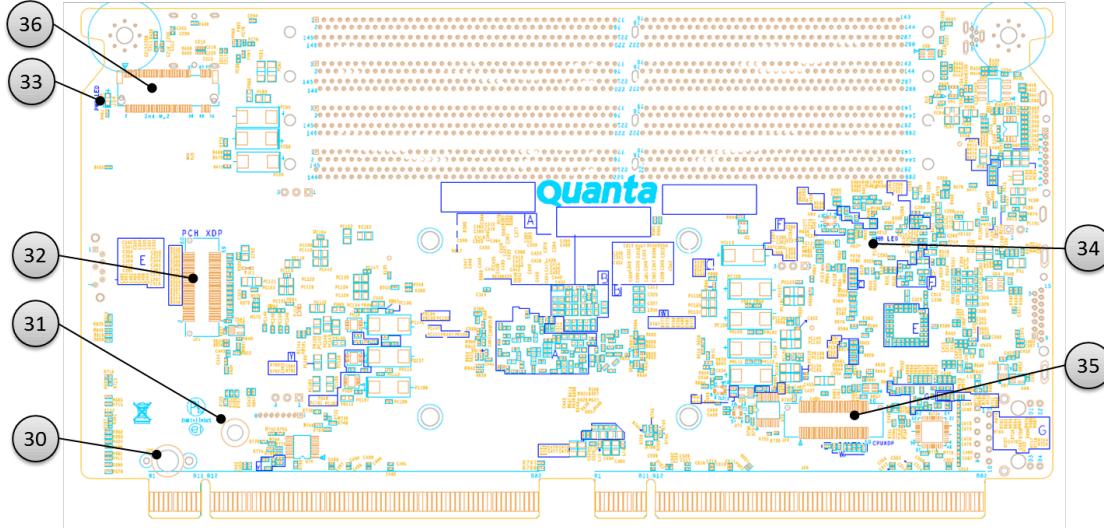
Item	Ref Designator / Silkscreen @PCB	Description	Note
30	**H9**	M.2 SSD latch	
31	**H7**	TPM stand off	
32	**J21 / PCH XDP**	Broadwell-DE PCH XDP connector	
33	**D12 /PWR LED**	MB Power LED (blue)	
34	**D13 / HB LED**	Bridge IC/BMC heart beat LED	
35	**J23 / CPU XDP**	Broaddwell-DE CPU XDP connector	
36	**J34 / 2nd M.2**	2nd M.2 connector	

Figure 6   Mono Lake board bottom overview

2.2 Mono Lake Models

➢ Feature Model

Function	Description	Note
Processor	• Intel Broadwell-DE, 1.8GHz (tbd), Xeon 8 cores, TDP 45W	
Memory	• Two channels, two DIMMs per channel • DDR4 RDIMM, UDIMM • Max Mem. cap. 128GB	
External I/O **Connections**	• X24 PCIe Gen3 Lanes • Two 10GBase-KR NICs • One USB 2.0 • Serial Port (Tx/Rx only) • SATA Gen3 • I2C Management • Power On/Off, Reset	10GBase-KR NIC only support 1 port in Yosemite.
Storage	• NGFF(m.2) Flash Card *with PCI-E Gen2 x2 or SATA3 I/F*	

Table 1 Mono Lake Feature Model

2.3 Mono Lake Block Diagram
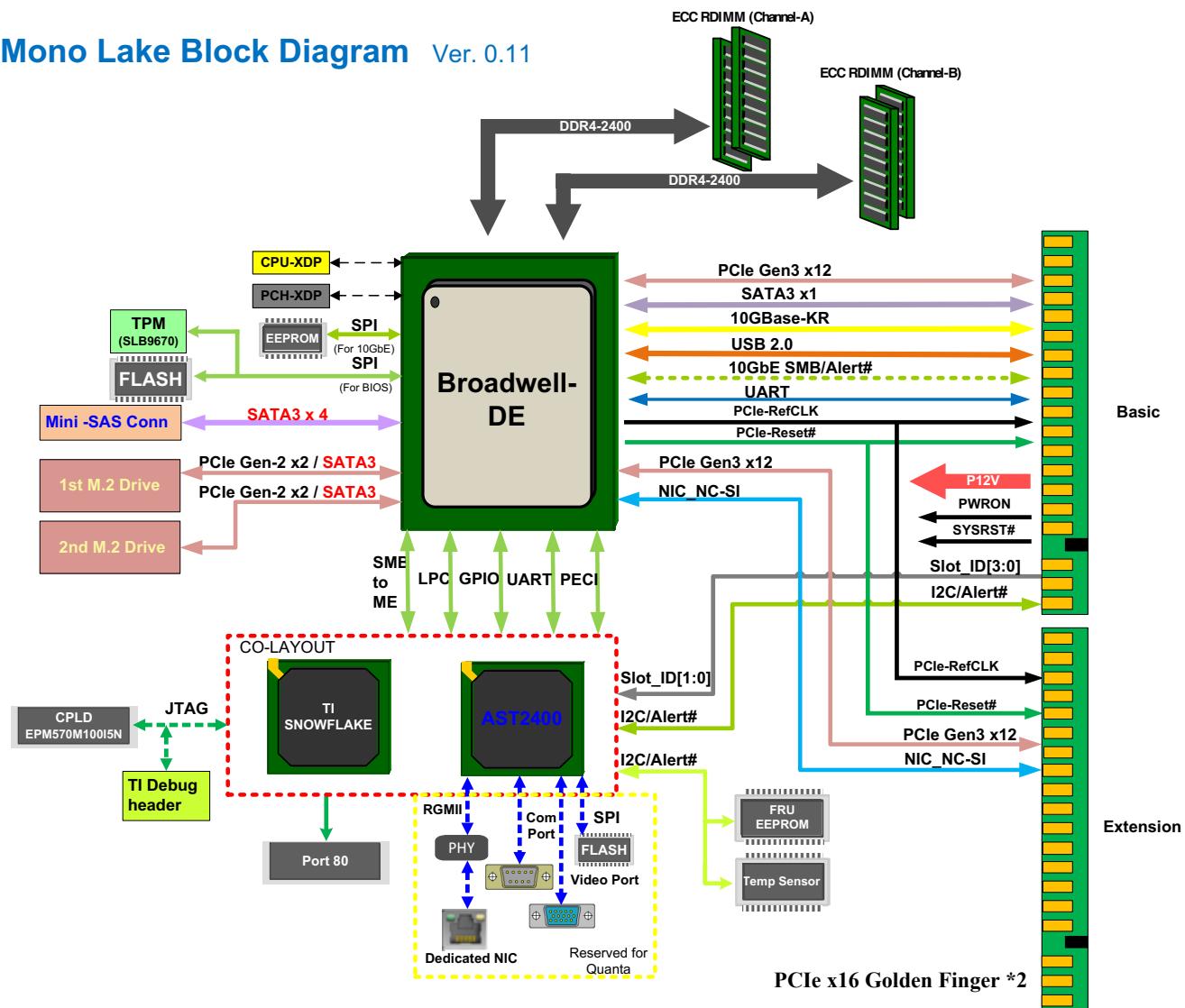
Figure 7   Mono Lake Block Diagram

2.4 Power Distribution Diagram
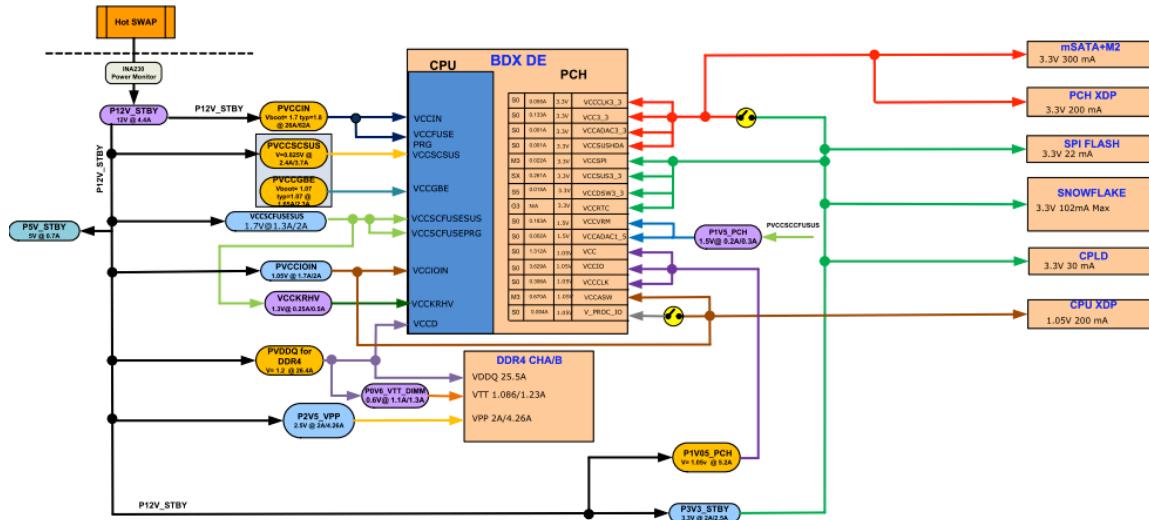
Figure 8   Power Distribution Diagram

2.5 Powergood / Reset Block Diagram
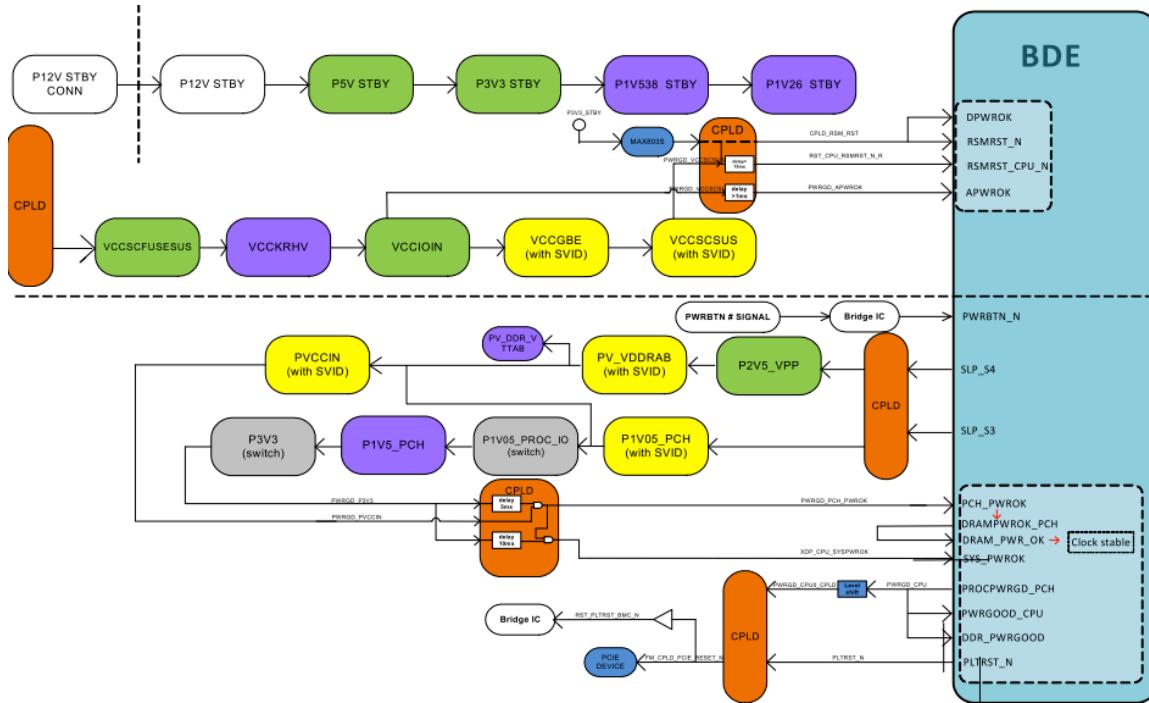
Figure 9   PWRGD/Reset Diagram

2.6 Clock Distribution Diagram
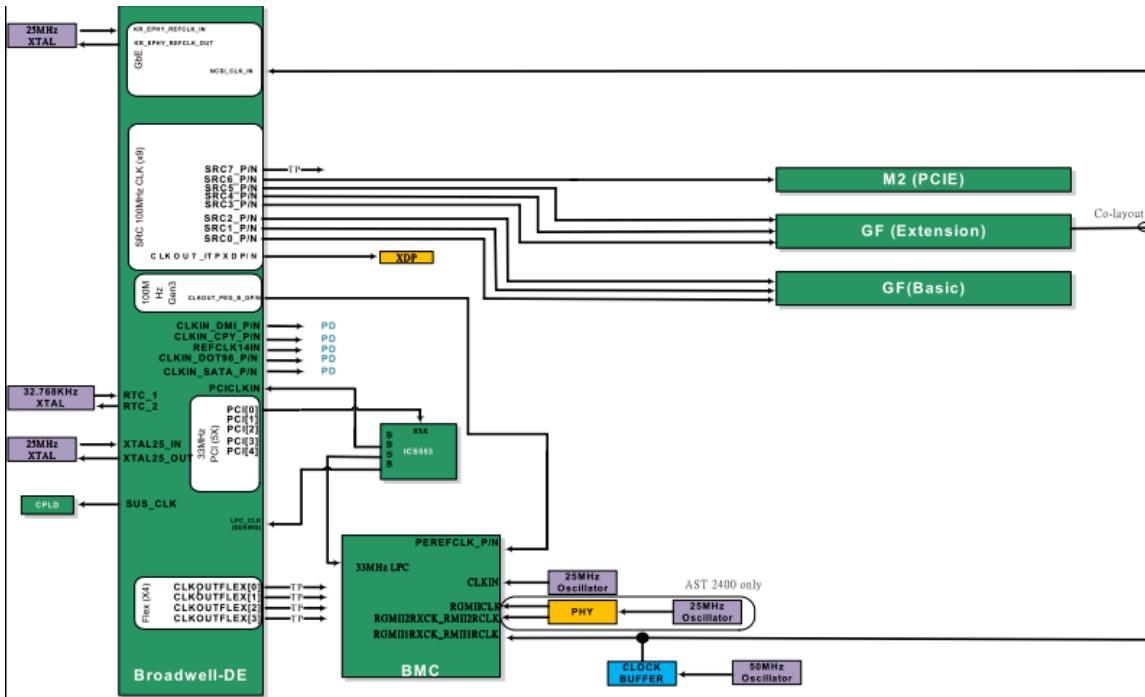
Figure 10   Clock Distribution Diagram

2.7 SMBUS Block Diagram
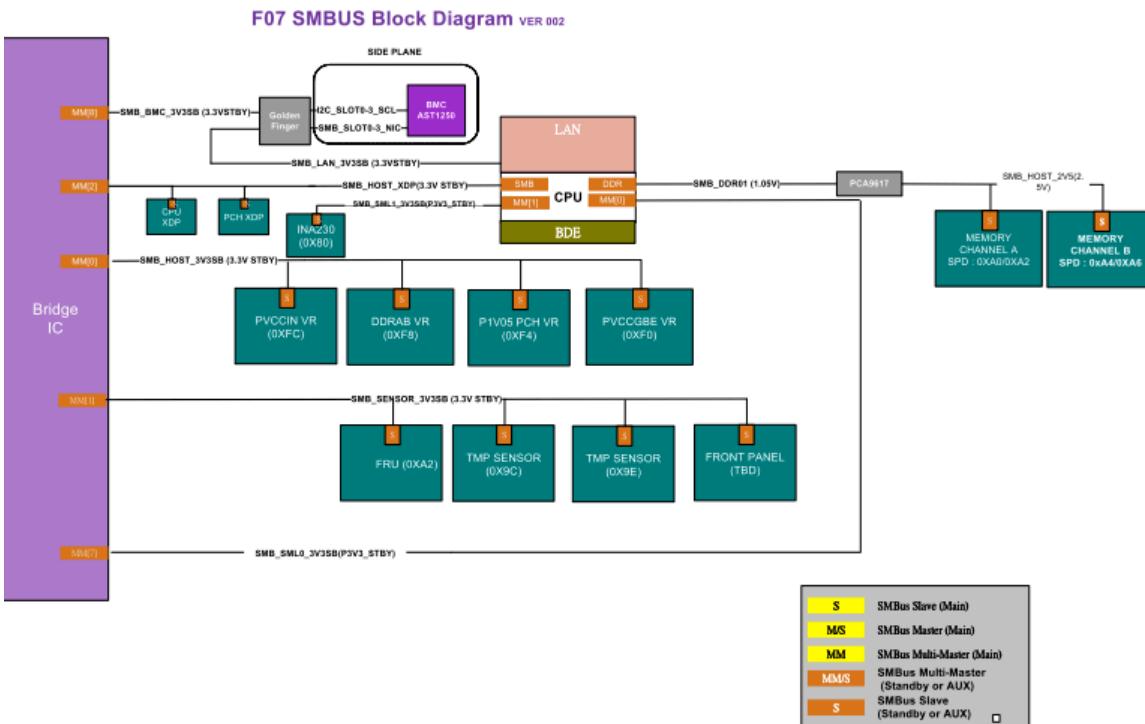
Figure 11   SMBUS Block Diagram

2.8 SMBus address lists

Below is SMBUS address lists for all devices on the I2C bus

Host	Bus Name	Device	Location	Address	Note
BIC/BDE	SMB_HOST_XDP	CPU XDP	J23		Mono Lake
BIC/BDE	SMB_HOST_XDP	PCH XDP	J21		Mono Lake
BIC/BDE	SMB_HOST_XDP	TPM	J33		Mono Lake
BIC	SMB_HOST_3V3SB	PVCCIN	PU10	0XFC	Mono Lake
BIC	SMB_HOST_3V3SB	DDRAB	PU2	0XF8	Mono Lake
BIC	SMB_HOST_3V3SB	P1V05 PCH	Pu14	0XF4	Mono Lake
BIC	SMB_HOST_3V3SB	PVCCGBE	Pu16	0XF0	Mono Lake
BIC	SMB_SENSOR_3V3SB	FRU	U60	0XA2	Mono Lake
BIC	SMB_SENSOR_3V3SB	TMP SENSOR	U17	0X9C	Mono Lake
BIC	SMB_SENSOR_3V3SB	TMP SENSOR	U8	0X9E	Mono Lake
BDE	SMB_DDR01	CHANNEL A DIMM0	J5	0XA0	Mono Lake
BDE	SMB_DDR01	CHANNEL A DIMM1	J7	0XA2	Mono Lake
BDE	SMB_DDR01	CHANNEL B DIMM0	J10	0XA4	Mono Lake
BDE	SMB_DDR01	CHANNEL B DIMM1	J12	0XA6	Mono Lake
Host	Bus Name	Device	Location	Address	Note
BMC	SMB_SLOT2_NIC	SLOT2	J7		Side-Plane
BMC	I2C_SLOT2	SLOT2	J7		Side-Plane
BMC	SMB_SLOT1_NIC	SLOT1	J6		Side-Plane
BMC	I2C_SLOT1	SLOT1	J6		Side-Plane
BMC	SMB_SLOT4_NIC	SLOT4	J17		Side-Plane
BMC	I2C_SLOT4	SLOT4	J17		Side-Plane
BMC	SMB_SLOT3_NIC	SLOT3	J16		Side-Plane
BMC	I2C_SLOT3	SLOT3	J16		Side-Plane
BMC	SMB_FRU	FRU	U44	0XA2	Side-Plane
BMC	SMB_TEMP	INLET TEMP SENSOR	U9	0X9C	Side-Plane
BMC	SMB_TEMP	OUTLET TEMP	U20	0X9E	Side-

			SENSOR			Plane
BMC	SMB_HOTSWAP	HSC	U7	0X11	Side-Plane
BMC	SMB_MEZZ_NIC	MEZZ card	J23		Side-Plane
BMC	SMB_MEZZ	MEZZ card	J23		Side-Plane

Table 2 SMBus address lists

2.9 GPIO Pin Definitions

➢ **CPU** GPIO Pin Definition:

GPIO Name/ Ball Name	SoC Ball/ Pin	Default Type	Power well	Net Name	Usage
BMBUSY_N_GPIO0	BB28	GPI	Core	PU_BMBUSY_N_GPIO0	NA
TACH1_GPIO1	AM4	GPI	Core	SKU_BDE_ID1	SKU ID1
PIRQE_N_GPIO2	BV16	GPI	Core	FM_BDXDE_ERR0_LVT3_N	ERR0
PIRQF_N_GPIO3	BN22	GPI	Core	FM_BDXDE_ERR1_LVT3_N	ERR1
PIRQG_N_GPIO4	BL22	GPI	Core	FM_CPU2PCH_THROT_LVT3	CPU to PCH_THROT
PIRQH_N_GPIO5	BW22	GPI	Core	FM_BDXDE_CATERR_LVT3_N	CATERR
TACH2_GPIO6	AV11	GPI	Core	SKU_BDE_ID2	SKU ID2
TACH3_GPIO7	AG2	GPI	Core	REV_BDE_ID0	SKU ID0
GPIO8_OCS	BJ4	GPO	SUS	IRQ_BMC_PCH_NMI_NOA1_CLK	BMC to PCH NMI
OC5_N_GPIO9	BF3	Native	SUS	FM_USB_OC_5_N	Use for XDP
OC6_N_GPIO10	BF1	Native	SUS	FM_USB_OC_6_N	Use for XDP
SMBALERT_N_GPIO11	BH7	Native	SUS	PU_SMBALERT_N_GPIO11	NA
LAN_PHY_PWR_CTRL_GPIO12	BD26	Native	SUS	IRQ_IBMC_PCH_SMI_LPC_N	BMC to PCH SMI
OC7_N_GPIO14	BD3	Native	SUS	FM_LVC3_RISER1_ID4_N_PU	Use for XDP
GPIO15	BA23	GPO	SUS	PD_P1V2_VDDQ_SEL_N	NA
SATA4GP_GPIO16	BN2	GPI	Core	FM_CPU_THROTTLE_N	CPU_THROTTLE
TACH0_GPIO17	AN3	GPI	Core	SKU_BDE_ID0	SKU ID0
GPIO18	BN4	Native	Core	FM_SRC1CLKRQB_GP18	SRC1CLKRQB
SATA1GP_GPIO19	BT3	GPI	Core	RST_PCIE_PCH_N_GPIO19	PCH XDP RST
GPIO20_SMI_N	BR4	Native	Core	SMI_BMC_N_R	PCH SMI
SATA0GP_GPIO21	BR2	GPI	Core	FM_SATA0GP_GP21	Use for XDP
SCLOCK_GPIO22	BN14	GPI	Core	SGPIO_SATA_CLOCK_R	SCLOCK
LDRQ1_N_GPIO23	AL5	Native	Core	TP_PCH_DRQ1_N	TP
GPIO24_MGPIO0	BB21	GPO	SUS	FAST_THROTTLE_N_R	FAST THROTTLE
GPIO25	BA5	Native	SUS	BMC_READY_N	BMC READY
GPIO26	BB14	Native	SUS	TP_GPIO26	TP

GPIO27_MGPIO6	BB16	GPI	SUS	FM_CPLD_GPIO27_MGPIO6	Use for CPLD
GPIO28_MGPIO7	BB23	GPO	SUS	FM_BDXDE_ME_DRIVE_N	Use for CPLD
SLP_WLAN_N_GPIO29_MGPIO3	BB12	Native	SUS	H_BDXDE_PROCHOT_DISABLE	PROCHOT_DISABLE
SUSWARN_N_SUSPWRDNACK_GPIO30	AY11	Native	SUS	SUSPWRDNACK	NA
GPIO31_MGPIO2	BC9	GPI	SUS	SMB_INA230_ALRT_N	INA230 Alert
GPIO32	BB27	GPO	Core	TP_GPIO32	TP
GPIO33	AN11	GPO	Core	PD_DMI_RX_TERMINATION	NA
GPIO35_NMI_N	BP1	GPO	Core	NMI_BDE_R	NMI
SATA2GP_GPIO36	BT1	GPI	Core	FM_BIOS_ADV_FUNCTIONS_GPIO36	Use for XDP
SATA3GP_GPIO37	BL2	GPI	Core	FM_ADR_TRIGGER_N_GPIO37	ADR TRIGGER
SLOAD_GPIO38	BP13	GPI	Core	SGPIO_SATA_LOAD_R	SGPIO_SATA_LOAD
SDATAOUT0_GPIO39	BU18	GPI	Core	SGPIO_SATA_DATAOUT0_R	SGPIO_SATA_DATAOUT0
OC1_N_GPIO40	BE2	Native	SUS	FM_USB_OC_1_N	Use for XDP
OC2_N_GPIO41	BG4	Native	SUS	FM_USB_OC_2_N	Use for XDP
OC3_N_GPIO42	BG2	Native	SUS	FM_USB_OC_3_N	Use for XDP
OC4_N_GPIO43	BE4	Native	SUS	FM_USB_OC_4_N	Use for XDP
GPIO44	BD18	Native	SUS	TP_GPIO44	TP
GPIO45	BA21	Native	SUS	TP_GPIO45	TP
GPIO46	BA19	Native	SUS	FM_BIOS_POST_CMPLT_N	BIOS POST COMPLETE
SDATAOUT1_GPIO48	BT16	GPI	Core	PU_SGPIO_SATA_DATAOUT1	NA
SATA5GP_GPIO49	BM1	GPI	Core	FM_XDP_PCH_OBSDATA_D<1>	Use for XDP
GPIO50	BV20	GPI	Core	PU_GP50_GSXCLK	NA
GPIO51	BL18	GPO	Core	PU_GPIO51_GSXDOUT	NA
GPIO52	BP16	GPI	Core	PD_GPIO52_CPUSV	NA
GPIO53	BT20	GPO	Core	PD_GPIO53_GSXDIN	NA
GPIO54	BW18	GPI	Core	PU_GP54_GSXSREST_N	NA
GPIO55	BU22	GPO	Core	PU_BIOS_RCVR_BOOT_J2	NA
GPIO57_MGPIO5	BP9	GPI	SUS	PU_GPIO57_ME_RCVR_N	NA
SML1CLK_GPIO58_MGPIO11	BG9	Native	SUS	SMB_SML1_3V3SB_CLK	SMB_SML1_3V3SB_CLK
OC0_N_GPIO59	BH1	Native	SUS	FM_USB_OC_0_N	Use for XDP
SML0ALERT_N_GPIO60_MGPIO4	BL7	Native	SUS	SMB_SML0_3V3SB_ALERT	SMB_SML0_3V3SB_ALERT
SUS_STAT_N_GPIO61	BB18	Native	SUS	SLP_SUS_STAT_N	SLP_SUS_STAT
SUSCLK_GPIO62	BD11	Native	SUS	CLK_CPLD_SUSCLK_R	SUSCLK
CLKOUTFLEX1_GPIO65	AC4	Native	Core		NA
CLKOUTFLEX3_GPIO67	AA2	Native	Core		NA
TACH4_GPIO68	AV7	GPI	Core	REV_BDE_ID1	BOARD ID
TACH5_GPIO69	AU9	GPI	Core	TPM_PRSNT_N	TPM PRESENT

TACH6_GPIO70	AU14	Native	Core		NA
TACH7_GPIO71	AM2	Native	Core		NA
GPIO72	BB4	Native	Core	PU_GPIO72_BATLOW_N	NA
SML1ALERT_N_PCHHOT_N_GPIO74	BF7	Native	SUS	PCHHOT_CPU_N	PCH HOT
SML1DATA_GPIO75_MGPIO12	BB11	Native	SUS	SMB_SML1_3V3SB_DAT	SMB_SML1_3V3SB_DAT

➢ **Bridge IC** GPIO Pin definition:

Ball Pin #	Pin Name	I/O	Type	Description	Net Name
A17	PB2/I2C0SCL	I/O	OD	I2C module 0 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.	SMB_HOST_3V3SB_CLK
B17	PB3/I2C0SDA	I/O	OD	I2C module 0 data.	SMB_HOST_3V3SB_DAT
N5	PR0/I2C1SCL	I/O	OD	I2C module 1 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.	I2C_SCL
N4	PR1/I2C1SDA	I/O	OD	I2C module 1 data.	I2C_SDA
B12	PP5/I2C2SCL	I/O	OD	I2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.	SMB_HOST_XDP_CLK
B8	PP6/I2C2SDA	I/O	OD	I2C module 2 data.	SMB_HOST_XDP_DAT
U19	PK4/EN0RXD3	I	TTL	Ethernet 0 Receive Data 3.	
V17	PK5/EN0RXD2	I	TTL	Ethernet 0 Receive Data 2.	
V16	PK6/EN0TXD2	O	TTL	Ethernet 0 Transmit Data 2.	
W16	PK7/EN0TXD3	O	TTL	Ethernet 0 Transmit Data 3.	
C6	PB4/I2C5SCL	I/O	OD	I2C module 5 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.	FP_RST_BTN_BUF_N
B6	PB5/I2C5SDA	I/O	OD	I2C module 5 data.	BMC_RST_BTN_OUT_N
F2	PB6/I2C6SCL	I/O	TTL	GPIO port B bit 6.	
F1	PB7/I2C6SDA	I/O	TTL	GPIO port B bit 7.	
C2	PD0/I2C7SCL	I/O	OD	I2C module 7 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.	SMB_SML0_3V3SB_CLK
C1	PD1/I2C7SDA	I/O	OD	I2C module 7 data.	SMB_SML0_3V3SB_DAT
D2	PD2/I2C8SCL	I/O	TTL	GPIO port D bit 2.	SMB_BMC_3V3SB_CLK
D1	PD3/I2C8SDA	I/O	TTL	GPIO port D bit 3.	SMB_BMC_3V3SB_DAT

W10	PT0/GPIOPT0	I/O	TTL	GPIO port T bit 0.	BMC_COM_SW_N
V10	PT1/GPIOPT1	I/O	TTL	GPIO port T bit 1.	SPI_SW_SELECT
E18	PT2/GPIOPT2	I/O	TTL	GPIO port T bit 2.	LED0_LAN_SPEED
F17	PT3/GPIOPT3	I/O	TTL	GPIO port T bit 3.	LED0_LAN_STAT_ACT
B14	PS2/GPIOPS2	I/O	TTL	GPIO port S bit 2.	
A14	PS3/GPIOPS3	I/O	TTL	GPIO port S bit 3.	FM_BDE_POST_CMPLT_N
V9	PS4/GPIOPS4	I/O	TTL	GPIO port S bit 4.	FM_BDXDE_SLP3_N
T13	PS5/GPIOPS5	I/O	TTL	GPIO port S bit 5.	BMC_HARTBEAT_LED_R
U10	PS6/GPIOPS6	I/O	TTL	GPIO port S bit 6.	
U2	PH6/GPIOPH6	I/O	TTL	GPIO port H bit 6.	PORT80_LED6
V2	PH7/GPIOPH7	I/O	TTL	GPIO port H bit 7.	PORT80_LED7
H17	PJ2/GPIOPJ2	I/O	TTL	GPIO port J bit 2.	
F16	PJ3/GPIOPJ3	I/O	TTL	GPIO port J bit 3.	BMC_READY_N
F18	PJ4/GPIOPJ4	I/O	TTL	GPIO port J bit 4.	FM_CPLD_FIVR_FAULT
E17	PJ5/GPIOPJ5	I/O	TTL	GPIO port J bit 5.	FM_BDXDE_ERR0_LVT3_N
N1	PJ6/GPIOPJ6	I/O	TTL	GPIO port J bit 6.	FM_BDXDE_ERR1_LVT3_N
K5	PJ7/GPIOPJ7	I/O	TTL	GPIO port J bit 7.	FM_BDXDE_ERR2_LVT3_N
K1	PK2/GPIOPK2	I/O	TTL	GPIO port K bit 2.	FM_CPLD_BDXDE_THERMTRIP_N
K2	PK3/GPIOPK3	I/O	TTL	GPIO port K bit 3.	NC_TI_GPIOK3
U12	PN7/GPIOPN7	I/O	TTL	GPIO port N bit 7.	NC_TI_GPION7
D8	PP4/GPIOPP4	I/O	TTL	GPIO port P bit 4.	PVDDR_VRHOT_N
A8	PP7/GPIOPP7	I/O	TTL	GPIO port P bit 7.	PVCCIN_VRHOT_N
M3	PQ7/GPIOPQ7	I/O	TTL	GPIO port Q bit 7.	FM_CPLD_CPU_DIMM_EVENT_CO_N
N2	PR2/GPIOPR2	I/O	TTL	GPIO port R bit 2.	SVR_ID0
V8	PR3/GPIOPR3	I/O	TTL	GPIO port R bit 3.	SVR_ID1
P3	PR4/GPIOPR4	I/O	TTL	GPIO port R bit 4.	SVR_ID2
R10	PR7/GPIOPR7	I/O	TTL	GPIO port R bit 7.	FM_PWR_LED_N
D12	PS0/GPIOPS0	I/O	TTL	GPIO port S bit 0.	
R13	PS7/GPIOPS7	I/O	TTL	GPIO port S bit 7.	RSM_RST_N
W12	PQ5/RMII0-EN0RXD0	I	TTL	Ethernet 0 Receive Data 0.	NCSI_TI_RXD0
U15	PQ6/RMII0-EN0RXD1	I	TTL	Ethernet 0 Receive Data 1.	NCSI_TI_RXD1
U14	PG7/RMII0-EN0RXDV	I	TTL	Ethernet 0 Receive Data Valid.	NCSI_TI_CRS_DV
V12	PG6/RMII0-EN0RXER	I	TTL	Ethernet 0 Receive Error.	NCSI_TI_RXER
M16	PG3/RMII0-EN0TXEN	O	TTL	Ethernet 0 Transmit Enable.	NCSI_TI_TX_EN_R
K17	PG4/RMII0-EN0TXD0	O	TTL	Ethernet 0 Transmit Data 0.	NCSI_TI_TXD0_R

K15	PG5/RMII0-EN0TXD1	O	TTL	Ethernet 0 Transmit Data 1.	NCSI_TI_TXD1_R
M18	PM4/RMII0-EN0RREF_CLK	I/O	TTL	Ethernet 0 Reference Clock.	NCSI_TI_50M_CLK
W6	PF2/RMII0-EN0MDC	O	TTL	Ethernet 0 MII management clock.	
T7	PF3/RMII0-EN0MDIO	I/O	TTL	Ethernet 0 MDIO signal.	
V5	PA6/EN0RXCK	I	TTL	Ethernet 0 Receive Clock.	
V11	PG2/EN0TXCK	I	TTL	Ethernet 0 Transmit Clock.	
T12	PN6/EN0TXER	O	TTL	Ethernet 0 MII transmit error.	
N18	PM7/EN0COL	I	TTL	Ethernet 0 MII collision detect.	
N19	PM6/EN0CRS	I	TTL	Ethernet 0 MII carrier sense.	
T6	PA2/SSI0CLK	I/O	TTL	SSI module 0 clock	
U5	PA3/SSI0FSS	I/O	TTL	SSI module 0 frame signal	
V4	PA4/SSI0XDAT0	I/O	TTL	SSI Module 0 Bi-directional Data Pin 0.	
W4	PA5/SSI0XDAT1	I/O	TTL	SSI Module 0 Bi-directional Data Pin 1.	
M2	PC4/FAN0PWM0	O	TTL	Output that provides a pulse-width modulated signal for FAN 0 channel 0 that is used to control the speed of the fan.	FM_FORCE_BMC_UPDATE
L2	PC6/FAN0PWM1	O	TTL	Output that provides a pulse-width modulated signal for FAN 0 channel 1 that is used to control the speed of the fan.	
U6	PF0/FAN0PWM2	O	TTL	Output that provides a pulse-width modulated signal for FAN 0 channel 2 that is used to control the speed of the fan.	
V7	PF4/FAN0PWM4	O	TTL	Output that provides a pulse-width modulated signal for FAN 0 channel 4 that is used to control the speed of the fan.	FM_SMI_BMC_N
T8	PF6/FAN0PWM5	O	TTL	Output that provides a pulse-width modulated signal for FAN 0 channel 5 that is used to control the speed of the fan.	SMB_BMC_3V3SB_ALRT_N
N15	PG0/FAN0PWM6	O	TTL	Output that provides a pulse-width modulated signal for FAN 0 channel 6 that is used to control the speed of the fan.	IRQ_IBMC_PCH_SMI_LPC_N

B5	PE5/FAN0PWM7/GPIO	O	TTL	Output that provides a pulse-width modulated signal for FAN 0 channel 7 that is used to control the speed of the fan.	SMB_INA230_ALRT_N_PROCHOT
M1	PC5/FAN0TACH0	I	TTL	Input to FAN 0 channel 0 driven from the fan's speed sensor.	
K3	PC7/FAN0TACH1	I	TTL	Input to FAN 0 channel 1 driven from the fan's speed sensor.	
V6	PF1/FAN0TACH2	I	TTL	Input to FAN 0 channel 2 driven from the fan's speed sensor.	
W7	PF5/FAN0TACH4	I	TTL	Input to FAN 0 channel 4 driven from the fan's speed sensor.	H_EDGE_FAST_PROCHOT_N
U8	PF7/FAN0TACH5	I	TTL	Input to FAN 0 channel 5 driven from the fan's speed sensor.	NCSI_SEL_BMC
T14	PG1/FAN0TACH6	I	TTL	Input to FAN 0 channel 6 driven from the fan's speed sensor.	PWRGD_PVCCIN
A5	PE4/FAN0TACH7	I	TTL	Input to FAN 0 channel 7 driven from the fan's speed sensor.	PWRGD_PCH_PWROK
R2	PH1/LPC0COMXCTS	I	TTL	LPC0 COMx Clear-to-Send signal.	PORT80_LED1
R1	PH2/LPC0COMXDCD	I	TTL	LPC0 COMx Data Carrier Detect modem signal.	PORT80_LED2
T1	PH3/LPC0COMXDSR	I	TTL	LPC0 COMx Data Set Ready modem output control.	PORT80_LED3
R3	PH4/LPC0COMXDTR	O	TTL	LPC0 COMx Data Terminal Ready modem status input.	PORT80_LED4
T2	PH5/LPC0COMXRI	I	TTL	LPC0 COMx Ring Indicator modem status input.	PORT80_LED5
P4	PH0/LPC0COMXRTS	O	TTL	LPC0 COMx Request-to-Send signal.	PORT80_LED0
V3	PA0/U0Rx	I	TTL	UART module 0 receive.	UART_BDE_TI_TX
W3	PA1/U0Tx	O	TTL	UART module 0 transmit.	UART_BDE_TI_R_RX
B11	PN1/U1CTS	I	TTL	UART module 1 Clear To Send modem flow control input signal.	JTAG_CPLD_TCK
A11	PN2/U1DCD	I	TTL	UART module 1 Data Carrier Detect modem status input signal.	JTAG_CPLD_TDI

B10	PN3/U1DSR	I	TTL	UART module 1 Data Set Ready modem output control line.	JTAG_CPLD_TDO
A10	PN4/U1DTR	O	TTL	UART module 1 Data Terminal Ready modem status input signal.	JTAG_CPLD_TMS
B9	PN5/U1RI	I	TTL	UART module 1 Ring Indicator modem status input signal.	
C10	PN0/U1RTS	O	TTL	UART module 1 Request to Send modem flow control output line.	
P2	PR5/U1RX	I	TTL	UART module 1 receive.	SVR_ID3
W9	PR6/U1TX	O	TTL	UART module 1 transmit.	
J2	PK1/U4TX	O	TTL	UART module 4 transmit.	UART_TI_R_TXD
J1	PK0/U4RX	I	TTL	UART module 4 receive.	UART_TI_RXD
C8	PJ0/PECIVTT	I	Analog	PECI voltage reference.	PVCCIOIN
E7	PJ1/PECI0SD	I/O	Analog	PECI serial data.	BMC_TI_PECI_R
D6	PP0/SGPMCLK	I/O	TTL		
D7	PP1/SGPMLD	I/O	TTL		FM_PCH_HOT_LVT3_N
A7	PE6/SGPMO	I/O	TTL		FM_FAST_PROCHOT_N
G15	PM5/SGPMI	I/O	TTL		
B15	PC0/TCK/SWDCLK	I	TTL	JTAG/SWD CLK.	JTAG_TI_TCK_R
D14	PC2/TDI	I	TTL	JTAG TDI.	JTAG_TI_TDI_R
C14	PC3/TDO/SWO	O	TTL	JTAG TDO and SWO.	JTAG_TI_TDO_R
C15	PC1/TMS/SWDIO	I	TTL	JTAG TMS and SWDIO.	JTAG_TI_TMS_R
E3	PQ0/SSI3CLK	I/O	TTL	SSI module 3 clock.	BMC_SPICLK_R
E2	PQ1/SSI3FSS	I/O	TTL	SSI module 3 frame signal.	BMC_SPICS0_N_R
H4	PQ2/SSI3XDAT0	I/O	TTL	SSI Module 3 Bi-directional Data Pin 0.	BMC_SPIMOSI_R
M4	PQ3/SSI3XDAT1	I/O	TTL	SSI Module 3 Bi-directional Data Pin 1.	BMC_SPIMISO_R
D13	PS1/LPC0RESET_N	I	TTL	LPC0 Bus reset signal.	RST_PLTRST_BMC_N
H19	PL1/LPC0CLK	I	TTL	LPC0 Bus 33MHz clock. Only stopped if sleeping or in reset.	CLK_33M_TI_LPC
G16	PL0/LPC0FRAME_N	I	TTL	This input signals the start or abort of a transaction.	LPC_TI_FRAME_N
J18	PL3/LPC0SERIRQ	I/O	OD	Sequence started by Host, so the microcontroller can fill in IRQs (host interrupts) along the message body.	IRQ_TI_SERIRQ

K18	PM0/LPC0AD3	I/O	TTL	Multiplexed command, address, and data.	TI_LAD0_R
K19	PM1/LPC0AD2	I/O	TTL	Multiplexed command, address, and data.	TI_LAD1_R
L18	PM2/LPC0AD1	I/O	TTL	Multiplexed command, address, and data.	TI_LAD2_R
L19	PM3/LPC0AD0	I/O	TTL	Multiplexed command, address, and data.	TI_LAD3_R
G19	PL5/LPC0PD_N	I	TTL	Power down and sleep signal from host.	IRQ_BMC_PCH_NMI_NOA1_CLK
H18	PL4/LPC0SCI_N	O	TTL	LPC0 Optional SCI interrupt for ACPI or other uses.	FM_BDXDE_CATERR_LVT3_N
G18	PL2/LPC0CLKRUN_N	O	OD	Application may optionally connect this pin to drive CLKRUN to wake a sleeping bus when wanted (or to prevent it from sleeping).	NC_LPC_CLKRUN_N
A13	PQ4/DIVSCLK	O	TTL	An optionally divided reference clock output based on a selected clock source.	
B7	PE7/NMI	I	TTL	Non-maskable interrupt.	FM_NMI_EVENT_BMC_N
B13	PP2/USB0NXT	O	TTL	Asserted by the external PHY to throttle all data types.	NC
A16	PB0/USB0ID	I	Analog	This signal senses the state of the USB ID signal. The USB PHY enables an integrated pull-up, and an external element (USB connector) indicates the initial state of the USB controller (pulled down is the A side of the cable and pulled up is the B side).	NC
R7	PA7/USB0EPEN	O	TTL	Optionally used in Host mode to control an external power source to supply power to the USB bus.	NC
B18	PL7/USB0DM	I/O	Analog	Bidirectional differential data pin (D- per USB specification) for USB0.	NC
C18	PL6/USB0DP	I/O	Analog	Bidirectional differential data pin (D+ per USB specification) for USB0.	NC
B16	PB1/USB0VBUS	I/O	Analog	This signal is used during the session request protocol. This signal allows the USB PHY to both sense the voltage level of VBUS, and pull up VBUS momentarily during VBUS pulsing.	NC

C12	PP3/RTCCLK	O	TTL	Buffered version of the Hibernation module's 32.768-kHz clock. This signal is not output when the part is in Hibernate mode.	NC

2.10 Mono Lake Power Consumption

	With 4 RDIMM
1P server card Total Power Consumption	<100W

Table 3 Mono Lake Power Budget

2.11 Mono Lake Connectors Pin Definitions

2.11.1 Pin assignments for Mono Lake Primary x16 OCP Golden Finger

Pin Name	Side B	Side A	Pin Name
P12V	1	1	PRSNT#
P12V	2	2	P12V
P12V	3	3	P12V
GND	4	4	GND
I2C_SCL	5	5	SVR_ID0/GPIO0
I2C_DATA	6	6	SVR_ID1/GPIO1
GND	7	7	COM_TX
PWR_BTN#	8	8	COM_RX
USB_P	9	9	SVR_ID2/GPIO2
USB_N	10	10	SVR_ID3/GPIO3
SYS_RESET#	11	11	PCIE_RESET#
I2C_ALERT#	12	12	GND
GND	13	13	PCIE0_REFCLK_P
GND	14	14	PCIE0_REFCLK_N
PCIE0_TX0_P	15	15	GND
PCIE0_TX0_N	16	16	GND
GND	17	17	PCIE0_RX0_P
GND	18	18	PCIE0_RX0_N
PCIE0_TX1_P	19	19	GND
PCIE0_TX1_N	20	20	GND
GND	21	21	PCIE0_RX1_P
GND	22	22	PCIE0_RX1_N
PCIE0_TX2_P	23	23	GND
PCIE0_TX2_N	24	24	GND
GND	25	25	PCIE0_RX2_P
GND	26	26	PCIE0_RX2_N
PCIE0_TX3_P	27	27	GND
PCIE0_TX3_N	28	28	GND
GND	29	29	PCIE0_RX3_P
GND	30	30	PCIE0_RX3_N
SATA0_TX_P	31	31	GND

SATA0_TX_N	32	32	GND
GND	33	33	SATA0_RX_P
GND	34	34	SATA0_RX_N
PCIE1_REFCLK_P	35	35	GND
PCIE1_REFCLK_N	36	36	GND
GND	37	37	PCIE2_REFCLK_P
GND	38	38	PCIE2_REFCLK_N
PCIE1_RESET#	39	39	GND
PCIE2_RESET#	40	40	GND
GND	41	41	FAST_THROTTLE_N
GND	42	42	NIC_SMBUS_ALERT#
NIC_SMBUS_SCL	43	43	GND
NIC_SMBUS_SDA	44	44	GND
GND	45	45	GE0_RX_P
GND	46	46	GE0_RX_N
GE0_TX_P	47	47	GND
GE0_TX_N	48	48	GND
GND	49	49	PCIE1_RX0_P
GND	50	50	PCIE1_RX0_N
PCIE1_TX0_P	51	51	GND
PCIE1_TX0_N	52	52	GND
GND	53	53	PCIE1_RX1_P
GND	54	54	PCIE1_RX1_N
PCIE1_RX1_P	55	55	GND
PCIE1_RX1_N	56	56	GND
GND	57	57	PCIE1_RX2_P
GND	58	58	PCIE1_RX2_N
PCIE1_TX2_P	59	59	GND
PCIE1_TX2_N	60	60	GND
GND	61	61	PCIE1_RX3_P
GND	62	62	PCIE1_RX3_N
PCIE1_TX3_P	63	63	GND
PCIE1_TX3_N	64	64	GND
GND	65	65	PCIE2_RX0_P
GND	66	66	PCIE2_RX0_N
PCIE2_TX0_P	67	67	GND
PCIE2_TX0_N	68	68	GND
GND	69	69	PCIE2_RX1_P
GND	70	70	PCIE2_RX1_N
PCIE2_RX1_P	71	71	GND
PCIE2_RX1_N	72	72	GND
GND	73	73	PCIE2_RX2_P
GND	74	74	PCIE2_RX2_N
PCIE2_TX2_P	75	75	GND
PCIE2_TX2_N	76	76	GND
GND	77	77	PCIE2_RX3_P
GND	78	78	PCIE2_RX3_N
PCIE2_TX3_P	79	79	GND
PCIE2_TX3_N	80	80	GND
GND	81	81	P12V
GND	82	82	P12V

Table 4 Mono Lake Primary x16 OCP Golden Finger Pin Definition

2.11.2 Pin assignments for Mono Lake Extension x16 OCP Golden Finger

Pin Name	Side B	Side A	Pin Nam e
P12V	1	1	PRSNT_B#
P12V	2	2	P12V
P12V	3	3	P12V
GND	4	4	GND
NCSI_TXEN	5	5	NCSI_RCLK
NCSI_TXD0	6	6	NCSI_RXD0
NCSI_TXD1	7	7	NCSI_RXD1
NCSI_CRSDV	8	8	GND
NCSI_RXER	9	9	PCIE4_REFCLK_P
GND	10	10	PCIE4_REFCLK_N
PCIE3_RESET#	11	11	GND
PCIE4_RESET#	12	12	GND
PCIE5_RESET#	13	13	PCIE5_REFCLK_P
GND	14	14	PCIE5_REFCLK_N
KR4_TX0_P / GE1_TX_P	15	15	GND
KR4_TX0_N / GE1_TX_N	16	16	GND
GND	17	17	KR4_RX0_P / GE1_RX_P
GND	18	18	KR4_RX0_N / GE1_RX_N
KR4_TX1_P / USB3_TX1+	19	19	GND
KR4_TX1_N / USB3_TX1-	20	20	GND
GND	21	21	KR4_RX1_P / USB3_RX1+
GND	22	22	KR4_RX1_N / USB3_RX1-
KR4_TX2_P / LAN_MDIO0	23	23	GND
KR4_TX2_N / LAN_MDC0	24	24	GND
GND	25	25	KR4_RX2_P / LAN_MDIO1
GND	26	26	KR4_RX2_N / LAN_MDC1

KR4_TX3_P / PS_EN#	27	27	GND
KR4_TX3_N / GPIO_RFU	28	28	GND
GND	29	29	KR4_RX2_P / ID_BTN_IN_N
GND	30	30	KR4_RX2_N / WAKE_N
PCIE3_REFCLK_P	31	31	GND
PCIE3_REFCLK_N	32	32	GND
GND	33	33	PCIE3_RX0_P
GND	34	34	PCIE3_RX0_N
PCIE3_TX0_P	35	35	GND
PCIE3_TX0_N	36	36	GND
GND	37	37	PCIE3_RX1_P
GND	38	38	PCIE3_RX1_N
PCIE3_TX1_P	39	39	GND
PCIE3_TX1_N	40	40	GND
GND	41	41	PCIE3_RX2_P
GND	42	42	PCIE3_RX2_N
PCIE3_TX2_P	43	43	GND
PCIE3_TX2_N	44	44	GND
GND	45	45	PCIE3_RX3_P
GND	46	46	PCIE3_RX3_N
PCIE3_RX3_P	47	47	GND
PCIE3_RX3_N	48	48	GND
GND	49	49	PCIE4_RX0_P
GND	50	50	PCIE4_RX0_N
PCIE4_TX0_P	51	51	GND
PCIE4_TX0_N	52	52	GND
GND	53	53	PCIE4_RX1_P
GND	54	54	PCIE4_RX1_N
PCIE4_TX1_P	55	55	GND
PCIE4_TX1_N	56	56	GND
GND	57	57	PCIE4_RX2_P
GND	58	58	PCIE4_RX2_N
PCIE4_TX2_P	59	59	GND
PCIE4_TX2_N	60	60	GND
GND	61	61	PCIE4_RX3_P
GND	62	62	PCIE4_RX3_N
PCIE4_TX3_P	63	63	GND
PCIE4_TX3_N	64	64	GND
GND	65	65	PCIE5_RX0_P
GND	66	66	PCIE5_RX0_N
PCIE5_TX0_P	67	67	GND
PCIE5_TX0_N	68	68	GND
GND	69	69	PCIE5_RX1_P
GND	70	70	PCIE5_RX1_N
PCIE5_TX1_P	71	71	GND
PCIE5_TX1_N	72	72	GND
GND	73	73	PCIE5_RX2_P
GND	74	74	PCIE5_RX2_N
PCIE5_TX2_P	75	75	GND

PCIE5_TX2_N	76	76	GND
GND	77	77	PCIE5_RX3_P
GND	78	78	PCIE5_RX3_N
PCIE5_TX3_P	79	79	GND
PCIE5_TX3_N	80	80	GND
GND	81	81	P12V
POWER_FAIL_N	82	82	P12V

Table 5 Mono Lake Extension x16 OCP Golden Finger Pin Definition

2.11.3 1st NGFF (m.2) Connector Pin Definition (J9)

Pin assignment	Function	Signal Name	Description
1	GND1	GND	GND
2	3.3VAUX_1	P3V3	3.3V Source
3	GND2	GND	GND
4	3.3VAUX_2	P3V3	3.3V Source
5	PERN3	NC	Host Receiver Differential Signal Pair This is an output of the SSD
6	NC1	NC	No Connect
7	PERP3	NC	Host Receiver Differential Signal Pair This is an output of the SSD
8	NC2	NC	No Connect
9	GND3	GND	GND
10	DAS/DSS#	NGFF_DA_DSS_N	Connect to a AND GATE (For Green LED)
11	PETN3	NC	Host Transmitter Differential Signal Pair This is an input of the SSD
12	3.3VAUX_3	P3V3	3.3V Source
13	PETP3	NC	Host Transmitter Differential Signal Pair This is an input of the SSD
14	3.3VAUX_4	P3V3	3.3V Source
15	GND4	GND	GND
16	3.3VAUX_5	P3V3	3.3V Source
17	PERN2	NC	Host Receiver Differential Signal Pair This is an output of the SSD
18	3.3VAUX_6	P3V3	3.3V Source
19	PERP2	NC	Host Receiver Differential Signal Pair This is an output of the SSD
20	NC3	NC	No Connect
21	GND5	GND	GND
22	NC4	NC	No Connect
23	PETN2	NC	Host Transmitter Differential Signal Pair This is an input of the SSD
24	NC5	NC	No Connect
25	PETP2	NC	Host Transmitter Differential Signal Pair This is an input of the SSD

26	NC6	NC	No Connect
27	GND6	GND	GND
28	NC7	NC	No Connect
29	PERN1	P2E_NGFF_RX_DN<1>	Host Receiver Differential Signal Pair This is an output of the SSD
30	NC8	NC	No Connect
31	PERP1	P2E_NGFF_RX_DP<1>	Host Receiver Differential Signal Pair This is an output of the SSD
32	NC9	NC	No Connect
33	GND7	GND	GND
34	NC10	NC	No Connect
35	PETN1	P2E_NGFF_TX_DN<1>	Host Transmitter Differential Signal Pair This is an input of the SSD
36	NC11	NC	No Connect
37	PETP1	P2E_NGFF_TX_DP<1>	Host Transmitter Differential Signal Pair This is an input of the SSD
38	DEVSLP	FM_CPLD_M2_DEVSLP_R	Send from CPLD. CPLD set the output as low all the time.
39	GND8	GND	GND
40	NC12	NC	No Connect
41	PERN0/SATA-B+	P2E_SATA_NGFF_RX_0_DP	Host Receiver Differential Signal Pair This is an output of the SSD
42	NC13	NC	No Connect
43	PERP0/SATA-B-	P2E_SATA_NGFF_RX_0_DN	Host Receiver Differential Signal Pair This is an output of the SSD
44	NC14	NC	No Connect
45	GND9	GND	GND
46	NC15	NC	No Connect
47	PETN0/SATA-A-	P2E_SATA_NGFF_TX_0_DN	Host Transmitter Differential Signal Pair This is an input of the SSD
48	NC16	NC	No Connect
49	PETP0/SATA-A+	P2E_SATA_NGFF_TX_0_DP	Host Transmitter Differential Signal Pair This is an input of the SSD
50	PERST#	RST_PLTRST_NGFF_N	SYSTEM_RESET
51	GND10	GND	GND
52	CLKREQ#	NC	No Connect
53	REFCLKN	CLK_100M_NGFF_PE_DN	100MHZ differential pair clock
54	PEWAKE#	TP_CPU_WAKE_NGFF_N_R	Test Point
55	REFCLKP	CLK_100M_NGFF_PE_DP	100MHZ differential pair clock
56	NC17	NC	No Connect
57	GND11	GND	GND
58	NC18	NC	No Connect
		KEY	
67	NC19	NC	No Connect
68	SUSCLK	CLK_CPLD_SUSCLK_R1	No Connect
69	PEDET	NC	No Connect

70	3.3VAUX_7	P3V3	3.3V Source
71	GND12	GND	GND
72	3.3VAUX_8	P3V3	3.3V Source
73	GND13	GND	GND
74	3.3VAUX_9	P3V3	3.3V Source
75	GND14	GND	GND
G1	G1	GND	GND
G2	G2	GND	GND

Table 6 1st m.2 connector pin Definition

2.11.4 2nd NGFF (m.2) Connector Pin Definition (J34)

Pin assignment	Function	Signal Name	Description
1	GND1	GND	GND
2	3.3VAUX_1	P3V3	3.3V Source
3	GND2	GND	GND
4	3.3VAUX_2	P3V3	3.3V Source
5	PERN3	NC	Host Receiver Differential Signal Pair This is an output of the SSD
6	NC1	NC	No Connect
7	PERP3	NC	Host Receiver Differential Signal Pair This is an output of the SSD
8	NC2	NC	No Connect
9	GND3	GND	GND
10	DAS/DSS#	NGFF_2_DA_DSS_N	Connect to a AND GATE (For Green LED)
11	PETN3	NC	Host Transmitter Differential Signal Pair This is an input of the SSD
12	3.3VAUX_3	P3V3	3.3V Source
13	PETP3	NC	Host Transmitter Differential Signal Pair This is an input of the SSD
14	3.3VAUX_4	P3V3	3.3V Source
15	GND4	GND	GND
16	3.3VAUX_5	P3V3	3.3V Source
17	PERN2	NC	Host Receiver Differential Signal Pair This is an output of the SSD
18	3.3VAUX_6	P3V3	3.3V Source
19	PERP2	NC	Host Receiver Differential Signal Pair This is an output of the SSD
20	NC3	NC	No Connect
21	GND5	GND	GND
22	NC4	NC	No Connect
23	PETN2	NC	Host Transmitter Differential Signal Pair This is an input of the SSD

24	NC5	NC	No Connect
25	PETP2	NC	Host Transmitter Differential Signal Pair This is an input of the SSD
26	NC6	NC	No Connect
27	GND6	GND	GND
28	NC7	NC	No Connect
29	PERN1	P2E_NGFF_RX_DN<3>	Host Receiver Differential Signal Pair This is an output of the SSD
30	NC8	NC	No Connect
31	PERP1	P2E_NGFF_RX_DP<3>	Host Receiver Differential Signal Pair This is an output of the SSD
32	NC9	NC	No Connect
33	GND7	GND	GND
34	NC10	NC	No Connect
35	PETN1	P2E_NGFF_TX_DN<3>	Host Transmitter Differential Signal Pair This is an input of the SSD
36	NC11	NC	No Connect
37	PETP1	P2E_NGFF_TX_DP<3>	Host Transmitter Differential Signal Pair This is an input of the SSD
38	DEVSLP	FM_CPLD_M2_NGFF_2_DEVSLP_R	Send from CPLD. CPLD set the output as low all the time
39	GND8	GND	GND
40	NC12	NC	No Connect
41	PERN0/SATA-B+	P2E_SATA_NGFF_RX_2_DP	Host Receiver Differential Signal Pair This is an output of the SSD
42	NC13	NC	No Connect
43	PERP0/SATA-B-	P2E_SATA_NGFF_RX_2_DN	Host Receiver Differential Signal Pair This is an output of the SSD
44	NC14	NC	No Connect
45	GND9	GND	GND
46	NC15	NC	No Connect
47	PETN0/SATA-A-	P2E_SATA_NGFF_TX_2_DN	Host Transmitter Differential Signal Pair This is an input of the SSD
48	NC16	NC	No Connect
49	PETP0/SATA-A+	P2E_SATA_NGFF_TX_2_DP	Host Transmitter Differential Signal Pair This is an input of the SSD
50	PERST#	RST_PLTRST_NGFF_N	SYSTEM_RESET
51	GND10	GND	GND
52	CLKREQ#	NC	No Connect
53	REFCLKN	CLK_100M_NGFF_2_PE_DN	100MHZ differential pair clock
54	PEWAKE#	TP_CPU_WAKE_NGFF_2_N_R	Test Point
55	REFCLKP	CLK_100M_NGFF_2_PE_DP	100MHZ differential pair clock
56	NC17	NC	No Connect
57	GND11	GND	GND
58	NC18	NC	No Connect
KEY			
67	NC19	NC	No Connect

68	SUSCLK	CLK_CPLD_SUSCLK_NGFF_2_R1	No Connect
69	PEDET	NC	No Connect
70	3.3VAUX_7	P3V3	3.3V Source
71	GND12	GND	GND
72	3.3VAUX_8	P3V3	3.3V Source
73	GND13	GND	GND
74	3.3VAUX_9	P3V3	3.3V Source
75	GND14	GND	GND
G1	G1	GND	GND
G2	G2	GND	GND

Table 7 2nd NGFF(m.2) connector pin Definition

2.11.5 Mono Lake Debug Connectors

2.11.5.1   Broadwell-DE SoC XDP CONNECTOR (J23 and J21)

There are two XDP connectors. J23 is used for Broadwell-DE processor CPU. J21 is used for Broadwell-DE PCH XDP. They are required for debug and should be populated in EVT and DVT samples

2.11.5.2   Bridge IC JTAG CONNECTOR (J13)

Pin#	Pin Name	Description
1	JTAG_TI_TCK	
2	JTAG_TI_TDI	
3	JTAG_TI_TDO	
4	JTAG_TI_TMS	

Table 8 Bridge IC JTAG connector pin Definition

2.11.5.3   Bridge IC UART Debug CONNECTOR (CN1)

Pin#	Pin Name	Description
1	P5V_STBY	
2	BMC_UART_TXD	
3	BMC_UART_RXD	
4	NC	Not Connect
5	GND	GND

Table 9 Bridge IC UART debug connector pin Definition

2.11.5.4   CPLD JTAG CONNECTOR (JP3)

Pin#	Pin Name	Description
1	P3V3_STBY	
2	JTAG_CPLD_TCK	

3	GND	
4	JTAG_CPLD_TDO	
5	JTAG_CPLD_TMS	
6	NC_JTAG_CPLDA_7	Not Connect
7	JTAG_CPLD_TDI	

Table 10 CPLD JTAG connector pin Definition

2.12   LED Definition

2.12.1 Power LED (D12)

Each card contains a power LED that illuminates when the power-on sequence on the card has completed successfully. The LED is blue in color and placed on the leading edge of the card (cold-aisle).

LED Status	LED COLOR	Description	Silk Screen Label
Off	N/A	Power LED. Power is off or system is power up successful.	D12
Solid ON	Blue	Power LED. System power up fail.	PWR LED

Table 11 Power LED Description

2.12.2 Bridge IC Heartbeat LED (D13)

There is a green color LED for heartbeat at bottom side of Bridge IC. It provides an easy way to know that Bridge IC is working for external world. BTW, there are 8 LEDs for System Port80 on the Mono Lake, and their placement is the Bridge IC Chip.

LED Status	LED COLOR	Description	Silk Screen Label
Off	N/A	Bridge IC is not ready	D13
Blink	Green	Bridge IC has already begun to work normally.	HB LED

Table 12 BEEP LED Description

2.12.3 HDD ACTIVE LED (D1)

There is a green color LED for HDD activity. Both 1st NGFF and 2nd NGFF will use the LED together. Its location is in the middle of these two connectors.

LED Status	LED COLOR	Description	Silk Screen Label
Off	N/A	SSD HDD Inactivity	D1
Blink	Green	SSD HDD Activity	HDD LED

Table 13 HDD Active LED Description

2.12.4 CPLD debug LED

There are four CPLD debug LEDs. They are used CPLD debug. They are required for debug and should be populated in EVT and DVT samples.

D14 is CPLD_D1; D15 is CPLD_D2; D16 is CPLD_D3, D17 is CPLD_D4.

2.13   Board Variations

2.13.1 Mono Lake Board

For Mono Lake Board, following board types are considered.

Board type Settings (SKU ID)			
ID	SKU_BDE_ID2	SKU_BDE_ID1	SKU_BDE_ID0
TBD	0	0	0
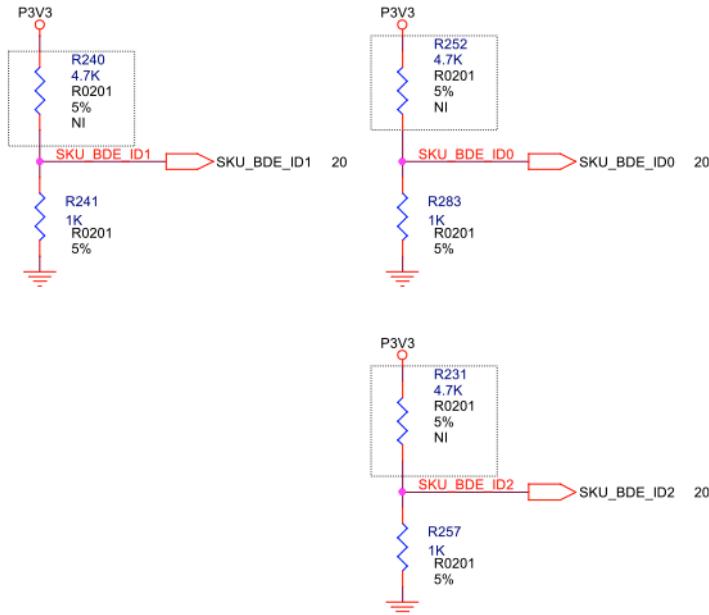
Table 14 Mono Lake Board SKU Type

2.13.2 Mono Lake Board HW Version setting

HW Version Settings		
Version	REV_BDE_ID1	REV_BDE_ID0
EVT	0	0
DVT	0	1
PVT	1	0
MP	1	1
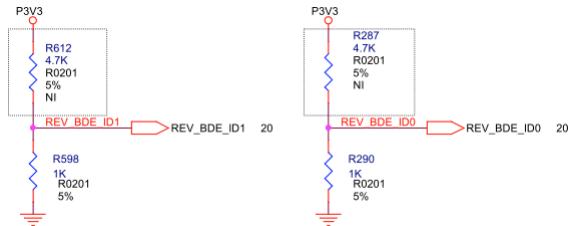
Table15 Mono Lake Board HW Version

3. System board

Yosemite system includes one installed side-plane to hold 1P server card horizontally. And side-plane also hold an adapter card to support OCP 2.0 40Gb Ethernet mezzanine or 10G-Base KR 40Gb capable PHY mezzanine card. The following chapter will introduce the following boards.

• Side-Plane

• Adapter board

• 10G-Base KR 40Gb capable PHY mezzanine card
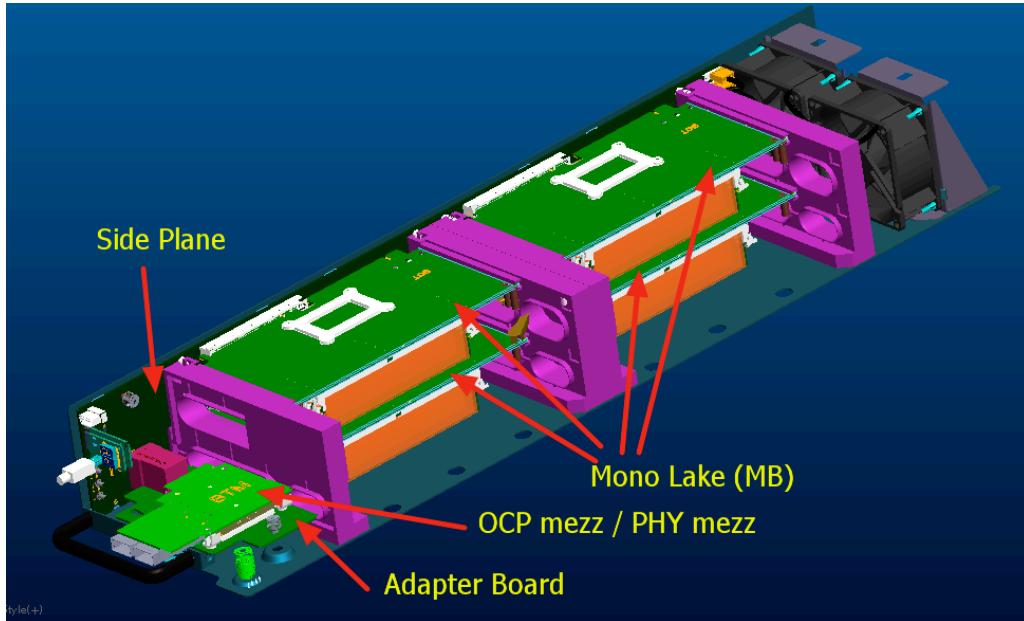
Figure 12   Yosemite System board overview

3.1 Outline and Placement

➢ Side-Plane
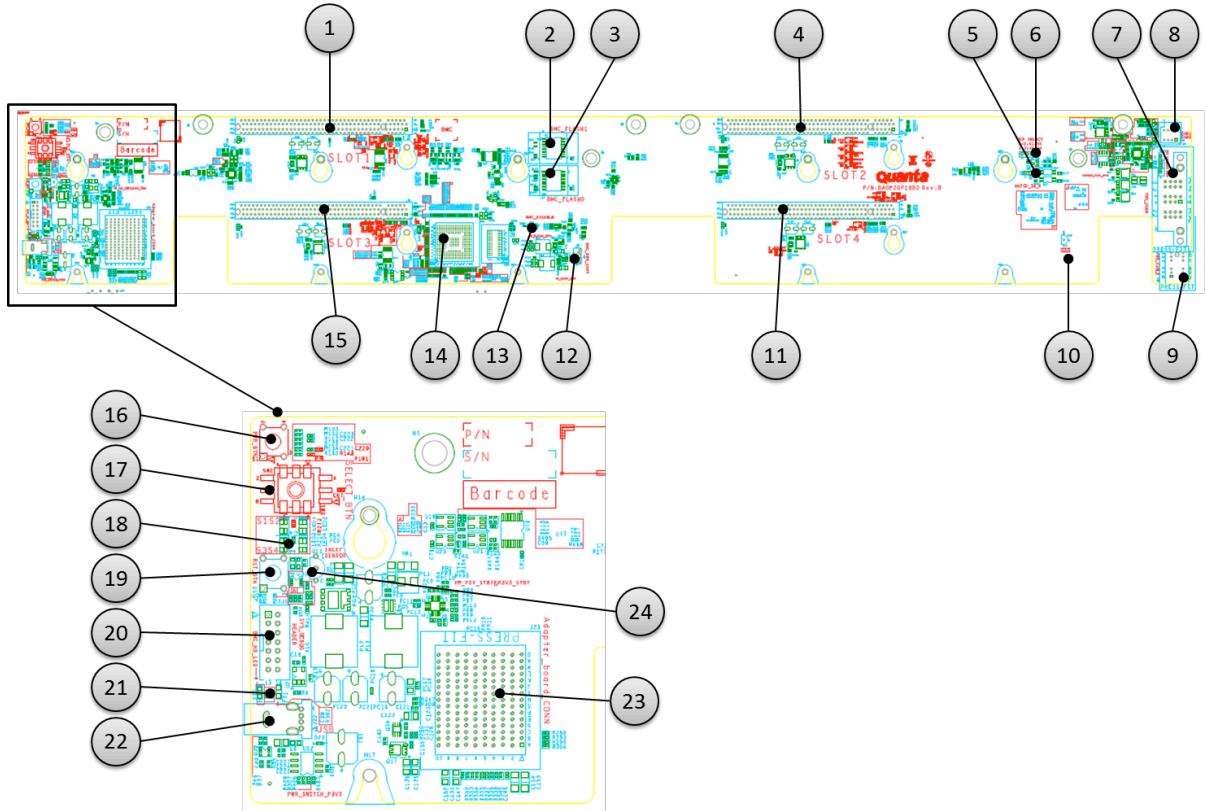
Item	Ref Designator / Silkscreen @PCB	Description	Note
1	J6 / SLOT1	1P server card – SLOT1	
2	J9,U6 / BMC FLASH1	J9: BMC Flash1 socket U6: BMC Flash1 2nd flash for firmware fail-over recovery	
3	J14,U29 / BMC FLASH0	J14: BMC Flash0 socket U29: BMC Flash0 Main flash	
4	J7 / SLOT2	1P server card – SLOT2	
5	J12 / MATED_IN_N	MATED_IN_N jumper 1-2 short: system mated in (default)	**Reserve for future**
6	JP1 / OCP SELECT	HSC OCP current select jumper 1-2: 41.1A 2-3: 48.8A (default)	
7	J15 / POWER_CONN	Power Connector	**Unstuff**
8	J4 / FAN0/FAN1	FAN0/FAN1 connector	

9	J24 / PWR_CABLE	Press-fit power cable	
10	Q13 / OUTLET SENSOR	Outlet temperature sensor	
11	J17 / SLOT4	1P server card – SLOT4	
12	J21 / BMC_DBG_UART	BMC debug UART connector	For BMC debug only
13	J18 / BMC_DISABLE	BMC disable jumper 1-2 open: BMC enable 1-2 short: BMC disable	
14	U36 / BMC	BMC ASPEED AST1250	
15	J16 / SLOT3	1P server card – SLOT3	
16	S1 / PWR_BTN	System Power button (Red Color)	
17	SW2 / SELECT_BTN	Rotary selector switch Position 0: 0000 Server Slot 1 Position 1: 0001 Server Slot 2 Position 2: 0010 Server Slot 3 Position 3: 0011 Server Slot 4 Position 4: 0100 BMC Slot Position 5 : 0101 Server Slot 1 Position 6: 0110 Server Slot 2 Position 7: 0111 Server Slot 3 Position 8: 1000 Server Slot 4 Position 9: 1001 BMC Slot	
18	LED1 / S1 LED2 / S2 LED3 / S3 LED4 / S4	Power /Status LEDs LED1 represent slot1 LED2 represent slot2 LED3 represent slot3 LED4 represent slot4	
19	S2 / RST_BTN	System Reset button (Black Color)	
20	J5 / SYS_DEBUG_HEADER	OCP Debug Card Header	
21	D15 / BMC_HB_LED	BMC Heartbeat LED	
22	J22 / USB	USB connector	
23	J23	Adapter board connector	Match with adapter board
24	Q11 / INLET SENSOR	Inlet temperature sensor	

Figure 13   Side-plane Top overview

➢   Adapter board
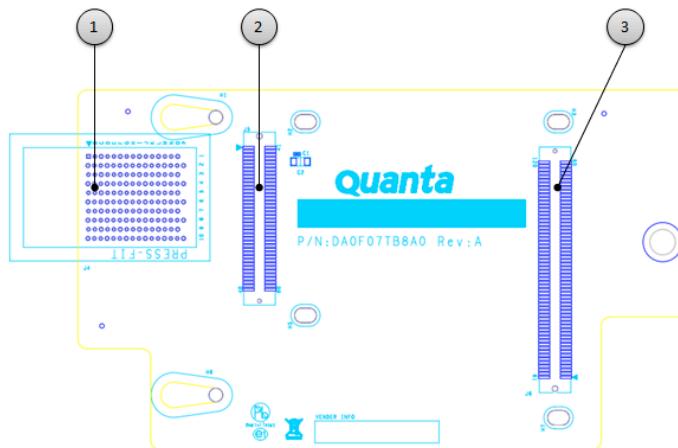
Item	Ref Designator / Silkscreen @PCB	Description	Note
1	J4	Adapter board connector	Match with Side-Plane
2	J5 / Mezz_Conn_B	OCP V2.0 Mezzanine Connector B	
3	J6 / Mezz_Conn_A	OCP V2.0 Mezzanine Connector A	

Figure 14 Adapter board Top overview

➢ 10G-Base KR 40Gb capable PHY mezzanine card – Cortina CS4223
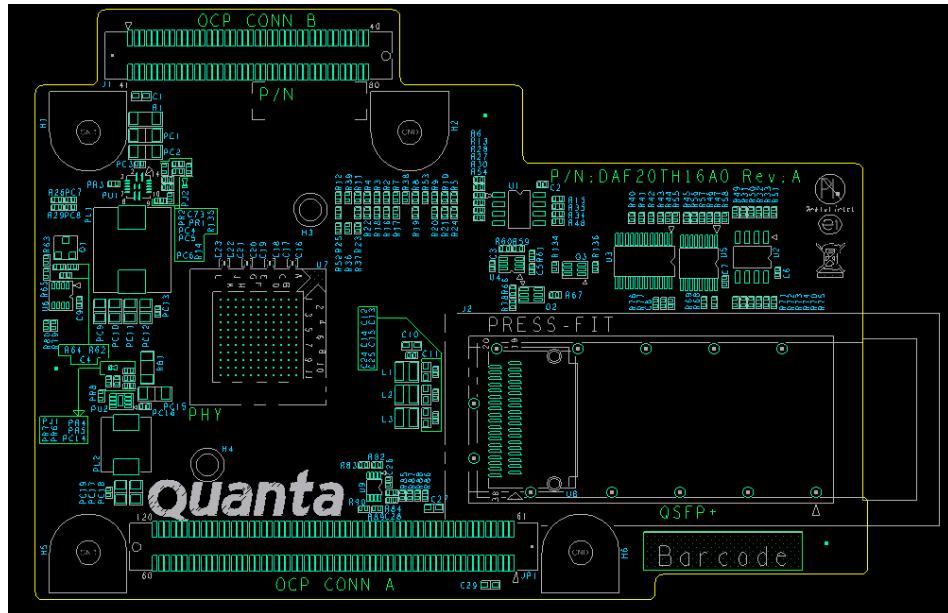
Item	Ref Designator / Silkscreen @PCB	Description	Note

1	J2 / QSFP+	QSFP+ connctor	
2	J1 / OCP CONN B	OCP V2.0 Mezzanine Connector B	
3	JP1 / OCP CONN A	OCP V2.0 Mezzanine Connector A	

Figure 15 PHY mezzanine Cortina CS4223 Top overview

➢ 10G-Base KR 40Gb capable PHY mezzanine card – Semtech GN2407
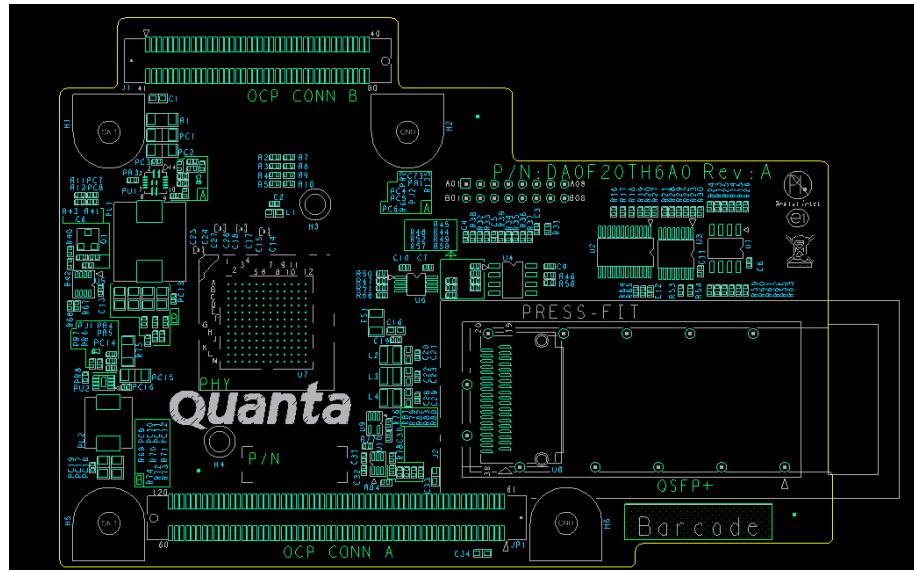
Item	Ref Designator / Silkscreen @PCB	Description	Note
1	J2 / QSFP+	QSFP+ connctor	
2	J1 / OCP CONN B	OCP V2.0 Mezzanine Connector B	
3	JP1 / OCP CONN A	OCP V2.0 Mezzanine Connector A	

Figure 16 PHY mezzanine Semtech GN2407 Top overview

3.2 System board Block Diagram

➢ Yosemite system board Block Diagram
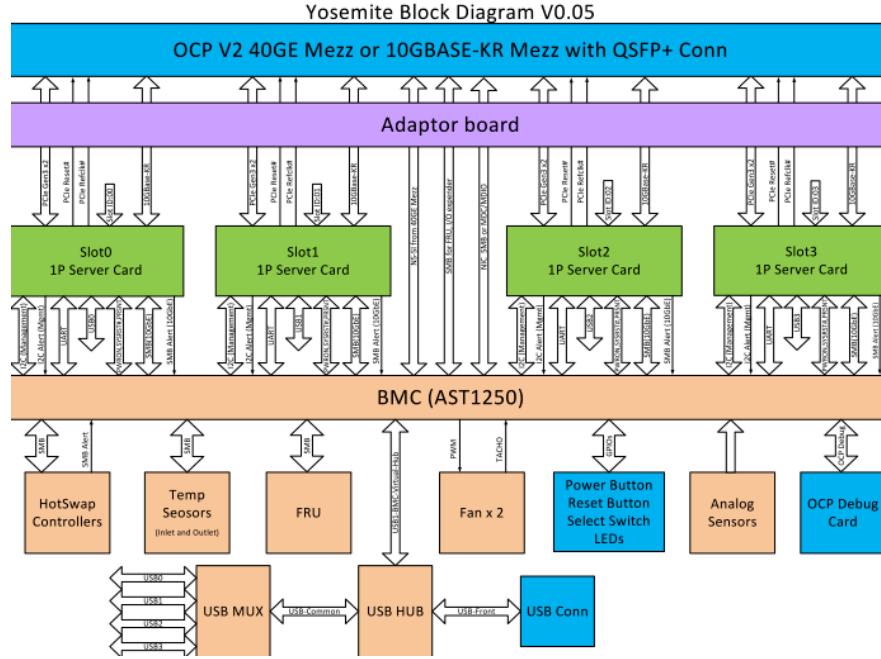
Figure 17   Yosemite system board Block Diagram

➢   10G-Base KR 40Gb capable PHY mezzanine card – Cortina CS4223 Block Diagram
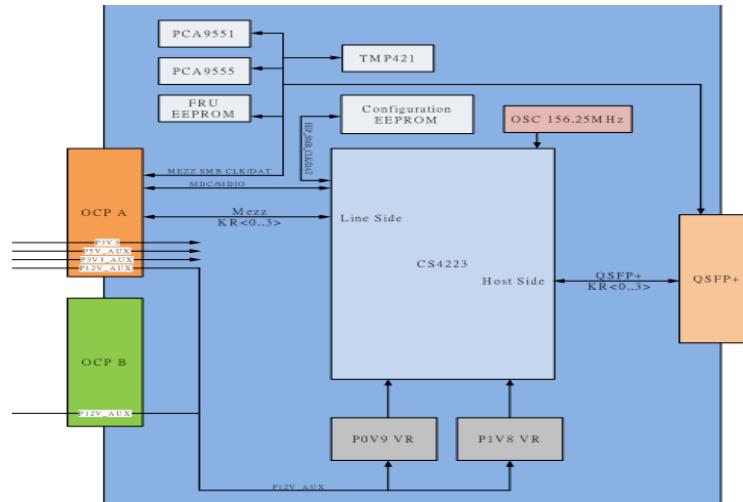
Figure 18   PHY Mezz Cortina CS4223 Block Diagram

➢   10G-Base KR 40Gb capable PHY mezzanine card – Semtech GN2407 Block Diagram
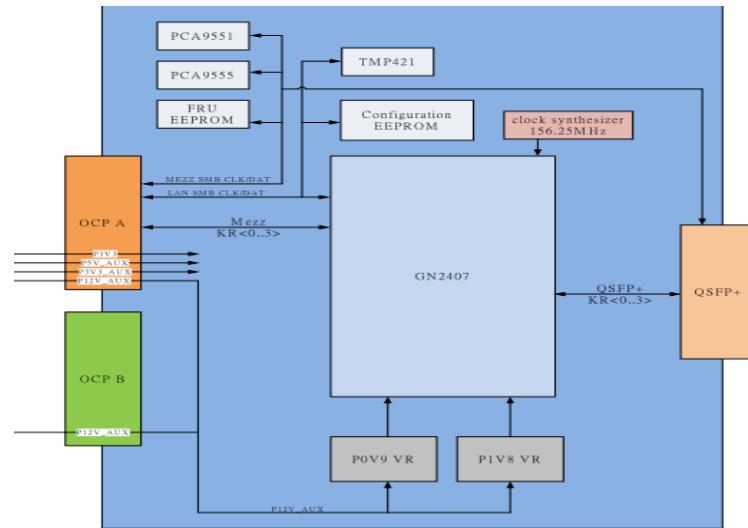
Figure 19   PHY Mezz Semtech GN2407 Block Diagram

3.3 Power Distribution Diagram
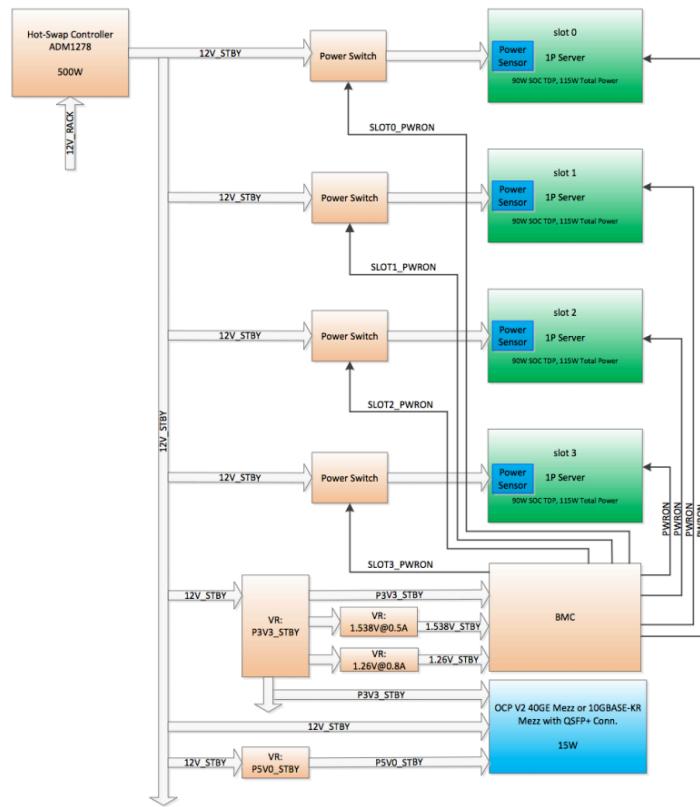
Figure 20   Power Distribution Diagram

3.4 Reset Block Diagram
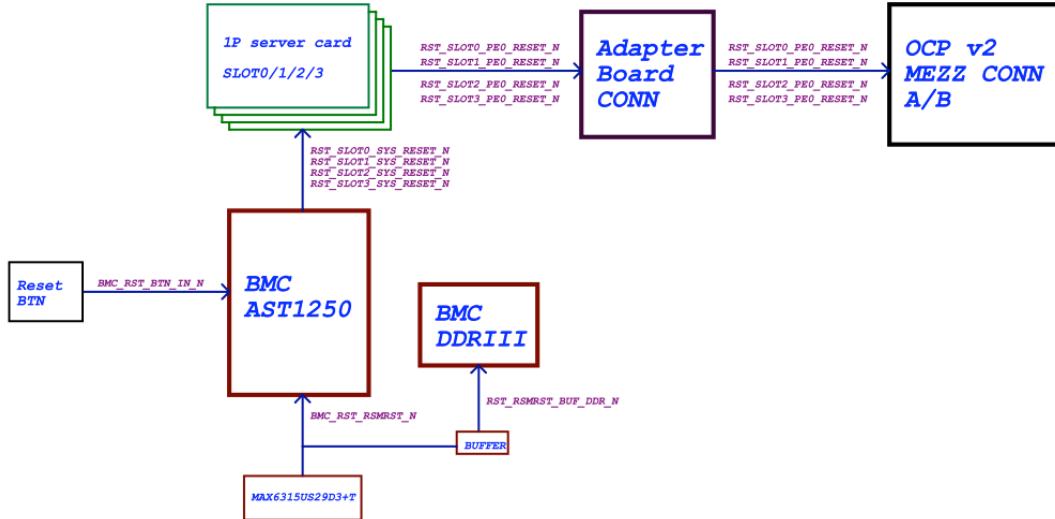
Figure 21   Reset Block Diagram

3.5 SMBUS Block Diagram
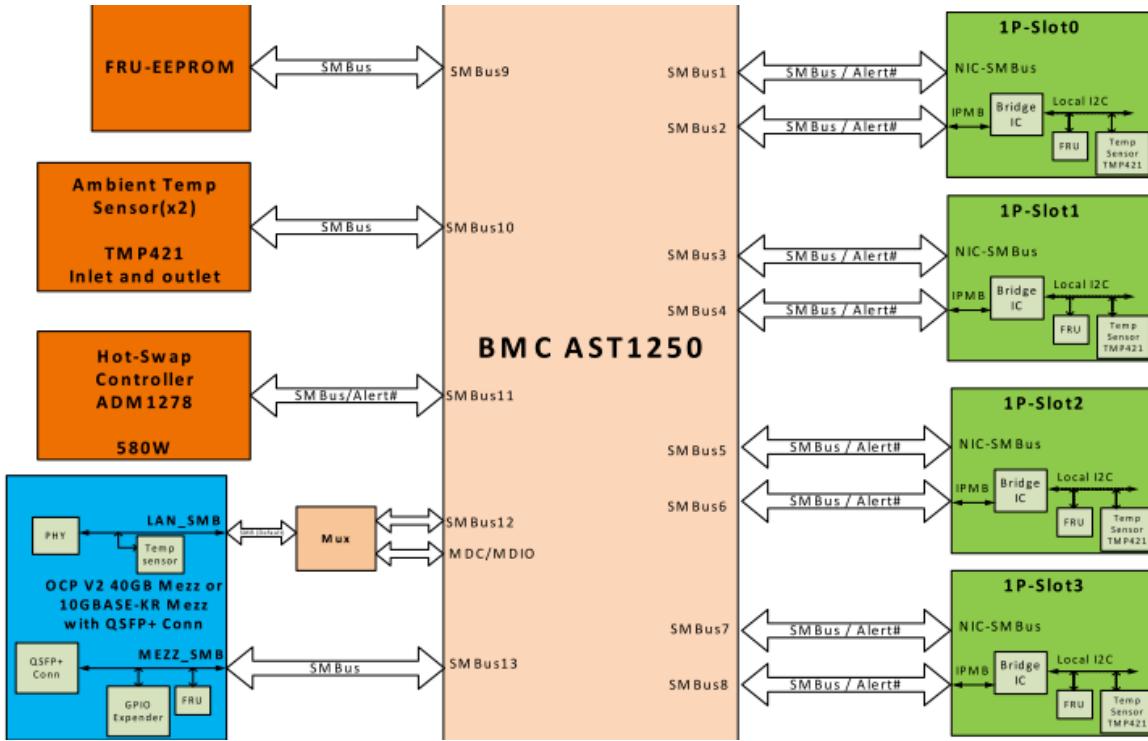
Figure 22   SMBus Block Diagram

3.6 PIO Pin Definitions

➤ **BMC** GPIO Pin Definition:

Pin Number	Pin Name	Net Name	Type	Function Description
D6	GPIOA0_MAC1LINK	NC	Float	N/A
B5	GPIOA1_MAC2LINK	BMC_GPIOA1	PD	PD for BSDL
A4	GPIOA2_TIMER3	BMC_GPIOA2	PU	PU for BSDL
E6	GPIOA3_TIMER4	BMC_GPIOA3	PD	PD for BSDL
C5	GPIOA4_TIMER5_SCL9	SMB_FRU_SCL_R	Out	I2C
B4	GPIOA5_TIMER6_SDA9	SMB_FRU_SDA_R	BI	I2C
A3	GPIOA6_TIMER7_MDC2	PD_BMC_MDC2	PD	MAC2
D5	GPIOA7_TIMER8_MDIO2	PD_BMC_MDIO2	PD	MAC2
J21	GPIOB0_SALT1	SMB_SLOT0_NIC_ALERT_N	In	SMBus Sideband Alert from Node0
J20	GPIOB1_SALT2	SMB_SLOT1_NIC_ALERT_N	In	SMBus Sideband Alert from Node1
H18	GPIOB2_SALT3	SMB_SLOT2_NIC_ALERT_N	In	SMBus Sideband Alert from Node2
F18	GPIOB3_SALT4	SMB_SLOT3_NIC_ALERT_N	In	SMBus Sideband Alert from Node3
E19	GPIOB4_LPCRST#	LED_POSTCODE_4	Out	POST Code LED
H19	GPIOB5_LPCPD#_LPCSMI#	LED_POSTCODE_5	Out	POST Code LED
H20	GPIOB6_LPCPME#	LED_POSTCODE_6	Out	POST Code LED
E18	GPIOB7_EXTRST#_SPICS1#	LED_POSTCODE_7	Out	POST Code LED
C4	GPIOC0_SD1CLK_SCL10	SMB_TEMP_SCL_R	Out	I2C
B3	GPIOC1_SD1CMD_SDA10	SMB_TEMP_SDA_R	BI	I2C
A2	GPIOC2_SD1DAT0_SCL11	SMB_HOTSWAP_SCL_R	Out	I2C
E5	GPIOC3_SD1DAT1_SDA11	SMB_HOTSWAP_SDA_R	BI	I2C
D4	GPIOC4_SD1DAT2_SCL12	SMB_MEZZ_NIC_CLK_R	Out	I2C
C3	GPIOC5_SD1DAT3_SDA12	SMB_MEZZ_NIC_DAT_R	BI	I2C
B2	GPIOC6_SD1CD#_SCL13	SMB_MEZZ_SMCLK_R	Out	I2C
A1	GPIOC7_SD1WP#_SDA13	SMB_MEZZ_SMDATA_R	BI	I2C
A18	GPIOD0_SD2CLK	BMC_PWR_BTN_IN_N	In	From Power Button, low trigger active
D16	GPIOD1_SD2CMD	PWR_SLOT0_BTN_N	Out	Power Button signal to Node0
B17	GPIOD2_SD2DAT0	BMC_PWR_BTN_BUFIN_N	In	From Power Button through buffer, low trigger active
A17	GPIOD3_SD2DAT1	PWR_SLOT1_BTN_N	Out	Power Button signal to Node1
C16	GPIOD4_SD2DAT2	BMC_PWR_BTN_BUFIN_N	In	From Power Button through buffer, low trigger active
B16	GPIOD5_SD2DAT3	PWR_SLOT2_BTN_N	Out	Power Button signal to Node2
A16	GPIOD6_SD2CD#	BMC_PWR_BTN_BUFIN_N	In	From Power Button through buffer, low trigger active
E15	GPIOD7_SD2WP#	PWR_SLOT3_BTN_N	Out	Power Button signal to Node3
D15	GPIOE0_NCTS3	DEBUG_UART_SEL_0	Float	To UART MUX

C15	GPIOE1_NDCD3	DEBUG_UART_SEL_1	Float	To UART MUX
B15	GPIOE2_NDSR3	DEBUG_UART_SEL_2	Float	To UART MUX
A15	GPIOE3_NRI3	DEBUG_UART_RX_SEL_N	Float	To UART MUX
E14	GPIOE4_NDTR3	FM_USB_SW0	Float	To USB MUX
D14	GPIOE5_NRTS3	FM_USB_SW1	Float	To USB MUX
C14	GPIOE6_TXD3	COM_SLOT2_RX_BMC	Out	Node2 UART
B14	GPIOE7_RXD3	COM_SLOT2_TX_BMC	In	Node2 UART
D18	GPIOF0_NCTS4	SYSTEM_ID0_LED_N	Out	Slot system LED, low active
B19	GPIOF1_NDCD4_SIOPBI#	SYSTEM_ID1_LED_N	Out	Slot system LED, low active
A20	GPIOF2_NDSR4_SIOPWRGD	SYSTEM_ID2_LED_N	Out	Slot system LED, low active
D17	GPIOF3_NRI4_SIOPBO#	SYSTEM_ID3_LED_N	Out	Slot system LED, low active
B18	GPIOF4_NDTR4	MEZZ_PRSNTID_A_SEL_N	Out	Default low, assert to high after 4 sec
A19	GPIOF5_NRTS4_SIOSCI#	MEZZ_PRSNTID_B_SEL_N	Out	Default low, assert to high after 4 sec
E16	GPIOF6_TXD4	COM_SLOT3_RX_BMC	Out	Node3 UART
C17	GPIOF7_RXD4	COM_SLOT3_TX_BMC	In	Node3 UART
A14	GPIOG0_SGPSCK	LED_POSTCODE_0	Out	POST Code LED
E13	GPIOG1_SGPSLD	LED_POSTCODE_1	Out	POST Code LED
D13	GPIOG2_SGPSI0	LED_POSTCODE_2	Out	POST Code LED
C13	GPIOG3_SGPSI1	LED_POSTCODE_3	Out	POST Code LED
B13	GPIOG4_WDTRST1_OSCCLK	NC	Float	N/A
Y21	GPIOG5_WDTRST2_USBCKI	NC	Float	N/A
AA22	GPIOG6_FLBUSY#	BMC_READY_N	Out	Enable PWR_LED control, low active
U18	GPIOG7_FLWP#	NC	Float	N/A
A8	GPIOH0_ROMD8_NCTS6	RST_SLOT0_SYS_RESET_N	Out	Reset signal to Node0
C7	GPIOH1_ROMD9_NDCD6	RST_SLOT1_SYS_RESET_N	Out	Reset signal to Node1
B7	GPIOH2_ROMD10_NDSR6	RST_SLOT2_SYS_RESET_N	Out	Reset signal to Node2
A7	GPIOH3_ROMD11_NRI6	RST_SLOT3_SYS_RESET_N	Out	Reset signal to Node3
D7	GPIOH4_ROMD12_NDTR6	SLOT0_PRSNT_N	In	Node0 Present
B6	GPIOH5_ROMD13_NRTS6	SLOT1_PRSNT_N	In	Node1 Present
A6	GPIOH6_ROMD14_TXD6	SLOT2_PRSNT_N	In	Node2 Present
E7	GPIOH7_ROMD15_RXD6	SLOT3_PRSNT_N	In	Node3 Present
C22	GPIOI0_SYSCS#	NC	Float	N/A
G18	GPIOI1_SYSCK	NC	Float	N/A
D19	GPIOI2_SYSDO	NC	Float	N/A
C20	GPIOI3_SYSDI	NC	Float	N/A
B22	GPIOI4_SPICS0#_VBCS#	BMC_THROTTLE_SLOT0_N	Out	BMC throttle
G19	GPIOI5_SPICK_VBCK	BMC_THROTTLE_SLOT1_N	Out	BMC throttle

C18	GPIOI6_SPIDO_VBDO	BMC_THROTTLE_SLOT2_N	Out	BMC throttle
E20	GPIOI7_SPIDI_VBDI	BMC_THROTTLE_SLOT3_N	Out	BMC throttle
J5	GPIOJ0_SGPMCK	OPT_PSU_REDUNDANCY_LOST	In	high is PSU_REDUNDANCY_LOST
J4	GPIOJ1_SGPMLD	OPT_PSU_POWER_FAIL	In	high is PSU_POWER_FAIL
K5	GPIOJ2_SGPMO	NC	Float	N/A
J3	GPIOJ3_SGPMI	NC	Float	N/A
T4	VGAHS_GPIOJ4	NC	Float	N/A
U2	VGAVS_GPIOJ5	NC	Float	N/A
T2	DDCCLK_GPIOJ6	NC	Float	N/A
T1	DDCDAT_GPIOJ7	NC	Float	N/A
E3	GPIOK0_SCL5	SMB_SLOT2_NIC_SCL_R	Out	I2C
D2	GPIOK1_SDA5	SMB_SLOT2_NIC_SDA_R	BI	I2C
C1	GPIOK2_SCL6	I2C_SLOT2_SCL_R	Out	I2C
F4	GPIOK3_SDA6	I2C_SLOT2_SDA_R	BI	I2C
E2	GPIOK4_SCL7	SMB_SLOT3_NIC_SCL_R	Out	I2C
D1	GPIOK5_SDA7	SMB_SLOT3_NIC_SDA_R	BI	I2C
G5	GPIOK6_SCL8	I2C_SLOT3_SCL_R	Out	I2C
F3	GPIOK7_SDA8	I2C_SLOT3_SDA_R	BI	I2C
U1	GPIOL0_NCTS1	MEZZ_PRSNT2_N	In	From OCP Mezz Conn A
T5	GPIOL1_NDCD1_VPIDE	MEZZ_PRSNTB2_N	In	From OCP Mezz Conn B
U3	GPIOL2_NDSR1_VPIODD	LAN_SMB_SELECT_N	Out	Set Low: I2C to Mezz; Set High: MDC/MDIO to Mezz
V1	GPIOL3_NRI1_VPIHS	PCIE_WAKE_N	in	PCIE wake#
U4	GPIOL4_NDTR1_VPIVS	HS0_FAULT_N	In	Hot swap fault
V2	GPIOL5_NRTS1_VPICLK	NC	Float	N/A
W1	GPIOL6_TXD1_VPIB0	COM_SLOT0_RX_BMC	Out	Node0 UART
U5	GPIOL7_RXD1_VPIB1	COM_SLOT0_TX_BMC	In	Node0 UART
V3	GPIOM0_NCTS2_VPIB2	PWR0_LED	Out	Node0 Power/ID LED
W2	GPIOM1_NDCD2_VPIB3	PWR1_LED	Out	Node1 Power/ID LED
Y1	GPIOM2_NDSR2_VPIB4	PWR2_LED	Out	Node2 Power/ID LED
V4	GPIOM3_NRI2_VPIB5	PWR3_LED	Out	Node3 Power/ID LED
W3	GPIOM4_NDTR2_VPIB6	DISABLE_FAN_N	Out	Disable FAN power
Y2	GPIOM5_NRTS2_VPIB7	NC	Float	N/A
AA1	GPIOM6_TXD2_VPIB8	COM_SLOT1_RX_BMC	Out	Node1 UART
V5	GPIOM7_RXD2_VPIB9	COM_SLOT1_TX_BMC	In	Node1 UART
W4	GPION0_PWM0_VPIG0	FAN_PWM_A	Out	PWM
Y3	GPION1_PWM1_VPIG1	FAN_PWM_B	Out	PWM
AA2	GPION2_PWM2_VPIG2	I2C_SLOT0_ALERT_N	In	SMBus Alert from Node0
AB1	GPION3_PWM3_VPIG3	I2C_SLOT1_ALERT_N	In	SMBus Alert from Node1

W5	GPION4_PWM4_VPIG4	I2C_SLOT2_ALERT_N	In	SMBus Alert from Node2
Y4	GPION5_PWM5_VPIG5	I2C_SLOT3_ALERT_N	In	SMBus Alert from Node3
AA3	GPION6_PWM6_VPIG6	LAN_3V3STB_ALERT_N	In	From OCP Mezz Conn A
AB2	GPION7_PWM7_VPIG7	SMB_HOTSWAP_ALERT_N	In	Form ADM1278
V6	GPIOO0_TACH0_VPIG8	FAN_TACH1	In	TACH
Y5	GPIOO1_TACH1_VPIG9	FAN_TACH2	In	TACH
AA4	GPIOO2_TACH2_VPIR0	FAN_TACH3	In	TACH
AB3	GPIOO3_TACH3_VPIR1	FAN_TACH4	In	TACH
W6	GPIOO4_TACH4_VPIR2	P12V_STBY_SLOT0_EN	Out	Set Low to disable Node0 power SW
AA5	GPIOO5_TACH5_VPIR3	P12V_STBY_SLOT1_EN	Out	Set Low to disable Node1 power SW
AB4	GPIOO6_TACH6_VPIR4	P12V_STBY_SLOT2_EN	Out	Set Low to disable Node2 power SW
V7	GPIOO7_TACH7_VPIR5	P12V_STBY_SLOT3_EN	Out	Set Low to disable Node3 power SW
Y6	GPIOP0_TACH8_VPIR6	PWRGD_P12V_STBY_SLOT0	In	Node0 power SW Power Good
AB5	GPIOP1_TACH9_VPIR7	PWRGD_P12V_STBY_SLOT1	In	Node1 power SW Power Good
W7	GPIOP2_TACH10_VPIR8	PWRGD_P12V_STBY_SLOT2	In	Node2 power SW Power Good
AA6	GPIOP3_TACH11_VPIR9	PWRGD_P12V_STBY_SLOT3	In	Node3 power SW Power Good
AB6	GPIOP4_TACH12	NC	Float	N/A
Y7	GPIOP5_TACH13	NC	Float	N/A
AA7	GPIOP6_TACH14_BMCINT	NC	Float	N/A
AB7	GPIOP7_TACH15_FLACK	NC	Float	N/A
D3	GPIOQ0_SCL3	SMB_SLOT1_NIC_SCL_R	Out	I2C
C2	GPIOQ1_SDA3	SMB_SLOT1_NIC_SDA_R	BI	I2C
B1	GPIOQ2_SCL4	I2C_SLOT1_SCL_R	Out	I2C
F5	GPIOQ3_SDA4	I2C_SLOT1_SDA_R	BI	I2C
H4	GPIOQ4_SCL14	PU_BMC_SCL14	PU	
H3	GPIOQ5_SDA14	PU_BMC_SDA14	PU	
H2	GPIOQ6	USB_OC_N	In	Indicate USB Over Current
H1	GPIOQ7	BMC_HEARTBEAT_N	Out	BMC Heartbeat LED
V20	GPIOR0_ROMCS1#	SPI_IBMC_BT_CS1_R_N	Out	SPI chip select 1
W21	GPIOR1_ROMCS2#	DEBUG_PORT_UART_SEL_BMC_N	In	From Debug Board
Y22	GPIOR2_ROMCS3#	HAND_SW_ID1	In	From select swtich
U19	GPIOR3_ROMCS4#	HAND_SW_ID2	In	From select swtich
V21	GPIOR4_ROMA24_VPOR6	HAND_SW_ID4	In	From select swtich
W22	GPIOR5_ROMA25_VPOR7	HAND_SW_ID8	In	From select swtich
C6	GPIOR6_MDC1	RMII_PHY_MDC_R	Out	MAC1

A5	GPIOR7_MDIO1	RMII_PHY_MDIO_R	BI	MAC1
U21	ROMD4_GPIOS0_VPODE	BMC_RST_BTN_IN_N	In	From Reset Button, low trigger active
T19	ROMD5_GPIOS1_VPOHS	P3V3_EN	Out	Enable P3V3 power switch
V22	ROMD6_GPIOS2_VPOVS	PWRGD_P3V3	In	P3V3 power good
U20	ROMD7_GPIOS3_VPOCLK	USB_MUX_EN_N	Out	USB mux enable
R18	ROMOE#_GPIOS4	FAST_PROCHOT_EN	Out	To FAST PROCHOT CURRENT circuit
N21	ROMWE#_GPIOS5	FAST_PROCHOT_N	In	Hot swap current over 40.6A
L22	ROMA22_GPIOS6_VPOR4	ROMA<22>	Float	Hardware Trapping
K18	ROMA23_GPIOS7_VPOR5	ROMA<23>	Float	Hardware Trapping
A12	RGMII1TXCK_RMII1TXEN_GPIOT0	BMC_NCSI_RMII_TX_EN_R	Out	MAC1
B12	RGMII1TXCTL_GPIOT1	NC	Float	MAC1
C12	RGMII1TXD0_RMII1TXD0_GPIOT2	BMC_NCSI_RMII_TXD_0_R	Out	MAC1
D12	RGMII1TXD1_RMII1TXD1_GPIOT3	BMC_NCSI_RMII_TXD_1_R	Out	MAC1
E12	RGMII1TXD2_GPIOT4	NC	Float	MAC1
A13	RGMII1TXD3_GPIOT5	NC	Float	MAC1
D9	RGMII2TXCK_RMII2TXEN_GPIOT6	NC	Float	MAC2
E9	RGMII2TXCTL_GPIOT7	NC	Float	MAC2
A10	RGMII2TXD0_RMII2TXD0_GPIOU0	NC	Float	MAC2
B10	RGMII2TXD1_RMII2TXD1_GPIOU1	NC	Float	MAC2
C10	RGMII2TXD2_GPIOU2	NC	Float	MAC2
D10	RGMII2TXD3_GPIOU3	NC	Float	MAC2
E11	RGMII1RXCK_RMII1RCLK_GPIOU4	REFCLK_50MHz_RMII_BMC_MAC1	In	MAC1
D11	RGMII1RXCTL_GPIOU5	BMC_RGMII_D11_B9_B8	PD	MAC1
C11	RGMII1RXD0_RMII1RXD0_GPIOU6	BMC_NCSI_RMII_RXD_0	In	MAC1
B11	RGMII1RXD1_RMII1RXD1_GPIOU7	BMC_NCSI_RMII_RXD_1	In	MAC1
A11	RGMII1RXD2_RMII1CRSDV_GPIOV0	BMC_NCSI_RMII_CSR_DV	In	MAC1
E10	RGMII1RXD3_RMII1RXER_GPIOV1	BMC_NCSI_RMII_RX_ER	In	MAC1
C9	RGMII2RXCK_RMII2RCLK_GPIOV2	NC	Float	MAC2
B9	RGMII2RXCTL_GPIOV3	BMC_RGMII_D11_B9_B8	PD	MAC2
A9	RGMII2RXD0_RMII2RXD0_GPIOV4	NC	Float	MAC2
E8	RGMII2RXD1_RMII2RXD1_GPIOV5	NC	Float	MAC2
D8	RGMII2RXD2_RMII2CRSDV_GPIOV6	NC	Float	MAC2
C8	RGMII2RXD3_RMII2RXER_GPIOV7	NC	Float	MAC2
L5	ADC0_GPIW0	P5V_STBY_SCALED	In	ADC
L4	ADC1_GPIW1	P12V_STBY_SCALED	In	ADC
L3	ADC2_GPIW2	P3V3_STBY_SCALED	In	ADC
L2	ADC3_GPIW3	P12V_STBY_SLOT0_SCALED	In	ADC
L1	ADC4_GPIW4	P12V_STBY_SLOT1_SCALED	In	ADC

M5	ADC5_GPIW5	P12V_STBY_SLOT2_SCALED	In	ADC
M4	ADC6_GPIW6	P12V_STBY_SLOT3_SCALED	In	ADC
M3	ADC7_GPIW7	P3V3_SCALED	In	ADC
M2	ADC8_GPIX0	PD	In	ADC
M1	ADC9_GPIX1	PD	In	ADC
N5	ADC10_GPIX2	PD	In	ADC
N4	ADC11_GPIX3	PD	In	ADC
N3	ADC12_GPIX4	PD	In	ADC
N2	ADC13_GPIX5	PD	In	ADC
N1	ADC14_GPIX6	PD	In	ADC
P5	ADC15_GPIX7	PD	In	ADC
C21	GPIOY0_SIOS3#	BOARD_REV_ID0	In	Board Revision ID
F20	GPIOY1_SIOS5#	BOARD_REV_ID1	In	Board Revision ID
G20	GPIOY2_SIOPWREQ#	BOARD_REV_ID2	In	Board Revision ID
K20	GPIOY3_SIOONCTRL#	BOARD_ID	In	0= sideplane, 1=test board
R22	ROMA2_GPIOZ0_VPOB0	ROMA<2>	Float	Hardware Trapping
P18	ROMA3_GPIOZ1_VPOB1	ROMA<3>	Float	Hardware Trapping
P19	ROMA4_GPIOZ2_VPOB2	ROMA<4>	Float	Hardware Trapping
P20	ROMA5_GPIOZ3_VPOB3	ROMA<5>	Float	Hardware Trapping
P21	ROMA6_GPIOZ4_VPOB4	ROMA<6>	Float	Hardware Trapping
P22	ROMA7_GPIOZ5_VPOB5	ROMA<7>	Float	Hardware Trapping
M19	ROMA8_GPIOZ6_VPOB6	ROMA<8>	PU	Hardware Trapping
M20	ROMA9_GPIOZ7_VPOB7	ROMA<9>	Float	Hardware Trapping
M21	ROMA10_GPIOAA0_VPOG0	ROMA<10>	PU	Hardware Trapping
M22	ROMA11_GPIOAA1_VPOG1	ROMA<11>	Float	Hardware Trapping
L18	ROMA12_GPIOAA2_VPOG2	ROMA<12>	Float	Hardware Trapping
L19	ROMA13_GPIOAA3_VPOG3	ROMA<13>	Float	Hardware Trapping
L20	ROMA14_GPIOAA4_VPOG4	ROMA<14>	Float	Hardware Trapping
L21	ROMA15_GPIOAA5_VPOG5	ROMA<15>	Float	Hardware Trapping
T18	ROMA16_GPIOAA6_VPOG6	ROMA<16>	Float	Hardware Trapping
N18	ROMA17_GPIOAA7_VPOG7	ROMA<17>	PU	Hardware Trapping
N19	ROMA18_GPIOAB0_VPOR0	ROMA<18>	Float	Hardware Trapping
M18	ROMA19_GPIOAB1_VPOR1	ROMA<19>	PU	Hardware Trapping
N22	ROMA20_GPIOAB2_VPOR2	ROMA<20>	Float	Hardware Trapping
N20	ROMA21_GPIOAB3_VPOR3	ROMA<21>	Float	Hardware Trapping

3.7 Baseboard Power Consumption

	With OCP MEZZ CARD
Baseboard Power Consumption	<60W

3.8 Connectors Pin Definitions

3.8.1   1P server card Primary x16 OCP connector *Pin Definition*

Pin Name	Side B	Side A	Pin Name
P12V	1	1	PRSNT#
P12V	2	2	P12V
P12V	3	3	P12V
GND	4	4	GND
I2C_SCL	5	5	SVR_ID0/GPIO0
I2C_DATA	6	6	SVR_ID1/GPIO1
GND	7	7	COM_TX
PWR_BTN#	8	8	COM_RX
USB_P	9	9	SVR_ID2/GPIO2
USB_N	10	10	SVR_ID3/GPIO3
SYS_RESET#	11	11	PCIE_RESET#
I2C_ALERT#	12	12	GND
GND	13	13	PCIE0_REFCLK_P
GND	14	14	PCIE0_REFCLK_N
PCIE0_TX0_P	15	15	GND
PCIE0_TX0_N	16	16	GND
GND	17	17	PCIE0_RX0_P
GND	18	18	PCIE0_RX0_N
PCIE0_TX1_P	19	19	GND
PCIE0_TX1_N	20	20	GND
GND	21	21	PCIE0_RX1_P
GND	22	22	PCIE0_RX1_N
PCIE0_TX2_P	23	23	GND
PCIE0_TX2_N	24	24	GND
GND	25	25	PCIE0_RX2_P
GND	26	26	PCIE0_RX2_N
PCIE0_TX3_P	27	27	GND
PCIE0_TX3_N	28	28	GND
GND	29	29	PCIE0_RX3_P
GND	30	30	PCIE0_RX3_N
SATA0_TX_P	31	31	GND
SATA0_TX_N	32	32	GND
GND	33	33	SATA0_RX_P
GND	34	34	SATA0_RX_N
PCIE1_REFCLK_P	35	35	GND
PCIE1_REFCLK_N	36	36	GND
GND	37	37	PCIE2_REFCLK_P
GND	38	38	PCIE2_REFCLK_N
PCIE1_RESET#	39	39	GND
PCIE2_RESET#	40	40	GND
GND	41	41	FAST_THROTTLE_N
GND	42	42	NIC_SMBUS_ALERT#
NIC_SMBUS_SCL	43	43	GND

NIC_SMBUS_SDA	44	44	GND
GND	45	45	GE0_RX_P
GND	46	46	GE0_RX_N
GE0_TX_P	47	47	GND
GE0_TX_N	48	48	GND
GND	49	49	PCIE1_RX0_P
GND	50	50	PCIE1_RX0_N
PCIE1_TX0_P	51	51	GND
PCIE1_TX0_N	52	52	GND
GND	53	53	PCIE1_RX1_P
GND	54	54	PCIE1_RX1_N
PCIE1_RX1_P	55	55	GND
PCIE1_RX1_N	56	56	GND
GND	57	57	PCIE1_RX2_P
GND	58	58	PCIE1_RX2_N
PCIE1_TX2_P	59	59	GND
PCIE1_TX2_N	60	60	GND
GND	61	61	PCIE1_RX3_P
GND	62	62	PCIE1_RX3_N
PCIE1_TX3_P	63	63	GND
PCIE1_TX3_N	64	64	GND
GND	65	65	PCIE2_RX0_P
GND	66	66	PCIE2_RX0_N
PCIE2_TX0_P	67	67	GND
PCIE2_TX0_N	68	68	GND
GND	69	69	PCIE2_RX1_P
GND	70	70	PCIE2_RX1_N
PCIE2_RX1_P	71	71	GND
PCIE2_RX1_N	72	72	GND
GND	73	73	PCIE2_RX2_P
GND	74	74	PCIE2_RX2_N
PCIE2_TX2_P	75	75	GND
PCIE2_TX2_N	76	76	GND
GND	77	77	PCIE2_RX3_P
GND	78	78	PCIE2_RX3_N
PCIE2_TX3_P	79	79	GND
PCIE2_TX3_N	80	80	GND
GND	81	81	P12V
GND	82	82	P12V

Table 16 1P server card Primary x16 OCP Connector Pin Definition

3.8.2 10G Mezzanine Connector

OCP Connect A : J6			
Net Name	Pin#	Pin#	Net Name
P12V_STBY	61	1	MEZZ_PRSNTA1_N
P12V_STBY	62	2	P5V_STBY
P12V_STBY	63	3	P5V_STBY
GND	64	4	P5V_STBY
GND	65	5	GND

P3V3_STBY	66	6	GND
GND	67	7	P3V3_STBY
GND	68	8	GND
P3V3	69	9	GND
P3V3	70	10	P3V3
P3V3	71	11	P3V3
P3V3	72	12	P3V3
GND	73	13	P3V3
LAN_3V3STB_ALERT_N	74	14	BMC_NCSI_RMII_CSR_DV
SMB_MEZZ_NIC_CLK_MDC	75	15	REFCLK_50MHZ_RMII_MEZZ
SMB_MEZZ_NIC_DAT_MDIO	76	16	BMC_NCSI_RMII_TX_EN
PCIE_WAKE_N	77	17	RST_PE_SLOT1_0_RESET_N
BMC_NCSI_RMII_RX_ER	78	18	SMB_MEZZ_SMCLK
GND	79	19	SMB_MEZZ_SMDATA
BMC_NCSI_RMII_TXD_0	80	20	GND
BMC_NCSI_RMII_TXD_1	81	21	GND
GND	82	22	BMC_NCSI_RMII_RXD_0
GND	83	23	BMC_NCSI_RMII_RXD_1
CLK_PE_SLOT1_0_REFCLK_P	84	24	GND
CLK_PE_SLOT1_0_REFCLK_N	85	25	GND
GND	86	26	CLK_PE_SLOT2_0_REFCLK_P
GND	87	27	CLK_PE_SLOT2_0_REFCLK_N
PE_SLOT1_0_TX0_P	88	28	GND
PE_SLOT1_0_TX0_N	89	29	GND
GND	90	30	PE_SLOT1_0_RX0_P
GND	91	31	PE_SLOT1_0_RX0_N
PE_SLOT1_0_TX1_P	92	32	GND
PE_SLOT1_0_TX1_N	93	33	GND
GND	94	34	PE_SLOT1_0_RX1_P
GND	95	35	PE_SLOT1_0_RX1_N
PE_SLOT2_0_TX0_P	96	36	GND
PE_SLOT2_0_TX0_N	97	37	GND
GND	98	38	PE_SLOT2_0_RX0_P
GND	99	39	PE_SLOT2_0_RX0_N
PE_SLOT2_0_TX1_P	100	40	GND
PE_SLOT2_0_TX1_N	101	41	GND
GND	102	42	PE_SLOT2_0_RX1_P
GND	103	43	PE_SLOT2_0_RX1_N
PE_SLOT3_0_TX0_P	104	44	GND

Net Name	Pin#	Pin#	Net Name
PE_SLOT3_0_TX0_N	105	45	GND
GND	106	46	PE_SLOT3_0_RX0_P
GND	107	47	PE_SLOT3_0_RX0_N
PE_SLOT3_0_TX1_P	108	48	GND
PE_SLOT3_0_TX1_N	109	49	GND
GND	110	50	PE_SLOT3_0_RX1_P
GND	111	51	PE_SLOT3_0_RX1_N
PE_SLOT4_0_TX0_P	112	52	GND
PE_SLOT4_0_TX0_N	113	53	GND
GND	114	54	PE_SLOT4_0_RX0_P
GND	115	55	PE_SLOT4_0_RX0_N
PE_SLOT4_0_TX1_P	116	56	GND
PE_SLOT4_0_TX1_N	117	57	GND
GND	118	58	PE_SLOT4_0_RX1_P
GND	119	59	PE_SLOT4_0_RX1_N
MEZZ_PRSNTA2_IN_N	120	60	GND

OCP Connect B : J5			
Net Name	Pin#	Pin#	Net Name
P12V_STBY	41	1	MEZZ_PRSNTB1_N
P12V_STBY	42	2	GND
NC	43	3	KR_SLOT1_RX0_P
GND	44	4	KR_SLOT1_RX0_N
KR_SLOT1_TX0_P	45	5	GND
KR_SLOT1_TX0_N	46	6	GND
GND	47	7	KR_SLOT2_RX0_P
GND	48	8	KR_SLOT2_RX0_N
KR_SLOT2_TX0_P	49	9	GND
KR_SLOT2_TX0_N	50	10	GND
GND	51	11	KR_SLOT3_RX0_P
GND	52	12	KR_SLOT3_RX0_N
KR_SLOT3_TX0_P	53	13	GND
KR_SLOT3_TX0_N	54	14	GND
GND	55	15	KR_SLOT4_RX0_P
GND	56	16	KR_SLOT4_RX0_N
KR_SLOT4_TX0_P	57	17	GND
KR_SLOT4_TX0_N	58	18	GND
GND	59	19	NC

GND	60	20	NC
NC	61	21	GND
NC	62	22	GND
GND	63	23	NC
GND	64	24	NC
NC	65	25	GND
NC	66	26	GND
GND	67	27	NC
GND	68	28	NC
NC	69	29	GND
NC	70	30	GND
GND	71	31	NC
GND	72	32	NC
NC	73	33	GND
NC	74	34	GND
GND	75	35	CLK_PE_SLOT3_0_REFCLK_P
GND	76	36	CLK_PE_SLOT3_0_REFCLK_N
CLK_PE_SLOT4_0_REFCLK_P	77	37	GND
CLK_PE_SLOT4_0_REFCLK_N	78	38	RST_PE_SLOT2_0_RESET_N
GND	79	39	RST_PE_SLOT3_0_RESET_N
MEZZ_PRSNTB2_IN_N	80	40	RST_PE_SLOT4_0_RESET_N

Table 17 10G Mezzanine Connector on Adaptor board

3.8.3   OCP Debug Card Connector

Pin#	Pin Name
1	Low HEX Character [0] least significant bit
2	Low HEX Character [1]
3	Low HEX Character [2]
4	Low HEX Character [3] most significant bit
5	High HEX Character [0] least significant bit
6	High HEX Character [1]
7	High HEX Character [1]
8	High HEX Character [3] most significant bit
9	Serial Transmit
10	Serial Receive
11	System Reset
12	UART Channel Selection
13	GND
14	VCC (5VDC)

Table18 OCP Debug Card Connector Pin Definition

3.9 Buttons, Selector and Jumpers

3.9.1   Power and Reset Buttons

There are two push buttons for system Power and Reset separately. Please refer to '**2.1   Outline and Placement**' for the placement.

3.9.2   Selector Switch

A rotary selector switch can select the current or active 1P server that is connected to the debug header, USB mux, serial mux, and power and reset buttons. LED 1-4 are used to indicate which 1P server is the current or active one.

For the LED's behavior, please refer to " 4.10.1 Power & System Identify LED (LED 1-4)".

Position	Server	LED
1	Slot 1	LED1
2	Slot 2	LED2
3	Slot 3	LED3
4	Slot 4	LED4
5	BMC	LED1-4 blinking with 1Hz
6	Slot 1	LED1
7	Slot 2	LED2
8	Slot 3	LED3
9	Slot 4	LED4
10	BMC	LED1-4 blinking with 1Hz

Table 19 Rotary Selector Switch Description

3.9.3   OCP select Jumper (JP1)

The Jumper is select hot swap controller over current protect setting.

Description	Jumper Status	Note
Select 41.4A	1-2	
Select 48.8A	2-3	Default

Table 20 MFG mode selection Jumper description

3.9.4   BMC Disable Jumper (J18)

The Jumper purposes to disable BMC function, and it is for debug only.

Description	Jumper Status	Note

BMC Enable	Open	Default
BMC Disable	Short	

Table 21 BMC Disable Jumper Description

3.10 LED Definition

3.10.1 Power & System Identify LED (LED 1-4)

Yosemite combines Power LED and System Identification LED to a single bicolor blue-yellow LED per 1P server. Total 4 LEDs place along at the front edge of the side-plane.

The Table summarizes the power and systems identify LED behaviors.

Power and System Identify	LED 1-4
Yosemite Sled is identified	All 4 Yellow LEDs blink in 2.5Hz (200ms on, 200ms off), and loop; all Blue LEDs off.
Slot is identified	Yellow LED blink in 2.5 Hz (200ms on, 200ms off), and loop; Blue LED off.
Rotary switch is turned to BMC position	All 4 Blue LEDs blink in 1Hz (500ms on, 500ms off), and loop; all Yellow LEDs off.
Power off, Slot is selected by switch, status good	Blue LED 100ms on, 900ms off, and loop.
Power on, Slot is not selected by switch, status good	LED consistently Blue
Power on, Slot is selected by switch, status good	Blue LED 900ms on, 100ms off, and loop.
Power off, Slot is selected by switch, status bad	Yellow LED 100ms on, 900ms off, and loop.
Power on, Slot is not selected by switch, status bad	LED consistently Yellow
Power on, Slot is selected by switch, status bad	Yellow LED 900ms on, 100ms off, and loop.

Table 22 Power & System Identify LED Description

### 3.10.2 BMC Heartbeat LED (D15)

There is a green color LED for heartbeat near BMC chip. It provides an easy way to know that BMC is working for external world.

LED Status	LED COLOR	Description
OFF	N/A	BMC is not ready
ON	Green	Entry into Boot Code
Blink	Green	BMC has already begun to work normally.

Table 23 BMC HB LED Description

3.10.3 OCP Mezzanine card LEDs

Follow "OCP Mezzanine card 2.0 Design Specification".
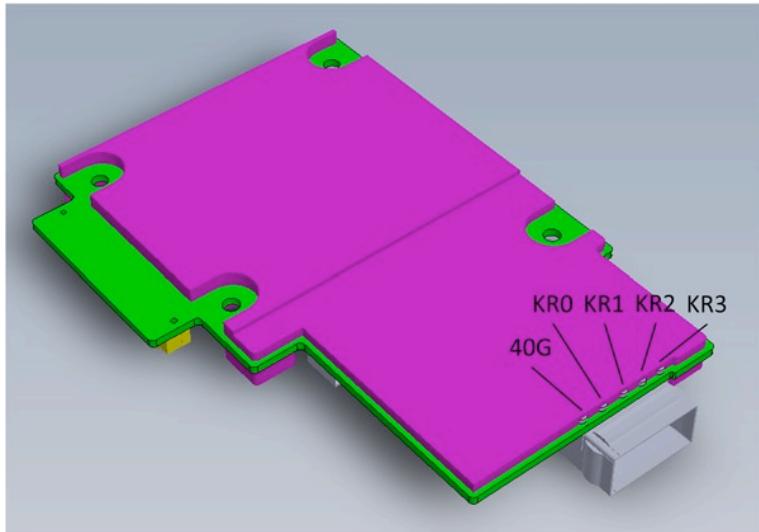
KR0/KR1/KR2/KR3 LED (Green):

Off-   No link

On-   Link as one 10G port

Blink-   Link as one 10G port with activity

40G LED(Green):

Off-   No link

On-   Link as one 40G port

Blink-   Link as one 40G port with activity

3.11   Board Variations

N/A

3.12   Appendix for Baseboard

N/A

4. OS Support

  Motherboard shall support CentOS 6.4 with updated FBK, and pass RedHat certification tests. The OS and FBK version support will be updated once customer has request.

5. Environmental Requirements

The Motherboard (Mono Lake) shall meet the following environmental requirements:

• Gaseous contamination: Severity Level G1 per ANSI/ISA 71.04-1985

• Ambient operating temperature range: -5°C to +45°C

• Operating and storage relative humidity: 10% to 90% (non-condensing)

• Storage temperature range: -40°C to +70°C

• Transportation temperature range: -55°C to +85°C (short-term storage)

The full system shall meet the following environmental requirements:

• Gaseous contamination: Severity Level G1 per ANSI/ISA 71.04-1985

• Ambient operating temperature range: -5°C to +35°C

• Operating and storage relative humidity: 10% to 90% (non-condensing)

• Storage temperature range: -40°C to +70°C

• Transportation temperature range: -55°C to +85°C (short-term storage)

• Operating altitude with no de- ratings: 1000m (3300 feet)

6. Vibration and Shock

The motherboard shall meet shack and vibration requirements according to following IEC specifications: IEC78-2-(*) & IEC721-3-(*) Standard & Levels. The testing requirements are listed in Table .

	Operating	**Non-Operating**
Vibration	0.5g acceleration, 1.5mm amplitude, 5 to 500 Hz, 10 sweeps at 1 octave/minute per each of the three axes (one sweep is 5 to 500 to 5 Hz)	1g acceleration, 3mm amplitude, 5 to 500 Hz, 10 sweeps at 1 octave/minute per each of the three axes (one sweep is 5 to 500 to 5 Hz)
Shock	6g, half-sine 11mS, 5 shocks per each of the three axes	12g, half-sine 11mS, 10 shocks per each of the three axes

Table 24 Vibration and Shock Requirements

7. MTBF Requirements

The motherboard shall have a minimum calculated MTBF of 300,000 hours at 90% confidence level at 45°C ambient temperature. The system shall also demonstrate the MTBF requirement above by running at full load and 50% of time and performing AC cycling test 50% of time at 45C. The system shall have a minimum service life of 5 years (24 hours/day, full load, at 45°C ambient temperature)