

Mono Lake M/B

COVER PAGE

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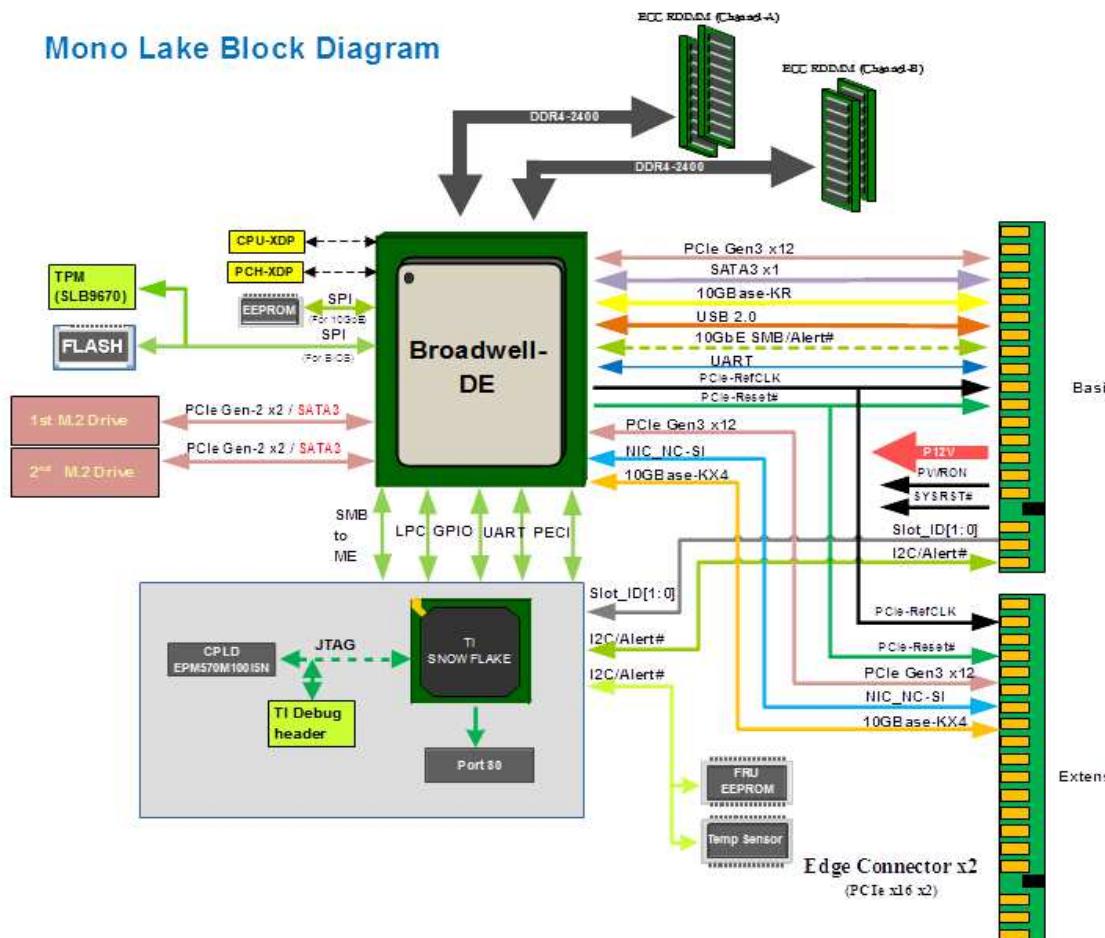
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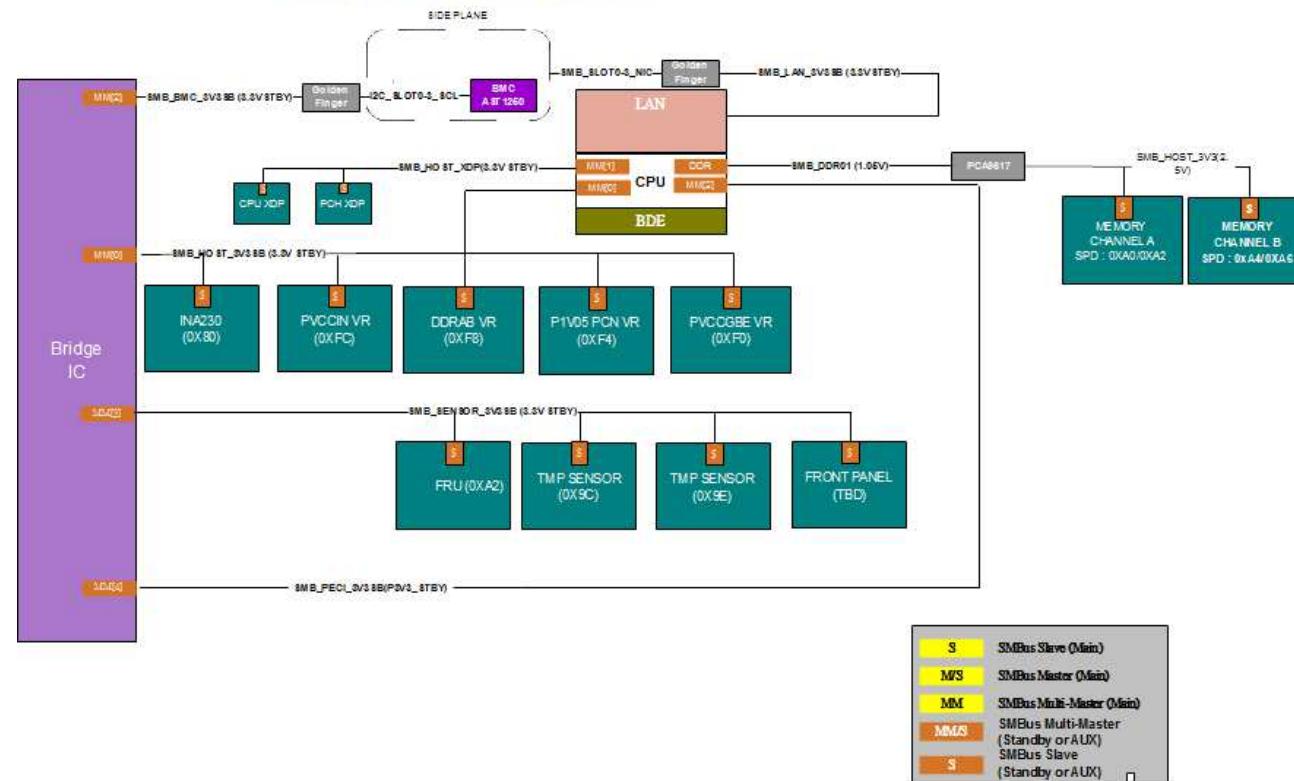
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Mono Lake Block Diagram



Mono Lake SMBus Block Diagram



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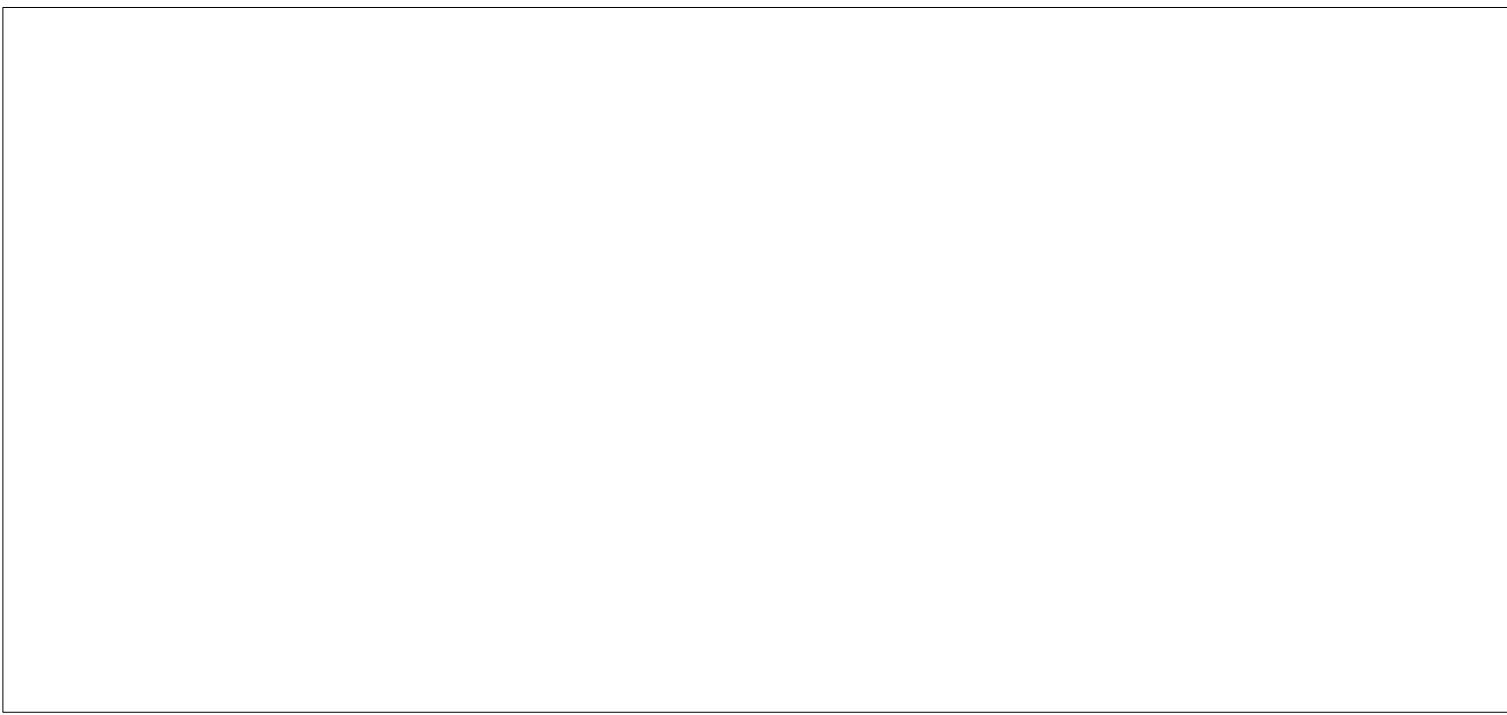
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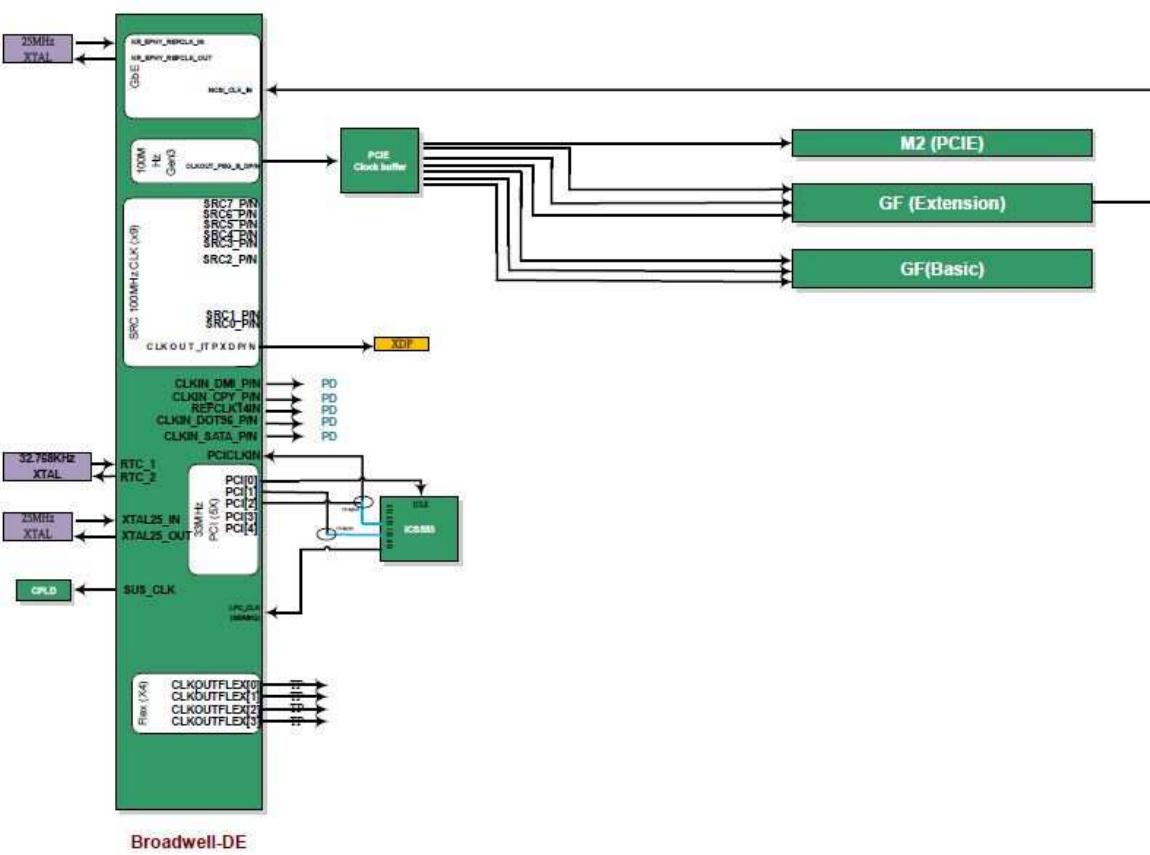
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Clock Diagram

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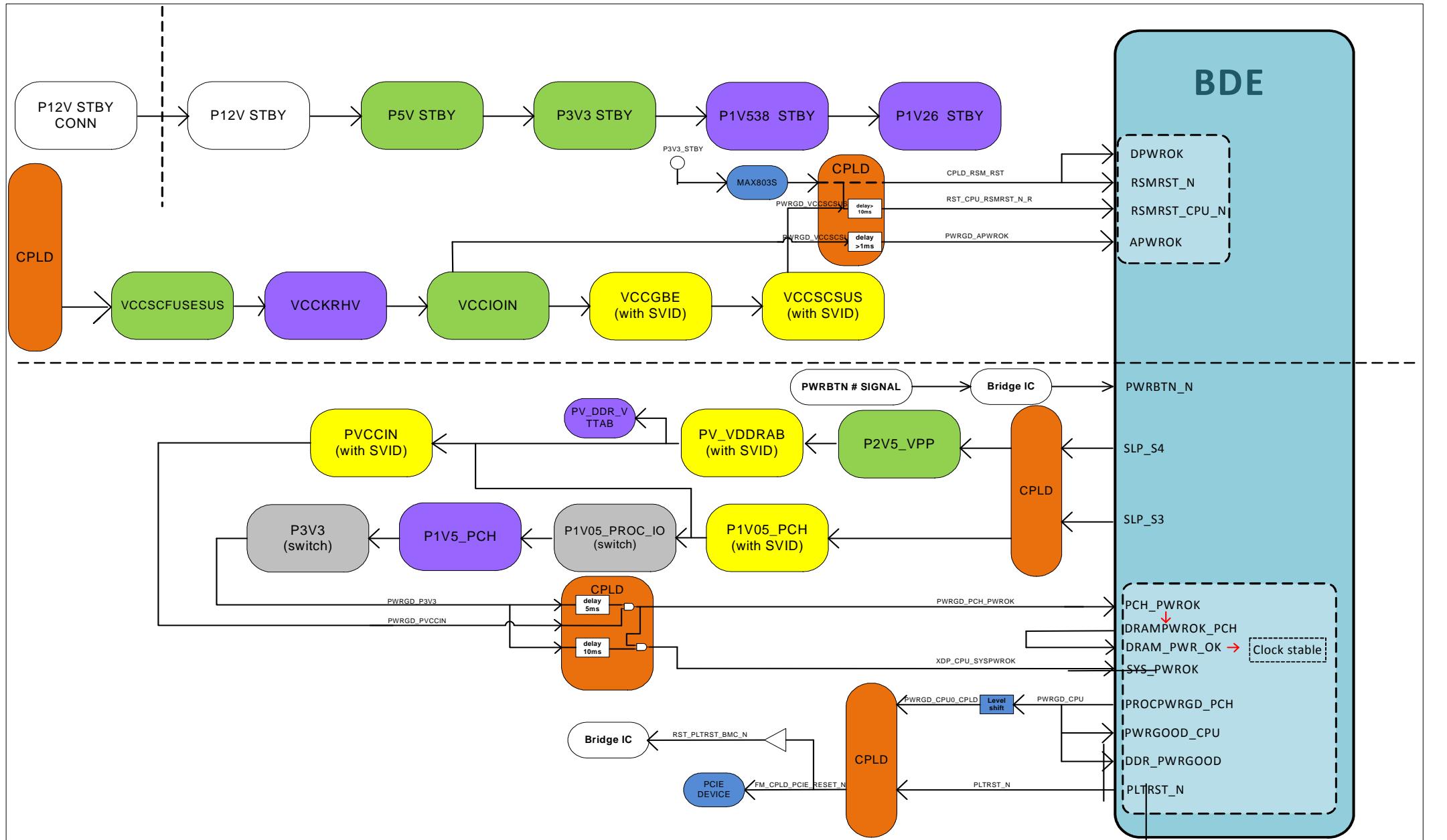
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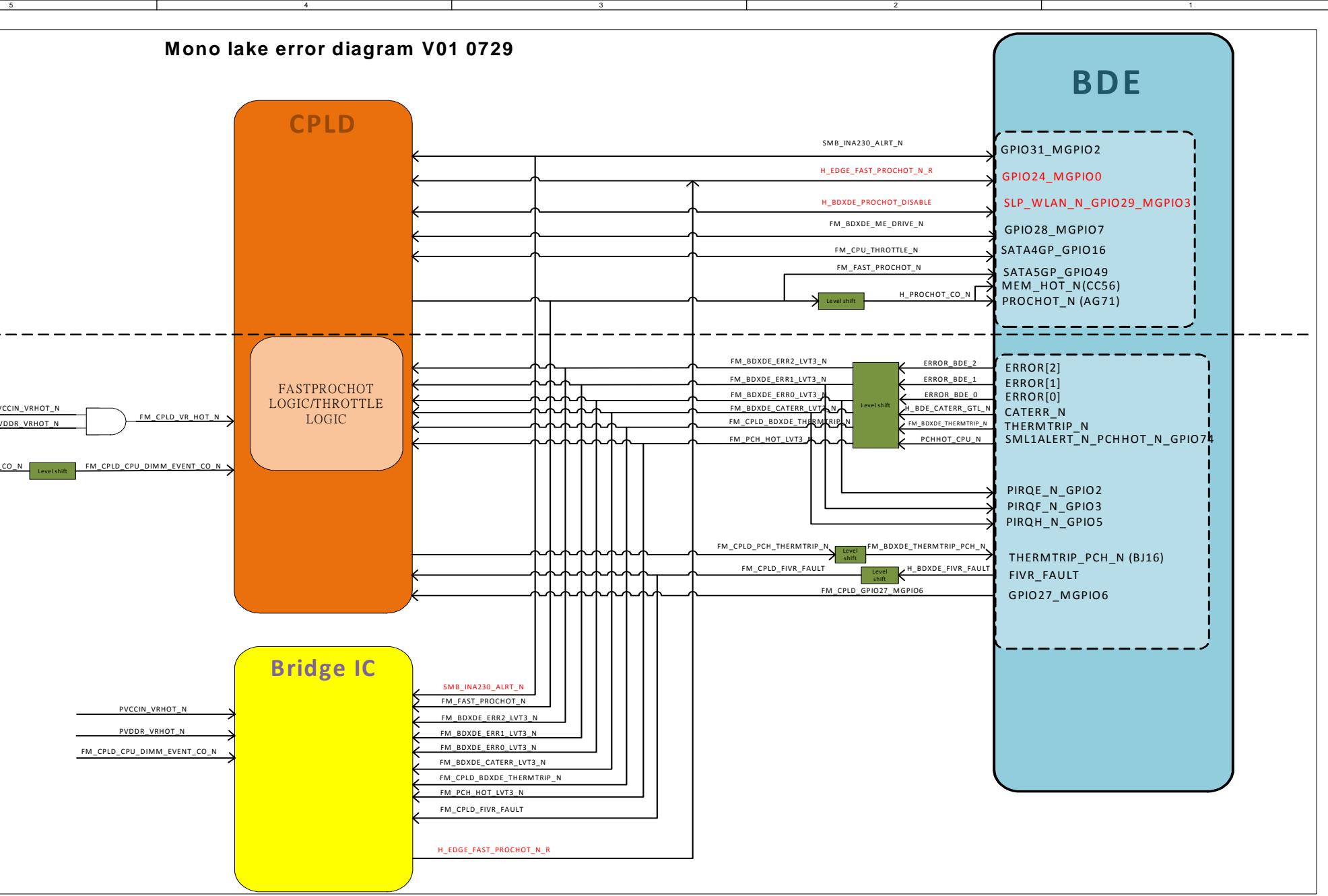
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PWRGD/RST DIAGRAM

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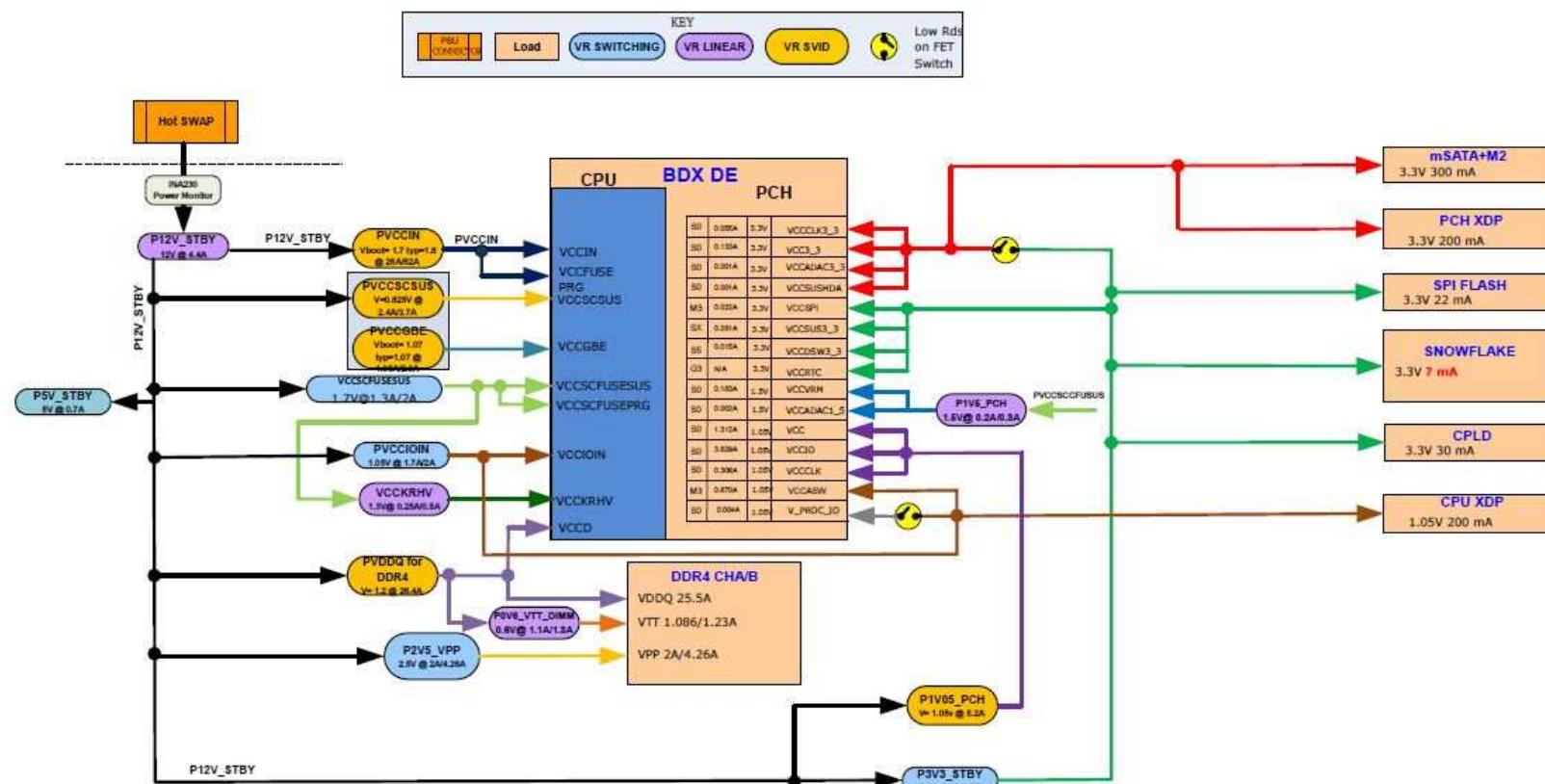


INTERRUPT/ERROR ESCALATION

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Mono Lake POWER DIAGRAM



POWER TOPOLOGY

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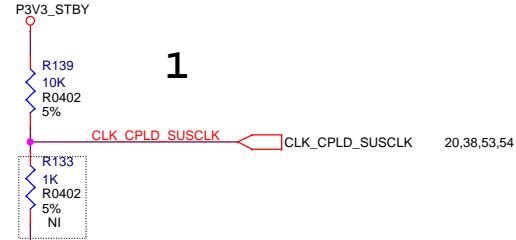
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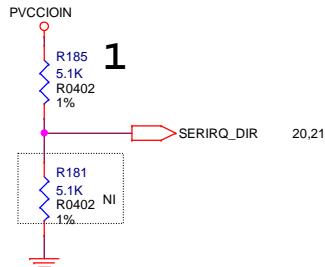
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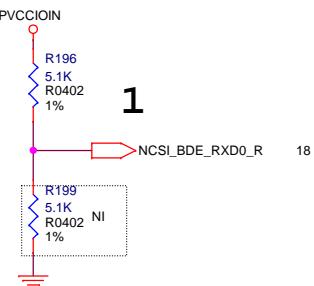
GPIO62



SERIRQ_DIR

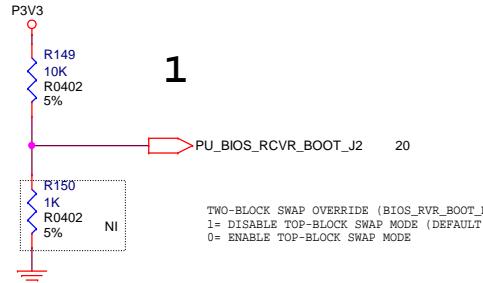


NCSI_RXD_0

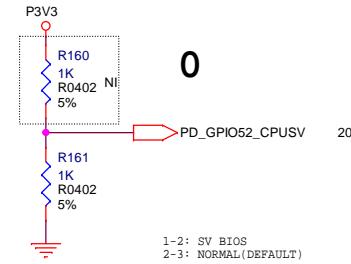


Pull-up : METAL KEY
Pull-down : UNIQUE KEY
FOR PC BASED FUSED UNITS THE DEFAULT WILL BE pull-down.
NCSI_RXD_0 NOW HAS pull-up AS THE DEFAULT.

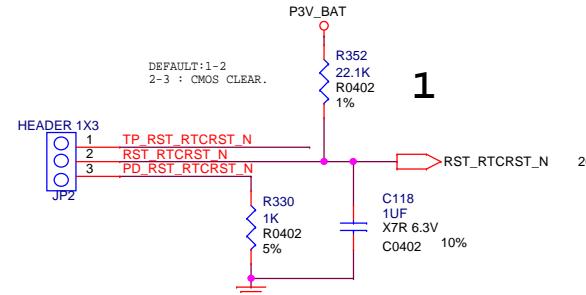
TOP_BLOCK_SWAP



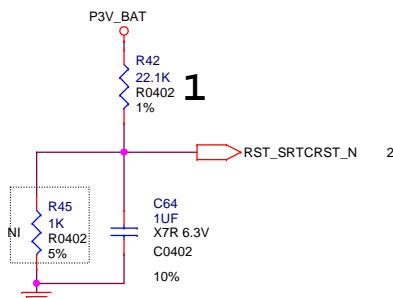
GP52_GSXLOAD



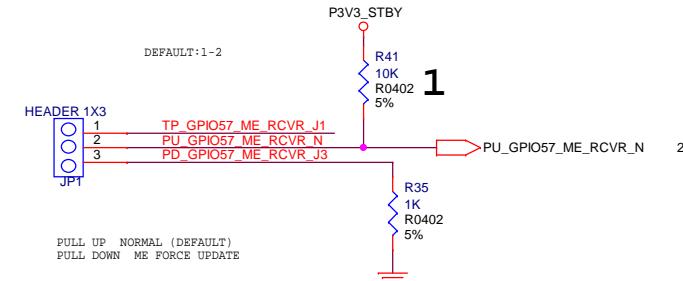
CMOS_CLEAR



CLEAR TPM REGISTERS

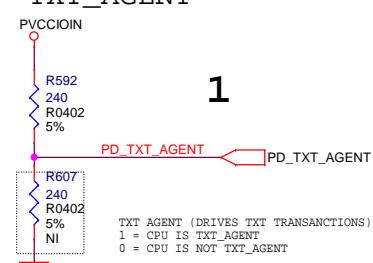


ME_RCVR



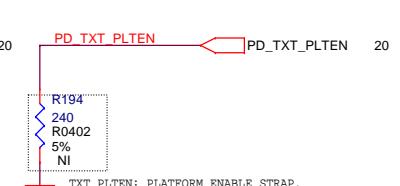
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TXT_AGENT



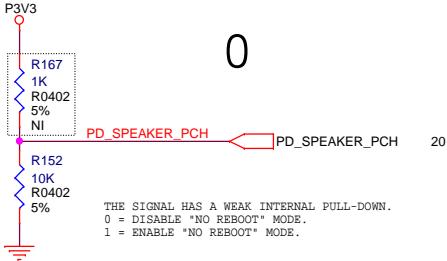
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TXT_PLTEN

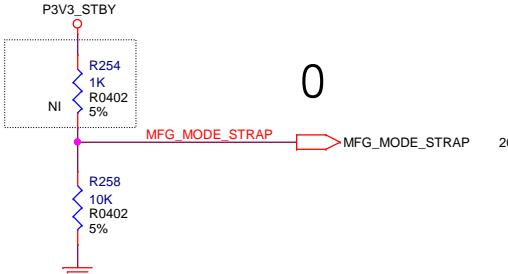


BDE STRAPPING 1

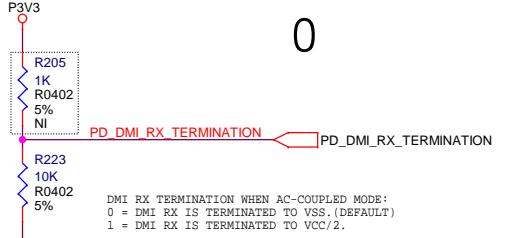
SPKR



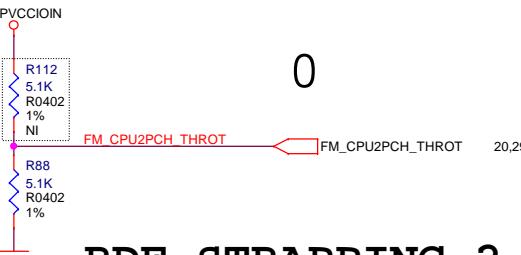
MFG_MODE_STRAP



GPIO33

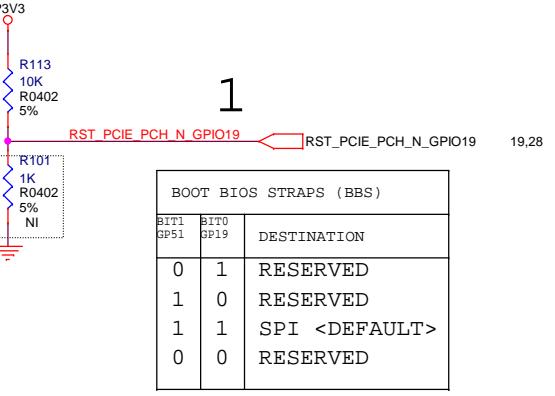


CPU2PCH_THROT

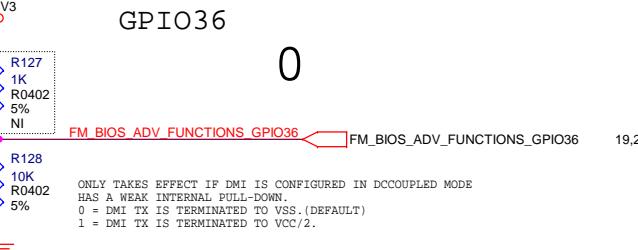


BDE STRAPPING 2

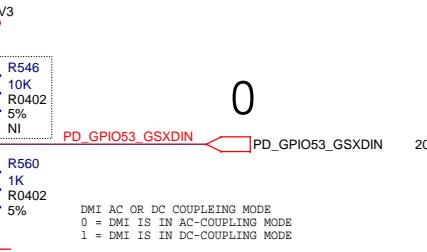
GPIO19



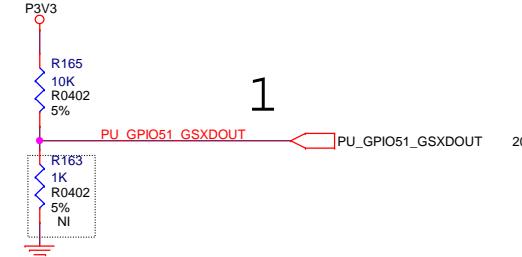
BIOS_ADV_FUNCTIONS



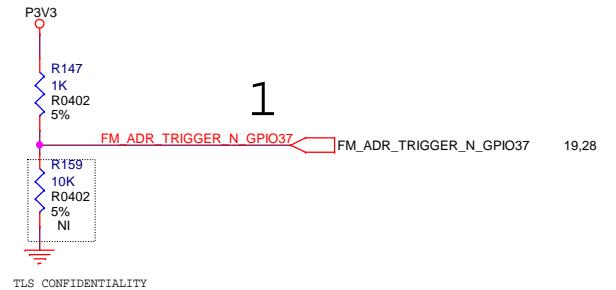
GP53_GSX DIN



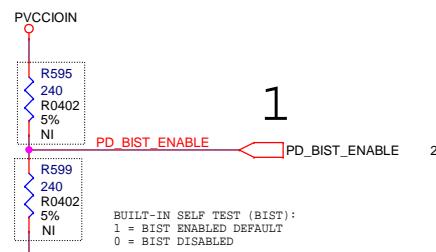
GPIO51



GPIO37

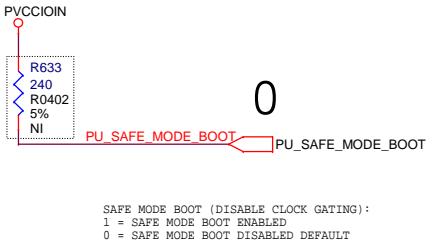


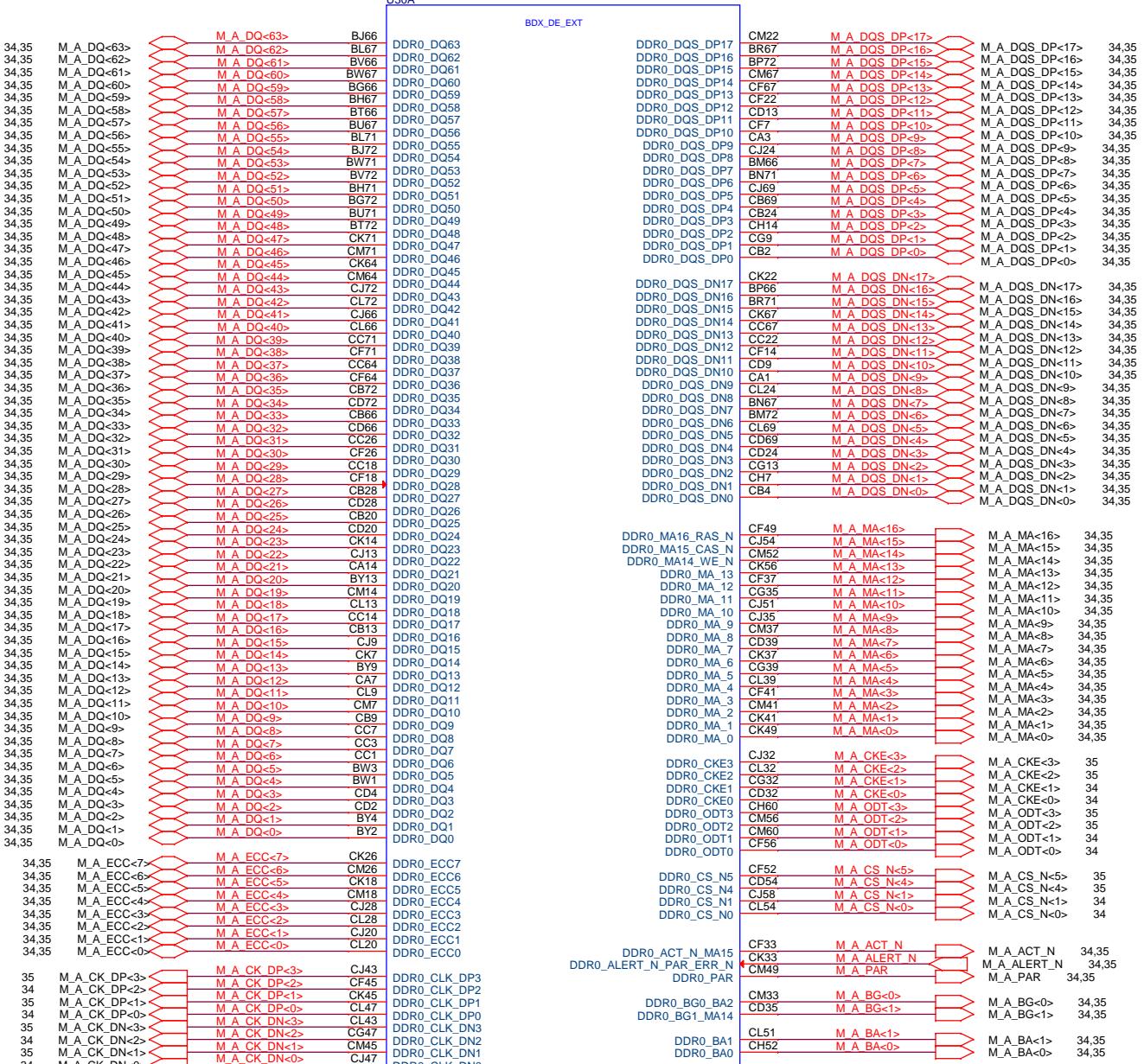
BIST_ENABLE



DESIGN NOTE :
The default setting should be checked for each board build

SAFE_MODE_BOOT



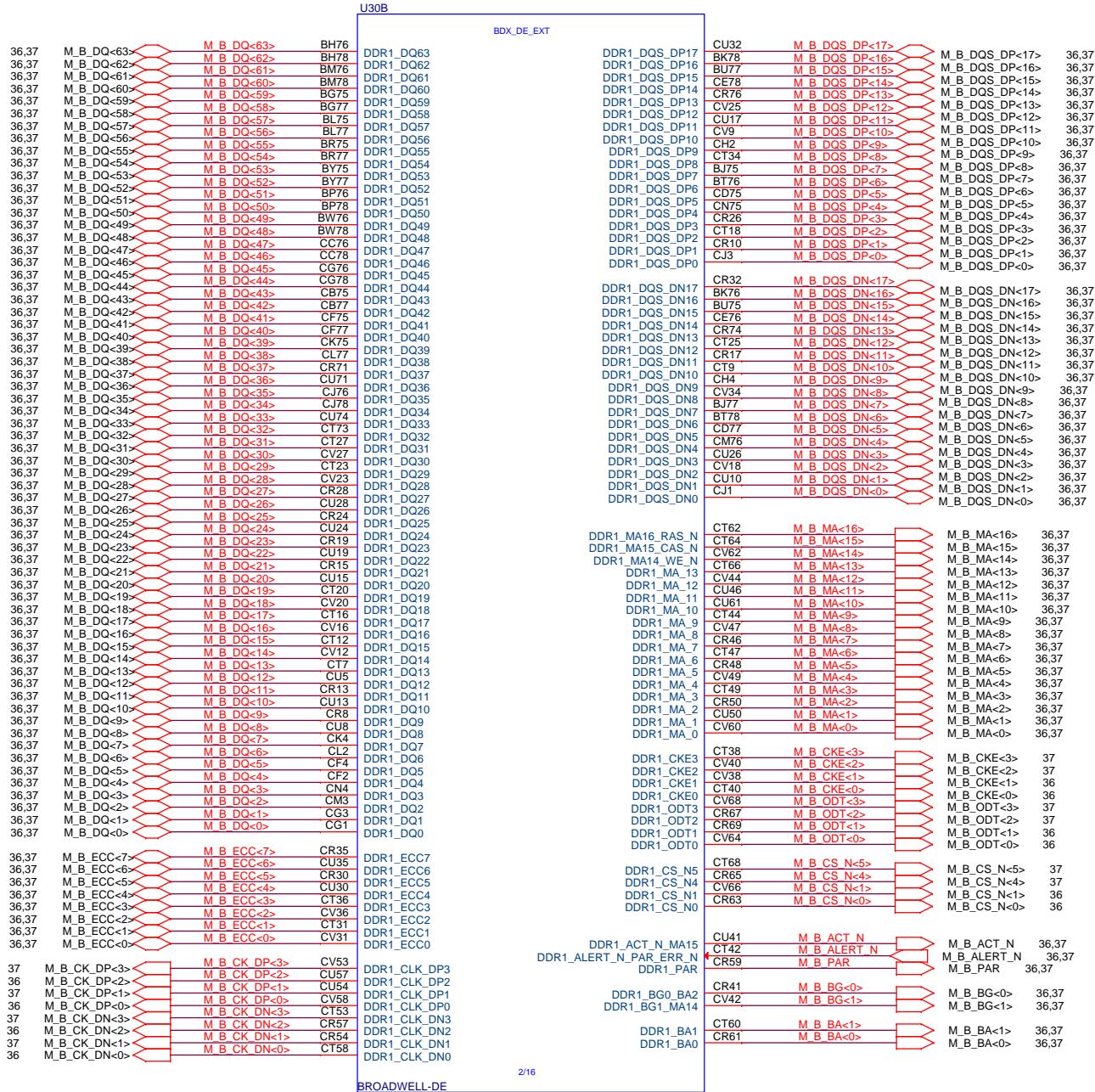


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BROADWELL-DE

BDX-DE DDR4 CHANNEL A**Quanta**
CCBU

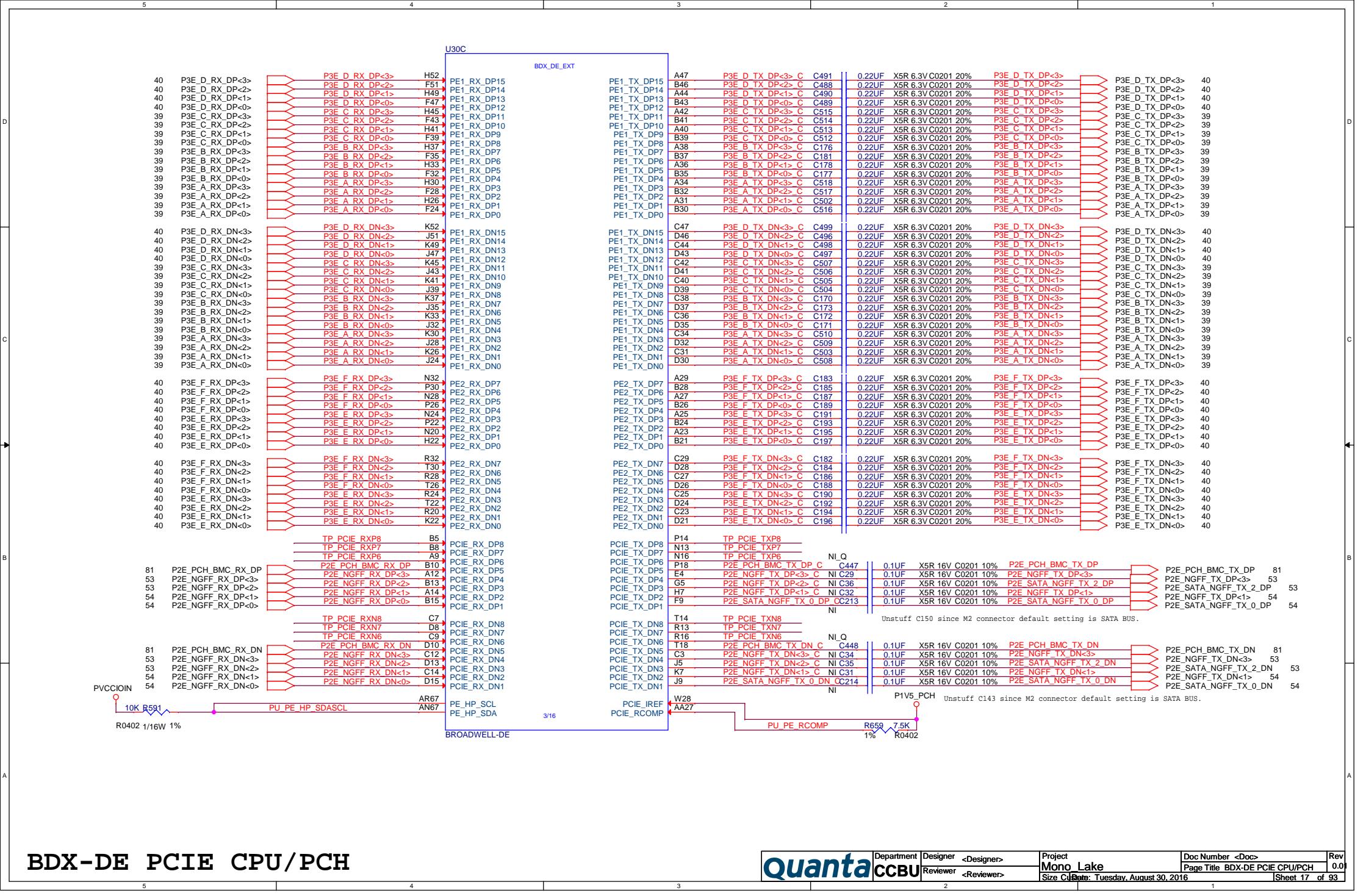
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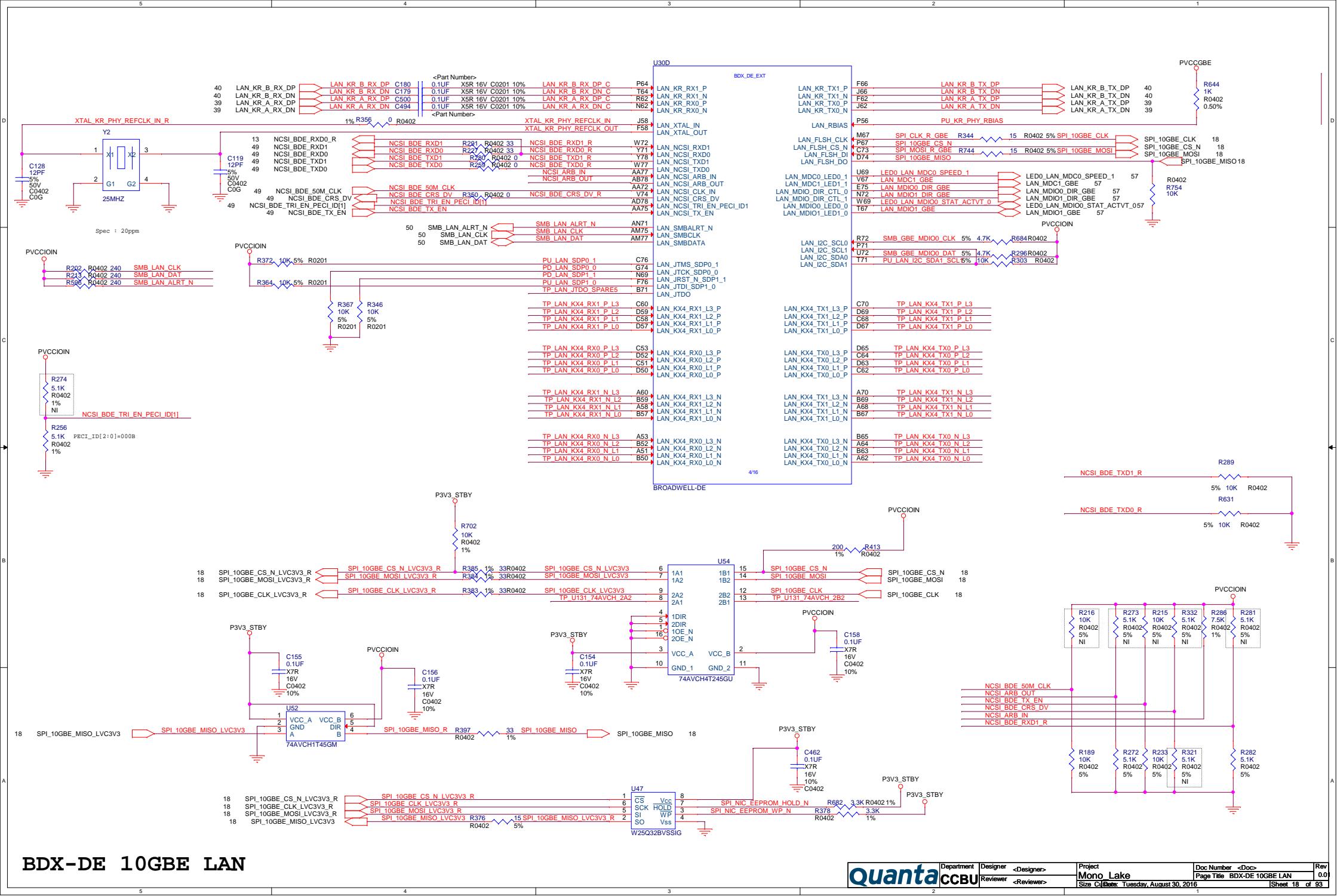


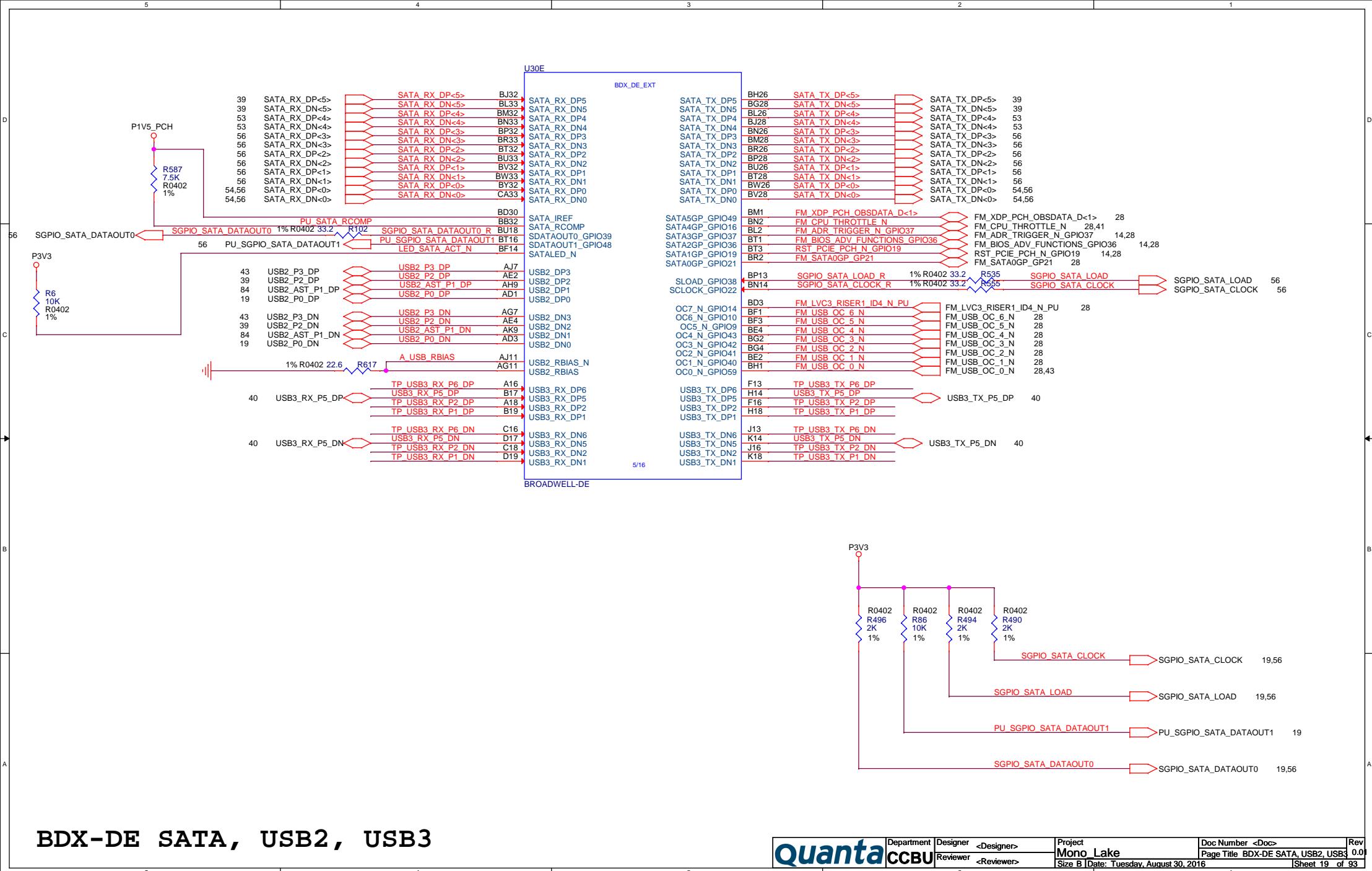
BDX-DE DDR4 CHANNEL B

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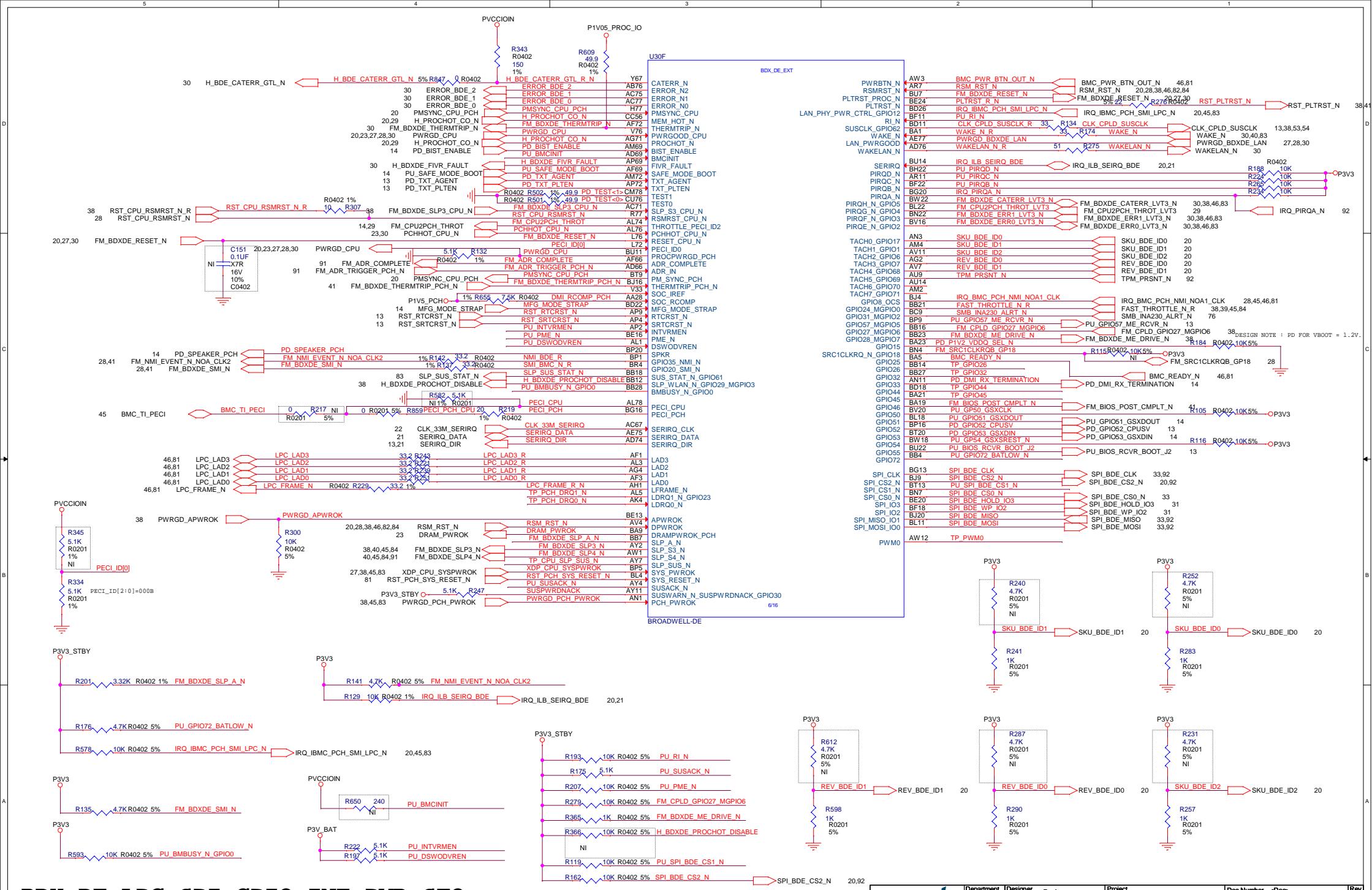
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Reviewer	<Reviewer>	Size	Page Title BDX-DE DDR4 CHANNEL B	0.0
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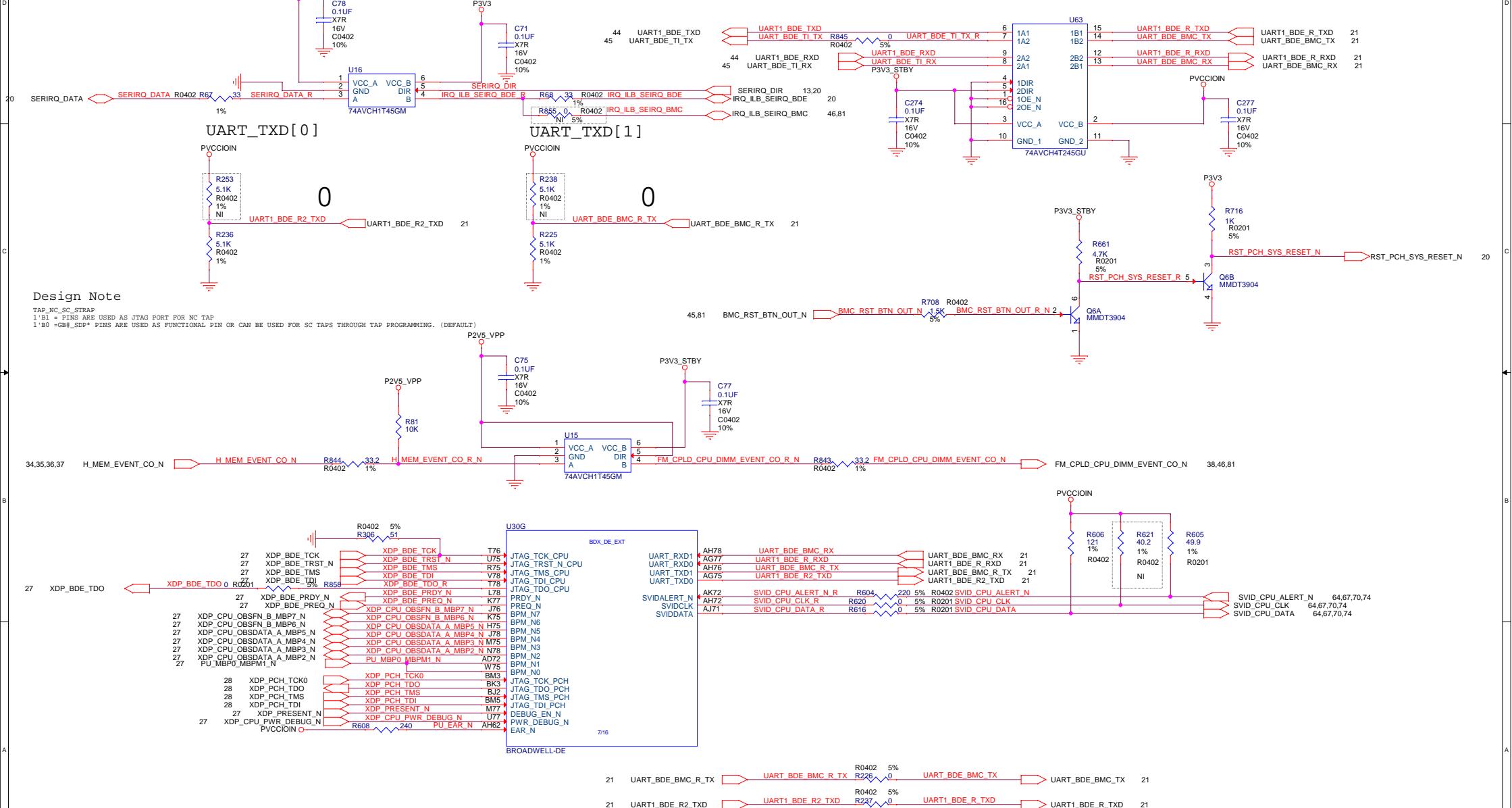
BDX-DE SATA, USB2, USB3

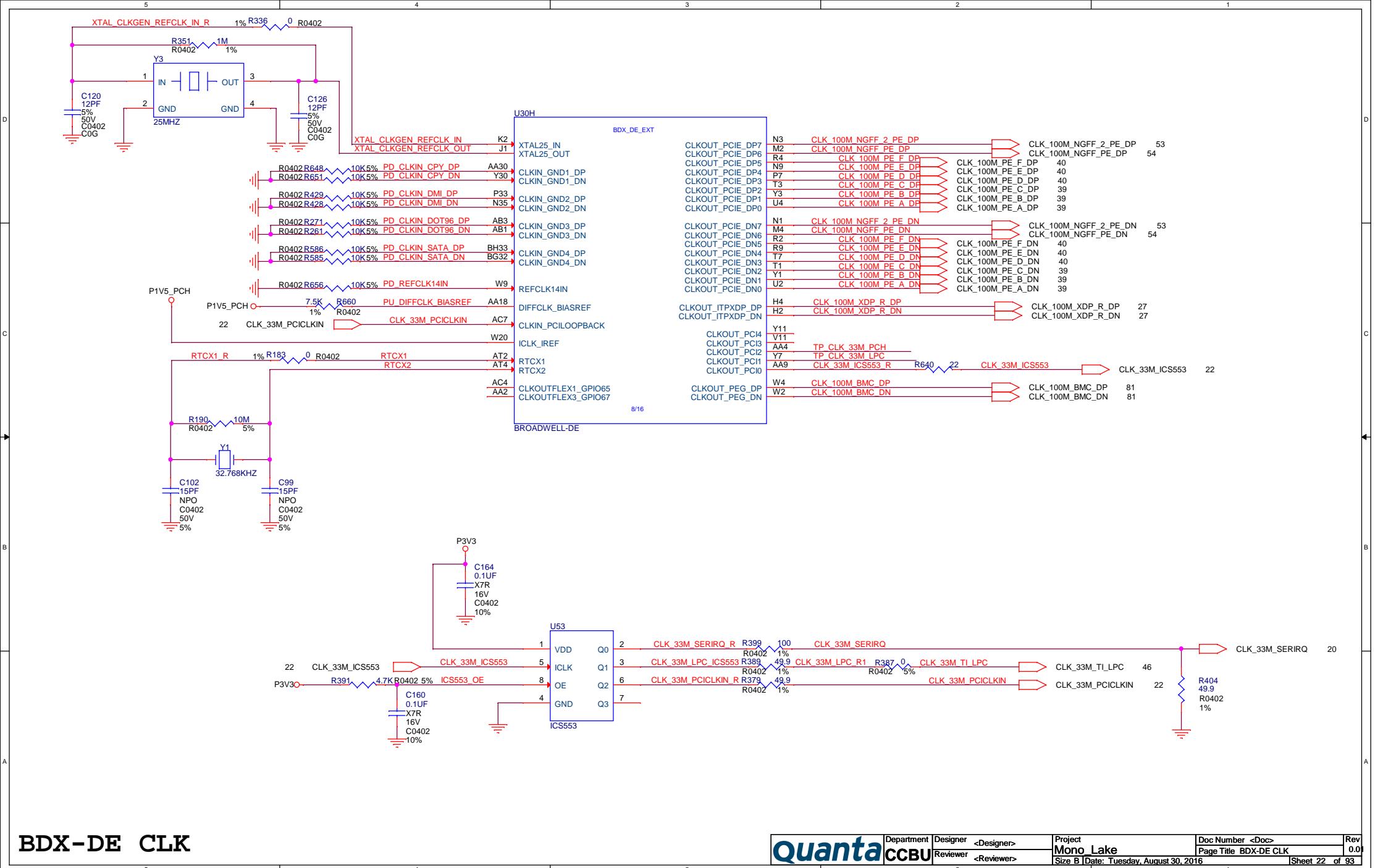


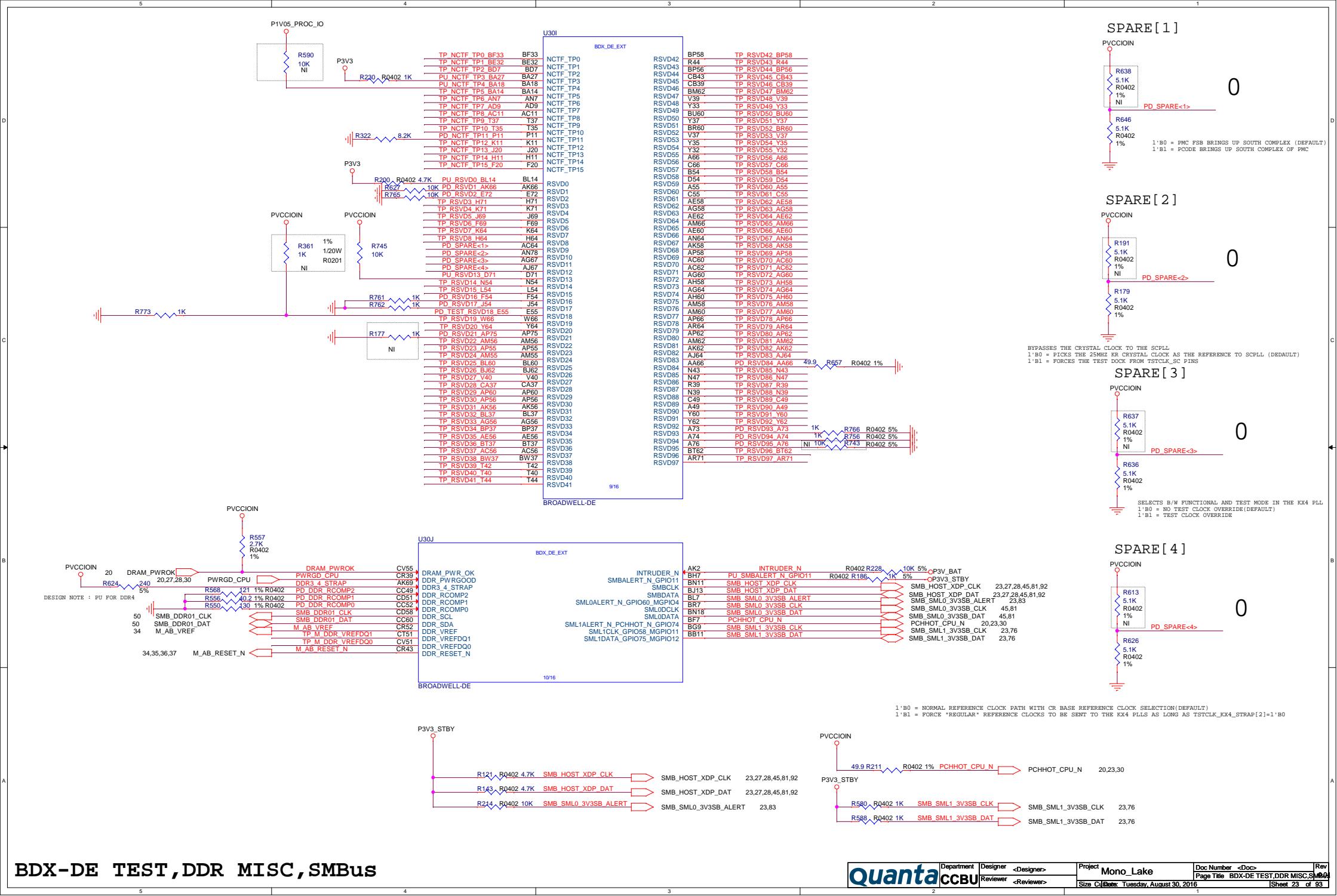
BDX-DE LPC, SPI, GPIO, INT, PWR SEQ

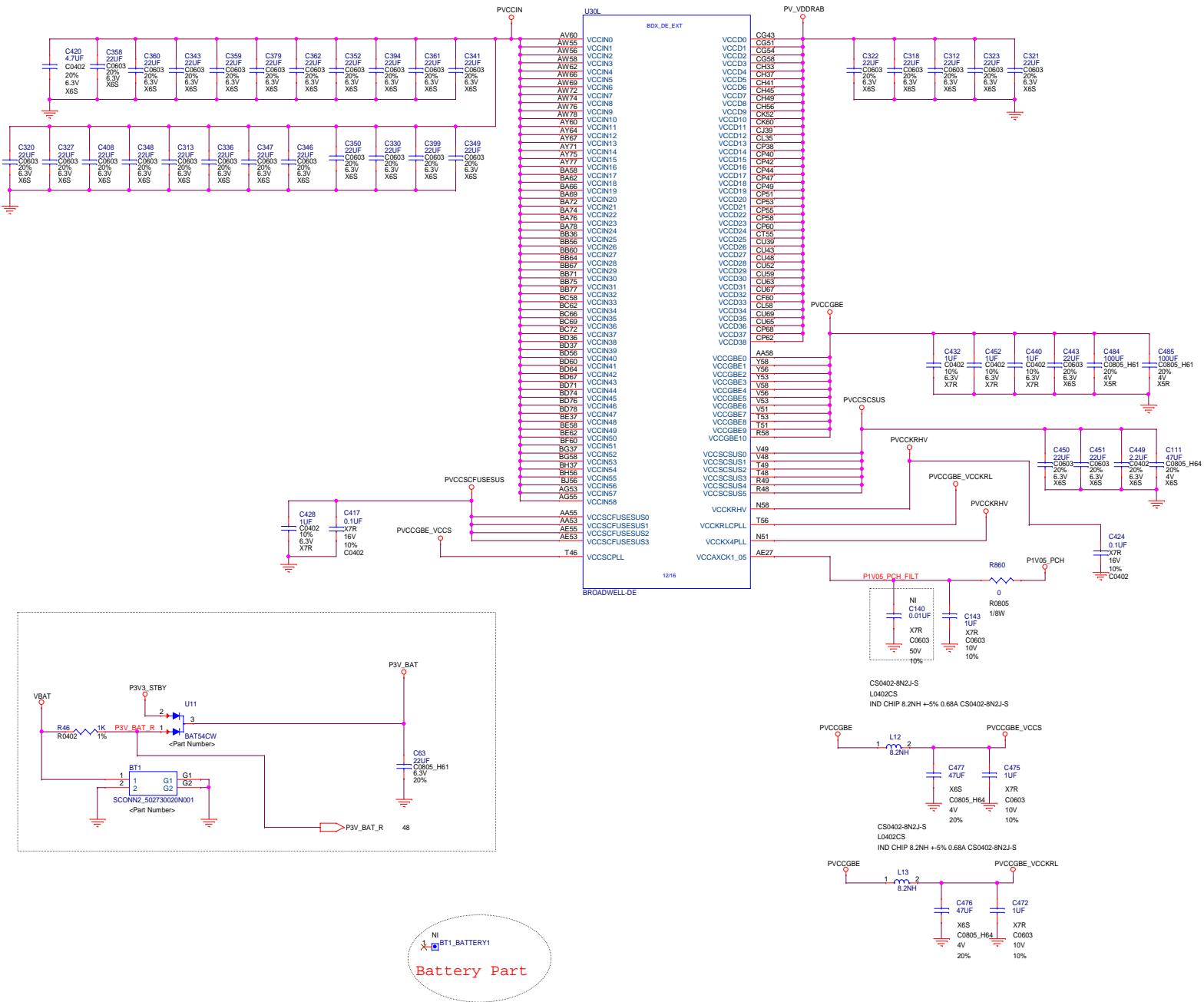
Need change to NXP and check CRB.

CHECK THIS. SUPPORT VOLTAGE BEED TO 0.8 to 3.6V

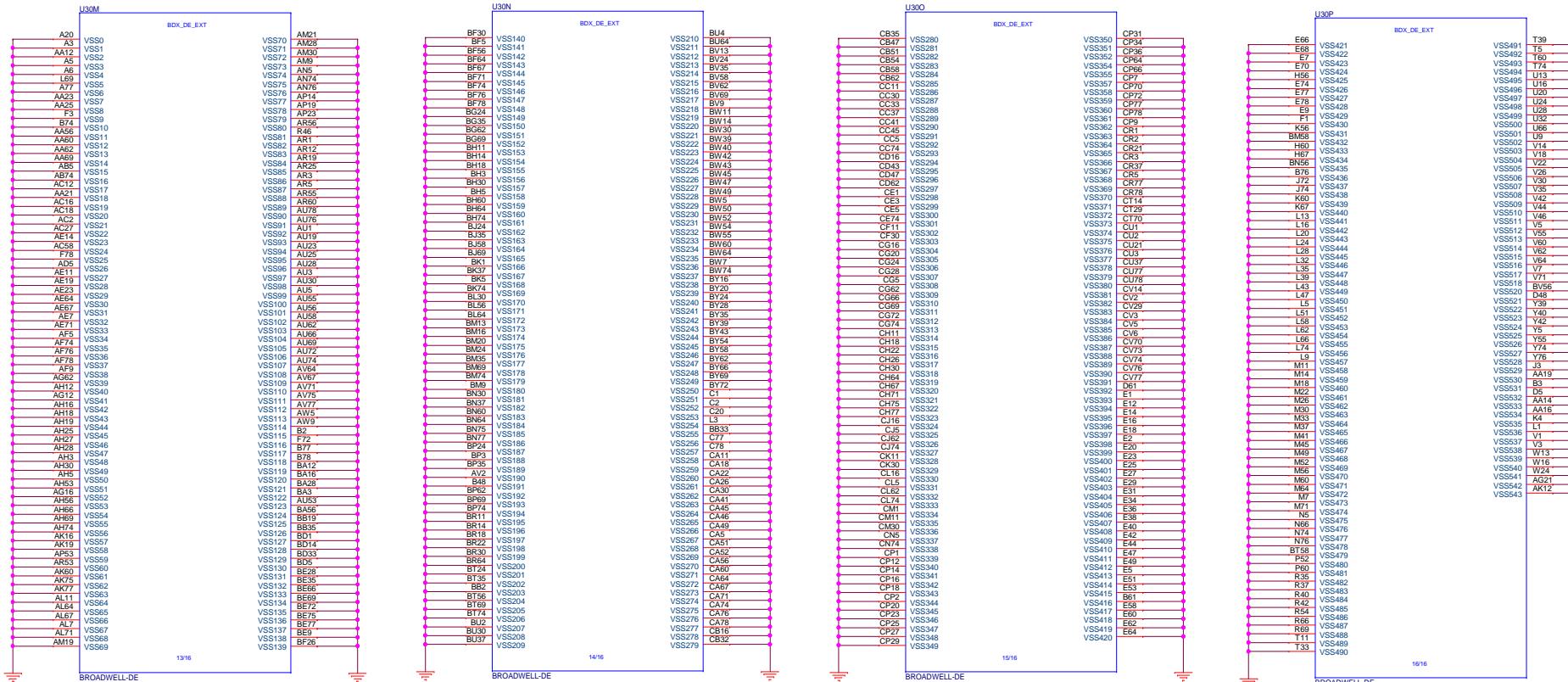


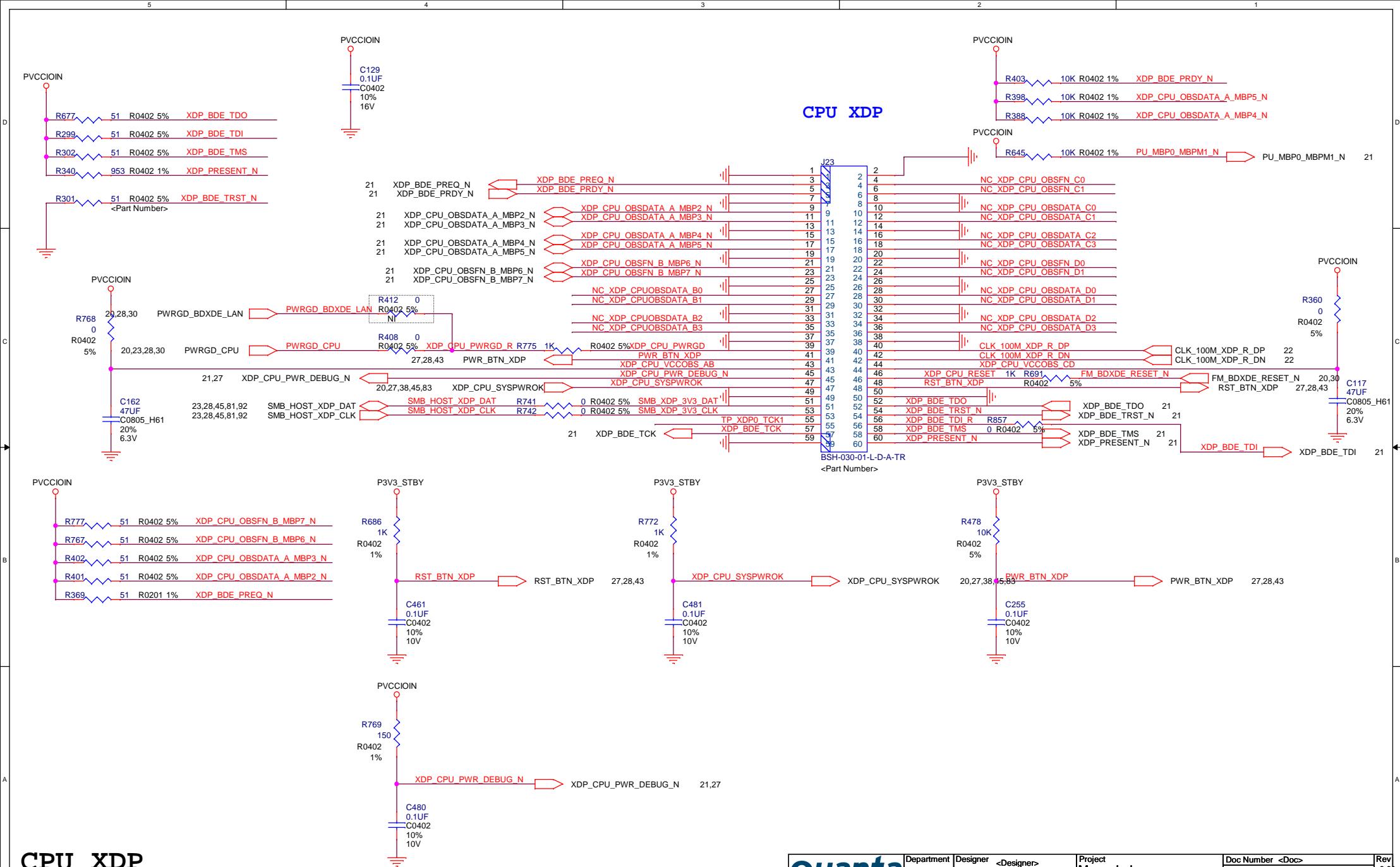


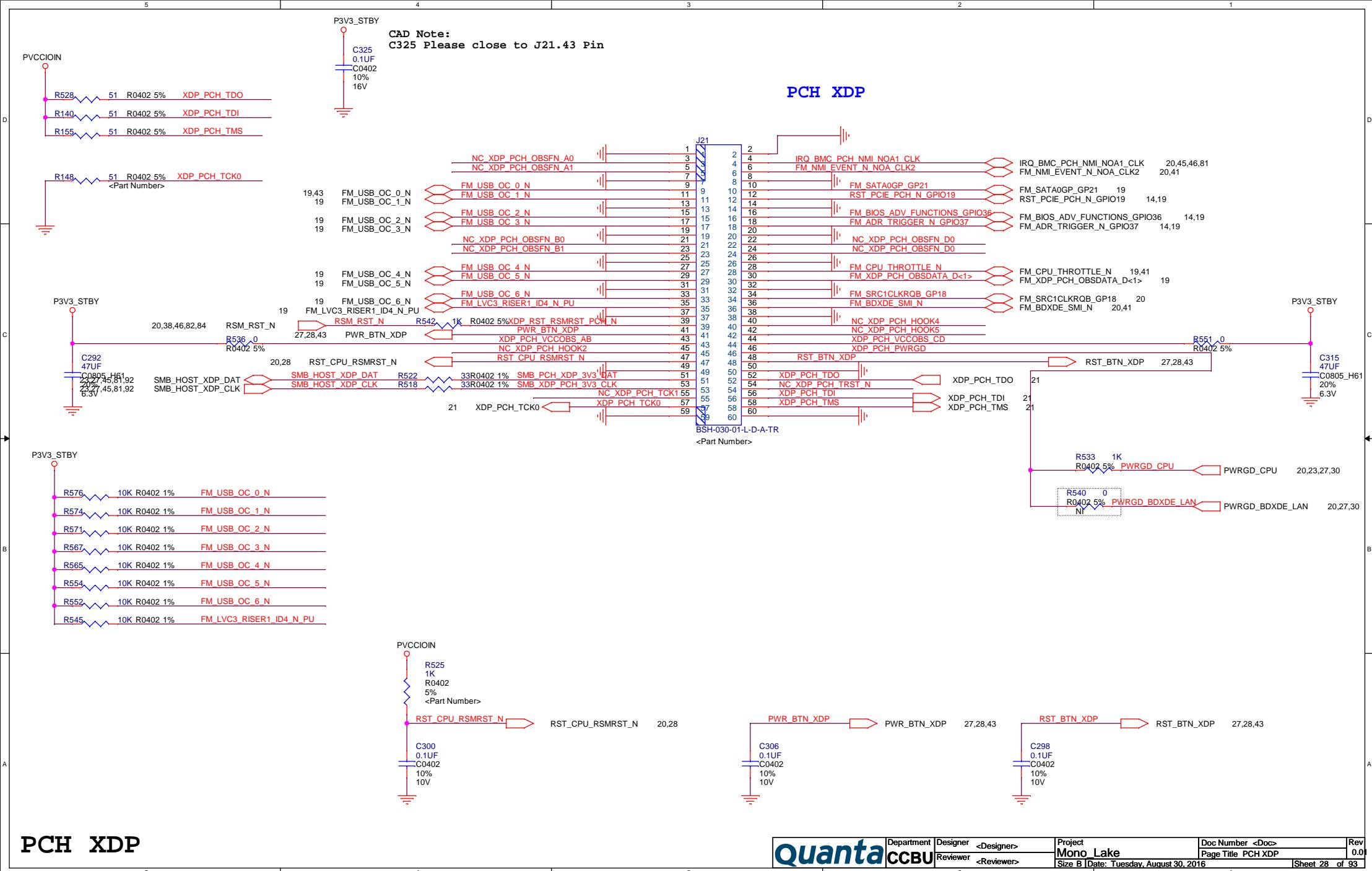


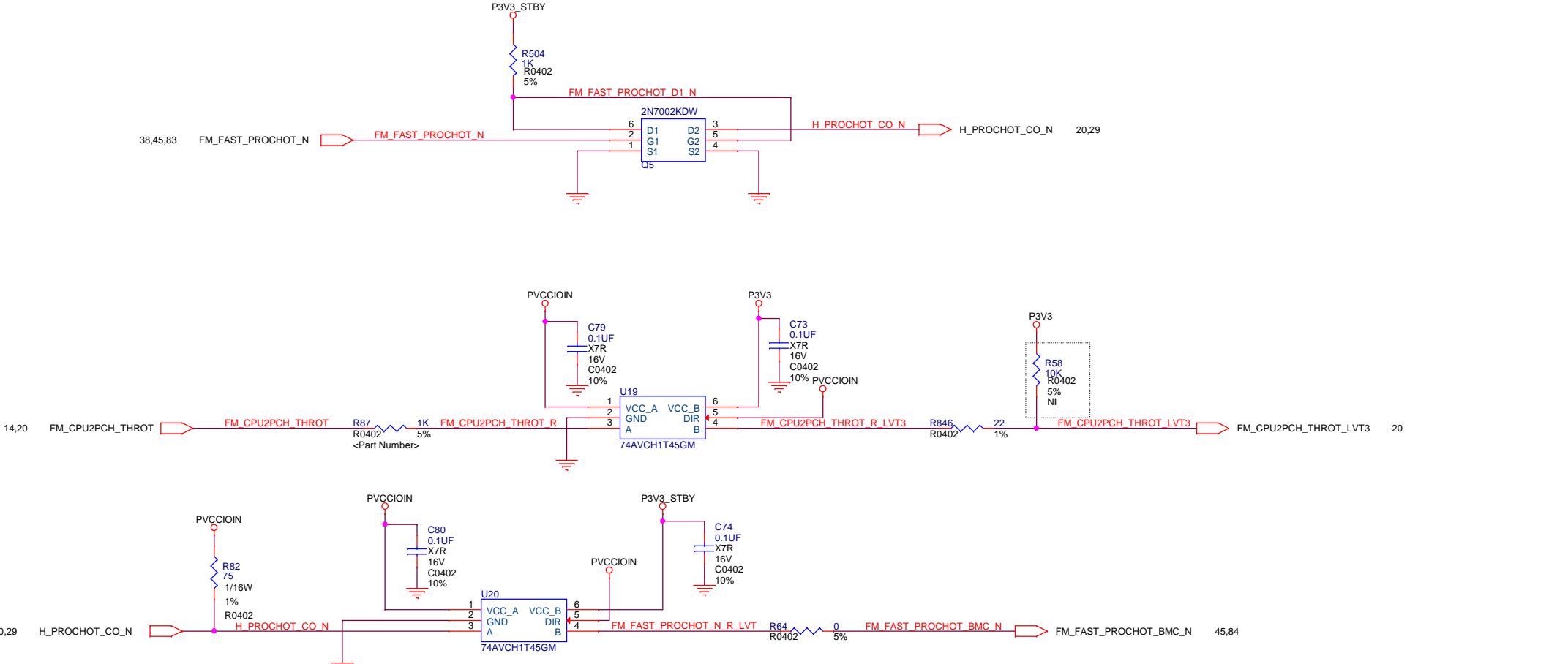


BOM Note
The Battery has 35mm cable

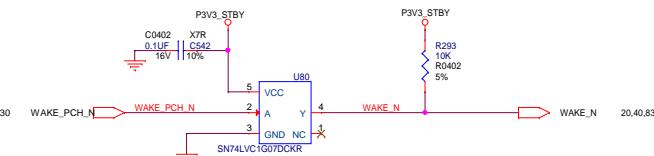
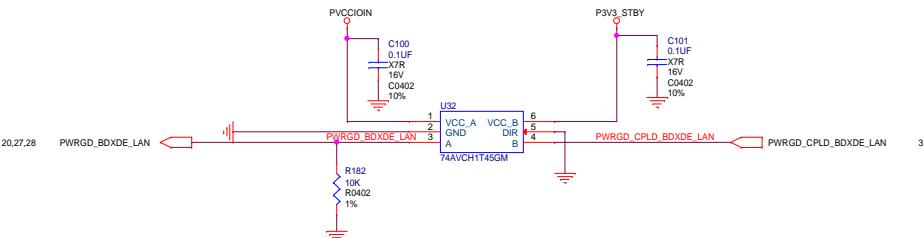
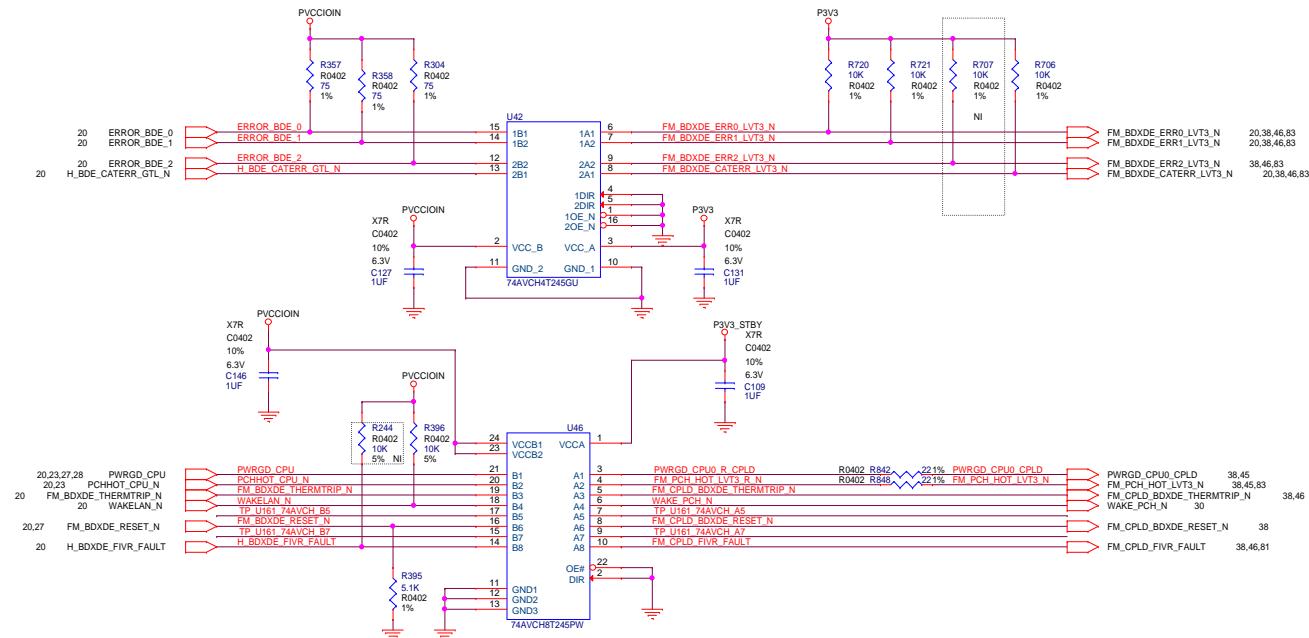




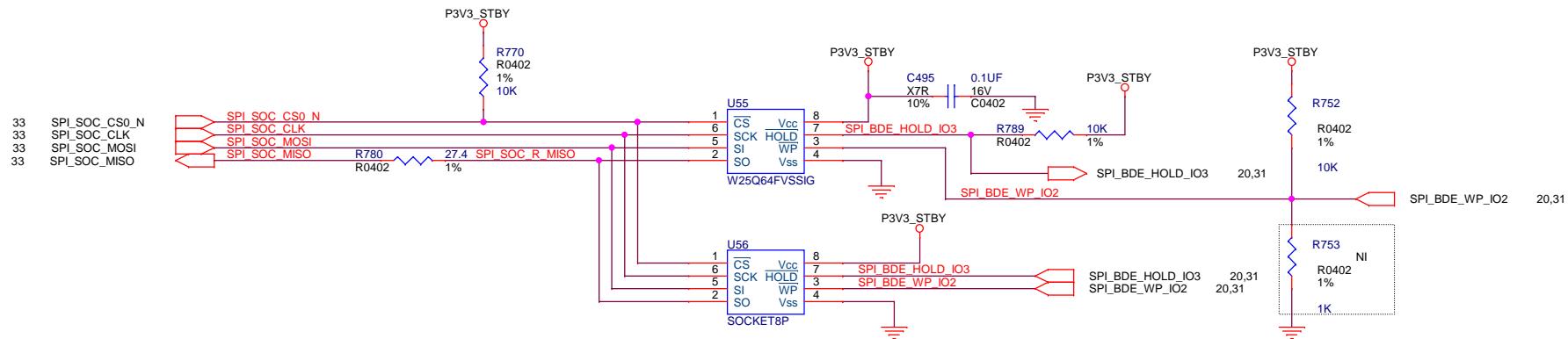




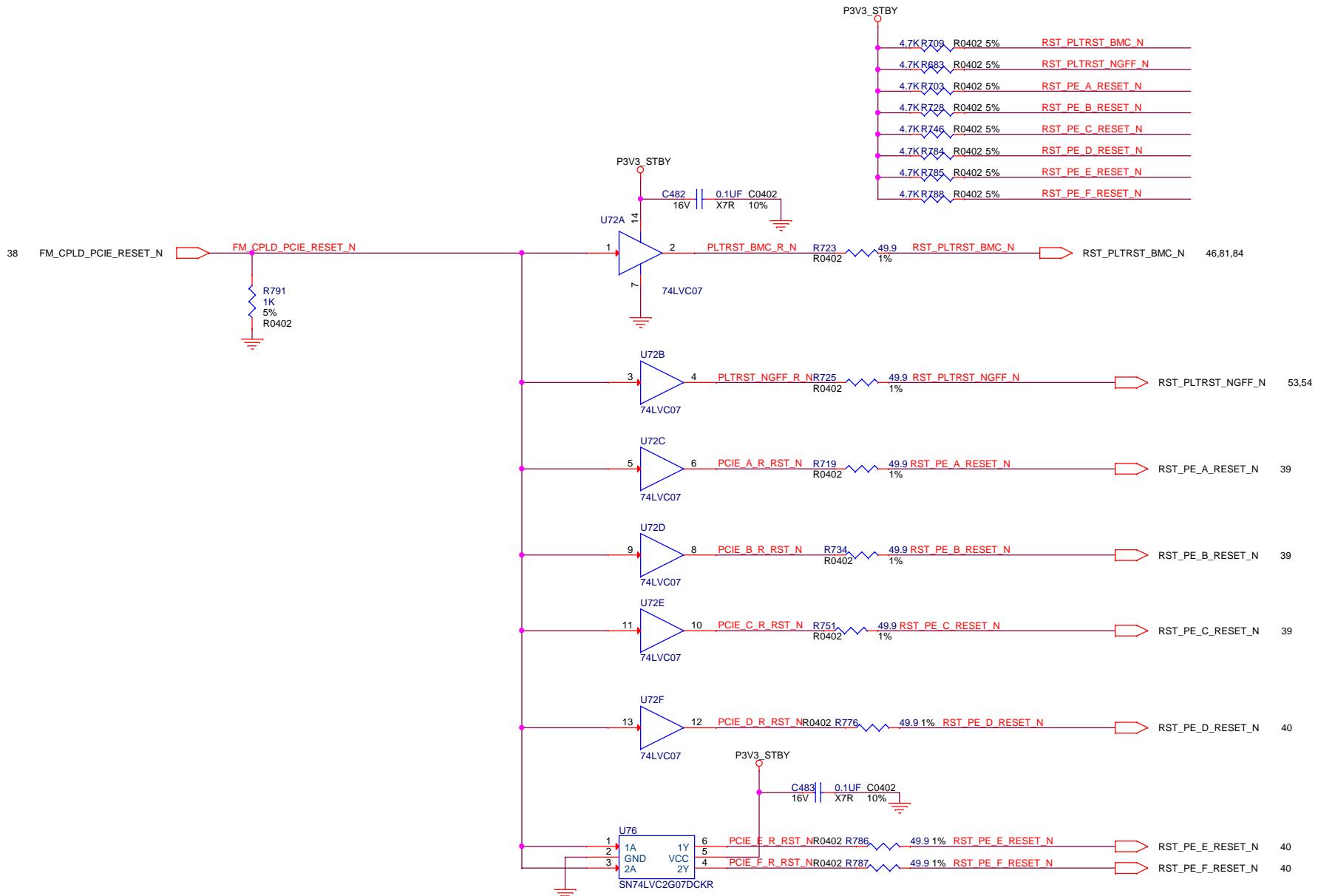
ERROR CNTL 1

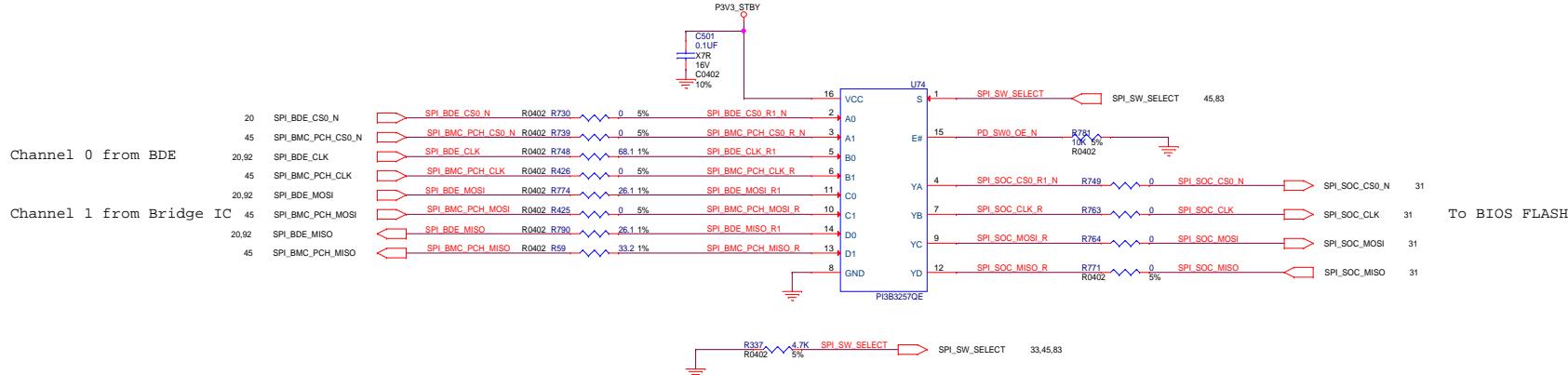


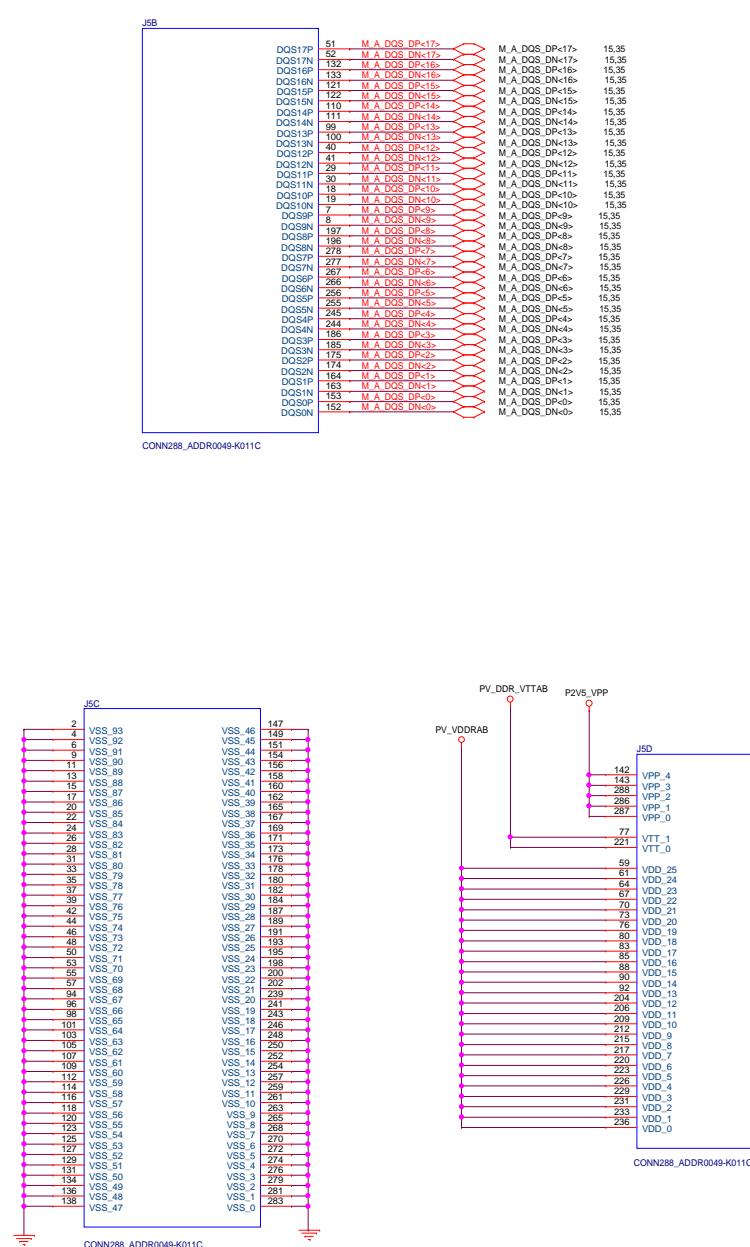
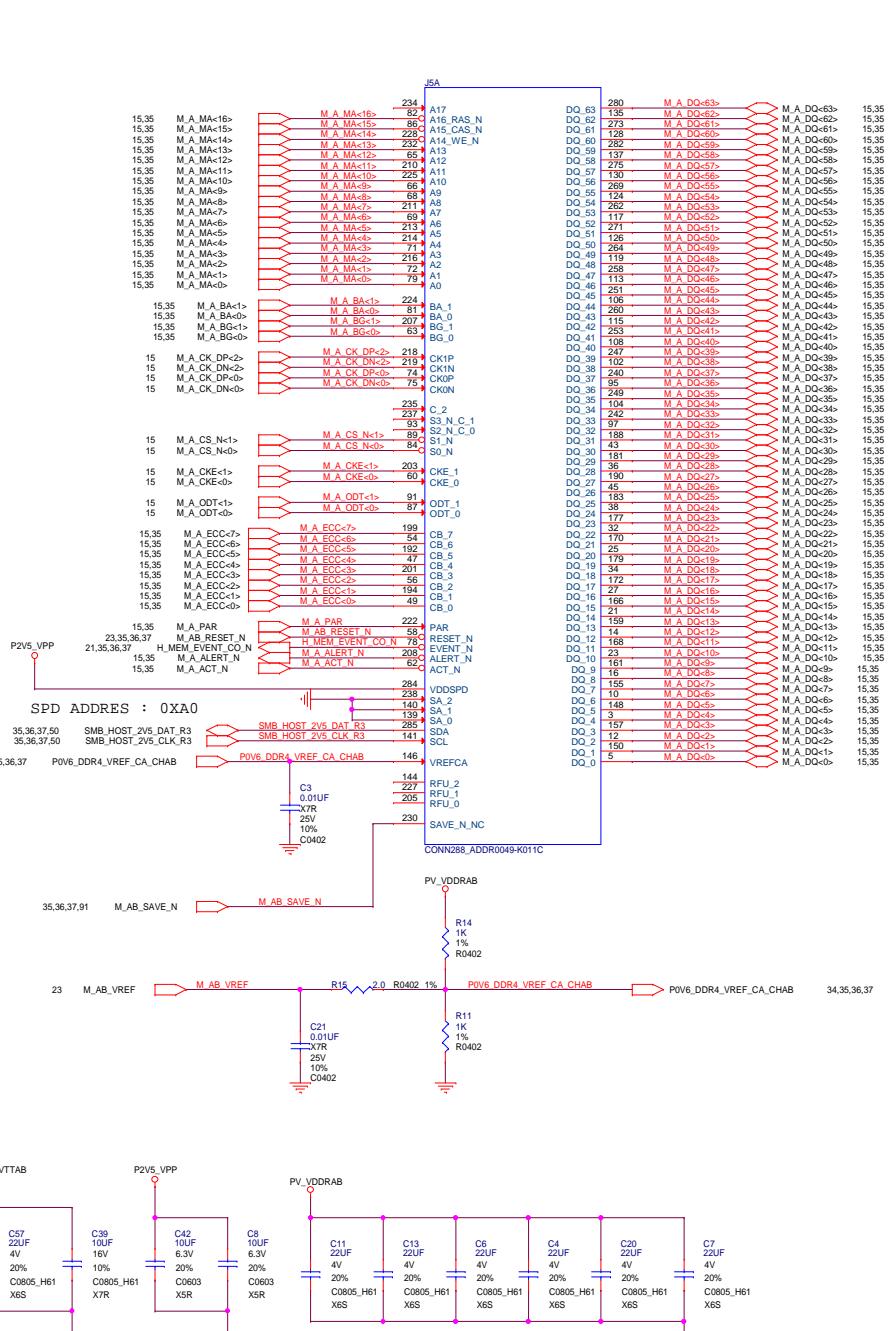
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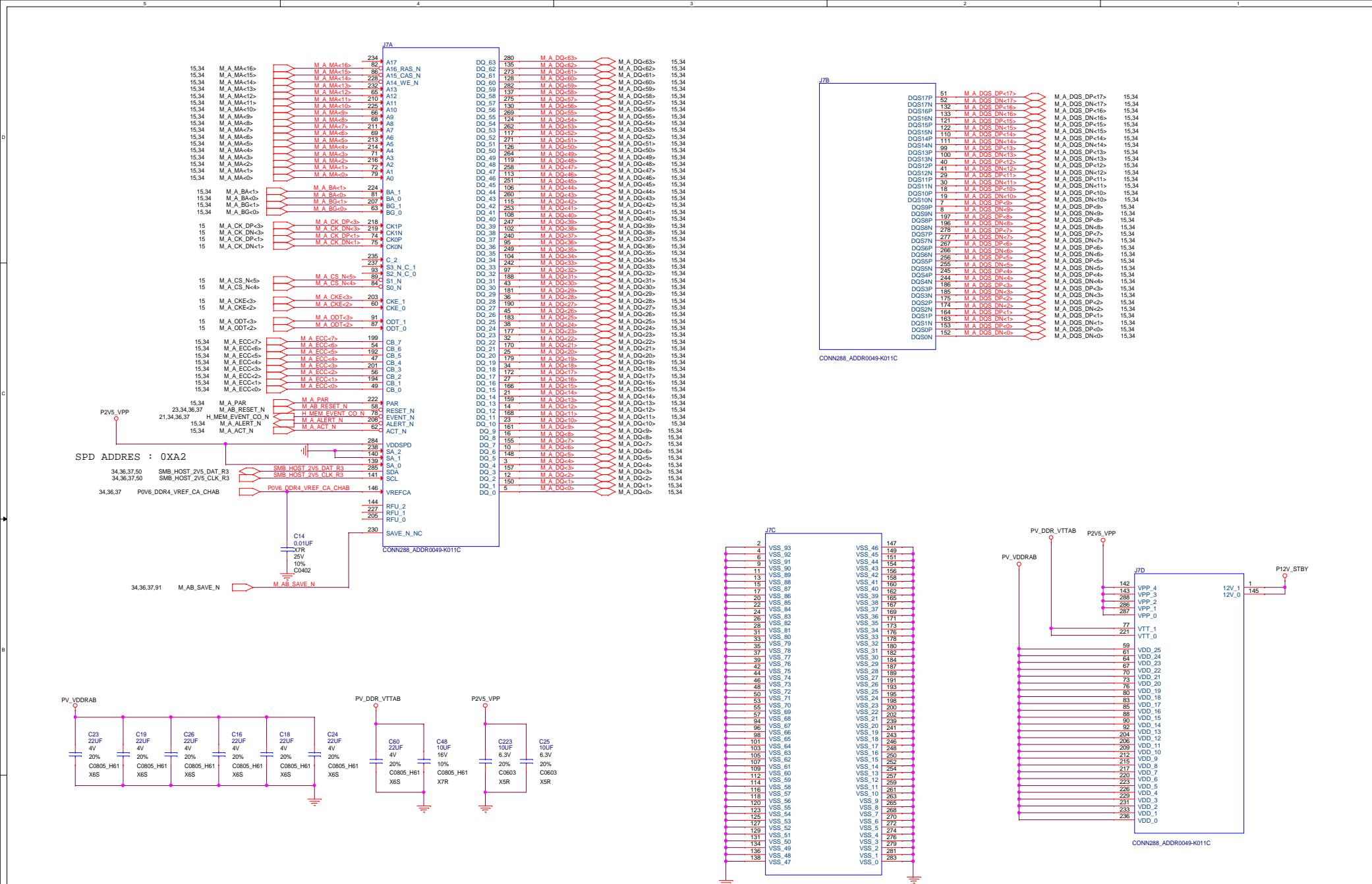


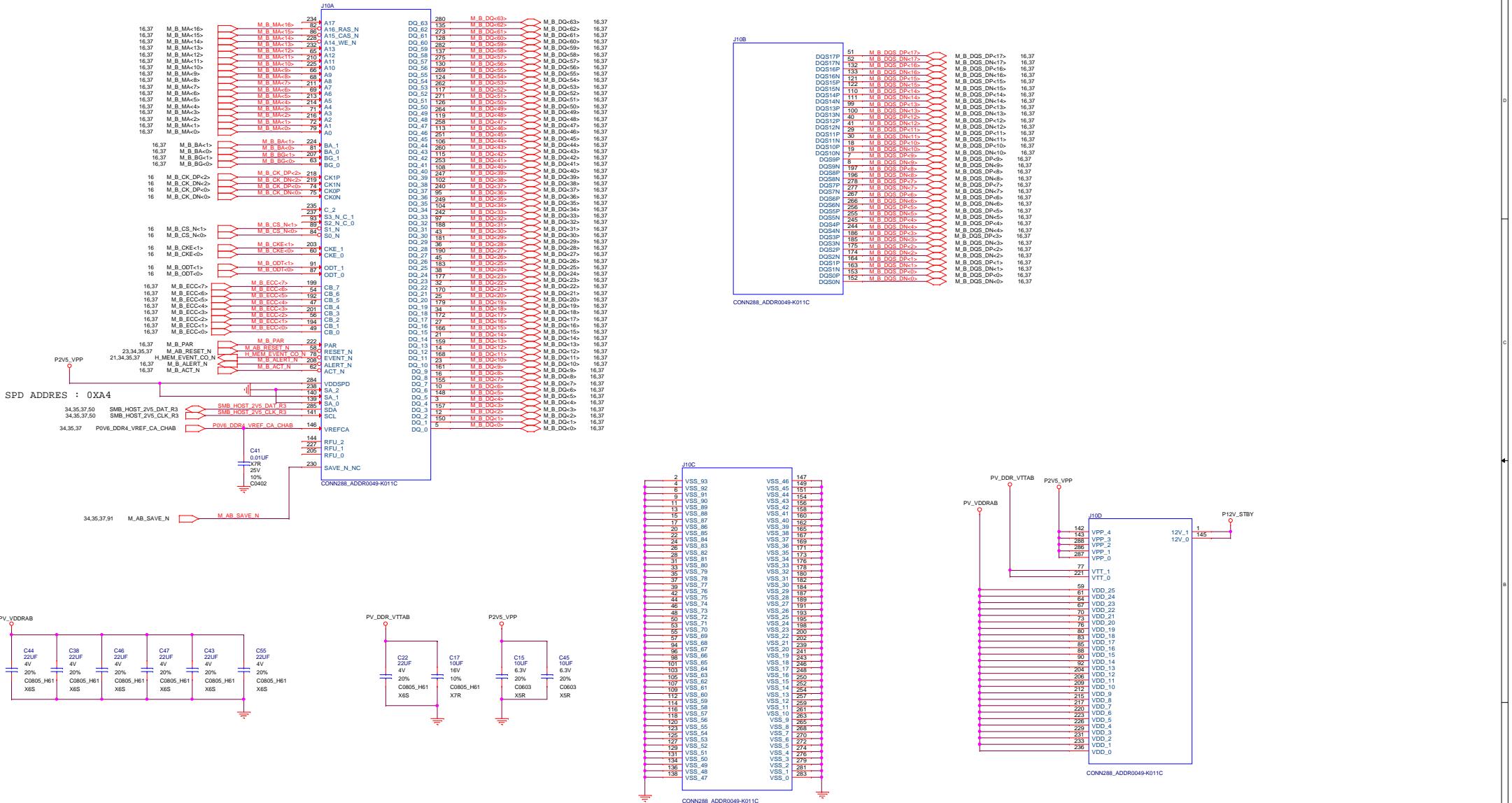
CAD Note:
 THIS PART WILL CO-LAY WITH SOCKET
 USE ALT SYMBOL ASSOCIATED WITH SOCKET FOOTPRINT

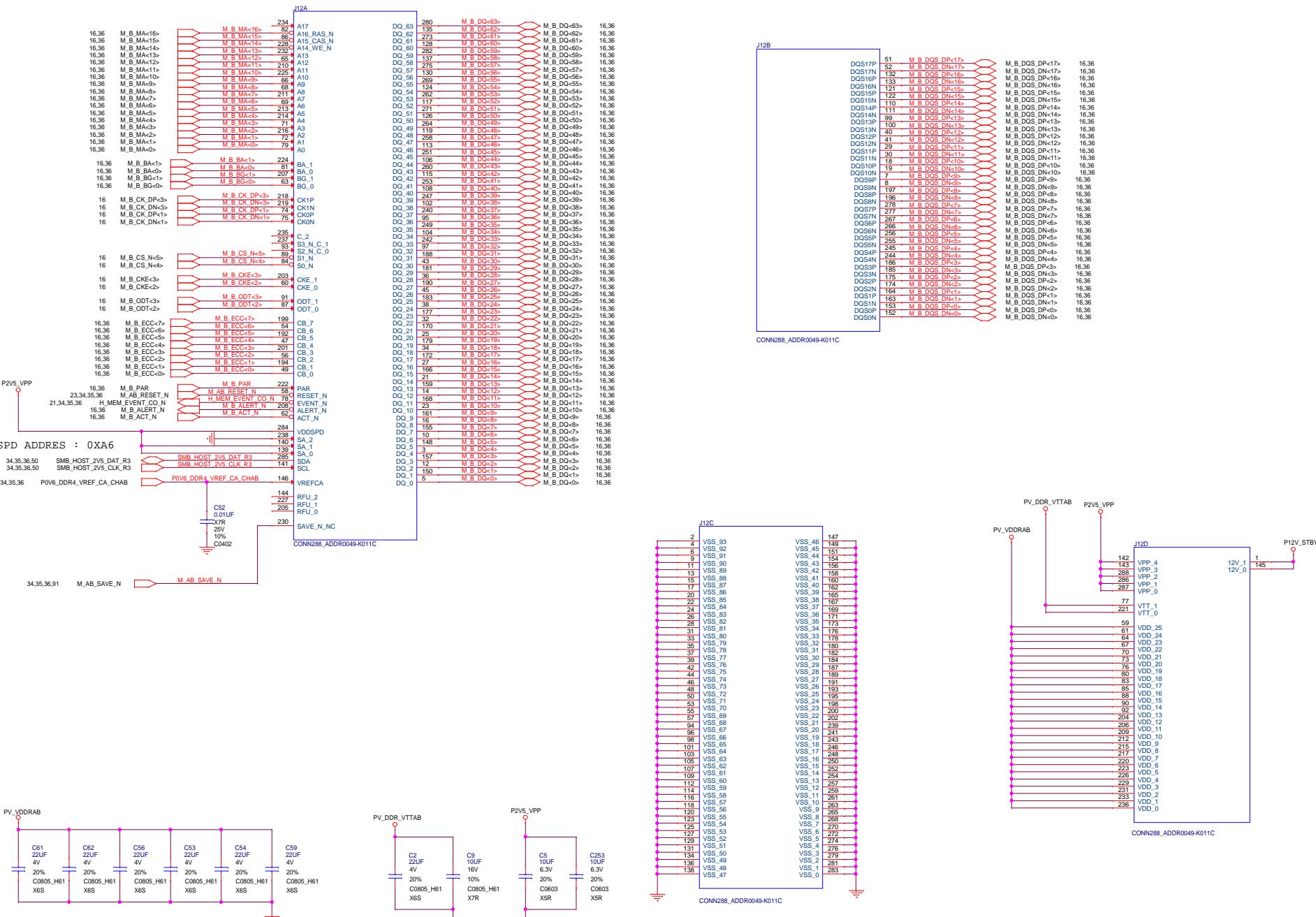


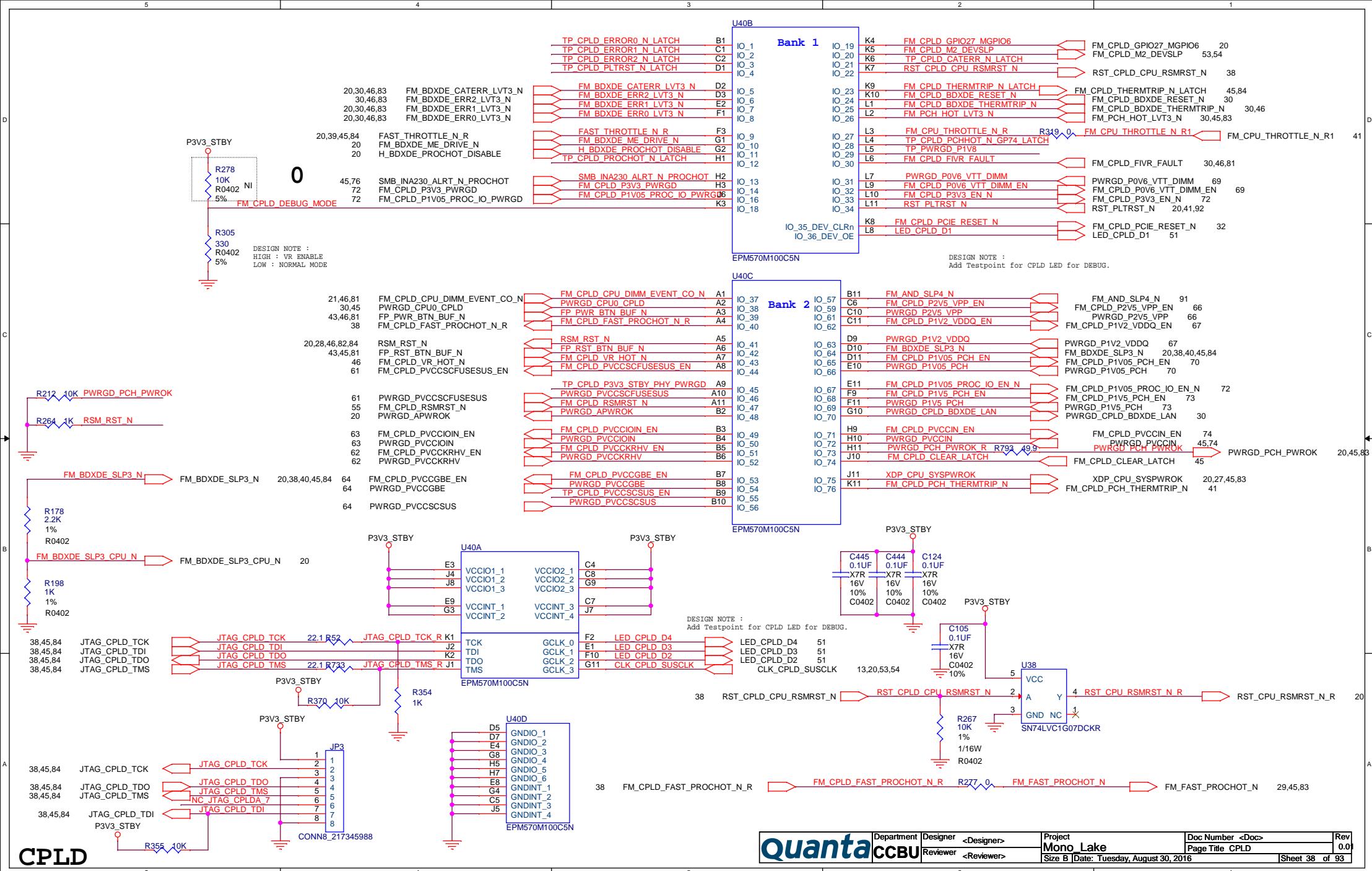


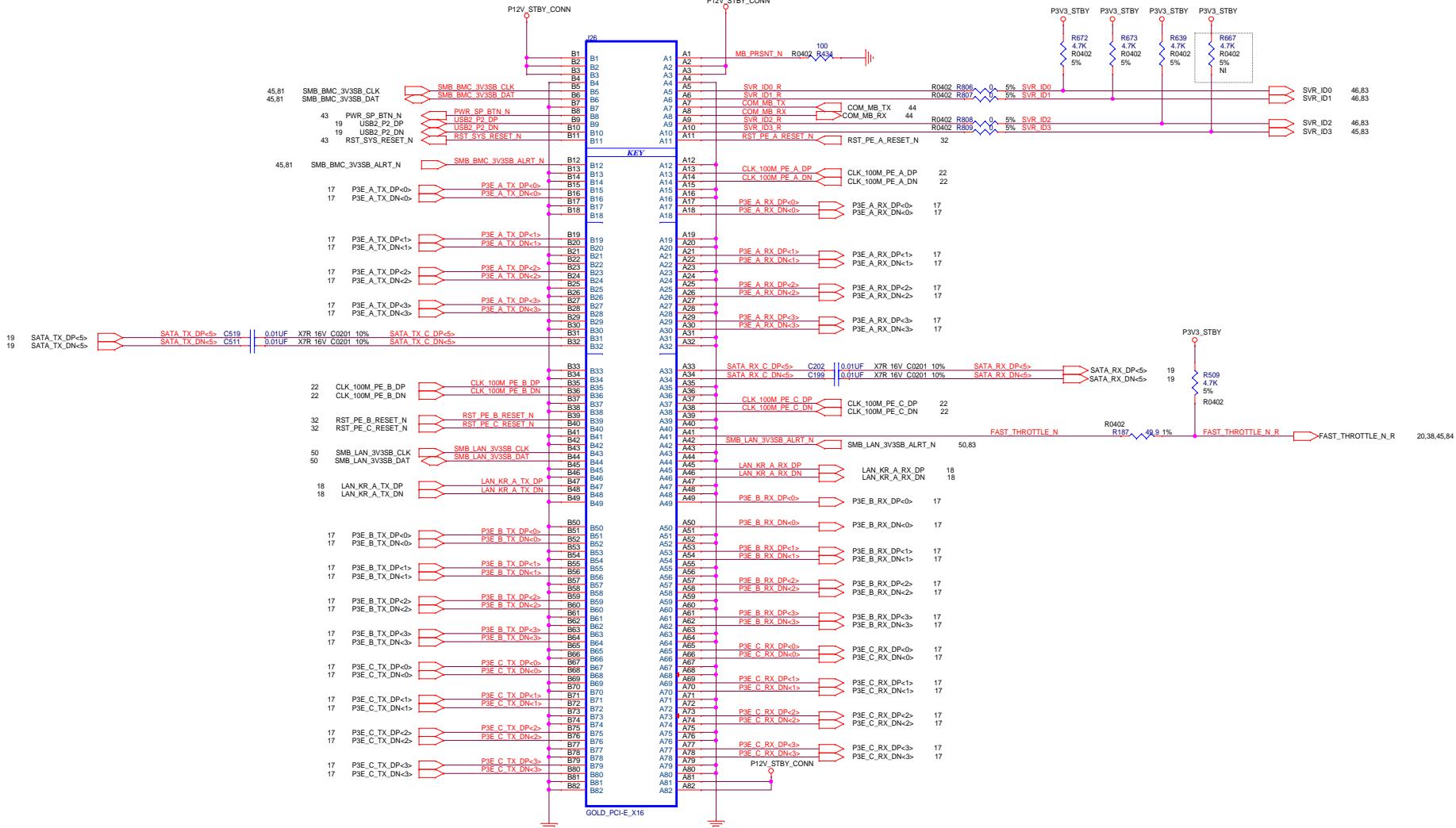


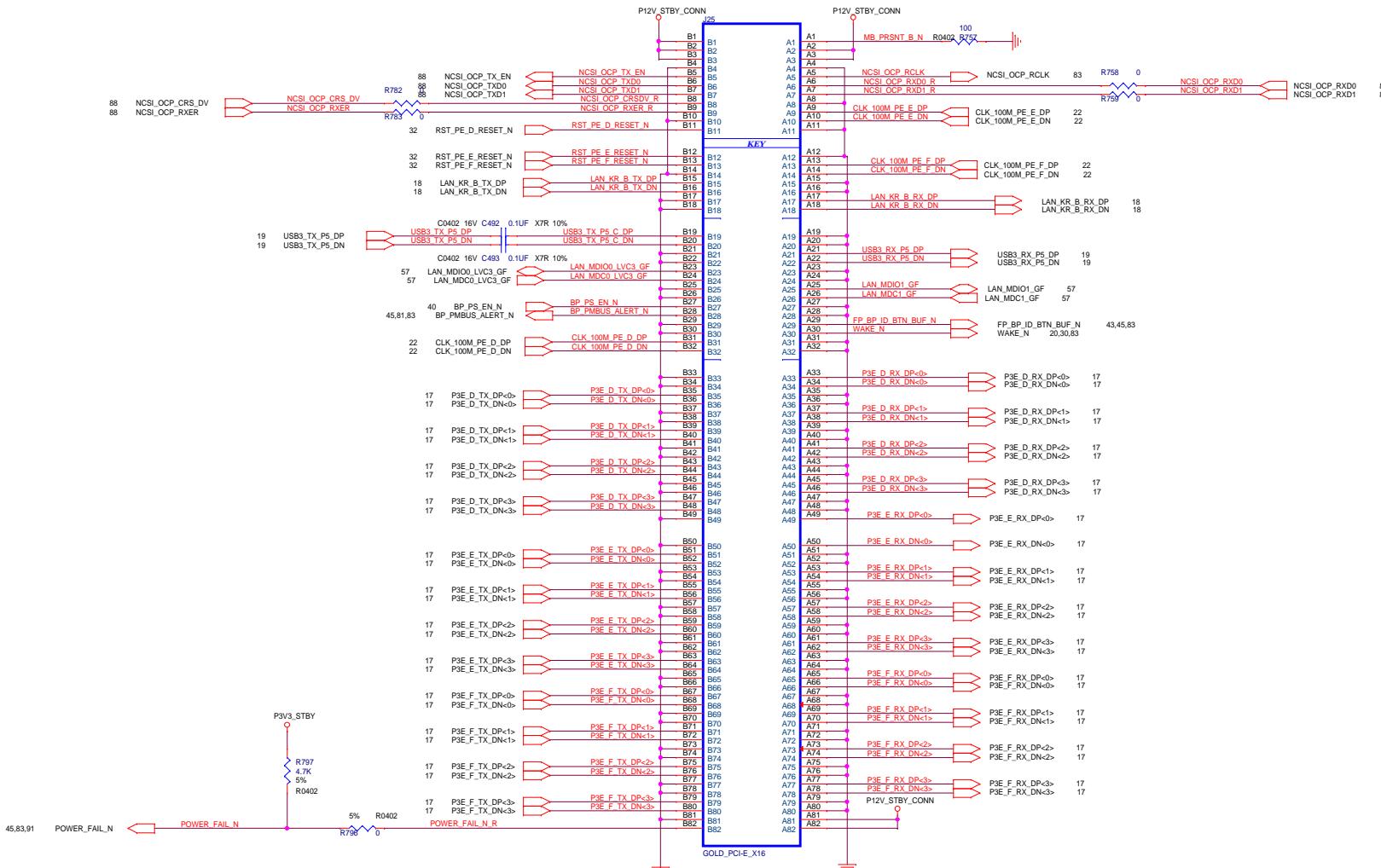


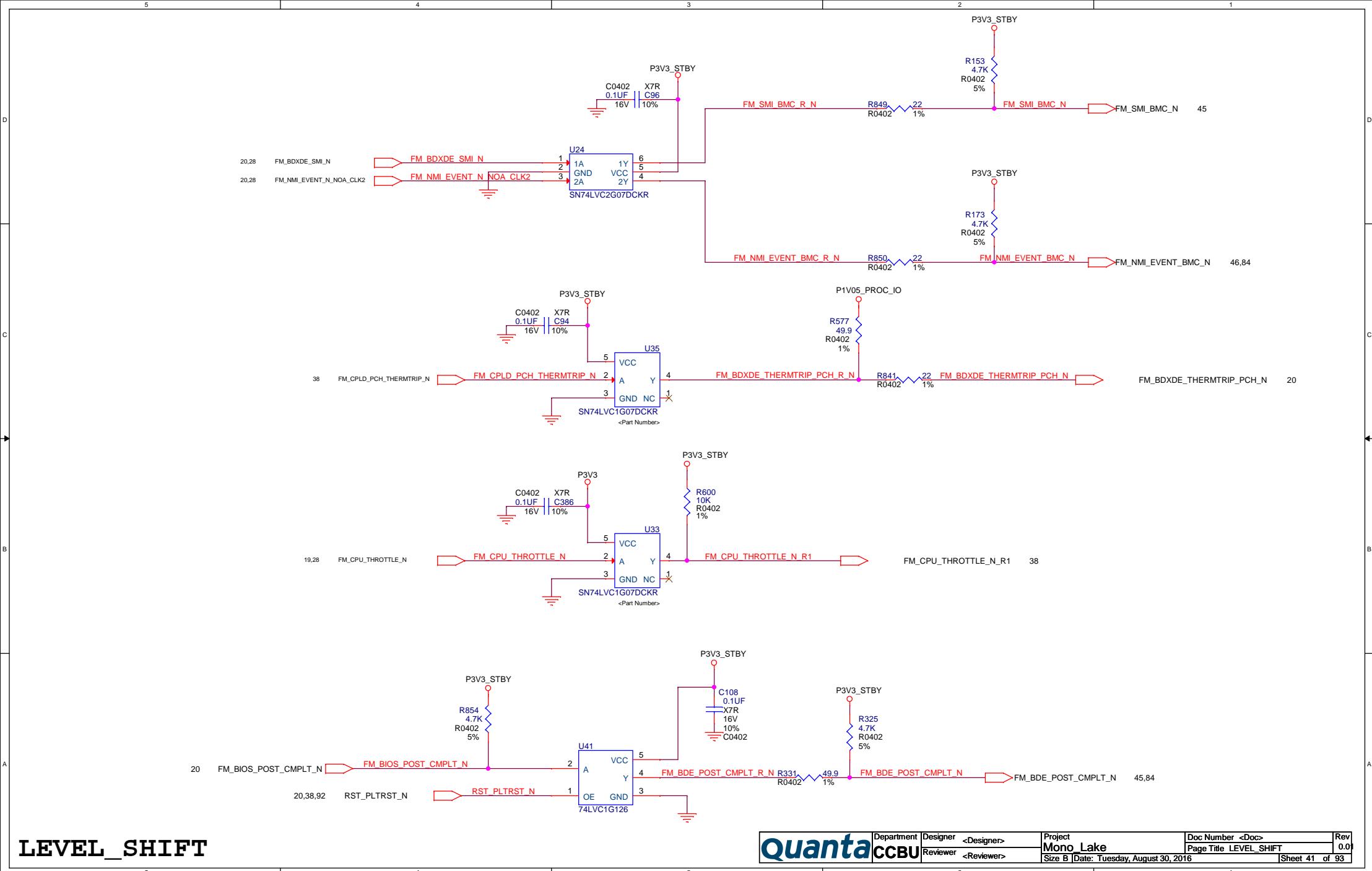






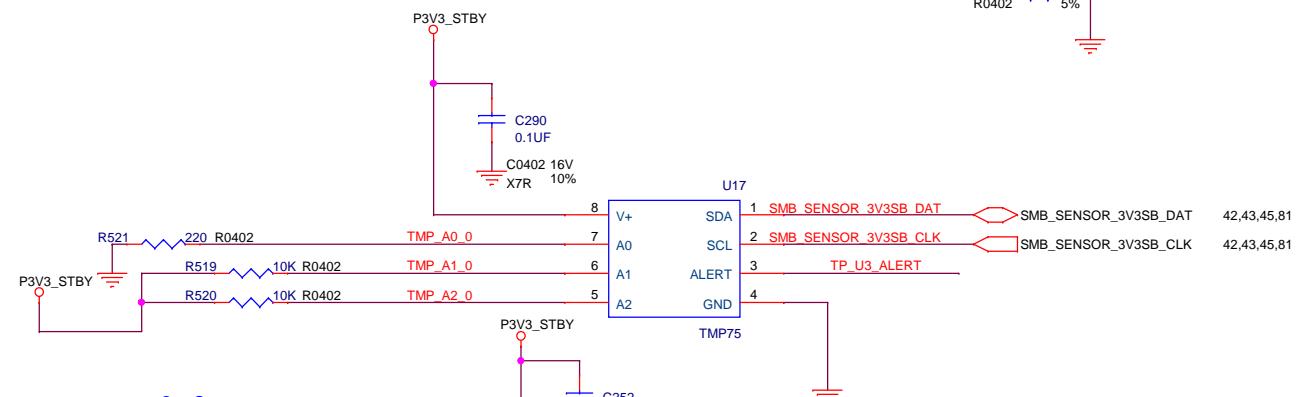
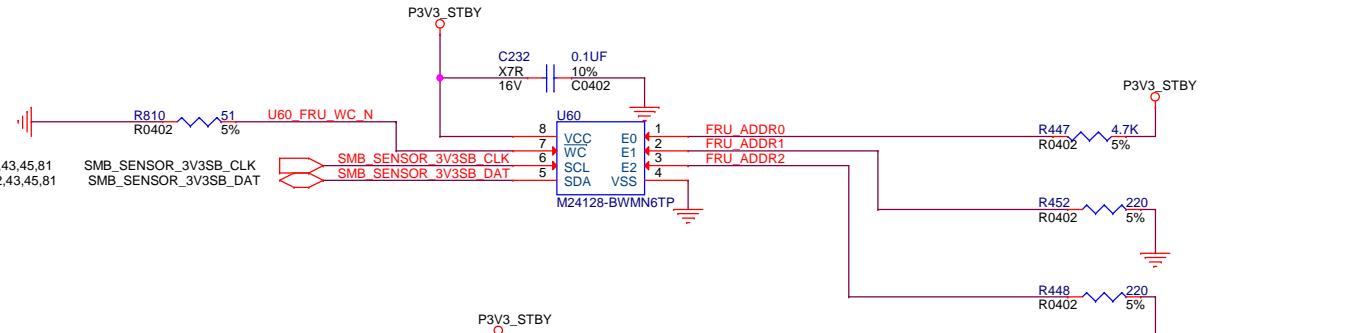




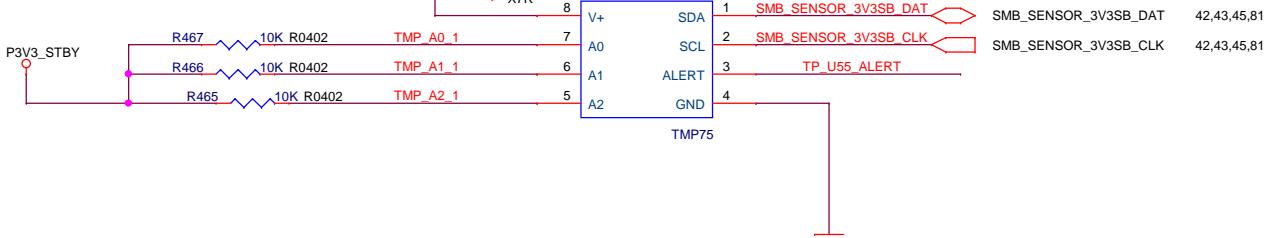


SMBus (8-bit) Address:0xA2

FRU



ADDRESS 0X9C

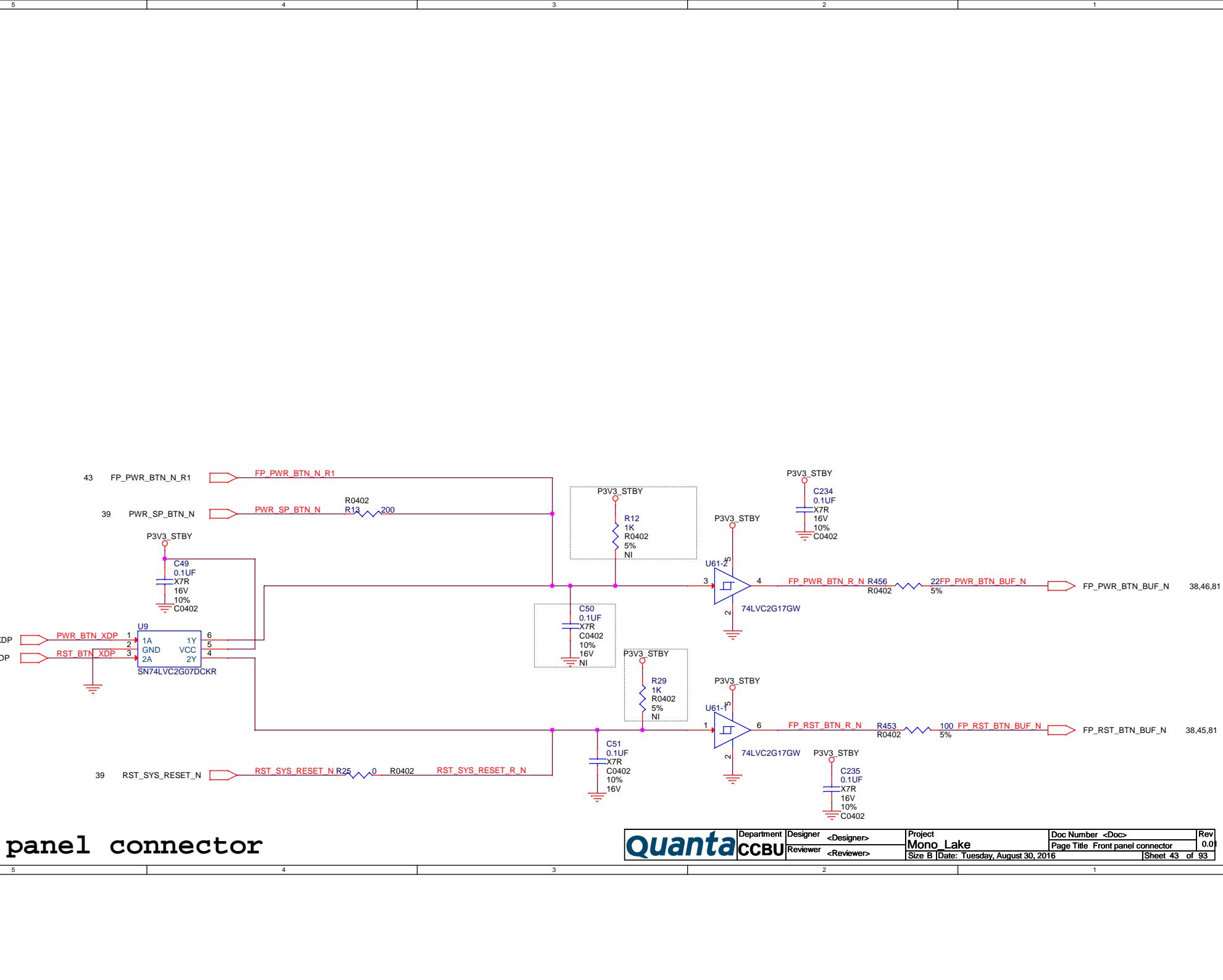


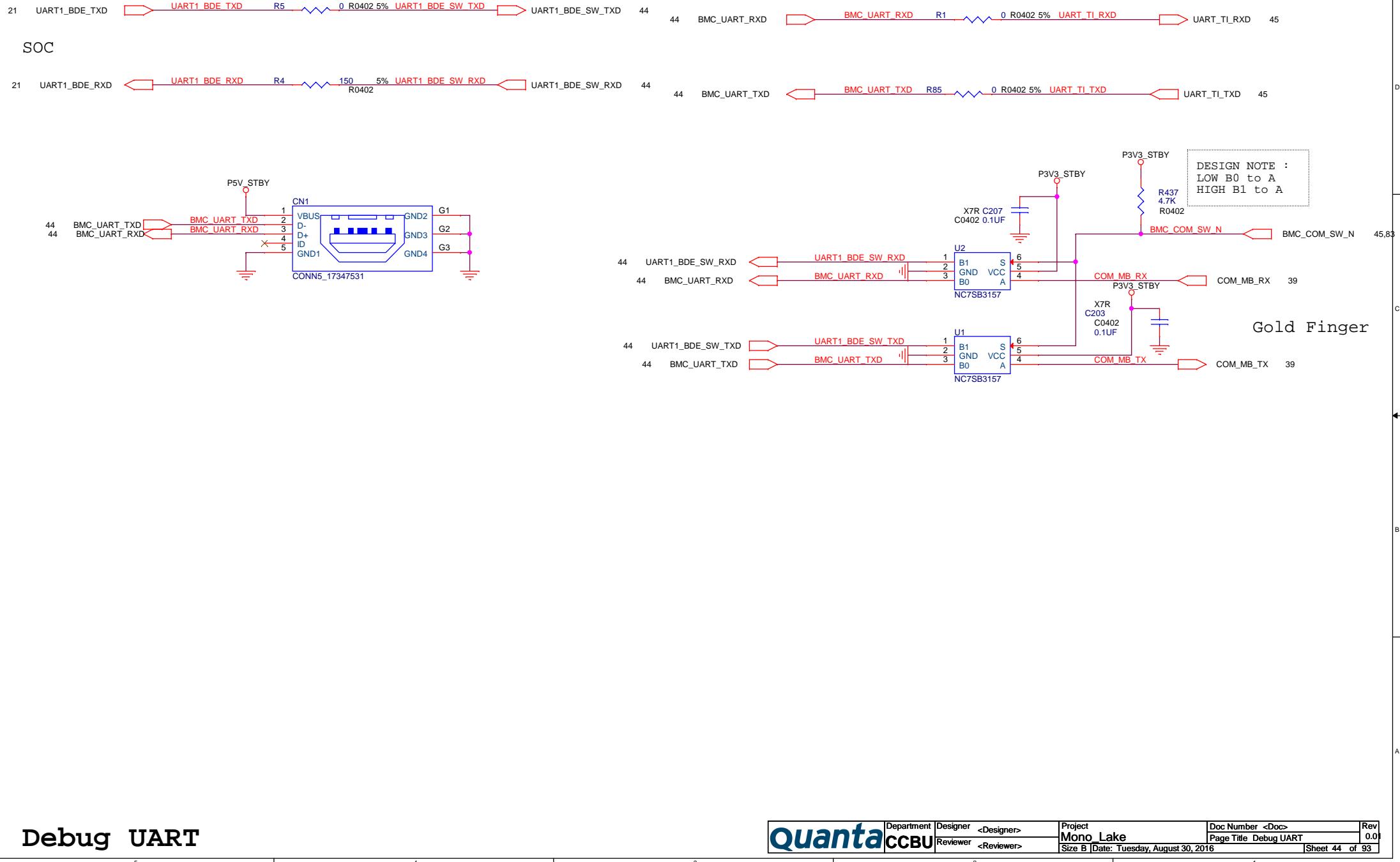
ADDRESS 0X9E

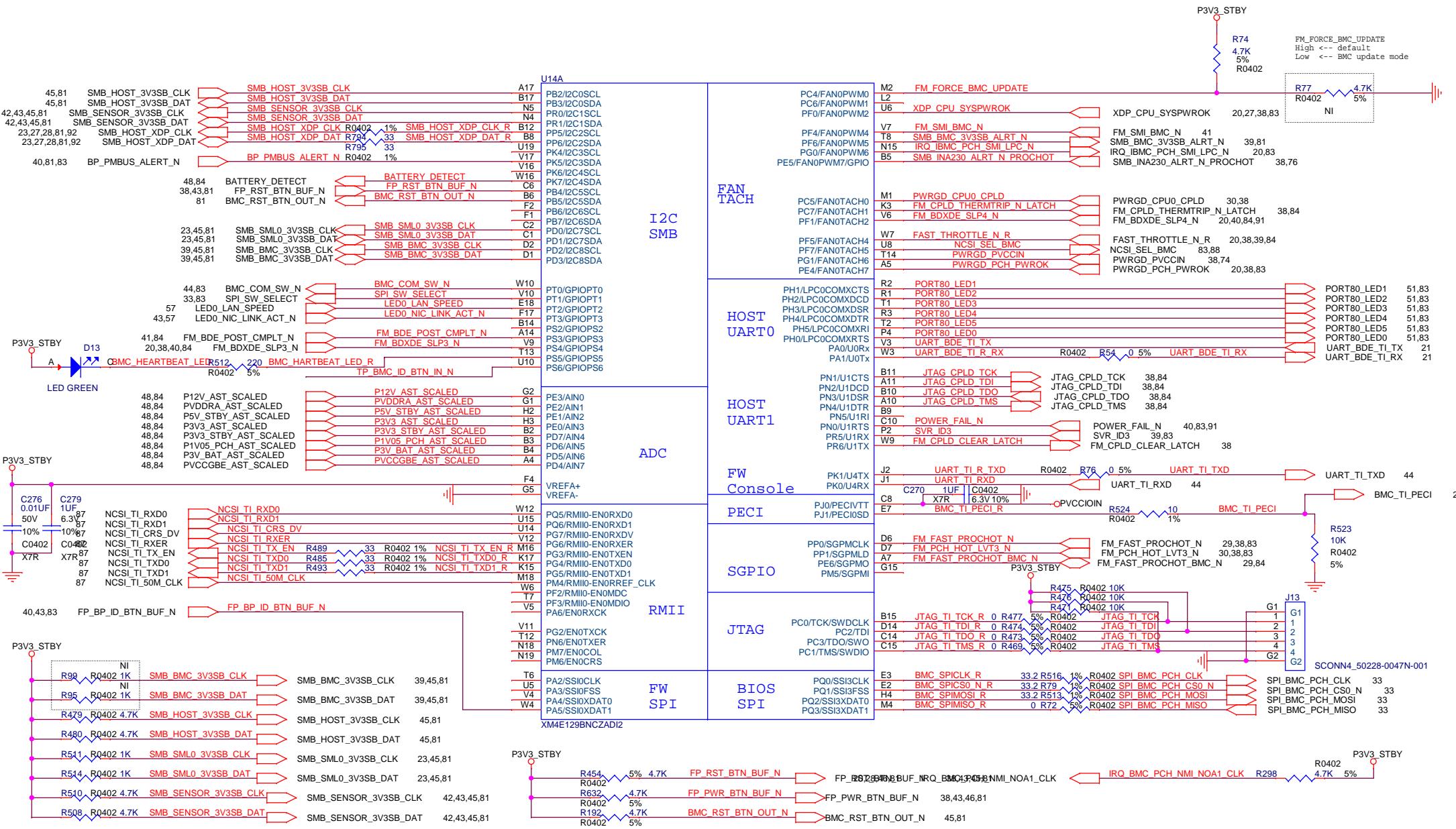
SYS_SENSOR

Quanta

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SNOWFLAKE_1

Quanta

CCBU

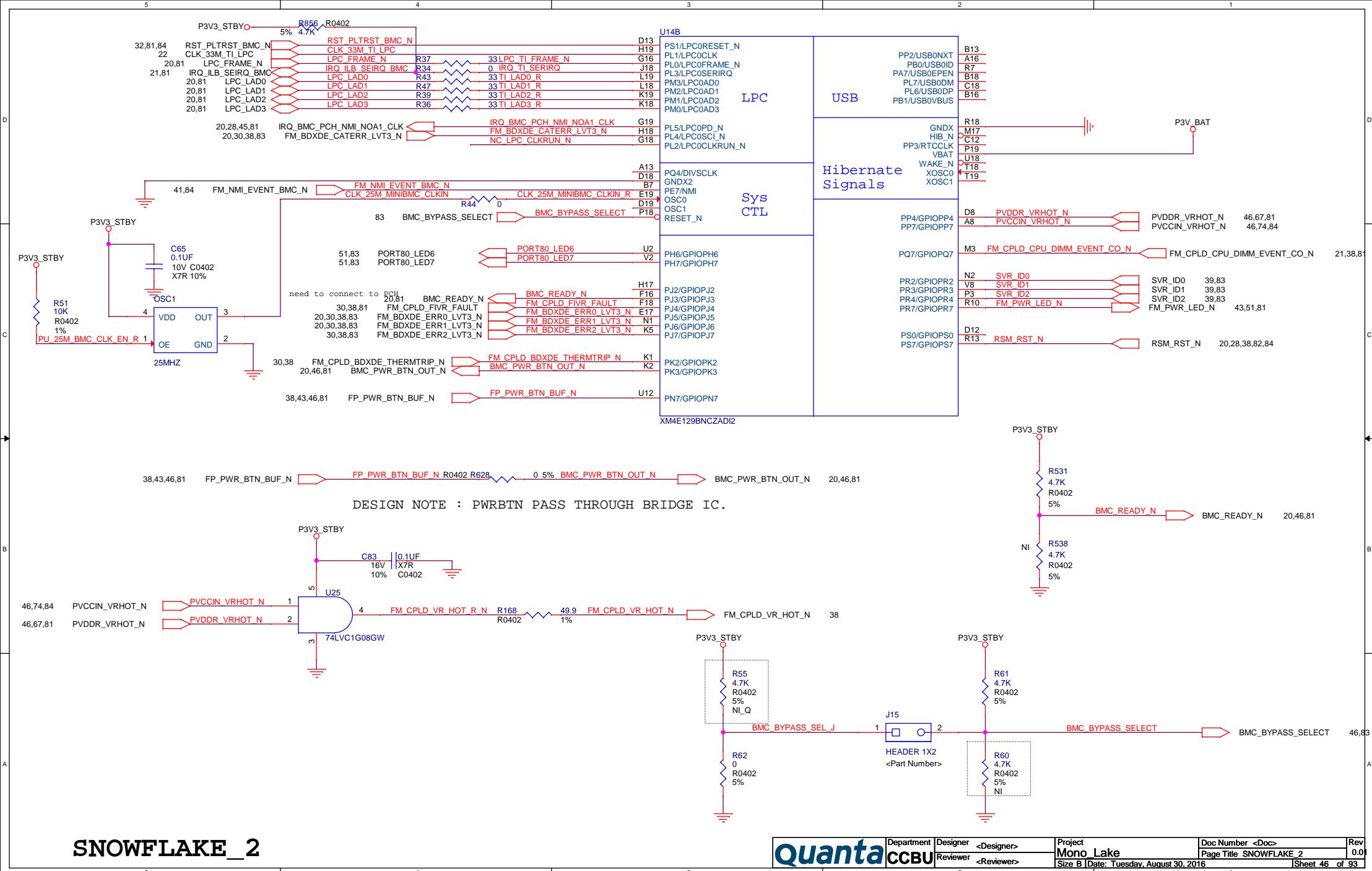
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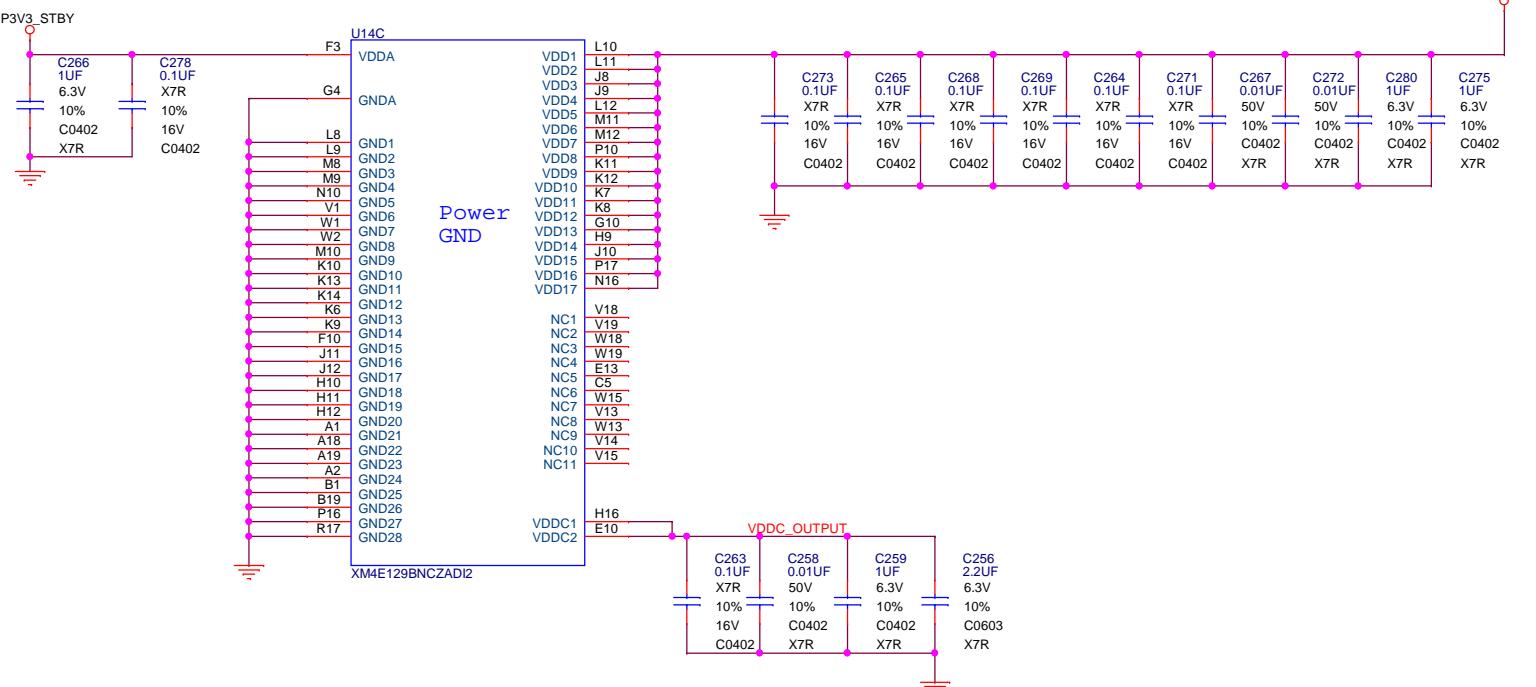
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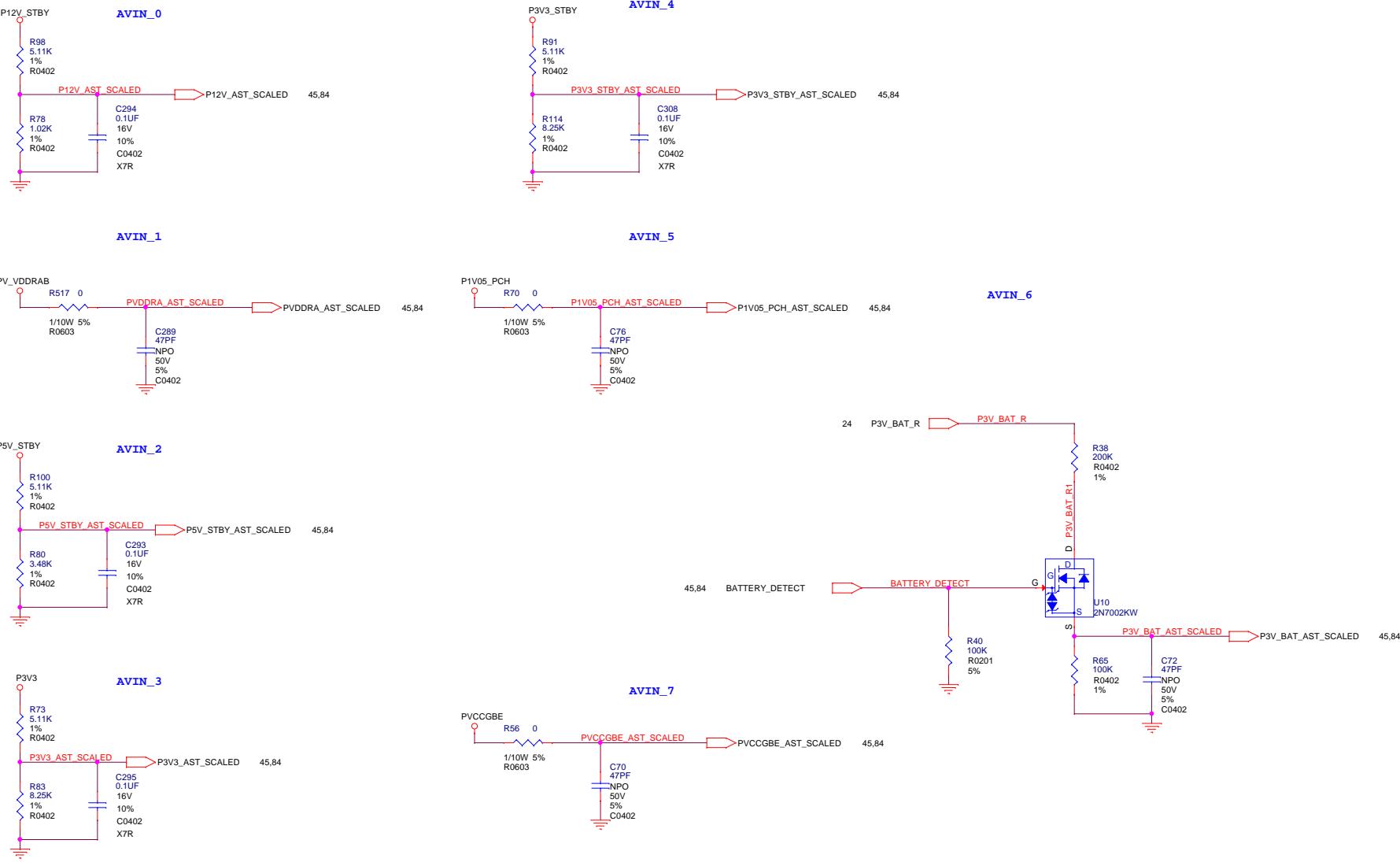


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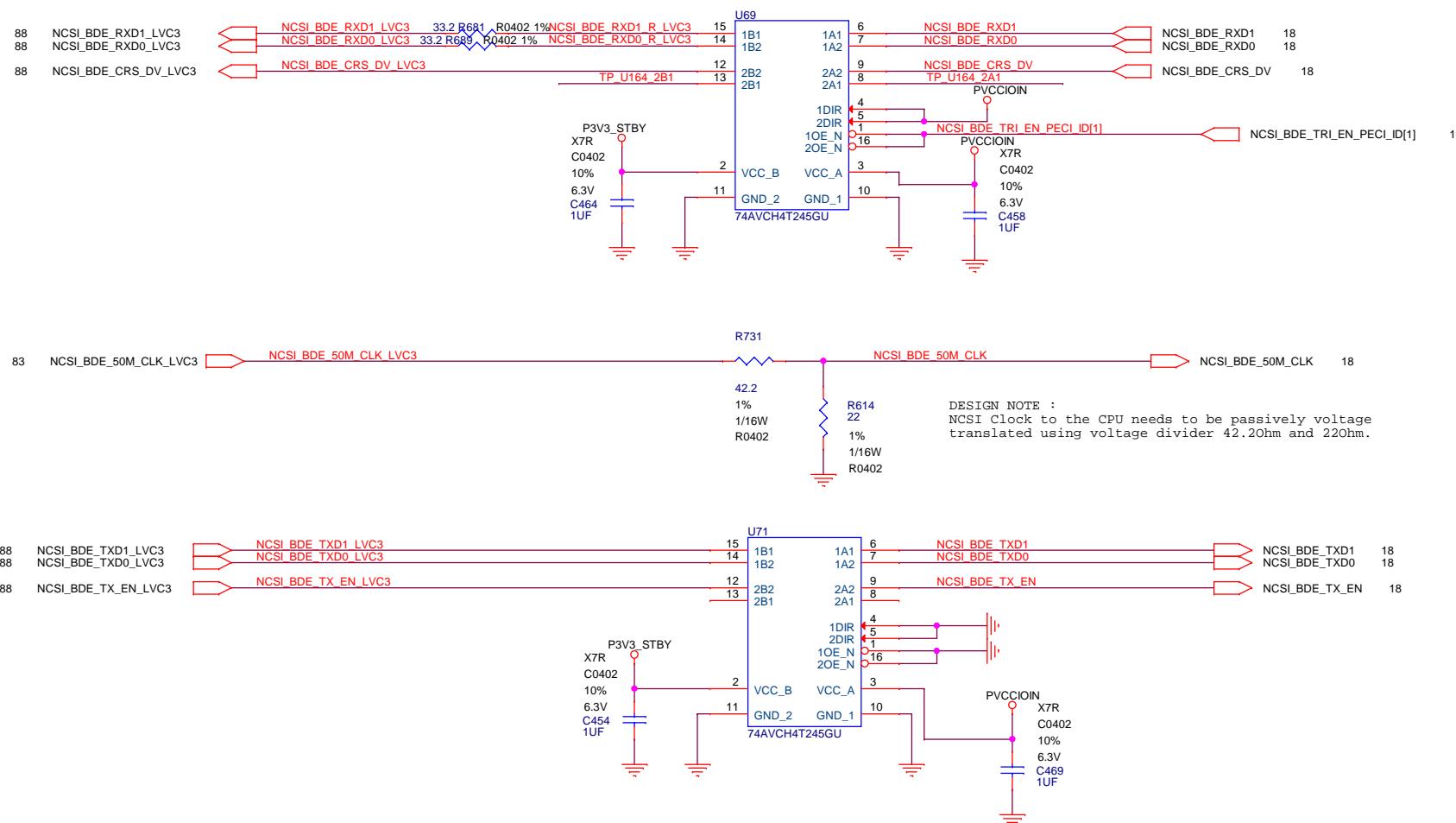


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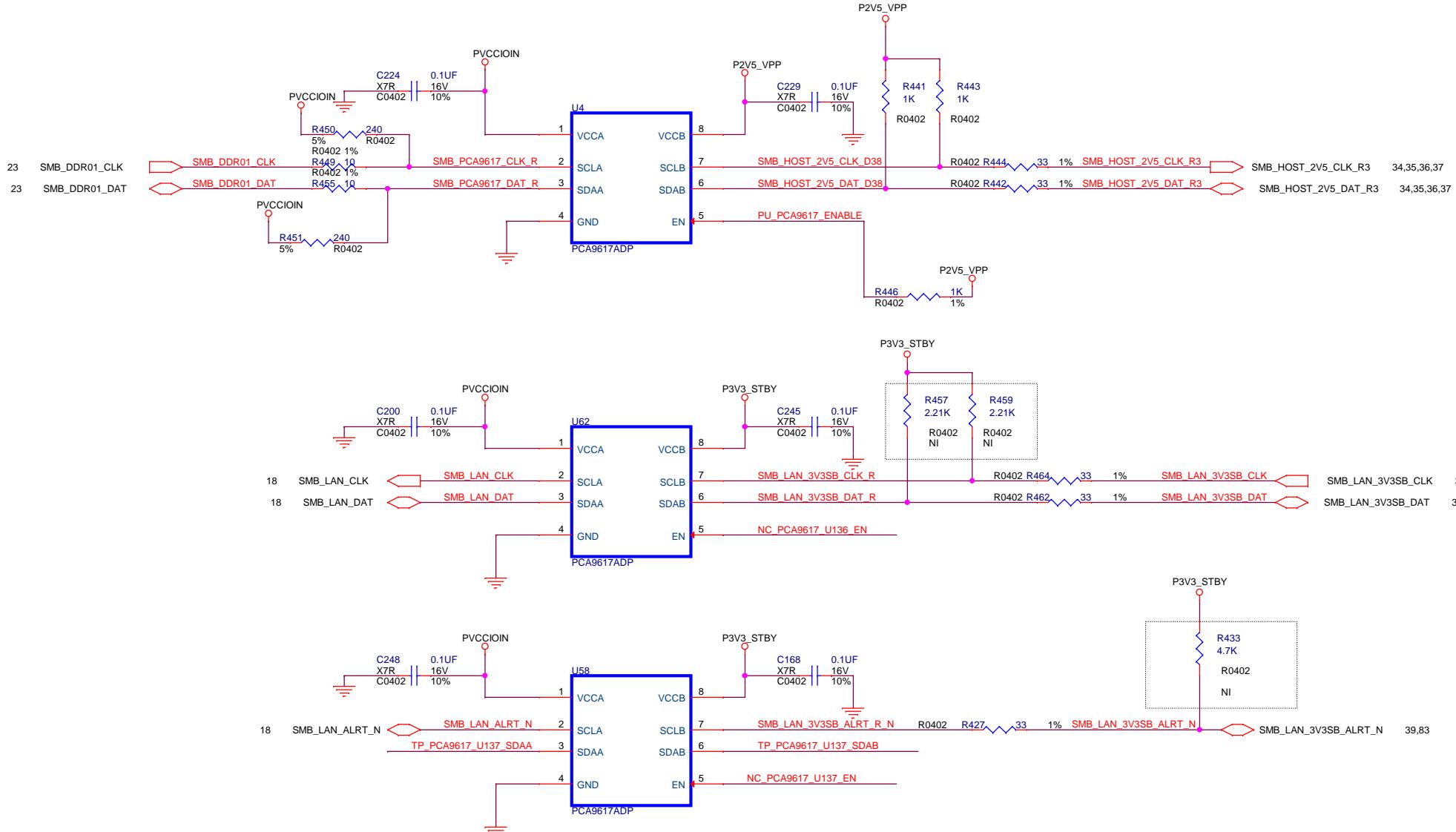
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VOLTAGE MONITOR

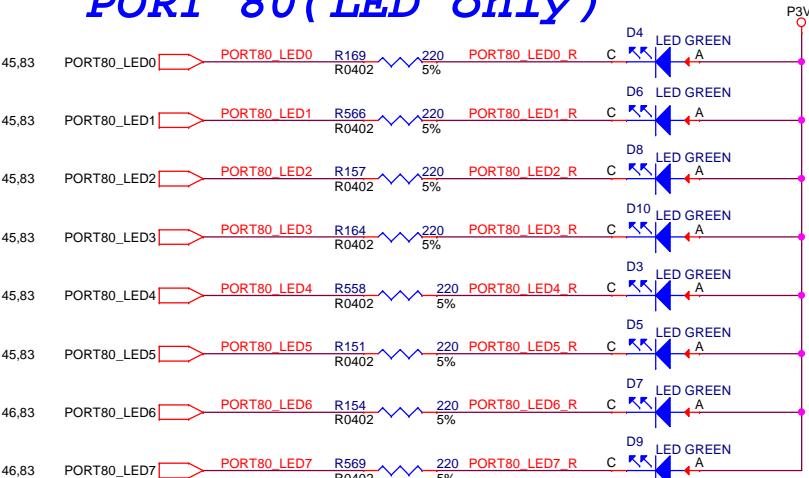


NCSI LEVEL SHIFT

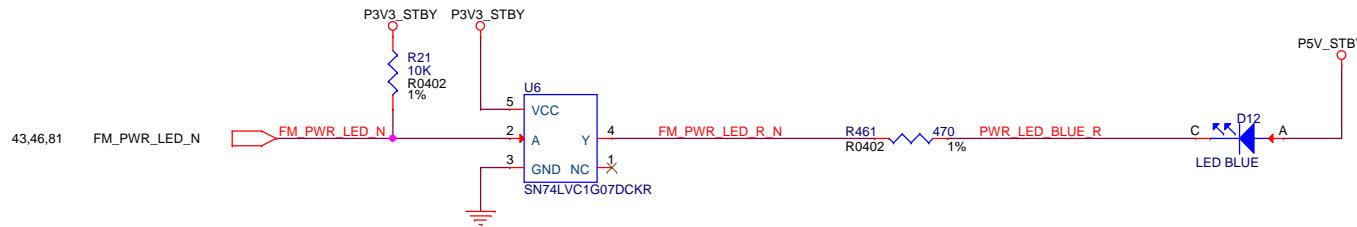


SMBUS ISOLATOR

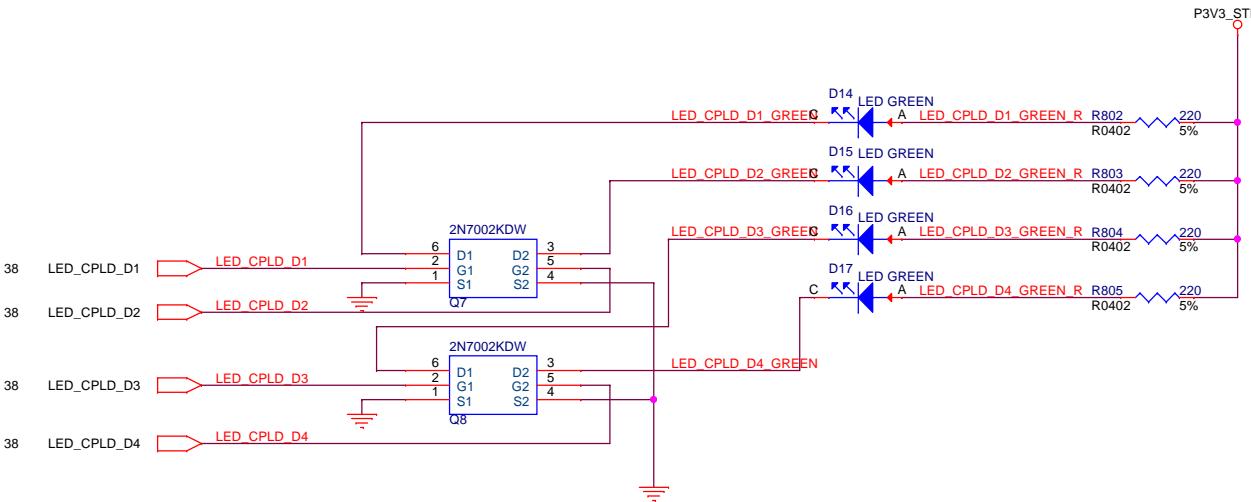
PORT 80 (LED only)



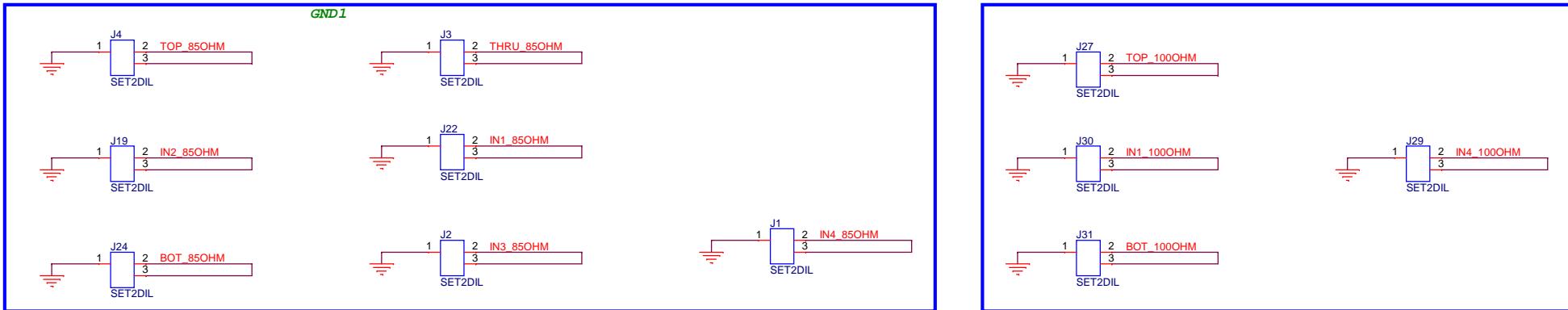
POWER LED (BLUE)



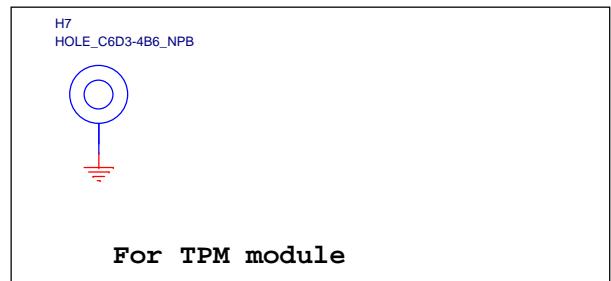
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SET2DEL



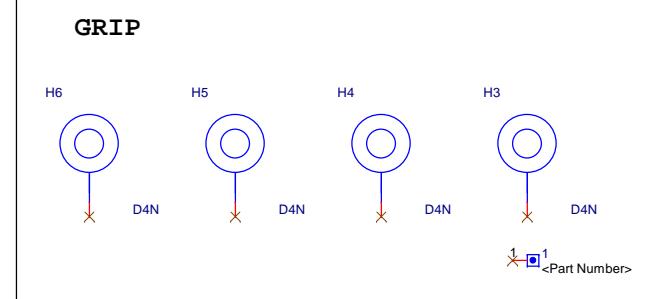
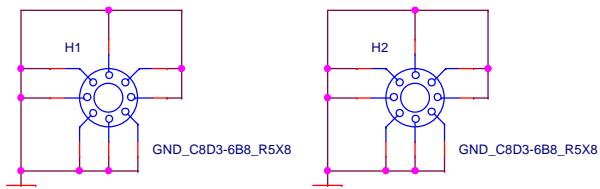
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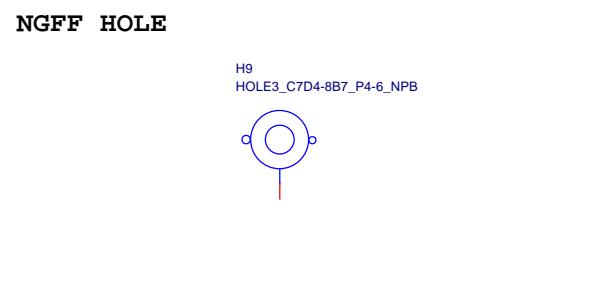
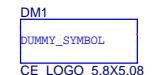
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 TP_SCREW_1
 TP_SCREW_2
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 TP BIOS_LABEL

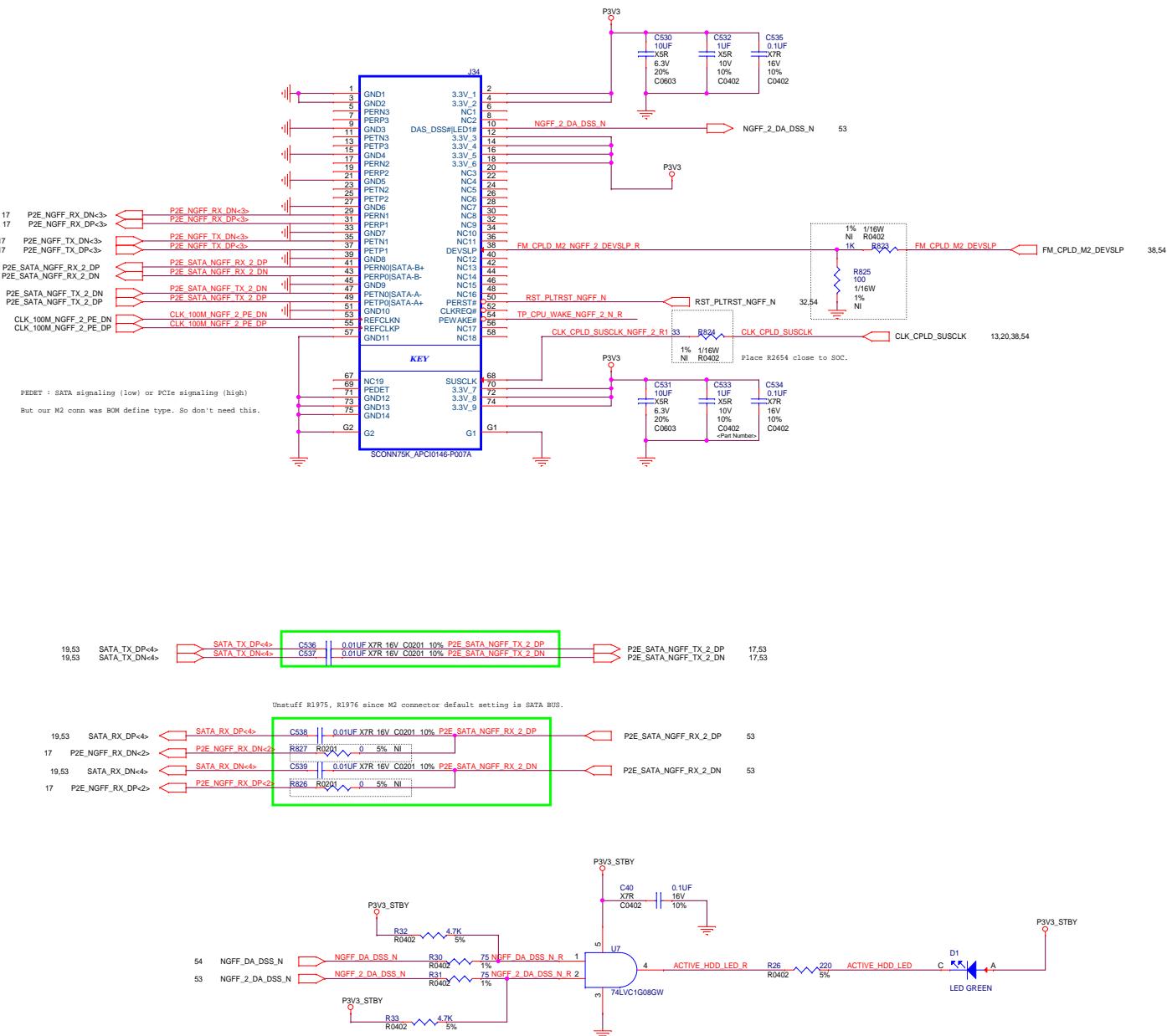
For TPM module

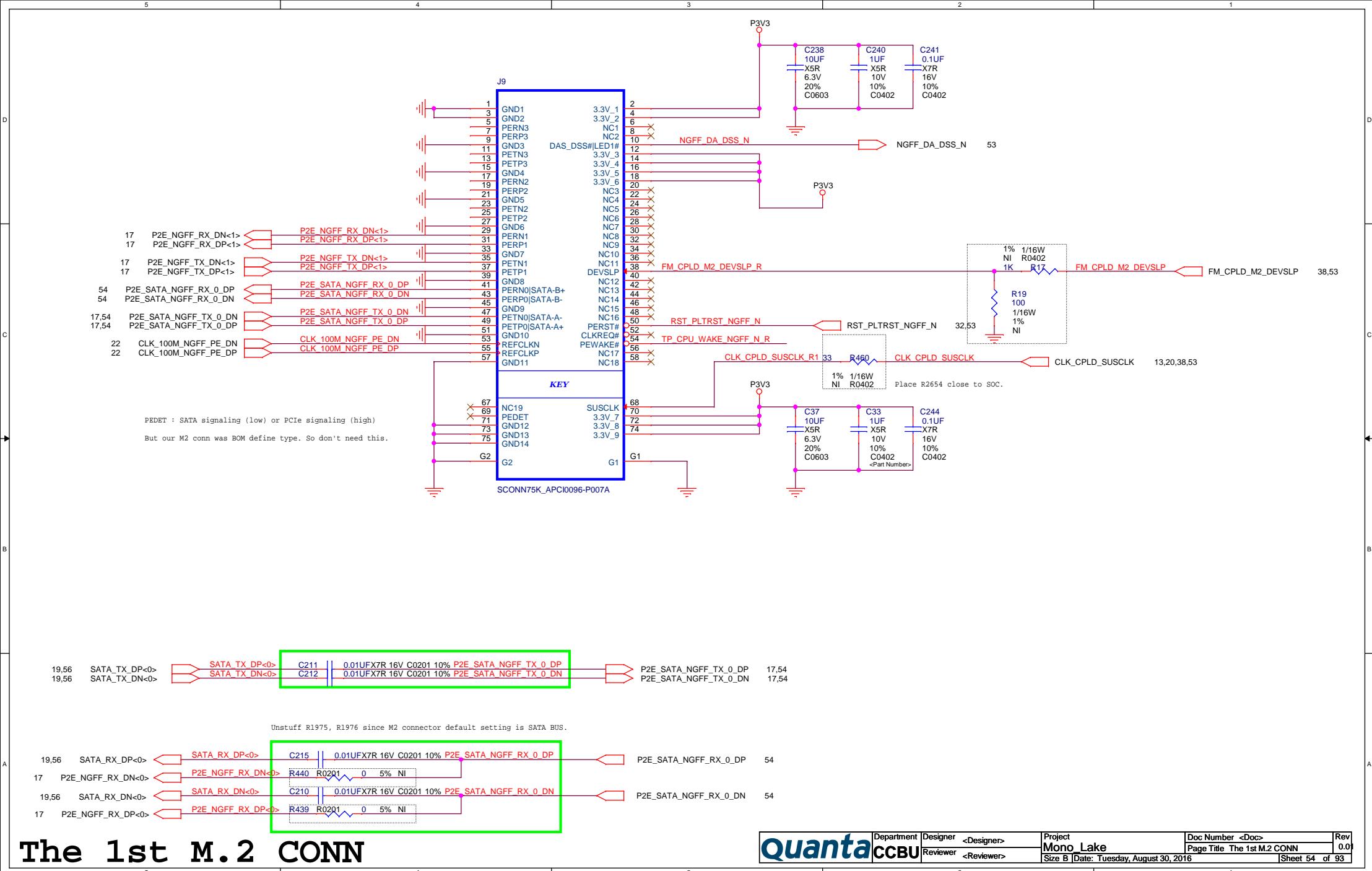
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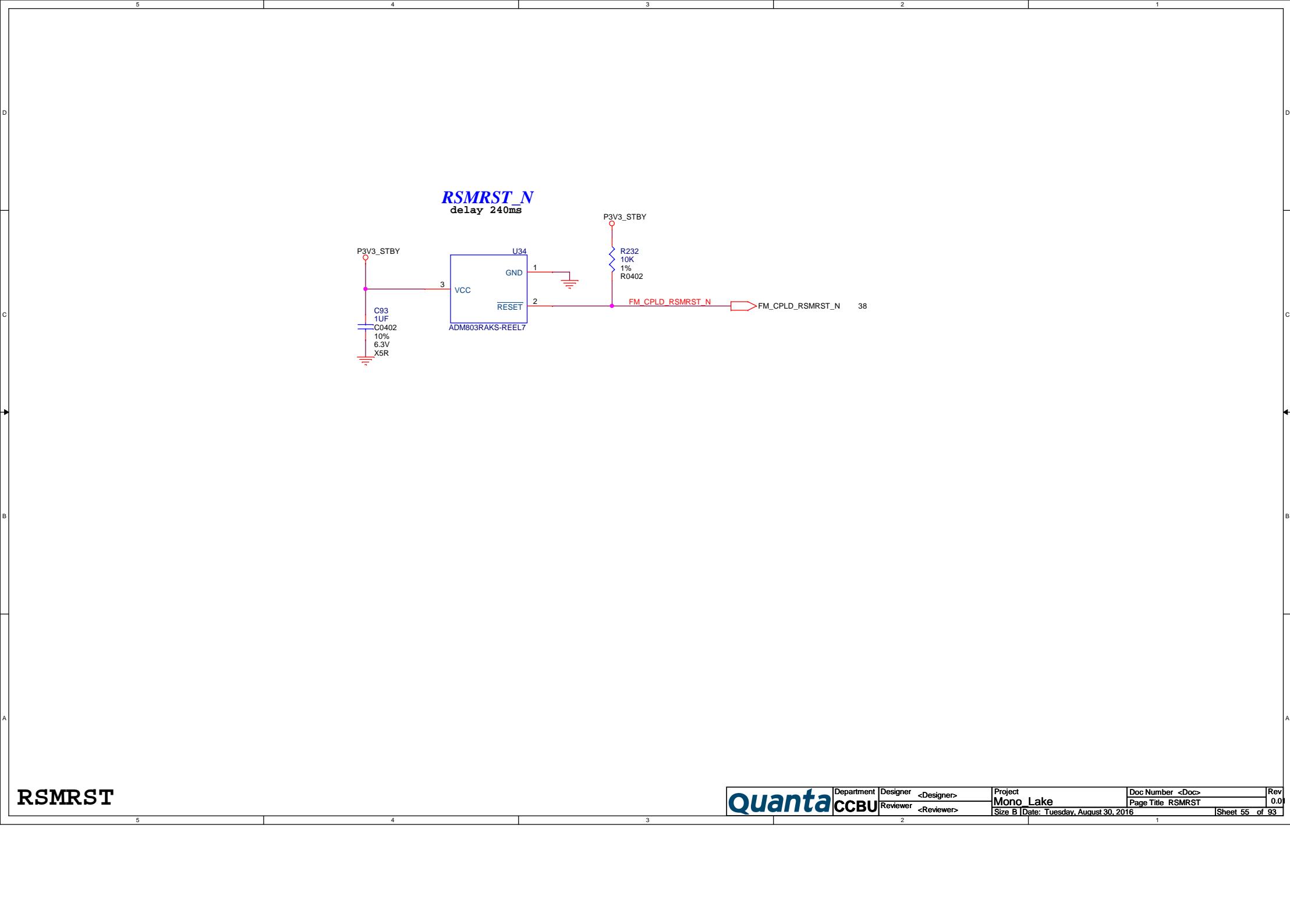


CE Logo









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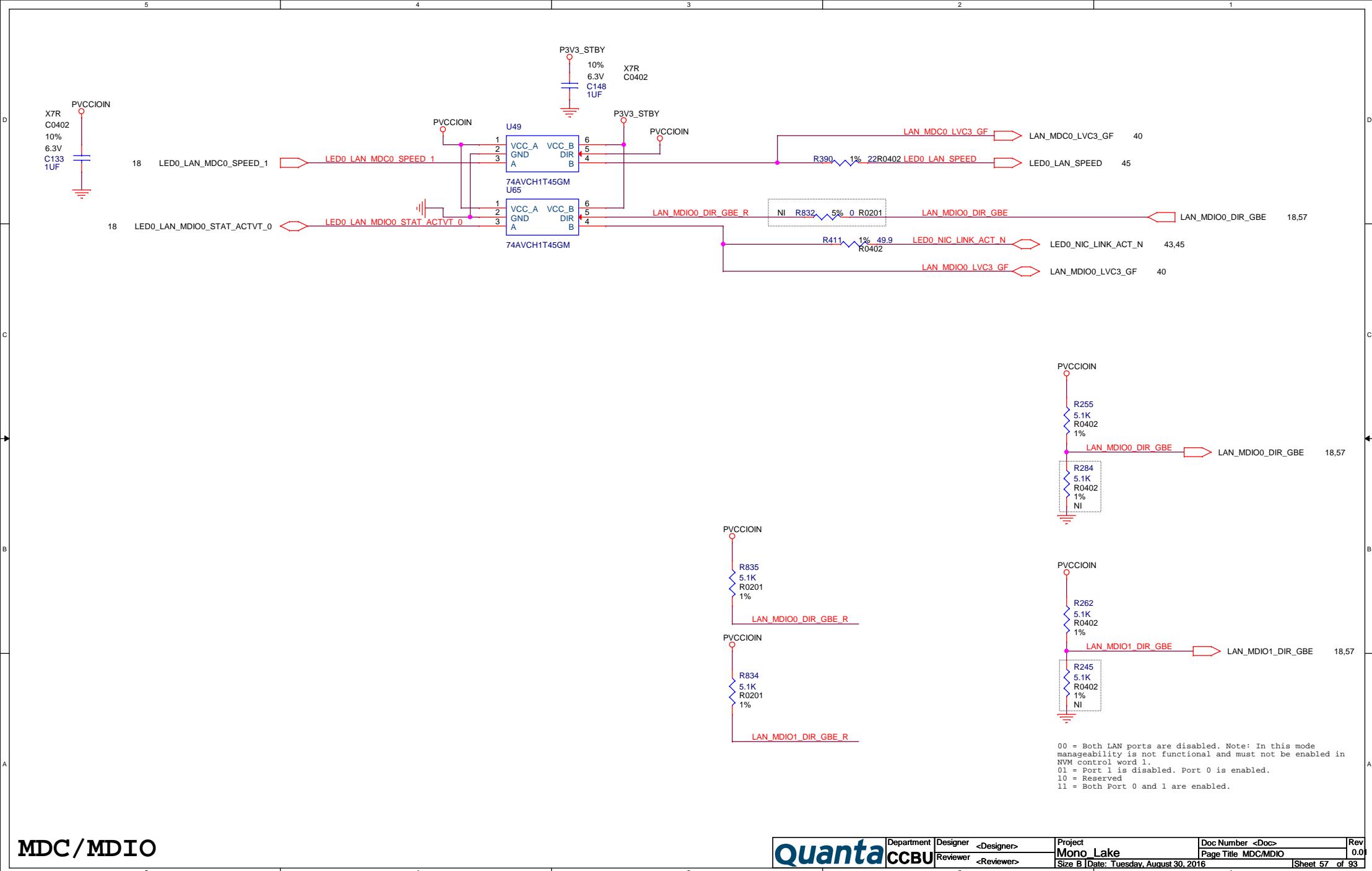
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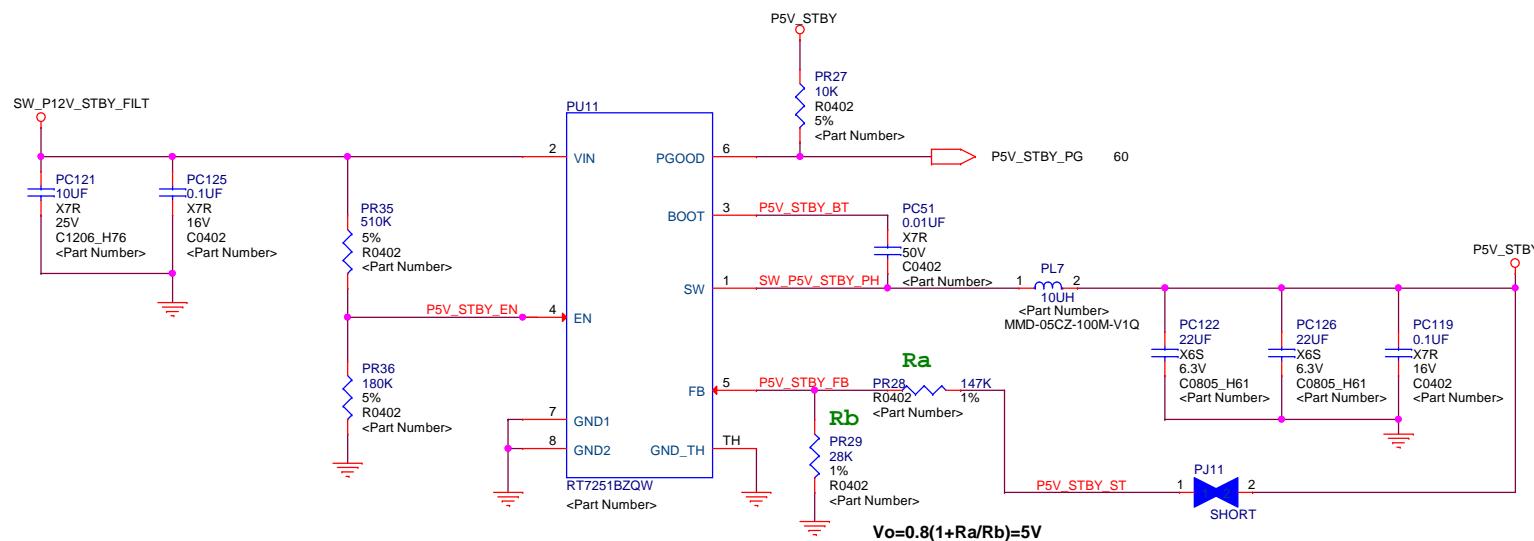
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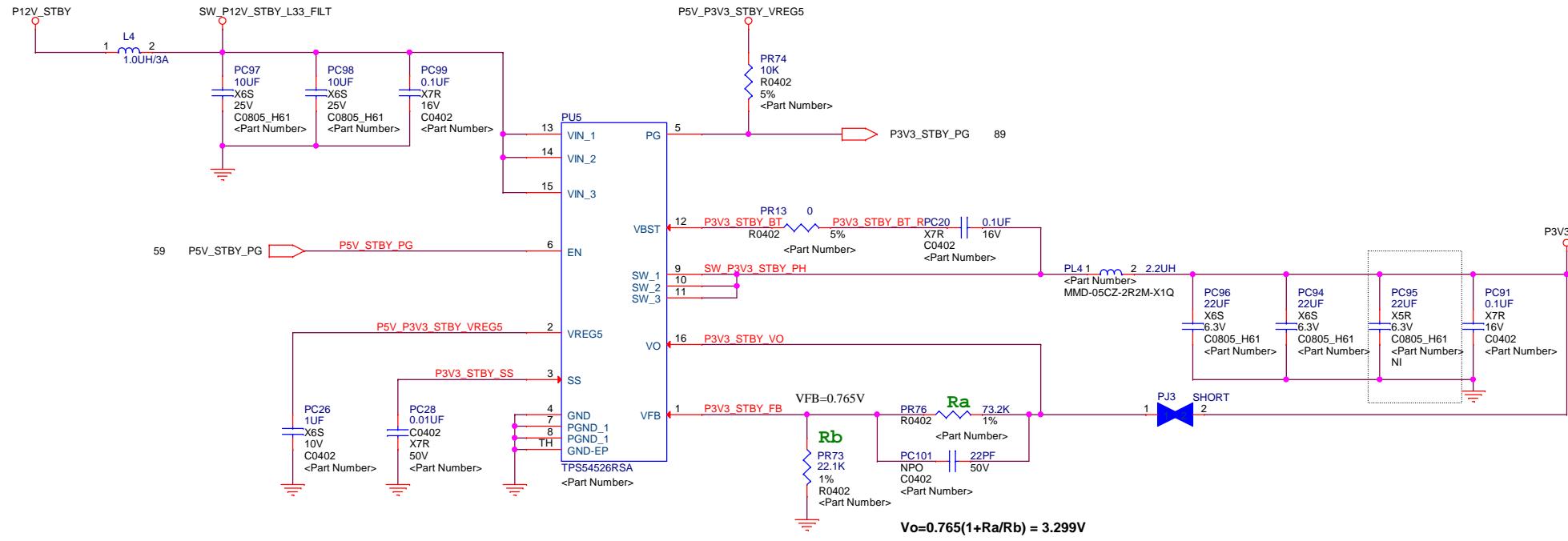
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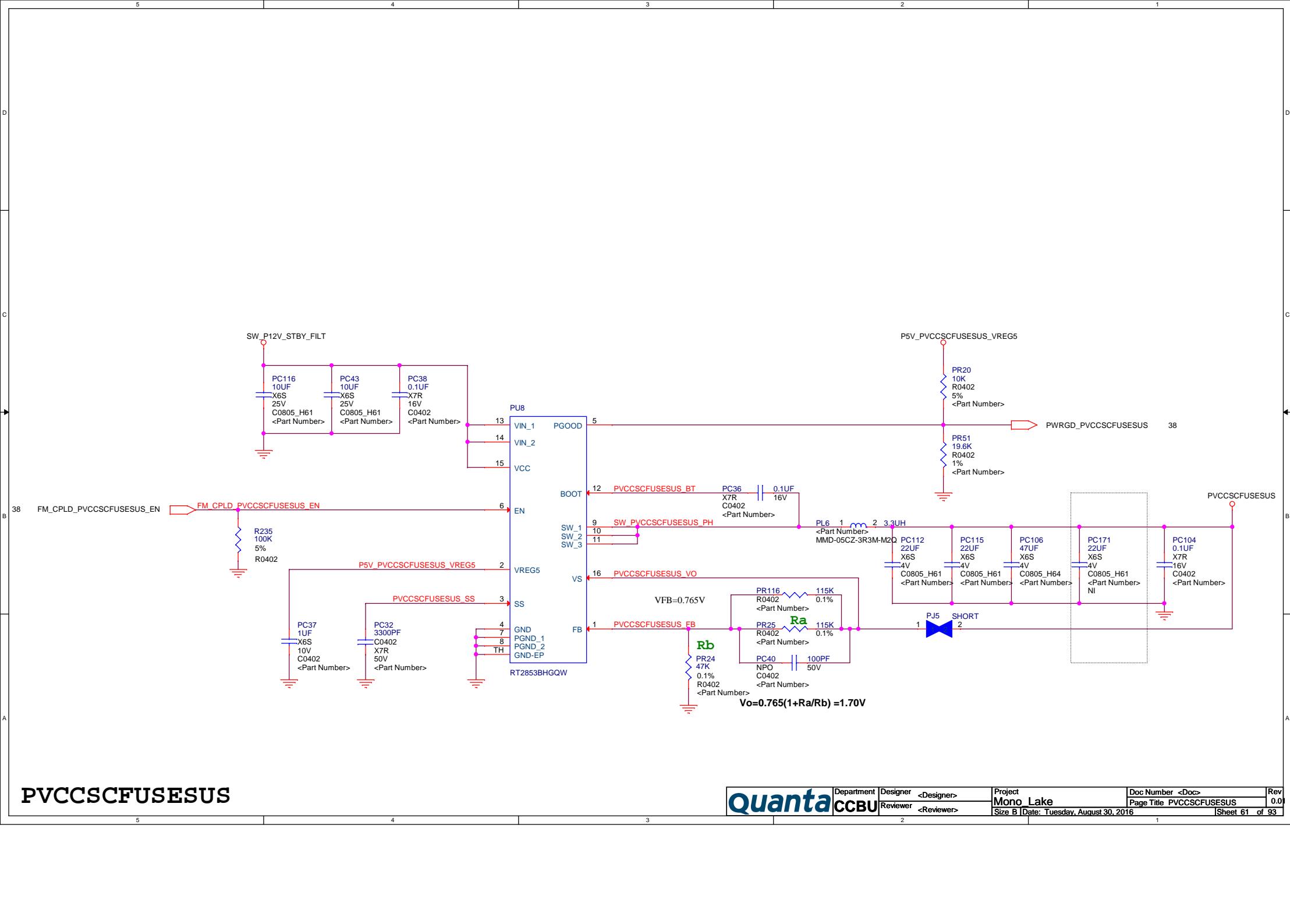
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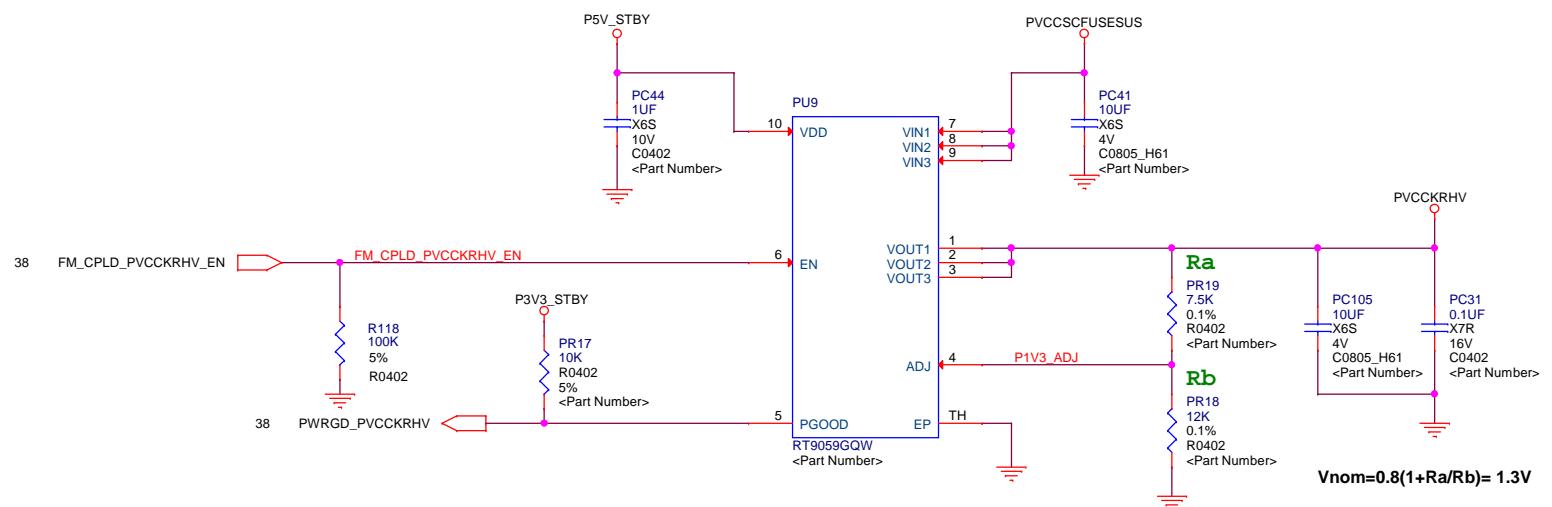


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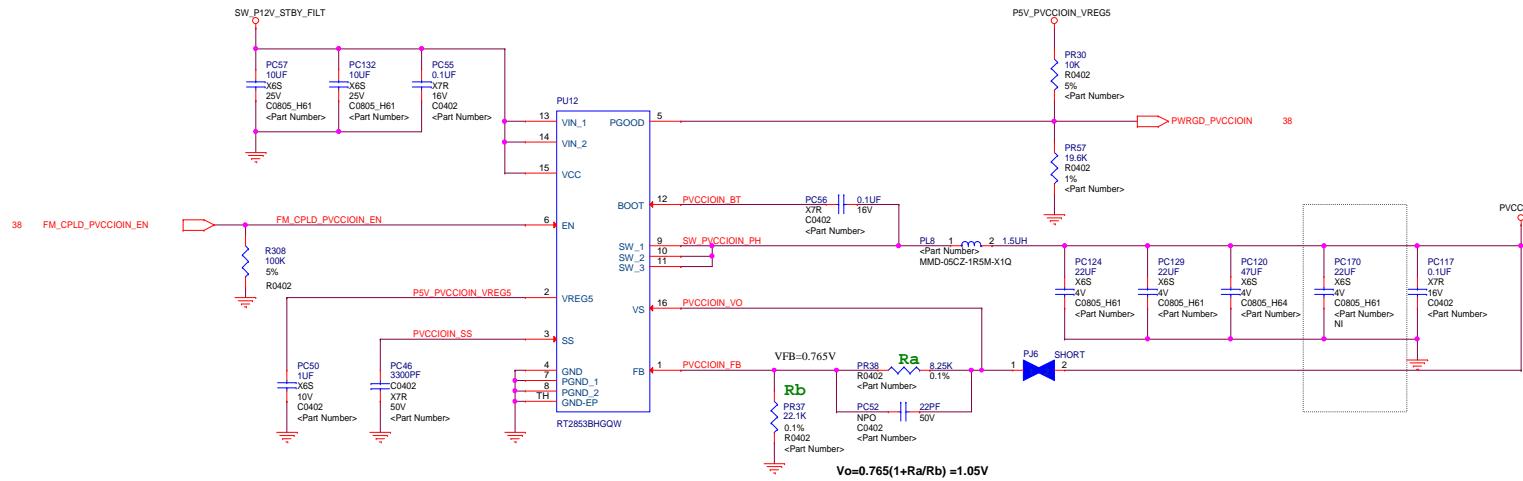




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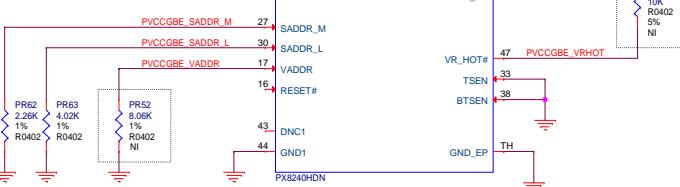
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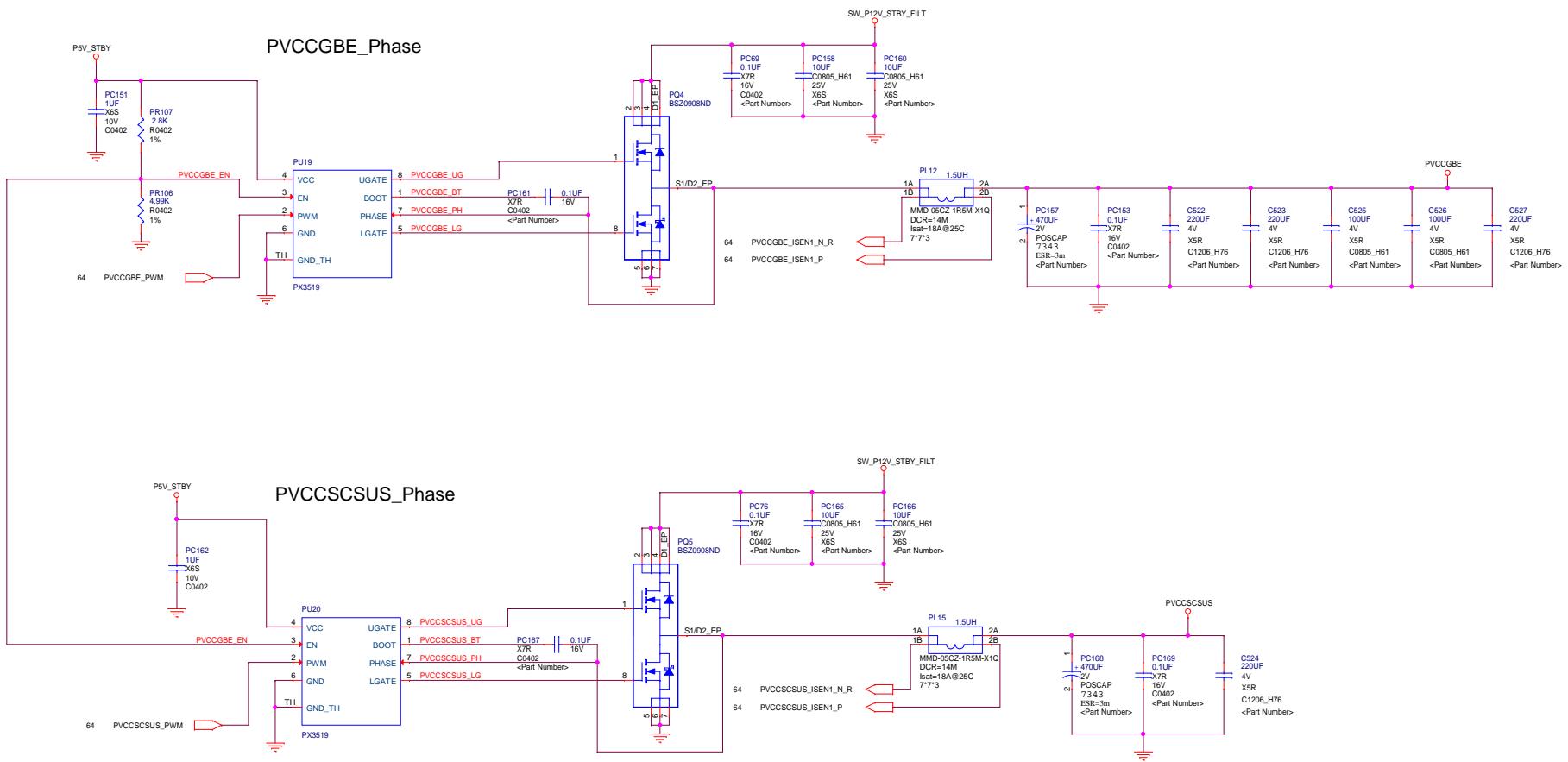


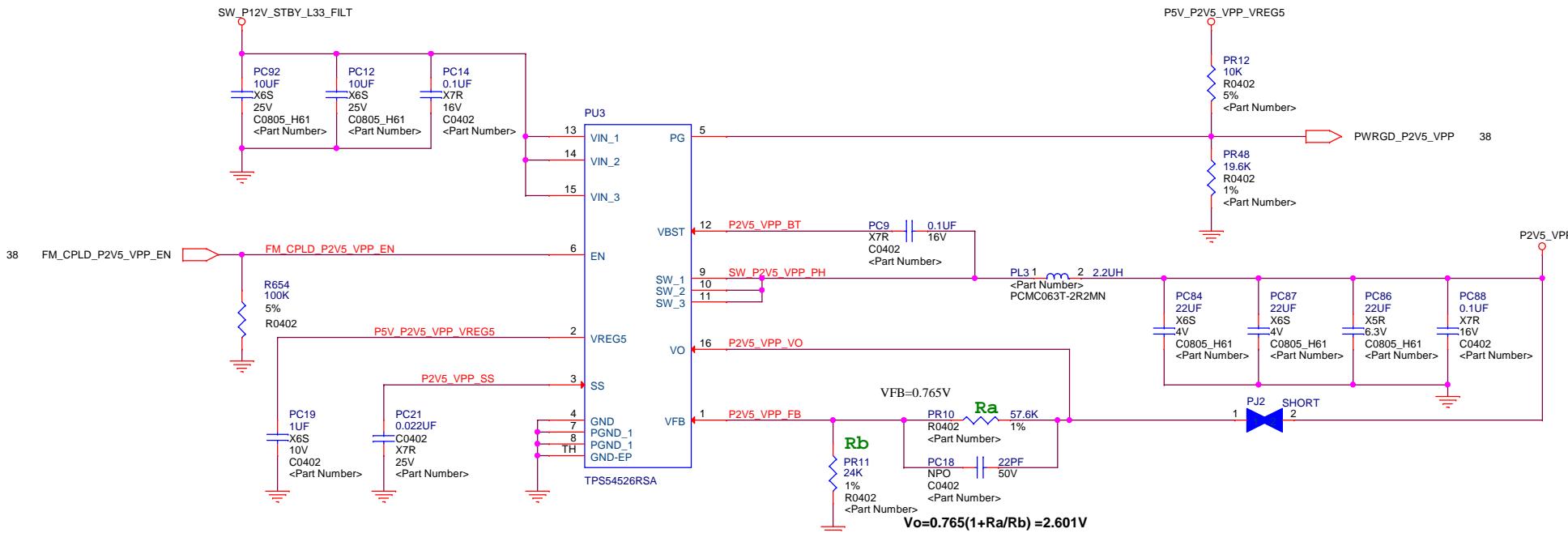
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3.16				98	78	58	38	18	
4.02				94	74	54	34	14	
5.06				90	70	50	30	10	
8.06				8C	6C	4C	2C	0C	
16.0				88	68	48	28	08	
OPEN	E0	C0	A0	80	60	40	20	00	RESERVED

I2C ADDRESS TABLE									
SADDR_L	2.26	2.67	3.16	4.02	5.36	8.06	16.0	OPEN	
2.26	FC	DC	BC	9C	7C	5C	3C	1C	
2.67	F8	D8	B8	98	78	58	38	18	
3.16	F4	D4	B4	94	74	54	34	14	
4.02	F0	D0	B0	90	70	50	30	10	
5.36	EC	CC	AC	8C	6C	4C	2C	0C	
8.06	E8	C8	A8	88	68	48	28	08	
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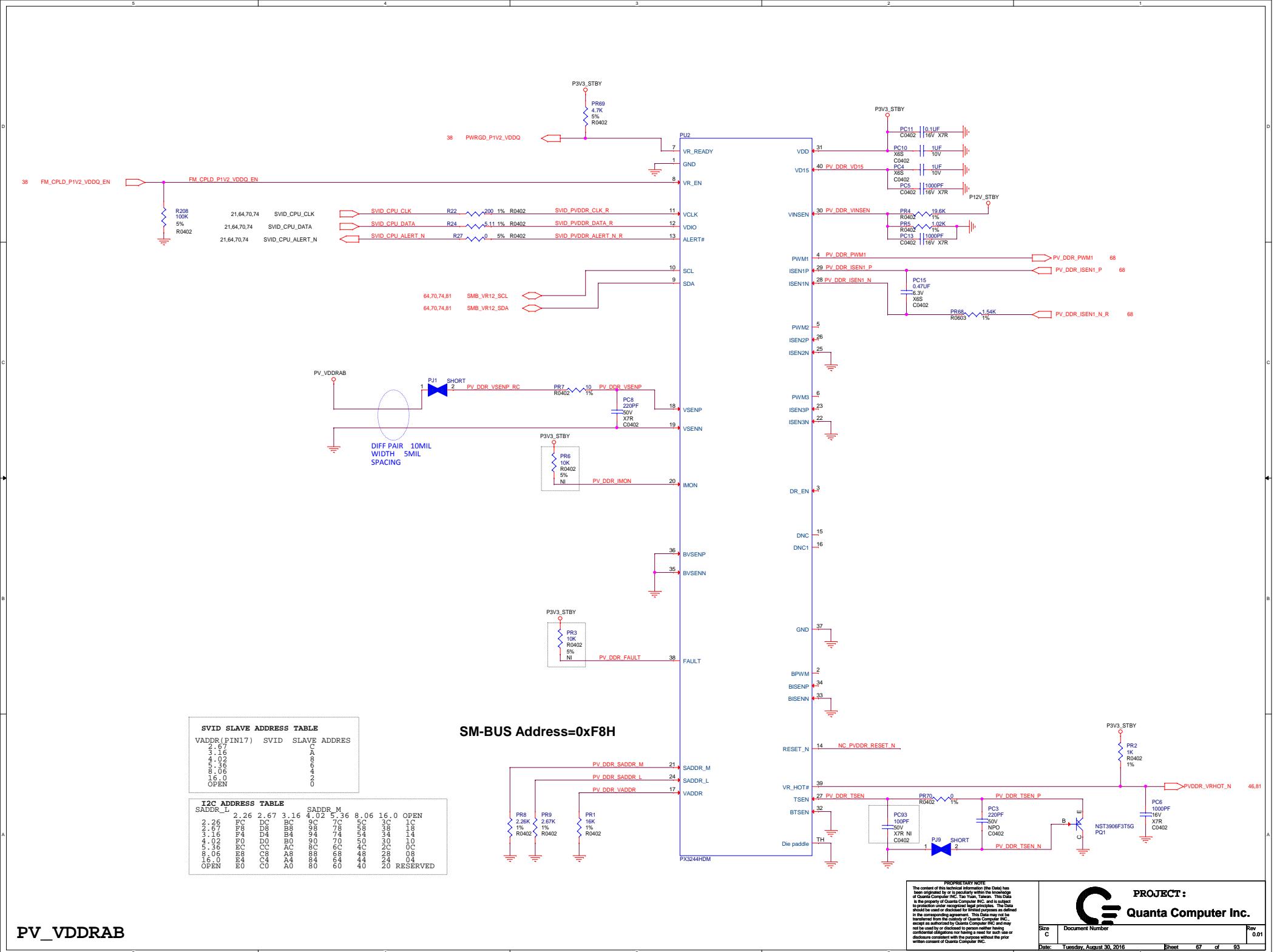


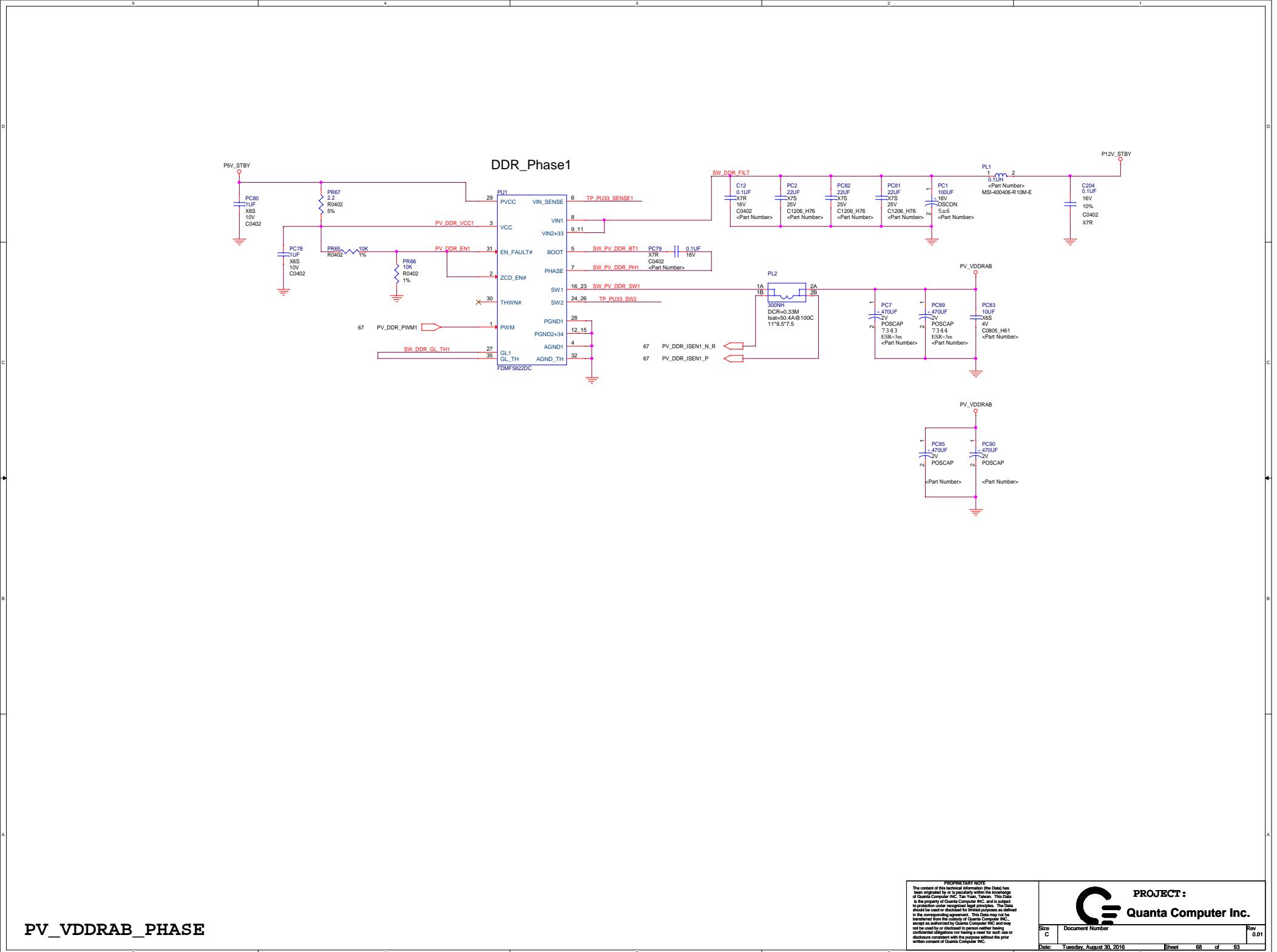


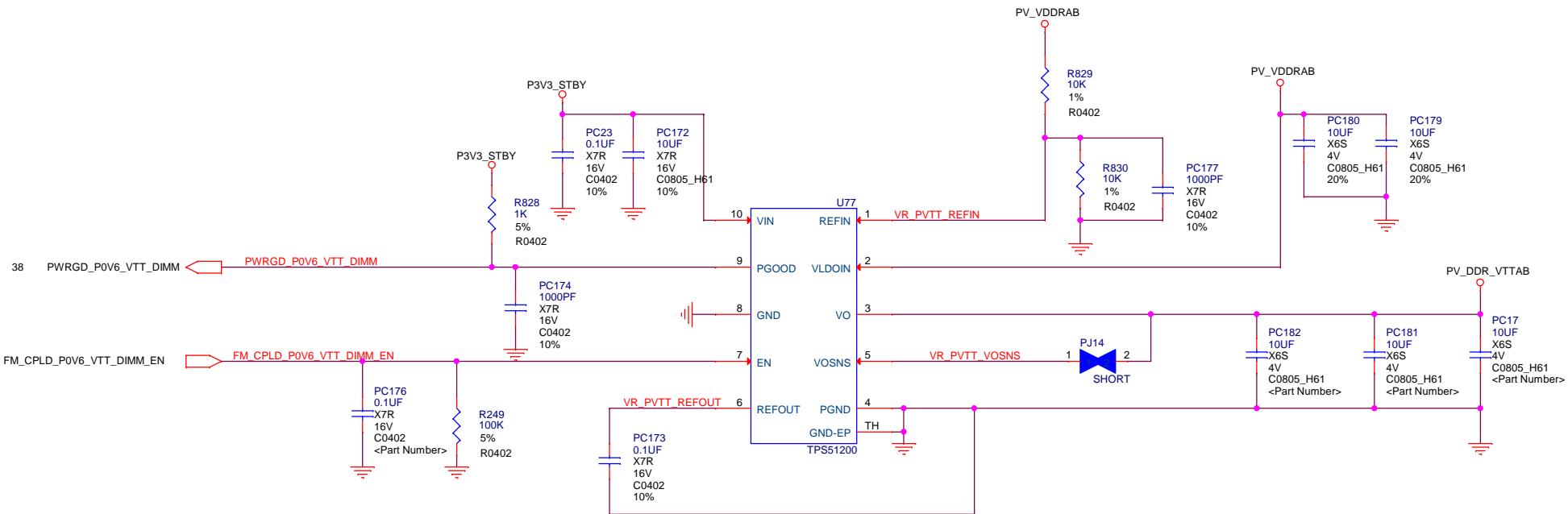


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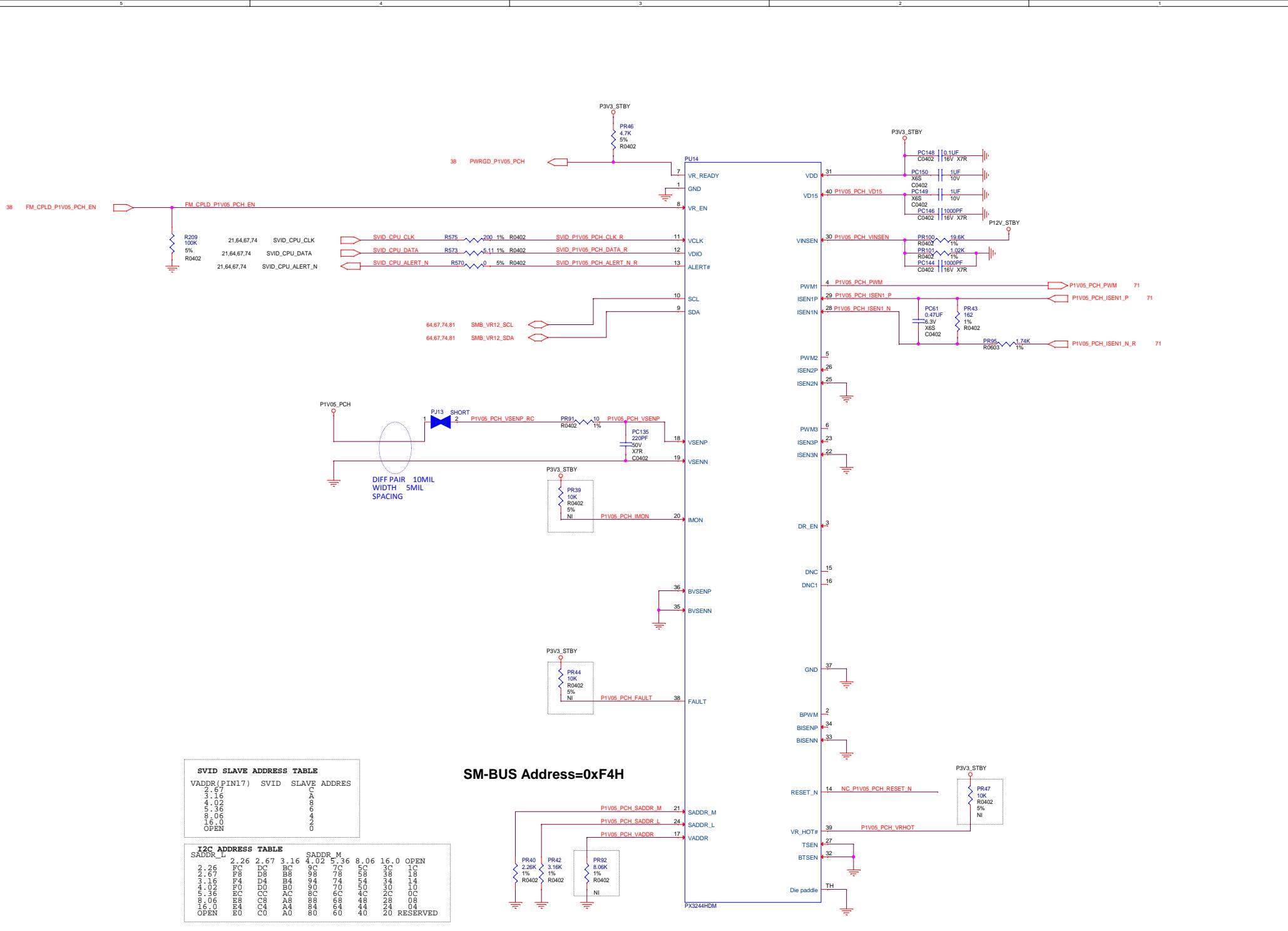


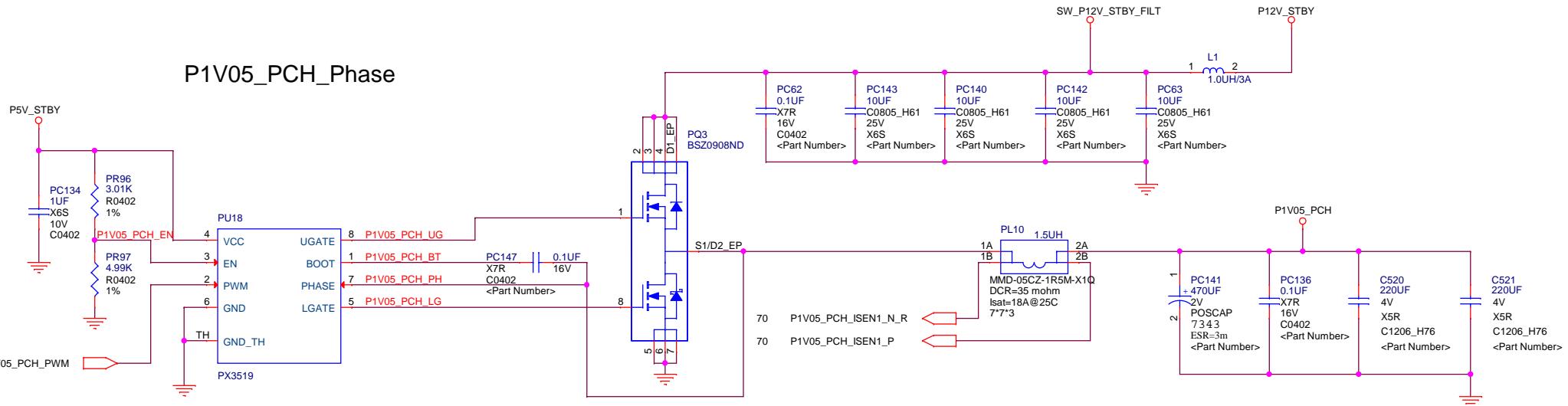


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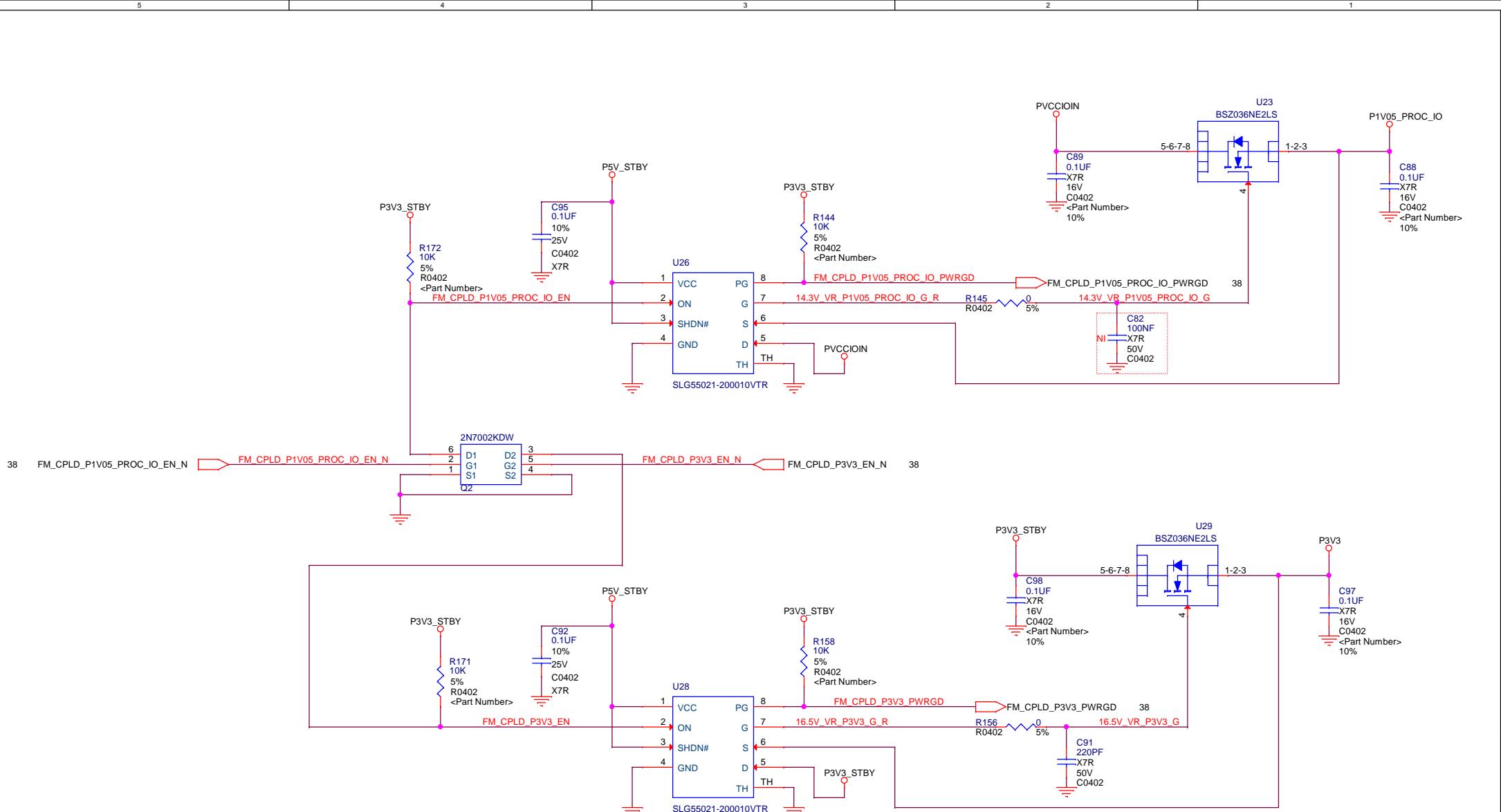
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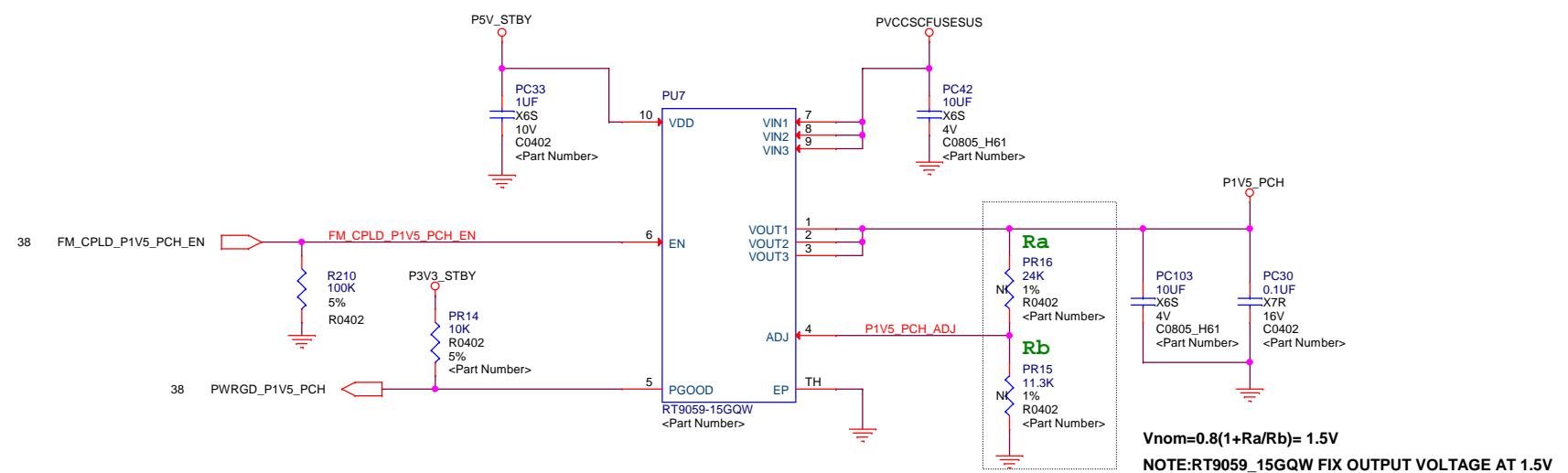




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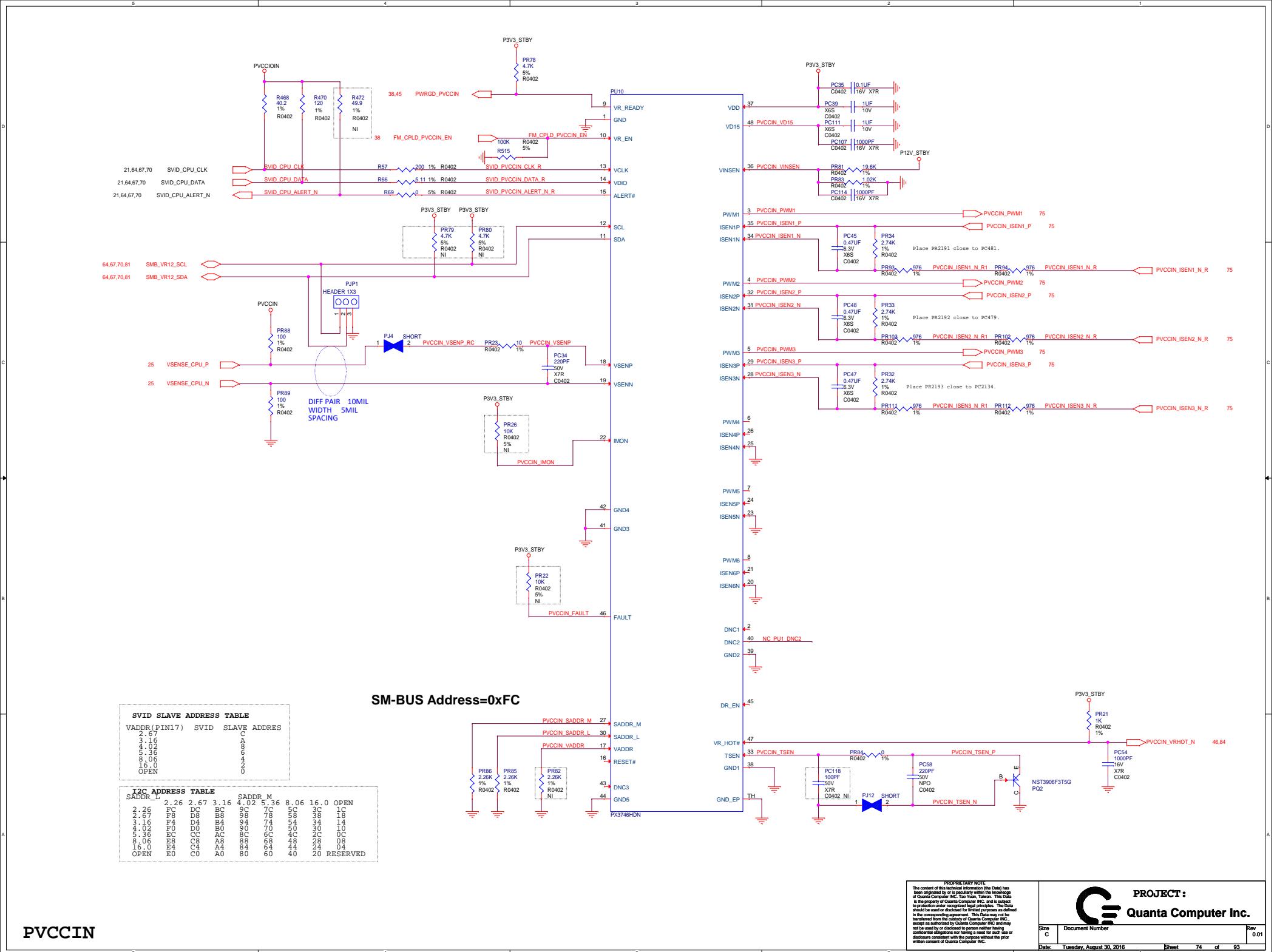
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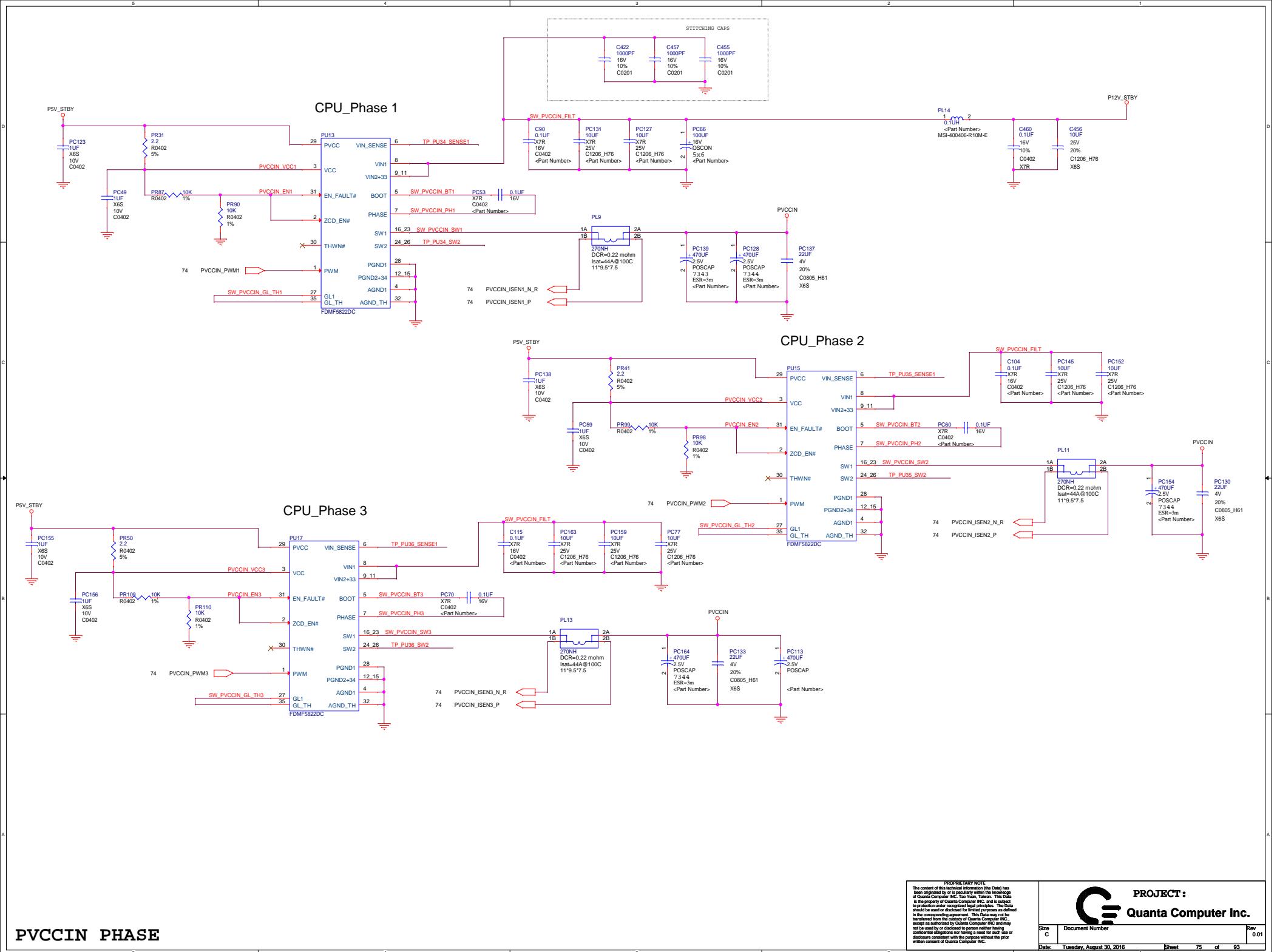


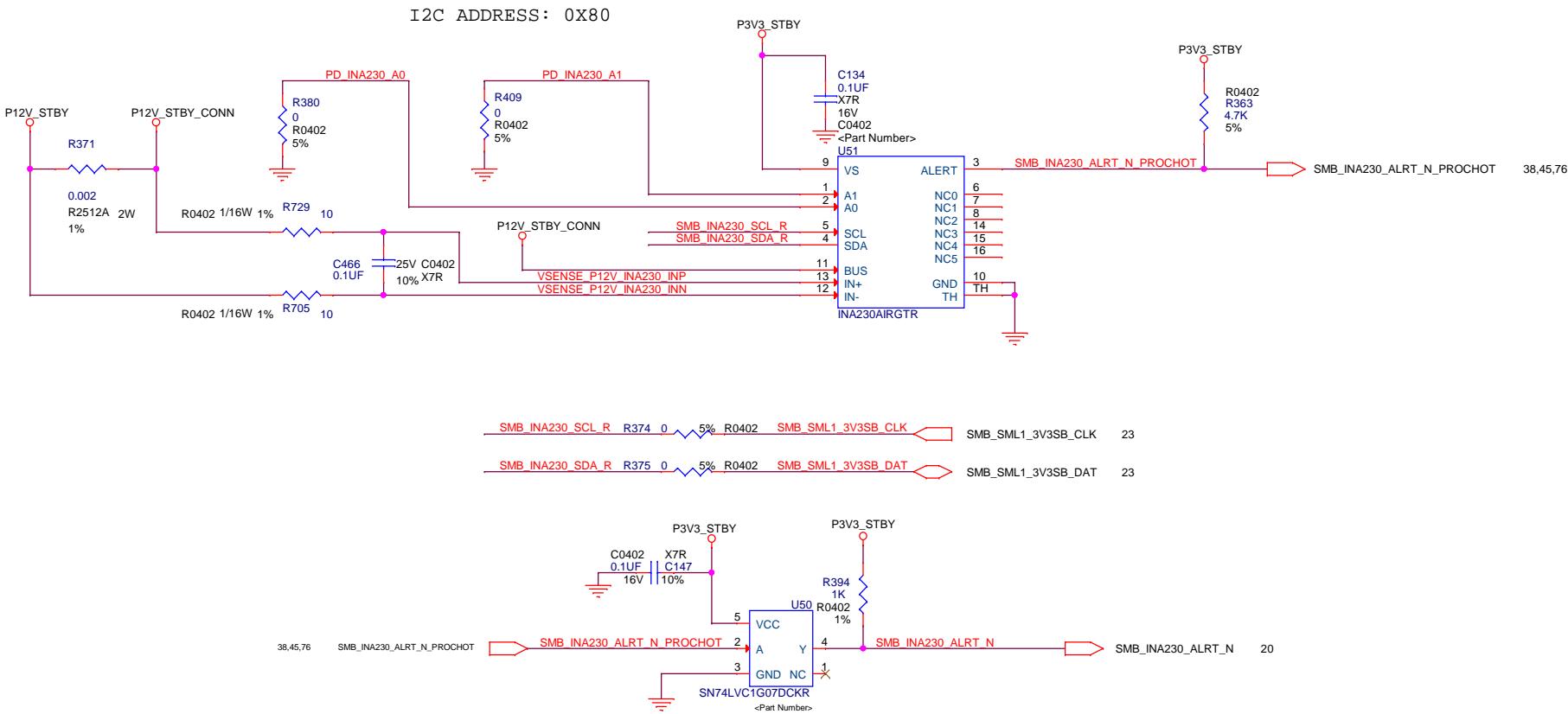
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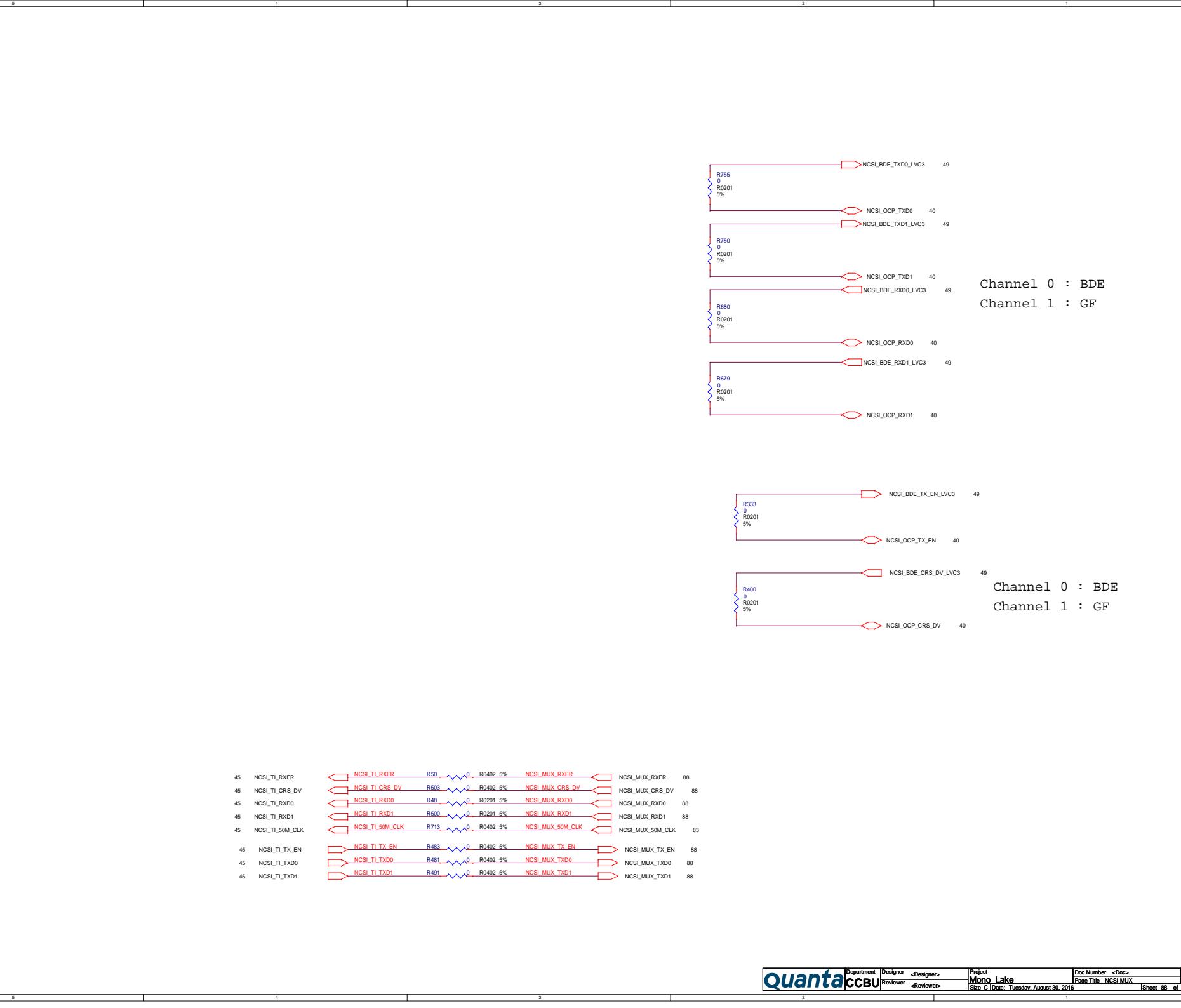
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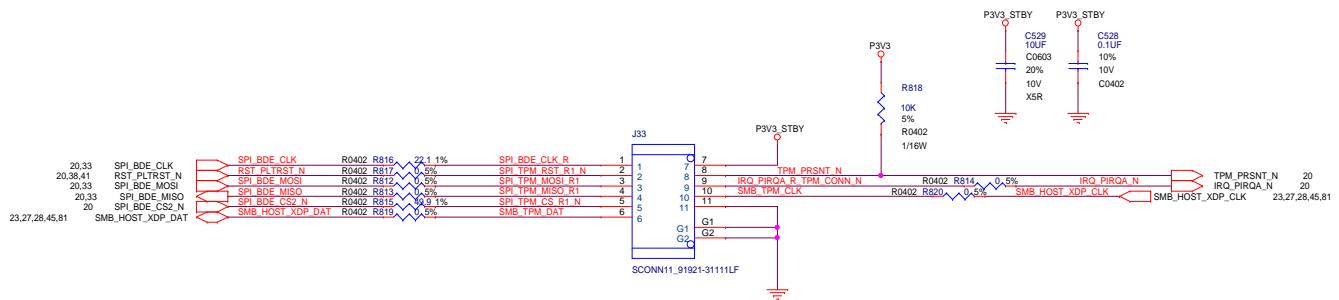


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