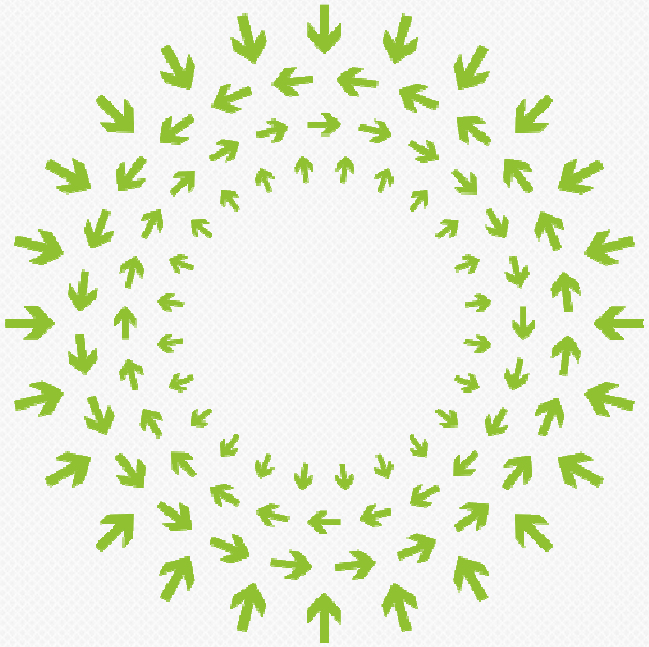

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Compute Engineering Workshop

March 9, 2015

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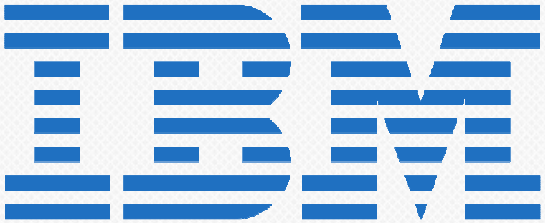
Barreleye

An OCP OpenPOWER Server

Norm James
IBM
Lead Engineer for OpenPOWER Enablement

Thanks to the following contributors:



Objective:

To design and build a totally open server

All open source firmware components:

- BMC
- BIOS
- Miscellaneous programmable parts

All hardware mechanical and board IP:

- Layouts
- Constraints
- Stackup
- Circuits
- Programmable parts code

POWER8 Processor

Cores

- 12 cores / 8 threads per core
- TDP: 130W and 190W
- 8 dispatch, 10 issue, 16 exec pipe
- 2X internal data flows/queues
- Enhanced prefetching
- 64K data cache, 32K instruction cache

Accelerators

- Crypto & memory expansion
- Transactional Memory

Caches

- 512 KB SRAM L2 / core
- 96 MB eDRAM shared L3

Energy Management

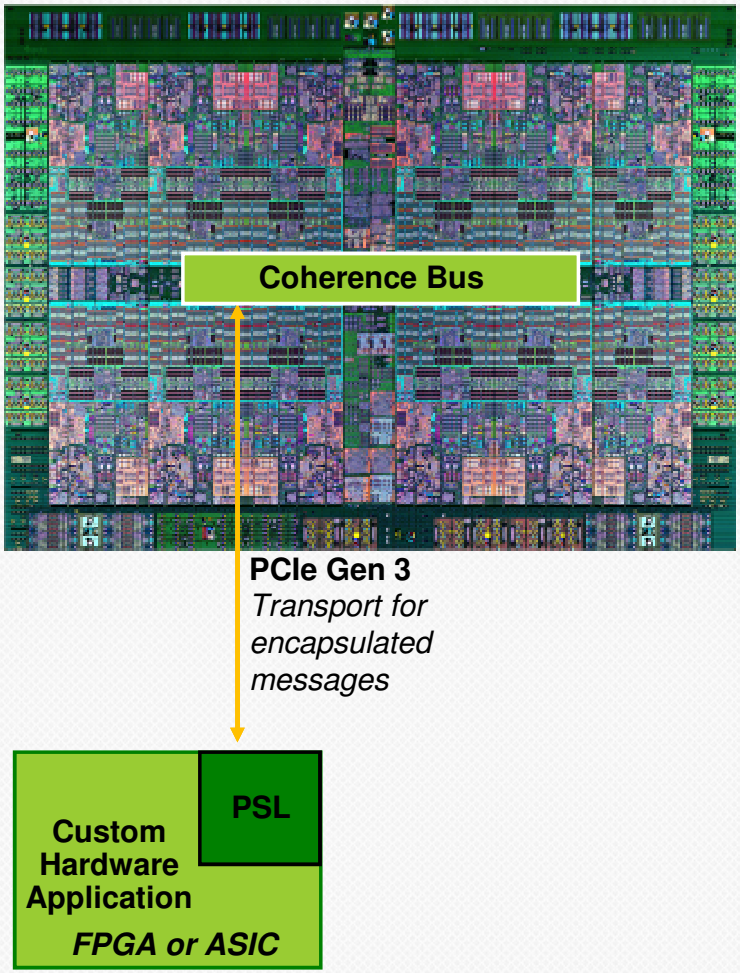
- On-chip Power Management Micro-controller
- Critical Path Monitors

Memory Subsystem

- Memory buffers with 128MB Cache
- ~70ns latency to memory
- 4 channels of DDR3 or DDR4
- 1 or 2 DIMMs/channel

Technology

•22nm SOI, eDRAM, 15 ML 650mm2



Bus Interfaces

•Durable memory attach interface (DMI)

•Up to 115 GB/s sustained memory bandwidth (9.6Gbps)

•Integrated PCIe Gen3

•SMP Interconnect for up to 4 sockets

•Up to 40 GB/s SMP bandwidth (6.4Gbps)

Coherent Accelerator Processor Interface (CAPI)

Virtual Addressing

- Accelerator can work with same memory addresses that the processors use
- Pointers de-referenced same as the host application
- Removes OS & device driver overhead

Hardware Managed Cache Coherence

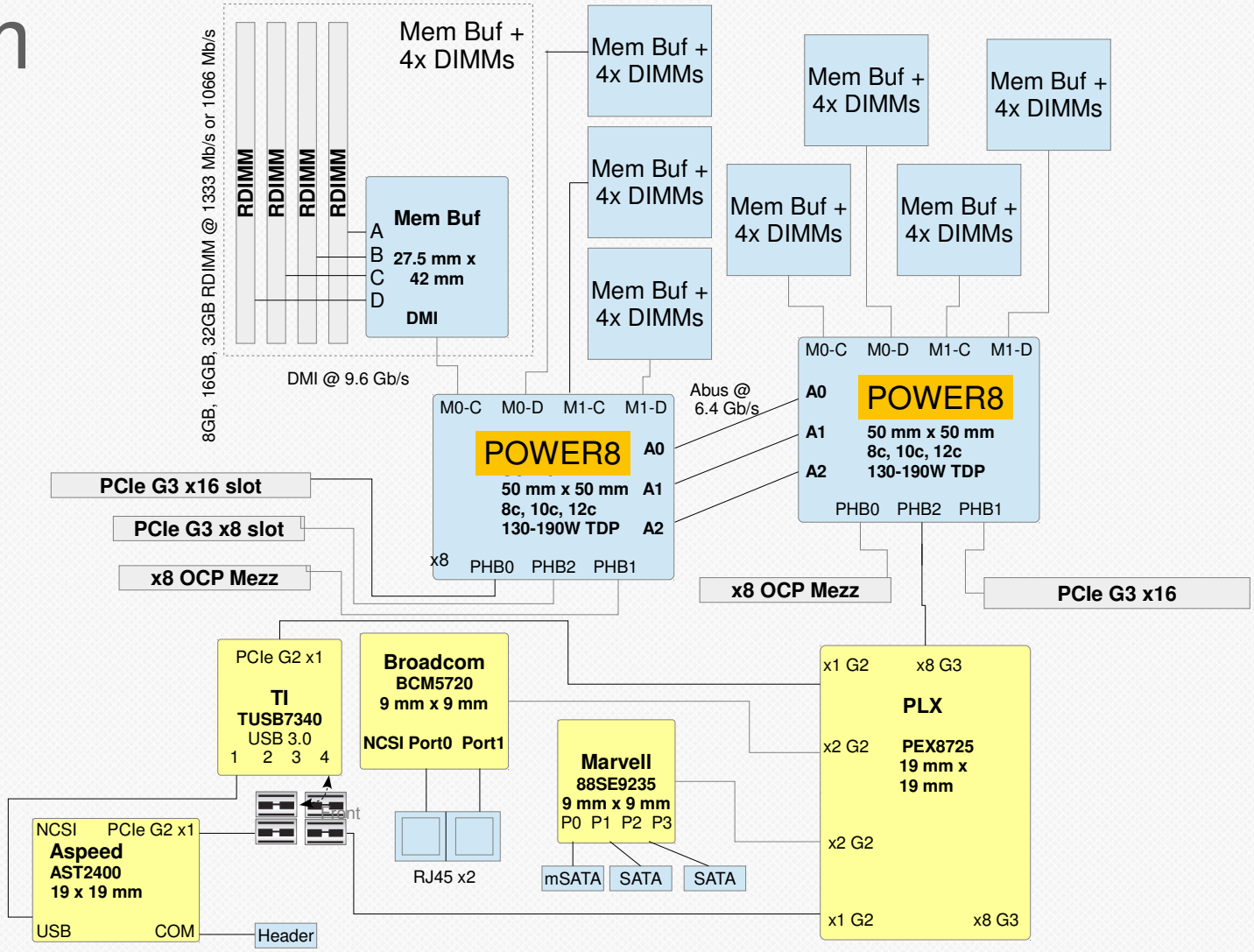
- Enables the accelerator to participate in "Locks" as a normal thread
- Lowers Latency over IO communication model

Processor Service Layer (PSL)

- Present robust, durable interfaces to applications
- Offload complexity / content from CAPP

Block Diagram

- 2 POWER8 CPU's
- 32 DDR3 DIMMs
  - 230GB/s Total Memory BW
- PCIe
  - 1 x16 FLFH (GPU)
  - 1 x16 HLHH
  - 1 x8 HLHH
  - 2 x8 OCP Mezz
- Storage
  - 15x 2.5" HDD/SDD
  - Hot swappable

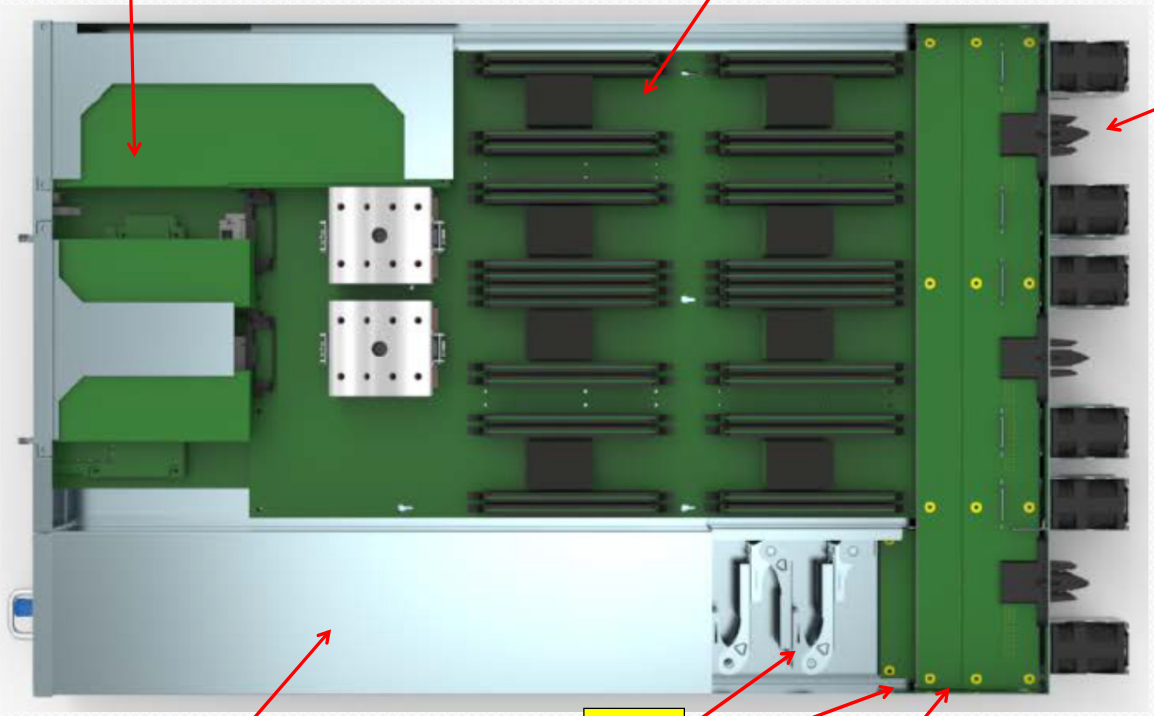


Main Board:
- 2x POWER8 8-12c; up to 3.857GHz
- 8x Memory Buffers
- 32x DDR3 DIMMs

I/O Board and PCIe Area

Hot Plug Fan Module (4056 x6)

12V Bus Bar clips 3x

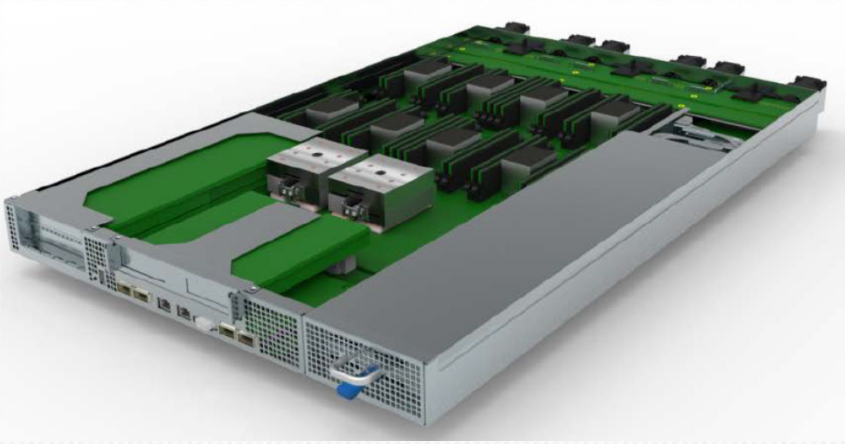


Hot Plug 15x 2.5" HDD (HDD Tray)

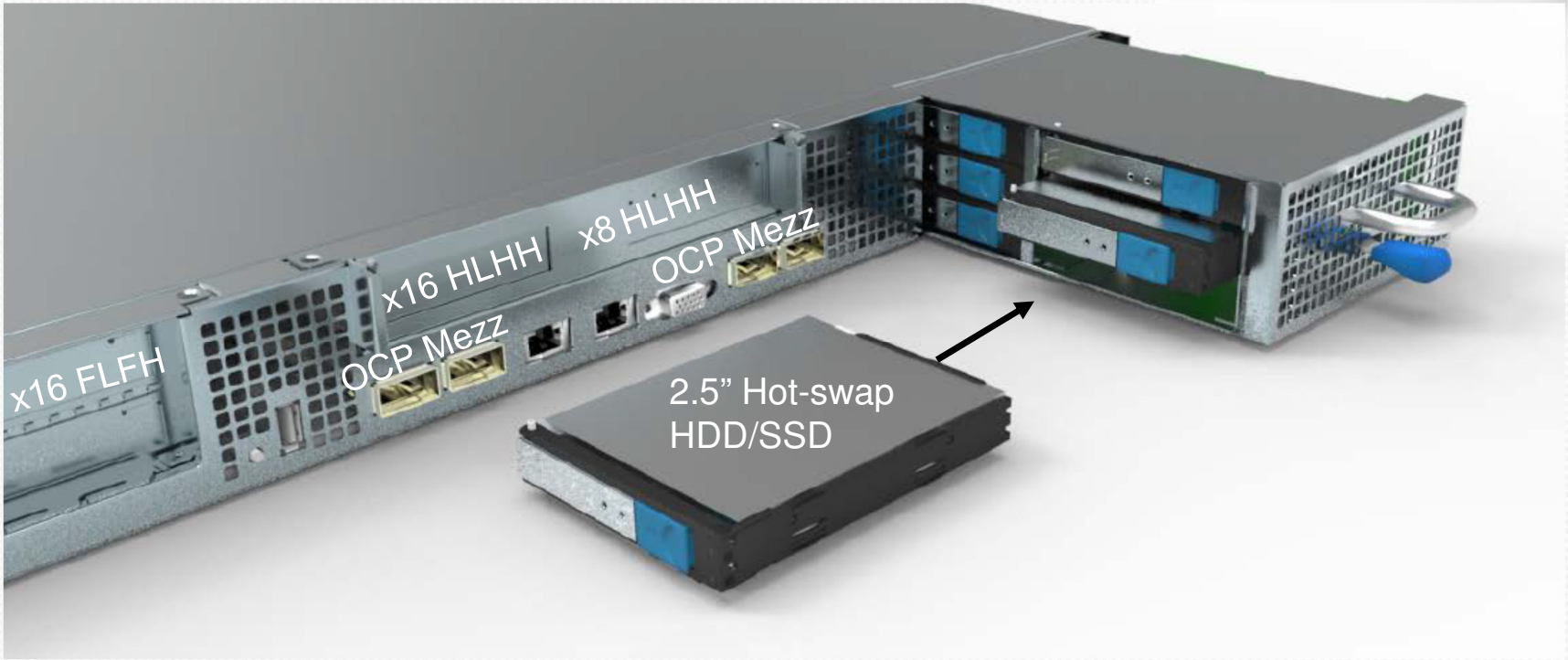
CMA

Expander Board

Power Distribution Board

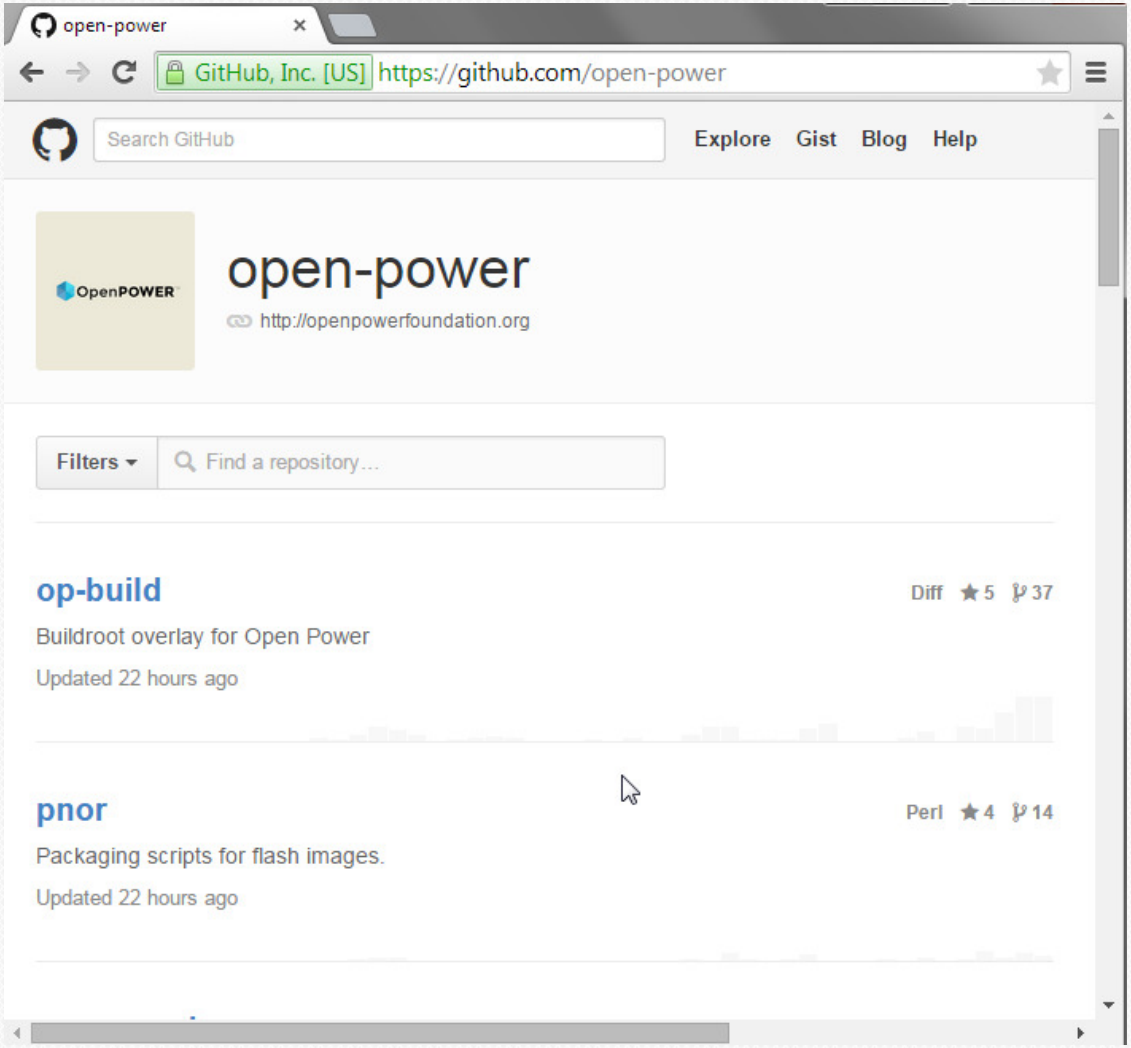


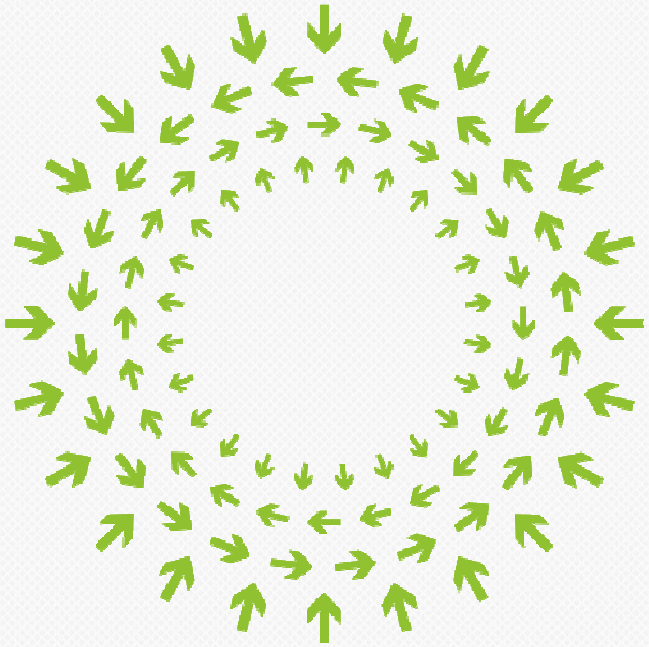
15x HDD/SSD
drawer


x16 FLFH
x16 HLHH
x8 HLHH
OCP Mezz
OCP Mezz
2.5” Hot-swap
HDD/SSD

POWER-BIOS

- Open-sourced at github
- POWER-BIOS is made up of 3 components
  - Hostboot – initializes chip and prepares cores for OS
  - OPAL – Linux based bootloader; scans PCIe busses; presents boot menu
  - OCC – Power management; power capping; thermal monitoring





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