## PCB Design (IL, RL, NEXT and FEXT)

Board design should follow the criteria from chip vendor to achieve proper operation of the high-speed signals. This table list below, refer to PAM4 as a reference. For different interface supported, it is good to consult with chip vendor.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Parameter | Min. | Typ. | Max. | Notes |
| Impedance | 81 ohm | 90 ohm | 99 ohm |  |
| SDD11(22) | - | - | -15 dB | DC~(BitRate/3), Note.1 |
| SDC11(22) | - | - | -25 dB | DC~(BitRate/3) |
| SDD21 |  |  | -30 dB | Note.2 |
| Intra-skew | - | - | 0.5 ps |  |
| Inter-skew | Note.3 | | | |
| NEXT | - | - | -55 dB | TX->RX, RX->TX |
| FEXT | - | - | -45 dB | RX->RX, TX->TX |

Note 1: PAM4 BitRate = 56Gbps, the DC~18.6GHz

Note 2: To control the total channel loss (included die+package of chip) under -30dB at 14.025GHz.

Assume the die+package loss is under -8dB at 14.025GHz. ODM can optimize the channel trace

length and the material to meet loss criteria.

Note 3: It should compliant with related protocol requirements.

## Layout Guideline

This layout recommendations are for achieving proper operation of the high-speed signals. Good to compare this guideline with chip vendor’s rule to have better signal integrity.

### Trace Impedance

In the UBB board, the TX and RX links have target impedance of 90 ohm+/-10%

### Stackup Design And Single-Ended / Differential Pair Geometry

Following PCB stackup should be followed for UBB design. Each vendor needs to fine tune the width/spacing design based on material target and impedance control table below. The loss per inch of PCB material should meet loss criteria -0.58dB/-0.88dB and -0.96dB at 8GHz/14GHz and 16 GHz.

* Loss comparison with different PP/Core design based on the same diff-pair (target to 90ohm impedance) with ultra-low-loss material

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Case | Core/PP  (mil) | Board thickness (mil) | Width/Spacing  (mil) | Loss/inch  @16GHz (dB) | Comparison  Vs. Case 1 | Note |
| 1 | 3.0/6.0 | 129.4 | 4.3/6.7 | -0.979 | NA |  |
| 2 | 4.0/5.0 | 128.4 | 4.8/6.2 | -0.914 | 6.64% |  |
| 3 | 4.0/7.0 | 144.4 | 5.1/5.9 | -0.89 | 9.09% | \*Note1 |

\*Note1: To be confirmed with vendor if Backdrill tech. implemented into this board thickness.

Table 1: 22L Stackup Design

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Layer | Plane Description | | | Copper (OZ) | | Thickness (mil) |
|  |  | Solder mask |  | | 0.5 | | |
| L1 | Top | Signal/PWR | 0.5oz + plating | | 1.9 | | |
|  |  | PrePreg |  | | 2.6 | | |
| L2 | GND1 | Ground | 1.0 | | 1.2 | | |
|  |  | Core (1/1) |  | | 4 | | |
| L3 | IN1 | Signal/PWR | 1.0 | | 1.2 | | |
|  |  | PrePreg |  | | 5 | | |
| L4 | GND2 | Ground | 1.0 | | 1.2 | | |
|  |  | Core (1/1) |  | | 4 | | |
| L5 | IN2 | Signal/PWR | 1.0 | | 1.2 | | |
|  |  | PrePreg |  | | 5 | | |
| L6 | GND3 | Ground | 1.0 | | 1.2 | | |
|  |  | Core (1/1) |  | | 4 | | |
| L7 | IN3 | Signal/PWR | 1.0 | | 1.2 | | |
|  |  | PrePreg |  | | 5 | | |
| L8 | GND4 | Ground | 1.0 | | 1.2 | | |
|  |  | Core (1/1) |  | | 4 | | |
| L9 | IN4 | Signal/PWR | 1.0 | | 1.2 | | |
|  |  | PrePreg |  | | 5 | | |
| L10 | GND5 | Ground | 1.0 | | 1.2 | | |
|  |  | Core (1/2) |  | | 4 | | |
| L11 | VCC1 | Power | 2.0 | | 2.4 | | |
|  |  | PrePreg |  | | 12 | | |
| L12 | VCC2 | Power | 2.0 | | 2.4 | | |
|  |  | Core (1/2) |  | | 4 | | |
| L13 | GND6 | Ground | 1.0 | | 1.2 | | |
|  |  | PrePreg |  | | 5 | | |
| L14 | IN5 | Signal/PWR | 1.0 | | 1.2 | | |
|  |  | Core (1/1) |  | | 4 | | |
| L15 | GND7 | Ground | 1.0 | | 1.2 | | |
|  |  | PrePreg |  | | 5 | | |
| L16 | IN6 | Signal/PWR | 1.0 | | 1.2 | | |
|  |  | Core (1/1) |  | | 4 | | |
| L17 | GND8 | Ground | 1.0 | | 1.2 | | |
|  |  | PrePreg |  | | 5 | | |
| L18 | IN7 | Signal/PWR | 1.0 | | 1.2 | | |
|  |  | Core (1/1) |  | | 4 | | |
| L19 | GND9 | Ground | 1.0 | | 1.2 | | |
|  |  | PrePreg |  | | 5 | | |
| L20 | IN8 | Signal/PWR | 1.0 | | 1.2 | | |
|  |  | Core (1/1) |  | | 4 | | |
| L21 | GND10 | Ground | 1.0 | | 1.2 | | |
|  |  | PrePreg |  | | 2.6 | | |
| L22 | BOT | Signal/PWR | 0.5oz + plating | | 1.9 | | |
|  |  | Solder Mask |  | | 0.5 | | |
|  |  | Total  Table 2: The Single-Ended and Diff-Pair Geometry | 128.4 mil (with +/- 10% tolerance) | | | | |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Trace Width  (mil) | Air Gap Spacing (mil) | | | Impedance Type | Layer | | Impedance Target  (ohm) | | | Tolerance  (+/- %) |
| 6.0 | |  | Single | | | 1,22 | | 45 | 10% | |
| 5.3 | |  | Single | | | 1,22 | | 50 | 10% | |
| 5.3 | | 5.6 | Differential | | | 1,22 | | 85 | 10% | |
| 4.8 | | 6.1 | Differential | | | 1,22 | | 90 | 10% | |
| 5.8 | |  | Single | | | 3,5,7,9,14,16,18,20 | | 45 | 10% | |
| 5.0 | |  | Single | | | 3,5,7,9,14,16,18,20 | | 50 | 10% | |
| 5.7 | | 5.2 | Differential | | | 3,5,7,9,14,16,18,20 | | 85 | 10% | |
| 5.0 | | 5.8 | Differential | | | 3,5,7,9,14,16,18,20 | | 90 | 10% | |

### Fiber Weave Effect

To avoid P/N pair skew difference in the received differential signals, the following guidelines to minimize the weave effect:

* Choose spread glass material such as the weave types: 1035, 1067, 1078, and 1086.
* Use two-ply spread glass for each layer instead of one-ply.
* Other options:
* Use the Zig-Zag routing to route the signals in 10 to 15 degrees angles.
* Rotate the board design by 10 to 15 degrees with respect to the panel. Should be confirmed the design size versus panel size effect.

### Routing Layer

Differential signals must be routed in stripline and two solid GND reference planes both near-end and far-end reference.

### Trace Clearances & Length Matching Requirement (H = the thickness between signal to the nearest reference plane)

* Pair to pair spacing on breakout region: TBD
* Pair to pair spacing of the same group on open field: 6H
* TX/RX group to group spacing: 6H
* Intra-pair length matching of DP/DN pair: 1 mil
* Lane to Lane length mismatch of TX or RX group: < 3 inch

### Others Requirement:

* Must to have Backdrill technology to minimize via stub length
* The non-function pads of all signals and ground must be removed

## Fanout Design Recommendation

* Break-out and anti-pad for different pair north routing recommendation

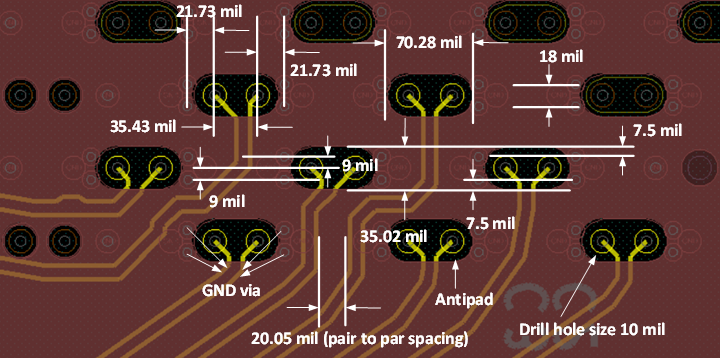


Figure 1: Fanout routing of via-in-pads on Top layer

* The upper layer routing (Top/L3/L5/L7/L9) can refer to oblong anti-pad from Top to Bottom layer as Fig 1 to get better impedance controlled.

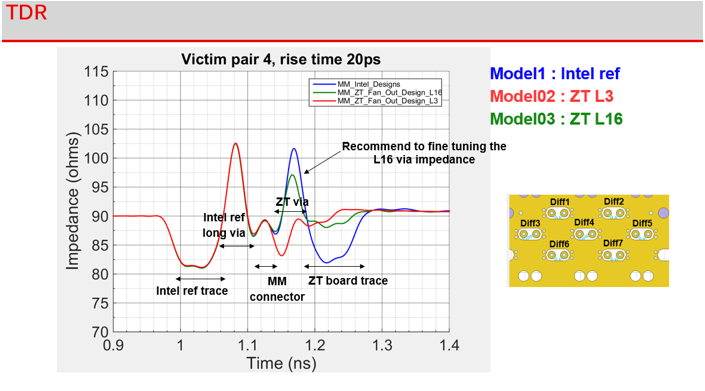


Figure 2: TDR Result of L3/L16 routing layer

* From figure 2, the TDR result of L16 is 97.5 ohm if keep the same anti-pad design with upper layer routing. Recommend making anti-pad modification to get better impedance controlled as Fig 3, the impedance will be 92.5 ohm as Fig 4.

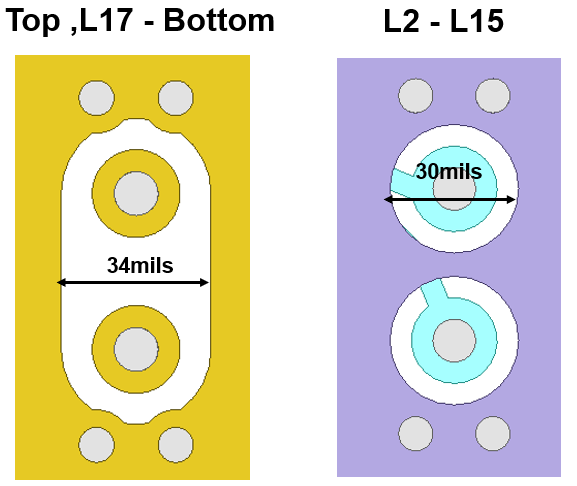


Figure 3: Recommendation of L16 routing layer anti-pad

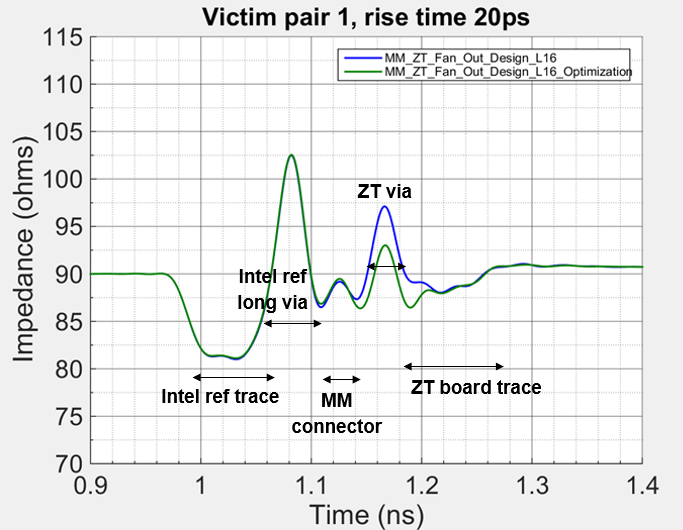


Figure 4: TDR result of anti-pad optimization on L16 routing

## 2.1 Test Procedure & Environment Setting Recommendation

* UBB design is tested using 4-port Vector Network Analyzer (VNA) up to 50GHz.
* To get total channel loss from OAM1 to OAM2 by using Molex test fixture.

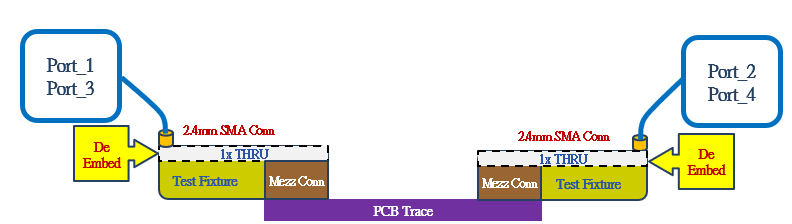


Figure 5: UBB with test fixture topology

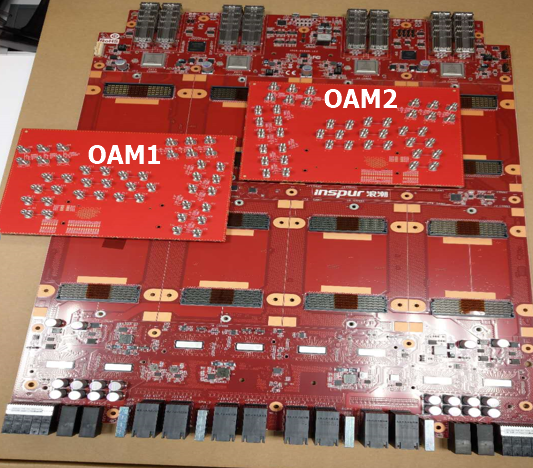
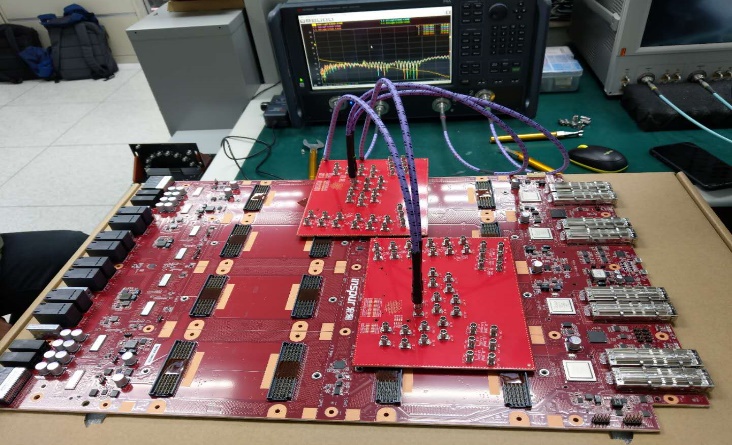
 

Figure 6: UBB Measurement Setting

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Figure 7: Channel IL of UBB board (with test fixture)

* Insertion Loss Measurement Data of 2X Thru Design

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Figure 8: Top View

Figure 9: Bottom View

Figure 10: 2X Thru



**2X\_THRU**

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Figure 11: 2X Thru IL Measurement

* De-embedding the test fixture to get the IL of UBB board.

(Ps. This data is included 2 Mirror Mezz Connector)

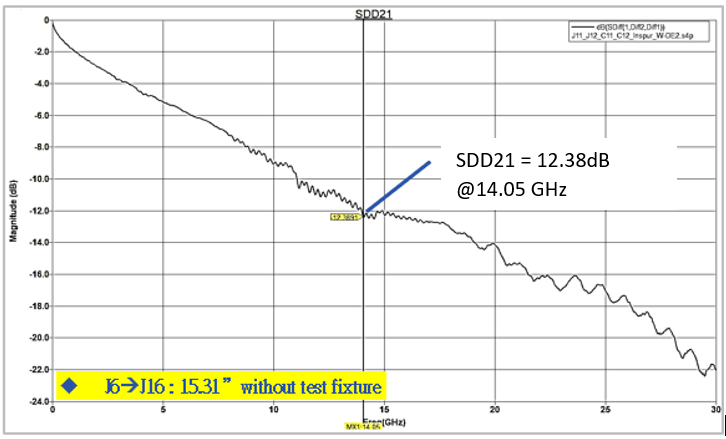


Figure 12: The IL result of UBB board with test fixture de-embedding