

OCP3 Thermal Test Fixture (TTF)

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PWA: WFTNX
PWB: GV51R
SCH: 41XPG

ADD

41XPG

Schematic

ADD

GV51R

PWB

1

2D BARCODE

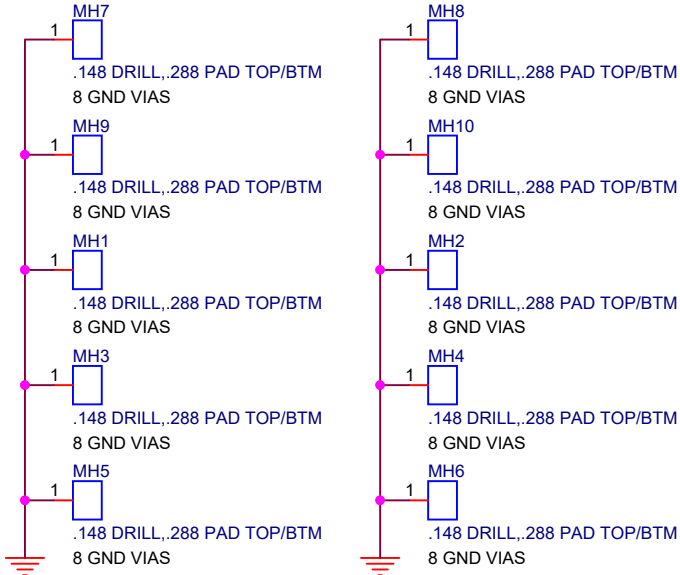
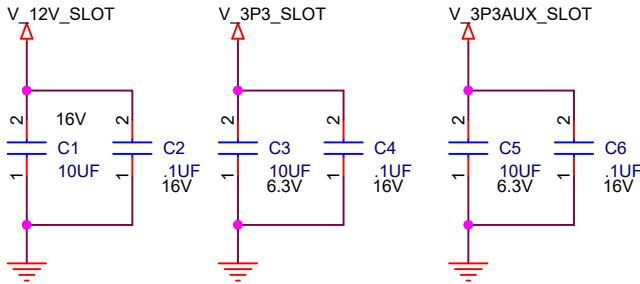
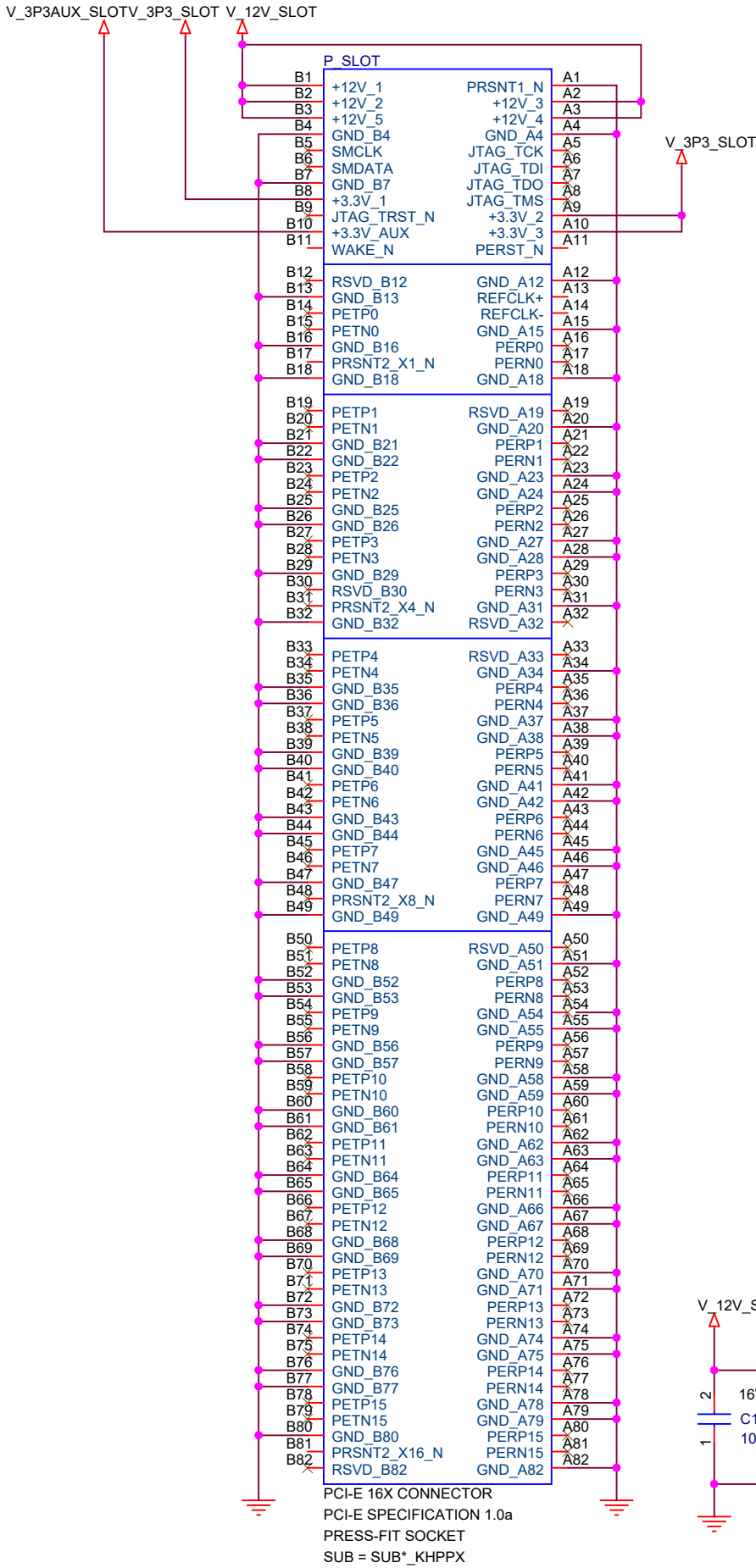
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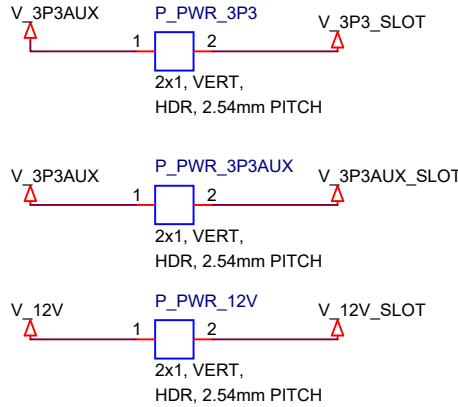
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		DWG NO.	41XPG	REV.	X00
		DATE	Wednesday, October 31, 2018	SHEET	1 of 8

Material: Meg6						Z50		Z85			Z100		
Z Type						Single Ended		Differential			Differential		
Included Technologies													
Target Z (ohms)						50		85			100		
Z tolerance (+/-)						10%		10%			10%		
Layer	Name	Cu Wt	Thickness	Tol	Er	Width	Z-Calc	Width	Space	Z-Calc	Width	Space	Z-Calc
SolderMask													
1	Top	1.5 oz	1.9			6.3	49.98	6.5	6	84.33	5	8	99.04
Prepreg													
2	GND	1 oz	1.3										
Core													
3	inner1	1 oz	1.3			8	48.21	7	5	84.22	5	6	99.8
Prepreg													
4	GD2	1 oz	1.3										
Core													
5	GD3	1 oz	1.3										
Prepreg													
6	inner2	1 oz	1.3			8	48.21	7	5	84.22	5	6	99.8
Core													
7	GD4	1 oz	1.3										
Prepreg													
8	Bottom	1.5 oz	1.9			6.3	49.98	6.5	6	84.33	5	8	99.04
SolderMask													
** Ignore Z requirements for layers where trace width does not exist.		mil	63.6	+/- 10%									

PCle Riser Slot

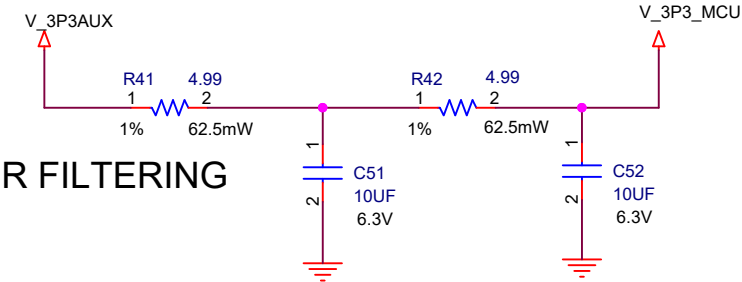


Connect jumpers to power PCIe slot

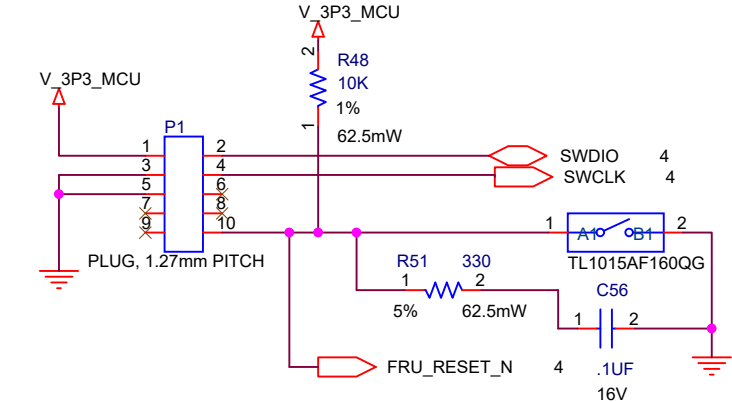


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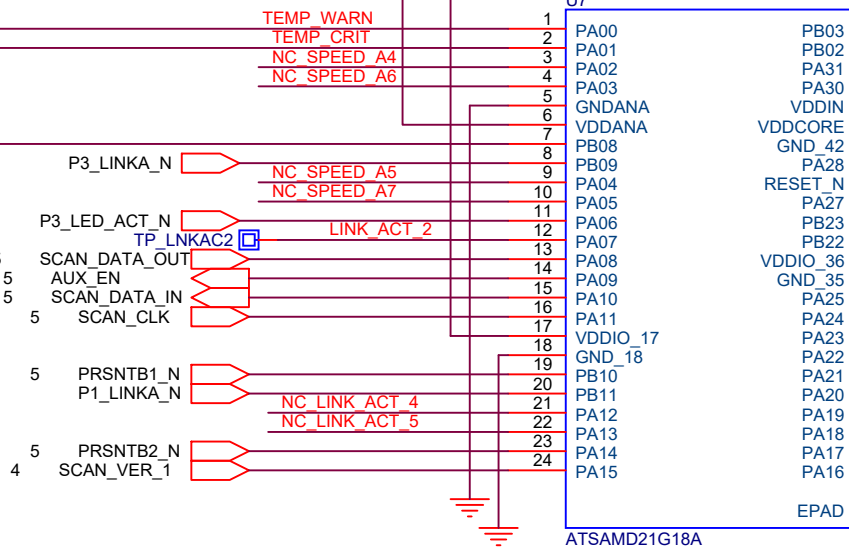
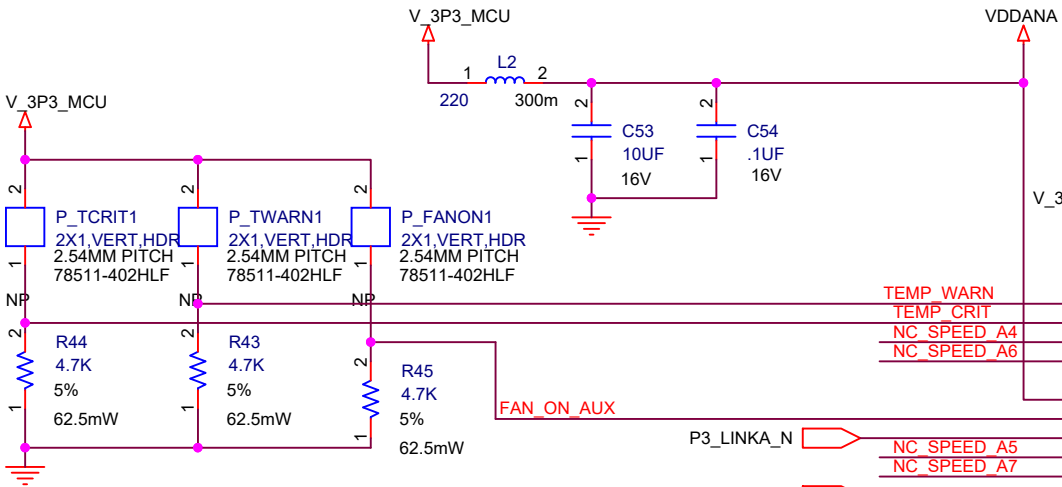
LOW PASS POWER FILTERING



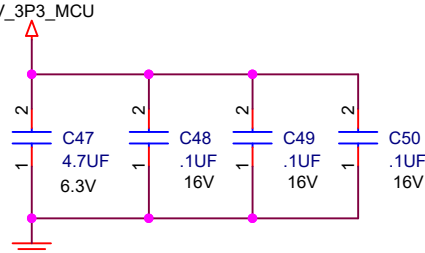
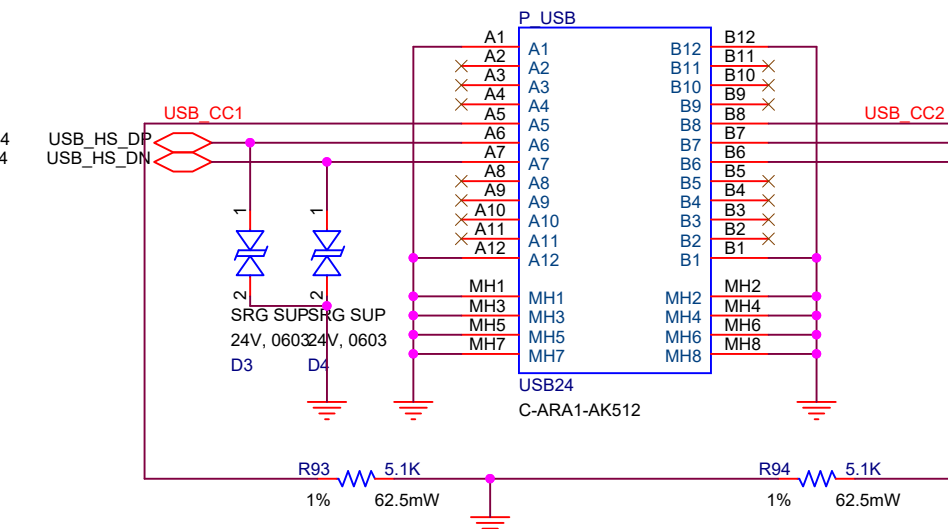
FRU



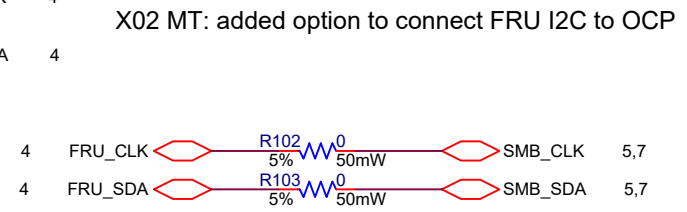
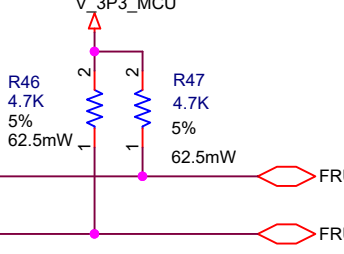
FRU PROGRAMMING HEADER



ROOM = FRU



V_3P3_MCU DECOUPLING



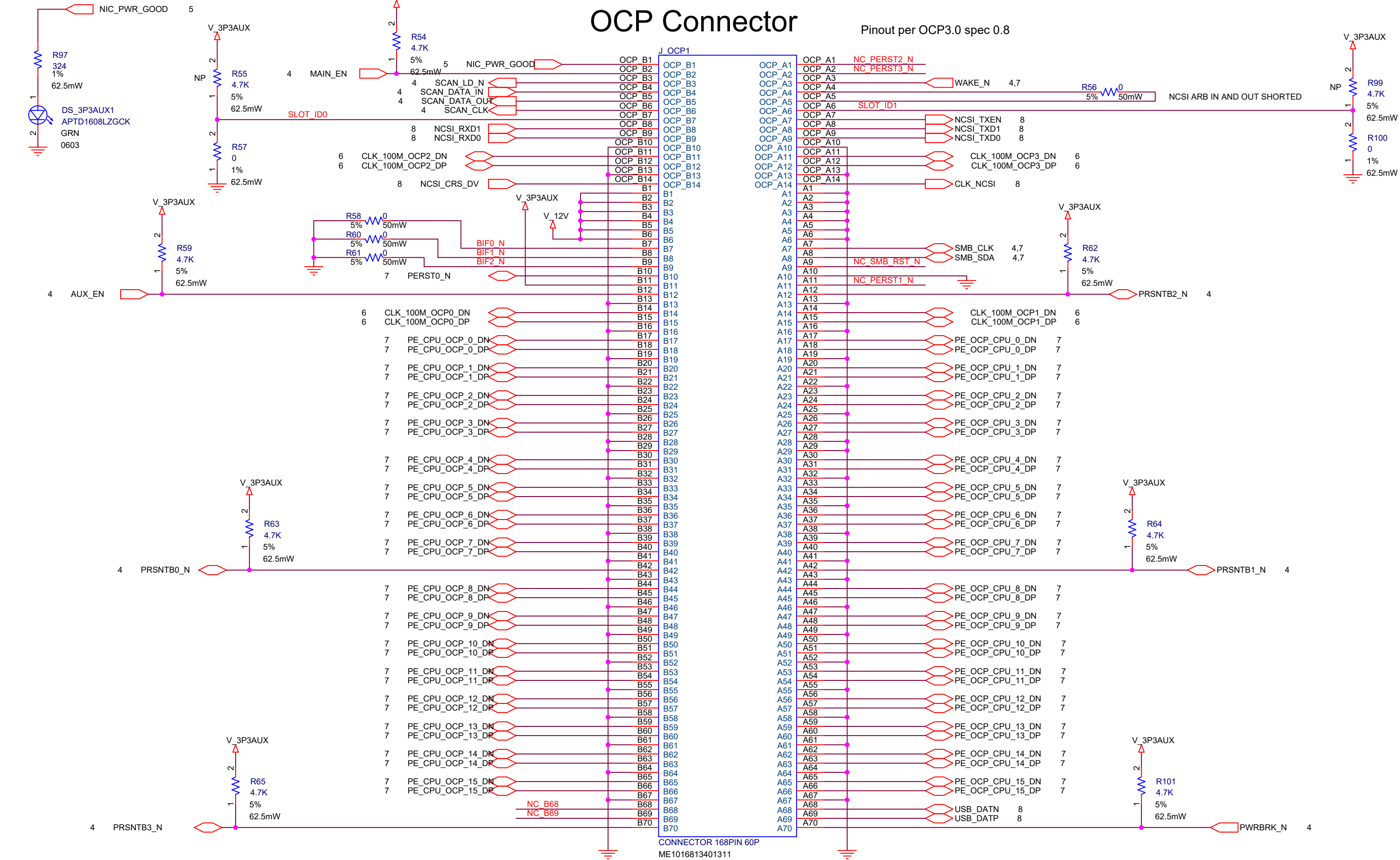
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X02 MT: added PWR_GOOD LED

X02 MT: updated pinout to spec 0.8. Added SLOT_ID1 and PWRBRK_N.

OCP Connector

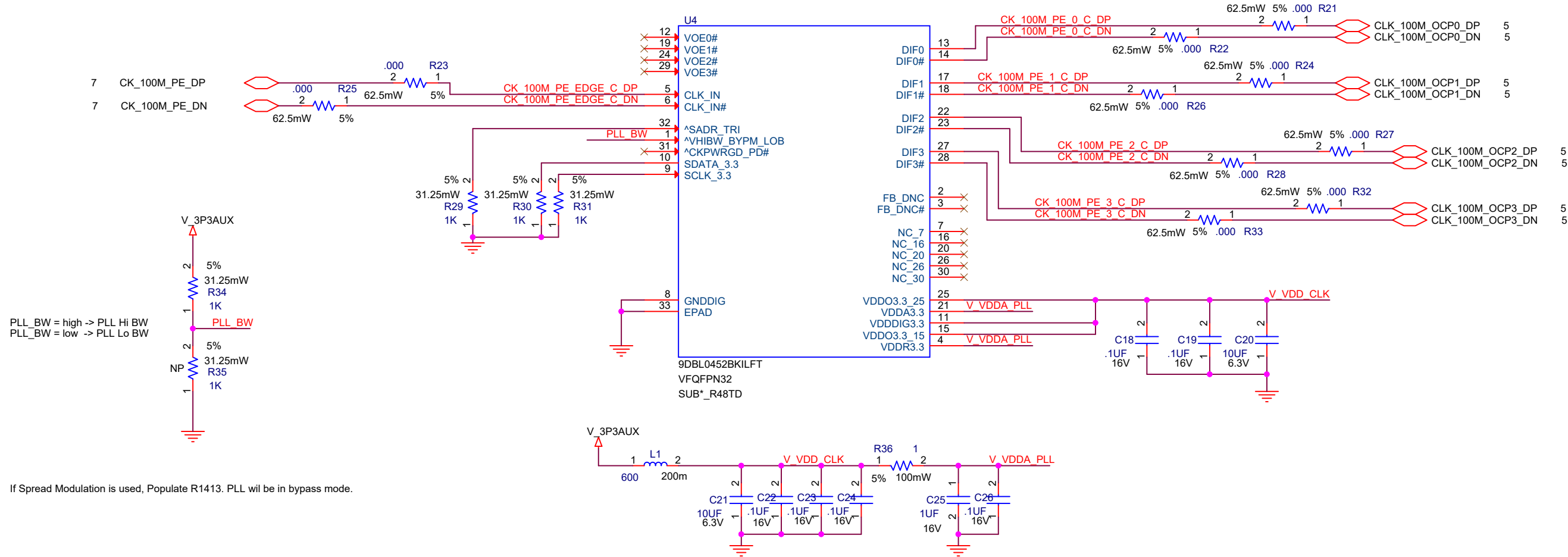
Pinout per OCP3.0 spec 0.8



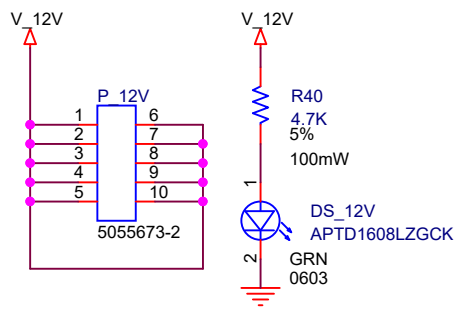
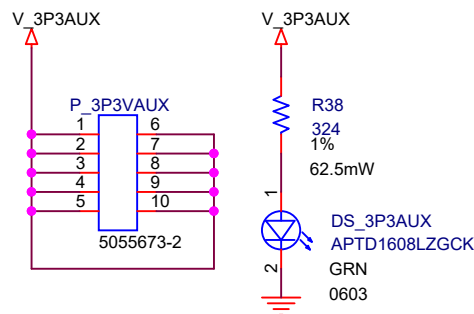
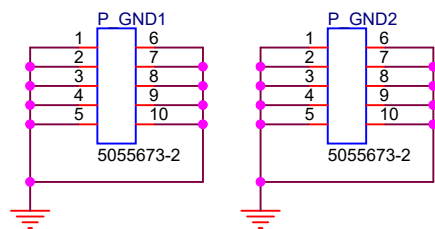
ROOM = OCPCONN

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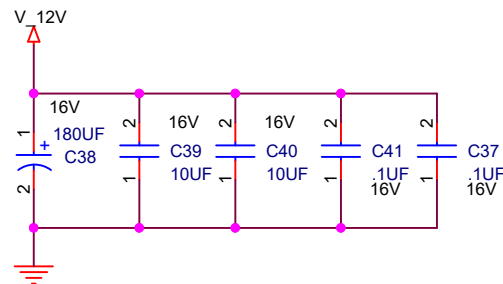
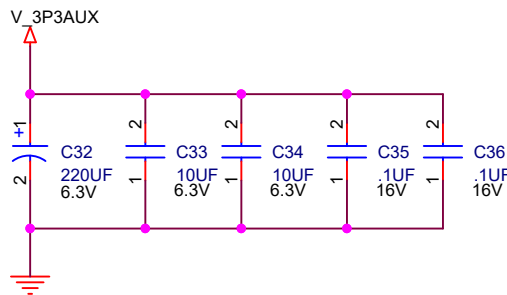
PCle Clk Buffer Mezz Conn A, B



Power Connectors



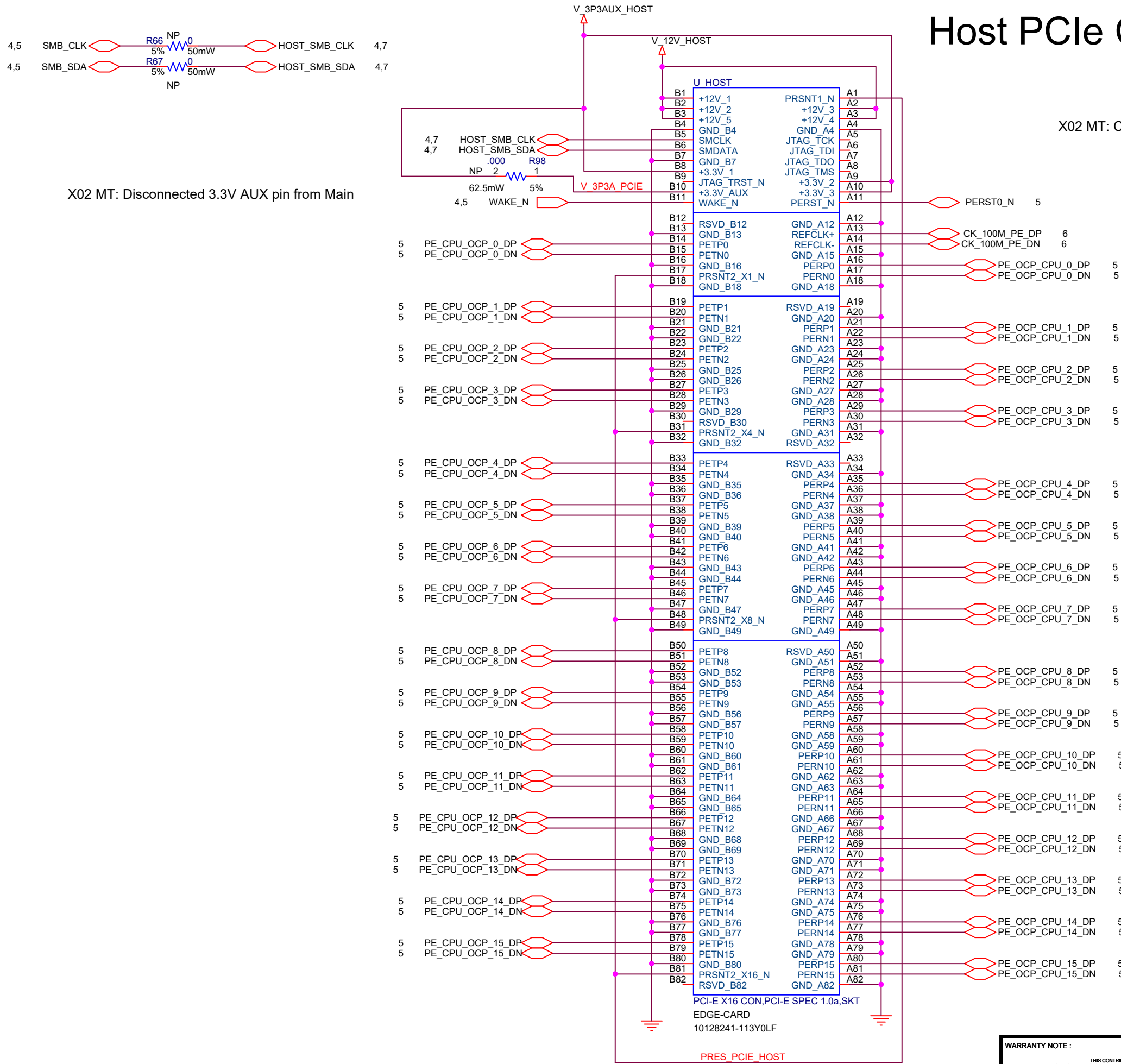
Decoupling Capacitors



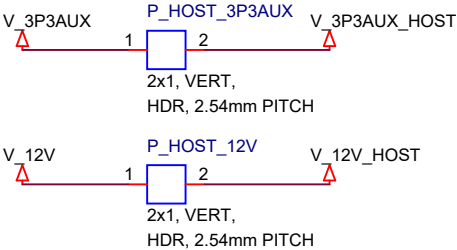
ECAD: Place close to P_TB*

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Host PCIe Conn



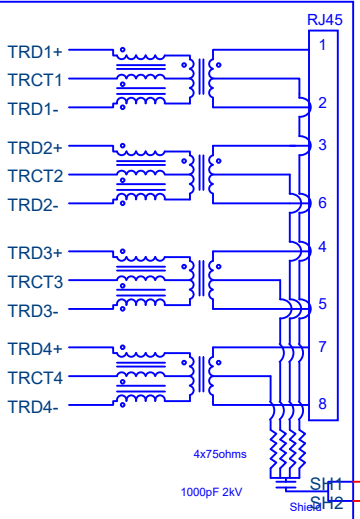
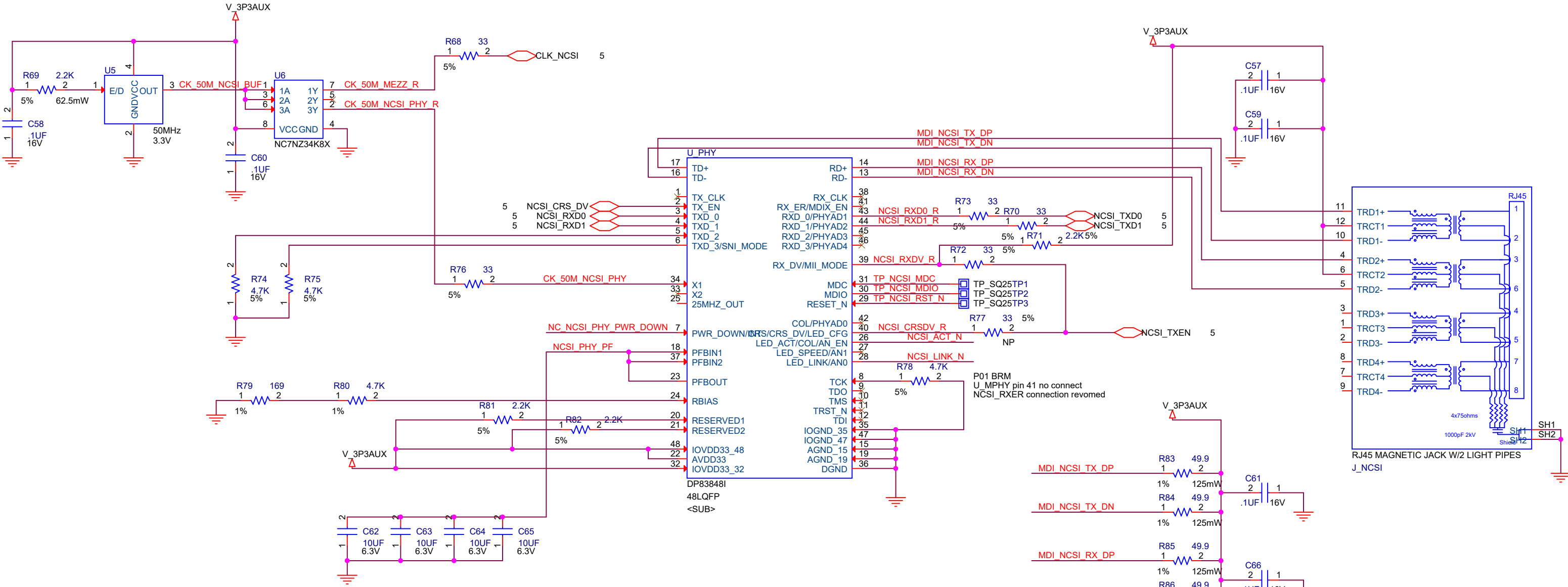
Connect jumpers to power card from Host



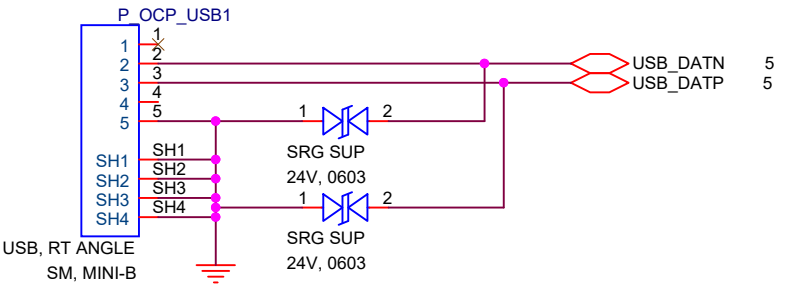
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NCSI Phy, RJMag and USB port

ROOM=CK_NCSI



ROOM=NCSI



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