CEI-112G-XSR-PAM4: NEED/USE CASES, CHALLENGES, STATUS, AND FUTURE

Valery Kugel

Sr. Distinguished Engineer, Silicon and System Technology

For OCP/ODSA February 28, 2020

DISCLAIMER

The views expressed in this talk are my own observations of technology trends and challenges, and they don't necessarily represent Juniper Networks' plans and directions.

AGENDA

- A NEED FOR XSR AND PROJECT START AT OIF

- DIFFERENCE BETWEEN PCB AND XSR SIGNALING MEDIA

- USE CASES

- BASIC REQUIREMENTS

- CHALLENGES, TIPS

- CURRENT STATUS & CONCLUSIONS

A NEED FOR XSR

NEED FOR 112G-XSR

- There is a constant request from Juniper customers to improve system bandwidth, power, and cost. Higher level integration promises to address the request;

- In the integration approach we see a tendency to design and place multiple homogeneous or heterogeneous chips/components on a common organic substrate. For networking applications dimensions of such substrates can be very large - >80mmX80mm, which results in up to ~50mm communication channels;

- Electrical channels supported by existing 100G OIF proposals are either too restrictive (CEI-112G-MCM-CNRZ - 25mm channel and requires clock forwarding) or results in too power hungry and large implementation (CEI-112G-VSR-PAM4 - ~120mm on-PCB signaling).

CEI-112G-XSR-PAM4 project aims to provide a framework for low power, high bandwidth electrical signaling for all types of applications requiring signaling on common organic substrate of a package.

organic substrate
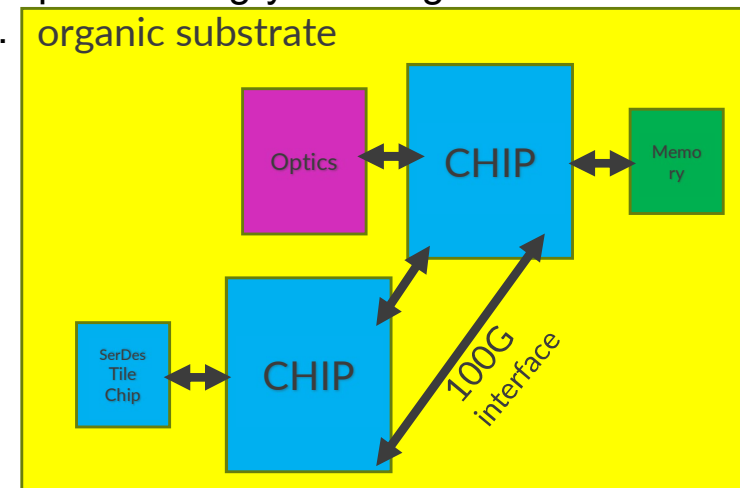
HISTORY OF 112G-XSR AT OIF

CONTRIBUTION NUMBER: oif2018.160.02
WORKING GROUP(s):   PLL
TITLE: CEI 112G System in Package (SiP) Project Start Proposal
SOURCE (Name, Company): Valery Kugel, Jeffery Maki, Juniper Networks
DATE: 04/24/2018

ABSTRACT: We propose a CEI 112G project to define a 112 Gb/s CMOS-to-CMOS and CMOS-to-SiGe on organic-package electrical interface for use in the range of 72 to 116 Gbps for System in Package (SiP) applications. The channel bump-to-bump distance is up to 50mm with up to 6 to 10 dB loss at 28 GHz.

www.oiforum.com
oif2018.160.02

CEI-112G-XSR Project Proposal

Contribution Number: OIF2018.178.01
Working Group: PLL
Title: CEI-112G-XSR Common Electrical Interface
    Project Proposal for Die-to-Die and Die-to-OE
Source: PLL Working Group

Presenters: Mike Li (Intel), Klaus-Holger Otto (Nokia)
Date: April 23, 2018

Abstract: This presentation proposes a CEI-112G-XSR project which will develop IA specifications for die-to-die (D2D) and die-to-OE (D2OE) electrical I/O interfaces which can be used to support Nx112G I/O links with significantly reduced power, complexity, and enhanced throughput density.

CEI-112G-XSR Project Proposal

Valery Kugel (Juniper), Mike Li (Intel), Jeffery Maki (Juniper), Klaus-Holger Otto (Nokia)

Apr. 26, 2018

Oif2018.214.02

Juniper Networks

DIFFERENCE BETWEEN PCB AND XSR SIGNALING MEDIA

WHAT IS SPECIAL ABOUT ORGANIC SUBSTRATE AND XSR?

Organic substrate is vastly different from PCB in both technology and sizing:

Minimum metal pitch is ~ 20um vs. ~200um.

Typical total thickness of top build up layers in a substrate is **~400um (8-2-8)** vs. **~4mm** PCB thickness for modern networking applications (~30 layers);

Vias, which are a major source of coupling, are by order of magnitude different in length between the substrate and PCB
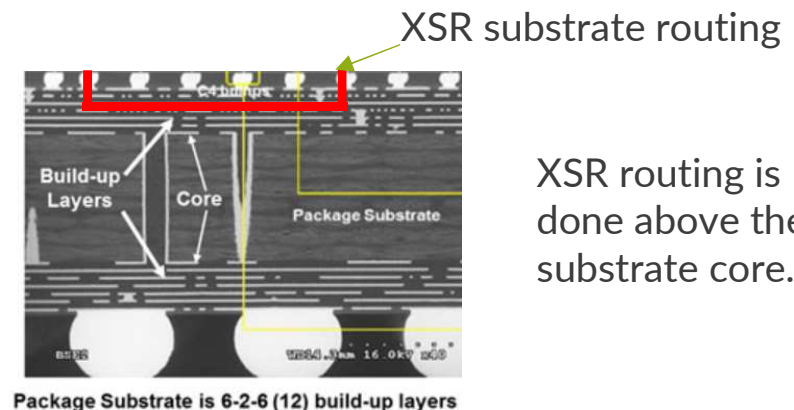

Example of PCB stackup

XSR substrate routing

XSR routing is done above the substrate core.

Package Substrate is 6-2-6 (12) build-up layers

USE CASES

XSR USE CASE: SPLITTING ASICS AND/OR USING CHIPLETS

Network BW scaling requirements above Moore law results in an increase in networking ASIC die size with every technology generation. The die size reaches dimensions dictated by reticle limit;

LR SerDeses occupy a large portion of the ASIC area - 20-30%;

Splitting networking ASICs and/or moving LR SerDeses to chiplets become a viable solution;

Using 112G-XSR requires FEC.
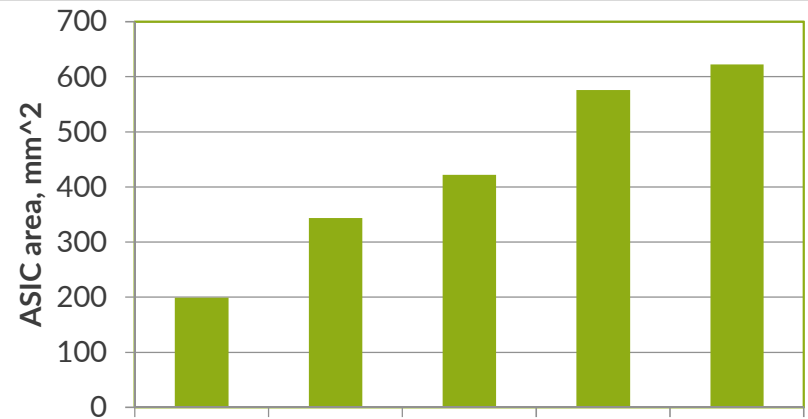
SerDes tile (chiplet)

ASIC

ASIC1   ASIC2
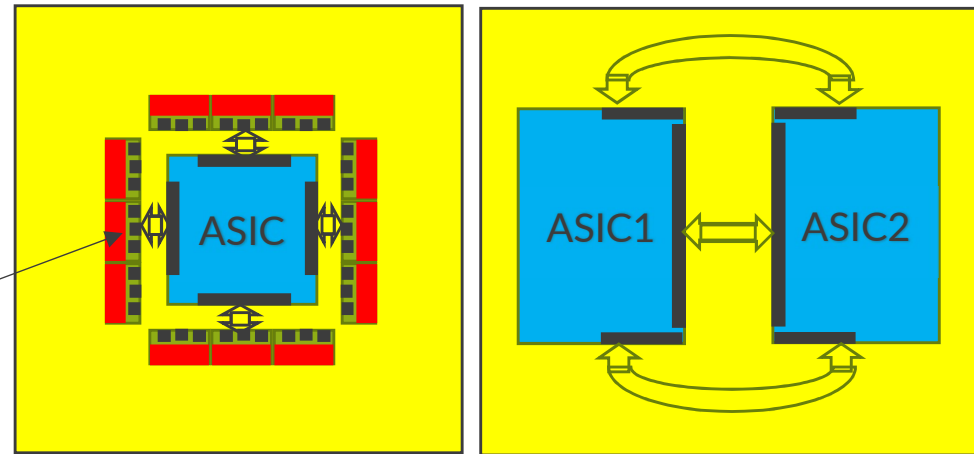
XSR USE CASE: INTEGRATED OPTICS

Example: Integrating 400G client optics with ASIC can both reduce overall system power and increase BW.

Supporting 100G-LR, 100G-FR, 100G-DR requires clock recovery per 100G lane. To keep functionality of the optics as in plug-able modules, per lane clock recovery needs to be supported by XSR.

BASIC REQUIREMENTS

BASIC REQUIREMENTS FOR THE XSR

- XSR SerDes Area, Power 4X better than the same for CEI-112G-LR, Beach Front BW 2X better than the same for LR;

- Need to support a reach from a couple of mm to 50mm (bump to bump);
  - The shortest channel is dictated by package design rules and can be a couple of millimeters;
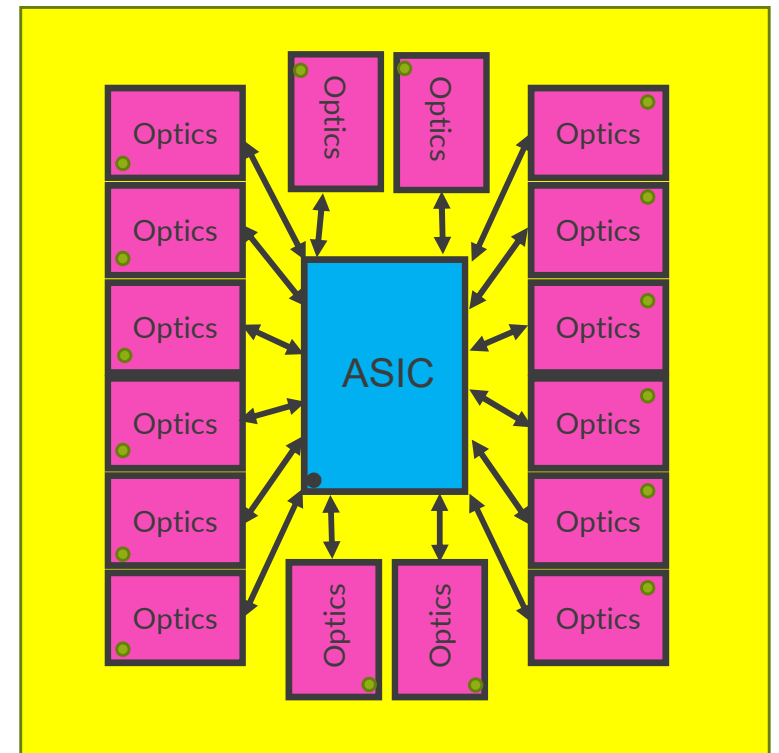 - As package size can reach 80-100mm on a side, electrical channel can reach 50mm in length;
  - Maximum insertion Loss (IL) @28GHz: 10dB; no connector;
  - preFEC BER 2 options: <1E-8 and <1E-9;
  - Must support Ethernet optics at 100G/200G/400G using 100G electrical lanes.
    - Means that the implementation agreement should support a retimed optical receive data path needing an n-wide electrical interface for which n can be as small as 1

XSR CHANNELS

Examples of Electrical Channels

CHIP   CHIP
organic substrate
Channel: bump – organic substrate - bump

substrate

CHIP   CHIP
organic substrate
Channel: bump -substrate –organic substrate - substrate - bump

substrate

CHIP   CHIP
organic substrate
Channel: bump - organic substrate - substrate – bump.
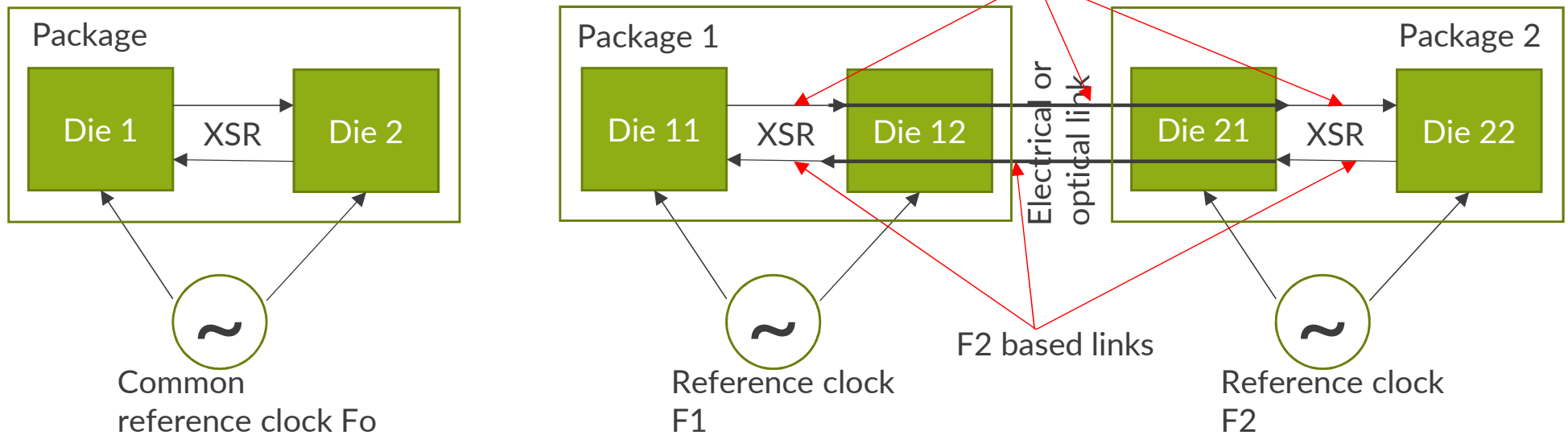
Organic substrate loss target:
0.12-0.14dB/mm @28GHz
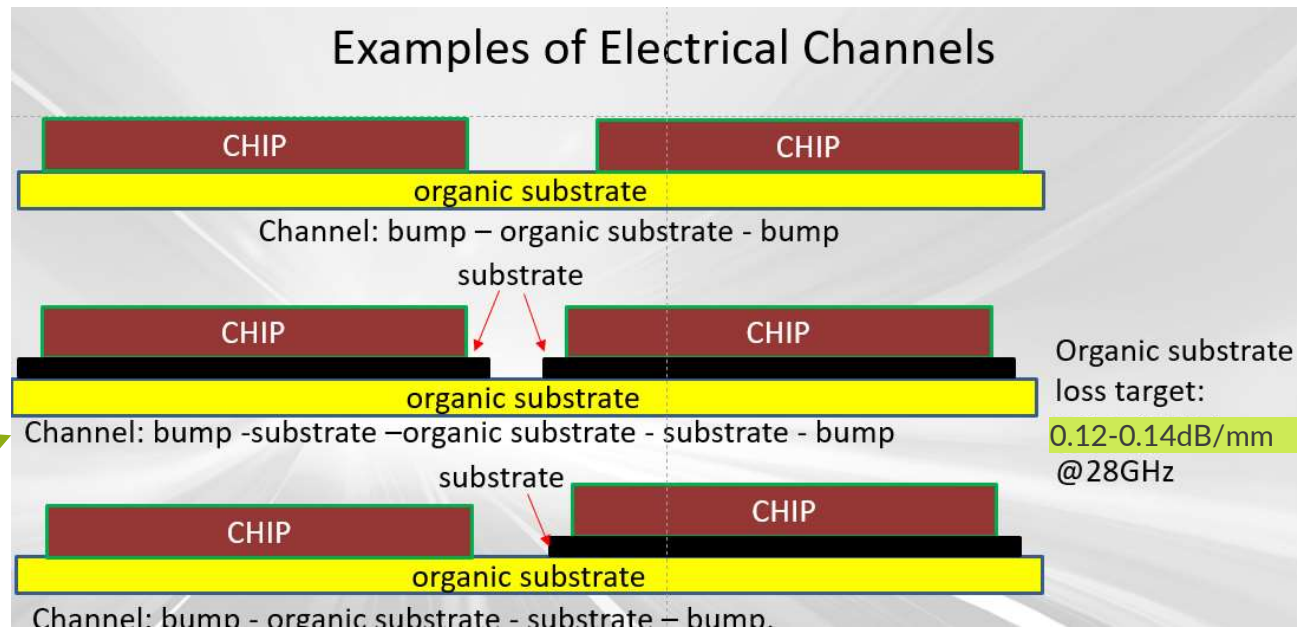
Can the standard support the electrical channels and similar? Can XSR support LGA?

Important observation: With current substrate technology IL is dominant by Ohmic loss till at least 56GHz and surface roughness is a very important factor in the Ohmic loss.

EXAMPLES OF SYSTEM LEVEL XSR REFERENCE CLOCKS

Common reference clock Fo

Reference clock F1

Reference clock F2

F1 based links

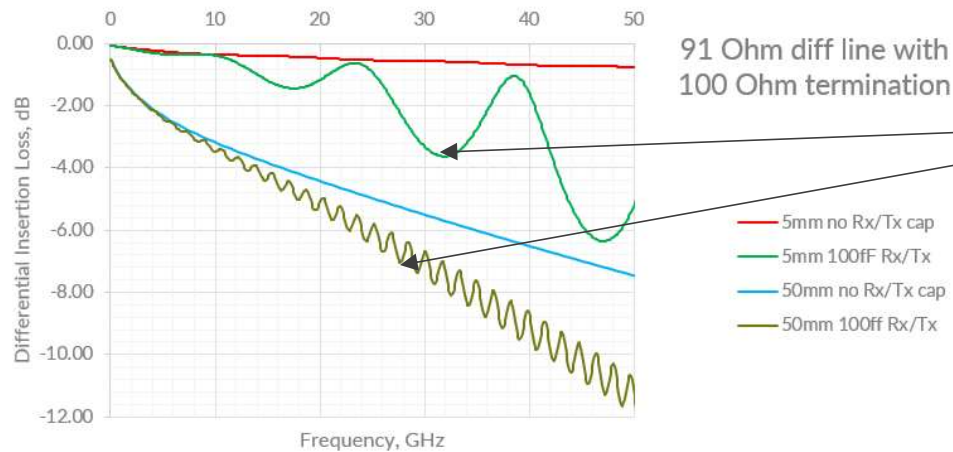F2 based links

Electrical or optical link

The picture above can represent all XSR links or a group of the links (a group could be as small as one link).
One of the packages can be w/o XSR links.

CHALLENGES & TIPS

CHALLENGES

Insertion Loss Deviation (ILD) can be significant in short channels and is caused by impedance mismatch due to capacitive load of Tx/Rx, substrate u-vias and routing in the escape area under dies;

TRANSMISSION LINE INSERTION LOSS

91 Ohm diff line with
100 Ohm termination

- 5mm no Rx/Tx cap
- 5mm 100fF Rx/Tx
- 50mm no Rx/Tx cap
- 50mm 100ff Rx/Tx

Caused by reflections at the cap loads

CHALLENGES (REUSE) CONTINUED

Reusing the same XSR SerDes IP in multiple chips/chiplets requires ability to route signals between a SerDes macro and its rotated/mirrored copy w/o transition via between dies.
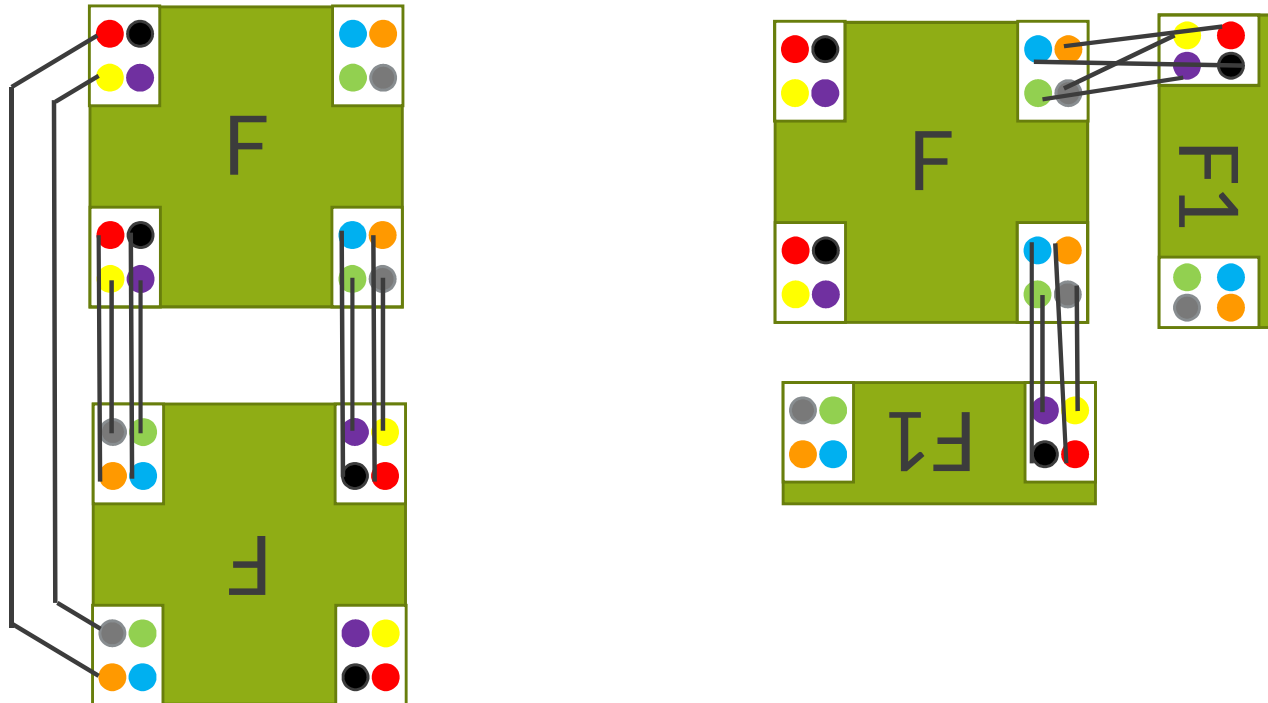
TIPS FOR XSR SERDES DESIGN

- Minimizing number of SerDes power suppliers – 2 is the best (including digital VDD);
- Minimizing number of test and misc. bumps;
- XSR SerDes bump map needs to be based on package routing studies. The routing studies must include both signal and power routing.

CURRENT STATUS

- Very significant momentum in the industry;
- All major ASIC and SerDes IP vendors are working on 112G-XSR designs (10+ suppliers); at least 2 suppliers have working silicon;
- OIF XSR project status: version 0.3 (OIF2019.065.03) was discussed at last OIF meeting in New Orleans (February 2020). Expect final version of the standard by end of 2020.

Juniper Networks

CONCLUSIONS AND FUTURE

- There is very significant momentum in the industry to develop 112G-XSR IP and the XSR has a potential to be the workhorse for in-package high-speed signaling over a common organic substrate.

- The XSR signaling should be able to scale for at least 2 more generations: 224G and 448G;

- This will require scalability of organic substrate technology, CMOS technology and new signaling formats.

JUNIPer
NETWORKS

THANK YOU!