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# RunBMC

BMC daughter board I/O specification

V0.17

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# Table of Contents

[1. License 2](#_Toc531265011)

[2. Table of Contents 3](#_Toc531265012)

[3. Scope 5](#_Toc531265013)

[4. Overview 6](#_Toc531265014)

[5. BMC Daughter Board Signaling Interface 6](#_Toc531265015)

[5.1 Signal Function Groups 6](#_Toc531265016)

[5.2 Signal Requirements and Descriptions 7](#_Toc531265017)

[5.2.1 Power 7](#_Toc531265018)

[5.2.2 ADC 7](#_Toc531265019)

[5.2.3 PCIe 7](#_Toc531265020)

[5.2.4 Ethernet and RGMII 8](#_Toc531265021)

[5.2.5 VGA 8](#_Toc531265022)

[5.2.6 RMII/NC-SI 9](#_Toc531265023)

[5.2.7 JTAG 9](#_Toc531265024)

[5.2.8 USB2A Host/Device 9](#_Toc531265025)

[5.2.9 USB2B Device 10](#_Toc531265026)

[5.2.10 Firmware SPI 10](#_Toc531265027)

[5.2.11 SPI Master Interface for Host 10](#_Toc531265028)

[5.2.12 LPC/eSPI 10](#_Toc531265029)

[5.2.13 I2C 11](#_Toc531265030)

[5.2.14 UART 11](#_Toc531265031)

[5.2.15 PWM 11](#_Toc531265032)

[5.2.16 TACH 11](#_Toc531265033)

[5.2.17 PECI 11](#_Toc531265034)

[5.2.18 GPIO / GPO / GPI 11](#_Toc531265035)

[5.2.19 SGPIO 12](#_Toc531265036)

[5.2.20 RESET and POWERGOOD 12](#_Toc531265037)

[5.2.21 WATCHDOG 12](#_Toc531265038)

[5.2.22 INDICATOR 12](#_Toc531265039)

[5.2.23 Reserved/KLUDGE 12](#_Toc531265040)

[*5.3* Pin Definition 12](#_Toc531265041)

[5.4 Signal Priority and Nomenclature 15](#_Toc531265042)

[6. Electrical and Timing Requirements 22](#_Toc531265043)

[6.1 Electrical Requirements 22](#_Toc531265044)

[6.2 Timing Requirements 23](#_Toc531265045)

[7. Mechanical 23](#_Toc531265046)

[7.1 Form Factor 23](#_Toc531265047)

[7.2 Component Height Keep-out Requirements 24](#_Toc531265048)

[7.3 RU/OU Mounting Options 25](#_Toc531265049)

[7.4 Mating Connector 25](#_Toc531265050)

[8. Thermal 26](#_Toc531265051)

[9. FRU Requirements 26](#_Toc531265052)

[10. Platform Guidelines 26](#_Toc531265053)

[11. References 26](#_Toc531265054)

# Scope

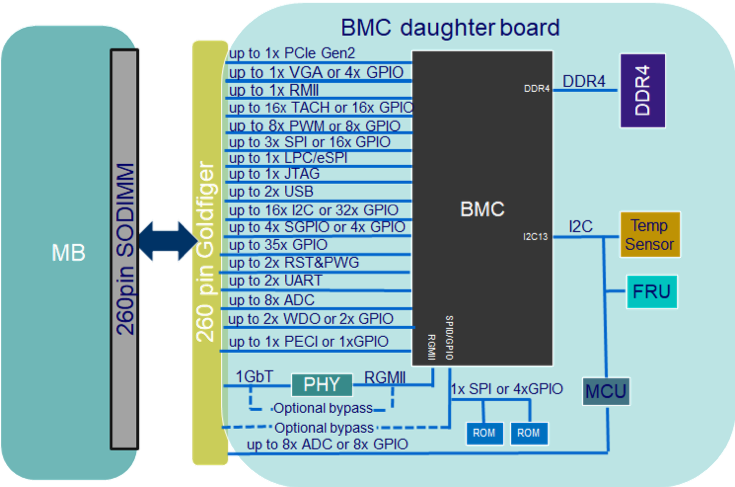
This document defines the technical specifications for the runBMC used in Open Compute Project.

# Overview

This document describes the runBMC daughter board card design for use with Open Compute Project motherboards. This specification defines the interface between the Baseboard Management Controller(BMC) subsystem and OCP hardware platforms, such as network or compute motherboards.

The runBMC daughter board interfaces with hardware platforms through a 260 pin SODIMM DDR4 connector, which is intended for mounting into a mating SODIMM DDR4 socket.

Figure 1 shows an example of the BMC daughter board I/O connectivity



# BMC Daughter Board Signaling Interface

## Signal Function Groups

Signal function groups can be summarized in Table 1.

*Table 1 BMC Function Group Summary*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function** | **Signal Count for Interface** | **Number of Interfaces** | **Number of used pins** | **Total Signals** |
|  |  |  |  |  |
| **Form Factor - 260 SO-DIMM4** |  |  |  |  |
| Power 3.3V |  |  | 5 | 5 |
| VDD\_IO\_REF |  |  | 1 | 1 |
| LPC 3.3v or ESPI 1.8v |  |  | 1 | 1 |
| Power 12 V |  |  | 1 | 1 |
| Ground |  |  | 38 | 38 |
| ADC | 1 | 8 | 8 | 8 |
| GPI/ADC | 1 | 8 | 8 | 8 |
| **PCIe** | 7 | 1 | 7 | 7 |
| **RGMII/1GT PHY** | 14 | 1 | 14 | 14 |
| VGA / GPIOs | 7 | 1 | 7 | 7 |
| RMII/NC-SI | 10 | 1 | 10 | 10 |
| **Master JTAG/GPIO** | 6 | 1 | 6 | 6 |
| **USB host** | 4 | 1 | 4 | 4 |
| **USB device** | 3 | 1 | 3 | 3 |
| SPI1: SPI for host - quad capable | 7 | 1 | 7 | 7 |
| SPI2: SPI for host | 5 | 1 | 5 | 5 |
| FWSPI: SPI for Boot - quad capable | 7 | 1 | 7 | 7 |
| SYSSPI: System SPI | 4 | 1 | 4 | 4 |
| LPC/eSPI | 8 | 1 | 8 | 8 |
| I2C / GPIOs | 2 | 12 | 24 | 24 |
| GPIOs / I2C | 2 | 3 | 6 | 6 |
| I2C | 2 | 1 | 2 | 2 |
| UARTs (TxD, RxD) | 2 | 4 | 8 | 8 |
| CONSOLE (Tx, Rx) | 2 | 1 | 2 | 2 |
| PWM | 1 | 8 | 8 | 8 |
| Tacho/GPIOs | 1 | 16 | 16 | 16 |
| **PECI** | 2 | 1 | 2 | 2 |
| GPIOs | 1 | 37 | 37 | 37 |
| GPIO/GPIO Expanders (Serial GPIO) | 4 | 1 | 4 | 4 |
| Reset and Power Good | 1 | 2 | 2 | 2 |
| Watchdogs/GPIO | 1 | 2 | 2 | 2 |
| BOOT\_IND# / GPIO | 1 | 1 | 1 | 1 |
| RESERVED/KLUDGE | 1 | 2 | 2 | 2 |

## Signal Requirements and Descriptions

## Power

For all power requirements (red cells highlighted Table-1), please reference “Electrical and Timing Requirements”.

## ADC

The Interface has 16 voltage sensing channels available to use. 8 of these are primary functional as ADC. The remaining 8 primarily function as GPI (General Purpose Input) but may be configured as ADC if desired.

## PCIe

The PCIe connection supports a PCI-Express Gen 2 One Lane (x1) connection.

## Ethernet and RGMII

The interface shall allow flexibility for a Ethernet interface as primary function as shown below in “1GbT Interface”. Secondary functionally I/Os allow for a RGMII interface to be routed over the connector if desired as shown in the “RGMII interface”

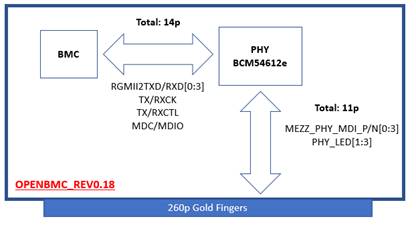


Figure 5‑1 1GbT Interface

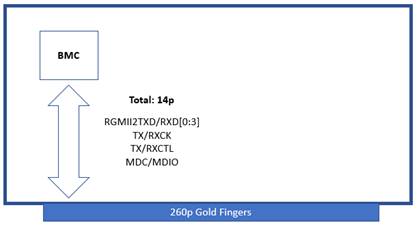


Figure 5‑2 RGMII Interface

## VGA

The following pins provide VGA functionality:

|  |  |
| --- | --- |
| Signal Name | Description |
| DACB | DAC B channel output |
| DACG | DAC G channel output |
| DACR | DAC R channel output |
| DDCCLK\_GPIO | VGA DDC clock pin |
| DDCDAT\_GPIO | VGA DDC data pin |
| VGAHS\_GPIO | VGA horizontal sync output |
| VGAVS\_GPIO | VGA vertical sync output |

Motherboard designer should ensure proper RGB terminations based on RGB trace impedance; termination schemes are not guaranteed by the RunBMC specification. Designers should reference BMC vendor design guide.

## RMII/NC-SI

RMII/NC-SI is provided through a single interface. MDC and MDIO signals are also routed over the connector specific to this interface.

## JTAG

Interface defines a single JTAG, which is meant to act as a master. The typical 5 signals are defined including RTCK as a sixth signal not typically used in master applications.

|  |  |
| --- | --- |
| Signal Name | Description |
| JTAG1TRST | Defines Test Reset, output from BMC |
| JTAG1TMS | Test Mode Select, output from BMC |
| JTAG1TDO | Test Data Out, input to BMC |
| JTAG1TDI | Test Data In, output from BMC |
| JTAG1TCK | Test Clock, output from BMC |
| JTAG1RTCK | Return Test Clock, input to BMC (if used) |

## USB2A Host/Device

The USB2A interface has the host and device functionality. Two additional signals for USB is included, which are optional.

|  |  |  |
| --- | --- | --- |
| Signal Name | Description | Notes |
| USB2AVBUSOVC | Host/device Overcurrent sense | Over-current interrupt input from motherboard to detect if a USB device powered by the motherboard and attached to the BMC exceeds the specified current for the USB port. |
| USB2AVBUSC | Host/device VBUS Control | Output to control 5V supply to USB device. In the case that the USB Device attached to the BMC enters an over-current state (as indicated by USB Over Current Sense) the BMC will de-assert this signal and 5 V supply to the USB device will go into a low voltage or low current state, such that the device will no longer have power. |

## USB2B Device

The USB2B interface has USB device capability. One additional signal for USB is included, which is optional.

|  |  |  |
| --- | --- | --- |
| Signal Name | Description | Notes |
| USB2BVBUSSNS | Device VBUS Sense | Detects 5 V supply is asserted and allows the BMC to have its device port begin USB host negotiation. Note that use of the 5 V supply detect is meant to indicate to the BMC as a device that a host is attached and supplying power. |

## Firmware SPI

The BMC boots from a flash memory device located on the Serial Peripheral Interface (SPI) bus. The device size is 256Mb (32MB) minimum and can be used to store FPGA, CPLD , and miscellaneous recovery images.

A secondary device is supported to provide BMC recovery and firmware updates, which can be used by the extra chip select. The daughterboard can have these onboard or utilize the secondary function signal pins over the connector if placement on the baseboard is mandatory. Refer to Signal Priority and Nomenclature section of this specification.

## SPI Master Interface for Host

Three additional Serial Peripheral Interface (SPI) Master Controller interface signals are routed over the connector. Two busses provide two chip selects used to select the primary or secondary SPI Flash device’s if used. The remaining bus (SYSSPI) only has 1 chip select.

All SPI Host interfaces are multiplexed with GPIOs.

|  |  |  |  |
| --- | --- | --- | --- |
| SPI | Net Name | Quad SPI Support1 | CS |
| Firmware/Boot SPI | FWSPI\* | Y | 2 |
| Host SPI Interface 1 | SPI1\* | Y | 2 |
| Host SPI Interface 2 | SPI2\* | N | 2 |
| System SPI | SYSSPI\* | N | 1 |

1. Quad SPI is supported by the RunBMC interface but not guaranteed by the SoC

## LPC/eSPI

The Low Pin Count (LPC) interface used by most systems to provide communication up to the host is provided; some future systems are designing towards the eSPI specification. Eight pins of the RunBMC connector can be exclusively used for one of these two interfaces.

## I2C

The interface features multiple I2C Bus compatible 2-wire interfaces consisting of a serial data line (SDA) and a serial clock line (SCL). If the daughterboard contains drives that are open-drain, the baseboard device shall require a pullup resistor to generate a logic high voltage and shall remain high even when the bus is idle.

Proper power domain isolation shall be implemented on the daughterboard. The AC/DC specifications are defined in the SMBus 2.0 and I2C bus specifications

## UART

5 total UART interfaces are available to use. 3 UART interfaces are expected to be primary functioning and 2 are available if daughter board supports functionality. 1 UART is to be named CONSOLE for default BMC console output if desired.

|  |  |  |
| --- | --- | --- |
| UART | Net Name | HW Flow Control Capable |
| Default Console | CONSOLE\* | N |
| UART[1-4] | UART[1-4]\* | N |

## PWM

PWM output from BMC, meant to drive fans or pumps. It is expected that these signals have whatever necessary level conversion on the baseboard. It is the responsibility of the motherboard designer to add circuitry to properly isolate the BMC signals from the fans or pumps being controlled.

## TACH

Tachometer input to BMC. It is expected that these signals have whatever necessary level conversion before going over the interface. It is the responsibility of the motherboard designer to add circuitry to properly isolate the BMC signals from tachometer signals being read from fans or pumps.

## PECI

An Intel proprietary bus meant to read die temperature. This defines two pins, PECI and PECIVDD. PECI is a 1-wire data signal that acts as bi-directional signal to the BMC. PECIVDD is the host voltage that defines a reference for the PECI interface.

## GPIO / GPO / GPI

Any GPIO is defined in the literal sense that it may be used for the purpose of defining an input or output signal to the BMC. These are software configurable for use throughout the baseboard as indicators, control pins, interrupts, and input logic read by the BMC. In the case of GPI and GPO, these pins are fixed as input and output respectively.

## SGPIO

SGPIO is the Serial GPIO interface. The HW Interface describes a single Serial GPIO Master, though in some modules this may also act as a slave monitor. There are four signals defined as master:

|  |  |
| --- | --- |
| Signal Name | Description |
| SGPMCK | Master Serial GPIO Clock Output, controlling clock for the bus, output from the BMC |
| SGPMI | Master Serial GPIO Serial Data Input, an input to the BMC |
| SGPMLD | Master Serial GPIO Serial Data Load, an output from the BMC |
| SGPMO | Master Serial GPIO Serial Data Output, an output from the BMC |

## RESET and POWERGOOD

Reset signal is an active low input to the BMC, this pin will reset the BMC subsystem. PWRGD is an input to the BMC; used for high priority interrupt derived from power supply status.

## WATCHDOG

Two Watchdog resets, which are output signals, are used to reset system components. For example, this signal can be used to reset a TPM in the scenario of a watchdog timeout on the BMC so that the system reboots properly.

## INDICATOR

This defines generic indication from the module to the system. The use of this pin is dependent on the BMC module used, so consult specific documentation for that module.

## Reserved/KLUDGE

Two KLUDGE pins are reserved for future use. Secondary functions support GPIO.

## Pin Definition

The BMC daughter board shall have the following pinout:

*Table 2 BMC connector/edge pinout*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Pin # | Name |  | Name | Pin # |
| 1 | VDD\_12V\_STBY |  | VDD\_IO\_REF | 2 |
| 3 | VDD3\_3V\_STBY |  | VDD3\_3V\_STBY | 4 |
| 5 | VDD3\_3V\_STBY |  | VDD3\_3V\_STBY | 6 |
| 7 | VDD3\_3V\_STBY |  | GND | 8 |
| 9 | GND |  | DACG | 10 |
| 11 | GND |  | DACB | 12 |
| 13 | GPIO0\_SGPMLD |  | DACR | 14 |
| 15 | GPIO1\_SGPMI |  | VGAHS\_GPIO2 | 16 |
| 17 | GPIO3\_SGPMO |  | VGAVS\_GPIO4 | 18 |
| 19 | GPIO5\_SGPMCK |  | DDCCLK\_GPIO6 | 20 |
| 21 | CONSOLERX |  | DDCDAT\_GPIO8 | 22 |
| 23 | CONSOLETX |  | GND | 24 |
| 25 | GPIO7 |  | PWM0\_GPIO10 | 26 |
| 27 | PWM2\_GPIO9 |  | PWM1\_GPIO12 | 28 |
| 29 | PWM4\_GPIO11 |  | PWM3\_GPIO14 | 30 |
| 31 | PWM6\_GPIO13 |  | PWM5\_GPIO16 | 32 |
| 33 | GND |  | PWM7\_GPIO18 | 34 |
| 35 | GPIO15 |  | GPIO19 | 36 |
| 37 | GPIO17 |  | GPIO20 | 38 |
| 39 | GND |  | GPIO21 | 40 |
| 41 | UART1RX\_GPIO23 |  | UART2RX\_GPIO22 | 42 |
| 43 | UART1TX\_GPO0 |  | UART2TX\_GPIO24 | 44 |
| 45 | GND |  | GPIO25 | 46 |
| 47 | I2C8SCL\_GPIO26 |  | I2C13SCL | 48 |
| 49 | I2C8SDA\_GPIO27 |  | I2C13SDA | 50 |
| 51 | GND |  | GND | 52 |
| 53 | I2C7SCL\_GPIO29 |  | I2C6SCL\_GPIO28 | 54 |
| 55 | I2C7SDA\_GPIO31 |  | I2C6SDA\_GPIO30 | 56 |
| 57 | GND |  | GND | 58 |
| 59 | GPIO33\_FWSPIWP# |  | I2C5SCL\_GPIO32 | 60 |
| 61 | GPIO35\_INDICATOR# |  | I2C5SDA\_GPIO34 | 62 |
| 63 | FWSPICS0# |  | GND | 64 |
| 65 | FWSPIMOSI\_IO0 |  | GPIO36 | 66 |
| 67 | FWSPIMISO\_IO1 |  | GPIO37 | 68 |
| 69 | FWSPI\_IO2\_GPIO39 |  | GPIO38 | 70 |
| 71 | FWSPI\_IO3\_GPIO41 |  | GPIO40 | 72 |
| 73 | FWSPICK |  | GPIO42 | 74 |
| 75 | FWSPICS1# |  | GPIO43 | 76 |
| 77 | PWRGD |  | TACH0\_GPIO44 | 78 |
| 79 | GPIO45 |  | TACH1\_GPIO46 | 80 |
| 81 | GPIO47 |  | TACH2\_GPIO48 | 82 |
| 83 | WDTRST2\_GPIO49 |  | TACH3\_GPIO50 | 84 |
| 85 | GPIO51 |  | TACH4\_GPIO52 | 86 |
| 87 | GPIO53 |  | TACH5\_GPIO54 | 88 |
| 89 | GPIO55 |  | TACH6\_GPIO56 | 90 |
| 91 | WDTRST1\_GPIO57 |  | TACH7\_GPIO58 | 92 |
| 93 | GPIO59 |  | TACH8\_GPIO60 | 94 |
| 95 | GPIO61 |  | TACH9\_GPIO62 | 96 |
| 97 | KLUDGE\_GPIO63 |  | TACH10\_GPIO64 | 98 |
| 99 | KLUDGE\_GPIO65 |  | TACH11\_GPIO66 | 100 |
| 101 | GPIO67 |  | TACH12\_GPIO68 | 102 |
| 103 | GPIO69 |  | TACH13\_GPIO70 | 104 |
| 105 | GPIO71 |  | TACH14\_GPIO72 | 106 |
| 107 | GPIO73 |  | TACH15\_GPIO74 | 108 |
| 109 | GPIO75 |  | GND | 110 |
| 111 | PECIVDD |  | PECI | 112 |
| 113 | GPIO76 |  | GND | 114 |
| 115 | GPIO77 |  | SPI2CK\_GPIO78 | 116 |
| 117 | GPIO79 |  | SPI2MISO\_GPIO80 | 118 |
| 119 | GPIO81 |  | SPI2MOSI\_GPIO82 | 120 |
| 121 | GPIO83 |  | SPI2CS0#\_GPIO84 | 122 |
| 123 | I2C2SCL\_GPIO85 |  | SPI2CS1#\_GPIO86 | 124 |
| 125 | I2C2SDA\_GPIO87 |  | GND | 126 |
| 127 | GND |  | I2C1SCL\_GPIO88 | 128 |
| 129 | GPIO89\_I2C14SCL |  | I2C1SDA\_GPIO90 | 130 |
| 131 | GPIO91\_I2C14SDA |  | GND | 132 |
| 133 | GND |  | I2C4SCL\_GPIO92 | 134 |
| 135 | GPIO93\_I2C16SCL |  | I2C4SDA\_GPIO94 | 136 |
| 137 | GPIO95\_I2C16SDA |  | GPIO96 | 138 |
| 139 | GND |  | GPIO97 | 140 |
| 141 | I2C12SCL\_GPIO98 |  | PERSTN | 142 |
| 143 | I2C12SDA\_GPIO99 |  | GPIO100\_UART3RX | 144 |
|  | Mechanical Key | | |  |
| 145 | GND |  | GPIO101\_UART3TX | 146 |
| 147 | PERXN |  | GPIO102\_UART4RX | 148 |
| 149 | PERXP |  | GPIO103\_UART4TX | 150 |
| 151 | GND |  | VDD\_LPC3V3\_ESPI1V8 | 152 |
| 153 | PETXN |  | GPIO104 | 154 |
| 155 | PETXP |  | GPIO105 | 156 |
| 157 | GND |  | GPIO106 | 158 |
| 159 | PEREFCLKN |  | GPIO107 | 160 |
| 161 | PEREFCLKP |  | JTAG1TRST | 162 |
| 163 | GND |  | JTAG1TDO | 164 |
| 165 | LPCRST#\_ESPIRST# |  | JTAG1TDI | 166 |
| 167 | LPCD1\_ESPID1 |  | JTAG1RTCK | 168 |
| 169 | LPCD0\_ESPID0 |  | JTAG1TCK | 170 |
| 171 | LPCIRQ#\_ESPIALERT# |  | JTAG1TMS | 172 |
| 173 | LPCFRAME#\_ESPICS# |  | ADC0 | 174 |
| 175 | LPCD3\_ESPID3 |  | ADC1 | 176 |
| 177 | LPCD2\_ESPID2 |  | ADC2 | 178 |
| 179 | LPCCLK\_ESPICLK |  | ADC3 | 180 |
| 181 | I2C9SCL\_GPIO108 |  | ADC4 | 182 |
| 183 | I2C9SDA\_GPIO109 |  | ADC5 | 184 |
| 185 | GND |  | ADC6 | 186 |
| 187 | I2C10SCL\_GPIO110 |  | ADC7 | 188 |
| 189 | I2C10SDA\_GPIO111 |  | SYSCS#\_GPIO112 | 190 |
| 191 | GND |  | SYSMISO\_GPO1 | 192 |
| 193 | GPIO113\_I2C15SCL |  | SYSMOSI\_GPO2 | 194 |
| 195 | GPIO115\_I2C15SDA |  | SYSCK\_GPIO114 | 196 |
| 197 | GND |  | SPI1CS0#\_GPIO116 | 198 |
| 199 | I2C11SCL\_GPIO117 |  | SPI1MOSI\_IO0\_GPO3 | 200 |
| 201 | I2C11SDA\_GPIO118 |  | SPI1MISO\_IO1\_GPO4 | 202 |
| 203 | GND |  | GPO5\_SPI1\_IO2 | 204 |
| 205 | I2C3SCL\_GPIO119 |  | GPIO120\_SPI1\_IO3 | 206 |
| 207 | I2C3SDA\_GPIO121 |  | SPI1CK\_GPIO122 | 208 |
| 209 | GPIO123\_USB2BVBUSSNS |  | SPI1CS1#\_GPIO124 | 210 |
| 211 | GPIO125\_USB2AVBUSSNS |  | GND | 212 |
| 213 | GPIO126\_USB2APWREN |  | RMIIMDIO | 214 |
| 215 | GND |  | RMIICRSDV | 216 |
| 217 | USB2A\_HD\_DN |  | RMIIMDC | 218 |
| 219 | USB2A\_HD\_DP |  | RMIIRCLKI | 220 |
| 221 | GND |  | RMIIRXER | 222 |
| 223 | USB2B\_D\_DN |  | RMIITXEN | 224 |
| 225 | USB2B\_D\_DP |  | GND | 226 |
| 227 | GND |  | RMIIRXD0 | 228 |
| 229 | TRD0P\_RGMIITXD0 |  | RMIIRXD1 | 230 |
| 231 | TRD0N\_RGMIIRXD0 |  | GND | 232 |
| 233 | GND |  | RMIITXD0 | 234 |
| 235 | TRD1N\_RGMIIRXD1 |  | RMIITXD1 | 236 |
| 237 | TRD1P\_RGMIITXD1 |  | GND | 238 |
| 239 | GND |  | PHYLED1\_RGMIITXCK | 240 |
| 241 | TRD2P\_RGMIITXD2 |  | PHYLED2\_RGMIIRXCTL | 242 |
| 243 | TRD2N\_RGMIIRXD2 |  | PHYLED3\_RGMIITXCTL | 244 |
| 245 | GND |  | GPIO127\_RGMIIMDC | 246 |
| 247 | TRD3N\_RGMIIRXD3 |  | GPIO128\_RGMIIMDIO | 248 |
| 249 | TRD3P\_RGMIITXD3 |  | RGMIIRXCK | 250 |
| 251 | GND |  | GPI0\_ADC8 | 252 |
| 253 | BMC\_RESET# |  | GPI1\_ADC9 | 254 |
| 255 | GPI3\_ADC11 |  | GPI2\_ADC10 | 256 |
| 257 | GPI5\_ADC13 |  | GPI4\_ADC12 | 258 |
| 259 | GPI7\_ADC15 |  | GPI6\_ADC14 | 260 |

## Signal Priority and Nomenclature

The BMC pinout specification outlines the functions of the physical pins. To allow for system flexibility many of the pins in the interface must be capable of dual-function; i.e. they must provide capability for both functions.

Most of these dual function pins are achieved through software multiplexing, however some pins only have a singular function. The direction column’s origin is the SOC on the runBMC module, i.e. “output” signals are driven from the SOC over the connector.

*Table 3 BMC functions*

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Functions** | **Net Name** | **Function 1** | **Function 2** | **Direction** | **Description Function 1** | **Description Function 2** |
| 1 GbT/RGMII/GPIO | RGMIIRXCK | RGMIIRXCK |  | BI | **RGMII 2 receive clock** |  |
| 1 GbT/RGMII/GPIO | PHYLED1\_RGMIITXCK | PHYLED1 | RGMIITXCK | BI | GPIO intended for MAGJACK LEDs, or signal from PHY | **RGMII 2 transmit clock** |
| 1 GbT/RGMII/GPIO | PHYLED2\_RGMIIRXCTL | PHYLED2 | RGMIIRXCTL | BI | GPIO intended for MAGJACK LEDs, or signal from PHY | **RGMII 2 receive control** |
| 1 GbT/RGMII/GPIO | PHYLED3\_RGMIITXCTL | PHYLED3 | RGMIITXCTL | BI | GPIO intended for MAGJACK LEDs, or signal from PHY | **RGMII 2 transmit control** |
| 1 GbT/RGMII/GPIO | GPIO\_RGMIIMDC | GPIO | RGMIIMDC | Output | GPIO | **Management Data Clock. The MDC clock input must be provided to allow MII management functions.** |
| 1 GbT/RGMII/GPIO | GPIO\_RGMIIMDIO | GPIO | RGMIIMDIO | BI | GPIO | **Management Data I/O. This serial input/output bit is used to read from and write to the MII registers** |
| 1 GbT/RGMII/GPIO | TRD0N\_RGMIIRXD0 | TRD0N | RGMIIRXD0 | BI | Transmit/Receive Pair 0 | **RGMII 2 receive data bus from PHY bit 0** |
| 1 GbT/RGMII/GPIO | TRD0P\_RGMIITXD0 | TRD0P | RGMIITXD0 | BI | Transmit/Receive Pair 0 | **RGMII 2 transmit data bus to PHY bit 0** |
| 1 GbT/RGMII/GPIO | TRD1N\_RGMIIRXD1 | TRD1N | RGMIIRXD1 | BI | Transmit/Receive Pair 1 | **RGMII 2 receive data bus from PHY bit 1** |
| 1 GbT/RGMII/GPIO | TRD1P\_RGMIITXD1 | TRD1P | RGMIITXD1 | BI | Transmit/Receive Pair 1 | **RGMII 2 transmit data bus to PHY bit 1** |
| 1 GbT/RGMII/GPIO | TRD2N\_RGMIIRXD2 | TRD2N | RGMIIRXD2 | BI | Transmit/Receive Pair 2 | **RGMII 2 receive data bus from PHY bit 2** |
| 1 GbT/RGMII/GPIO | TRD2P\_RGMIITXD2 | TRD2P | RGMIITXD2 | BI | Transmit/Receive Pair 2 | **RGMII 2 transmit data bus to PHY bit 2** |
| 1 GbT/RGMII/GPIO | TRD3N\_RGMIIRXD3 | TRD3N | RGMIIRXD3 | BI | Transmit/Receive Pair 3 | **RGMII 2 receive data bus from PHY bit 3** |
| 1 GbT/RGMII/GPIO | TRD3P\_RGMIITXD3 | TRD3P | RGMIITXD3 | BI | Transmit/Receive Pair 3 | **RGMII 2 transmit data bus to PHY bit 3** |
| 1.8V | VDD\_IO\_REF | VDD\_IO\_REF |  | Output | Reference voltage output for PCB | none |
| 12v | VDD\_12V\_STBY | VDD\_12V\_STBY |  | Power | 12v supply to PCB | none |
| 3.3V | VDD3\_3V\_STBY | VDD3\_3V\_STBY |  | Power | 3.3v supply to PCB | none |
| 3.3V | VDD3\_3V\_STBY | VDD3\_3V\_STBY |  | Power | 3.3v supply to PCB | none |
| 3.3V | VDD3\_3V\_STBY | VDD3\_3V\_STBY |  | Power | 3.3v supply to PCB | none |
| 3.3V | VDD3\_3V\_STBY | VDD3\_3V\_STBY |  | Power | 3.3v supply to PCB | none |
| 3.3V | VDD3\_3V\_STBY | VDD3\_3V\_STBY |  | Power | 3.3v supply to PCB | none |
| 3.3Vlpc or 1.8espi | VDD\_LPC3V3\_ESPI1V8 | VDD\_LPC3V3 | ESPI1V8 | Input | 3.3v supply to PCB LPC/eSPI | 1.8v supply if needed for eSPI |
| ADC | ADC0 | ADC0 |  | INPUT | channel 0 analog input |  |
| ADC | ADC1 | ADC1 |  | INPUT | **channel 1 analog input** |  |
| ADC | ADC2 | ADC2 |  | INPUT | **channel 2 analog input** |  |
| ADC | ADC3 | ADC3 |  | INPUT | **channel 3 analog input** |  |
| ADC | ADC4 | ADC4 |  | INPUT | **channel 4 analog input** |  |
| ADC | ADC5 | ADC5 |  | INPUT | **channel 5 analog input** |  |
| ADC | ADC6 | ADC6 |  | INPUT | **channel 6 analog input** |  |
| ADC | ADC7 | ADC7 |  | INPUT | **channel 7 analog input** |  |
| ADC/GPIO | GPI\_ADC10 | GPI | ADC10 | BI | GPI | **channel 10 analog input** |
| ADC/GPIO | GPI\_ADC11 | GPI | ADC11 | BI | GPI | **channel 11 analog input** |
| ADC/GPIO | GPI\_ADC12 | GPI | ADC12 | BI | GPI | **channel 12 analog input** |
| ADC/GPIO | GPI\_ADC13 | GPI | ADC13 | BI | GPI | **channel 13 analog input** |
| ADC/GPIO | GPI\_ADC14 | GPI | ADC14 | BI | GPI | **channel 14 analog input** |
| ADC/GPIO | GPI\_ADC15 | GPI | ADC15 | BI | GPI | **channel 15 analog input** |
| ADC/GPIO | GPI\_ADC8 | GPI | ADC8 | BI | GPI | **channel 8 analog input** |
| ADC/GPIO | GPI\_ADC9 | GPI | ADC9 | BI | GPI | **channel 9 analog input** |
| FWSPI | FWSPICK | FWSPICK |  | OUTPUT | BMC FW clock output for FW living on MB |  |
| FWSPI | FWSPICS0# | FWSPICS0# |  | OUTPUT | BMC FW chip select 0 for FW living on MB |  |
| FWSPI | FWSPICS1# | FWSPICS1# |  | OUTPUT | BMC FW chip select 1 for FW living on MB |  |
| FWSPI | FWSPIMISO\_IO1 | FWSPIMISO\_IO1 |  | BI | BMC FW MISO/IO0 for FW living on MB |  |
| FWSPI | FWSPIMOSI\_IO0 | FWSPIMOSI\_IO0 |  | BI | BMC FW MOSI/IO1 for FW living on MB |  |
| FWSPI | FWSPI\_IO2\_GPIO | FWSPI\_IO2 | GPIO | BI | BMC FW IO2 for FW living on MB to support quad | GPIO |
| FWSPI | FWSPI\_IO3\_GPIO | FWSPI\_IO3 | GPIO | BI | BMC FW IO3 for FW living on MB to support quad | GPIO |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GND | GND | GND |  |  | GND |  |
| GPIO | GPIO\_UART3TX | GPIO | UART3TX | BI | GPIO |  |
| GPIO | GPIO\_UART3RX | GPIO | UART3RX | BI | GPIO |  |
| GPIO | GPIO\_UART4TX | GPIO | UART4TX | BI | GPIO |  |
| GPIO | GPIO\_UART4RX | GPIO | UART4RX | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| GPIO | GPIO | GPIO |  | BI | GPIO |  |
| I2C | I2C10SCL\_GPIO | I2C10SCL | GPIO | BI | **I2C/SMBUS 10 clock** | GPIO |
| I2C | I2C10SDA\_GPIO | I2C10SDA | GPIO | BI | **I2C/SMBUS 10 data** | GPIO |
| I2C | I2C11SCL\_GPIO | I2C11SCL | GPIO | BI | **I2C/SMBUS 11 clock** | GPIO |
| I2C | I2C11SDA\_GPIO | I2C11SDA | GPIO | BI | **I2C/SMBUS 11 data** | GPIO |
| I2C | I2C12SCL\_GPIO | I2C12SCL | GPIO | BI | **I2C/SMBUS 12 clock** | GPIO |
| I2C | I2C12SDA\_GPIO | I2C12SDA | GPIO | BI | **I2C/SMBUS 12 data** | GPIO |
| I2C | I2C1SCL\_GPIO | I2C1SCL | GPIO | BI | **I2C/SMBUS 1 clock** | GPIO |
| I2C | I2C1SDA\_GPIO | I2C1SDA | GPIO | BI | **I2C/SMBUS 1 data** | GPIO |
| I2C | I2C2SCL\_GPIO | I2C2SCL | GPIO | BI | **I2C/SMBUS 2 clock** | GPIO |
| I2C | I2C2SDA\_GPIO | I2C2SDA | GPIO | BI | **I2C/SMBUS 2 data** | GPIO |
| I2C | I2C3SCL\_GPIO | I2C3SCL | GPIO | BI | **I2C/SMBUS 3 clock** | GPIO |
| I2C | I2C3SDA\_GPIO | I2C3SDA | GPIO | BI | **I2C/SMBUS 3 data** | GPIO |
| I2C | I2C4SCL\_GPIO | I2C4SCL | GPIO | BI | **I2C/SMBUS 4 clock** | GPIO |
| I2C | I2C4SDA\_GPIO | I2C4SDA | GPIO | BI | **I2C/SMBUS 4 data** | GPIO |
| I2C | I2C5SCL\_GPIO | I2C5SCL | GPIO | BI | **I2C/SMBUS 5 clock** | GPIO |
| I2C | I2C5SDA\_GPIO | I2C5SDA | GPIO | BI | **I2C/SMBUS 5 data** | GPIO |
| I2C | I2C6SCL\_GPIO | I2C6SCL | GPIO | BI | **I2C/SMBUS 6 clock** | GPIO |
| I2C | I2C6SDA\_GPIO | I2C6SDA | GPIO | BI | **I2C/SMBUS 6 data** | GPIO |
| I2C | I2C7SCL\_GPIO | I2C7SCL | GPIO | BI | **I2C/SMBUS 7 clock** | GPIO |
| I2C | I2C7SDA\_GPIO | I2C7SDA | GPIO | BI | **I2C/SMBUS 7 data** | GPIO |
| I2C | I2C8SCL\_GPIO | I2C8SCL | GPIO | BI | **I2C/SMBUS 8 clock** | GPIO |
| I2C | I2C8SDA\_GPIO | I2C8SDA | GPIO | BI | **I2C/SMBUS 8 data** | GPIO |
| I2C | I2C9SCL\_GPIO | I2C9SCL | GPIO | BI | **I2C/SMBUS 9 clock** | GPIO |
| I2C | I2C9SDA\_GPIO | I2C9SDA | GPIO | BI | **I2C/SMBUS 9 data** | GPIO |
| I2C | I2C13SCL | I2C13SCL |  | BI | **I2C/SMBUS 13 clock** |  |
| I2C | I2C13SDA | I2C13SDA |  | BI | **I2C/SMBUS 13 data** |  |
| I2C | GPIO\_I2C14SCL | GPIO | I2C14SCL | BI | **GPIO** | **I2C/SMBUS 14 clock** |
| I2C | GPIO\_I2C14SDA | GPIO | I2C14SDA | BI | **GPIO** | **I2C/SMBUS 14 data** |
| I2C | GPIO\_I2C15SCL | GPIO | I2C15SCL | BI | **GPIO** | **I2C/SMBUS 15 clock** |
| I2C | GPIO\_I2C15SDA | GPIO | I2C15SDA | BI | **GPIO** | **I2C/SMBUS 15 data** |
| I2C | GPIO\_I2C16SCL | GPIO | I2C16SCL | BI | **GPIO** | **I2C/SMBUS 16 clock** |
| I2C | GPIO\_I2C16SDA | GPIO | I2C16SDA | BI | **GPIO** | **I2C/SMBUS 16 data** |
| INDICATOR | GPIO\_INDICATOR | GPIO | INDICATOR | BI | Boot indication from BMC / GPIO option | GPIO |
| JTAG | JTAG1RTCK | JTAG1RTCK |  | INPUT | JTAG Return Test Clock Input |  |
| JTAG | JTAG1TCK | JTAG1TCK |  | OUTPUT | JTAG Master Clock Output |  |
| JTAG | JTAG1TDI | JTAG1TDI |  | OUTPUT | JTAG Master Data Output |  |
| JTAG | JTAG1TDO | JTAG1TDO |  | INPUT | JTAG Master Data Input |  |
| JTAG | JTAG1TMS | JTAG1TMS |  | OUTPUT | JTAG Master Mode Select Output |  |
| JTAG | JTAG1TRST | JTAG1TRST |  | OUTPUT | JTAG Test Reset Output |  |
| LPC/eSPI | LPCCLK\_ESPICLK | LPCCLK | ESPICLK | INPUT | LPC bus clock input (default) | eSPI clock input |
| LPC/eSPI | LPCD0\_ESPID0 | LPCD0 | ESPID0 | BI | LPC address and data bus bit 0 | eSPI data bus bit 0 |
| LPC/eSPI | LPCD1\_ESPID1 | LPCD1 | ESPID1 | BI | LPC address and data bus bit 1 | eSPI data bus bit 1 |
| LPC/eSPI | LPCD2\_ESPID2 | LPCD2 | ESPID2 | BI | LPC address and data bus bit 2 | eSPI data bus bit 2 |
| LPC/eSPI | LPCD3\_ESPID3 | LPCD3 | ESPID3 | BI | LPC address and data bus bit 3 | eSPI data bus bit 3 |
| LPC/eSPI | LPCFRAME#\_ESPICS# | LPCFRAME# | ESPICS# | INPUT | LPC FRAME# (default) | eSPI chip select input |
| LPC/eSPI | LPCIRQ#\_ESPIALERT# | LPCIRQ# | ESPIALERT# | BI | LPC serial IRQ (default) | eSPI Alert |
| LPC/eSPI | LPCRST#\_ESPIRST# | LPCRST# | ESPIRST# | INPUT | LPC reset input (default) | eSPI reset input |
| PCIE | PEREFCLKN | PEREFCLKN |  | INPUT | PCI Express Reference clock input, 100MHz negative input of the differential clock pair | none |
| PCIE | PEREFCLKP | PEREFCLKP |  | INPUT | PCI Express Reference clock input, 100MHz positive input of the differential clock pair | none |
| PCIE | PERSTN | PERSTN |  | OUTPUT | PCI Express reset pin This reset signal reset PCI Express bus controller and VGA/2D device. | none |
| PCIE | PERXN | PERXN |  | INPUT | PCI Express Serial Data Receiver It receives negative input of the differential signal pair. | none |
| PCIE | PERXP | PERXP |  | INPUT | PCI Express Serial Data Receiver It receives positive input of the differential signal pair. | none |
| PCIE | PETXN | PETXN |  | OUTPUT | PCI Express Serial Data Transmitter It transmits negative output of the differential signal pa | none |
| PCIE | PETXP | PETXP |  | OUTPUT | PCI Express Serial Data Transmitter It transmits positive output of the differential signal pair. | none |
| PECI | PECI | PECI |  | INPUT | PECI signal input/output to BMC | none |
| PECI | PECIVDD | PECIVDD |  | INPUT | PECI power | none |
| PWM/GPIO | PWM0\_GPIO | PWM0 | GPIO | BI | PWM output | GPIO |
| PWM/GPIO | PWM1\_GPIO | PWM1 | GPIO | BI | PWM output | GPIO |
| PWM/GPIO | PWM2\_GPIO | PWM2 | GPIO | BI | PWM output | GPIO |
| PWM/GPIO | PWM3\_GPIO | PWM3 | GPIO | BI | PWM output | GPIO |
| PWM/GPIO | PWM4\_GPIO | PWM4 | GPIO | BI | PWM output | GPIO |
| PWM/GPIO | PWM5\_GPIO | PWM5 | GPIO | BI | PWM output | GPIO |
| PWM/GPIO | PWM6\_GPIO | PWM6 | GPIO | BI | PWM output | GPIO |
| PWM/GPIO | PWM7\_GPIO | PWM7 | GPIO | BI | PWM output | GPIO |
| RESET | BMC\_RESET# | BMC\_RESET# |  | INPUT | Core Reset circuitry for SOC and any periphery components needed for reset |  |
| RESET | PWRGD | PWRGD |  | INPUT | power Good from power supply |  |
| RFU | KLUDGE\_GPIO | KLUDGE | GPIO | BI | Kludge pins | **GPIO** |
| RFU | KLUDGE\_GPIO | KLUDGE | GPIO | BI | Kludge pins | **GPIO** |
| RMII | RMIICRSDV | RMIICRSDV |  | INPUT | RMII/NCSI 1 receive carrier sense and data valid |  |
| RMII | RMIIMDC | RMIIMDC |  | OUTPUT | Management Data Clock. The MDC clock input must be provided to allow MII management functions. |  |
| RMII | RMIIMDIO | RMIIMDIO |  | BI | Management Data I/O. This serial input/output bit is used to read from and write to the MII registers |  |
| RMII | RMIIRCLKI | RMIIRCLKI |  | INPUT | RMII/NCSI 1 50MHz reference clock input |  |
| RMII | RMIIRXD0 | RMIIRXD0 |  | INPUT | RMII/NCSI 1 receive data bus from PHY bit 0 |  |
| RMII | RMIIRXD1 | RMIIRXD1 |  | INPUT | RMII/NCSI 1 receive data bus from PHY bit 1 |  |
| RMII | RMIIRXER | RMIIRXER |  | INPUT | RMII/NCSI 1 receive data error |  |
| RMII | RMIITXD0 | RMIITXD0 |  | OUTPUT | RMII/NCSI 1 transmit data bus to PHY bit 0 |  |
| RMII | RMIITXD1 | RMIITXD1 |  | OUTPUT | RMII/NCSI 1 transmit data bus to PHY bit 1 |  |
| RMII | RMIITXEN | RMIITXEN |  | OUTPUT | RMII/NCSI 1 transmit enable |  |
| SGPIO/GPIO | GPIO\_SGPMCK | GPIO | SGPMCK | OUTPUT | GPIO | Master Serial GPIO clock output |
| SGPIO/GPIO | GPIO\_SGPMI | GPIO | SGPMI | INPUT | GPIO | Master Serial GPIO serial data input |
| SGPIO/GPIO | GPIO\_SGPMLD | GPIO | SGPMLD | OUTPUT | GPIO | Master Serial GPIO serial data load output |
| SGPIO/GPIO | GPIO\_SGPMO | GPIO | SGPMO | OUTPUT | GPIO | Master Serial GPIO serial data output |
| SPI/GPIO | SPI1MISO\_IO1\_GPO | SPI1MISO\_IO1 | GPO | BI | SPI 1 MISO/IO1 | GPO |
| SPI/GPIO | SPI1MOSI\_IO0\_GPO | SPI1MOSI\_IO0 | GPO | BI | SPI 1 MOSI/IO0 | GPO |
| SPI/GPIO | SPI1CK\_GPIO | SPI1CK | GPIO | BI | SPI 1 clock output | GPIO |
| SPI/GPIO | SPI1CS0#\_GPIO | SPI1CS0# | GPIO | BI | SPI 1 chip select 0 | GPIO |
| SPI/GPIO | SPI1CS1#\_GPIO | SPI1CS1# | GPIO | BI | SPI 1 chip select 1 | GPIO |
| SPI/GPIO | GPO\_SPI1\_IO2 | GPO | SPI1\_IO2 | BI | GPO | SPI1 IO2 to support quad |
| SPI/GPIO | GPIO\_SPI1\_IO3 | GPIO | SPI1\_IO3 | BI | GPIO | SPI1 IO3 to support quad |
| SPI/GPIO | SPI2CK\_GPIO | SPI2CK | GPIO | BI | SPI 2 clock output | GPIO |
| SPI/GPIO | SPI2CS0#\_GPIO | SPI2CS0# | GPIO | BI | SPI 2 chip select 0 | GPIO |
| SPI/GPIO | SPI2CS1#\_GPIO | SPI2CS1# | GPIO | BI | SPI 2 chip select 1 | GPIO |
| SPI/GPIO | SPI2MISO\_GPIO | SPI2MISO | GPIO | BI | SPI 2 MISO | GPIO |
| SPI/GPIO | SPI2MOSI\_GPIO | SPI2MOSI | GPIO | BI | SPI 2 MOSI | GPIO |
| SPI/GPIO | SYSCS#\_GPIO | SYSCS# | GPIO | BI | System SPI Chip Select input | GPIO |
| SPI/GPIO | SYSMISO\_GPO | SYSMISO | GPO | BI | System SPI MOSI | GPO |
| SPI/GPIO | SYSMOSI\_GPO | SYSMOSI | GPO | BI | System SPI MISO | GPO |
| SPI/GPIO | SYSCK\_GPIO | SYSCK | GPIO | BI | System SPI Clock input | GPIO |
| TACH/GPIO | TACH0\_GPIO | TACH0 | GPIO | BI | Fan Tachometer input | GPIO |
| TACH/GPIO | TACH1\_GPIO | TACH1 | GPIO | BI | Fan Tachometer input | GPIO |
| TACH/GPIO | TACH10\_GPIO | TACH10 | GPIO | BI | Fan Tachometer input | GPIO |
| TACH/GPIO | TACH11\_GPIO | TACH11 | GPIO | BI | Fan Tachometer input | GPIO |
| TACH/GPIO | TACH12\_GPIO | TACH12 | GPIO | BI | Fan Tachometer input | GPIO |
| TACH/GPIO | TACH13\_GPIO | TACH13 | GPIO | BI | Fan Tachometer input | GPIO |
| TACH/GPIO | TACH14\_GPIO | TACH14 | GPIO | BI | Fan Tachometer input | GPIO |
| TACH/GPIO | TACH15\_GPIO | TACH15 | GPIO | BI | Fan Tachometer input | GPIO |
| TACH/GPIO | TACH2\_GPIO | TACH2 | GPIO | BI | Fan Tachometer input | GPIO |
| TACH/GPIO | TACH3\_GPIO | TACH3 | GPIO | BI | Fan Tachometer input | GPIO |
| TACH/GPIO | TACH4\_GPIO | TACH4 | GPIO | BI | Fan Tachometer input | GPIO |
| TACH/GPIO | TACH5\_GPIO | TACH5 | GPIO | BI | Fan Tachometer input | GPIO |
| TACH/GPIO | TACH6\_GPIO | TACH6 | GPIO | BI | Fan Tachometer input | GPIO |
| TACH/GPIO | TACH7\_GPIO | TACH7 | GPIO | BI | Fan Tachometer input | GPIO |
| TACH/GPIO | TACH8\_GPIO | TACH8 | GPIO | BI | Fan Tachometer input | GPIO |
| TACH/GPIO | TACH9\_GPIO | TACH9 | GPIO | BI | Fan Tachometer input | GPIO |
| UART | CONSOLETX\_GPIO | CONSOLETX | GPIO | BI | Transmit serial data output, primary console |  |
| UART | CONSOLERX\_GPIO | CONSOLERX | GPIO | BI | Receive serial data input, primary console |  |
| UART | UART1TX\_GPIO | UART1TX | GPIO | BI | Transmit serial data output |  |
| UART | UART1RX\_GPIO | UART1RX | GPIO | BI | Receive serial data input |  |
| UART | UART2TX\_GPIO | UART2TX | GPIO | BI | Transmit serial data output |  |
| UART | UART2RX\_GPIO | UART2RX | GPIO | BI | Receive serial data input |  |
| UART | GPIO\_UART3TX | GPIO | UART3TX | BI | Transmit serial data output |  |
| UART | GPIO\_UART3RX | GPIO | UART3RX | BI | Receive serial data input |  |
| UART | GPIO\_UART4TX | GPIO | UART4TX | BI | Transmit serial data output |  |
| UART | GPIO\_UART4RX | GPIO | UART4RX | BI | Receive serial data input |  |
| USB | USB2A\_HD\_DN | USB2A\_HD\_DN |  | BI | D− signal of USB 2.0 port A, USB host |  |
| USB | USB2A\_HD\_DP | USB2A\_HD\_DP |  | BI | D+ signal of USB 2.0 port A, USB host |  |
| USB | GPIO\_USB2AVBUSOVC | GPIO | USB2AVBUSOVC | BI | Host/device Overcurrent sense | GPIO |
| USB | GPIO\_USB2AVBUSC | GPIO | USB2AVBUSC | BI | Host/device VBUS Control | GPIO |
| USB | USB2B\_D\_DN | USB2B\_D\_DN |  | BI | D− signal of USB 2.0 port B, device |  |
| USB | USB2B\_D\_DP | USB2B\_D\_DP |  | BI | D+ signal of USB 2.0 port B, device |  |
| USB | GPIO\_USB2BVBUSSNS | GPIO | USB2BVBUSSNS | BI | Device VBUS Sense | GPIO |
| VGA | DACB | DACB |  | OUTPUT | DAC B channel output |  |
| VGA | DACG | DACG |  | OUTPUT | DAC G channel output |  |
| VGA | DACR | DACR |  | OUTPUT | DAC R channel output |  |
| VGA | DDCCLK\_GPIO | DDCCLK | GPIO | BI | VGA DDC clock pin | GPIO |
| VGA | DDCDAT\_GPIO | DDCDAT | GPIO | BI | VGA DDC data pin | GPIO |
| VGA | VGAHS\_GPIO | VGAHS | GPIO | BI | VGA horizontal sync output | GPIO |
| VGA | VGAVS\_GPIO | VGAVS | GPIO | BI | VGA vertical sync output | GPIO |
| WATCHDOG/GPIO | WDTRST1\_GPIO | WDTRST1 | GPIO | OUTPUT | Watchdog timer 1 pulse output | GPIO |
| WATCHDOG/GPIO | WDTRST2\_GPIO | WDTRST2 | GPIO | OUTPUT | Watchdog timer 2 pulse output | GPIO |

# Electrical and Timing Requirements

## Electrical Requirements

|  |  |  |
| --- | --- | --- |
| **DC Electrical Requirements** | **Requirement** | **Notes** |
| Current carrying capability at 30 °C temperature rise per contact | 0.50 amp/pin De-rated | Electrical Requirements shall meet PS-003A-01 JEDEC specification |

|  |  |  |  |
| --- | --- | --- | --- |
| **Power and Ground Requirements** | **Pin Count** | **Description** | **Maximum Current/Power** |
| VDD\_12V\_STBY | 1 | +12V main or +12v aux | 0.5amps/6watts |
| VDD3\_3V\_STBY | 5 | +3.3V main or +3.3 aux | 2.5amps/8.25watts |
| GND | 38 | Ground Return |  |

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Requirements** | **Description** | **Notes** | **Typical** |
| I2C | I2C serial data (SDA) and serial clock (SCL) signals. | Pullups should be placed on System Board. | 3.3V |
| RGB |  |  |  |
| TACH | Fan Tachometer Controller | Tachometer Input | 3.3V |
| PWM | Pulse Width Modulation | Output | 3.3V, 8mA drive strength |
| RGMII | Reduced Gigabit Media Independent Interface | If lower voltages are desired (ex: 1.8v), the runBMC daughterboard must translate to 3.3V | 3.3V |
| ADC | Analog to Digital Converter | Inputs are reference to 1.8v (ADC0-15) | 1.8V |
| ESPI or LPC | Enhanced Serial Peripheral Interface Bus or Low Pin Count Interface | Voltage is selectable by VDD\_LPC3V3\_ESPI1V8 voltage pin. | 3.3V or 1.8V |
| VDD\_IO\_REF | Voltage reference output | For scenarios where BMC’s have different voltage IO requirements. This signal can be referenced on the MB for 1v8 or 3v3 I/O references. See figure 6.1 for an example. | Up to designer. |

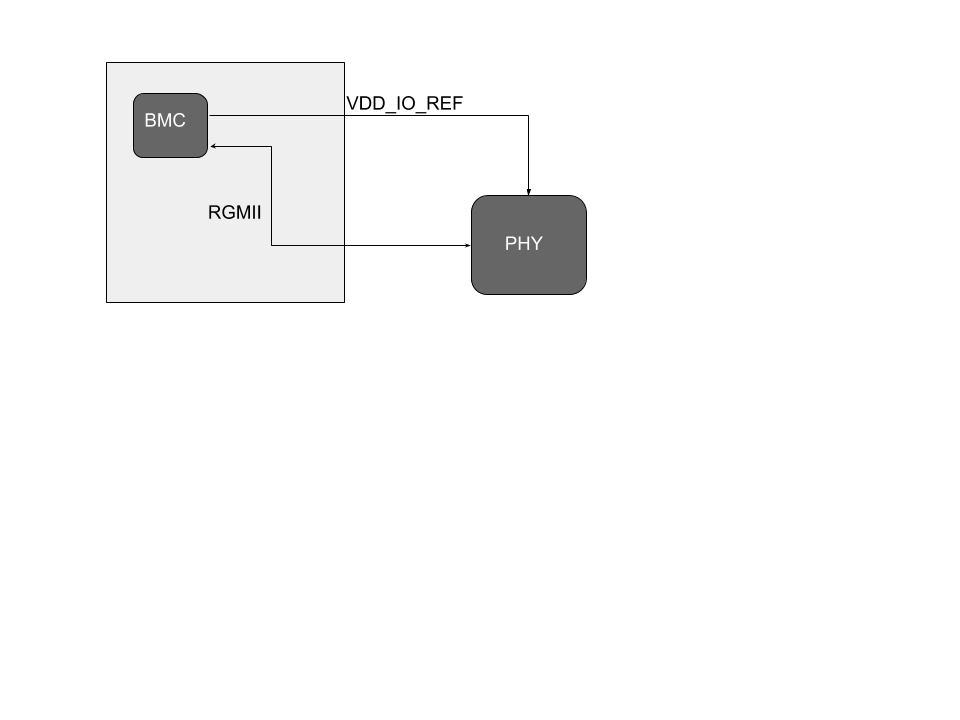


Figure 6‑1

Figure 6-1 is an example of VDD\_IO\_REF driving a voltage reference pin in the case where the BMC vendor has specific RGMII voltage requirements. For example, 1v8 HSTL vs 3v3 TTL.

## Timing Requirements

[To ask in next OCP Server Talk]: Should we include skew, stackup, material, etc requirements.

|  |  |  |
| --- | --- | --- |
| **Skew Requirements** | **Requirement** | **Notes** |
| PCIe |  |  |
| USB |  |  |
| 1GbT |  |  |
| RGMII |  |  |
| VGA |  |  |
| RMII/NC-SI |  |  |
| LPC |  |  |
| SPI |  |  |

# Mechanical

## Form Factor

Below is a table of EIA vs OU (OCP) mounting increments.

|  |  |  |
| --- | --- | --- |
|  | EIA | OCP |
| Increment Naming | RU | OU |
| Mounting Increments | EIA RU = 1.75", 44.45mm | OU=1.88", 45.72mm |
| Mounting Increments (mm) | 44.45 | 45.72 |

The BMC module shall conform to the 260 Pin DDR4 SODIMM, .50mm Pitch DIMM Registration form factor, defined by MO-310C, with the exception of the height and component height keepout requirements. The module has a 260 pin edge connector. Refer to JEDEC spec for dimensions and tolerances. The following heights are supported per below table.

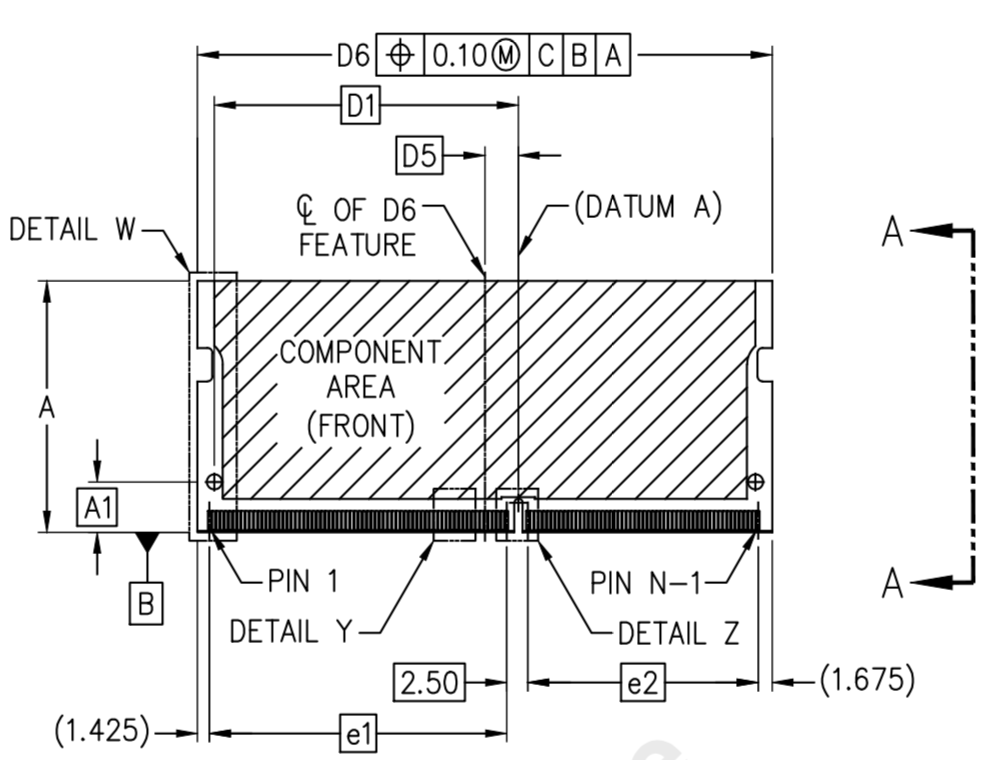


Figure 7‑1

Figure 7-1 outlines the SO-DIMM DDR4 JEDEC registration. RunBMC will follow this registration, with the exceptions to the “A” height. The below table shows the permissible A heights.

|  |  |
| --- | --- |
| Card Types | “A” height denoted in Figure 7-1 |
| Standard | 32mm |
| Large | 50mm |

## Component Height Keep-out Requirements

Reference boards should have major components on the top side of the PCB, referenced by E1 in Figure 7-3 below. Smaller components with low height can be placed on the bottom, E2.

When placed in a right-angle configuration, E1 will face towards the top of the compute or network platform.

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  |  | | --- | --- | --- | | Dimension for Figure 7-3 | mm | Notes | | E1 (top) | 5.44mm | Right Angle config this is the top of the PCB | | E (pcb thickness) | 1.2mm |  | | E2 (bottom) | 1.6mm | Right Angle config this is the bottom of the PCB |     Figure 7‑2 BMC Thickness |

The below figure demonstrates a right angle SO-DIMM connector of 8mm height.

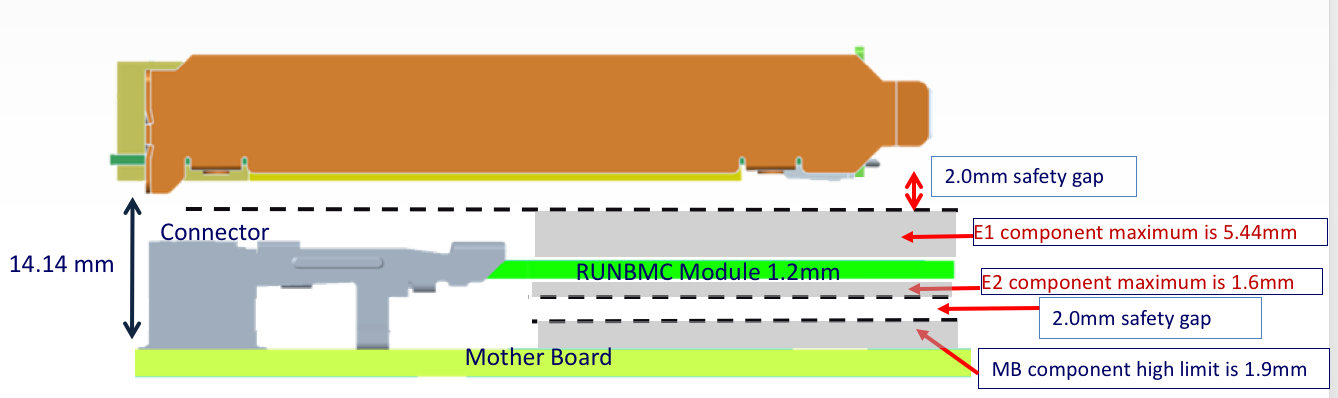


Figure 7‑3

## RU/OU Mounting Options

* System Height = 1OU/1RU:
  + *Standard* vertical card supported.
  + Right-angle for *Standard* or *Large* supported.
* System Height > 1OU/1RU:
  + *Standard* and *Large* supported in vertical or right-angle.

## Mating Connector

The BMC mating connector shall conform to the DDR4 Small Outline Dual Inline Memory Module (SODIMM), 260 pin, 0.50 mm pitch Socket Outline, defined by SO-018D.

A conforming vertical connector, Amphenol G634B2610X22HR, or equivalent can be mounted on the motherboard or network device, to mate with the BMC module edge connector. Right Angle or Angled connectors are permissible if conformant to SO-18D specification.

# Thermal

The BMC mezzanine card can be located in any position of the server or network motherboard. The worst-case environmental conditions can be expected to be (Shobe TO FILL OUT). The thermal solution, component selections, and design should consider for these conditions.

TBD CHART to show Operating Conditions

# FRU Requirements

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| FRU Requirements | Description | Location | I2C BUS | I2C address |
| I2C Identification EEPROM | EEPROM used for FRU data, logging, system purposes, etc | runBMC | 13 | 0XA2, 8bit |
| I2C Personality EEPROM | EEPROM used by SOC to define personality of system | System Board | 4 | 0xA0, 8bit |

# Platform Guidelines

* BMC programmers should be advised to create an abstraction layer. This layer will help map the runBMC connector pinout to SOC pins specific to the vendor module.
* VDD\_IO\_REF is intended to be used as a reference voltage, which is provided by the runBMC module.
  + Scenario 1: RGMII from vendorA expects 1.8v and vendorB expects 3.3v. Some PHYs allows you to set different voltages based on an IO voltage reference.
  + Scenario 2: I2C bidirectional voltage translators typically utilize a VREF pin to allow voltage level translation.

# References

* Registration - 260 Pin DDR4 SODIMM, 0.50 mm Pitch. DIMM; M0-310C, Item No. 11-14-164
* Registration - DDR4 Small Outline Dual Inline Memory Module (SODIMM), 260 pin, 0.50 mm pitch Socket Outline; SO-018D, Item No. 14-180
* NXP Semiconductors. *I2C-bus specification and user manual.* NXP Semiconductors, Rev 6, April 4th, 2014.

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