Q-WAVE INC

WEDGE 100C CPLD REGISTER DOCUMENT

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	Initials	Sign & Date
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REVISION HISTORY

Revision Number	Date	Change Description	Author(s)
0.1	Mar 01, 2016	First Draft	

"Q-Wave Inc"

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3. Registers Description

3.1 Register List

The Register list of the Wedge100C is as shown in below.

Note: The column "Reset Condition" is the reset source which resets the register to default value. Where Cold reset and warm reset are based on several Reset sources as explained in the Reset Chapter, while power on reset is the internally generated reset after board powers on. This reset is not dependent on any reset source.

Table 1: Registers List

Sl. No	Registers	Access	Reset condition	Width	Addr Offset
1.	3.2.1 Board Identifier Register	R	N/A	8	0x00
2.	3.2.2 CPLD Code Revision Register	R	N/A	8	0x01
3.	3.2.3 CPLD Code Sub-Revision Register	R	N/A	8	0x02
4.	3.2.4 Slot Information Register	R	N/A	8	0x03
5.	3.2.5 QSFP Status LED Position Status Register	R	N/A	8	0x04
6.	UART unused signal status register	R	N/A	8	0x05
7.	BMC Heart status register	R	N/A	8	0x06
8.	-	R	N/A	8	0x07
9.	3.2.8 Card Present Status register	R	N/A	8	0x08
10.	-	R	N/A	8	0x09
11.	-	R	N/A	8	0x0A
12.	-	R	N/A	8	0x0B
13.	-	R	N/A	8	0x0C
14.	3.2.9 Reset Reason Register	R	N/A	8	0x0D
15.	Reset Status Register-1	R	N/A	8	0x0E
16.	3.2.11 Reset Status Register-2	R	N/A	8	0x0F
17.	PSU Status Register	R	N/A	8	0x10
18.	3.2.13 On Board Power Status Register-1	R	N/A	8	0x11
19.	3.2.14 On Board Power Status Register-2	R	N/A	8	0x12

Sl. No	Registers	Access	Reset condition	Width	Addr Offset
20.	I2C PCA9535 interrupt status Register	R	N/A	8	0x13
21.	3.2.16 Alert Status Register	R	N/A	8	0x14
22.	Internal Interrupt status Register	R	N/A	8	0x15
23.	-	R	N/A	8	0x16
24.	-	R	N/A	8	0x17
25.	-	R	N/A	8	0x18
26.	-	R	N/A	8	0x19
27.	-	R	N/A	8	0x1A
28.	Top and Bottom selection register	R	N/A	8	0x1B
29.	-	R	N/A	8	0x1C
30.	-	R	N/A	8	0x1d
31.	-	R	N/A	8	0x1e
32.	3.2.19 GPIO CP2112 Input Register	R	N/A	8	0x1f
33.	Interrupt Block Register: PSU	RW	warm_reset_n	8	0x20
34.	3.2.21 Interrupt Block Register: Power OK	RW	warm_reset_n	8	0x21
35.	3.2.22 Interrupt Block Register: Power Ready, Hot	RW	warm_reset_n	8	0x22
36.	Interrupt Block Register: PCA9535	RW	warm_reset_n	8	0x23
37.	3.2.24 Interrupt Block Register: Alert	RW	warm_reset_n	8	0x24
38.	3.2.25 Interrupt Block Register: Global Interrupt	RW	warm_reset_n	8	0x25
39.	UART Mux Control Register	RW	warm_reset_n	8	0x26
40.	-	RW	warm_reset_n	8	0x27
41.	-	RW	warm_reset_n	8	0x28
42.	-	RW	warm_reset_n	8	0x29
43.	-	RW	warm_reset_n	8	0x2A
44.	-	RW	warm_reset_n	8	0x2B
45.	3.2.27 CP2112 Direction Register	RW	warm_reset_n	8	0x2C
46.	3.2.28 CP2112 Output Data Register	RW	warm_reset_n	8	0x2D

Sl. No	Registers	Access	Reset condition	Width	Addr Offset
47.	-	RW	warm_reset_n	8	0x2E
48.	Miscellaneous Register	RW	power_on_reset_n	8	0x2F
49.	3.2.30 Power Control Register	RW	power_on_reset_n	8	0x30
50.	3.2.31 Reset Request Register	RW	cold_reset_n	8	0x31
51.	Reset Control Register-1	RW	warm_reset_n	8	0x32
52.	-	RW	N/A	8	0x33
53.	3.2.33 QSFP Reset Register-1	RW	warm_reset_n	8	0x34
54.	3.2.34 QSFP Reset Register-2	RW	warm_reset_n	8	0x35
55.	QSFP Reset Register-3	RW	warm_reset_n	8	0x36
56.	3.2.36 QSFP Reset Register-4	RW	warm_reset_n	8	0x37
57.	3.2.37 I2C Mux Reset Register	RW	warm_reset_n	8	0x38
58.	3.2.38 Reset Control Register-2	RW	warm_reset_n	8	0x39
59.	3.2.39 Reset Enable register-1	RW	power_on_reset_n	8	0x3A
60.	3.2.40 Reset Enable Register-2	RW	warm_reset_n	8	0x3B
61.	LED-0 control Register	RW	warm_reset_n	8	0x3C
62.	3.2.42 LED-1 control Register	RW	warm_reset_n	8	0x3D
63.	3.2.43 Stream LED Control Register-1	RW	warm_reset_n	8	0x3E
64.	Stream LED Control Register-2	RW	warm_reset_n	8	0x3F
65.	3.2.45 MISC Interrupt status register	R	N/A	8	0x40
66.	3.2.46 MISC Interrupt enable register	R/W	N/A	8	0x41
67.	GPIO read register	R	N/A	8	0x42
68.	3.2.48 PLL_CLOCK_LOCK status register	R	N/A	8	0x43
69.	3.2.49 CLK_PLL_RESET register	R/W	N/A	8	0x44
70.	GPIO write register	R/W	N/A	8	0x45
71.	Speed selection register	R/W	N/A	8	0x46

3.2 Register Description

3.2.1 Board Identifier Register

Table 2: Board Identifier Register

Board Identifier Register		**Address Offset=0x00**			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:6]	-	R	2	'b00	Reserved
[5:4]	model_id	R	2	'b00	Model Identifier 2'b00 : wedge100 2'b01 : 6-pack100 Line card 2'b10 : 6-pack100 Fabric card 2'b11 : Unused * ***These bits are hard-coded to 2'b00***
[3:0]	board_rev	R	4	'b0xxx	Board Revision Number **** These bits are updated by 3 input pins BOARD_REV_IDn (n=2,1,0)*** ***(external resister strapping)***

3.2.2 CPLD Code Revision Register

Table 31: CPLD Code Revision Register

CPLD Code Revision Register		**Address Offset=0x01**			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7]	-	R	1	'b0	Reserved
[6]	release_bit	R	1	'b0	Release Bit * ***This bit is hard-coded to 1'b0***
[5:0]	revision	R	6	'b1	CPLD Code Revision Number for Wedge100 *** 6 LSB bits of parameter *cpld_revision* are assigned to**

CPLD Code Revision Register		Address Offset=0x01			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
					these bits where parameter *cpld_revision* is assigned a value 8'd1.

3.2.3 CPLD Code Sub-Revision Register

Table 4: CPLD Code Sub- Revision Register

CPLD Code Revision Register		Address Offset=0x02			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:0]	CPLD Code Sub-Revision Number	R	8	'h05	Code Sub-Revision Number. This is used to keep track of all changes made. * ***These bits are hard-coded to 8'd05***

3.2.4 Slot Information Register

Table 5: Slot Information Register

Slot Information Register		Address Offset=0x03			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:0]	Slot Information Register	R	8	'h10	This Register defines the Slot Information as listed below. These are reserved for 6-pack100 design 8'd00: line card slot-1 8'd01: line card slot-2 8'd02: line card slot-3 8'd03: line card slot-4 8'd04: line card slot-5

Slot Information Register		Address Offset=0x03			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
					8'd05: line card slot-6 8'd06: line card slot-7 8'd07: line card slot-8 8'd08:fabric card slot-1,Block-0 8'd09:fabric card slot-1,Block-1 8'd0a:fabric card slot-2,Block-0 8'd0b:fabric card slot-2,Block-1 8'd10:reserved for TOR others: Not defined yet * ***These bits are hard-coded to 8'd10***

3.2.5 QSFP Status LED Position Status Register

Table 62: QSFP Status LED Position Status register

QSFP Status LED Position Status register		Address Offset=0x04			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:6]	-	R	7	'hx	Reserved
[0]	CPLD_QSFP_LED_POSITION	R	1	'bx	CPLD QSFP LED position status indication. **** This bit is updated directly by input pin CPLD_QSFP_LED_POSITION***

3.2.6 UART unused signal status register

Table 7: UART unused signal status register

UART unused signal status register		Address Offset=0x05			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:3]	-	R	6	'h0	Reserved
[1]	DEBUG_UART_SEL_N	R	1	'bx	Debug UART Select status. **** This bit is updated directly by input pin DEBUG_UART_SEL_N***
[0]	BMC UART-1 RTS status	R	1	'bx	BMC UART-1 RTS status indication. **** This bit is updated directly by input pin BMC_UART_1_RTS***

3.2.7 BMC Heart status register

Table 8: BMC Heart status register

BMC Heart status register		Address Offset=0x06			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:3]	-	R	7	'h0	Reserved
[0]	BMC_HEARTBEAT_N	R	1	'bx	BMC power good signal **** This bit is updated directly by input pin BMC_HEARTBEAT_N***

3.2.8 Card Present Status register

Table 9: Card Present status register

Card Present status register		Address Offset=0x08			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:4]	-	R	4	'hx	Reserved
[3]	MICROSRV_PRSNT_N	R	1	'bx	Microserver present signal **** This bit is updated directly by input pin MICROSRV_PRSNT_N***
[2]	CARD_PRNT_N	R	1	'bx	Rackmon card present signal **** This bit is updated directly by input pin CARD_PRNT_N***
[1]	PSU2_PRSNT_N	R	1	'bx	PSU-2 Present Signal **** This bit is updated directly by input pin PSU2_PRSNT_N.***
[0]	PSU1_PRSNT_N	R	1	'bx	PSU-1 Present Signal **** This bit is updated directly by input pin PSU1_PRSNT_N.***

3.2.9 Reset Reason Register

Table 10: Reset Reason Register

Reset Reason Register		Address Offset=0x0D			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:0]	Reset Reason Register	R	8	'hxx	Reset Reason Register : This register describes the reason for the occurred reset. Each value on the register corresponds to specific resets. The value of this register is determined by the values of

<table>
<tr><td colspan="2">Reset Reason Register</td><td colspan="4">Address Offset=0x0D</td></tr>
<tr><td>Bit</td><td>Bit Name</td><td>Access</td><td>Width</td><td>Default Value</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>reset status registers (offset – 0x0e 0x0f) and Sources of Resets (External and software resets(offset -0x31)).

The below values are only updated when system_reset_n_edge (positive edge) occurs, i.e system reset terminates (any of cold, warm and hot reset terminates) and when the corresponding resets occur.
Note: the below one describes how to understand the register
say eg: 8'h01 : will be updated only when system reset is not there, and PD_STBY_RESET_N occurs.
say eg: 8'h10 : will be updated only when system reset is not there, and rw_0x31[4] is asserted for hot reset request occurs.

Note: The priority of resets is as below.
<table><tr><th>Val</th><th>Reset Cause</th></tr><tr><td>8'h01</td><td>PD_STBY_RESET_N</td></tr><tr><td>8'h02</td><td>PD_MAIN_RESET_N de-asserted when PD_STBY_RESET_N is not terminated</td></tr><tr><td>8'h03</td><td>PUSHBUTTON_RST_N</td></tr></table></td></tr>
</table>

Reset Reason Register		Address Offset=0x0D			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
					8'h04 CPLD_PUSH_BTN_RST_IN_N 8'h05 DEBUG_RST_BTN_N 8'h10 rw_0x31[4] - hot reset request 8'h11 rw_0x31[4] - hot reset request 8'h12 rw_0x31[4] - hot reset request 8'h13 rw_0x31[4] - hot reset request 8'h20 BMC_MAIN_RESET_N 8'h21 BMC_CPLD_RESET1 8'h22 BMC_CPLD_RESET2 8'h23 LS_BMC_CPLD_RESET3 8'h24 LS_BMC_CPLD_RESET4 8'h25 LS_BMC_WDTRST1 8'h26 LS_BMC_WDTRST2 **others: not defined yet**

Note1: System reset- de-assertion is determined if hot, warm or cold reset is de-asserted.

Note2: The resets mentioned in the descriptions in 0x0E and 0x0F are active low namely,

- *hot reset, warm reset, cold reset, system reset*
- *watchdog timer reset*
- *warm push button reset, cold push button reset*
- *BMC warm reset, BMC cold reset*
- *FB debug reset,*

- *PD main reset, PD standby reset*
- *rst_all_warm, rst_all_cold*

Hence,

- *Asserted indicates that these signals are made low.*
- *De-asserted indicates that these signals are made high.*

3.2.10 Reset Status Register-1

Table 11: Reset Status Register-1

Reset Status Register-1		**Address Offset=0x0E**			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[0]	pb_reset_neg_pul_active	R	1	'bx	Reset status register -1 Each bit consists of status of reset signals (external or Software controlled) When the bit value is set to '1', it indicates that the reset has been asserted, provided cold (reset_cold_n) and warm (reset_warm_n) resets are not there. The register value will be updated on every system reset de-assertion. When appropriate reset occurs its corresponding bit will be set to 1 as mentioned below and all other bits of the registers will be cleared. [0] push button reset pulse :PUSHBUTTON_RST_N [1] on board push button for debug : CPLD_PUSH_BTN_RST_IN_N [2] facebook debug reset input :
[1]	pb_dbg_reset_neg_pul_active	R	1	'bx	
[2]	facebook_dbg_reset_neg_pul_active	R	1	'bx	
[3]	1'b0	R	1	'bx	
[4]	reg_hot_req_pul_active	R	1	'bx	
[5]	reg_warm_req_pul_active	R	1	'bx	
[6]	reg_cold_req_pul_active	R	1	'bx	
[7]	reg_pwr_req_pul_active	R	1	'bx	

Reset Status Register-1		Address Offset=0x0E			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
					[ ] DEBUG_RST_BTN_N [3] PD_MAIN_RESET_N [4] hot reset request: rw_0x30 bit 4 negative edge [5] hot reset request: rw_0x30 bit 5 negative edge [6] hot reset request: rw_0x30 bit 6 negative edge [7] hot reset request: rw_0x30 bit 7 negative edge

3.2.11 Reset Status Register-2

Table 12: Reset Status Register-2

Reset Status Register-2		Address Offset=0x0F			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[0]	bmc_req_reset_neg_pul_active	R	1	'bx	Reset status register -2 Each bit consists of status of reset signals (external or Software controlled) When the bit value is set to '1', it indicates that the reset has been asserted, provided cold (reset_cold_n) and warm (reset_warm_n) resets are not there.
[1]	bmc_reset_th_neg_pul_active	R	1	'bx	
[2]	bmc_reset_usrv_neg_pul_active	R	1	'bx	
[3]	bmc_reset_main_neg_pul_active	R	1	'bx	
[4]	bmc_reset_all_neg_pul_active	R	1	'bx	
[5]	wdt_reset_1_neg_pul_active	R	1	'bx	

<table>
<tr><td colspan="2">Reset Status Register-2</td><td colspan="4">Address Offset=0x0F</td></tr>
<tr><td>Bit</td><td>Bit Name</td><td>Access</td><td>Width</td><td>Default Value</td><td>Description</td></tr>
<tr><td>[6]</td><td>wdt_reset_2_neg_pul_active</td><td>R</td><td>1</td><td>'bx</td><td rowspan="2">The register value will be updated on every system reset de-assertion.
When appropriate reset occurs its corresponding bit will be set to 1 as mentioned below and all other bits of the registers will be cleared.

<table><tr><td>[0]</td><td>bmc request reset input :BMC_MAIN_RESET_N</td></tr><tr><td>[1]</td><td>bmc reset request to cpld, input #1 : BMC_CPLD_RESET1</td></tr><tr><td>[2]</td><td>bmc reset request to cpld, input #2 : BMC_CPLD_RESET2</td></tr><tr><td>[3]</td><td>bmc reset request to cpld, input #3 : LS_BMC_CPLD_RESET3</td></tr><tr><td>[4]</td><td>bmc reset request to cpld, input #4 : LS_BMC_CPLD_RESET4</td></tr><tr><td>[5]</td><td>wdt_reset_1_neg_pul : LS_BMC_WDTRST1</td></tr><tr><td>[6]</td><td>wdt_reset_2_neg_pul : LS_BMC_WDTRST2</td></tr><tr><td>[7]</td><td>PD_STBY_RESET_N</td></tr></table></td></tr>
<tr><td>[7]</td><td>pd_stby_reset_n_edge_active</td><td>R</td><td>1</td><td>'bx</td></tr>
</table>

3.2.12 PSU Status Register

Table 13: PSU Status Register

TBD Register		**Address Offset=0x10**			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7]	-	R	1	'b1	Reserved
[6]	PSU2_INPUT_OK	R	1	'bx	Active Low PSU2 Input OK status The input pin PSU2_INPUT_OK is mapped directly to this register.
[5]	PSU2_PWR_OK	R	1	'bx	Active Low PSU1 Power OK status The input pin PSU2_PWR_OK is mapped directly to this register.
[4]	PSU2_PRSNT_N	R	1	'bx	Active Low PSU2 Present status The input pin PSU2_PRSNT_N is mapped directly to this register.
[3]	-	R	1	'b1	Reserved
[2]	PSU1_INPUT_OK	R	1	'bx	Active Low PSU1 Input OK status The input pin PSU1_INPUT_OK is mapped directly to this register.
[1]	PSU1_PWR_OK	R	1	'bx	Active Low PSU1 Power OK status The input pin PSU1_PWR_OK is mapped directly to this register.
[0]	PSU1_PRSNT_N	R	1	'bx	Active Low PSU1 Present status The input pin PSU1_PRSNT_N is mapped directly to this register.

3.2.13 On Board Power Status Register-1

Table 14: On Board Power Status Register-1

On Board Power Status Register-1		Address Offset=0x11			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:3]	-	R	7	'h0	Reserved
[0]	P1V2_STBY_OK	R	1	'bx	1.2V Power OK. The input pin P1V2_STBY_OK is mapped directly to this register.

3.2.14 On Board Power Status Register-2

Table 153: On Board Power Status Register-2

On Board Power Status Register-2		Address Offset=0x12			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:6]	Reserved	R	2	'b00	***These bits are hard coded to 0***
[5]	V3V3_HOT	R	1	'bx	3.3V over temperature or over current alarm The active low input pin V3V3_HOT is mapped directly to this register.
[4]	V3V3_VRDY1	R	1	'bx	3.3V voltage ready status (Active high) The Active high input pin V3V3_VRDY1 is mapped directly to this register.
[3]	VANLG_HOT	R	1	'bx	Analog Voltage over temperature or over current alarm The active low input pin VANLG_HOT is mapped directly to this register.

On Board Power Status Register-2		Address Offset=0x12			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[2]	VANLG_VRDY1	R	1	'bx	Analog Voltage voltage ready status (Active high) The Active high input pin VANLG_VRDY1 is mapped directly to this register.
[1]	VCORE_HOT	R	1	'bx	Vcore over temperature or over current alarm The active low input pin VCORE_HOT is mapped directly to this register.
[0]	VCORE_VRDY1	R	1	'bx	Vcore voltage ready status (Active high) The Active high input pin VCORE_VRDY1 is mapped directly to this register.

3.2.15 I2C PCA9535 interrupt status Register

Table 16: I2C PCA9535 interrupt status Register

I2C PCA9535 interrupt status Register		Address Offset=0x13			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:6]	Reserved	R	2	'b11	***These bits are hard coded to 1***
[5:0]	I2C_IO_**N**_INT_N (where **N**=5,4,3,2,1,0)	R	1	'bx	I2C IO **N** Interrupt The active low input pins I2C_IO_**N**_INT_N is mapped directly to this register. (where **N**=5,4,3,2,1,0)

3.2.16 Alert Status Register

Table 17: Alert Status Register

Alert Status Register		**Address Offset=0x14**			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7]	PSU2_SMB_ALERT_N	R	1	'bx	active low PSU-2 SM bus alert, The input pin PSU2_SMB_ALERT_N is mapped directly to this register.
[6]	PSU1_SMB_ALERT_N	R	1	'bx	active low PSU-1 SM bus alert, The input pin PSU1_SMB_ALERT_N is mapped directly to this register.
[5:0]	SMB_ALERT TEMP_SENSOR_ALERT VANLG_SMB_ALERT V3_3V_SMB_ALERT VCORE_SMB_ALERT PM_SM_ALERT_N	R	6	'bx	Alert status signals: The input or output status of Alert signals are directly mapped to this register. The bits are mapped to corresponding Power Alert status [0]:PM_SM_ALERT_N [1]:VCORE_SMB_ALERT [2]:V3_3V_SMB_ALERT [3]:VANLG_SMB_ALERT [4]:TEMP_SENSOR_ALERT [5]:SMB_ALERT

3.2.17 Internal Interrupt status Register

Table 18: Internal Interrupt Status Register

Internal Interrupt Status Register		Address Offset=0x15			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:4]	-	R	1	'hF	Reserved
[3]	**irq_pca9535_n**	R	1	'b1	Internal PCA9535 Interrupt Interrupt formed using All PCA9535 signals and rw_0x23.
[2]	**irq_ir_pwr_n**	R	1	'b1	Internal Power Hot and Ready Interrupt Interrupt formed using All Power Hot and Ready signals and rw_0x22.
[1]	**irq_power_n**	R	1	'b1	Internal Power OK Interrupt Interrupt formed using Power OK signal signal and rw_0x21.
[0]	**irq_psu_n**	R	1	'b1	Internal PSU Status Interrupt Interrupt formed using All PSU Status signals and rw_0x20.

Note: The internal reset signals are generated, for description of these interrupts, see respective Interrupt block register description.

3.2.18 Top and Bottom selection register

Table 19: Top and Bottom selection register

Top and Bottom selection register			Address Offset=0x1b		
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:2]	-	R	6	'bx	Reserved
[0]	top_led_active_n_out	R	1	'b0	Top LED active speed register
[1]	bot_led_active_n_out	R	1	'b0	Bottom LED active speed register

3.2.19 GPIO CP2112 Input Register

Table 20: GPIO CP2112 Input Register

GPIO CP2112 Input Register		**Address Offset=0x1F**			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:0]	LS_CP2112_CPLD_GPION where (**N**= 7,6,..,0)	R	1	'bx	GPIO**N** from CP2112 The input pins CP2112_GPIO**N** is mapped directly to this register. where (**N**= 7,6,..,0)

3.2.20 Interrupt Block Register: PSU

Table 21: Interrupt Block Register: PSU

Interrupt Block Register: PSU		**Address Offset=0x20**			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:0]	**psu_int_blk**	RW	8	'h00	PSU Interrupt Block: Interrupt Block Register for PSU Interrupts. Set 1 to Block corresponding PSU interrupts. Set 0 to enable corresponding PSU interrupts. Note: The bit and corresponding Interrupts which is blocked or enabled are listed below [7]:Not used [6]:PSU2_INPUT_OK [5]:PSU2_PWR_OK [4]:PSU2_PRSNT_N [3]:Not used [2]:PSU1_INPUT_OK

Interrupt Block Register: PSU		Address Offset=0x20			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
					[1]:PSU1_PWR_OK [0]:PSU1_PRSNT_N ***These interrupts with mask bits are combined to form a single interrupt (irq_psu_n)***

3.2.21 Interrupt Block Register: Power OK

Table 22: Interrupt Block Register: Power OK

Interrupt Block Register: Power OK		Address Offset=0x21			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:1]	-	RW	7	'h0	Reserved
[0]	**pwr_ok_int_blk**	RW	1	'b0	Power OK Interrupt Block: Interrupt Block Register for power OK Interrupt. Set 1 to Block corresponding Alert interrupts. Set 0 to enable corresponding Alert interrupts. The bit and corresponding Interrupts which is blocked or enabled are listed below**.** [0]: P1V2_STBY_OK ***These interrupts with mask bits are combined to form a single interrupt (irq_power_n)***

3.2.22 Interrupt Block Register: Power Ready, Hot

Table 23: Interrupt Block Register: Power Ready, Hot

Interrupt Block Register: Power Ready, Hot		Address Offset=0x22			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:0]	**pwr_ir_int_blk**	RW	8	'h00	Power Ready, Hot Interrupt Block: Interrupt Block Register for Power Ready, Hot Interrupts. Set 1 to block corresponding Main Board Power interrupts. Set 0 to enable corresponding Main Board Power interrupts. The bit and corresponding Interrupts which is blocked or enabled are listed below. [0]:VCORE_VRDY1 [1]:VCORE_HOT [2]:VANLG_VRDY1 [3]:VANLG_HOT [4]:V3V3_VRDY1 [5]:V3V3_HOT [6]: not used [7]: not used ***These interrupts with mask bits are combined to form a single interrupt (irq_ir_pwr_n)***

3.2.23 Interrupt Block Register: PCA9535

Table 24: Interrupt Block Register: PCA9535

Interrupt Block Register: PCA9535		Address Offset=0x23			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:0]	**pca9535_int_blk**	RW	8	'h00	PCA9535 Interrupt Block: Interrupt Block Register for I2C IO device PCA9535 Interrupts. Set 1 to block corresponding Main Board Power interrupts. Set 0 to enable corresponding Main Board Power interrupts. The bit and corresponding Interrupts which is blocked or enabled are listed below. [7]: Not used [6]: Not used [5]:I2C_IO_5_INT_N [4]:I2C_IO_4_INT_N [3]:I2C_IO_3_INT_N [2]:I2C_IO_2_INT_N [1]:I2C_IO_1_INT_N [0]:I2C_IO_0_INT_N ***These interrupts with mask bits are combined to form a single interrupt (irq_pca9535_n)***

3.2.24 Interrupt Block Register: Alert

Table 25: Interrupt Block Register: Alert

Interrupt Block Register: Alert		Address Offset=0x24			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:0]	**smb_int_blk**	RW	8	'h0	Alert Interrupt Block : Interrupt Block Register for Alert Interrupts. These Alert signals are power alert and voltage alert signals. Set 1 to Block corresponding Alert interrupts. Set 0 to enable corresponding Alert interrupts. The bit and corresponding Interrupts which is blocked or enabled are listed below. [0]:PM_SM_ALERT_N [1]:VCORE_SMB_ALERT [2]:V3_3V_SMB_ALERT [3]:VANLG_SMB_ALERT [4]:TEMP_SENSOR_ALERT [5]:Not used [6]:PSU1_SMB_ALERT_N [7]:PSU2_SMB_ALERT_N

3.2.25 Interrupt Block Register: Global Interrupt

Table 26: Interrupt Block Register: Global Interrupt

Interrupt Block Register: Global Interrupt Enable		**Address Offset=0x25**			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7]	BMC CPLD QSFP Interrupt Block	RW	1	'b0	Output **BMC_CPLD_QSFP_INT** is interrupt formed by **irq_pca9535_n.** This Interrupt is blocked/enabled by this bit.
[6]	BMC CPLD Power Interrupt Block	RW	1	'b0	Output **BMC_CPLD_POWER_INT** is formed by three internal interrupts generated from **irq_psu_n & irq_power_n & irq_ir_pwr_n** This Interrupt is blocked/enabled by this bit.
[5]	-	RW	1	'b0	Reserved
[4]	SMB Alert Interrupt	RW	1	'b0	Output **SMB_ALERT** is interrupt output formed using Alert interrupt source and **Reg 0x24**. This Interrupt is blocked/enabled by this bit. Global Interrupt Mask bit for combination of all Alert interrupts.
[3]	Internal I2C Interrupt Block	RW	1	'b0	**irq_pca9535_n** is interrupt output formed using I2C interrupt source and **Reg 0x23**. This Interrupt is blocked/enabled by this bit.
[2]	Power Ready, Hot, Interrupt Block	RW	1	'b0	**irq_ir_pwr_n** is interrupt output formed using Power Ready &

Interrupt Block Register: Global Interrupt Enable		Address Offset=0x25			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
					Hot interrupt source and **Reg 0x22**. This Interrupt is blocked/enabled by this bit.
[1]	Power OK Interrupt Block	RW	1	'b0	**irq_power_n** is interrupt output formed using Power OK interrupt source and **Reg 0x21**. This Interrupt is blocked/enabled by this bit.
[0]	Global PSU Interrupt Block	RW	1	'b0	**irq_psu_n** is interrupt output formed from all the PSU Status interrupt sources and **Reg 0x20**. This Interrupt is blocked/enabled by this bit.

3.2.26 UART Mux Control Register

Table 27: UART Mux Control Register

UART Mux Control Register		Address Offset=0x26			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:2]		RW	6	'h0	Reserved
[7:6]	UART Mux Control Bits uart_ctrl[7:6]	RW	2	'b0	Reserved
[5:2]	-	RW	4	‘b0	Reserved
[1:0]	UART Mux Control Bits uart_ctrl[1:0]	RW	2	'b0	Used as select line for DEBUG_UART_SEL_0 , DEBUG_PORT_UART_SEL_N or hardcode value(0,1). Based on these bits the value for ***uart_dbg_sel*** is assigned.

UART Mux Control Register		Address Offset=0x26			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
					Values are assigned to ***uart_dbg_sel*** are given below when the uart_ctrl[1:0] are, 2'b00: DEBUG_UART_SEL_0 2'b01:DEBUG_PORT_UART_SEL_N. 2'b10: 1'b0 ***(hardcoded)*** 2'b00: 1'b1 ***(hardcoded)*** **** uart_dbg_sel is used to implement the DEBUG UART Mux implementation as mentioned in the spec. If uart_ctrl[1:0] = 00, then the implementation is as per spec.***

3.2.27 CP2112 Direction Register

Table 28: CP2112 Direction Register

CP2112 Direction Register		Address Offset=0x2C			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:0]	CP2112 Output Enable Bits	RW	8	'h00	Defines Output enable bits for bidirectional GPIO**n**(**n**=7:0) from CP2112. 0: defines respective GPIOs as input(s) 1: defines respective GPIOs as output(s) and the contents of CP2112 Output Data Register(0x2d) will be loaded on CP2112_GPIOs.. ***LS_CP2112_CPLD_GPIO0 to LS_CP2112_CPLD_GPIO7 are affected by these output value.***

3.2.28 CP2112 Output Data Register

Table 29: CP2112 Output Data Register

CP2112 Output Data Register		Address Offset=0x2D			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:0]	CP2112 Output Data Bits	RW	8	'h00	Defines Output Data bits for output CP2112 GPIO**n** (**n**=7:0) ***LS_CP2112_CPLD_GPIO0 to LS_CP2112_CPLD_GPIO7 are affected by these output value.***

3.2.29 Miscellaneous Register

Table 304: Miscellaneous Register

Miscellaneous Register		Address Offset=0x2F			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7]	CPLD_IN3	RW	1	‘b1	*** currently not used**
[6]	iso_force_mode	RW	1	‘b1	*** currently not used**
[5]	iso_force_buffer	RW	1	‘b1	*** currently not used**
[4]	iso_force_usrv	RW	1	‘b1	*** currently not used**
[3]	-	RW	1	‘b1	
[2]	force_2nd_write	RW	1	‘b1	*** currently not used**
[1]	enable_2nd_write_protect	RW	1	‘b1	*** currently not used**
[0]	DUAL_BOOT_EN	RW	1	‘b1	DUAL_BOOT_EN Output is directly driven by the value of this register.

3.2.30 Power Control Register

Table 31: Power Control Register

Power Control Register		Address Offset=0x30			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:2]	-	RW	6	‘h3F	Reserved
[1]	PWR_MAIN_EN	RW	1	'b1	Active high Enable main power output PWR_MAIN_EN is directly mapped to this register bit.
[0]	PWR_CYC_ALL_N	RW	1	'b1	Power cycle output to PWR1014a output PWR_CYC_ALL_N is directly mapped to this register bit.

3.2.31 Reset Request Register (power, cold, warm, hot)

Table 32: Reset Request Register (power, cold, warm, hot)

Reset Request Register (power, cold, warm, hot)		Address Offset=0x31			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7]	Power reset request	RW	1	'b1	Active low Power/Cold/ Warm/hot reset request bits. When this bit is written, the system generates a pulse for [7]: power reset request. [6]: cold reset request. [5]: warm reset request. [4]: hot reset request.
[6]	Cold reset request	RW	1	'b1	
[5]	Warm reset request	RW	1	'b1	
[4]	Hot Reset request	RW	1	'b1	
[3:0]	-	RW	4	‘hF	Reserved

3.2.32 Reset Control Register-1

Table 33: Reset Control Register-1

Reset Control Register-1		Address Offset=0x32			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:4]	-	RW	4	‘h0	Reserved
[3]	-	RW	1	'b0	Active low output resets are generated when the corresponding Software reset bits are ‘0’. This Software resets are combined with cold and warm reset to generate output reset. [0] : MICROSRV_RST_N [1]:MICROSERV_PCIE_RST_N [2]: ISO_XPLIANT_RST_N [3]: LS_DPLL_RESET_N
[2]	Xpliant reset	RW	1	'b0	
[1]	Microserver pcie reset	RW	1	'b0	
[0]	micro-server reset	RW	1	'b0	

3.2.33 QSFP Reset Register-1

Table 34: QSFP Reset Register-1

QSFP Reset Register-1		Address Offset=0x34			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:0]	QSFP Reset bits[7:0]	RW	8	'h00	Defines Active low [7:0] QSFP Reset bits This bit is used to generate active low output P**i**_QRESET_N where **i**=[7:0]

3.2.34 QSFP Reset Register-2

Table 35: QSFP Reset Register-2

QSFP Reset Register-2		**Address Offset=0x35**			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:0]	QSFP Reset bits[15:8]	RW	8	'h00	Defines Active low [15:8] QSFP Reset bits This bit is used to generate active low output P**i**_QRESET_N where **i**=[15:8]

3.2.35 QSFP Reset Register-3

Table 36: QSFP Reset Register-3

QSFP Reset Register-3		**Address Offset=0x36**			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:0]	QSFP Reset bits[23:16]	RW	8	'h00	Defines Active low [23:16] QSFP Reset bits This bit is used to generate active low output P**i**_QRESET_N where **i**=[23:16]

3.2.36 QSFP Reset Register-4

Table 37: QSFP Reset Register-4

QSFP Reset Register-4		**Address Offset=0x37**			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:0]	QSFP Reset bits[31:24]	RW	8	'h00	Defines Active low [31:24] QSFP Reset bits This bit is used to generate active low output P**i**_QRESET_N where **i**=[31:24]

3.2.37 I2C Mux Reset Register

Table 38: I2C Mux Reset Register

I2C Mux Reset Register		Address Offset=0x38			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:6]	-	RW	2	'b11	Reserved
[5]	I2C Mux QSFP Reset	RW	1	'b1	Active low output resets are generated when the corresponding Software reset bits are '0'. This Software resets are combined with cold and warm reset to generate output reset. [0] :I2C_MUX_RST0_N [1]: I2C_MUX_RST1_N [2]: I2C_MUX_RST2_N [3]: I2C_MUX_RST3_N [4]: I2C_MUX_PSU_RST_N [5]: I2C_MUX_EXP_RST_N ***note: the default values of these bits are '0', so the output resets are asserted by default after power on,**
[4]	I2C Mux PSU Reset	RW	1	'b1	
[3:0]	I2C Mux **i** Reset (where **i** = 3,2,1,0)	RW	4	'h0	

3.2.38 Reset Control Register-2

Table 39: Reset Control Register-2

Reset Control Register-2		Address Offset=0x39			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7]	DPLL Reset	RW	1	'b1	Active low output resets are generated when the
[6]	USB SPI BRIDGE Reset	RW	1	'b1	

Reset Control Register-2		Address Offset=0x39			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[5]	On-board PHY Reset	RW	1	'b1	corresponding Software reset bits are '0'. This Software resets are combined with cold and warm reset to generate output reset. [0] :FANCARD_RST_N [1]:USB_BRDG_RST_N [2]: USB_HUB_RST_N [3]: BCM5387_PHY_RST_N [4]: FP_PHY_RST_N [5]: BCM54616_PHY_RST_N [6]: LS_USB_SPI_RST_N [7]: LS_DPLL_RST_N ***** *****_LS_DPLL_RST_N also includes BMC_MAIN_REST_N along with cold and warm resets._
[4]	Front Port PHY Reset	RW	1	'b1	
[3]	OOB Switch Reset	RW	1	'b1	
[2]	USB Hub Reset	RW	1	'b1	
[1]	USB Bridge Reset	RW	1	'b1	
[0]	Fan Control Card Reset	RW	1	'b1	

3.2.39 Reset Enable register-1

Table 405: Reset Enable Register-1

Reset Enable Register-1		Address Offset=0x3A			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7]	-	RW	1	'b0	Reserved
[6:0]	Reset Enable Register-1	RW	1	'b0	Reset Enable bits Defines Active high enable for pushbutton Reset inputs. 1: Bypass the Reset.

Reset Enable Register-1		Address Offset=0x3A			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
					0: Blocks the input Reset and send 1 instead of reset. Each Bit Enables corresponding resets as, [0] : BMC_MAIN_RESET_N [1] : BMC_CPLD_RESET1 [2] : BMC_CPLD_RESET2 [3] : LS_BMC_CPLD_RESET3 [4] : LS_BMC_CPLD_RESET4 [5] : LS_BMC_WDTRST1 [6] : LS_BMC_WDTRST2

3.2.40 Reset Enable Register-2

Table 416: Reset Enable Register-2

Reset Enable Register-2		Address Offset=0x3B			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:4]	-	RW	5	'h0	Reserved
[2:0]	Reset Enable Bits for pushbuttons	RW	3	'b000	Reset Enable bits Defines Active high enable for pushbutton Reset inputs. 1: Bypass the Reset. 0: Blocks the input Reset and send 1 instead of reset. Each Bit Enables corresponding resets as, [0] : PUSHBUTTON_RST_N

Reset Enable Register-2		Address Offset=0x3B			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
					[1] : CPLD_PUSH_BTN_RST_IN_N [2] : DEBUG_RST_BTN_N

3.2.41 LED-0 control Register

Table 42: LED-0 control Register

LED-0 control Register		Address Offset=0x3C			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:2]	-	RW	8	-	Reserved
[1]	TH LED0 Clear	RW	1	'b1	Active high LED0 Clear bit If warm reset is not there, then this bit controls the output signal LED_CLEAR0, Drives ‘0’ if this bit is 1 else Drives ‘1’ if this bit is 0.
[0]	TH LED0 Enable	RW	1	'b1	Active high LED0 Enable bit If this bit is set to 1, LED_DATA0 is driven by input TH_LED_DATA0 and LED_CLK0 will be driven by input TH_LED_CLK0 If this bit is 0, '0' will be driven on LED_DATA0 and LED_CLK0.

3.2.42 LED-1 control Register

Table 43: LED-1 control Register

LED control-1 Register		**Address Offset=0x3D**			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:2]	-	RW	8	-	Reserved
[1]	TH LED1 Clear	RW	1	'b1	Active high LED1 Clear bit. If warm reset is not there, then this bit controls the output signal LED_CLEAR1, Drives '0' if this bit is 1 else Drives '1' if this bit is 0.
[0]	TH LED1 Enable	RW	1	'b1	Active high LED1 Enable bit If this bit is set to 1, LED_DATA1 is driven by input TH_LED_DATA1 and LED_CLK1 will be driven by input TH_LED_CLK1 If this bit is 0, '0' will be driven on LED_DATA1 and LED_CLK1.

3.2.43 Stream LED Control Register-1

Table 44: Stream LED Control Register-1

Stream LED control Register-1		**Address Offset=0x3E**			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:4]	-	RW	5	'h1	Reserved
[3]	Select line for LED1	RW	1	'b1	Defines select bit for LED1 1: Selects clock blink : LED Blinks at 1Hz 0: Selects corresponding LED1 Data bits (Red, Green, Blue - **0x3E[2:0]**)
[2]	LED1 Blue Data bit	RW	1	'b0	LED1 Blue Data bit
[1]	LED1 Green Data bit	RW	1	'b0	LED1 Green Data bit
[0]	LED1 Red Data bit	RW	1	'b0	LED1 Red Data bit

3.2.44 Stream LED Control Register-2

Table 457: Stream LED Control Register-2

Stream LED control Register-2		**Address Offset=0x3F**			
Bit	**Bit Name**	**Access**	**Width**	**Reset Value**	**Description**
[7:4]	TBD	RW	5	'h0	Reserved
[3]	Select bit for LED2	RW	1	'b0	Defines select bit for LED2 1: Selects clock blink : LED Blinks at 1Hz 0: Selects corresponding LED2 Data bits (Red, Green, Blue - **0x3F[2:0]**)
[2]	LED2 Blue Data bit	RW	1	'b0	LED2 Blue Data bit
[1]	LED2 Green Data bit	RW	1	'b0	LED2 Green Data bit
[0]	LED2 Red Data bit	RW	1	'b1	LED2 Red Data bit

3.2.45 MISC Interrupt status register

Table 46: MISC Interrupt status register

MISC Interrupt status register		Address Offset=0x40			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:4]		R	4	'bx	Reserved
[3]	ISO_XP_REI_INIT_DONE	R	1	'bx	Rei init done output
[2]	ISO_XP_INT_N	R	1	'bx	Xpliant interrupt signal
[1]	ISO_XP_OVERT_N	R	1	'bx	Xpliant temp sensor output
[0]	ISO_XP_TEMP_ALRT_N	R	1	'bx	Xpliant temp sensor output

3.2.46 MISC Interrupt enable register

Table 47: MISC interrupt enable register

MISC interrupt enable register		Address Offset=0x41			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:4]		R/W	4	'bx	Reserved
[3]	misc_int_n	R/W	1	1'b1	Active low Global MISC interrupt enable
[2:0]	misc_int_blk	R/W	3	3'b111	[5]- active low ISO_XP_INT_N interrupt enable [6]- active low ISO_XP_OVERT_N interrupt enable [7]- active low ISO_XP_TEMP_ALRT_N interrupt enable

3.2.47 GPIO read register

Table 88: GPIO read register

GPIO read register		Address Offset=0x42			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:4]	-	R	4	'bx	Reserved
[3:0]	ISO_XP_GPIO[3:0] read data	R	4	'bx	GPIO read register

3.2.48 PLL_CLOCK_LOCK status register

Table 49: PLL_CLOCK_LOCK status register

PLL_CLOCK_LOCK status register		Address Offset=0x43			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:3]		R	5	'bx	Reserved
2	ISO_XP_CORE_PLL_LOCK	R	1	1'b0	Core clock PLL lock indication 0-not locked,1- locked
1	ISO_XP_MAC_PLL_LOCK	R	1	1'b0	Mac clock PLL lock indication 0-not locked,1- locked
0	ISO_XP_PEX_PLL_LOCK	R	1	1'b0	PEX clock PLL lock indication 0-not locked,1- locked

3.2.49 CLK_PLL_RESET register

Table 50: CLK_PLL_RESET register

CLK_PLL_RESET register		Address Offset=0x44			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:5]		R/W	5	'bx	Reserved
2	ISO_XP_PEX_CLK_PLL_RST_N	R/W	1	1'b1	PEX Clock PLL reset
1	ISO_XP_MAC_CLK_PLL_RST_N	R/W	1	1'b1	MAC Clock PLL reset
0	ISO_XP_CORE_CLK_PLL_RST_N	R/W	1	1'b1	Core Clock PLL reset

3.2.50 GPIO write register

Table 51: GPIO write register

GPIO write register		Address Offset=0x45			
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:4]	ISO_XP_GPIO	R/W	4	'b0	GPIO direction bit 1- GPIO bit acts as output and data is written 0- GPIO bit acts as input and is tri-stated. Data can be read from the GPIO read register
[3:0]	ISO_XP_GPIO data output bits [3:0]	R/W	4	'b0	GPIO data write register

3.2.51 Speed selection register

Table 52: Speed selection register

Speed selection register			**Address Offset=0x46**		
Bit	**Bit Name**	**Access**	**Width**	**Default Value**	**Description**
[7:2]	-	R /W	6	'bx	Reserved
[1:0]	speed_sel	R /W	2	2'b00	00-Speed selection 100G 01-Speed selection 50G, 1x-Speed selection 25G,