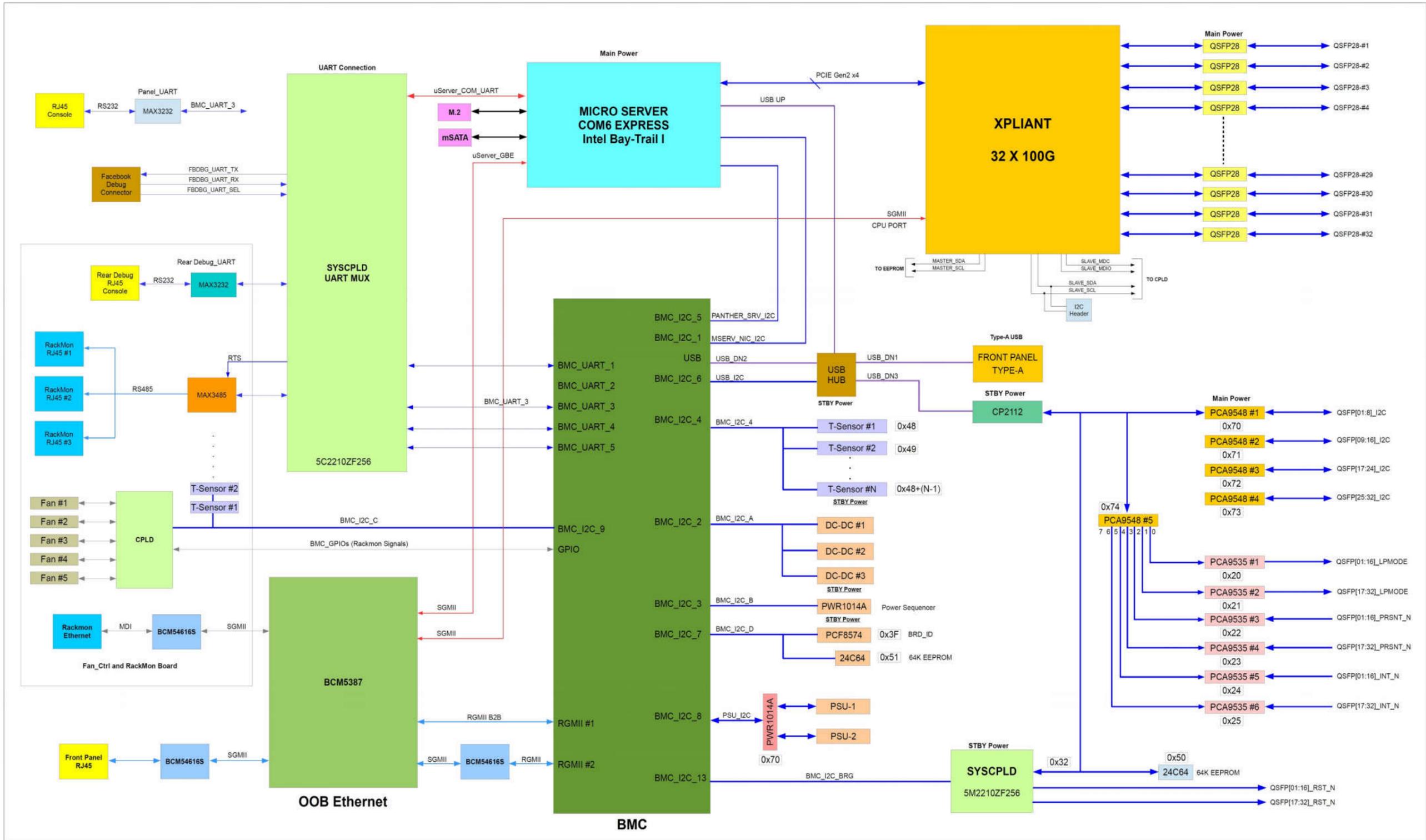


SL.No	TITLE	PAGE NO	SL.No	TITLE	PAGE NO
1	Block Diagrams	Page2-Page10	23	BMC DDR	Page57
2	Clock Circuits	Page11-Page12	24	BMC Strapping and Temp Sensor	Page58
3	CNX88091 Contol Interface	Page14	25	BMC signal isolation buffer	Page59
4	CNX88091 PORTS	Page15-16	26	USB HUB	Page60
5	CNX88091 Strapping	Page17	27	USB I2C Bridge	Page61
6	CNX88091 CORE & AVDD POWER	Page18	28	GE Switch	Page62
7	CNX88091 Decoupling Caps	Page19	29	BMC PHY	Page63
8	CNX88091 GND	Page20	30	FRONT PANEL PHY	Page64
9	CNX88091 GND	Page21	31	CPLD	Page65
10	LEFT BLANK	Page22-Page25	32	BOARD ID & EEPROMS	Page66
11	P/S 2.5V and 1V PLL LDOs	Page26	33	STANDBY POWER	Page67-Page68
12	P/S 1.0V Core switching supply	Page27-Page28	34	MAIN POWER CONNECTOR	Page69
13	P/S 1.0V analog switching supply	Page29-Page30	35	FRONT PANEL CONNECTORS	Page70
14	P/S 3.3V switching supply	Page31-Page32	36	RACKMON & FAN CONNECTOR	Page71
15	P/S 1.8V	Page33	37	HOTSWAP CIRCUIT	Page72
16	POWER MANAGER	Page34	38	DPLL CIRCUIT	Page73
17	QSFP CONNECTORS 2X2	Page35-Page42	39	COM6	Page74-Page79
18	QSFP I2C & IO EXPANDERS	Page43-Page45	40	M.2	Page80
19	QSFP LEDS	Page46-Page49	41	MSATA	Page81
20	QSFP LEDS CLOCK BUFFER & SHIFTREGISTERS	Page50-Page51	42	COM PHY	Page82
21	MICROSERVER CONNECTOR	Page52	43	LEVEL SHIFTERS	Page83
22	Board Management Controller (BMC)	Page53-Page56	44	CHANGE LOG	Page84

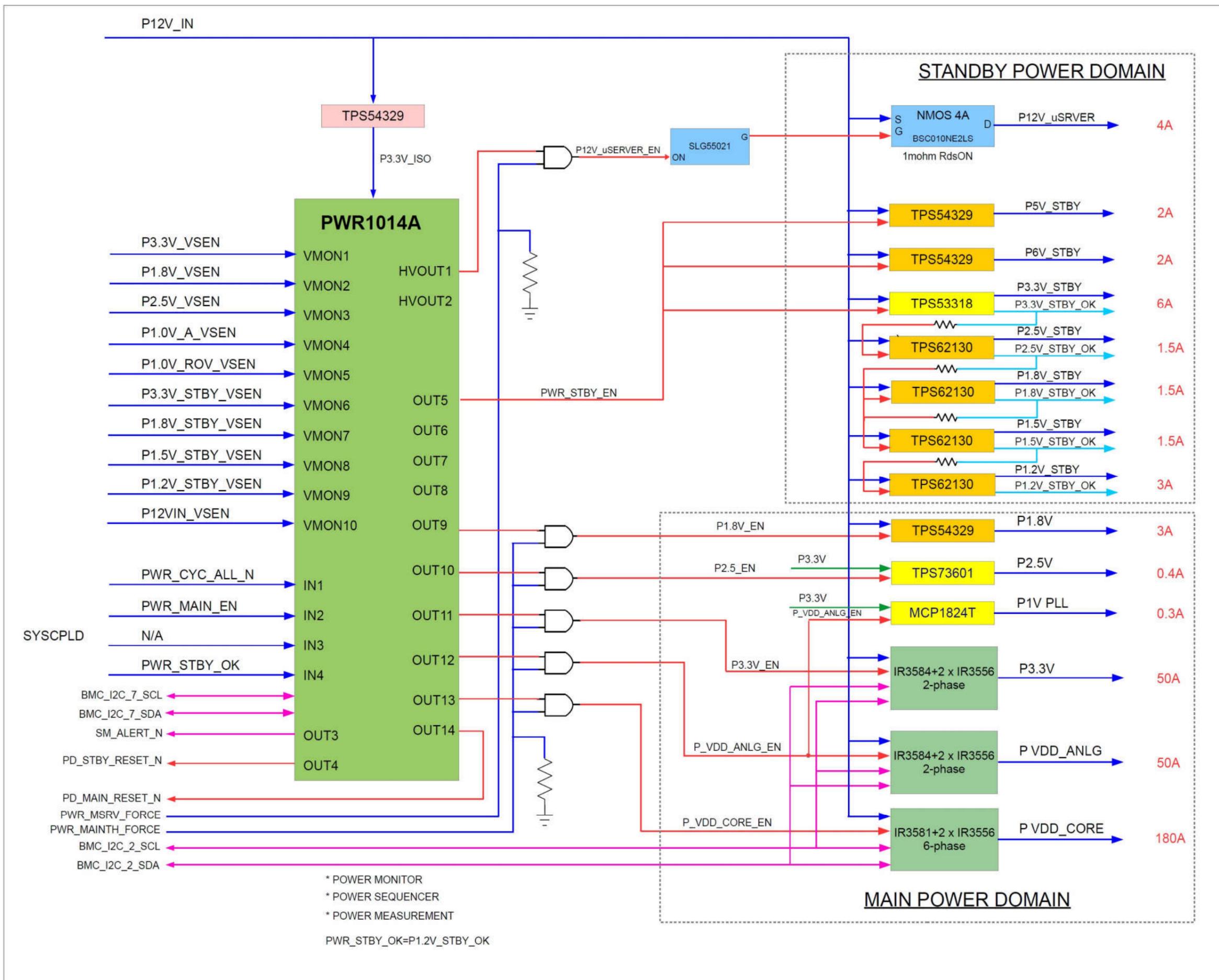
**INDEX**

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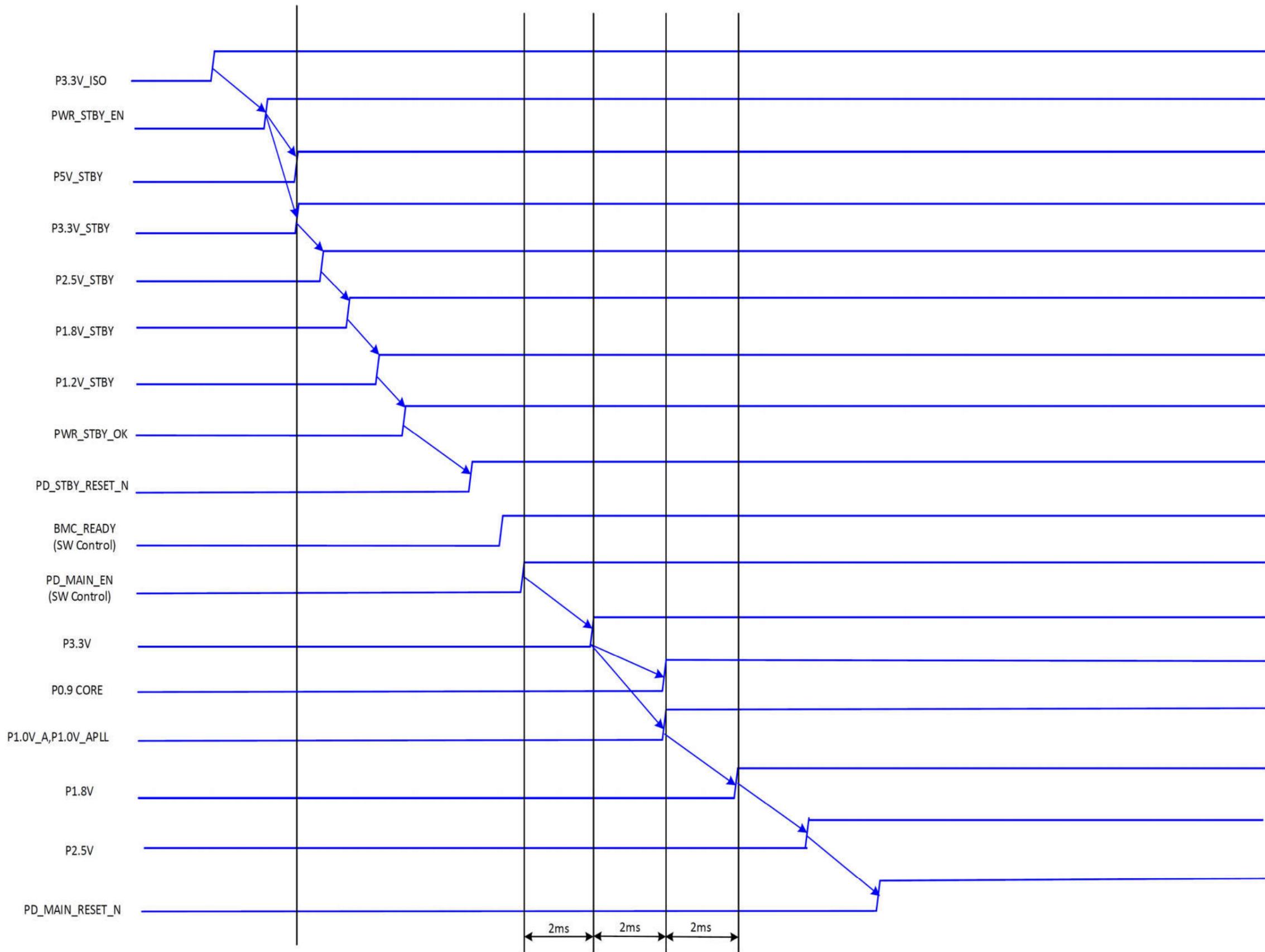
# SYSTEM BLOCK DIAGRAM

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# POWER BLOCK DIAGRAM

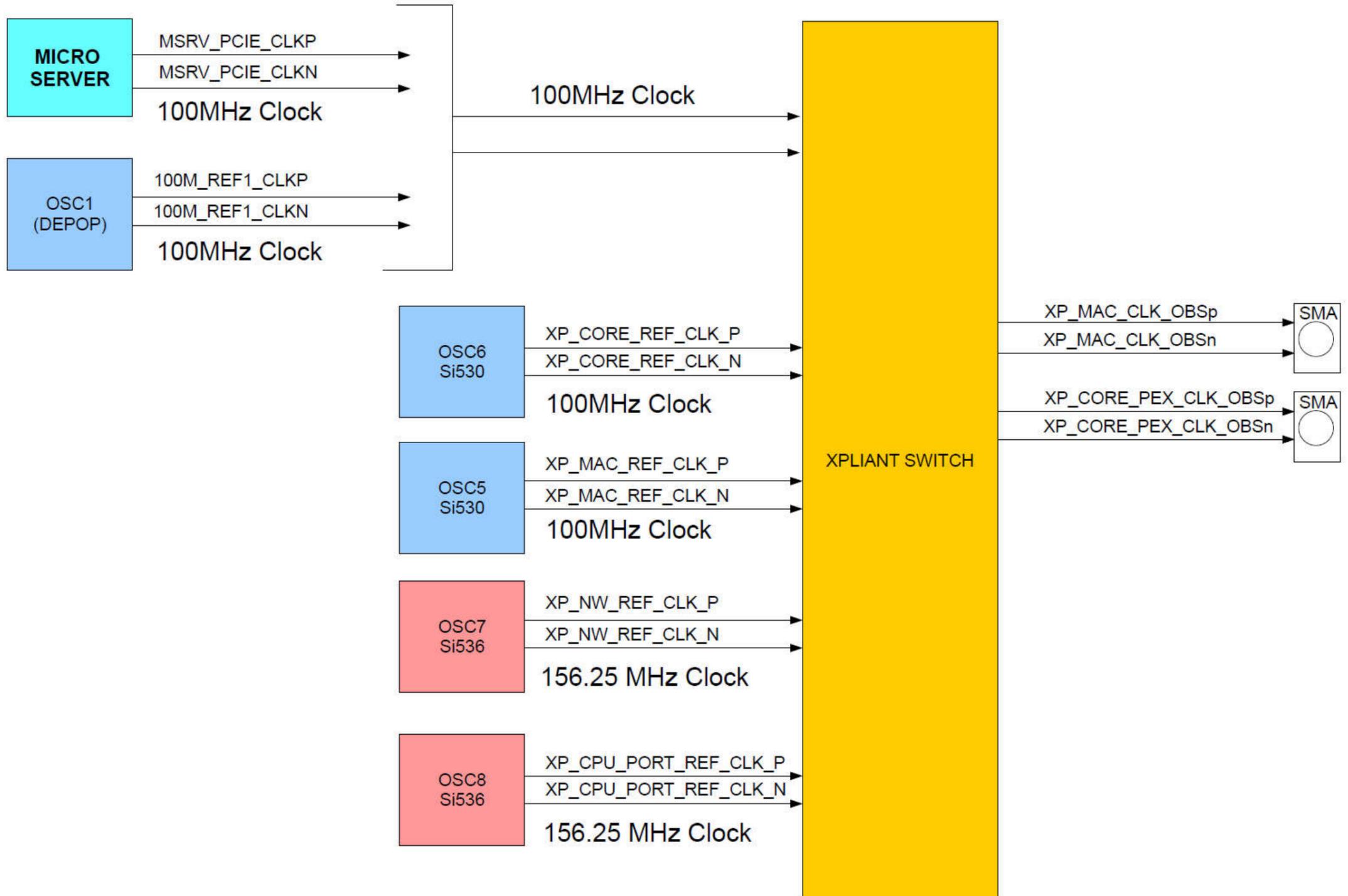
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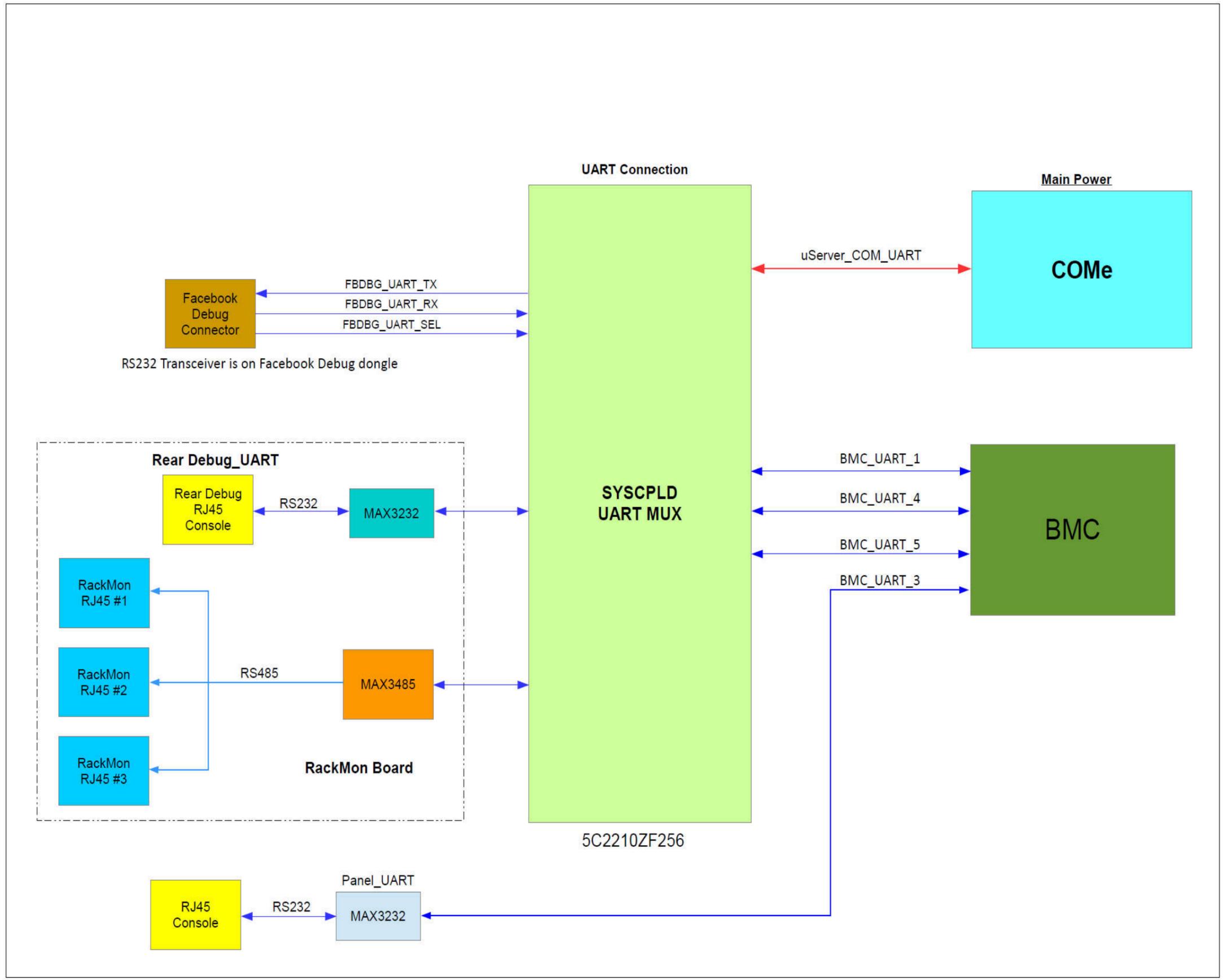
# POWER SEQUENCING

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# XPLIANT CLOCKS

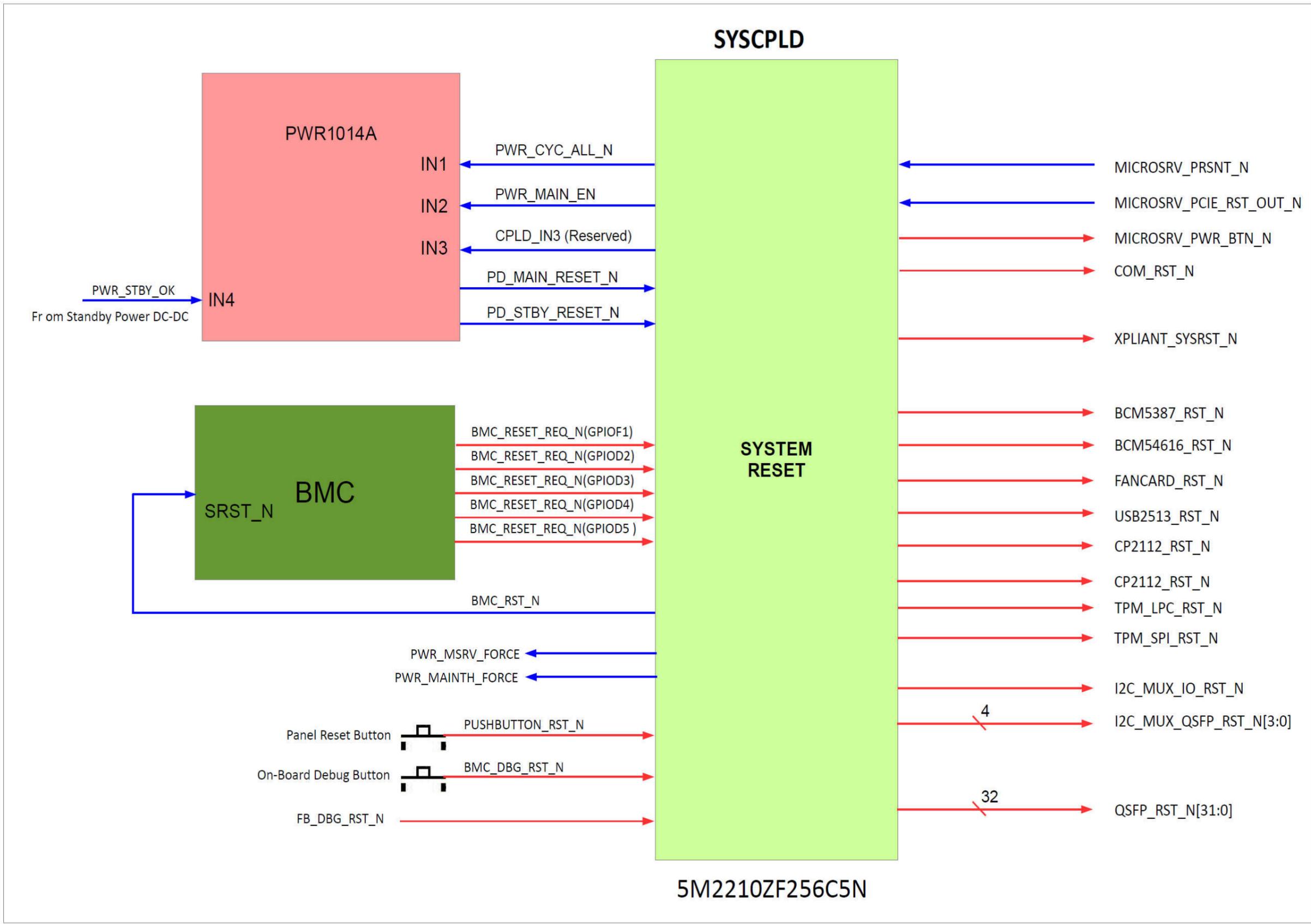


## XPLIANT CLOCKS



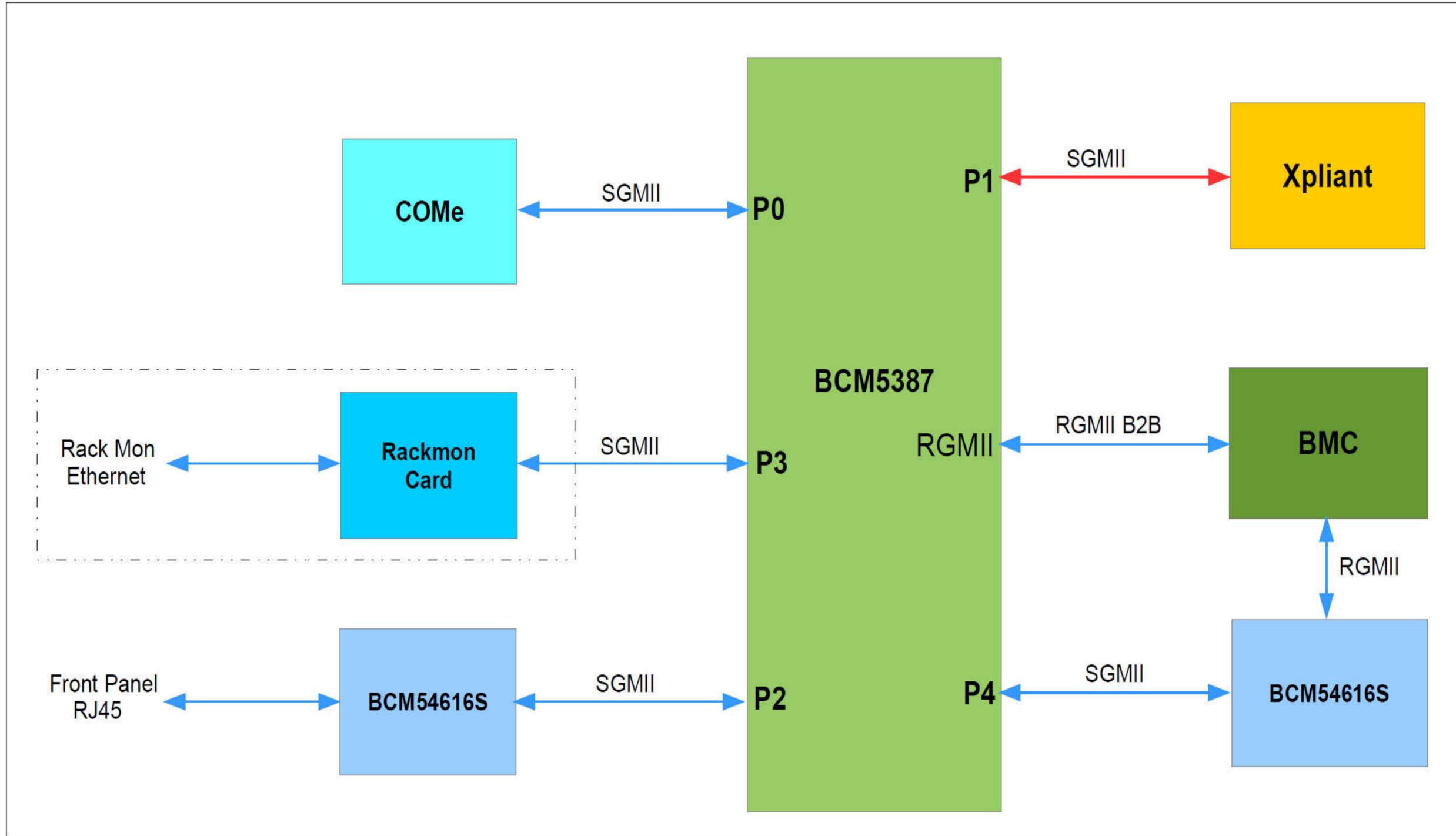
# UART BLOCK DIAGRAM

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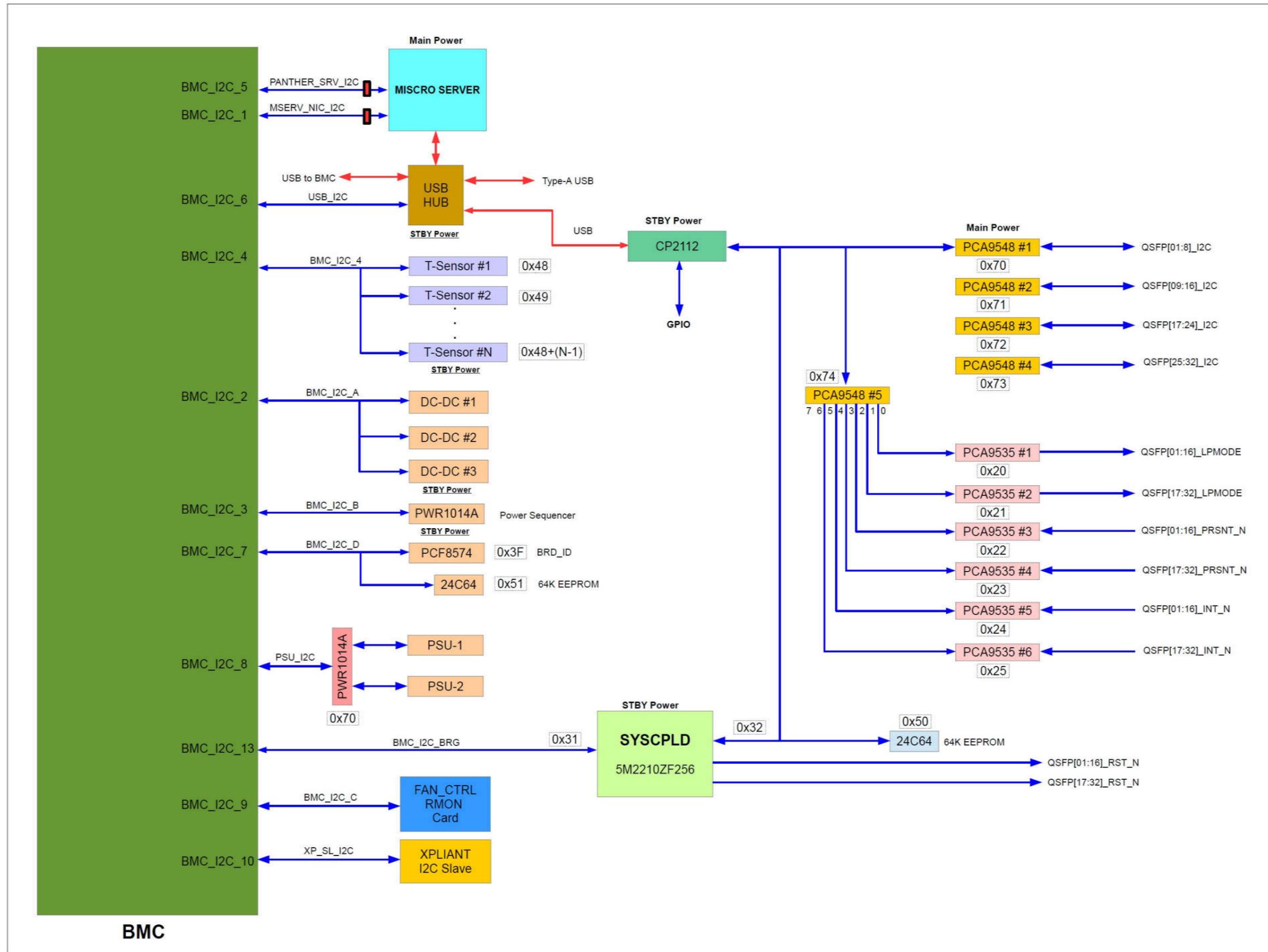
# RESET BLOCK DIAGRAM

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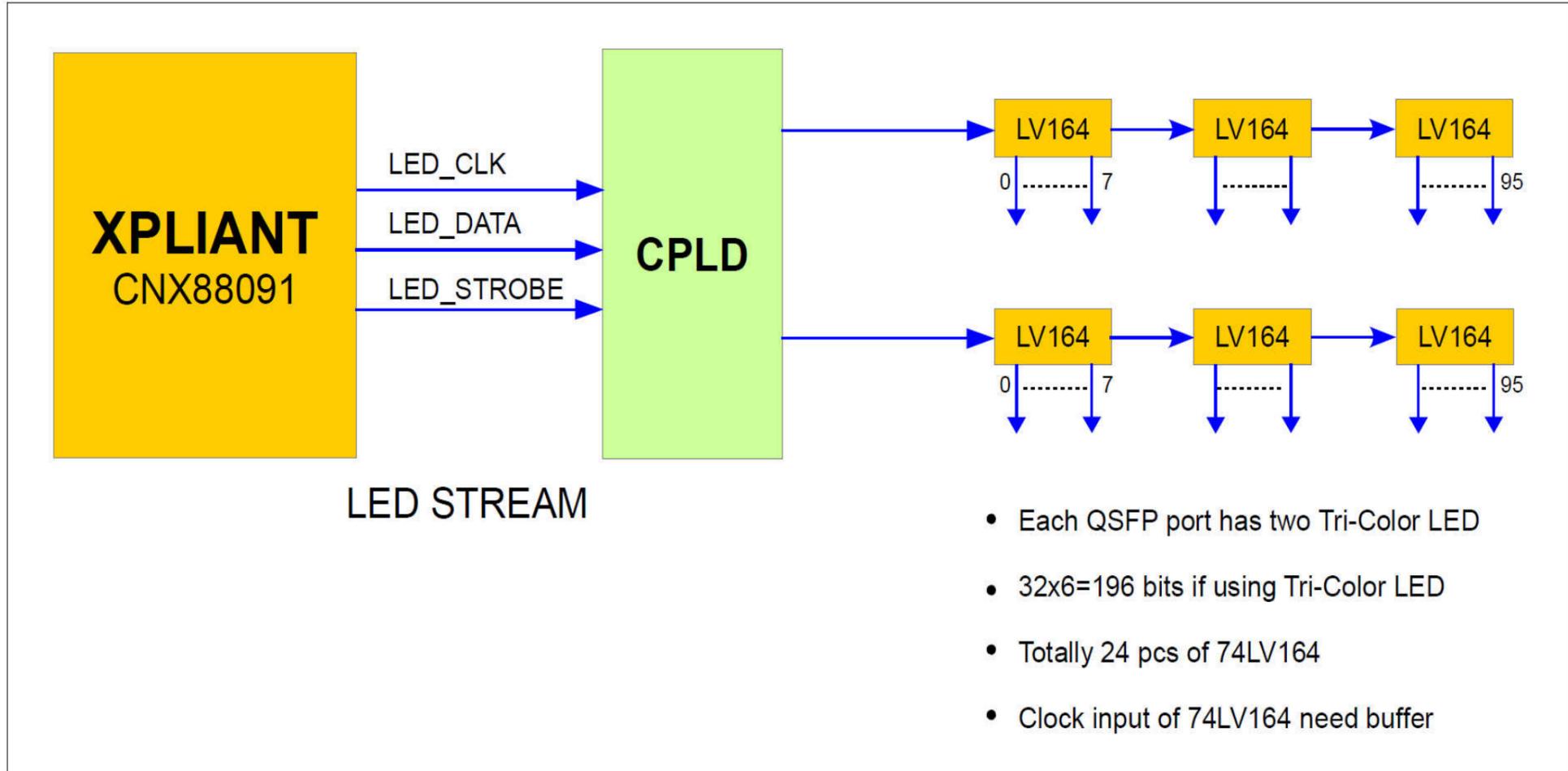
**ETHERNET BLOCK DIAGRAM**

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# I2C BLOCK DIAGRAM

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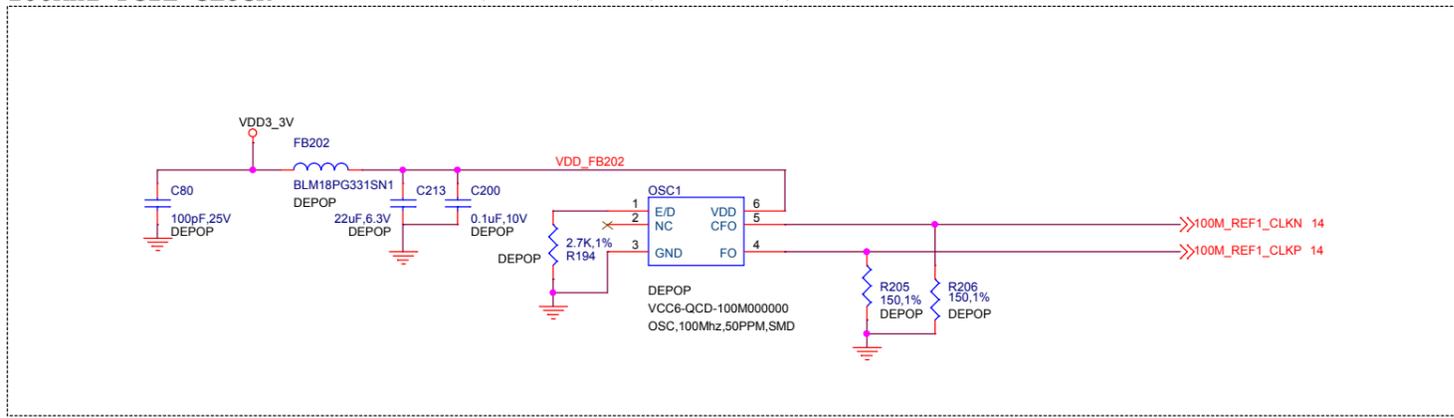


**LED BLOCK DIAGRAM**

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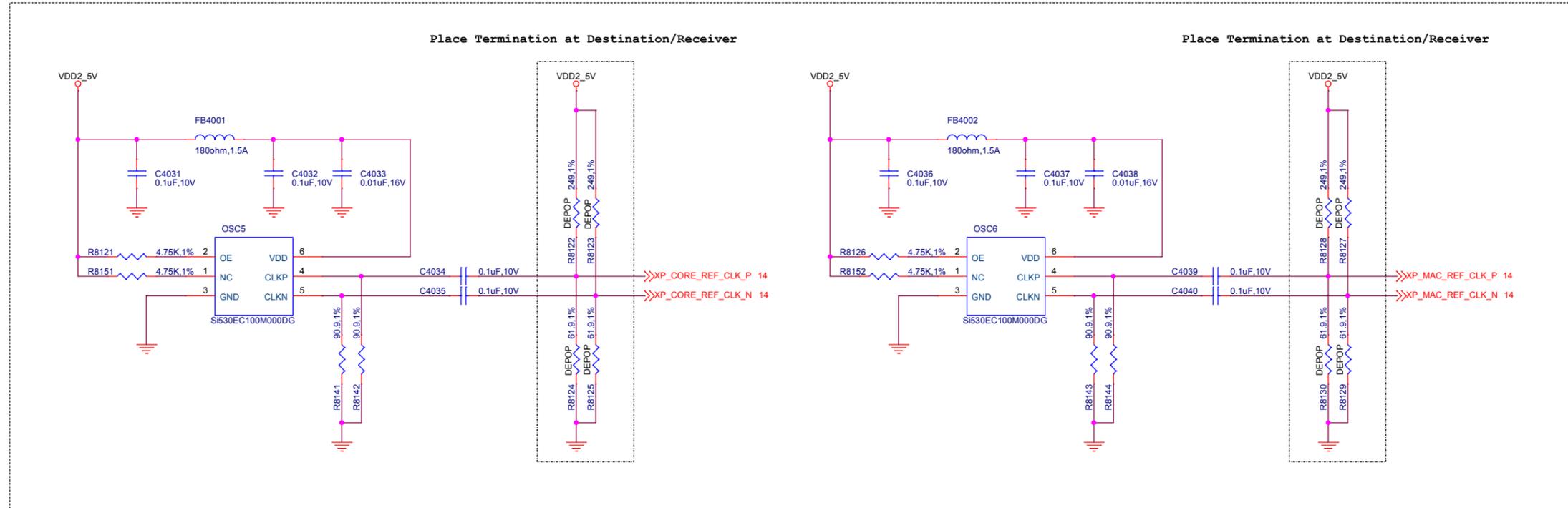
**100MHz PCIE CLOCK**

L= BLM18PG331SN1 (FB,  
3300OHM, PKG:0603,1200mA, DCR:150mOHM, SMD)



**100MHz CORE & MAC CLOCKS**

FB= BLM18PG181SN1D  
(FB, 180OHM, PKG:0603,1500mA, DCR:90mOHM, SMD)

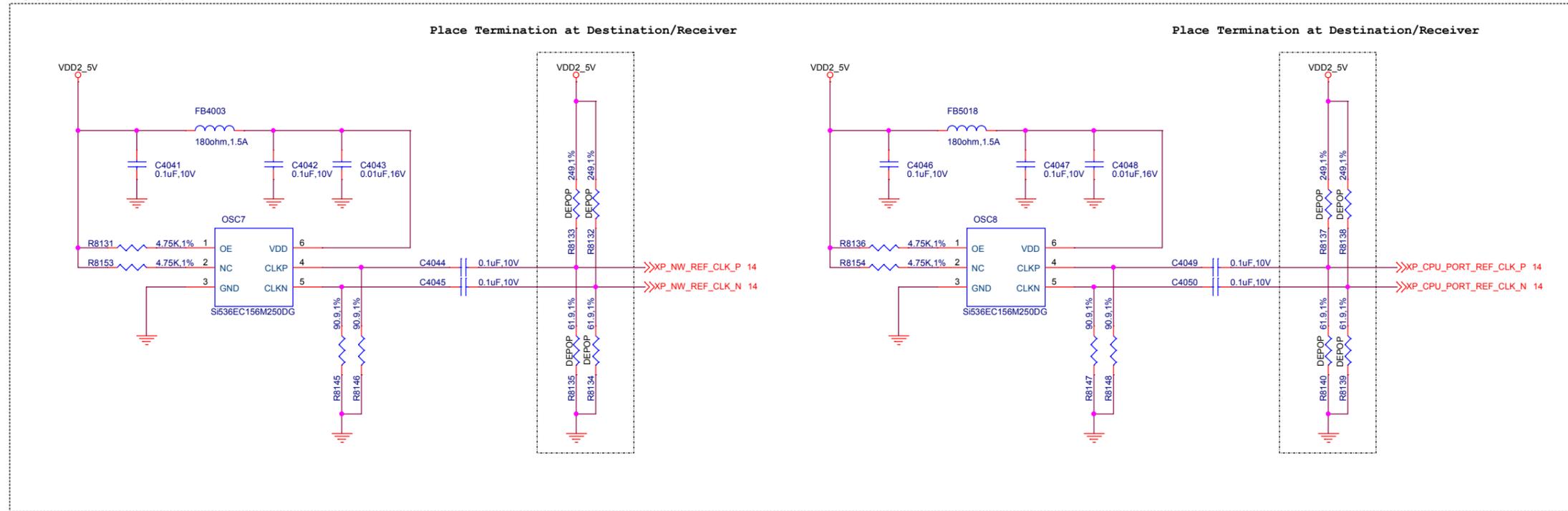


**XPLIANT 100MHz Clocks**

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156.25MHz CLOCKS

FB= BLM18PG181SN1D  
(FB, 180OHM, PKG: 0603, 1500mA, DCR: 90mOHM, SMD)

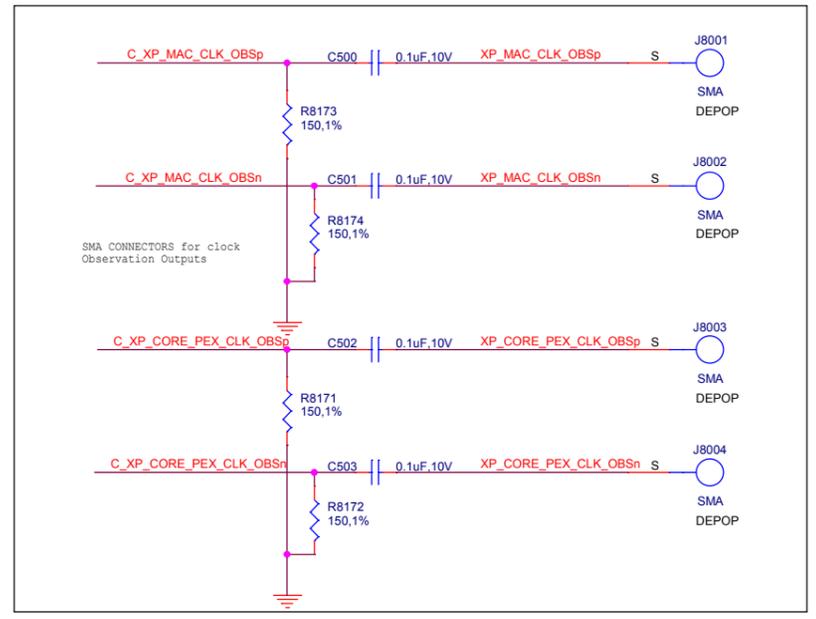
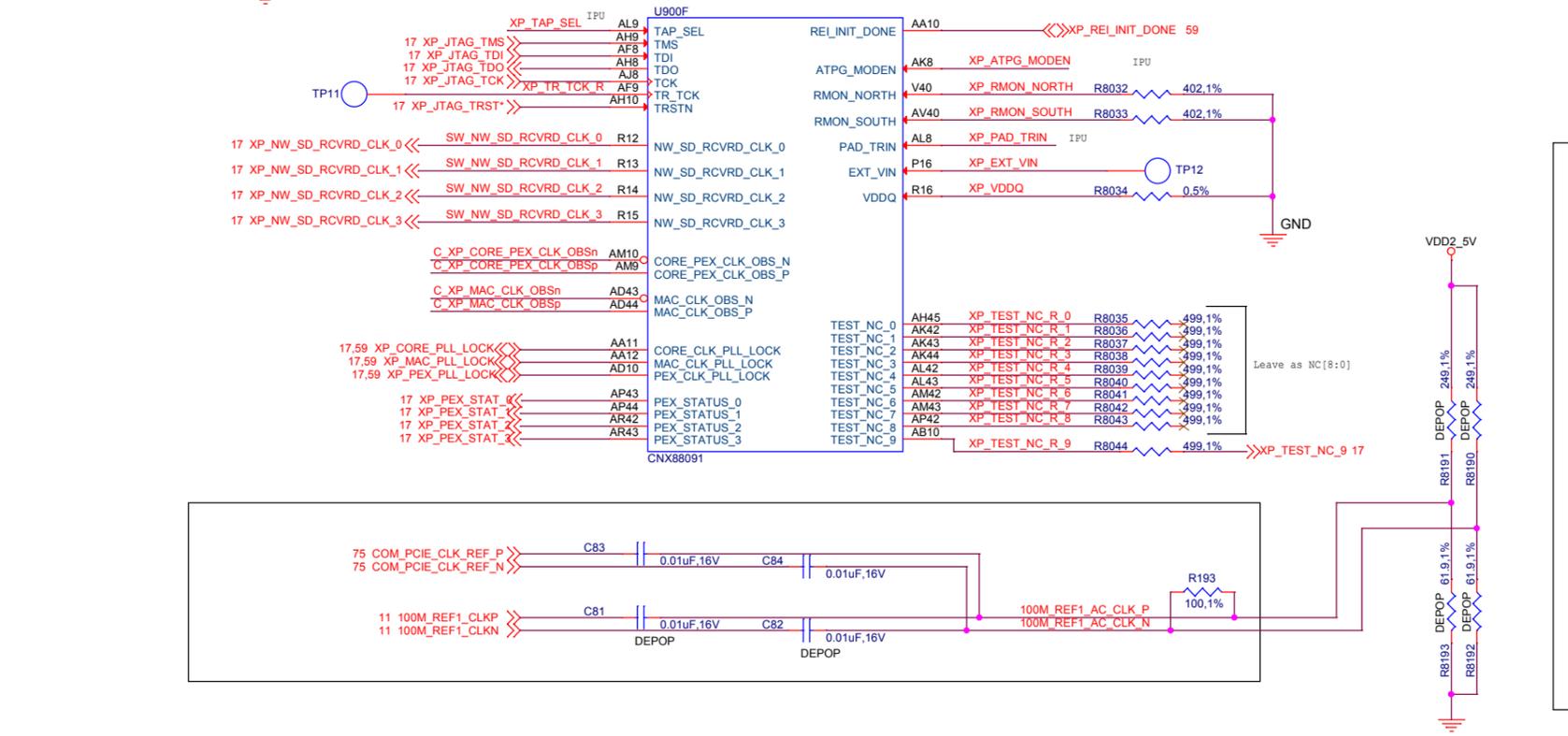
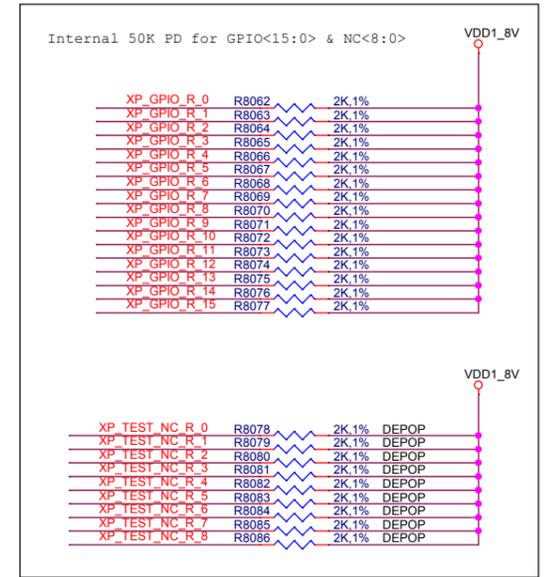
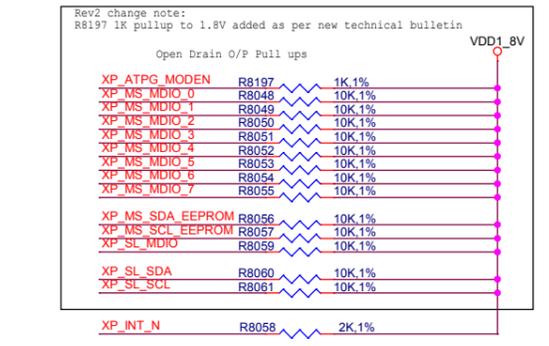
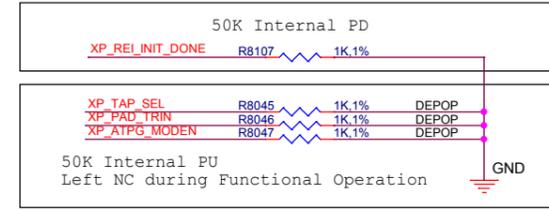
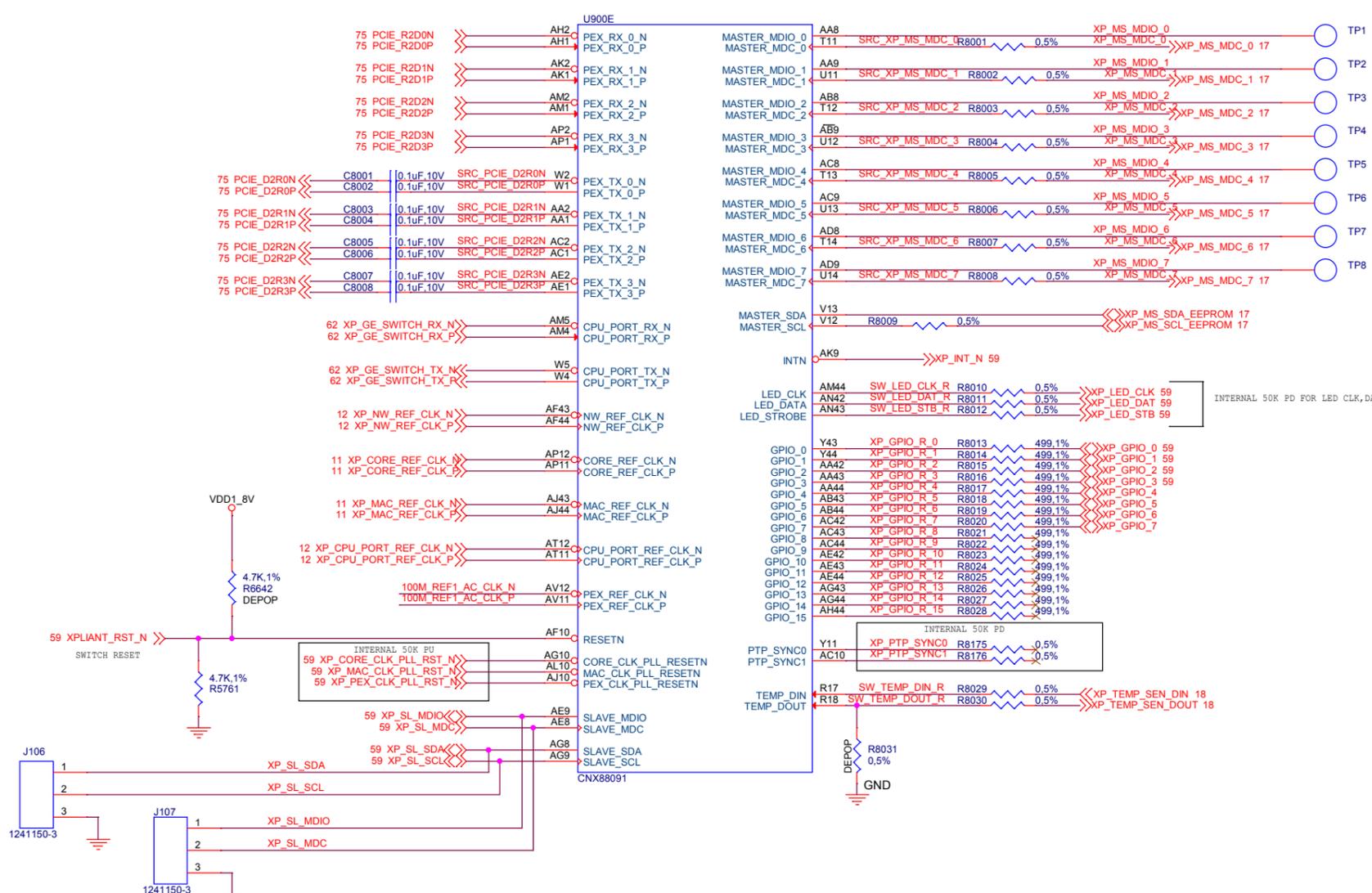


**XPLIANT 156.25MHz Clocks**

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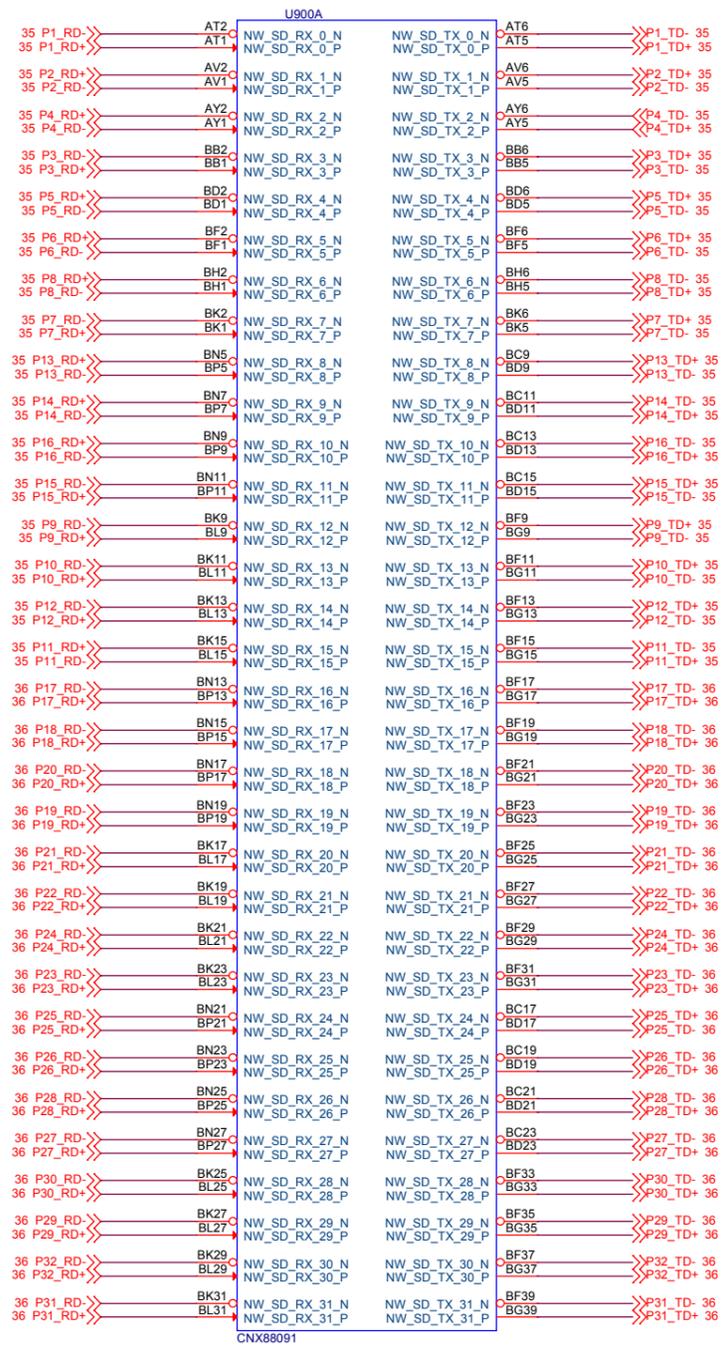
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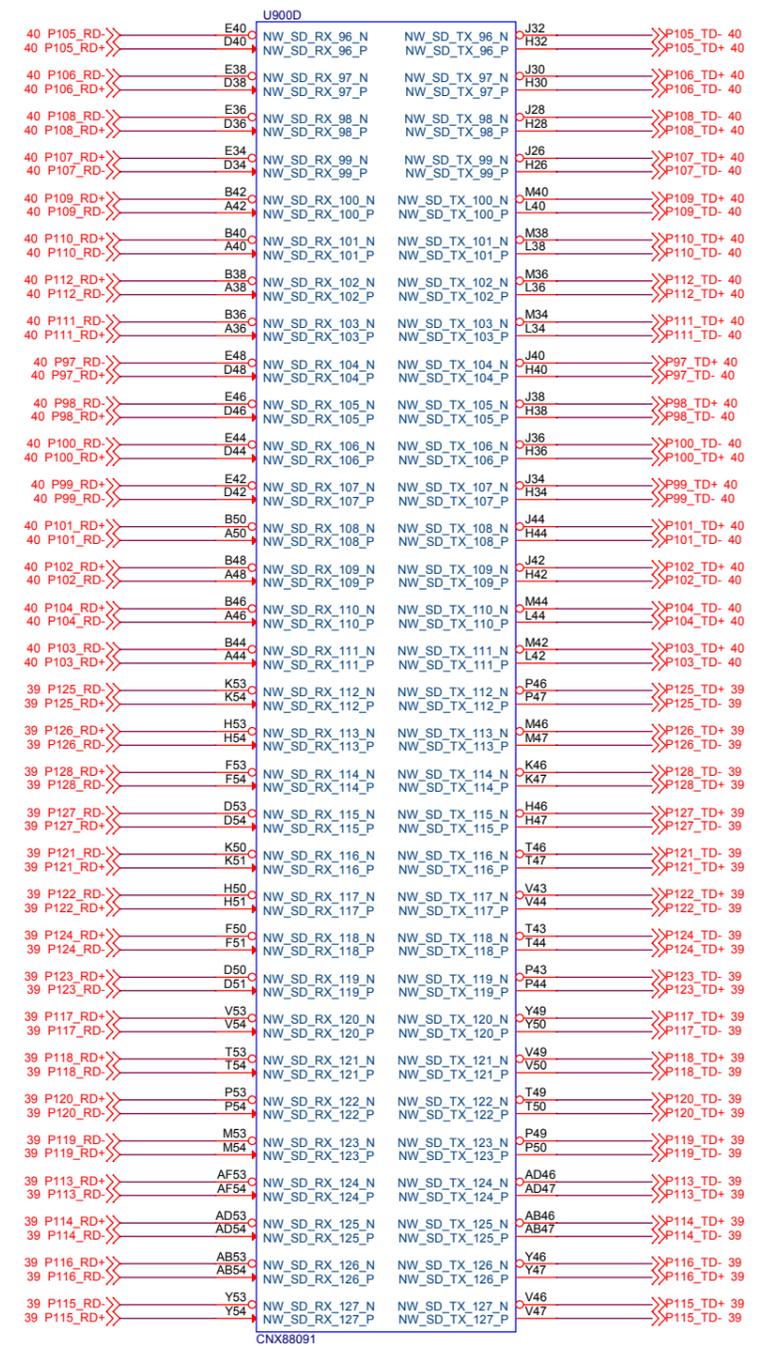
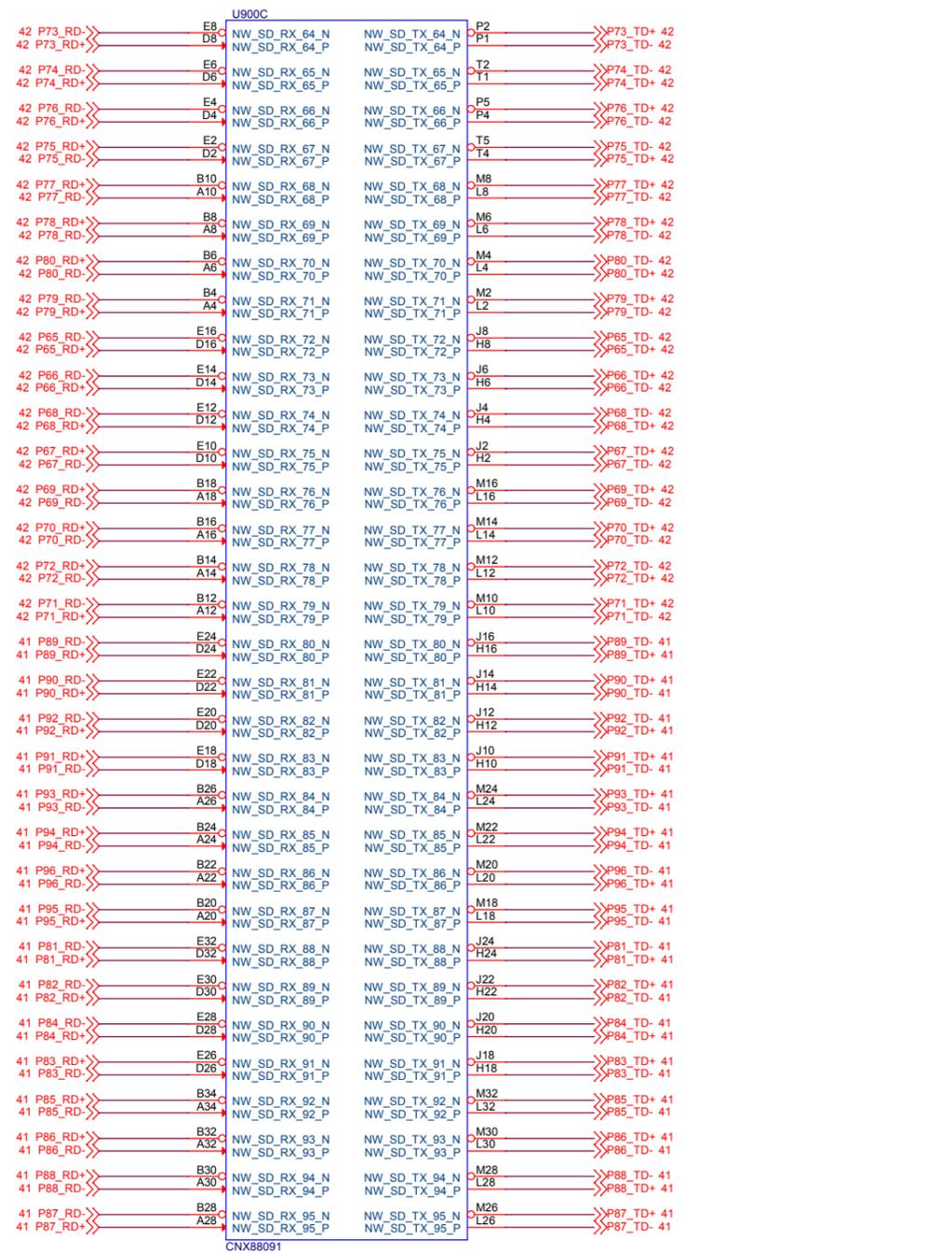


# XPLIANT-CONTROL INTERFACE

REV1 CHANGE NOTE : Deleted SMAs J4217,J4218,J4219,J4220

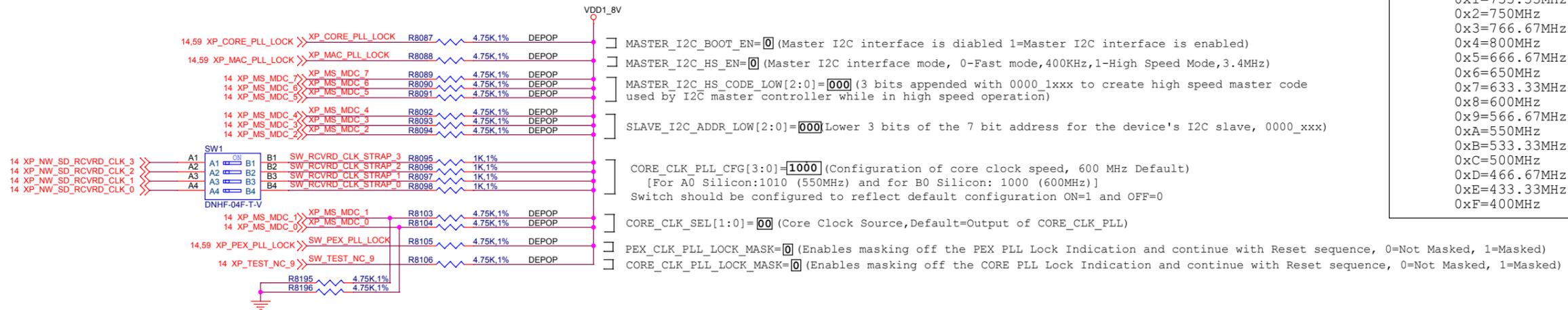


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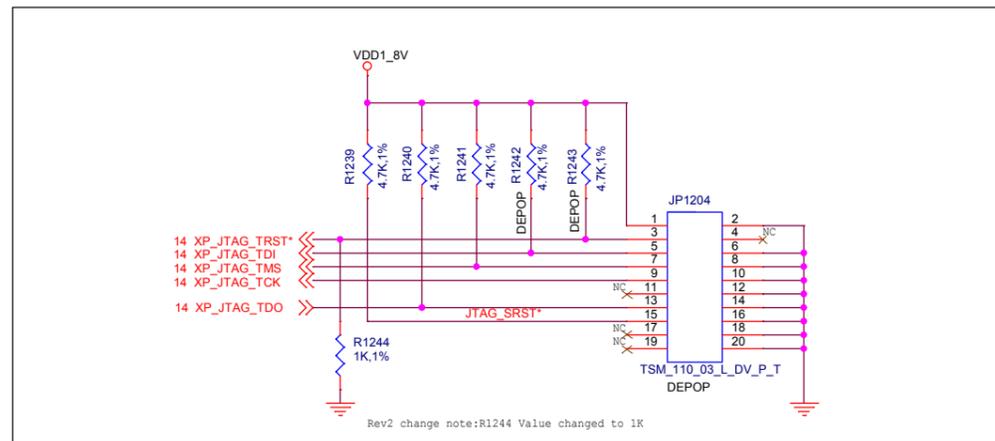
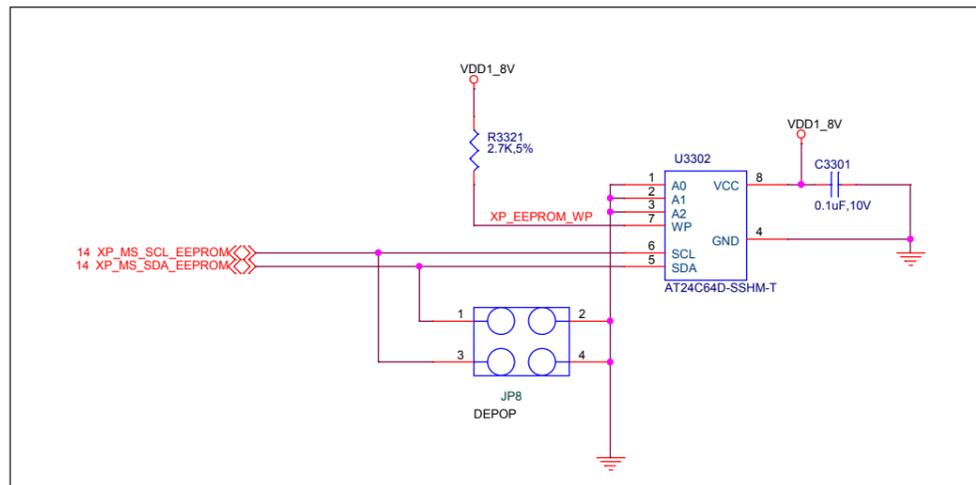
STRAPPING OPTIONS  
(ALL THESE PINS HAVE 50K INTERNAL PULL DOWN)



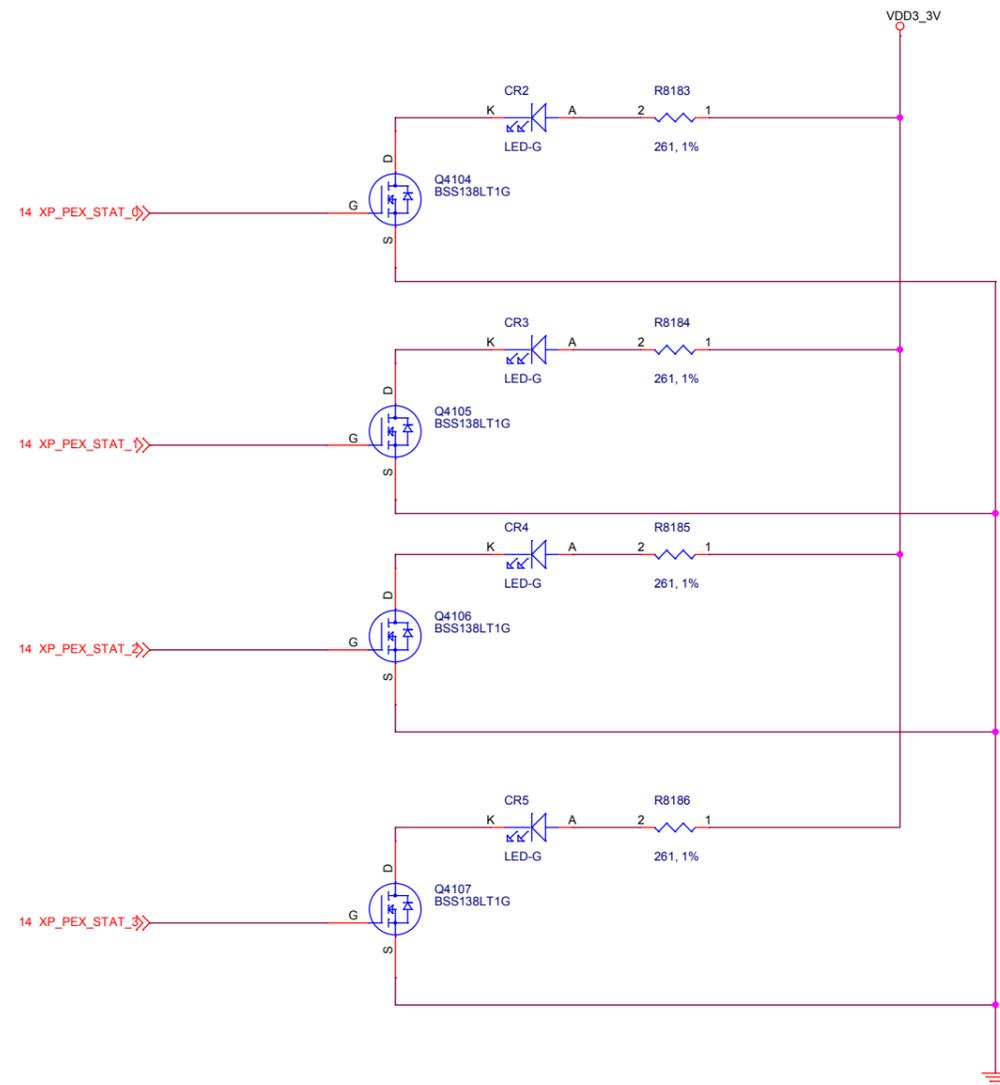
**CORE CLOCK FREQUENCY SWITCH CONFIG**

0x0	= 700MHz
0x1	= 733.33MHz
0x2	= 750MHz
0x3	= 766.67MHz
0x4	= 800MHz
0x5	= 666.67MHz
0x6	= 650MHz
0x7	= 633.33MHz
0x8	= 600MHz
0x9	= 566.67MHz
0xA	= 550MHz
0xB	= 533.33MHz
0xC	= 500MHz
0xD	= 466.67MHz
0xE	= 433.33MHz
0xF	= 400MHz

REV1 CHANGE NOTE : SW1 part number changed to DNHf-04F-T-V from Dawning.

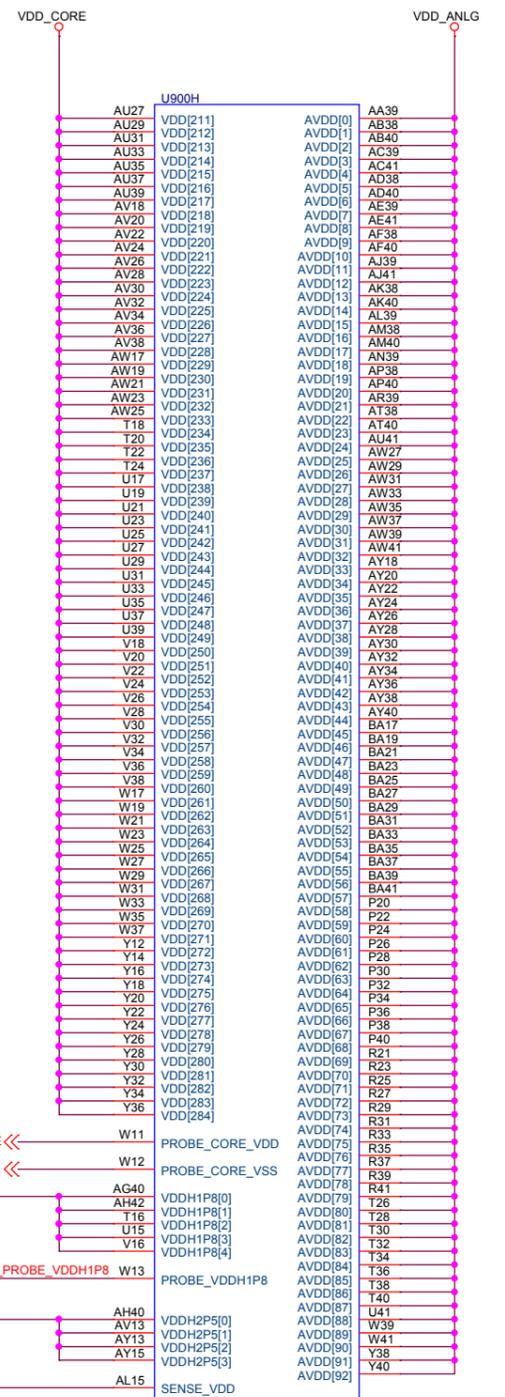
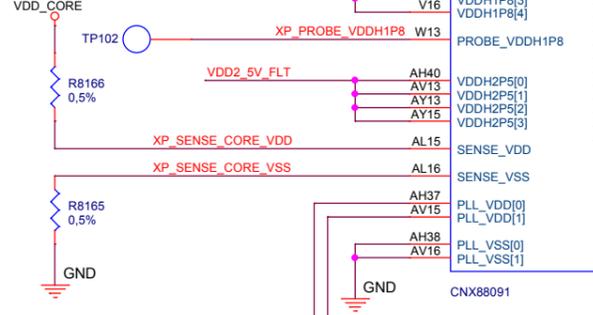
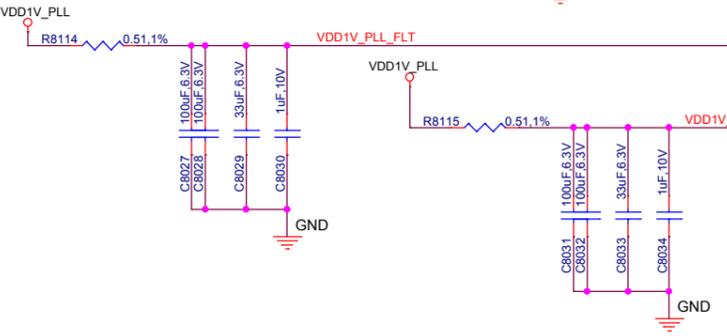
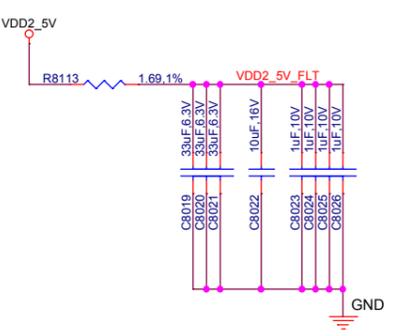
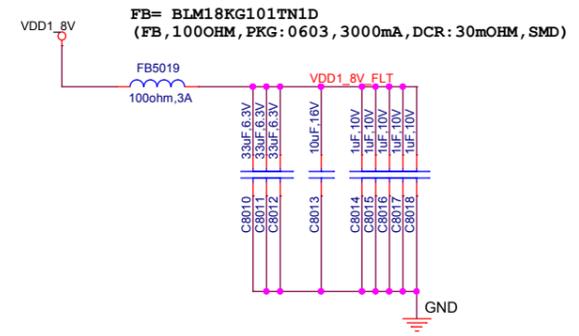
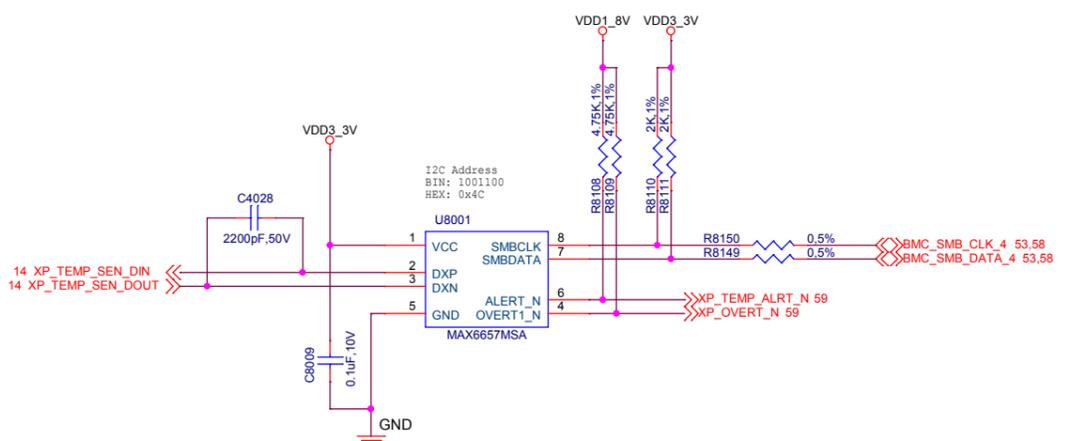
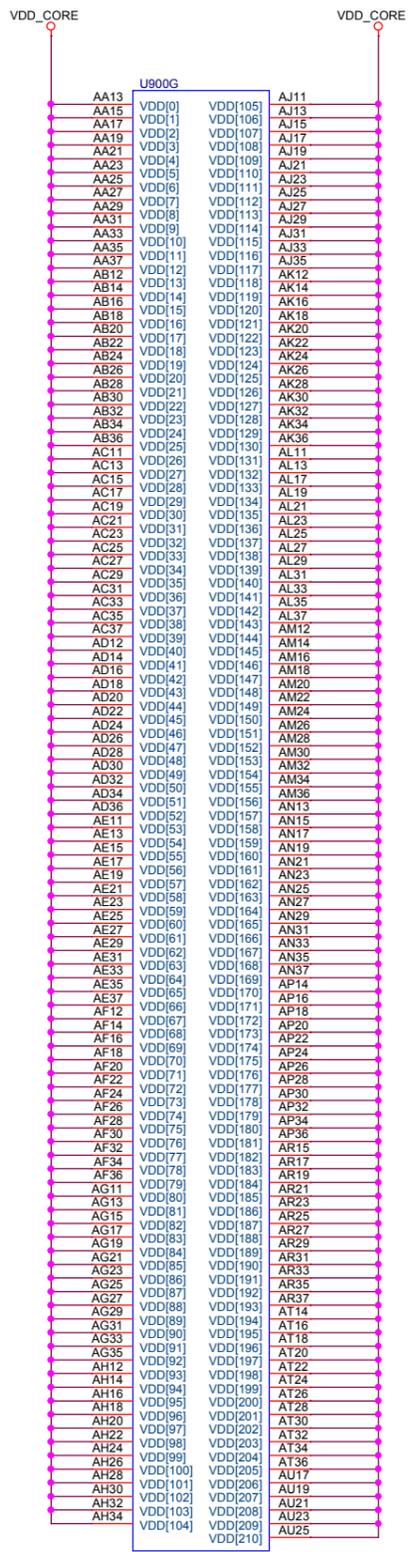


PEX STATUS LEDES



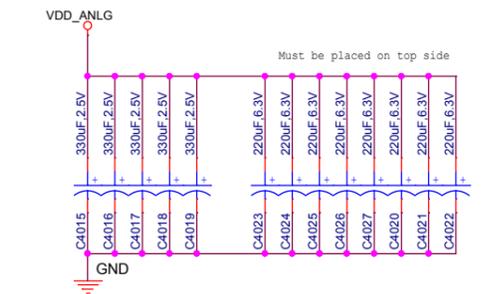
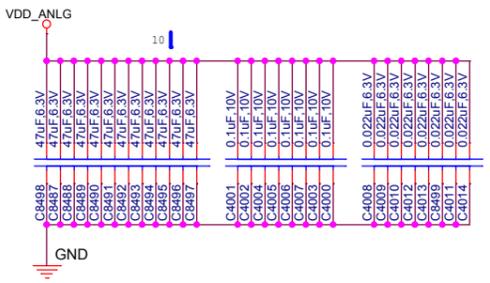
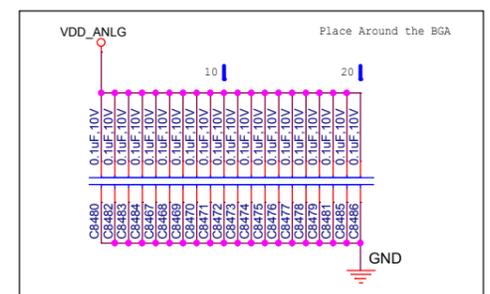
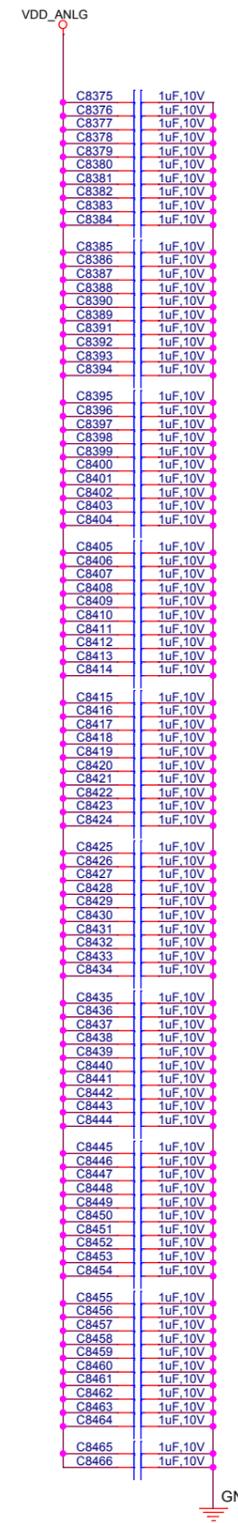
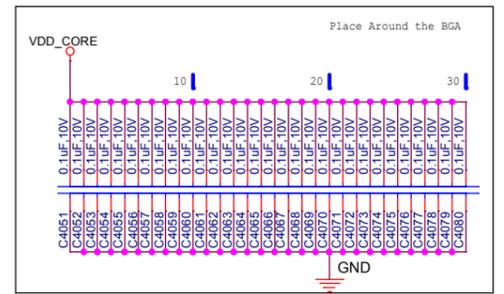
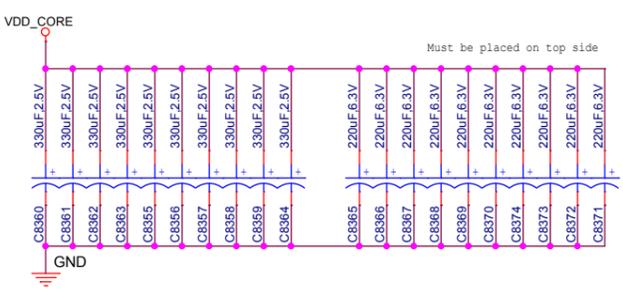
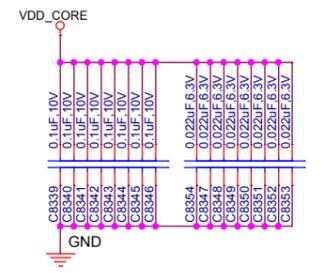
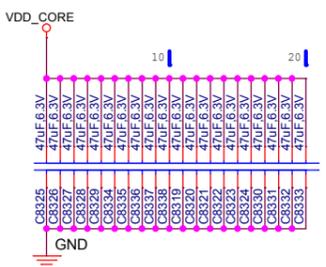
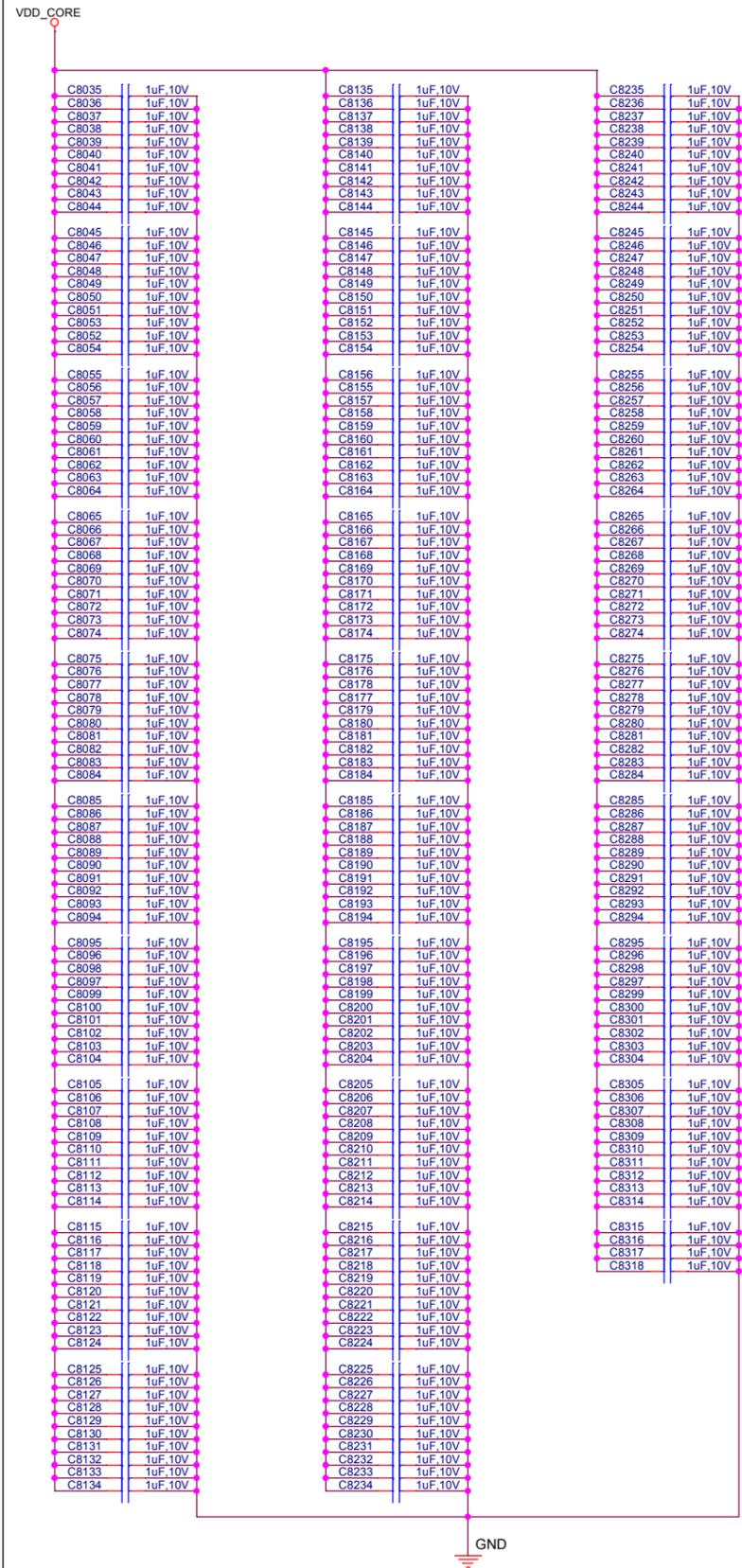
**XPLIANT-STRAPPING & JTAG**

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# XPLIANT-CORE & AVDD POWER

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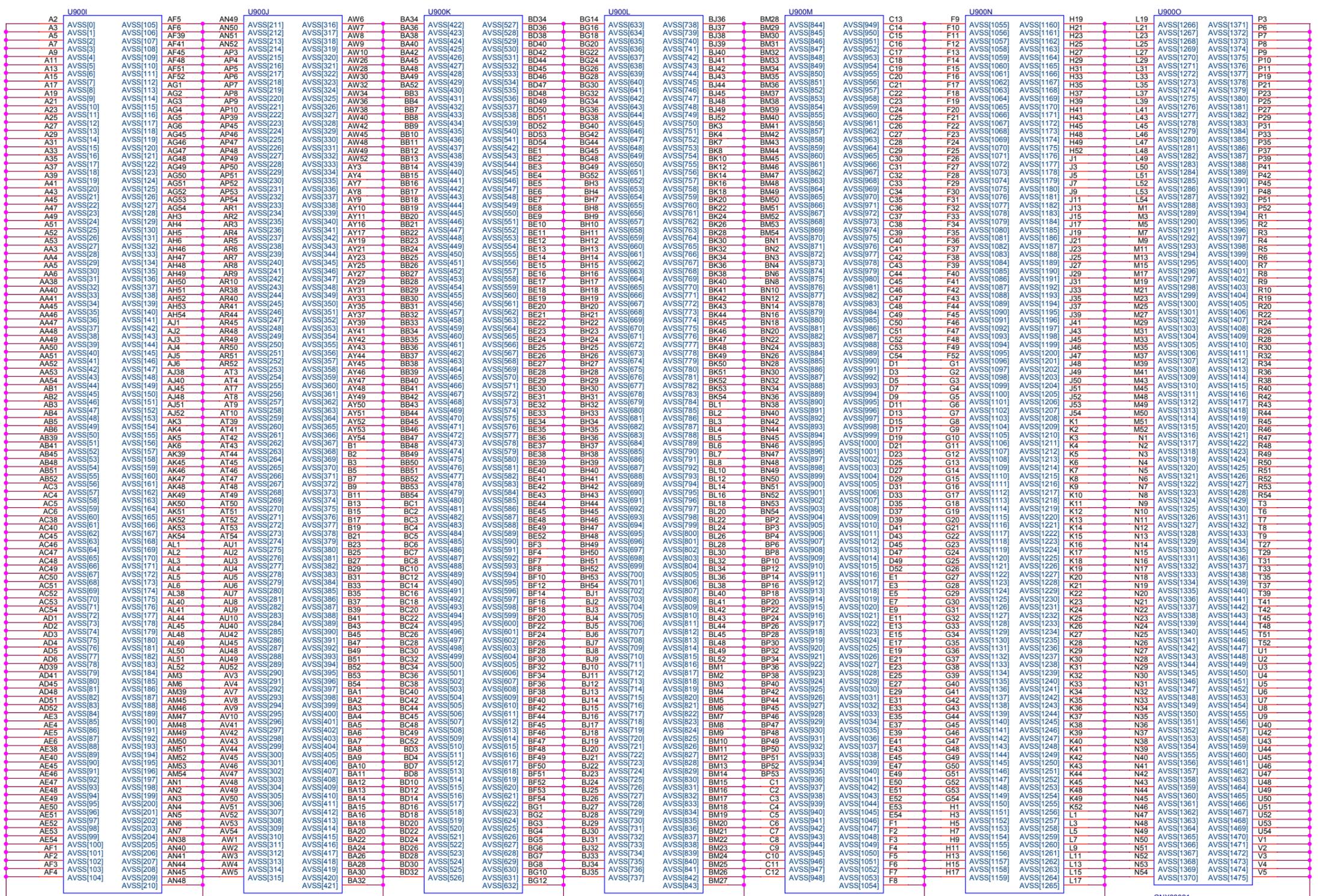


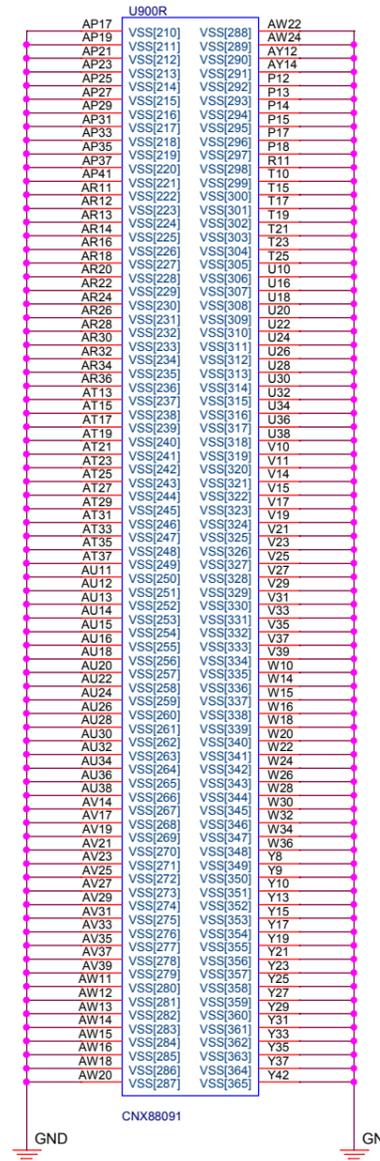
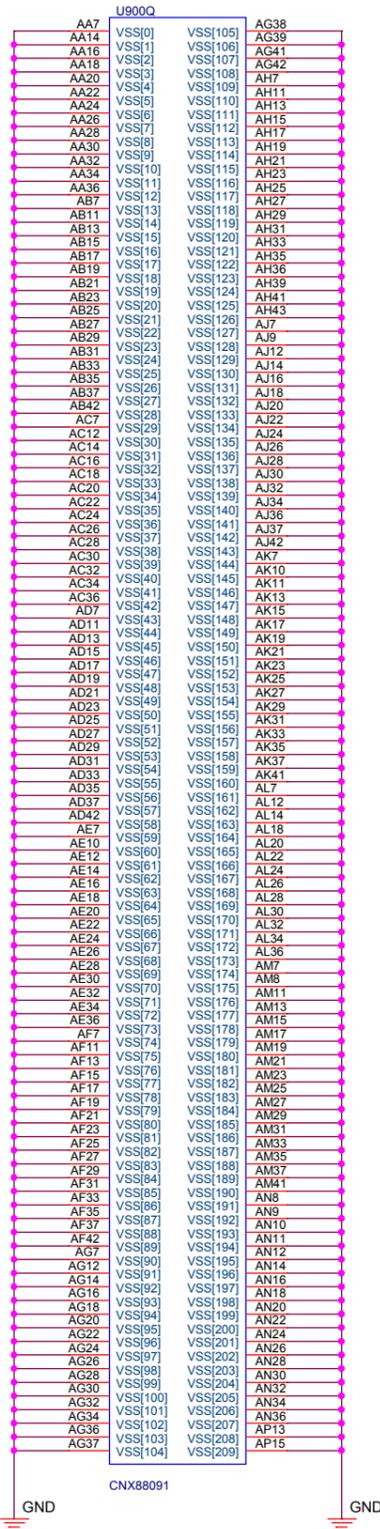
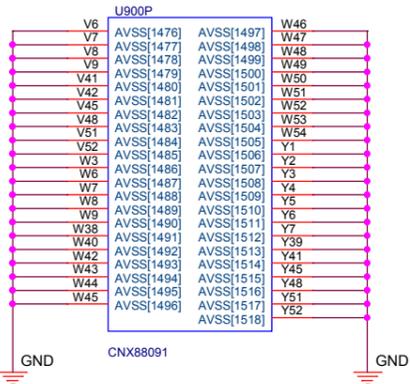
NOTE: KC1 and KC2 NEED TO BE PLACED AT AN OPTIMAL LOCATION NEAR LOAD AND ROUTE DIFFERENTIALLY

REV1 CHANGE NOTE : Changed C4015,C4016,C4017,C4018,C4019,C8355,C8356,C8357,C8358,C8359,C8360,C8361,C8362,C8363,C8364 with 330UF,2.5V PART (EEF-HX0E331R4 part from Panasonic)

# XPLIANT-DECOUPLING CAPS

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**XPLIANT-GND**

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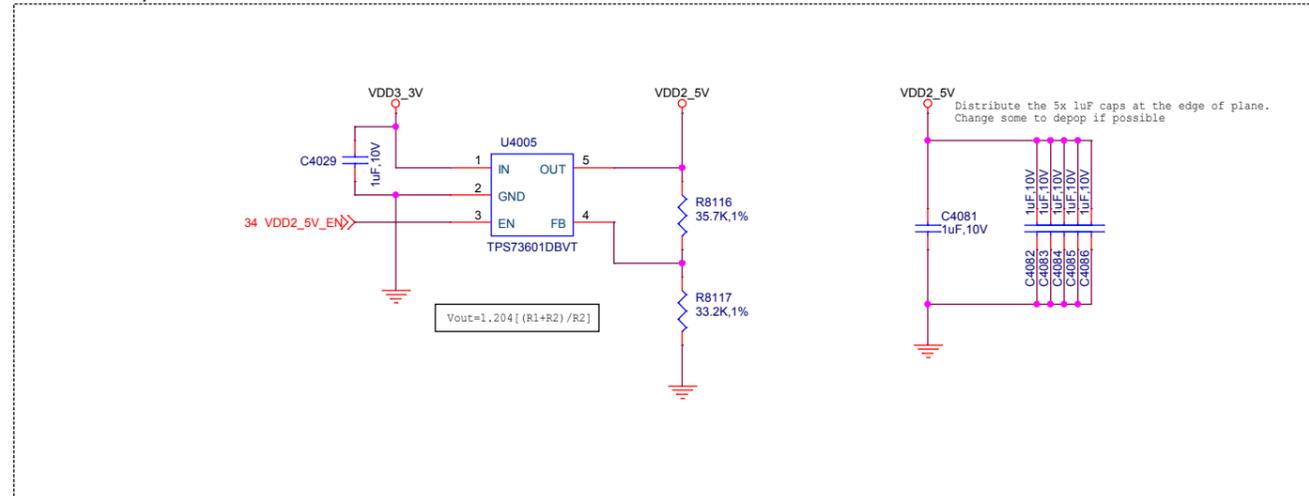
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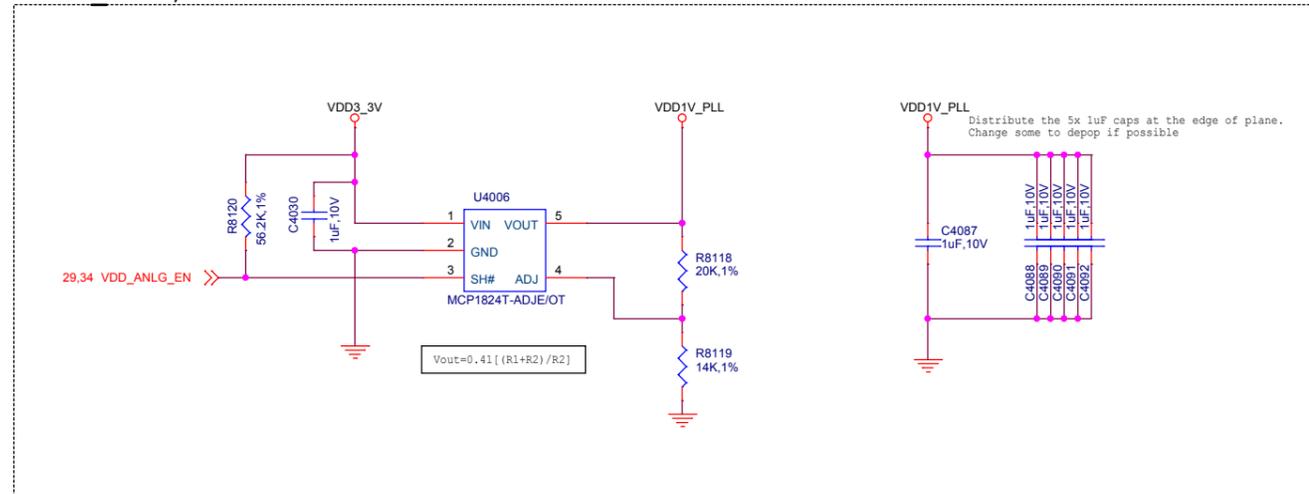
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**PS 2.5V , 0.4A**

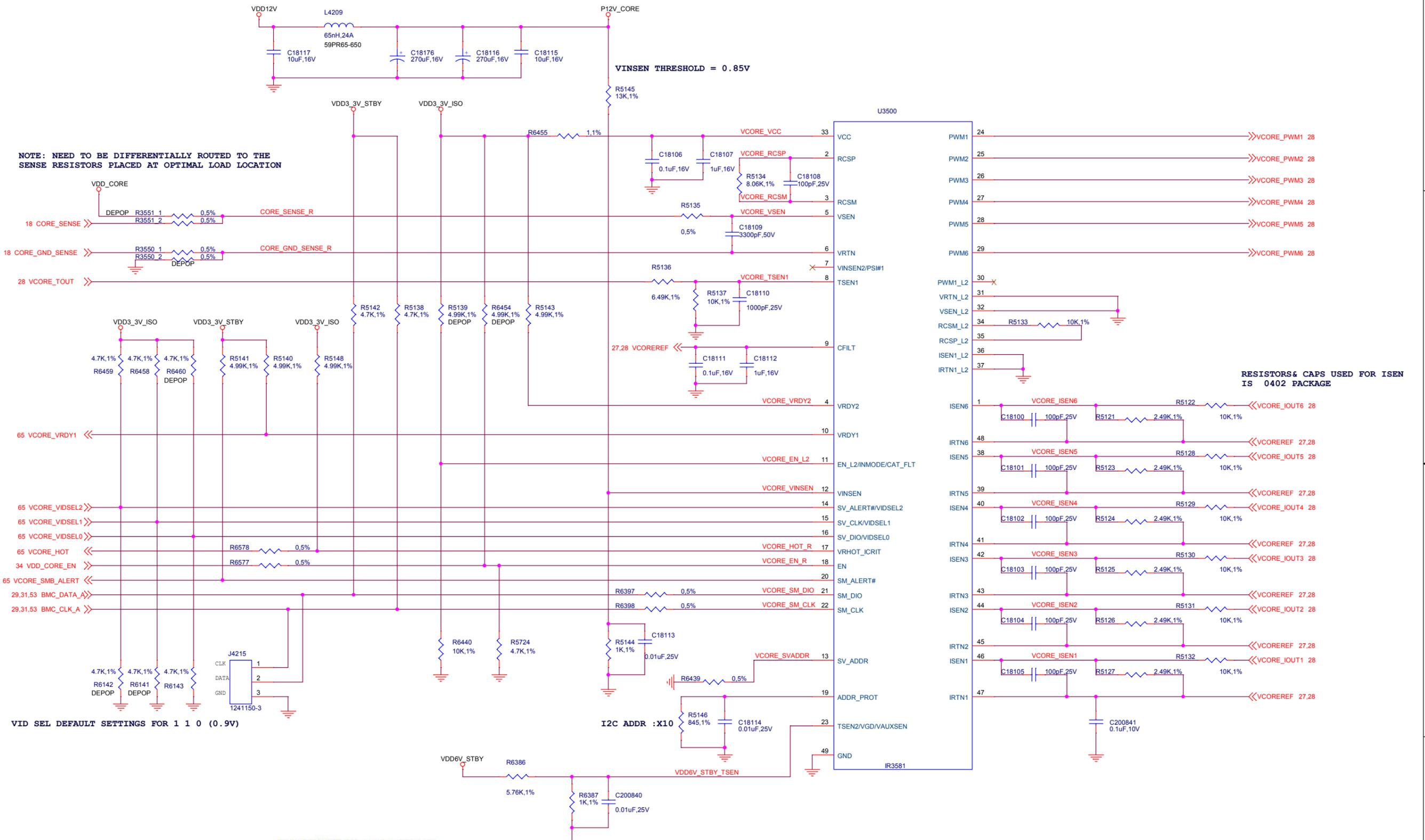


**PS 1V PLL , 0.3A**



**PS-2.5V & 1V PLL**

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VINSEN THRESHOLD = 0.85V

NOTE: NEED TO BE DIFFERENTIALLY ROUTED TO THE SENSE RESISTORS PLACED AT OPTIMAL LOAD LOCATION

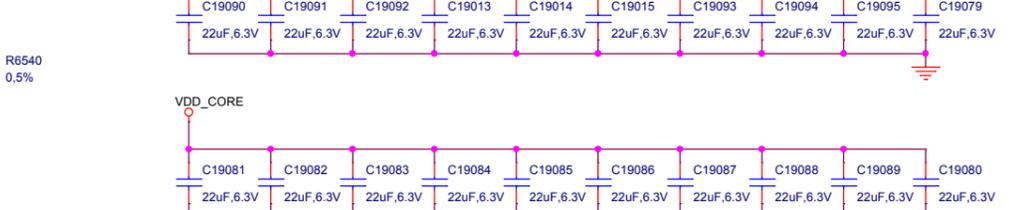
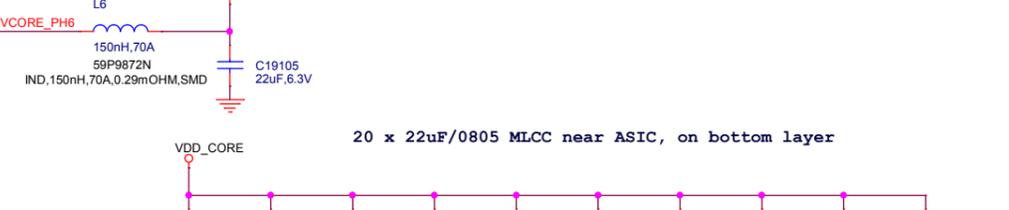
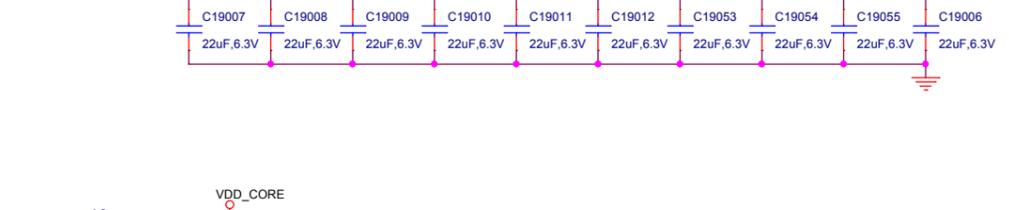
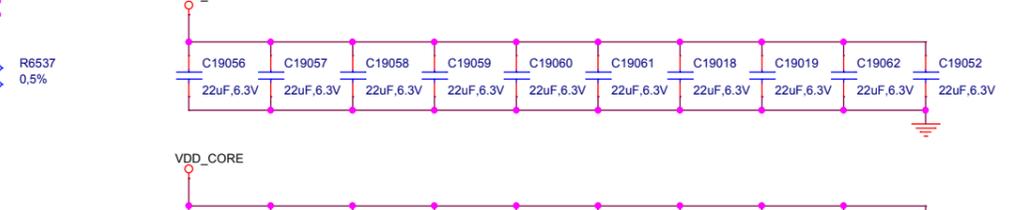
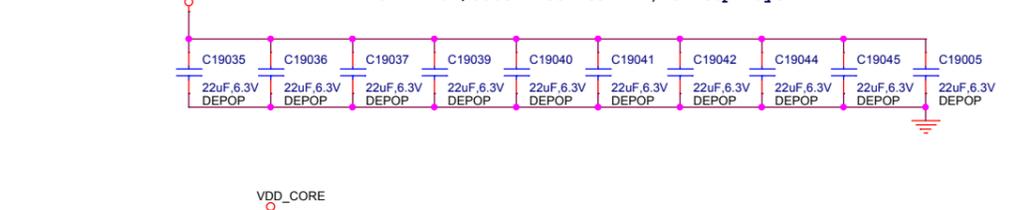
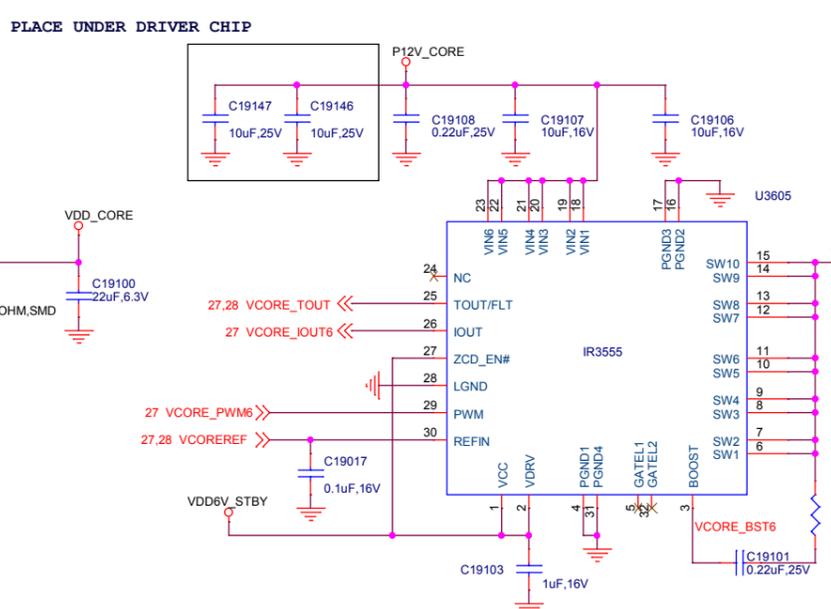
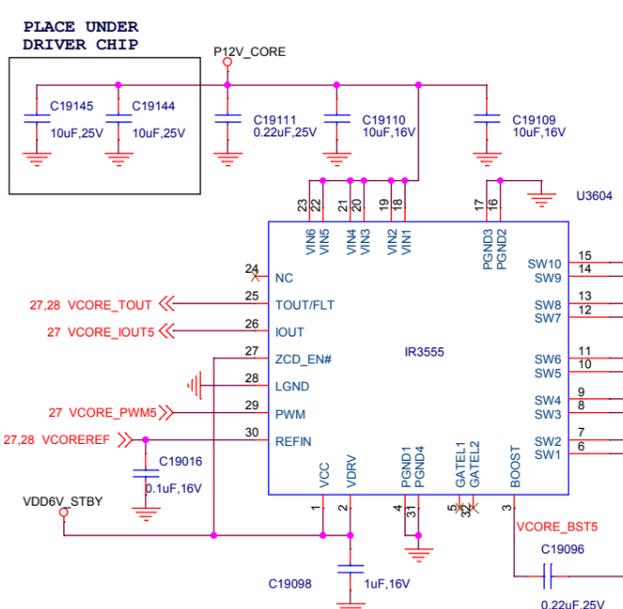
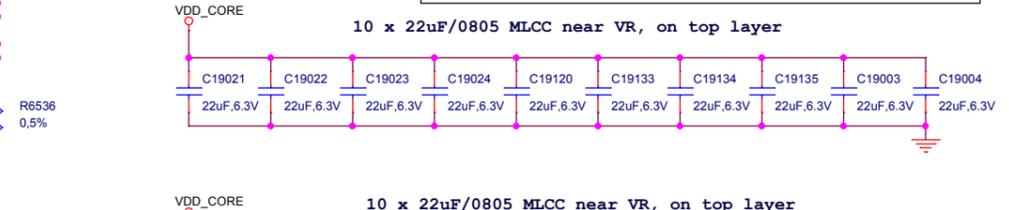
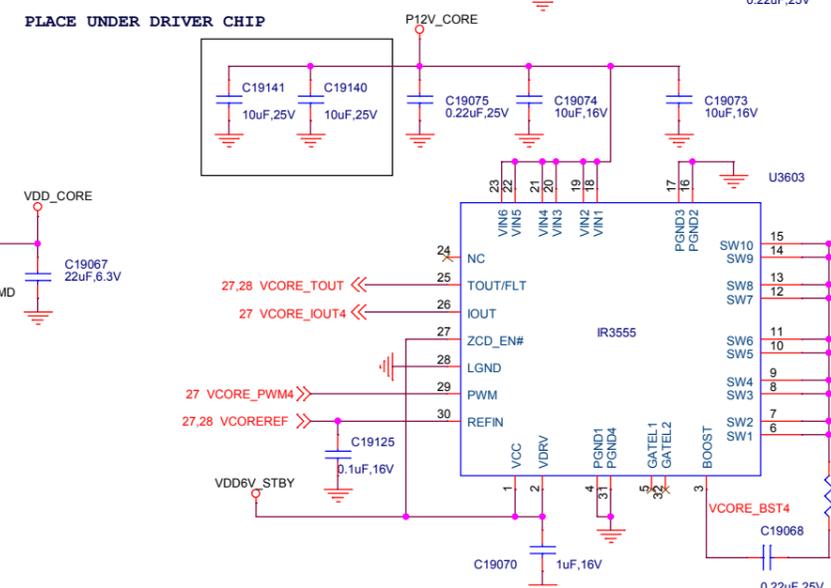
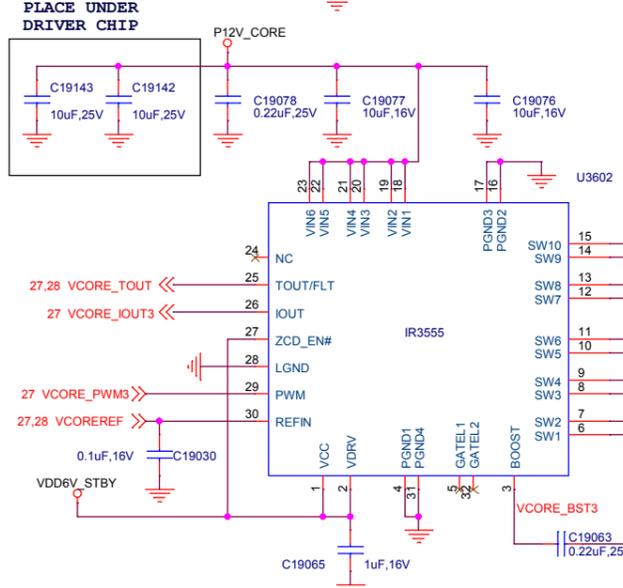
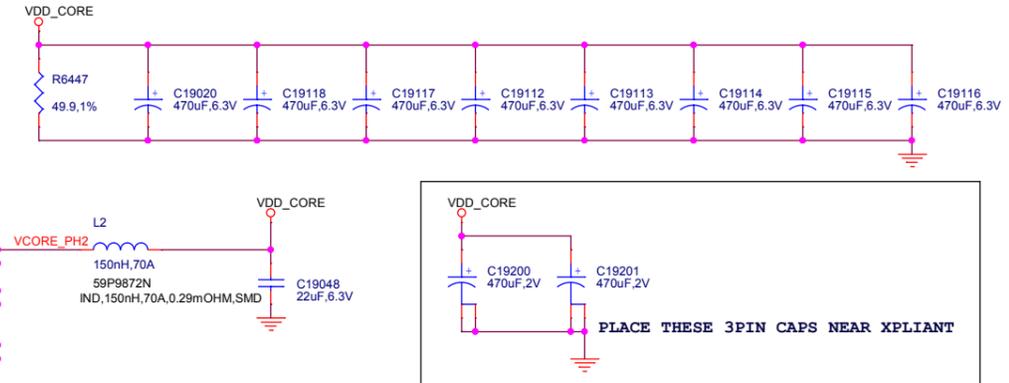
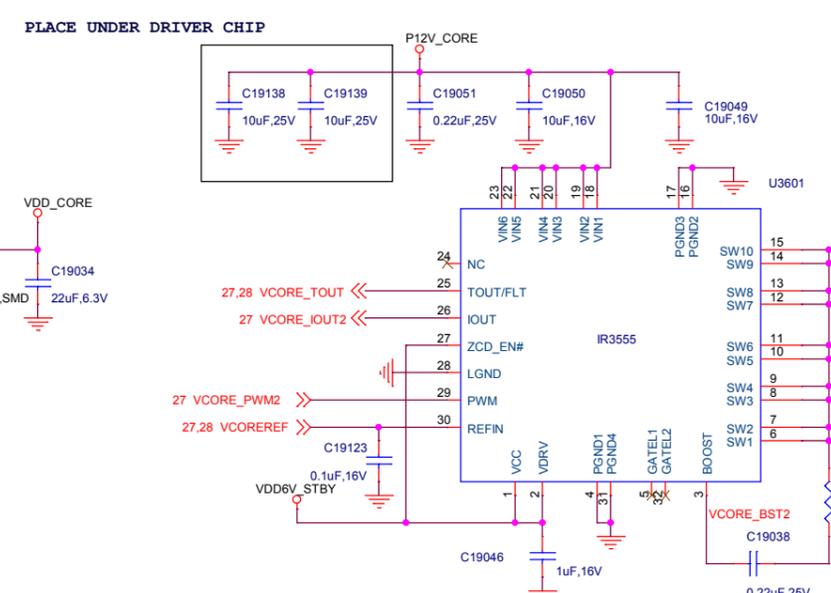
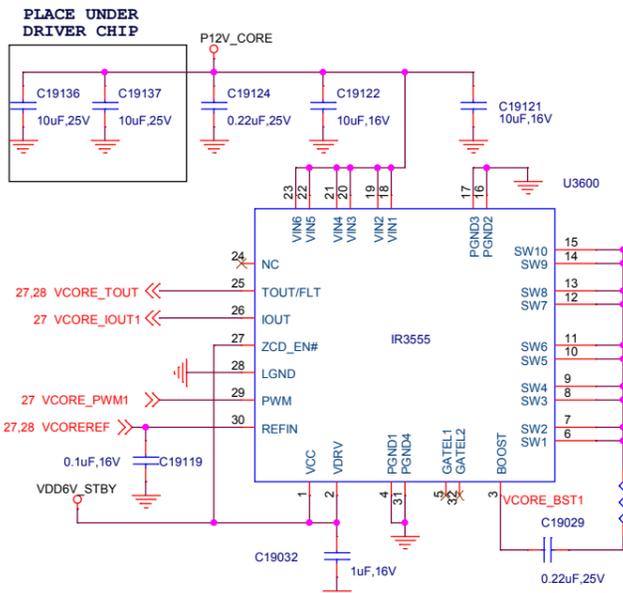
RESISTORS & CAPS USED FOR ISEN IS 0402 PACKAGE

VID SEL DEFAULT SETTINGS FOR 1 1 0 (0.9V)

TABLE 3: VAUXSEN TURN-ON/OFF VOLTAGES

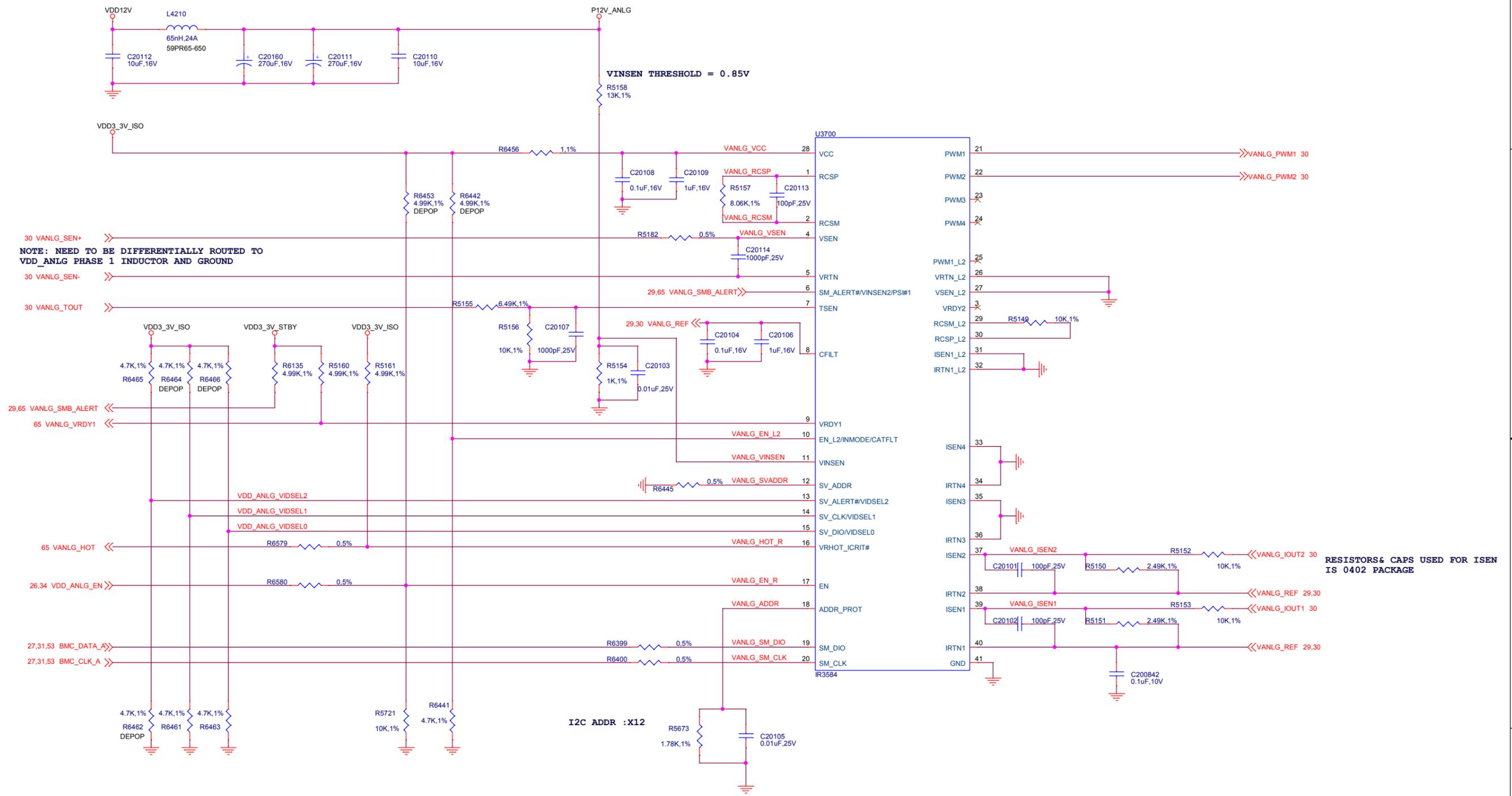
R1	VAUX_on	VAUX_off
KΩ	Volt	Volt
5.77	4.50	3.97

# PS0.9V-CORE



# PS0.9V-CORE

<b>CAVIUM</b>		
<b>WEDGE100C</b>		
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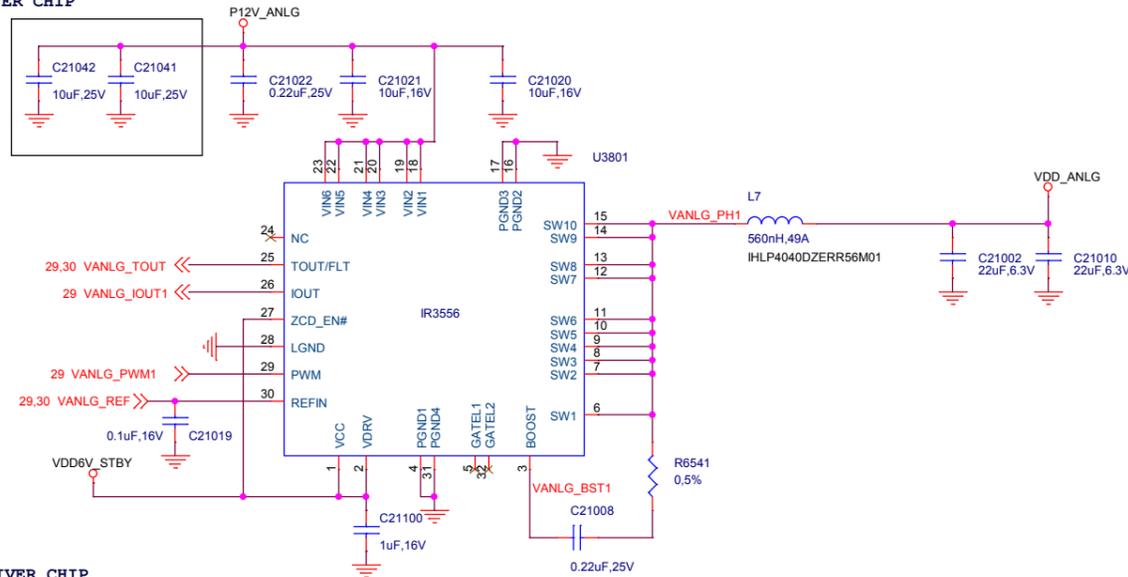
NOTE: NEED TO BE DIFFERENTIALLY ROUTED TO VDD\_ANLG PHASE 1 INDUCTOR AND GROUND

RESISTORS & CAPS USED FOR ISEN IS 0402 PACKAGE

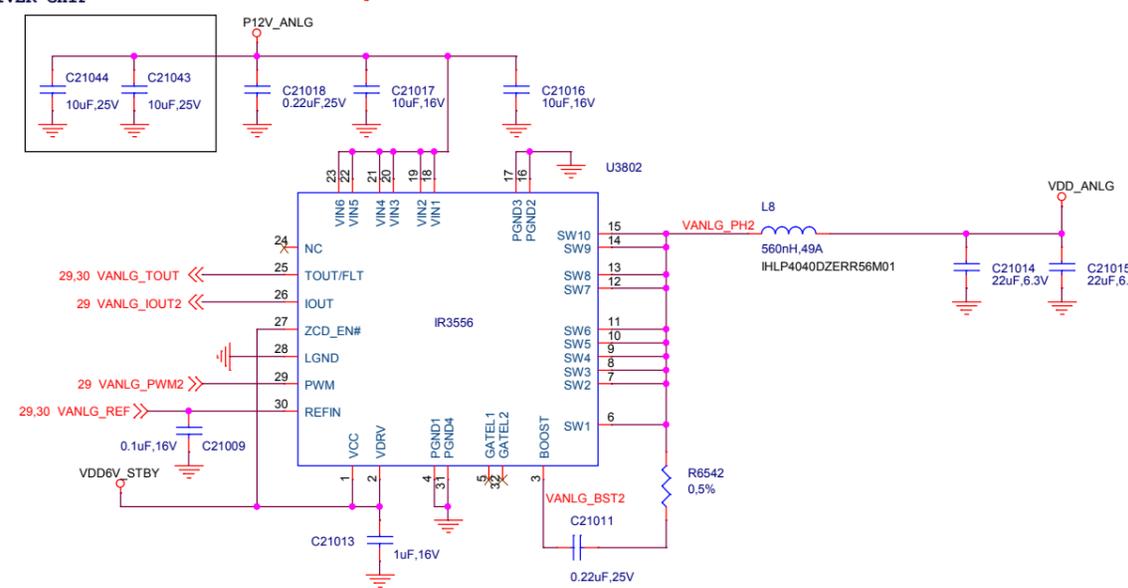
# PS1V-ANLG

Title			CAVIUM		
Document Number			WEDGE100C		
Size	80-00010-03	Rev	2.0		
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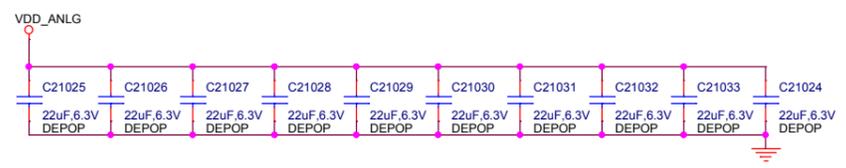
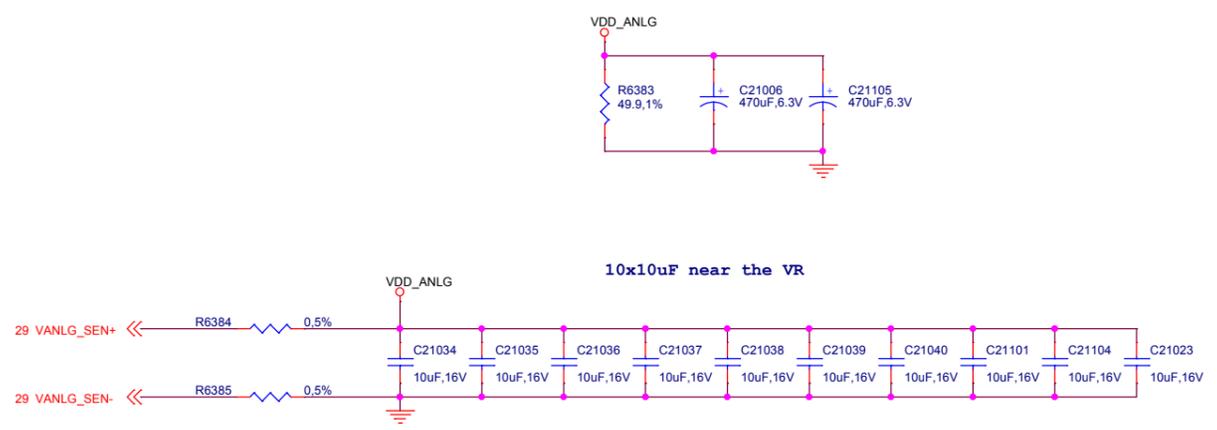
PLACE UNDER DRIVER CHIP



PLACE UNDER DRIVER CHIP

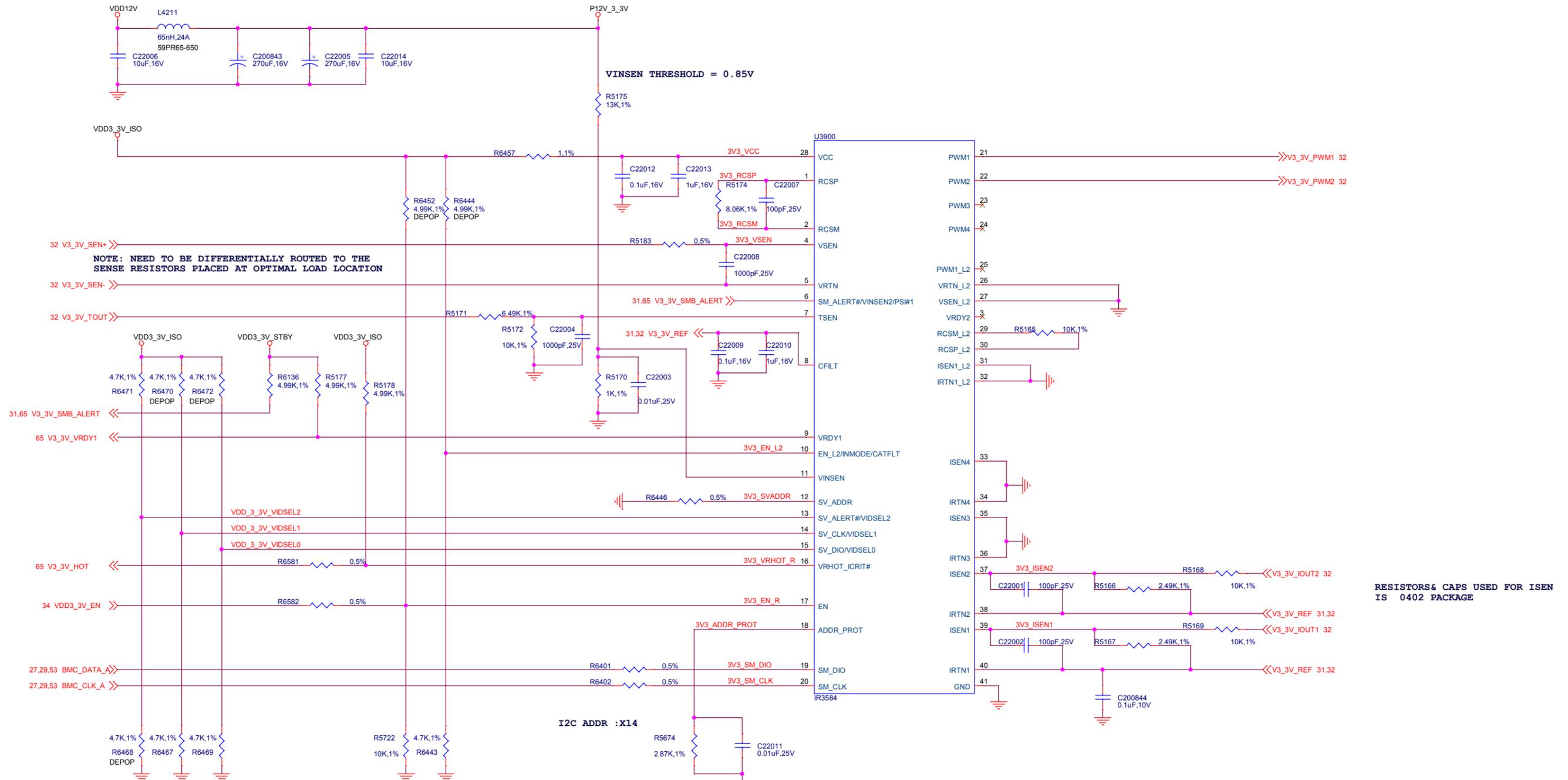


NOTE: THESE RESISTORS NEED TO BE PLACED AT AN OPTIMAL LOCATION NEAR LOAD AND ROUTE DIFFERENTIALLY



# PS1V-ANLG

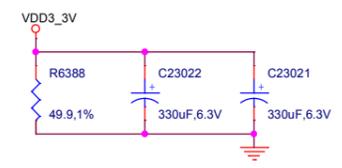
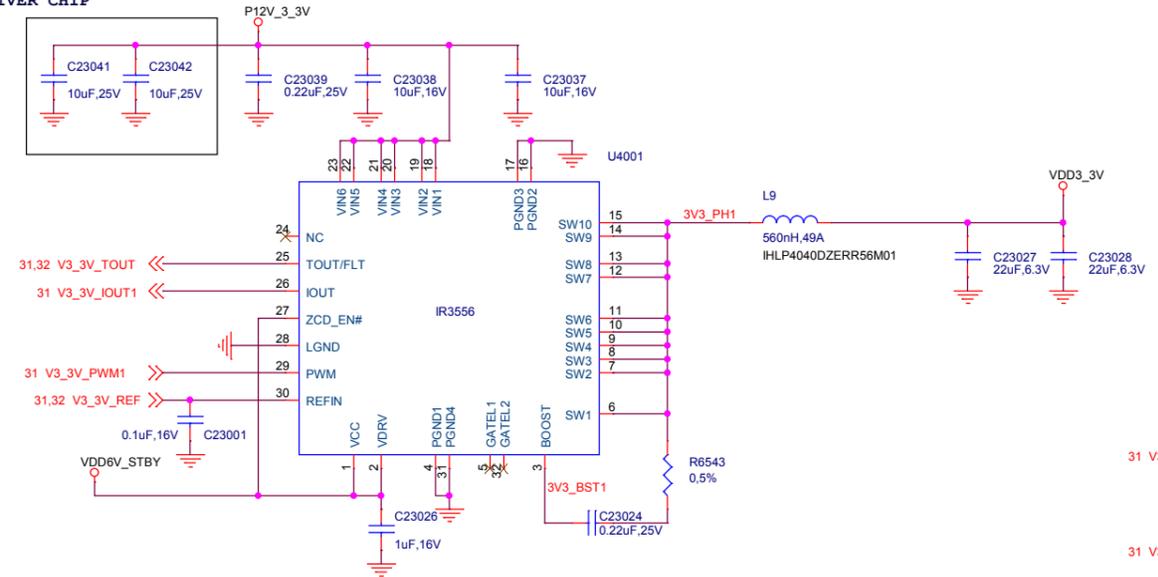
CAVIUM		
Title	WEDGE100C	
Size	Document Number	Rev
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# PS3.3V

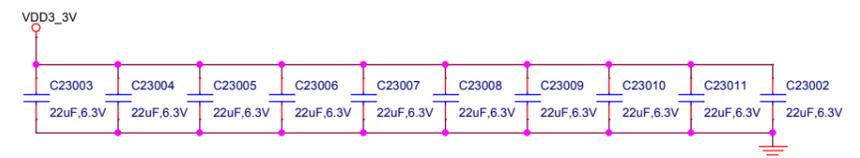
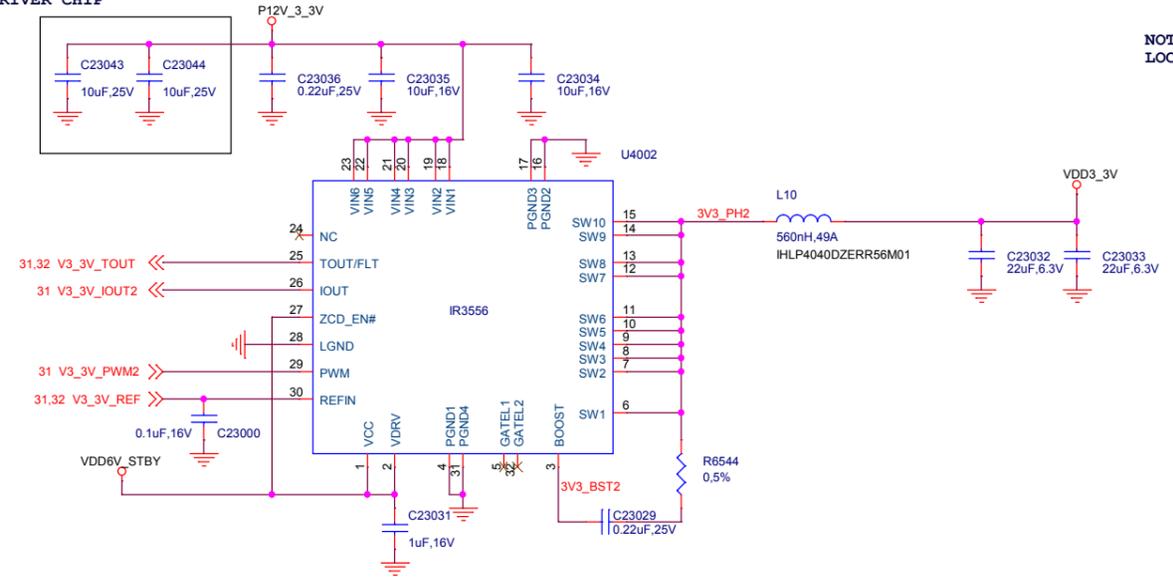
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Title <b>WEDGE100C</b>		
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PLACE UNDER DRIVER CHIP

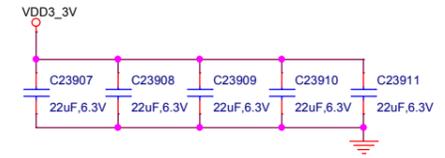


NOTE: THESE RESISTORS NEED TO BE PLACED AT AN OPTIMAL LOCATION NEAR LOAD AND ROUTE DIFFERENTIALLY

PLACE UNDER DRIVER CHIP



CHANGE NOTE: Populated C23002, C23003, C23004, C23005, C23006, C23006, C23007, C23008, C23009, C23010, C23011

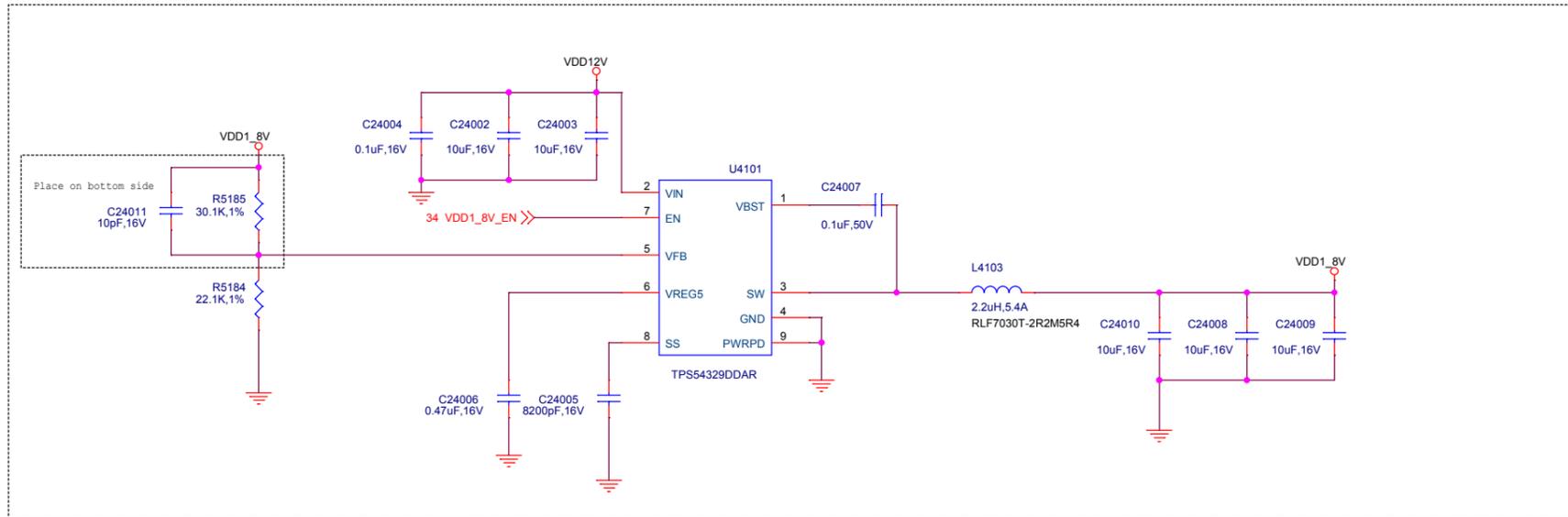


CHANGE NOTE: Added C23907, C23908, C23909, C23910, C23911

# PS3.3V

Title		
CAVIUM		
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**PS 1.8V ,3A**



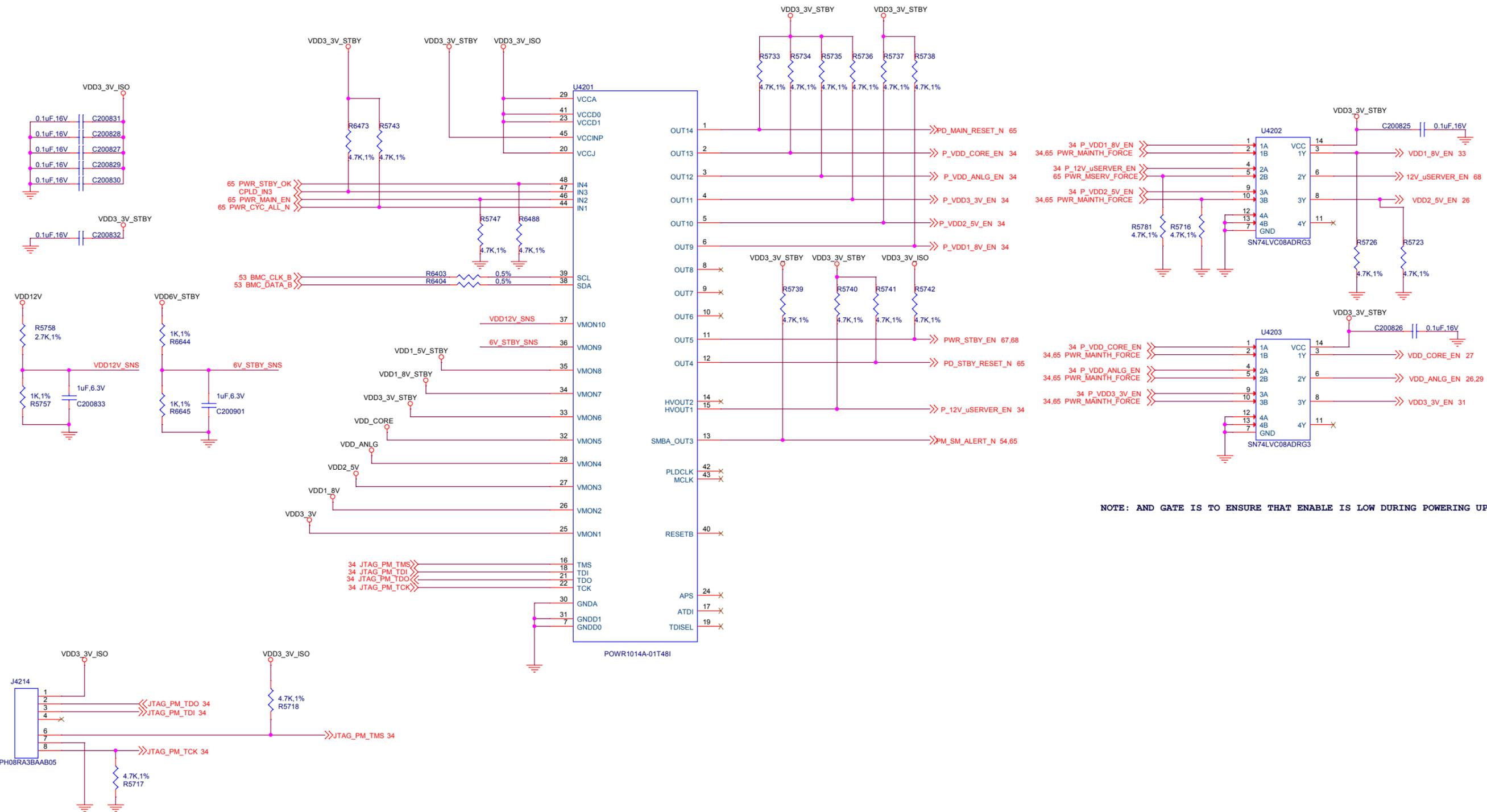
**VIN =12V**  
**Device =TPS54329DDAR**  
**Vout =1.8V**  
**Ioutmax = 3A**  
**Softstart = 1.15ms**  
**L= RLF7030T-2R2M5R4 (2.2uH,5.4A,DCR=10mOhms)**  
**Cout=GRM21BR61C106KE15L (CER,10UF,0805,16V)**

**PS 1.8V**

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NOTE: PWR\_STBY\_OK = P1\_2V\_STBY\_OK

A PULLDOWN IS PROVIDED TO PWR\_STBY\_OK SO THAT TILL CPLD IS PROGRAMMED, PWR\_STBY\_OK WILL BE LOW

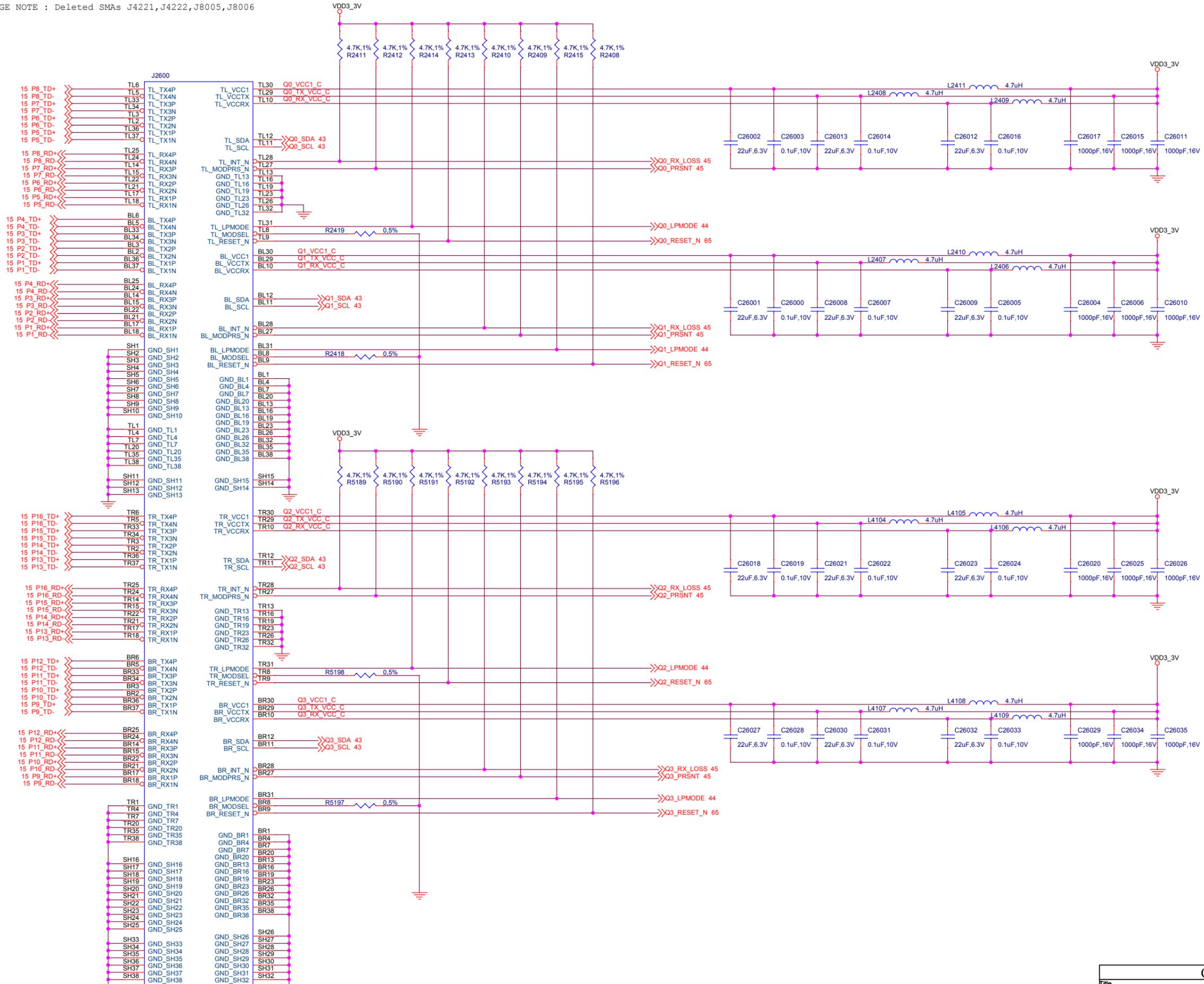


NOTE: AND GATE IS TO ENSURE THAT ENABLE IS LOW DURING POWERING UP

CHANGE NOTE: J4214 changed with 8pin connector PH08RA3BAAB05  
Pin5 deleted after acton feedback

# POWER MANAGEMENT

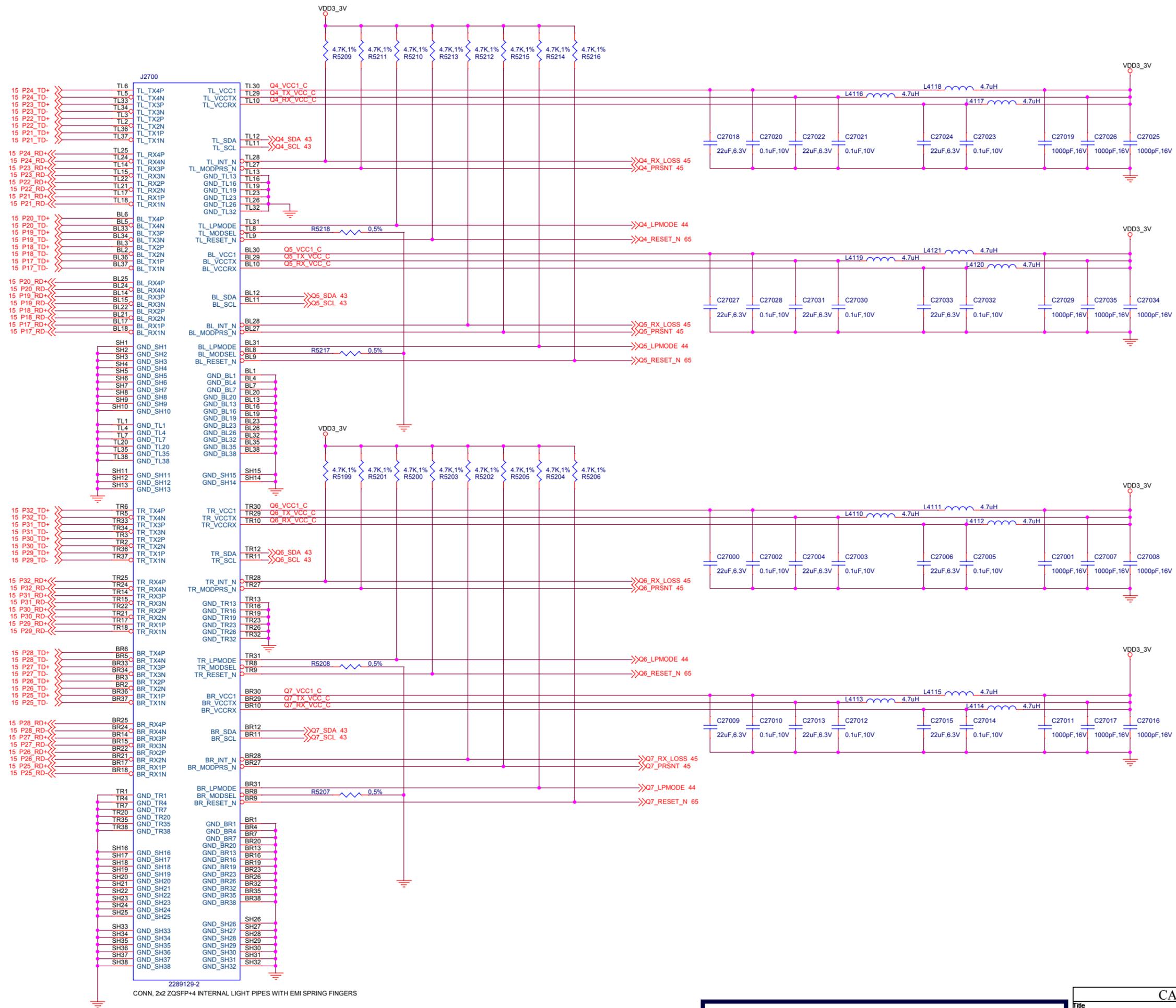
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Title		
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2289129-2  
CONN, 2x2 QSFP+4 INTERNAL LIGHT PIPES WITH EMI SPRING FINGERS

# QSFP CONNECTOR 2X2

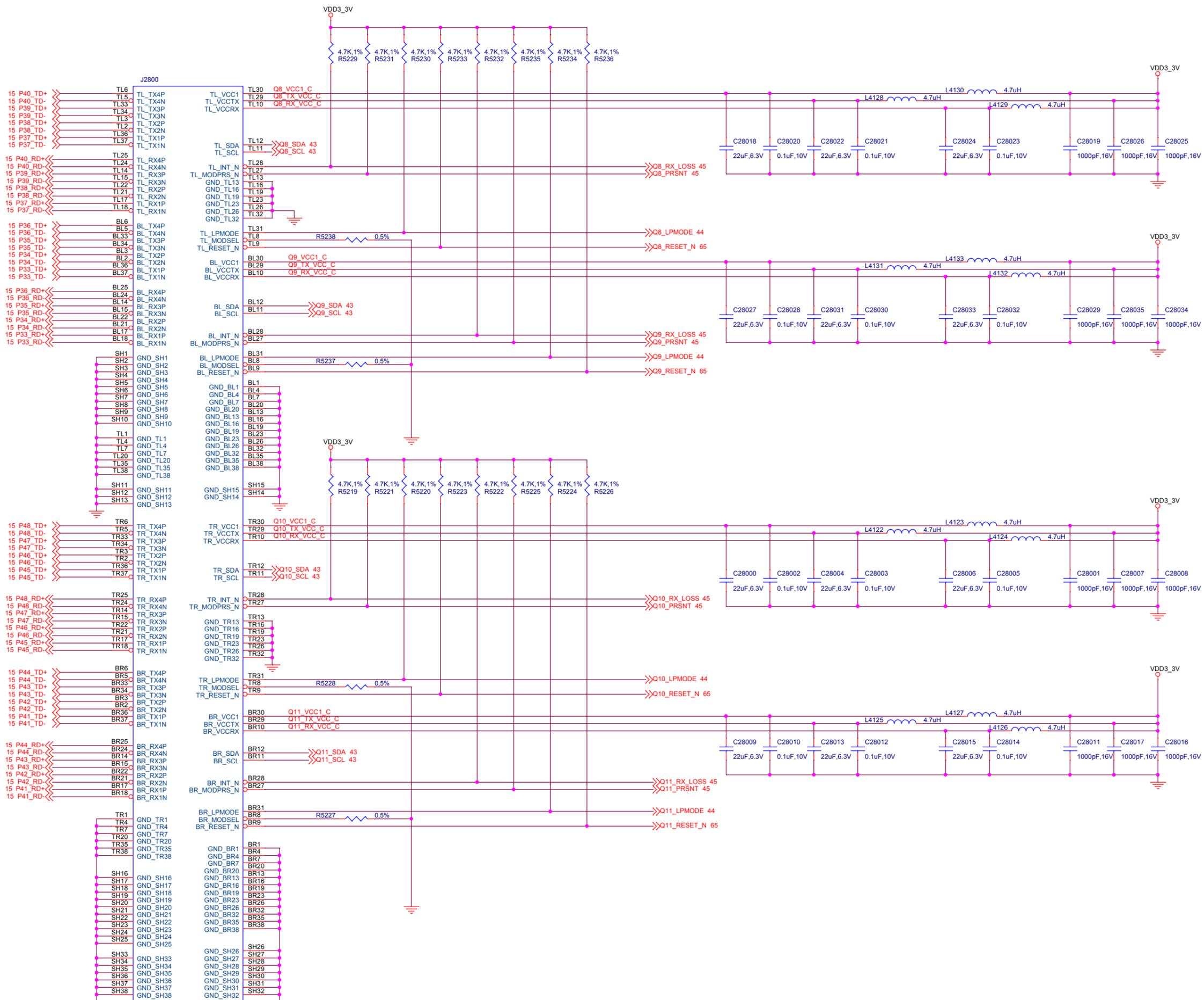
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Size			WEDGE100C
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2289129-2  
CONN, 2x2 QSFP+4 INTERNAL LIGHT PIPES WITH EMI SPRING FINGERS

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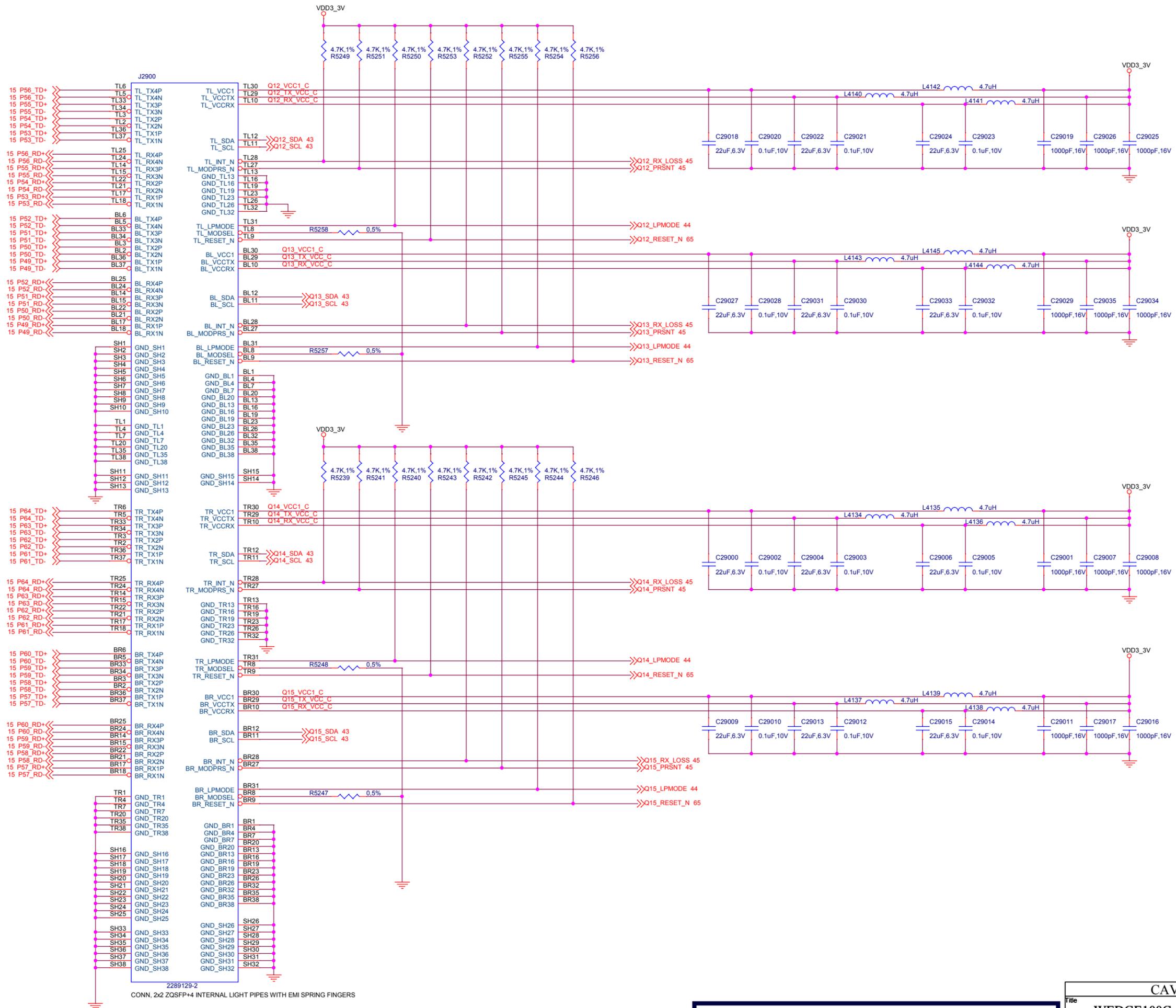
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Title	WEDGE100C	
Size	Document Number	Rev
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2289129-2  
CONN, 2x2 QSFP+4 INTERNAL LIGHT PIPES WITH EMI SPRING FINGERS

# QSFP CONNECTOR 2X2

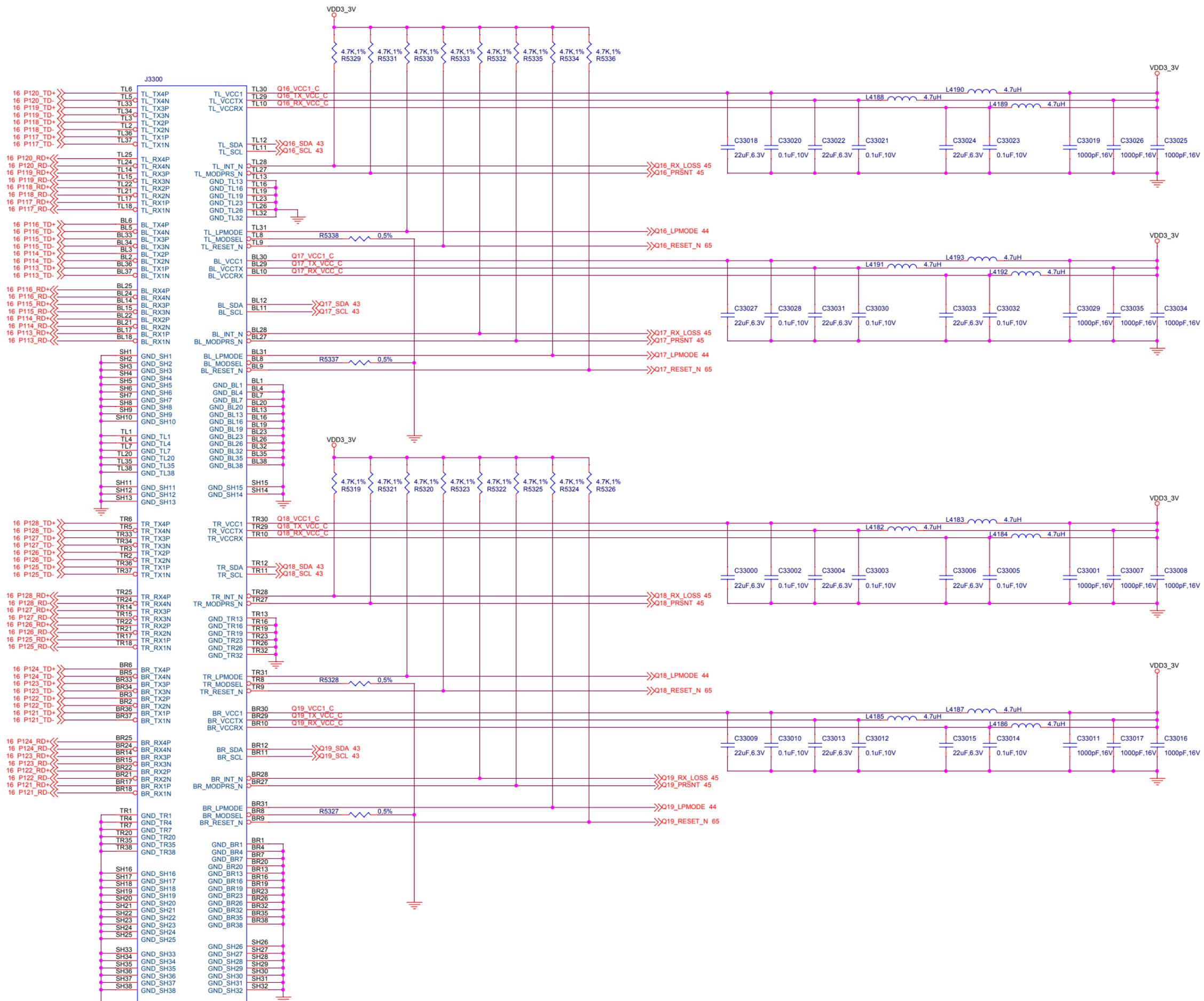
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Title	Document Number	
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C	2.0	



2289129-2  
CONN, 2x2 QSFP+4 INTERNAL LIGHT PIPES WITH EMI SPRING FINGERS

# QSFP CONNECTOR 2X2

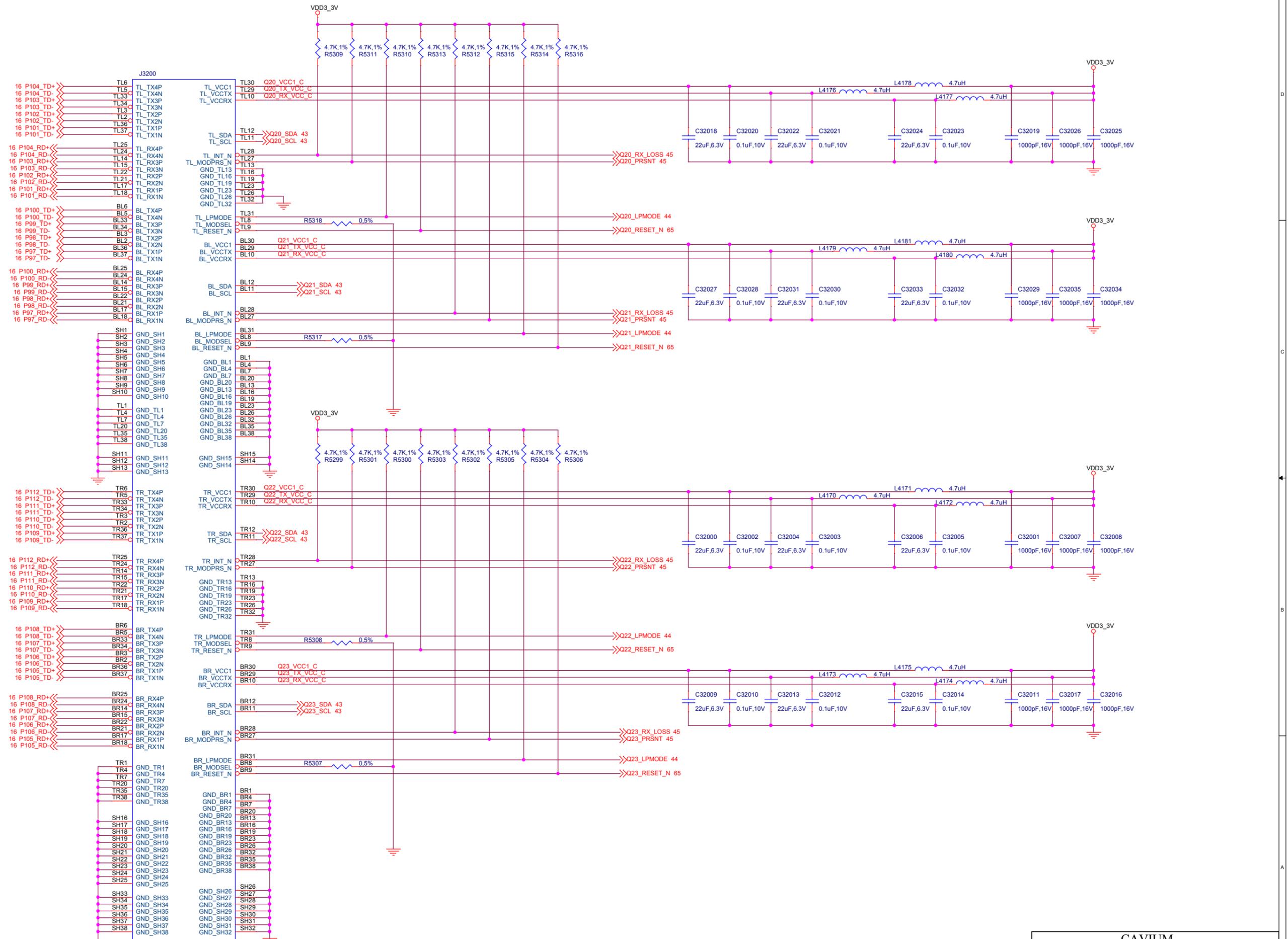
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Title <b>WEDGE100C</b>		
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2289129-2  
CONN, 2x2 ZQSPF+4 INTERNAL LIGHT PIPES WITH EMI SPRING FINGERS

# QSFP CONNECTOR 2X2

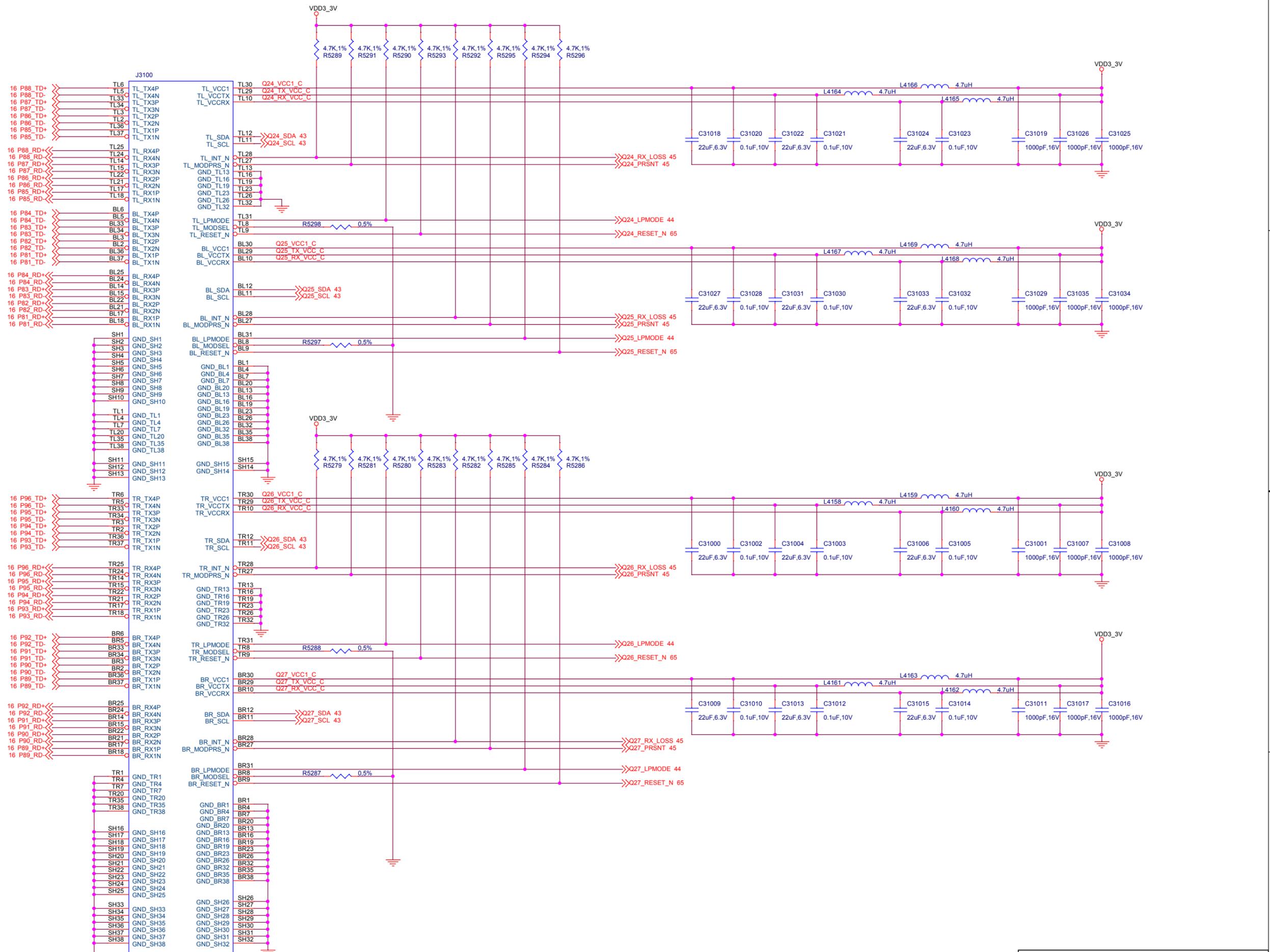
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2289129-2  
CONN, 2x2 QSFP+4 INTERNAL LIGHT PIPES WITH EMI SPRING FINGERS

# QSFP CONNECTOR 2X2

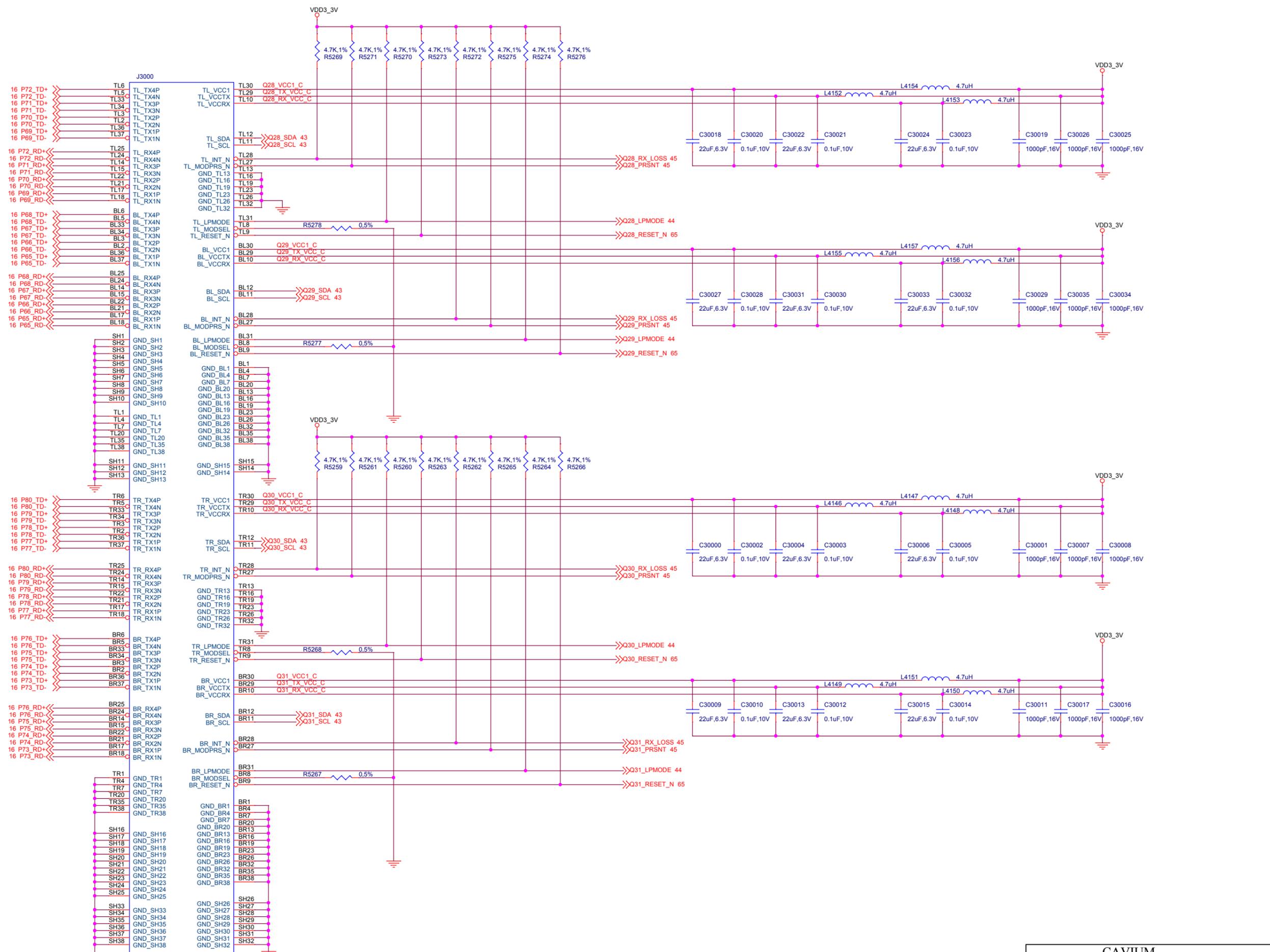
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<b>Size</b> C	<b>Document Number</b> 80-0010-03	<b>Rev</b> 2.0
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2289129-2  
CONN, 2x2 QSFP+4 INTERNAL LIGHT PIPES WITH EMI SPRING FINGERS

# QSFP CONNECTOR 2X2

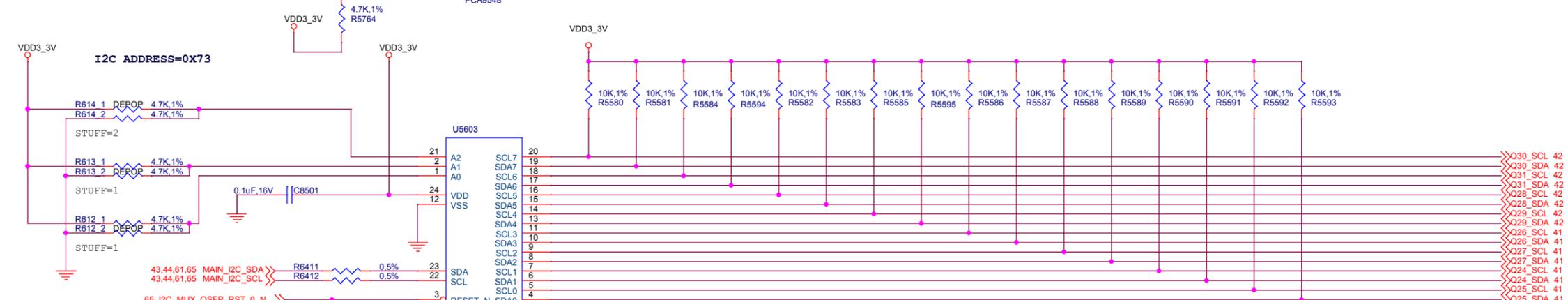
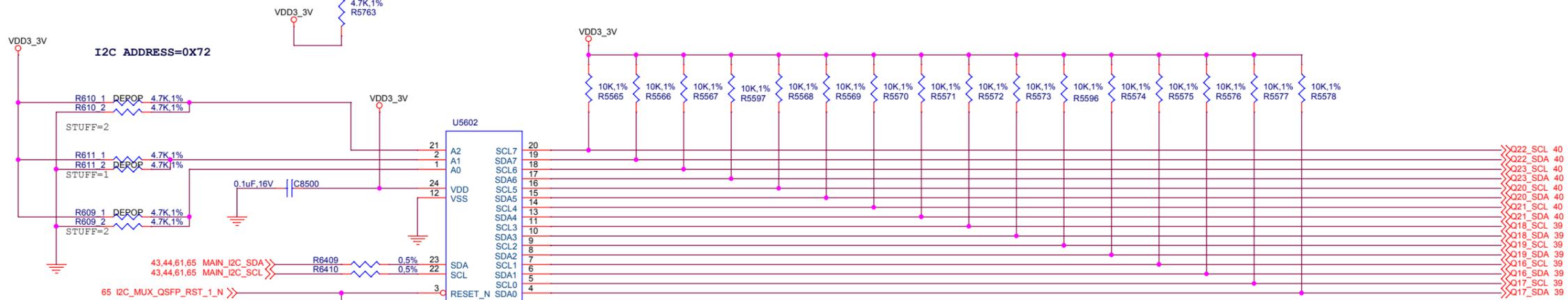
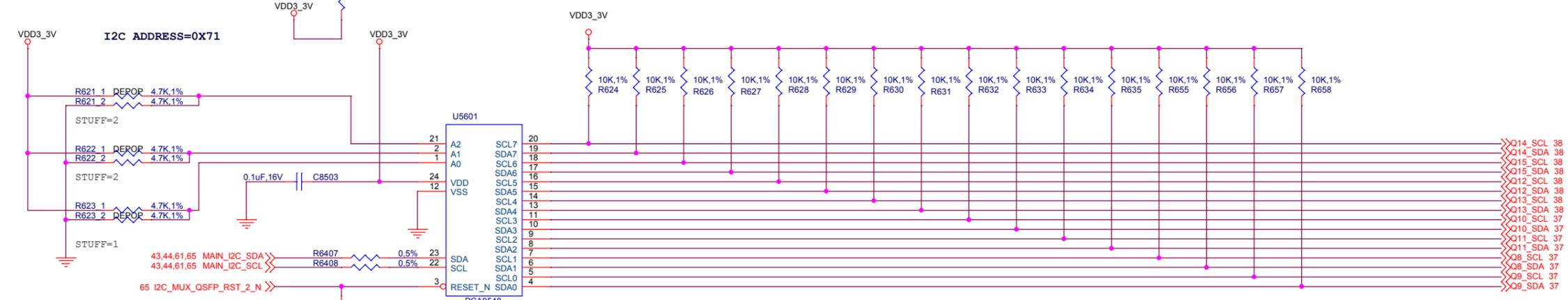
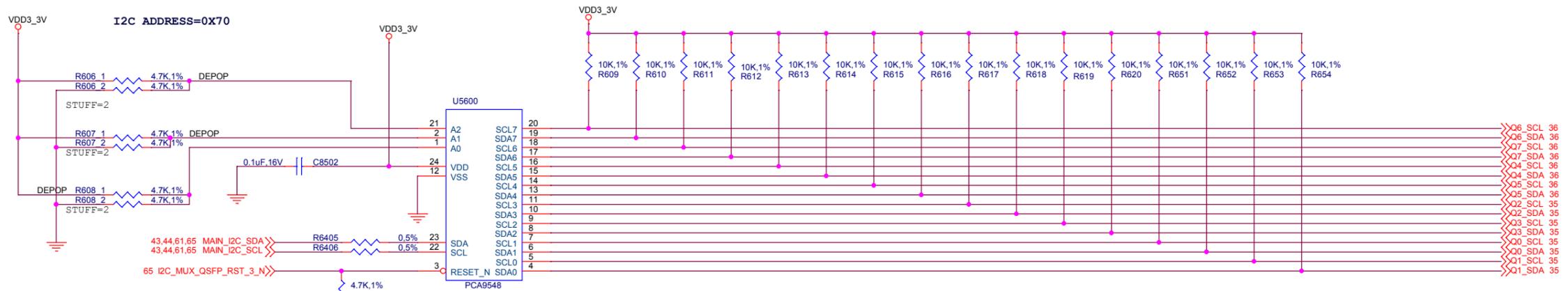
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<b>Size</b> C	<b>Document Number</b> 80-00010-03	<b>Rev</b> 2.0
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2289129-2  
CONN, 2x2 QSFP+4 INTERNAL LIGHT PIPES WITH EMI SPRING FINGERS

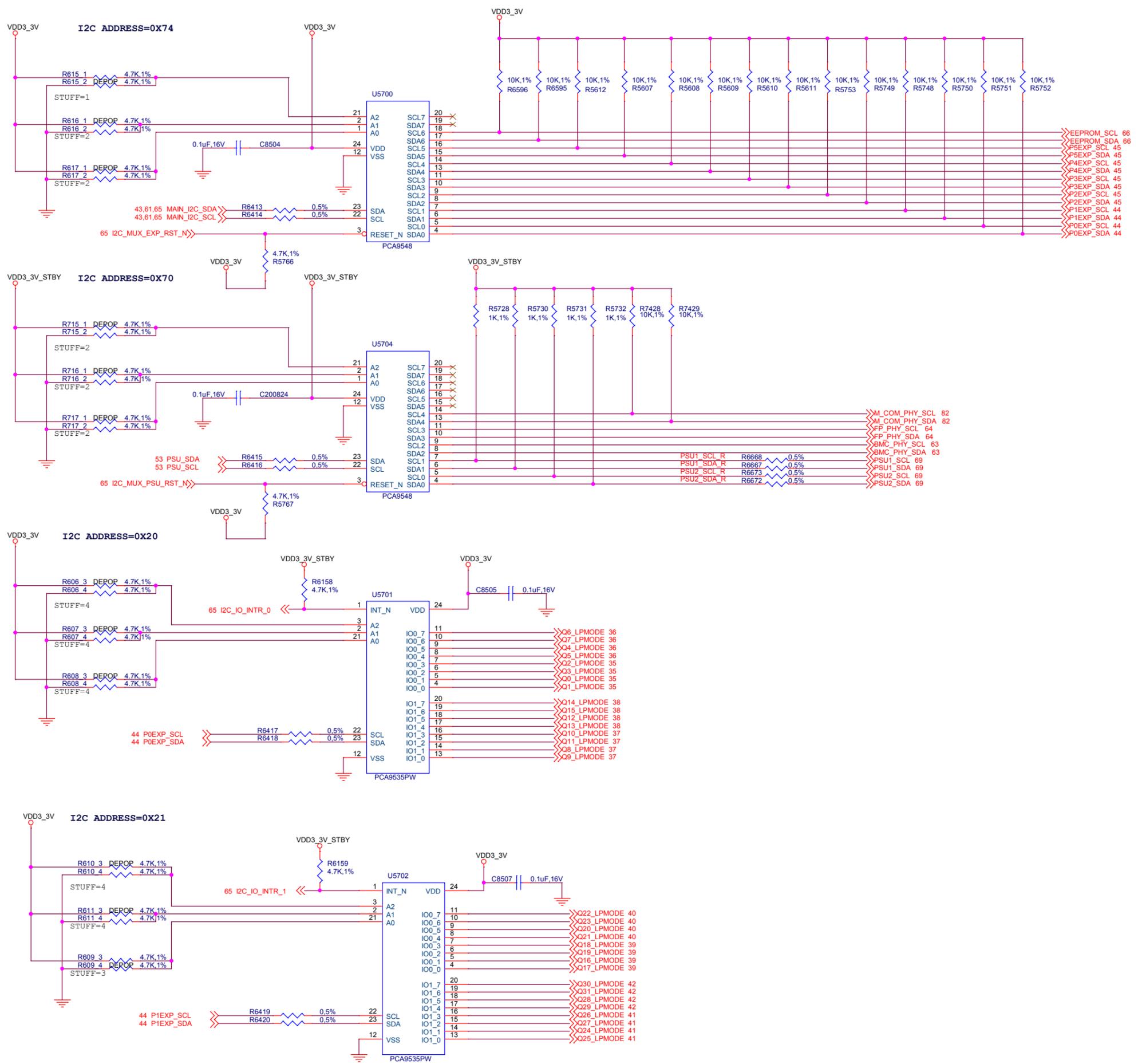
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<b>Size</b> C	<b>Document Number</b> 80-00010-03	<b>Rev</b> 2.0
<b>Date:</b> Thursday, December 22, 2016 <b>Sheet</b> 42 <b>of</b> 84		



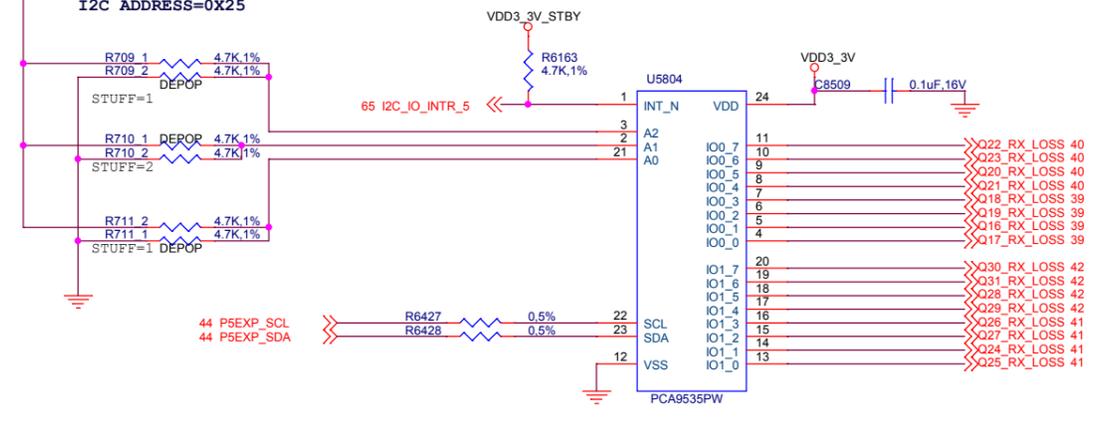
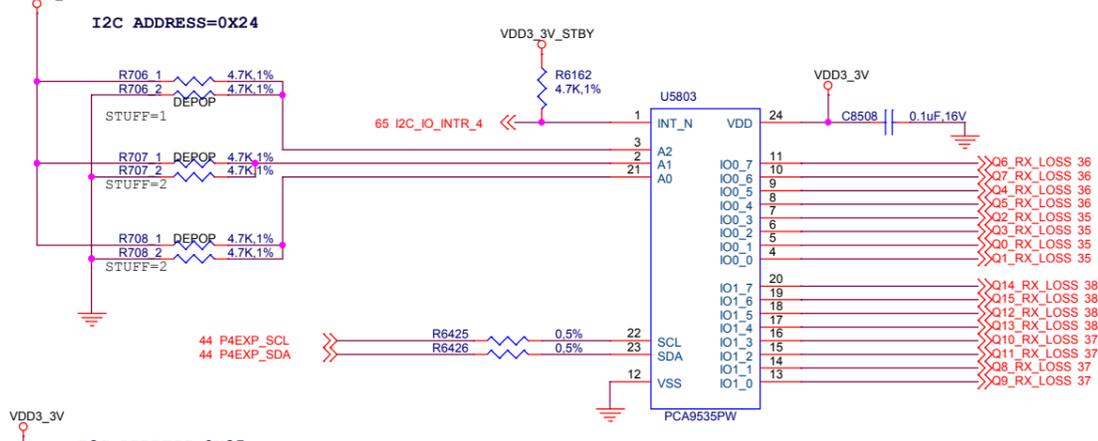
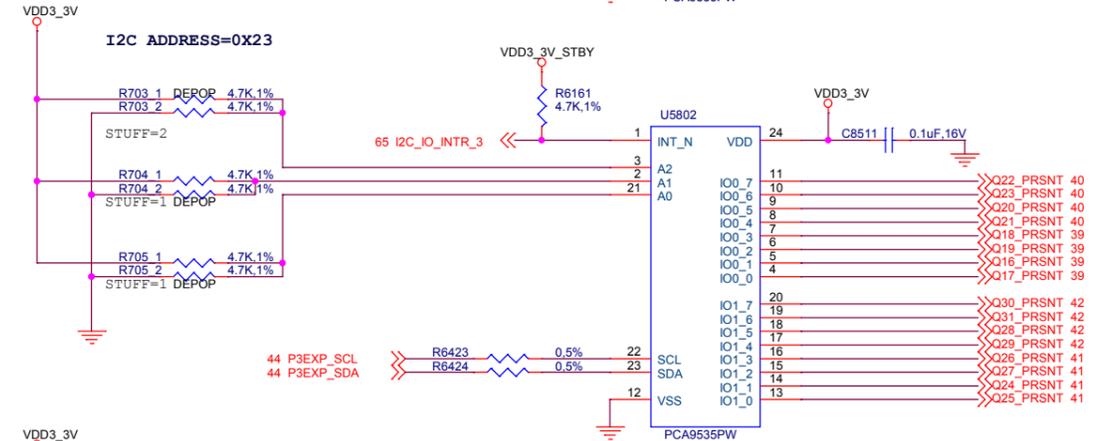
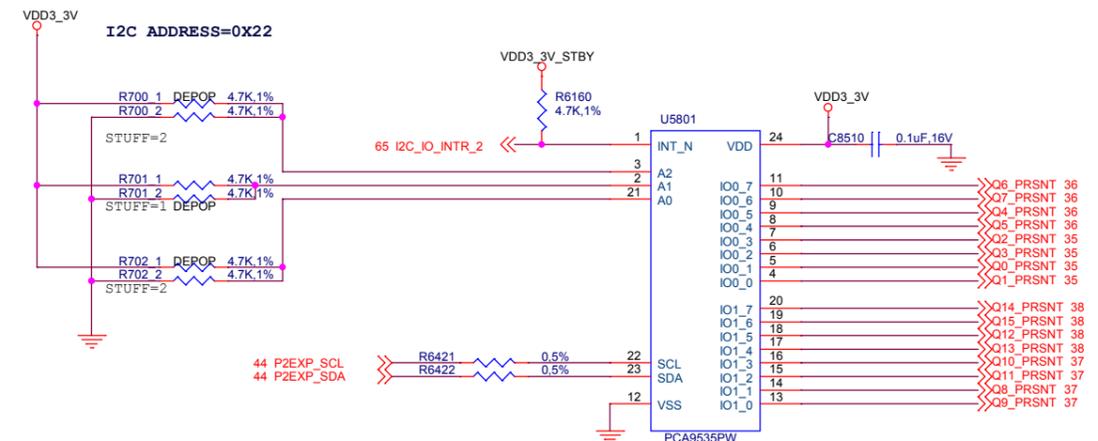
# QSFP I2C INTERFACE

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Title <b>WEDGE100C</b>		
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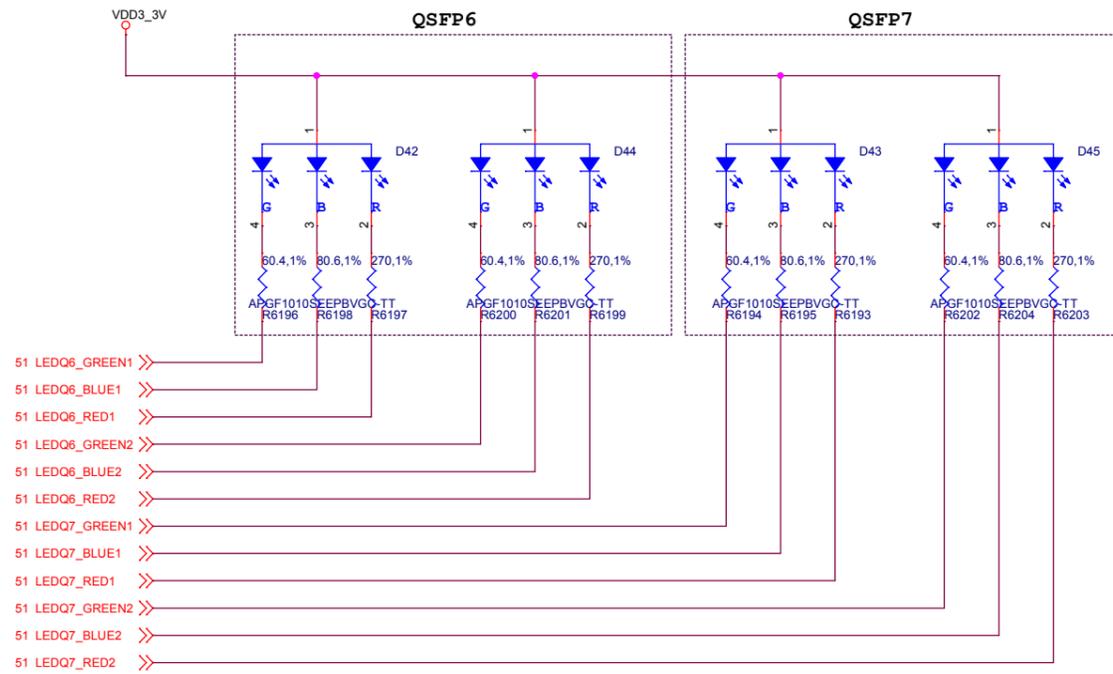
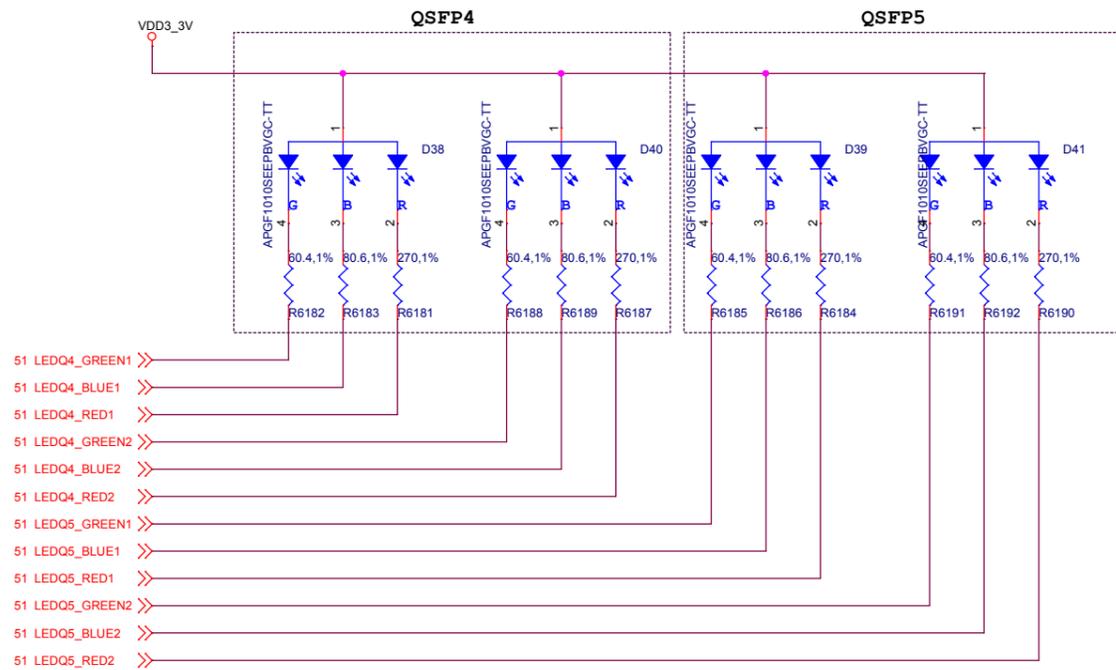
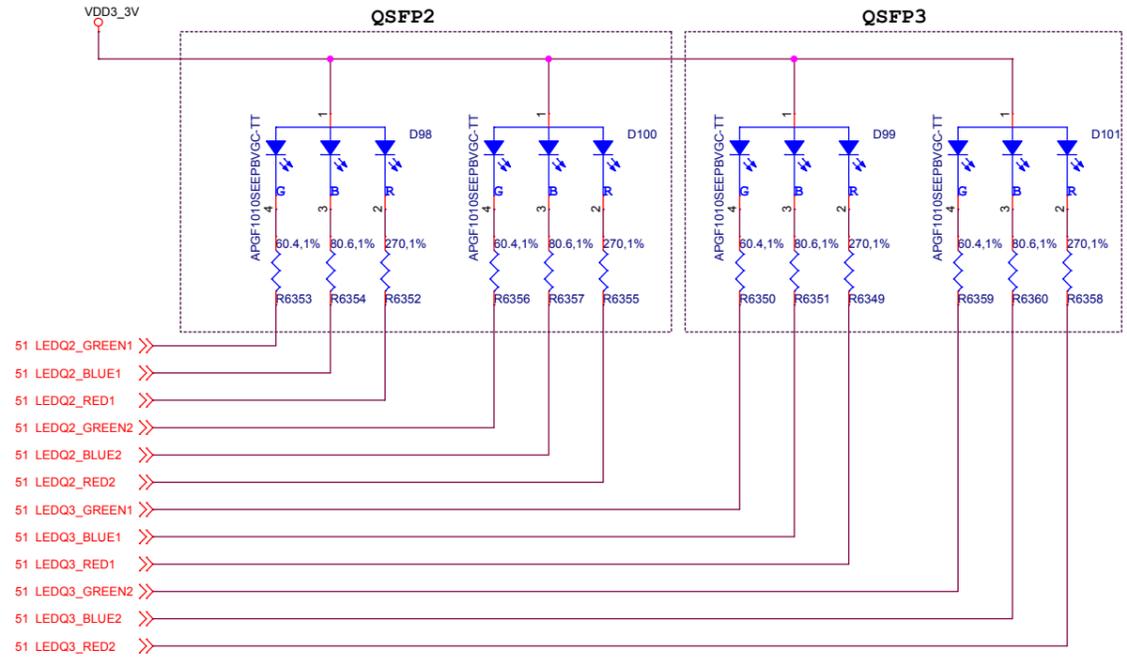
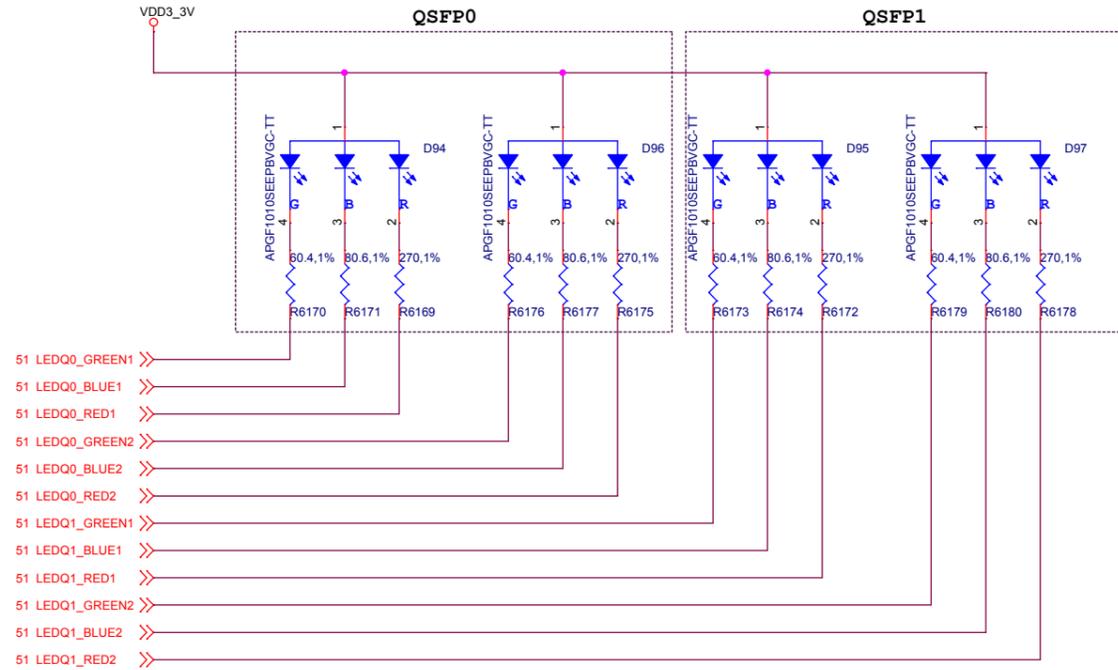
# QSFP I2C EXPANDER

CAVIUM		
Title <b>WEDGE100C</b>		
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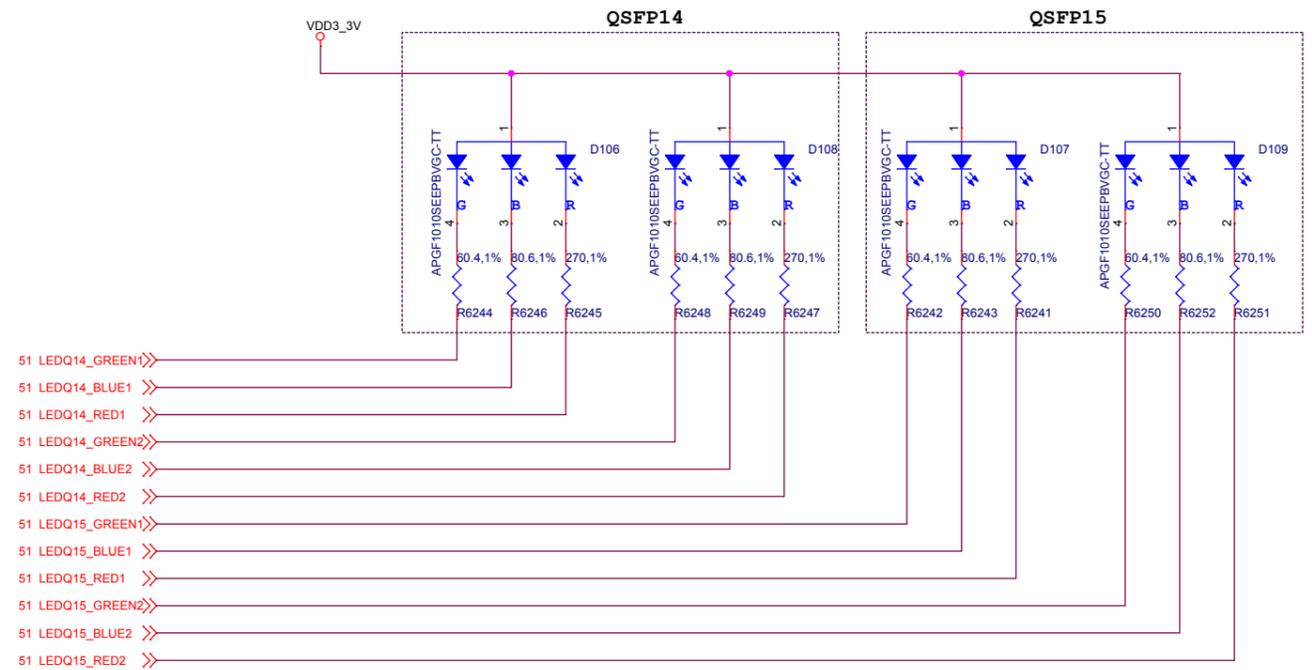
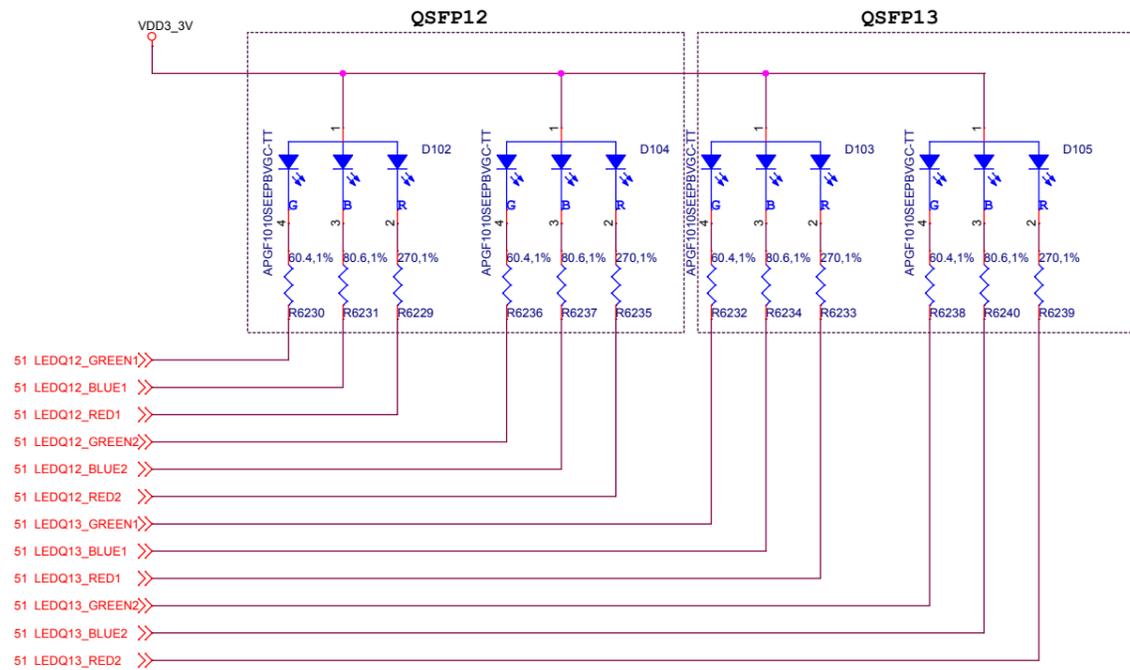
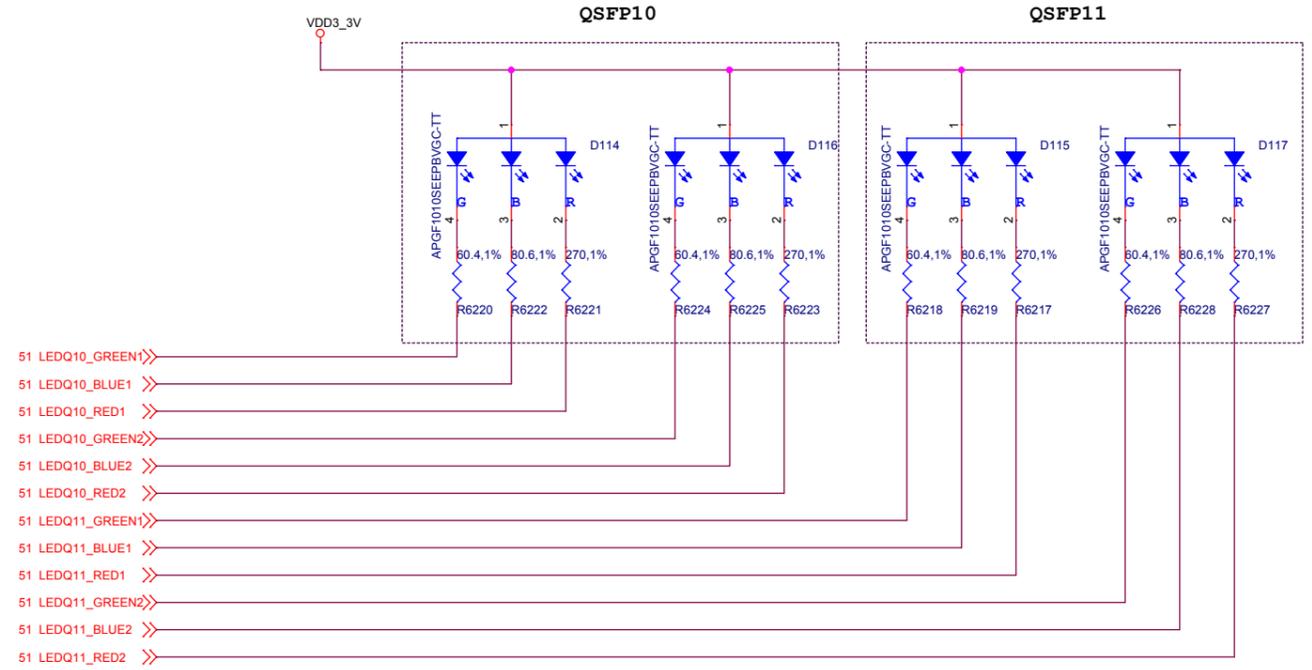
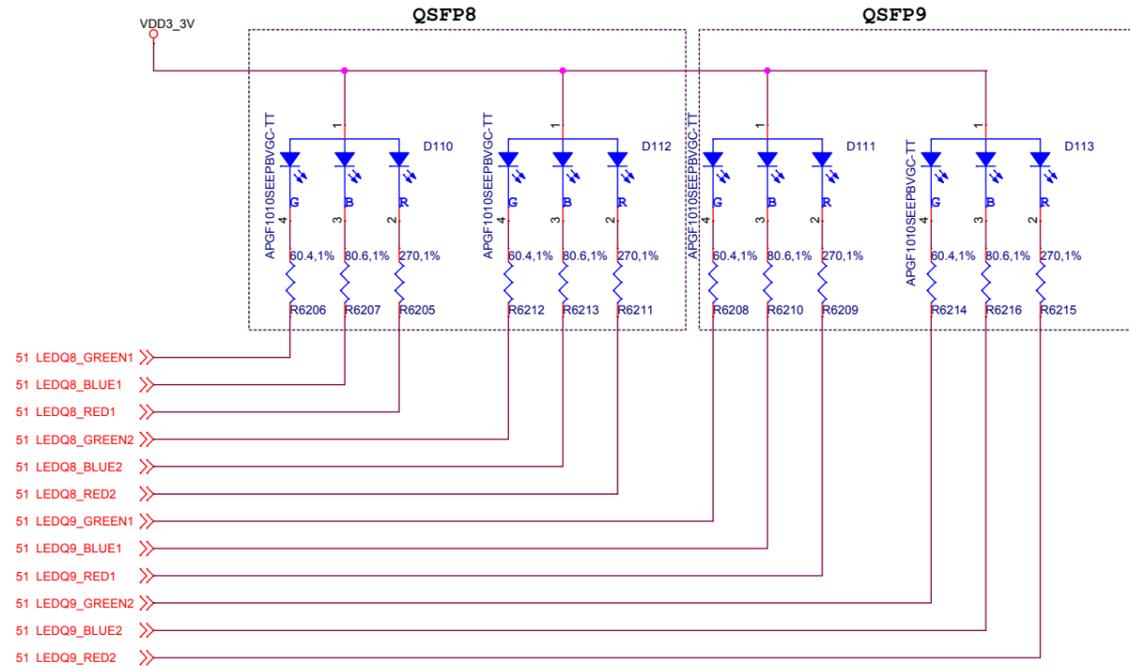
# QSFP I2C EXPANDER

<b>CAVIUM</b>		
Title: <b>WEDGE100C</b>		
Size: C	Document Number: 80-00010-03	Rev: 2.0
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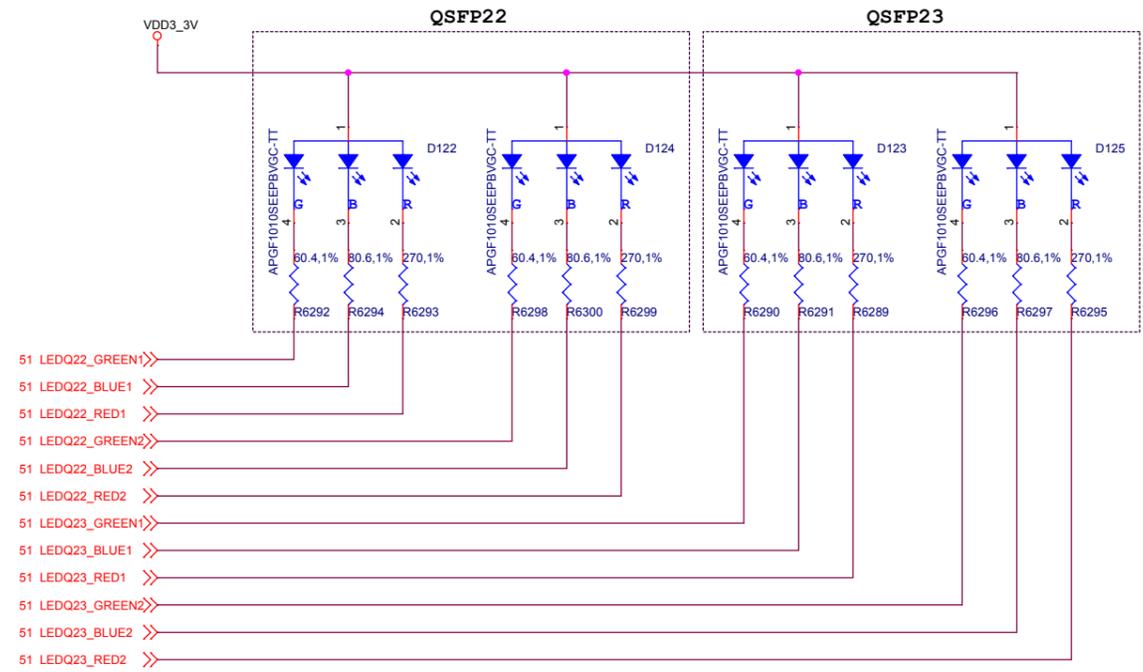
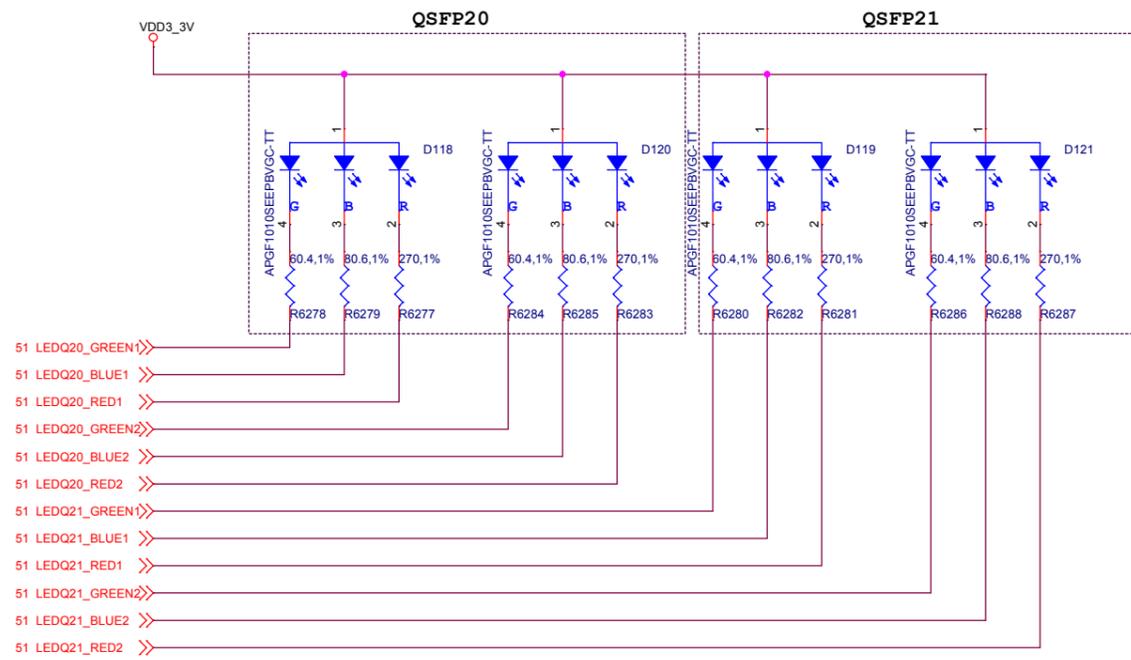
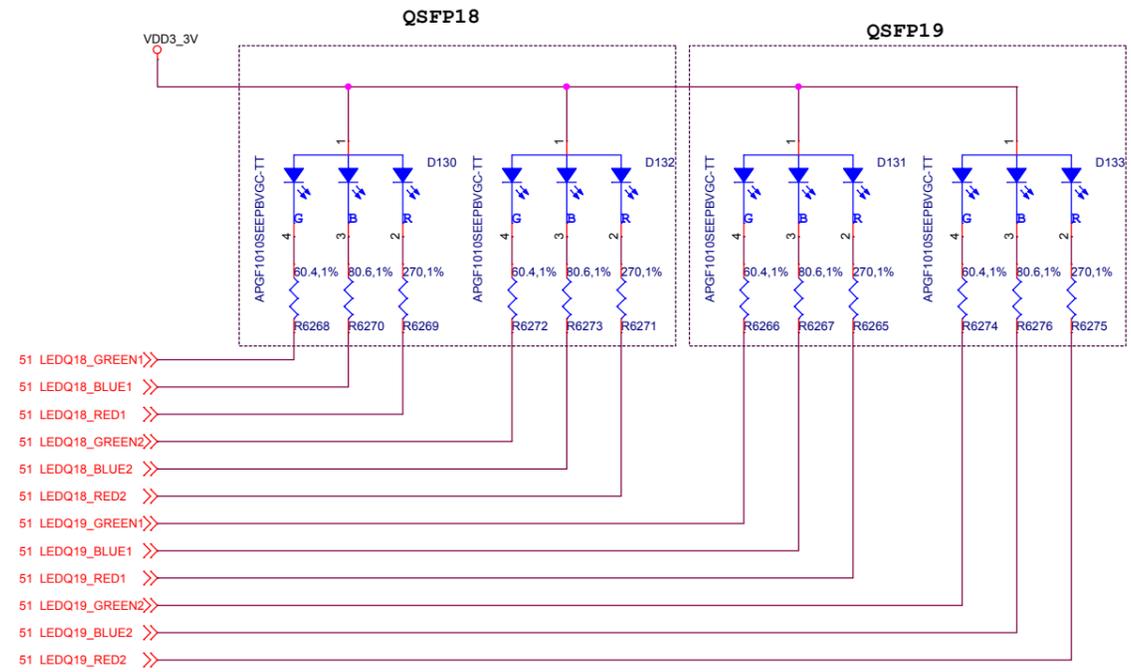
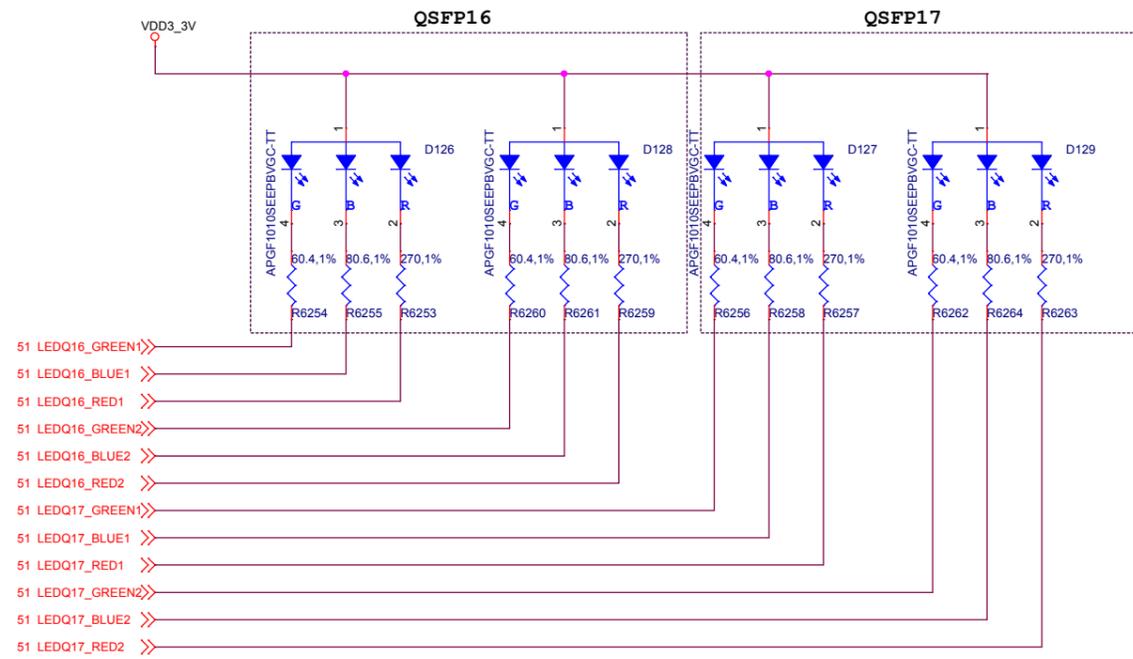
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Title			CAVIUM
Size			WEDGE100C
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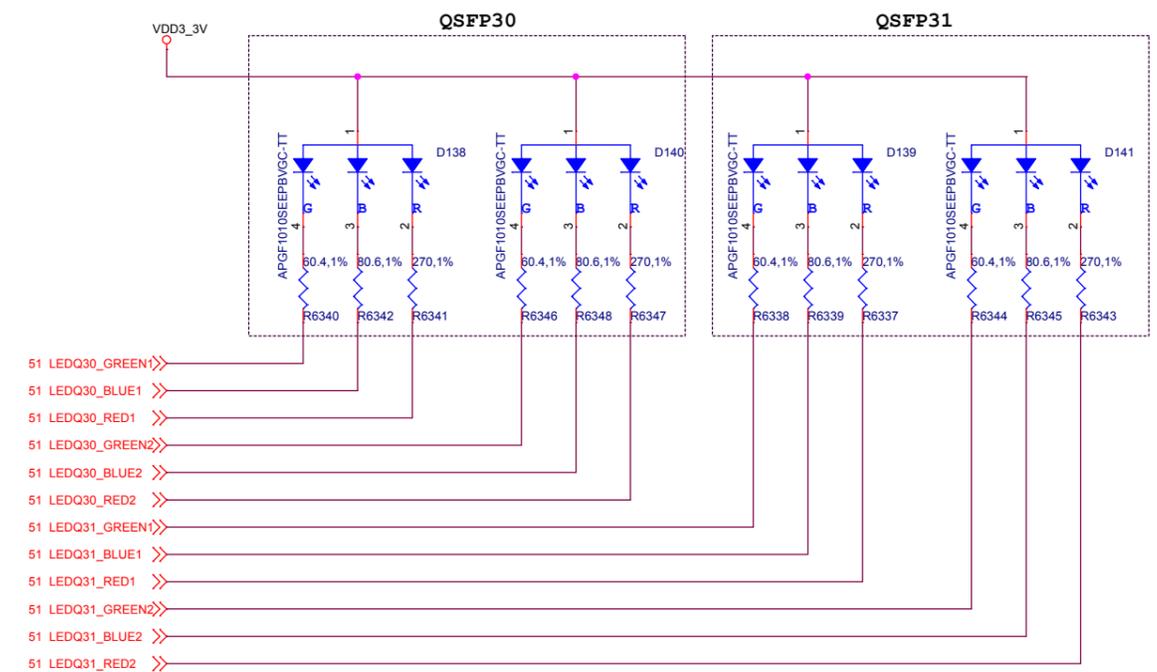
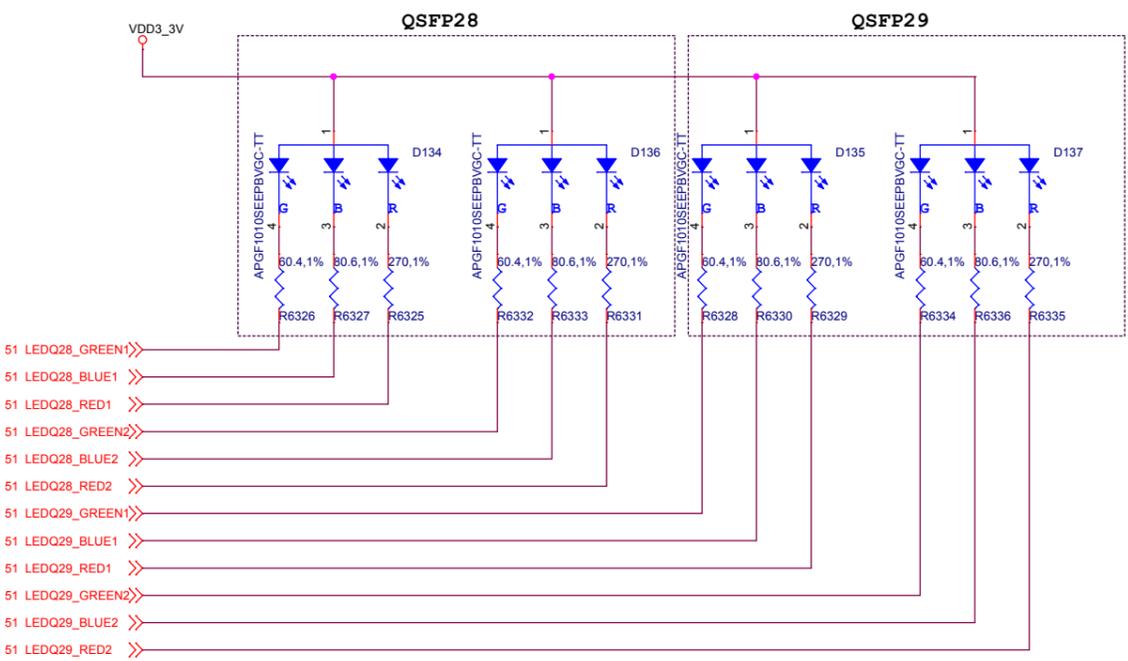
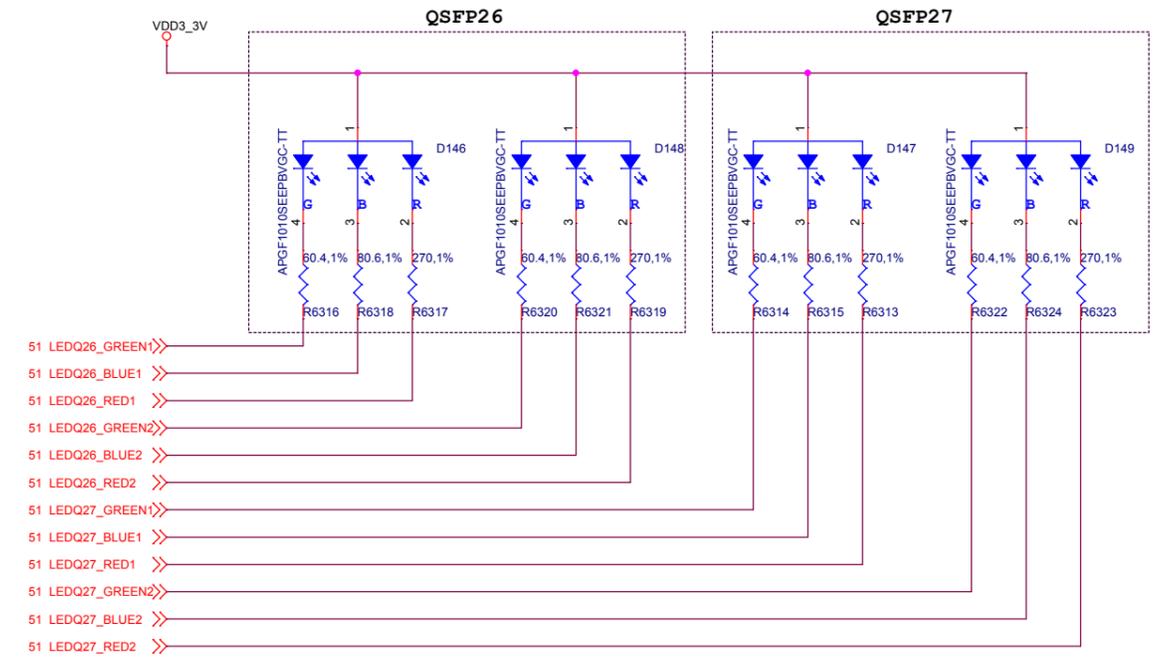
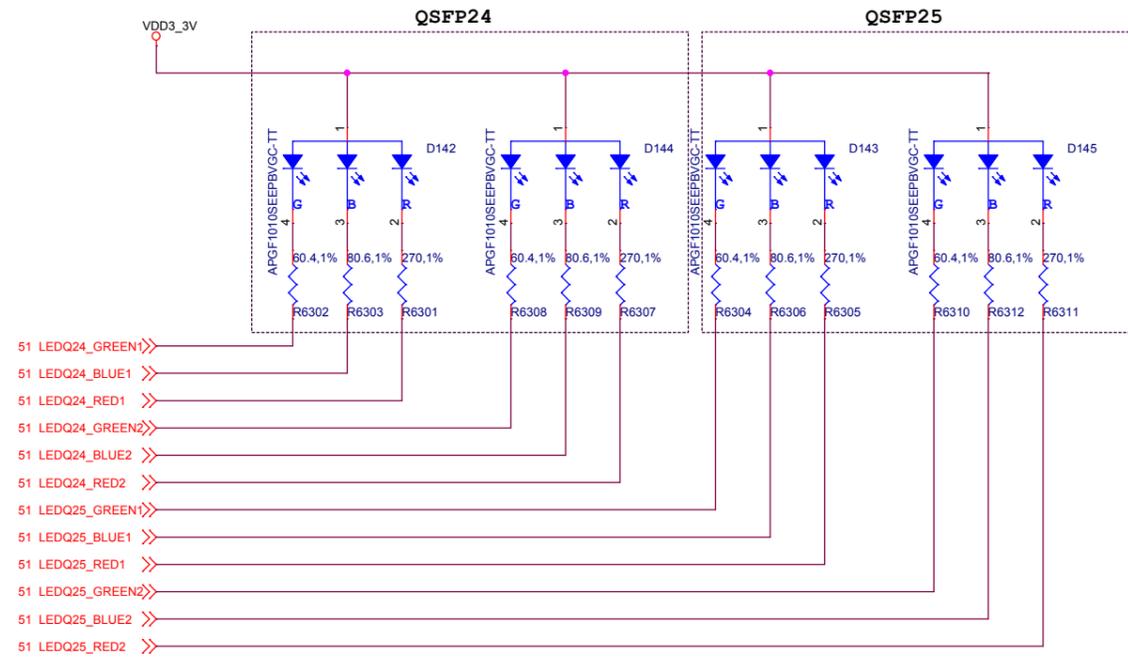
# QSFP LEDS-2

Title			CAVIUM
Size			WEDGE100C
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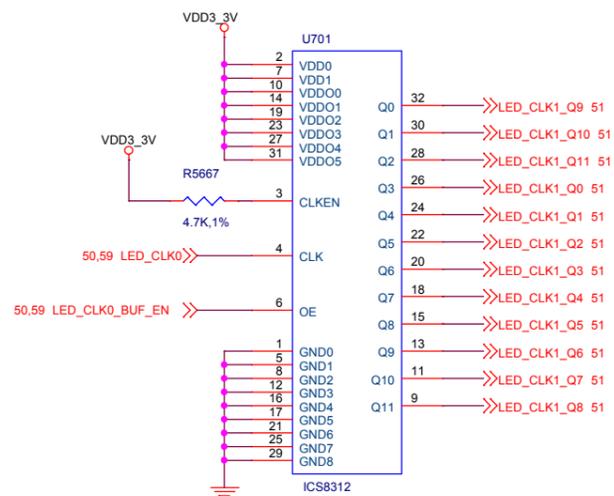
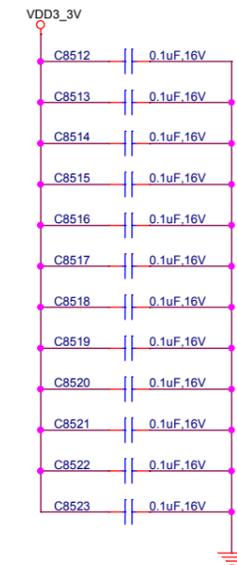
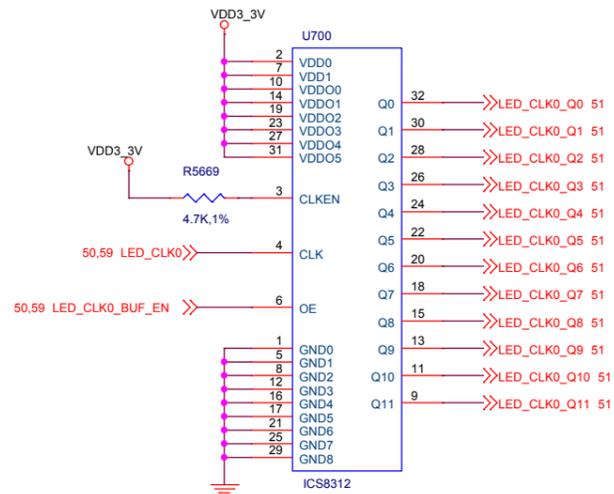
# QSFP LEDS-3

CAVIUM		
WEDGE100C		
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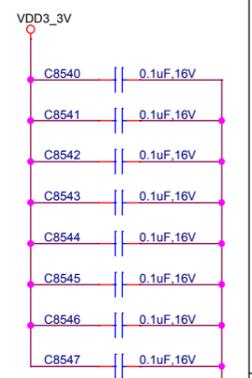
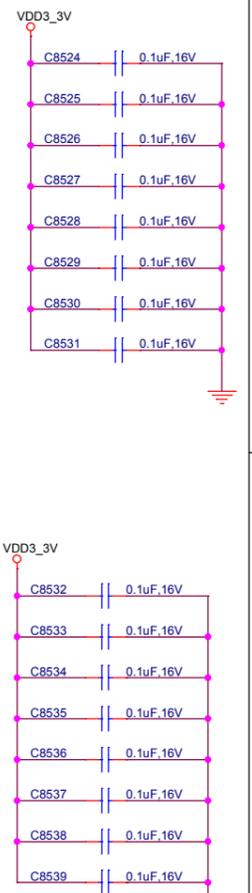
# QSFP LEDS-4

<b>CAVIUM</b>		
<b>WEDGE100C</b>		
Title		
Size	Document Number	Rev
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# QSFP LED CLOCK FANOUT BUFFERS

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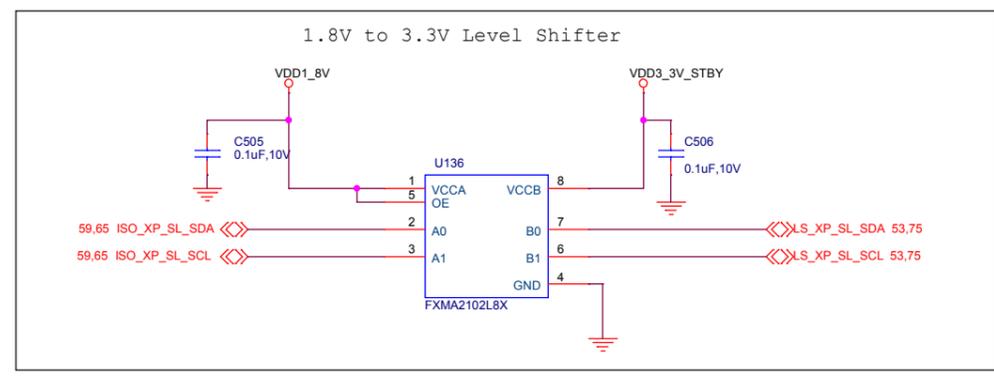
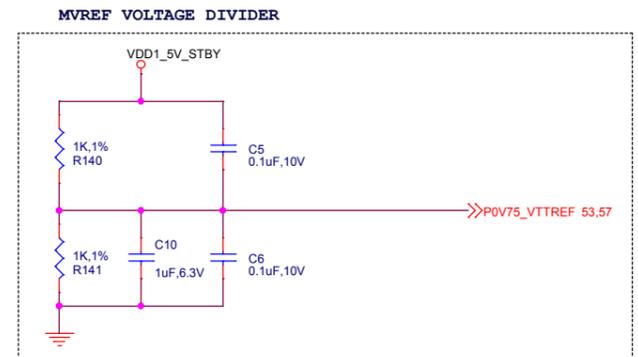
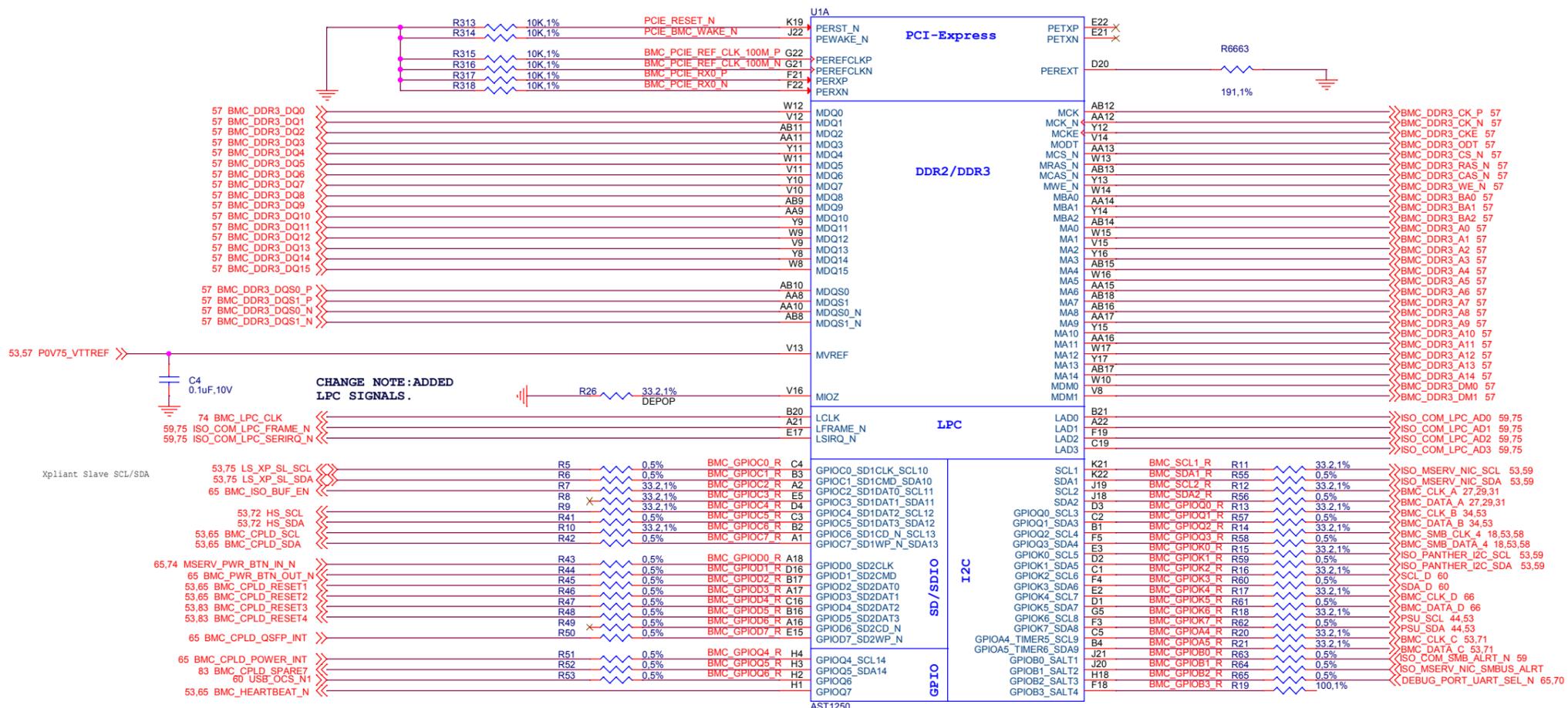


# QSFP LED SHIFT REGISTERS

Title			CAVIUM		
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			80-00010-03		
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Title		
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WEDGE100C		
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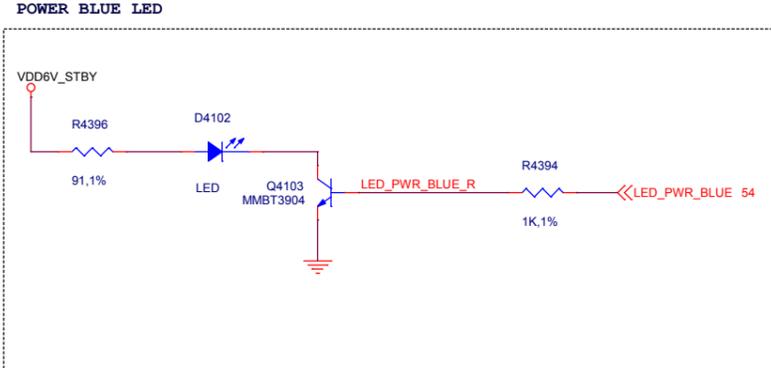
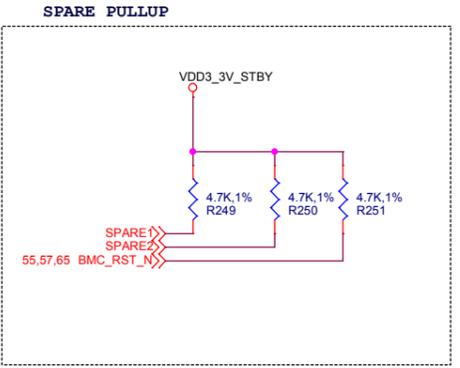
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CAVIUM		
Title	WEDGE100C	
Size	Document Number	Rev
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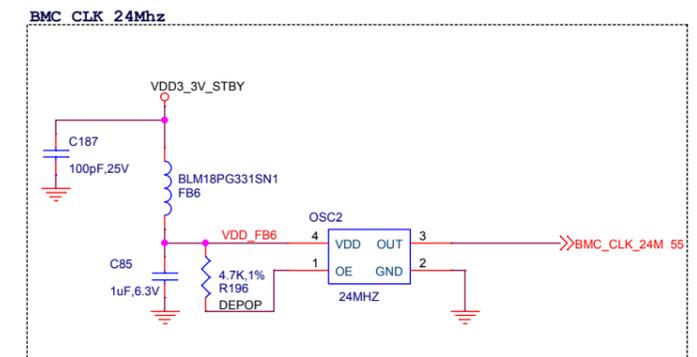
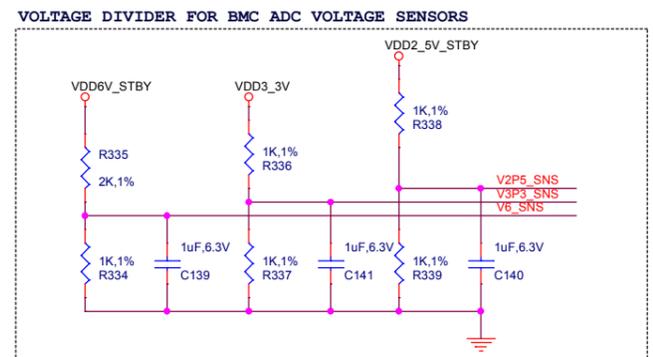
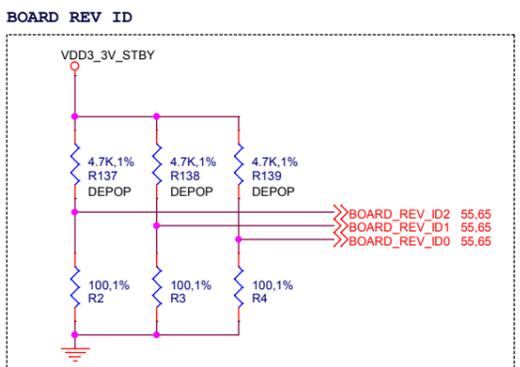
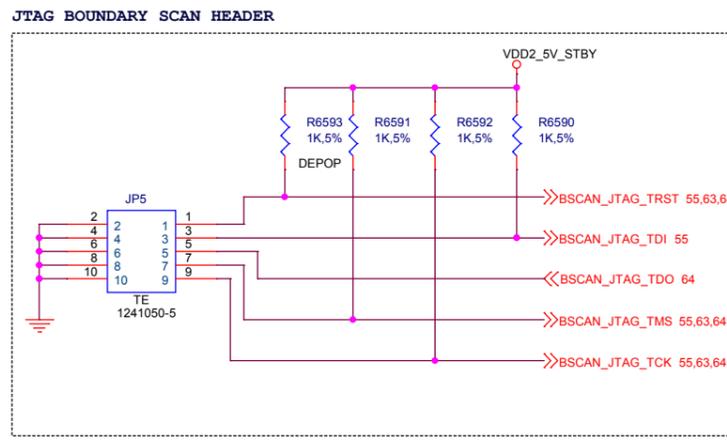
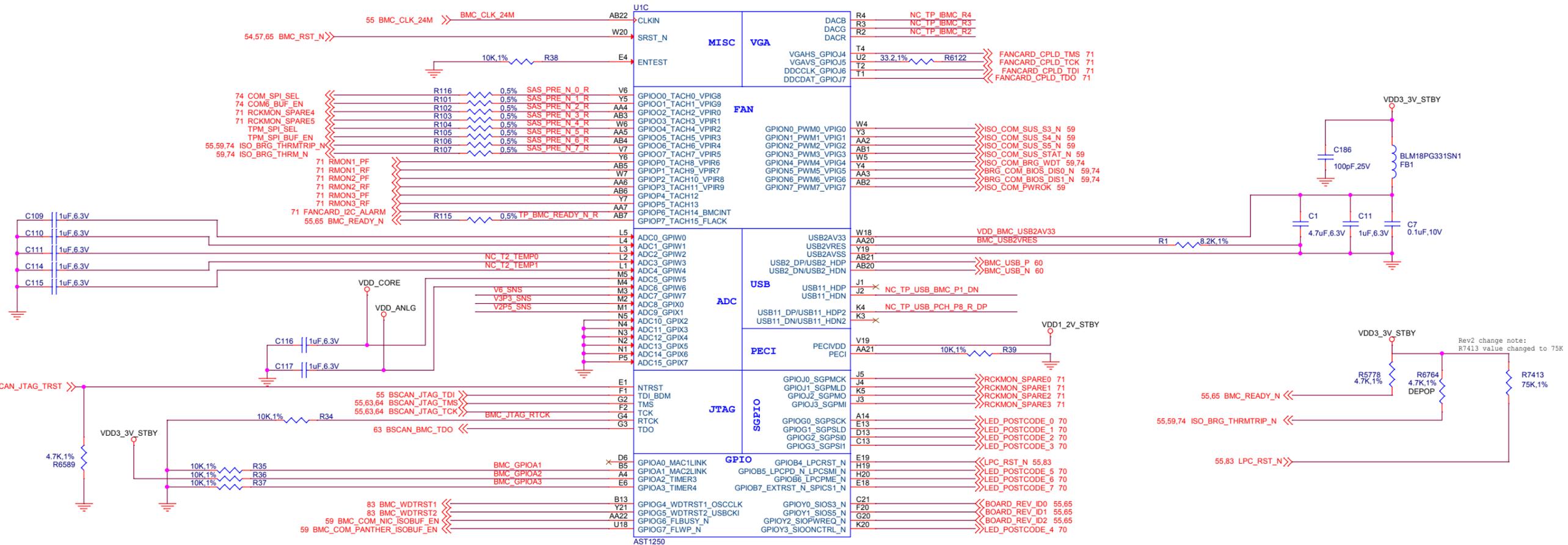


RACKPORT BITS ARE DELETED BECAUSE THESE FUNCTIONS ARE MOVED TO RACKMON CONNECTOR

PREVIOUSLY ALL 12V INFORMATION WERE COLLECTED FROM HOT SWAP ,NOW ITS THROUGH I2C



# BMC- PAGE2



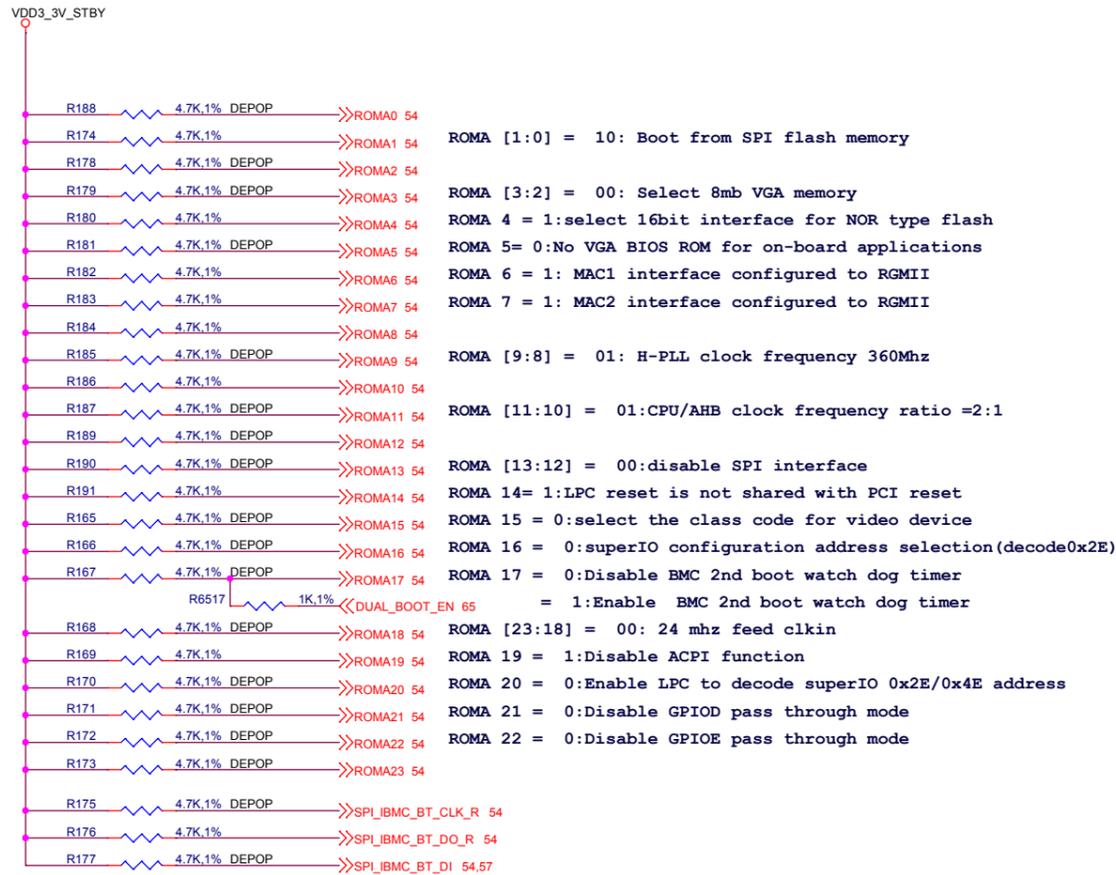
# BMC- PAGE3

<b>CAVIUM</b>		
<b>WEDGE100C</b>		
Title	80-00010-03	
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### BMC STRAPPING



ROMA [1:0] = 10: Boot from SPI flash memory

ROMA [3:2] = 00: Select 8mb VGA memory

ROMA 4 = 1:select 16bit interface for NOR type flash

ROMA 5 = 0:No VGA BIOS ROM for on-board applications

ROMA 6 = 1: MAC1 interface configured to RGMII

ROMA 7 = 1: MAC2 interface configured to RGMII

ROMA [9:8] = 01: H-PLL clock frequency 360Mhz

ROMA [11:10] = 01:CPU/AHB clock frequency ratio =2:1

ROMA [13:12] = 00:disable SPI interface

ROMA 14= 1:LPC reset is not shared with PCI reset

ROMA 15 = 0:select the class code for video device

ROMA 16 = 0:superIO configuration address selection(decode0x2E)

ROMA 17 = 0:Disable BMC 2nd boot watch dog timer  
= 1:Enable BMC 2nd boot watch dog timer

ROMA [23:18] = 00: 24 mhz feed clkln

ROMA 19 = 1:Disable ACPI function

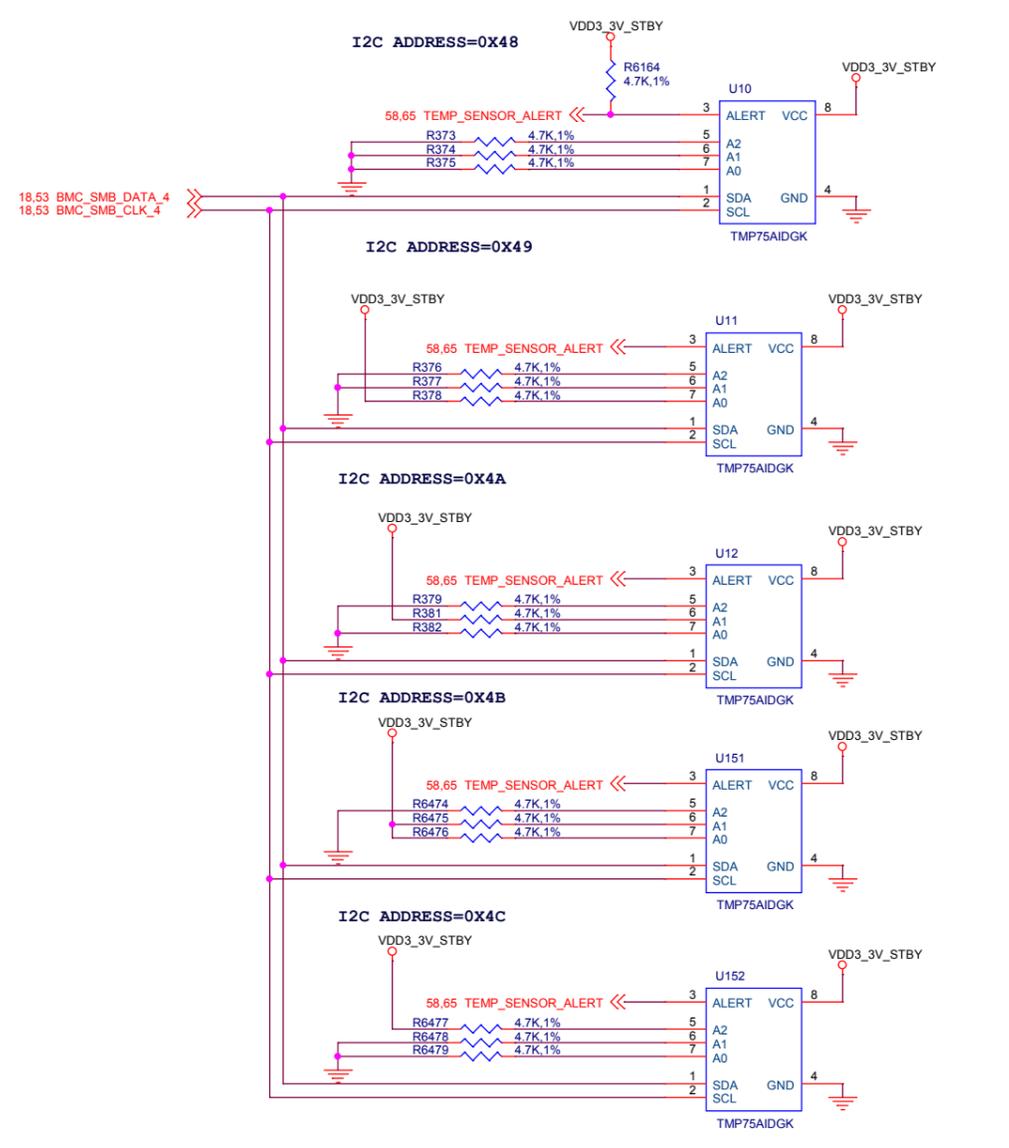
ROMA 20 = 0:Enable LPC to decode superIO 0x2E/0x4E address

ROMA 21 = 0:Disable GPIOD pass through mode

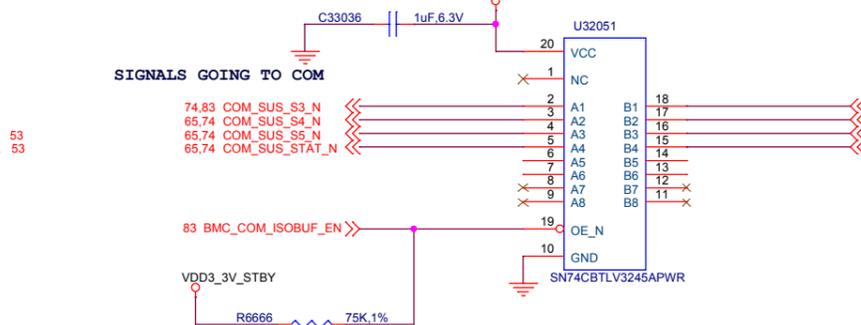
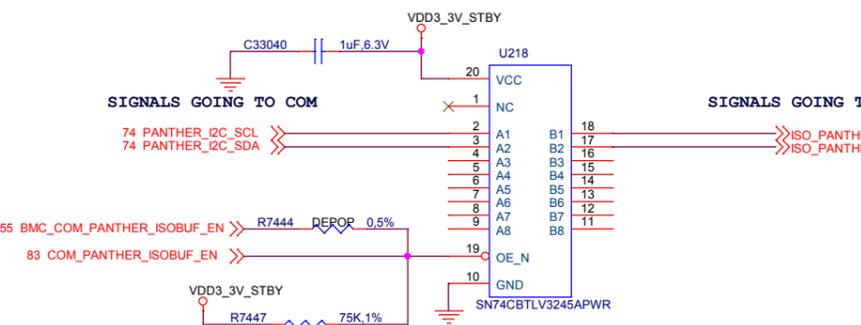
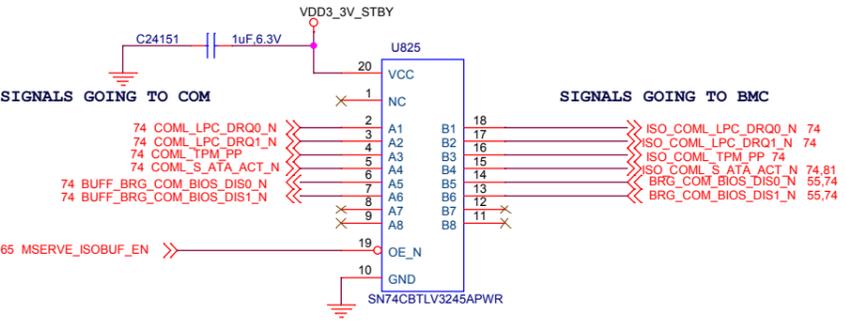
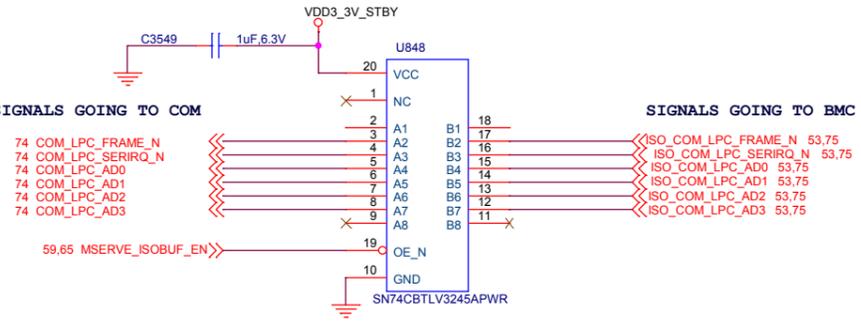
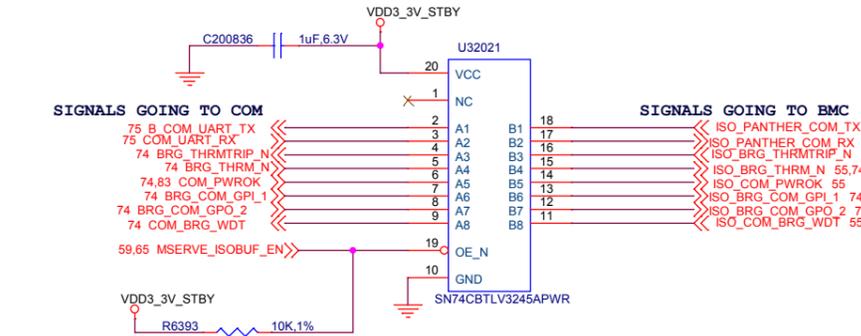
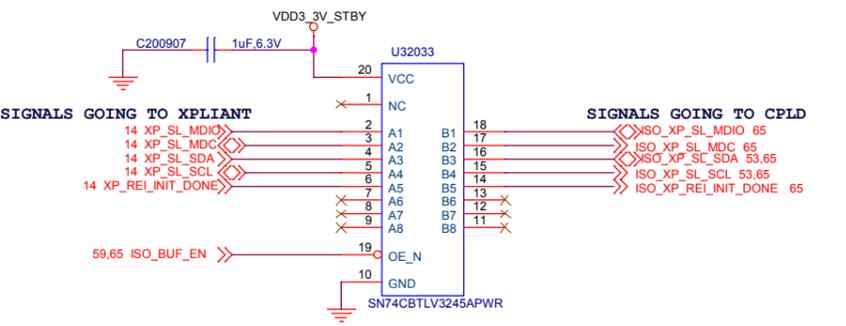
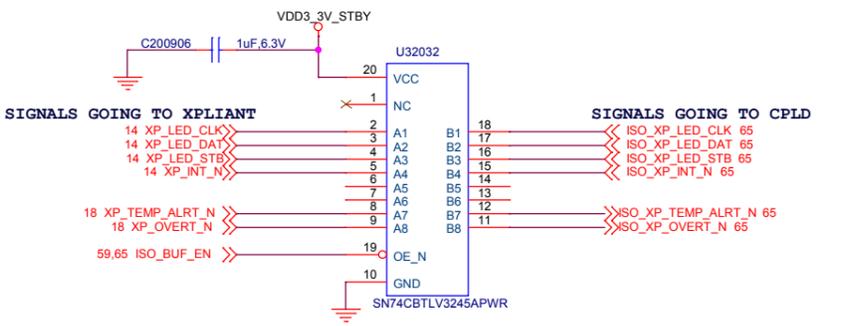
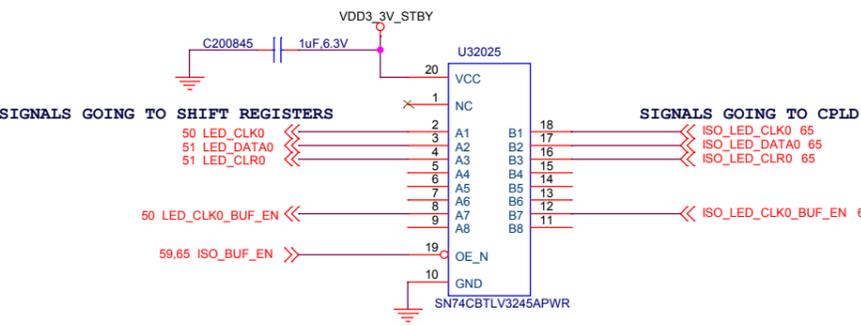
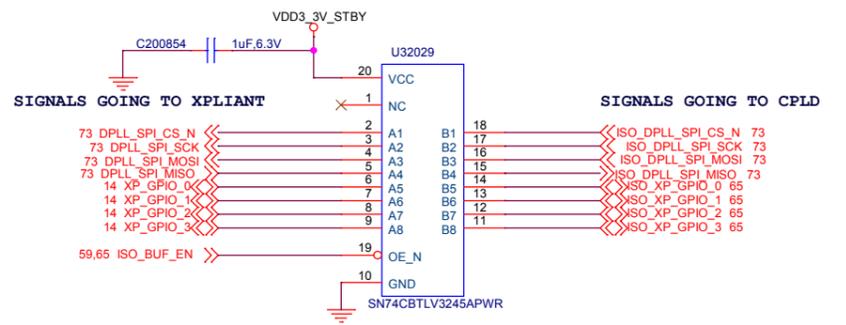
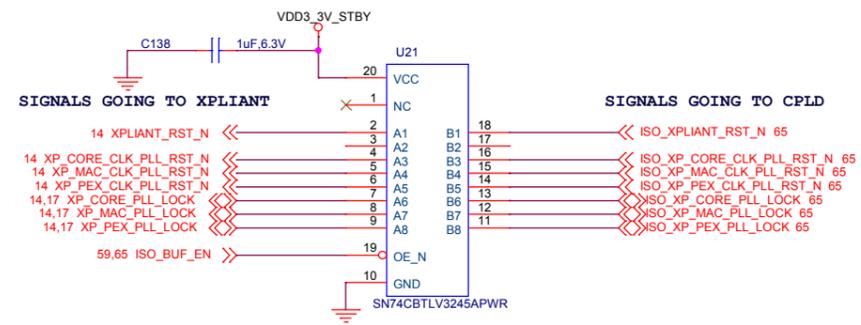
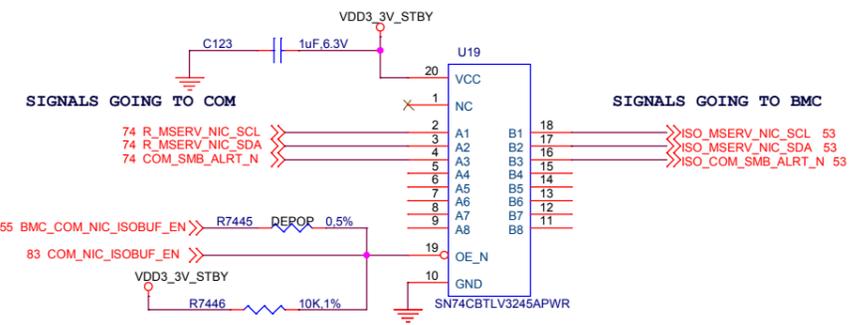
ROMA 22 = 0:Disable GPIOE pass through mode

NOTE: FOR ROMA 17 CPLD will make it high or low to enable or disable Dual BOOT option

### TEMP SENSORS



## BMC STRAPPING & TEMP SENSOR



Rev2 change note:  
R7447 value changed to 75K

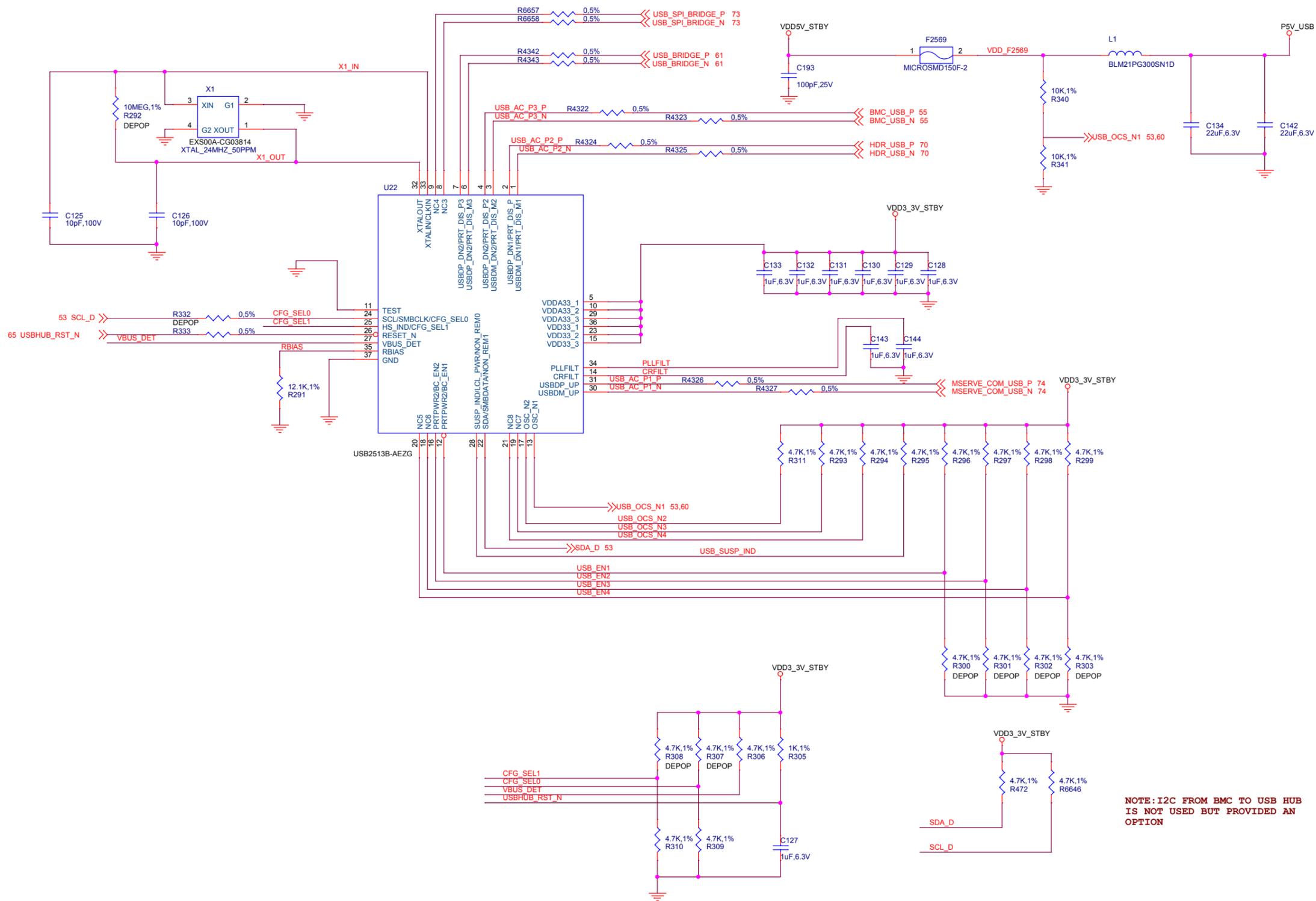
COMe INTEGRATION CHANGE NOTE:  
COM NIC AND COM PANTHER ISO  
BUFFER ENABLE ADDED TO CPLD

Rev2 change note:  
R6666 value changed to 75K

# SIGNAL ISOLATION BUFFERS

CAVIUM		
WEDGE100C		
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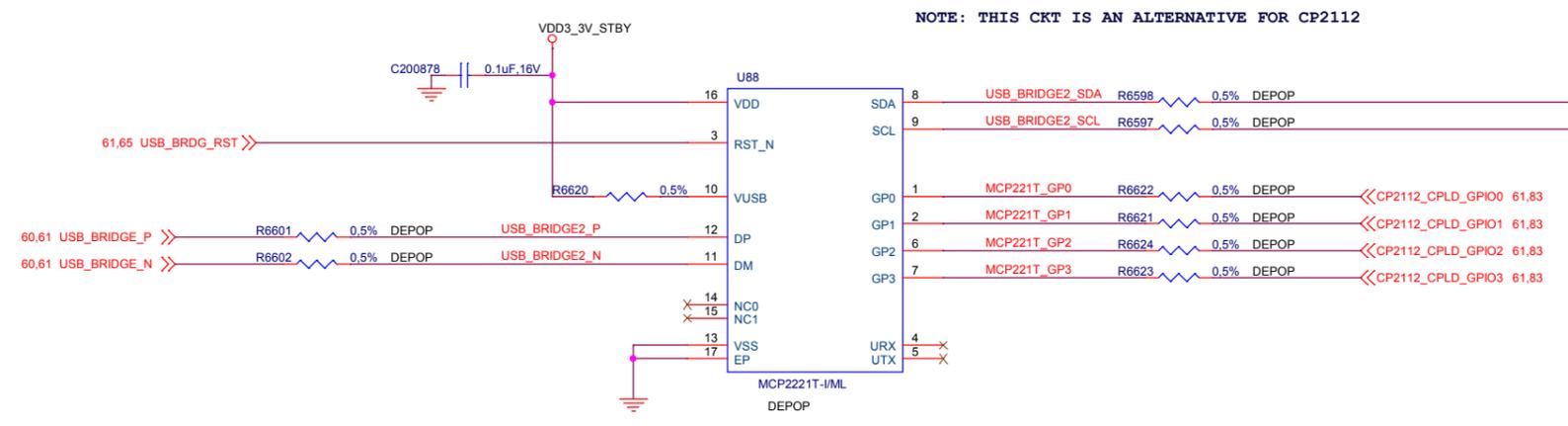
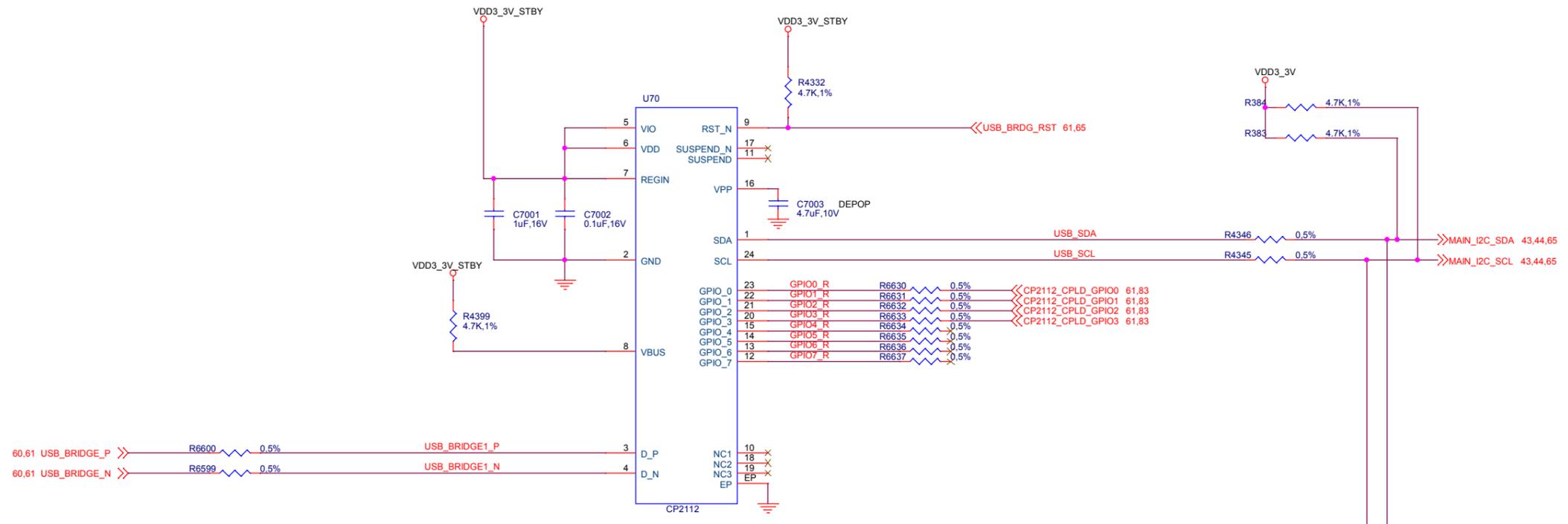
NOTE: FOR EVTA THE USB HUB USED IS 3PORT (USB2513B-AEZG) ; WHEN WE ARE IMPLEMENTING DPLL MODULE USB HUB WILL BE CHANGED TO 4 PORT PART (USB2514)



NOTE: I2C FROM BMC TO USB HUB IS NOT USED BUT PROVIDED AN OPTION

# USB HUB

Title			CAVIUM		
WEDGE100C					
Size	Document Number	Rev			
C	80-00010-03	2.0			
Date:	Thursday, December 22, 2016	Sheet	60	of	84

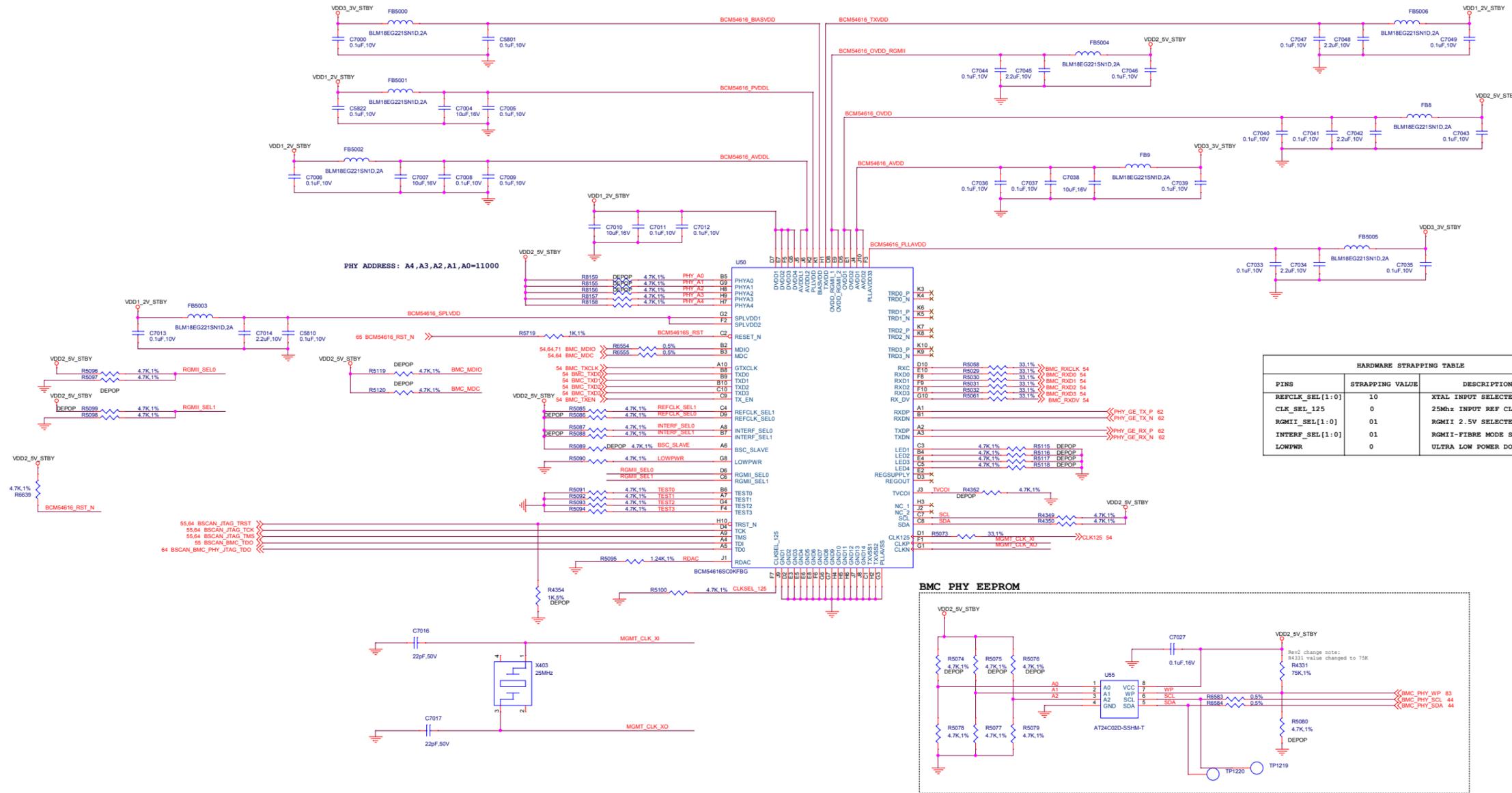


# USB I2C BRIDGE

Title			CAVIUM
Size			WEDGE100C
Document Number	80-00010-03	Rev	2.0
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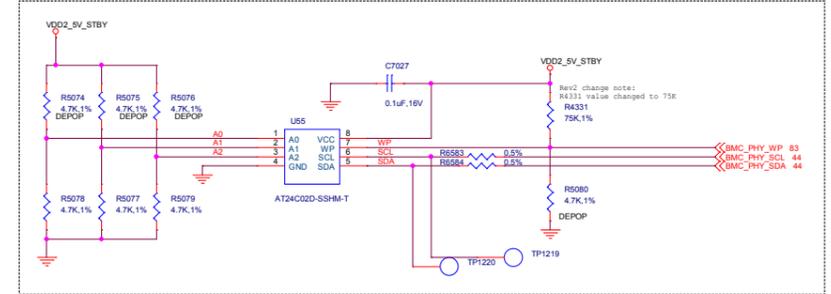
L= BLM18EG221SN1D (FB, 220OHM, 2A, DCR: 50mOHMS, PKG: 0603, SMD)



PHY ADDRESS: A4, A3, A2, A1, A0=11000

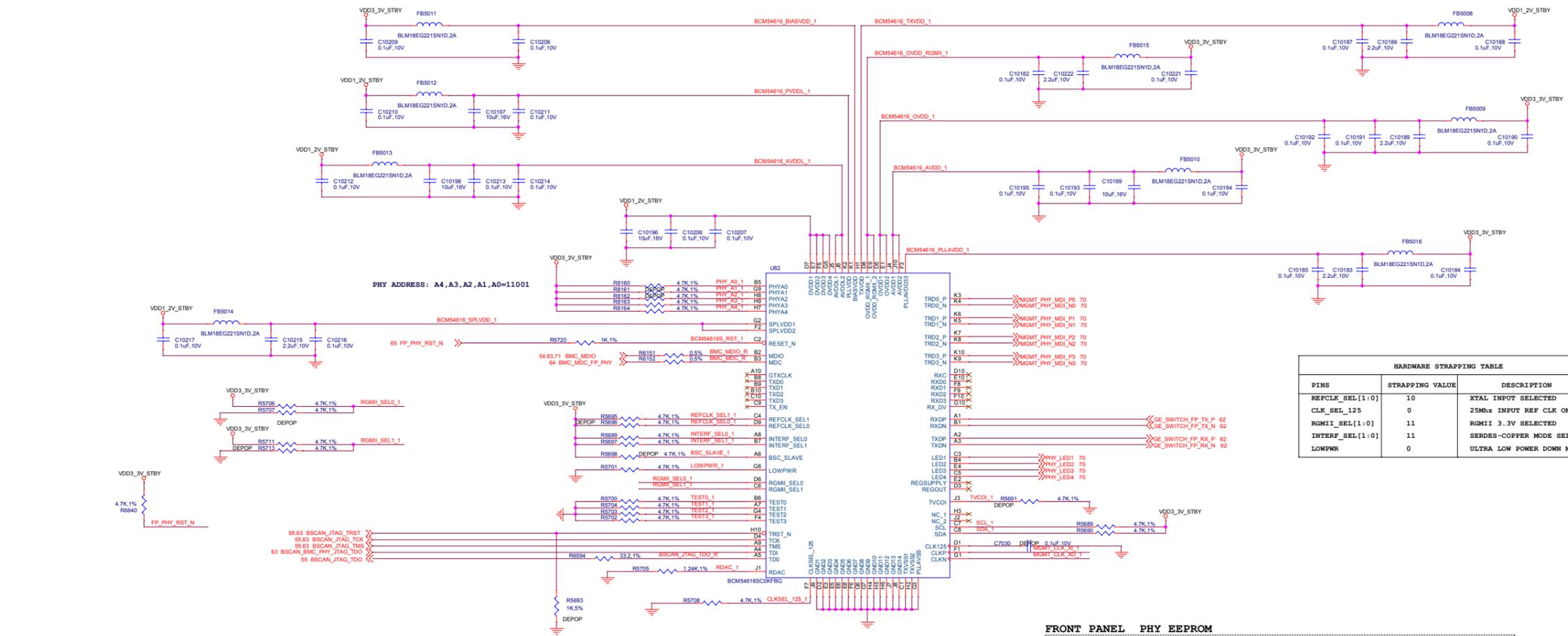
HARDWARE STRAPPING TABLE		
PINS	STRAPPING VALUE	DESCRIPTION
REFCLK_SEL[1:0]	10	XTAL INPUT SELECTED
CLK_SEL_125	0	25MHz INPUT REF CLK ON CLK PINS
RGMII_SEL[1:0]	01	RGMII 2.5V SELECTED
INTERF_SEL[1:0]	01	RGMII-FIBRE MODE SELECTED
LOWPWR	0	ULTRA LOW POWER DOWN MODE DISABLED

**BMC PHY EEPROM**

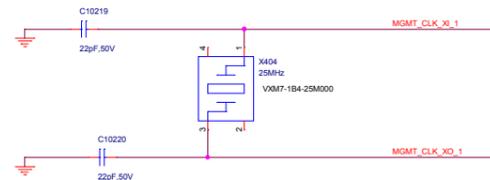


**BMC PHY**

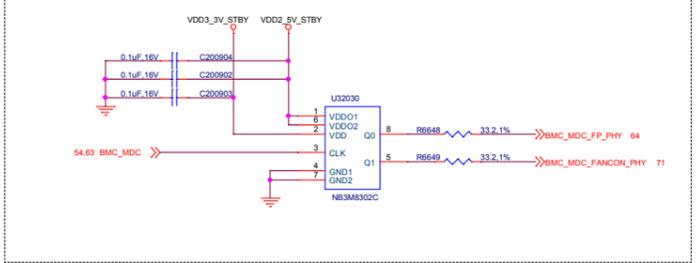
L= BLM18EG221SN1D (FB, 220OHM, 2A, DCR: 50mOHMS, PKG: 0603, SMD)



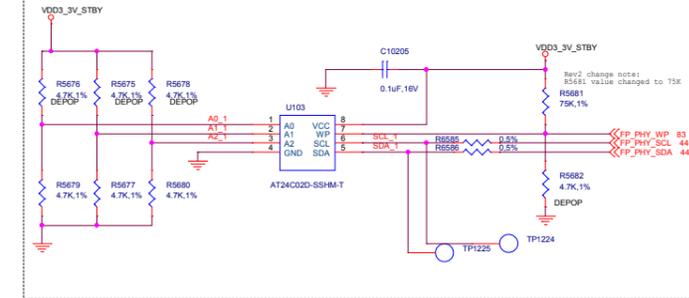
HARDWARE STRAPPING TABLE		
PINS	STRAPPING VALUE	DESCRIPTION
REFCLK_SEL[1:0]	10	XTAL INPUT SELECTED
CLK_SEL_125	0	25MHz INPUT REF CLK ON CLK PINS
RGMII_SEL[1:0]	11	RGMII 3.3V SELECTED
INTERF_SEL[1:0]	11	SERDES-COPPER MODE SELECTED
LOWPWR	0	ULTRA LOW POWER DOWN MODE DISABLED



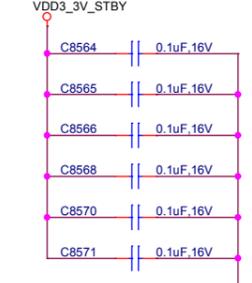
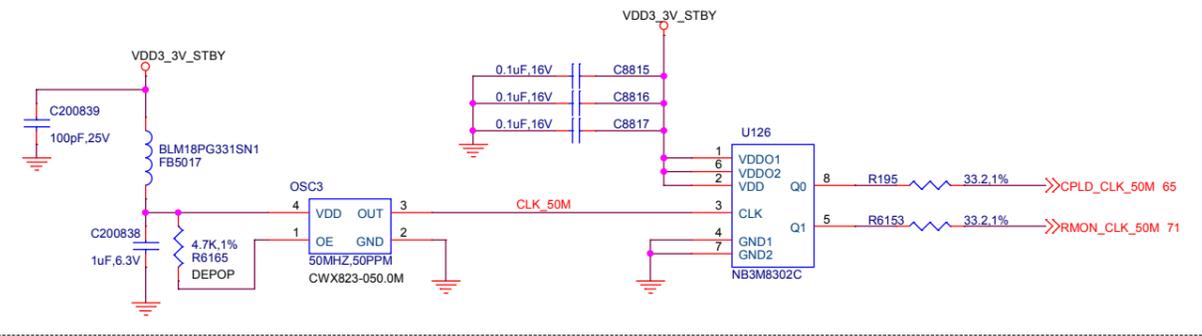
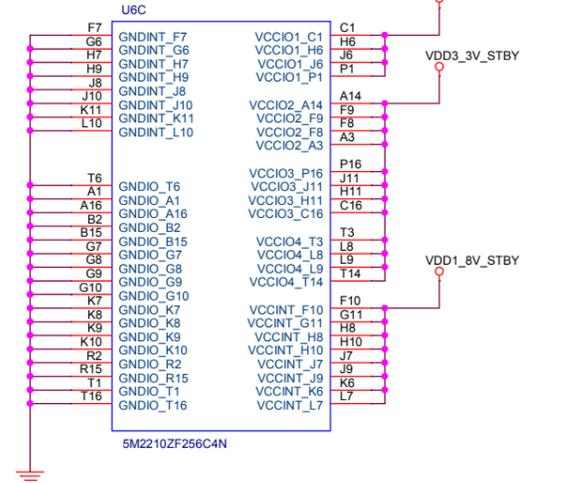
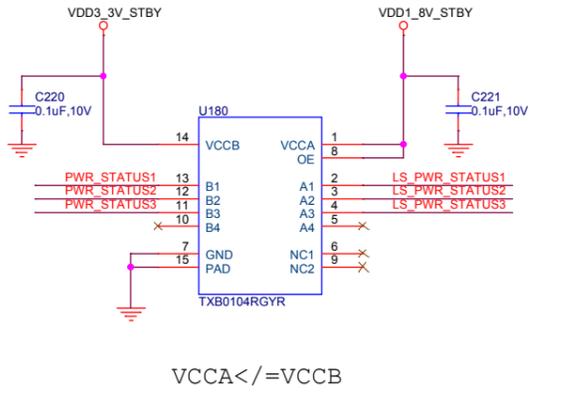
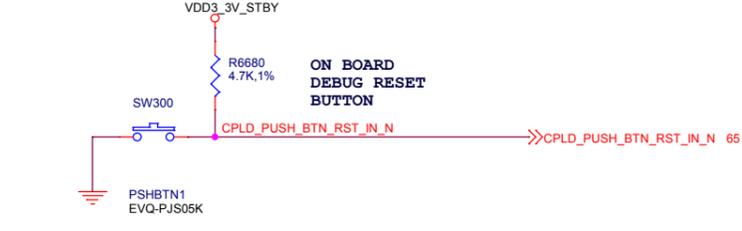
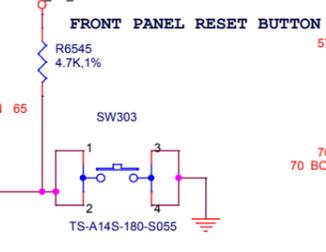
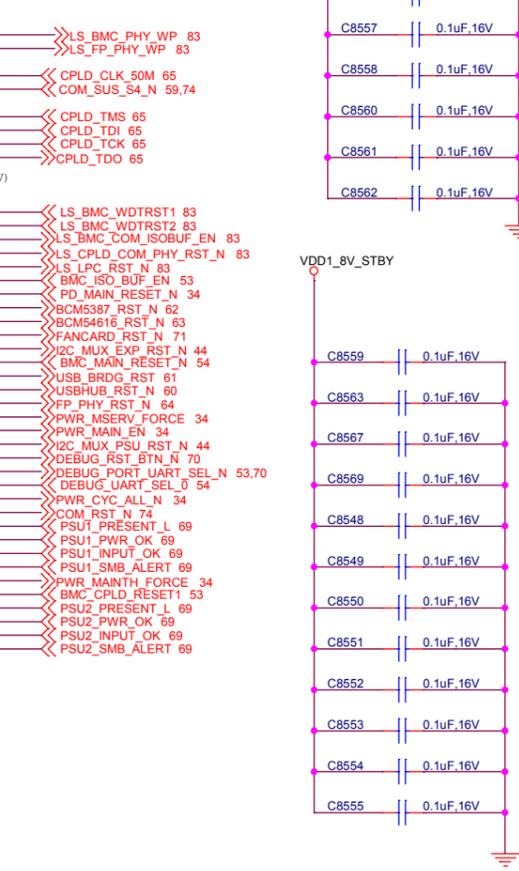
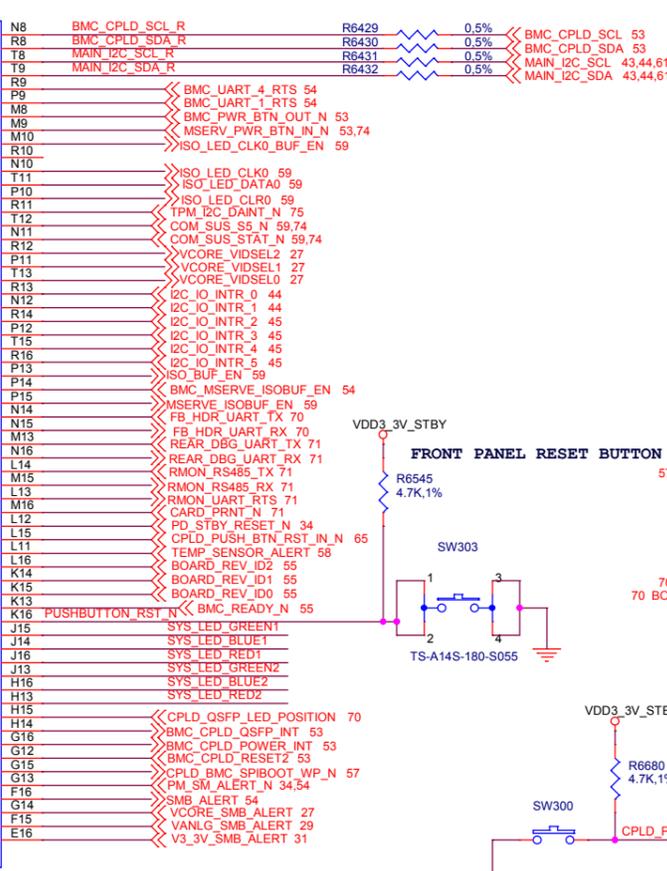
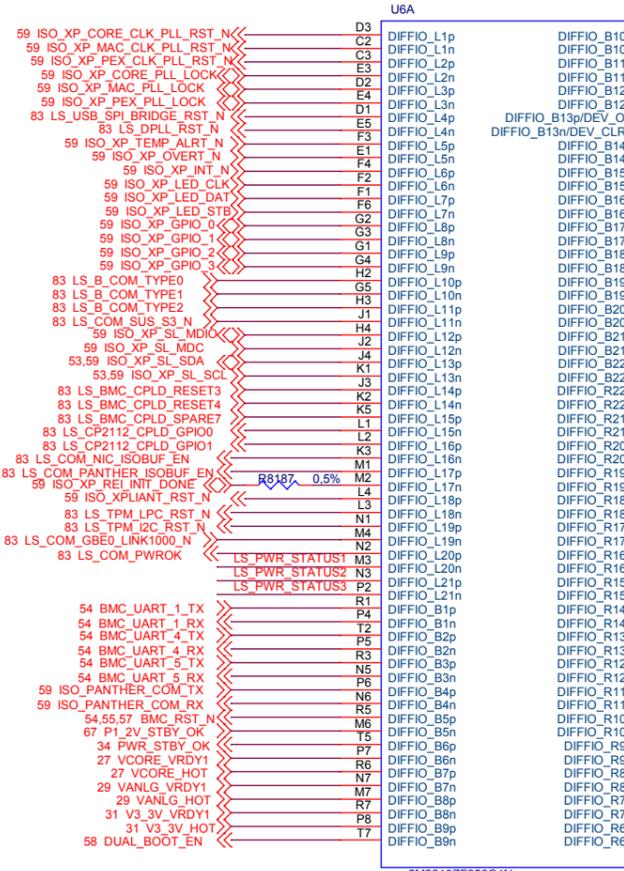
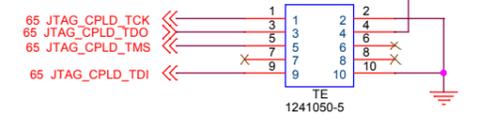
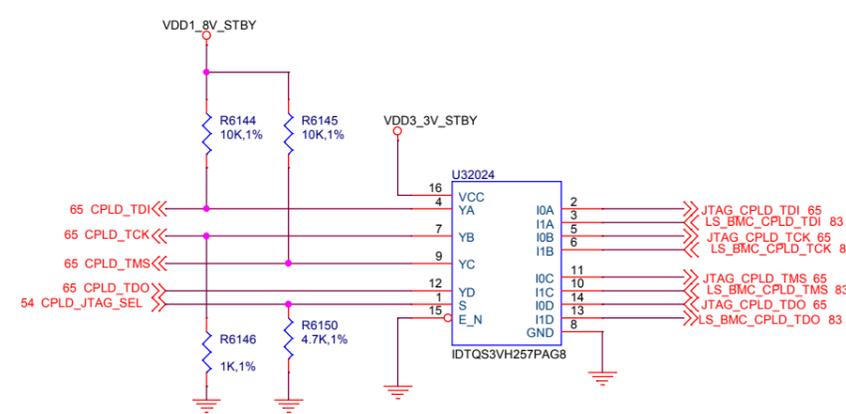
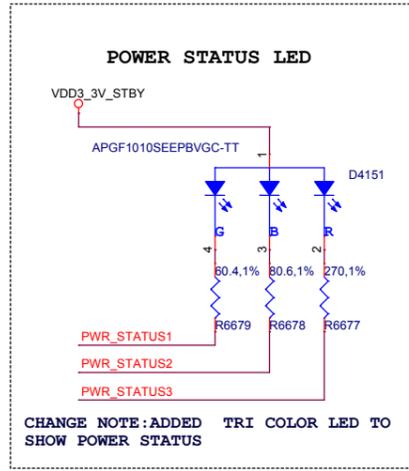
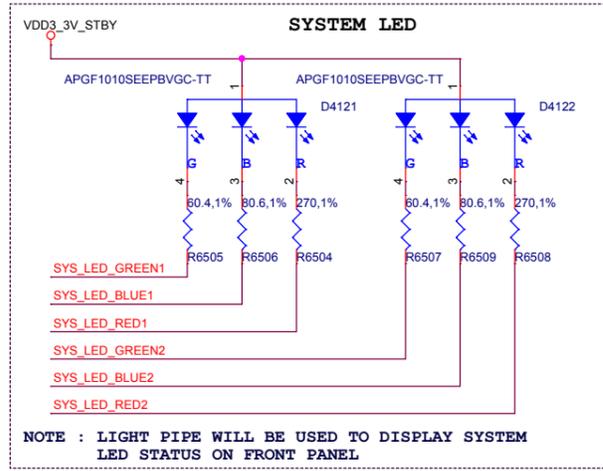
**BMC MDC FAN OUT BUFFER**



**FRONT PANEL PHY EEPROM**

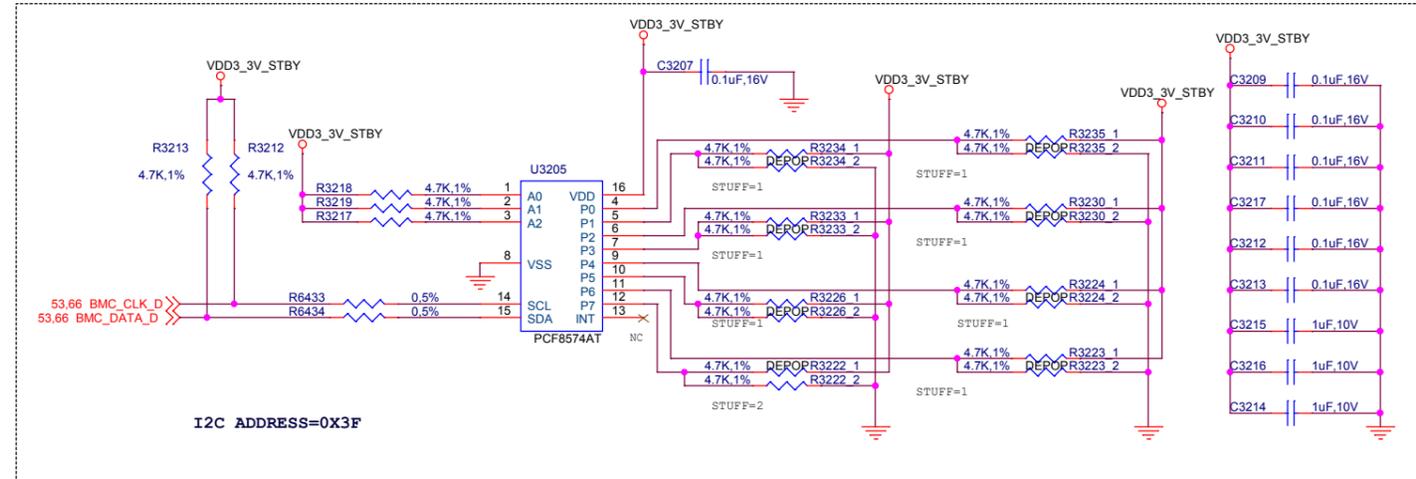


**FRONT PANEL PHY**

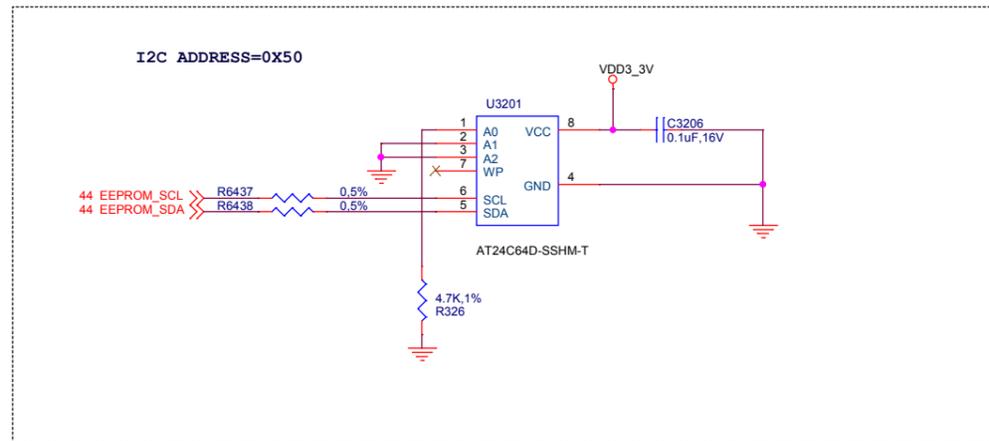


BOARD	BASE BOARD ID
WEDGE100C	0X3F

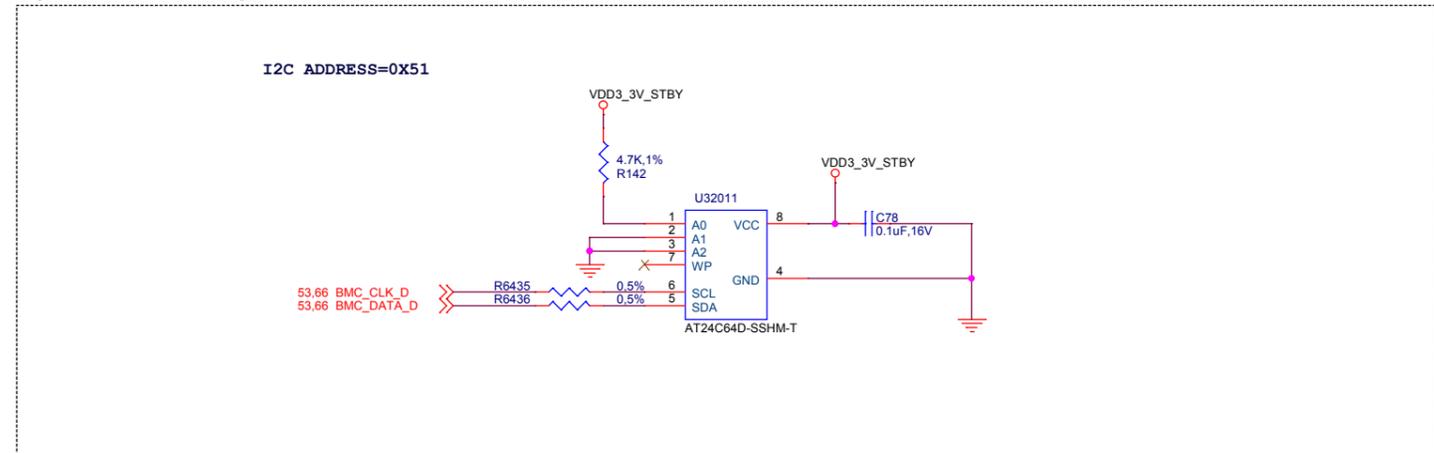
**I2C Baseboard ID = 0x3F**



**ADDITIONAL EEPROM**



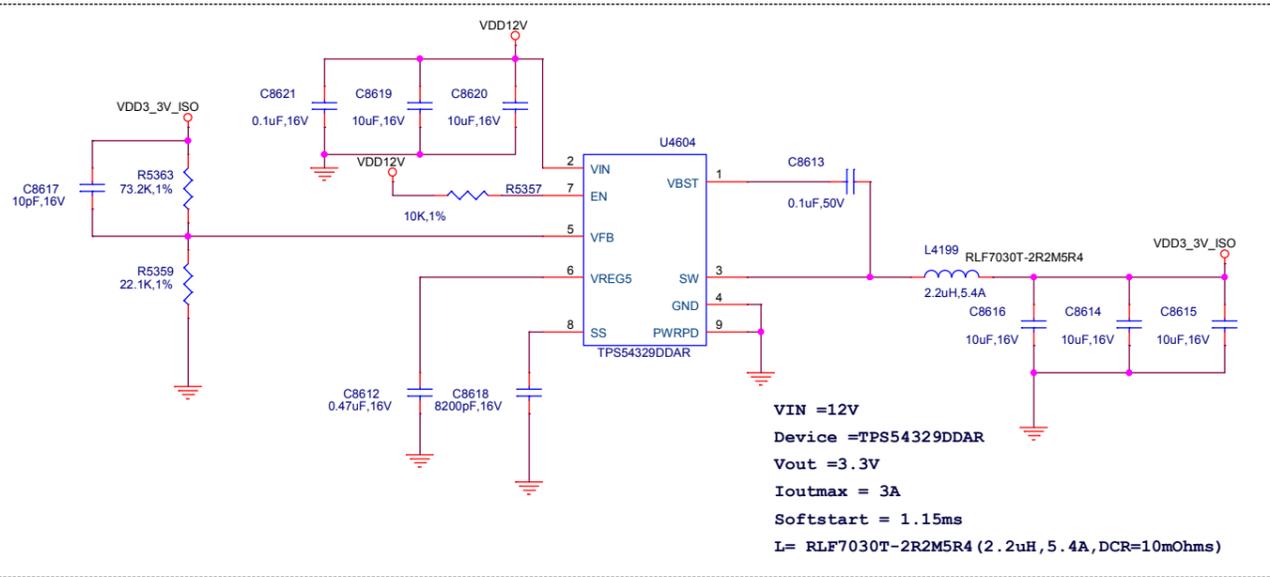
**BOARD ID EEPROM**



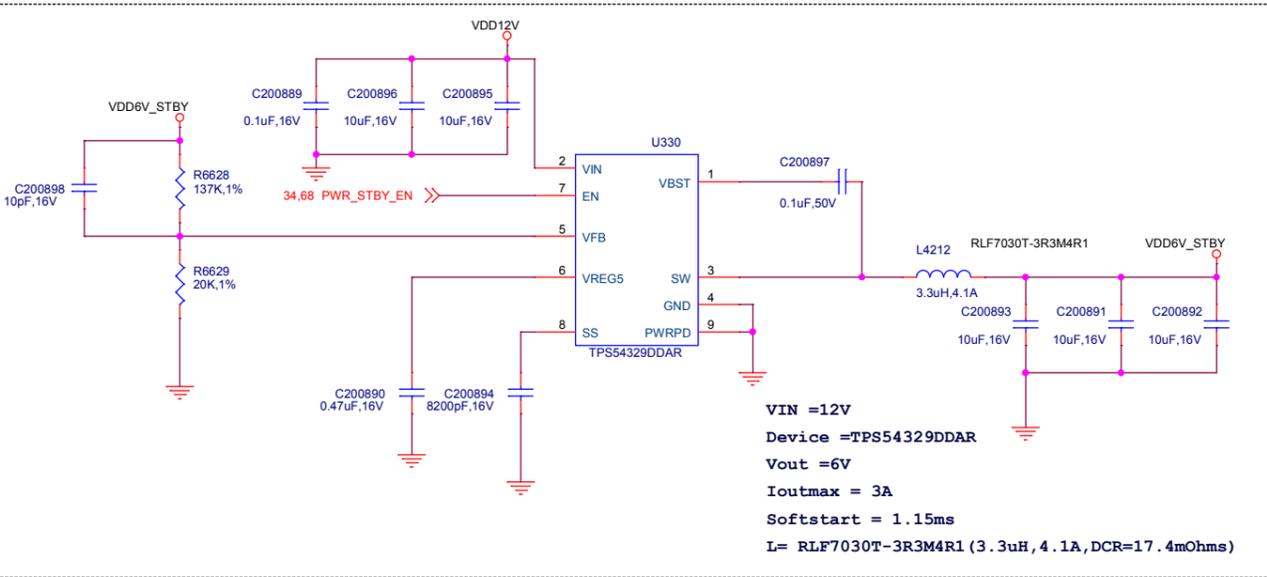
**BOARD ID & EEPROMS**

CAVIUM		
Title	WEDGE100C	
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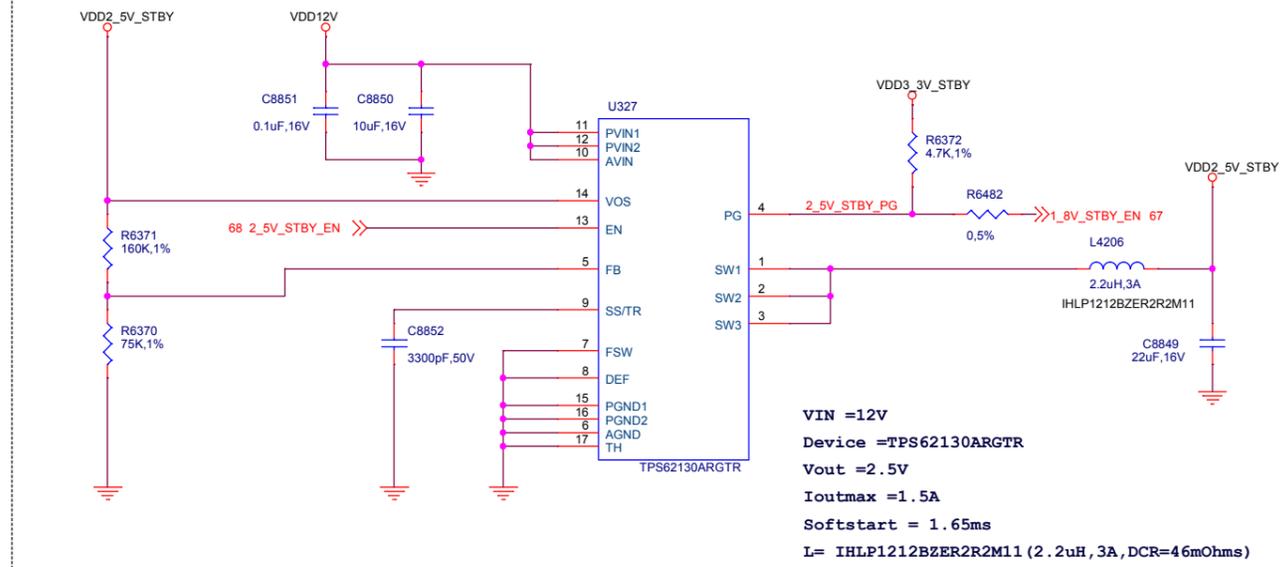
**PS 3.3V ISO, 3A**



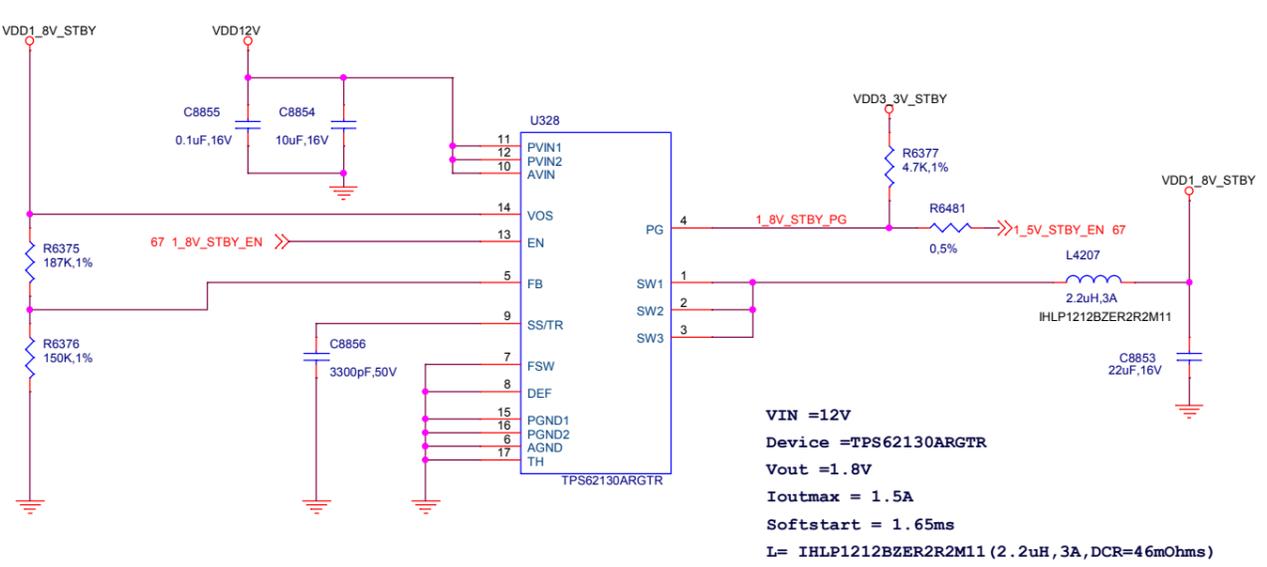
**PS 6V STBY, 1.5A**



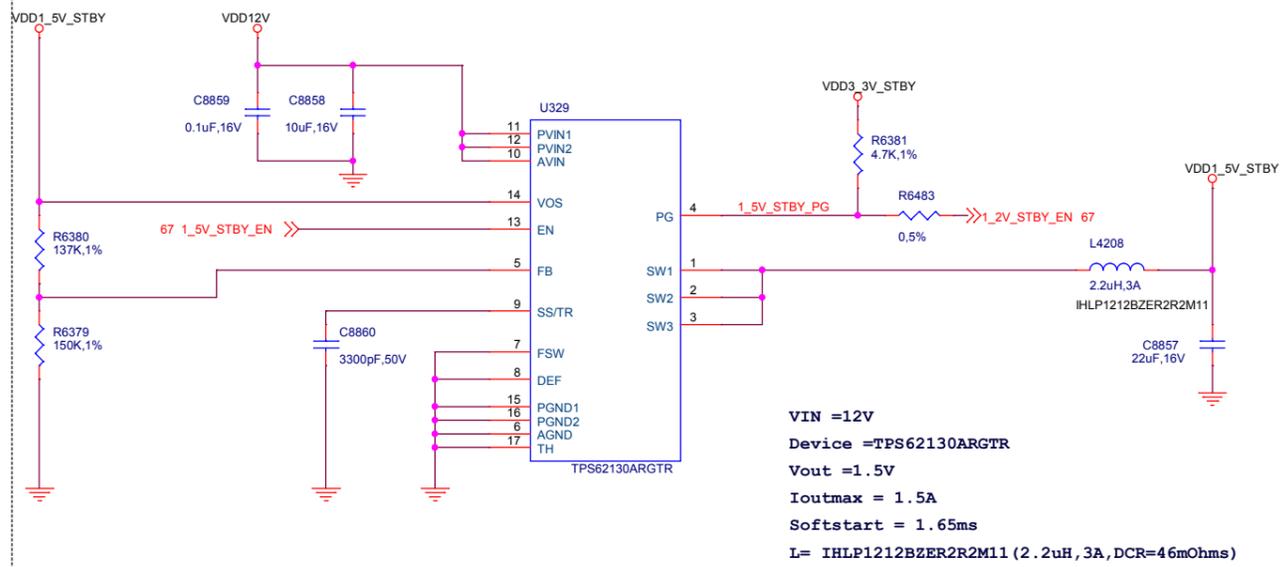
**2.5V STBY, 1.5A**



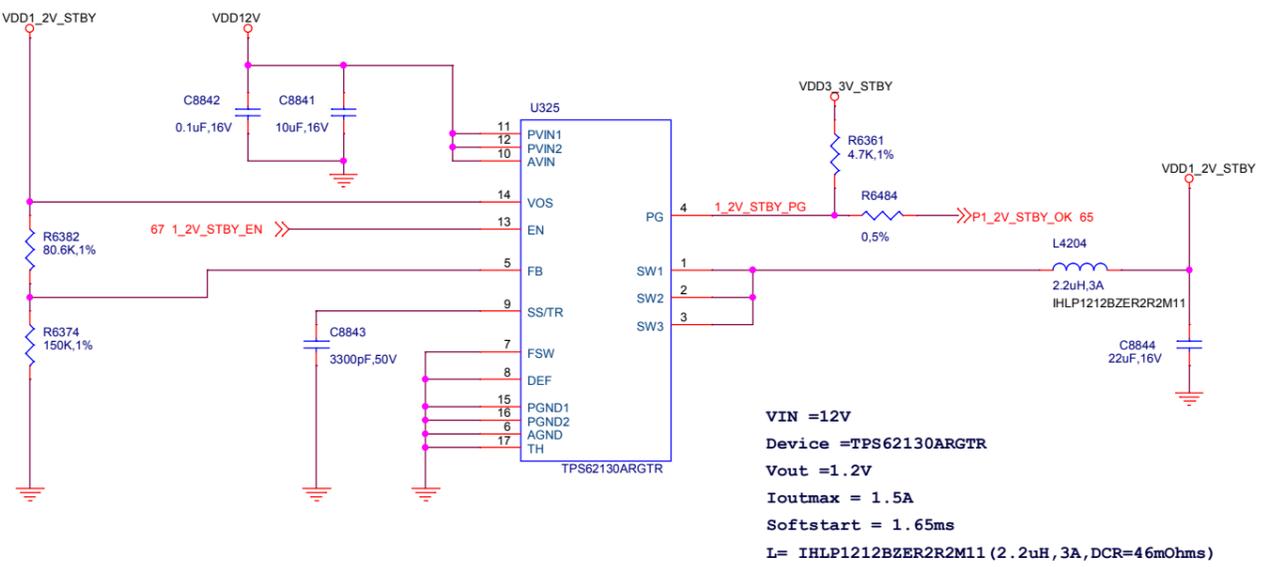
**PS 1.8V STBY, 1.5A**



**PS 1.5V STBY, 1.5A**



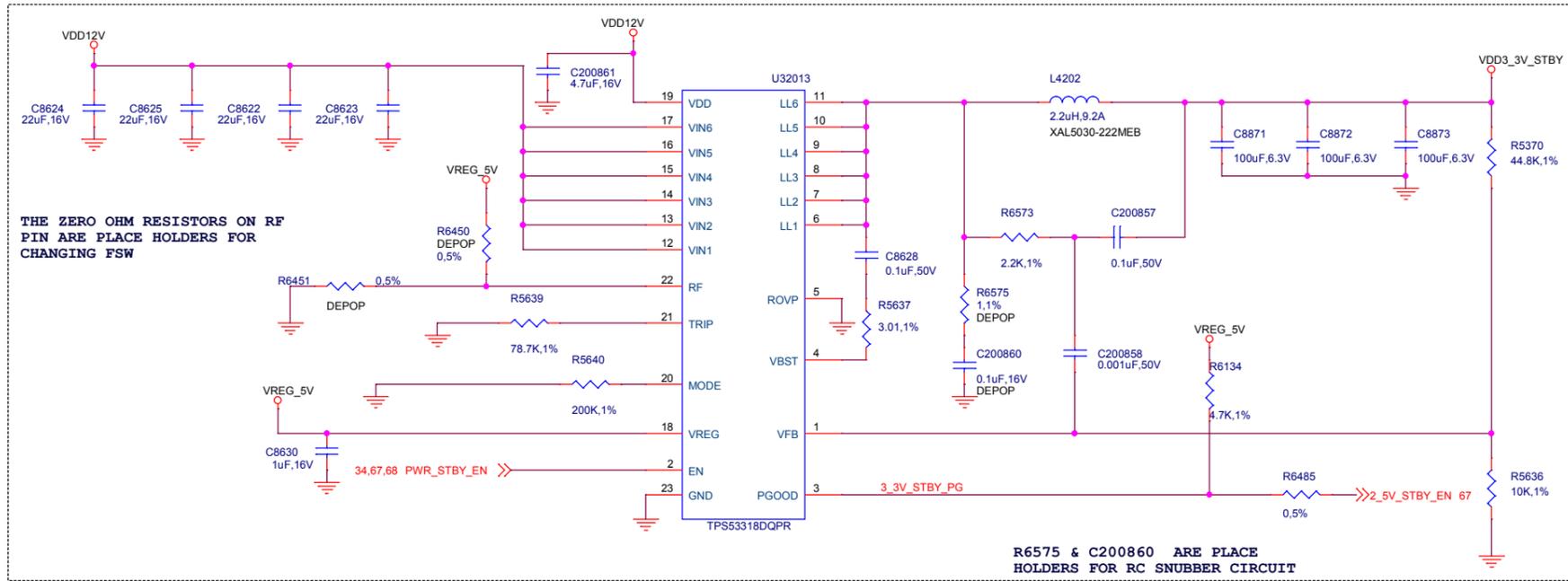
**PS1.2V STBY, 1.5A**



**STBY POWER**

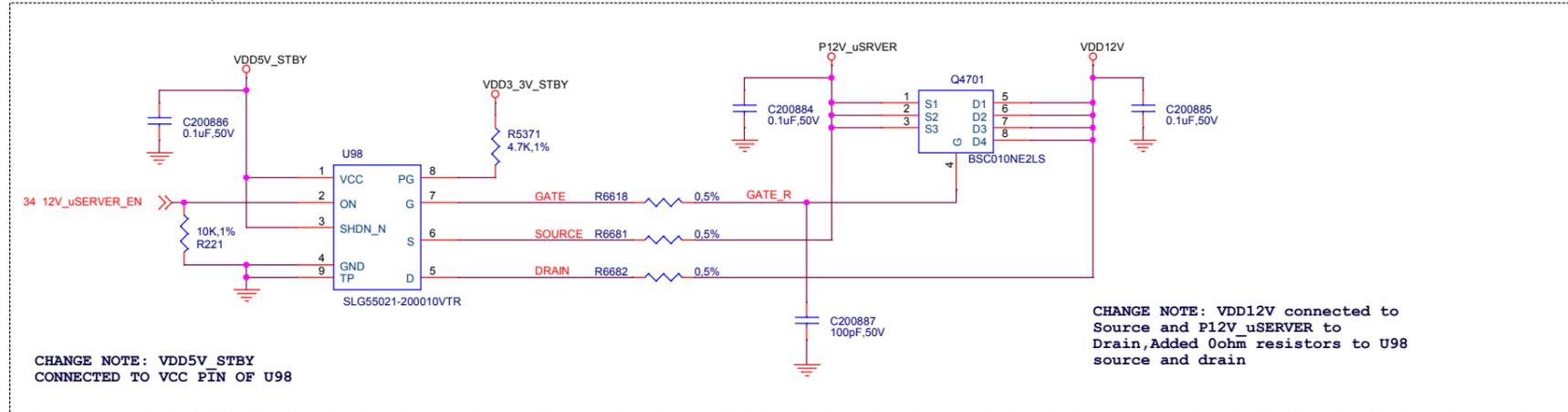
CAVIUM		
WEDGE100C		
Size	Document Number	Rev
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Date:	Thursday, December 22, 2016	Sheet 67 of 84

**PS 3.3V STBY ,6A**

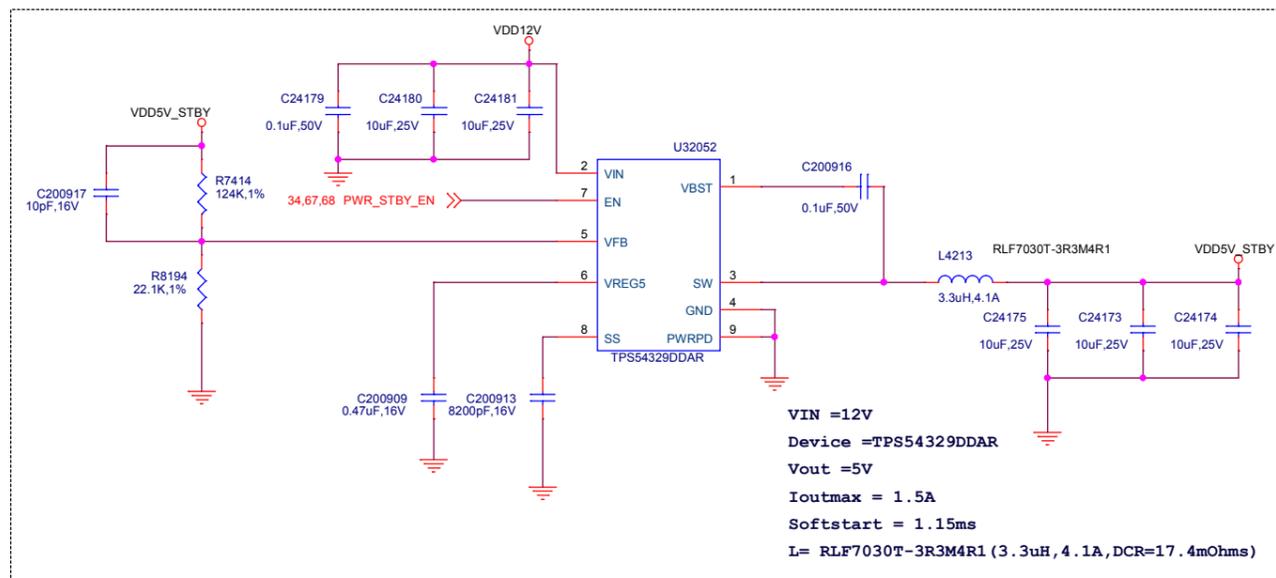


VIN =12V  
 Device =TPS53318DQPR  
 Vout =3.3V  
 Ioutmax = 6A  
 Iocp = 7.5A  
 Fsw= 500Khz  
 Rtrip= 78.7K  
 Rmode= 200K to GND: Softstart =2.8ms  
 L=XAL5030-222MEB (2.2uH, 9.2A,DCR=13.2mOhms)  
 Cout=GRM31CR60J107ME39L (CER,100UF,1206,6.3V)

**PS12V uSERVER, 4A**

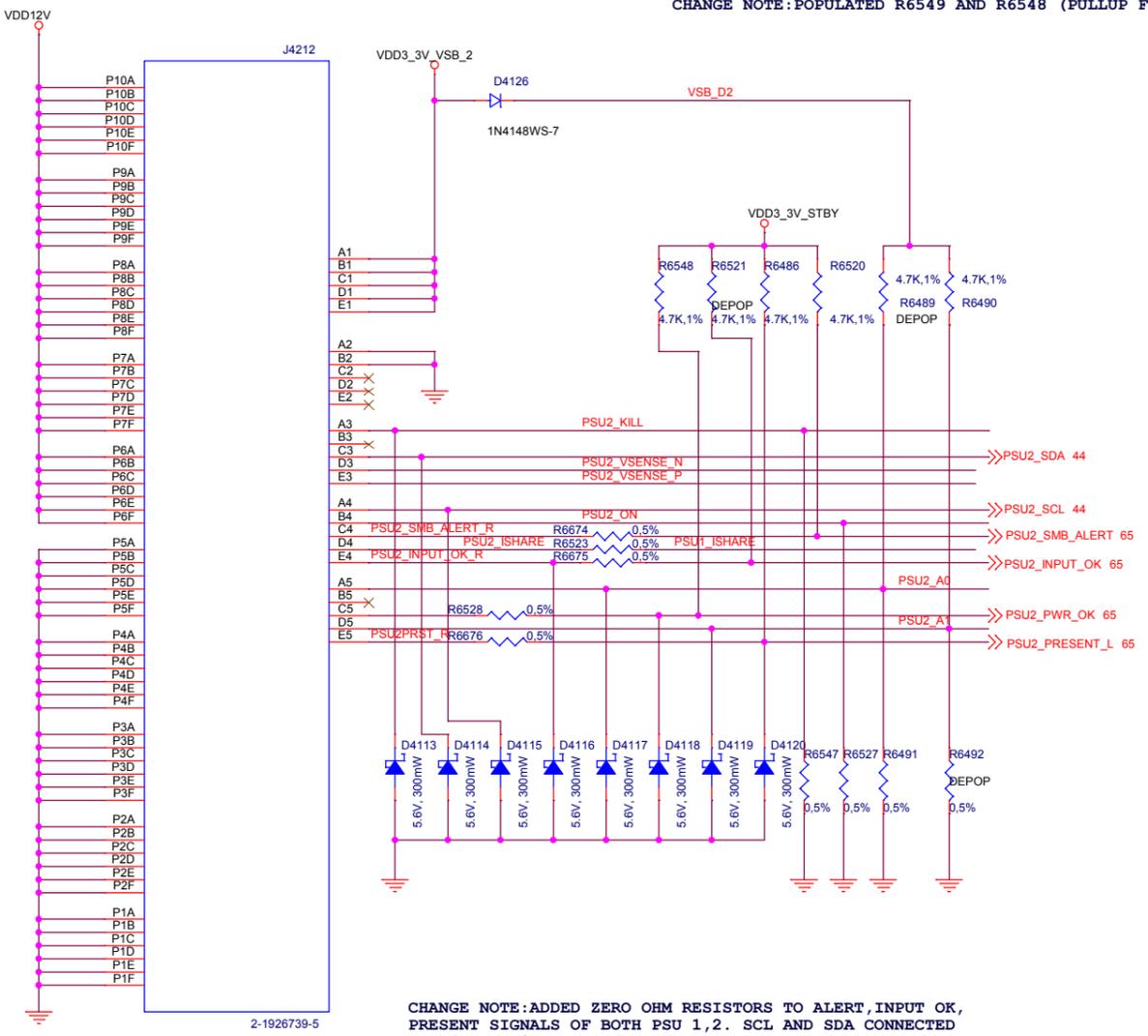
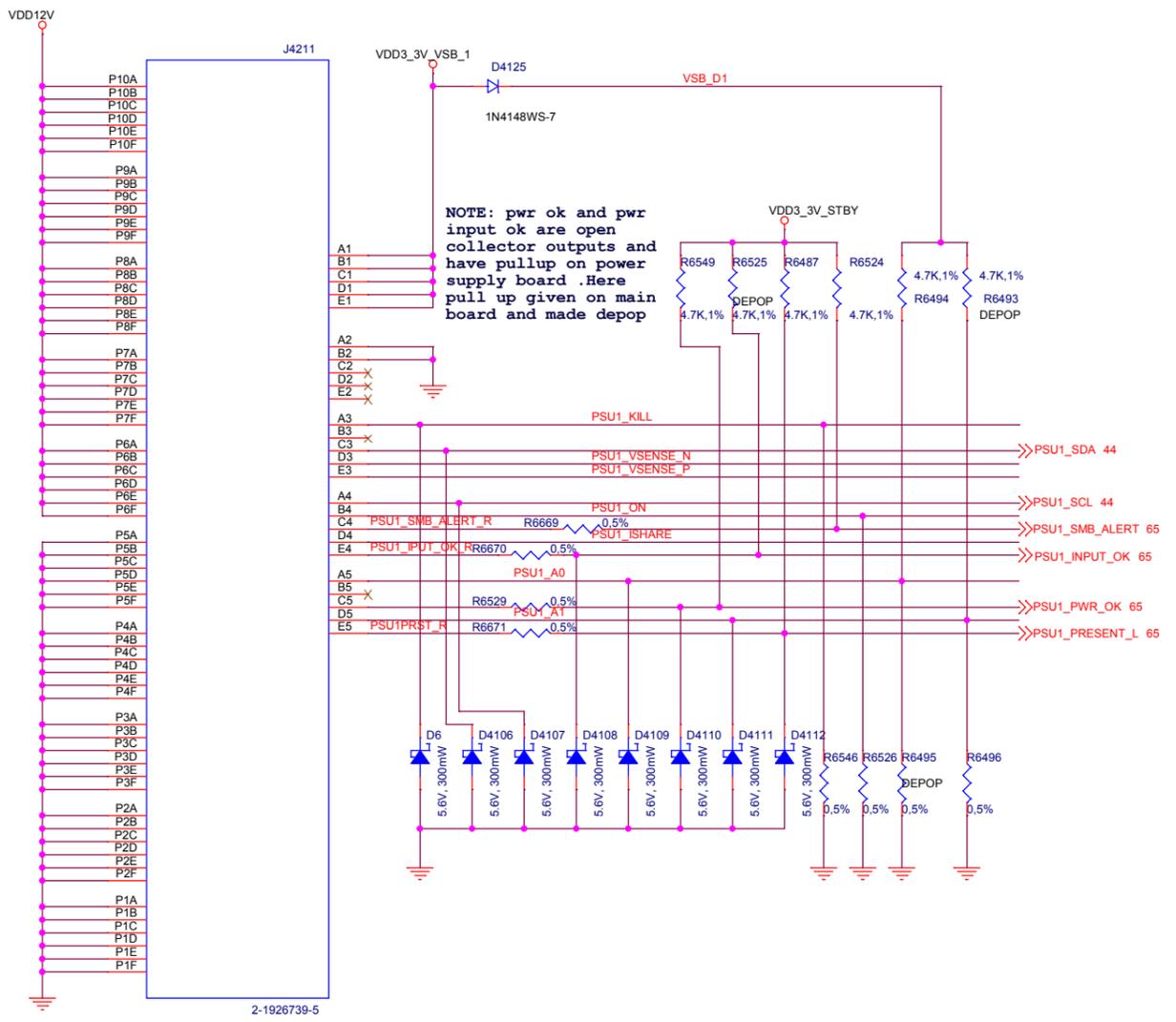
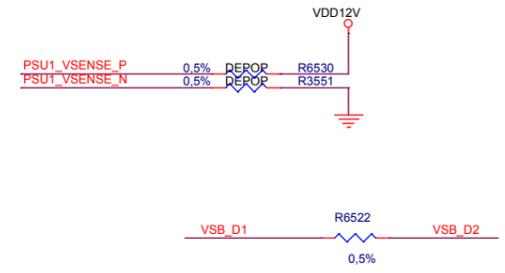


**PS 5V STBY, 1.5A**



**STBY POWER**

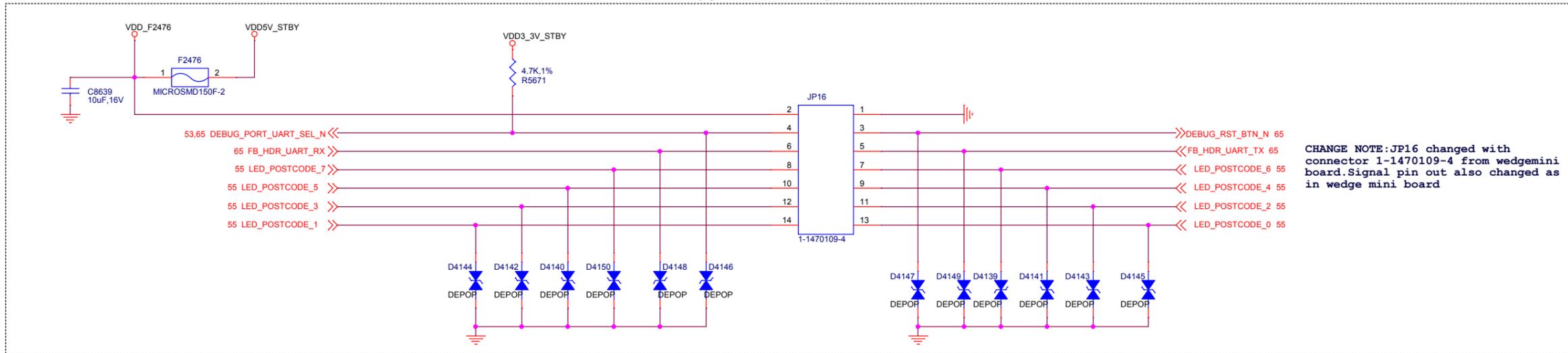
Title			CAVIUM
WEDGE100C			
Size	Document Number	Rev	
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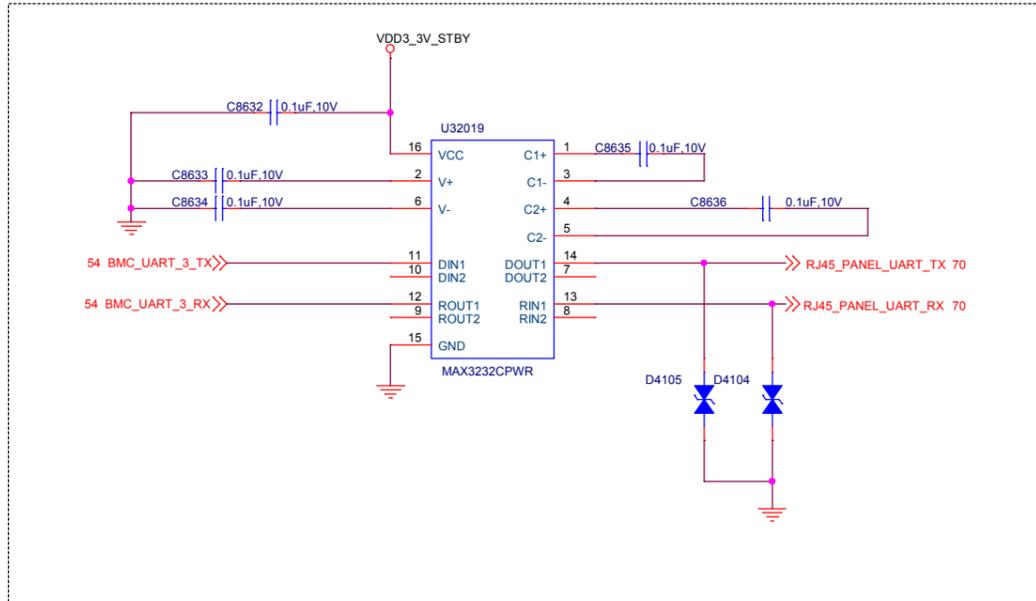
# POWER CONNECTOR

CAVIUM		
Title <b>WEDGE100C</b>		
Size C	Document Number 80-00010-03	Rev 2.0
Date:	Thursday, December 22, 2016	Sheet 69 of 84

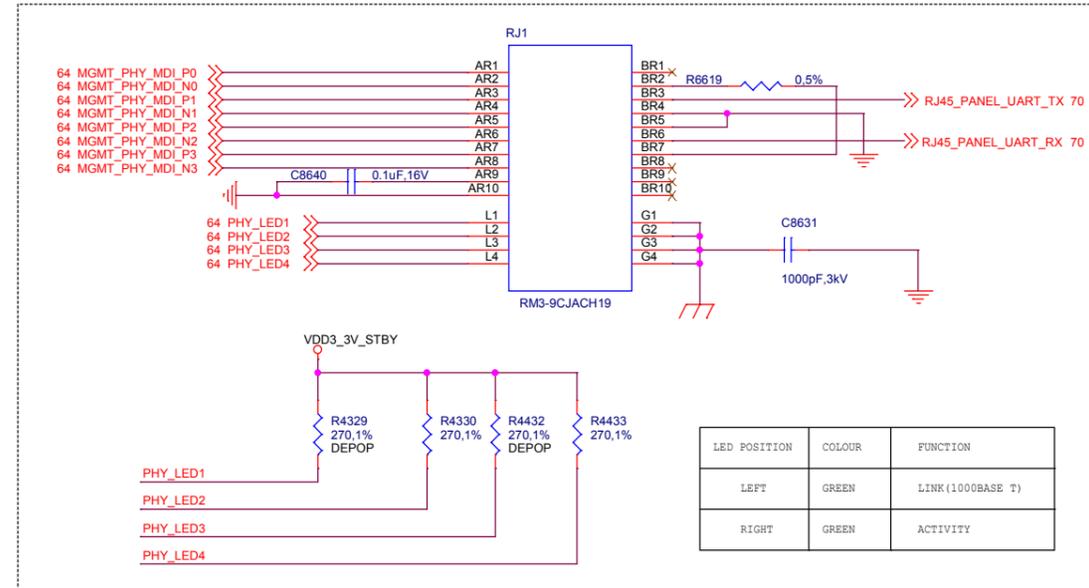
### FB DEBUG HEADER PORT



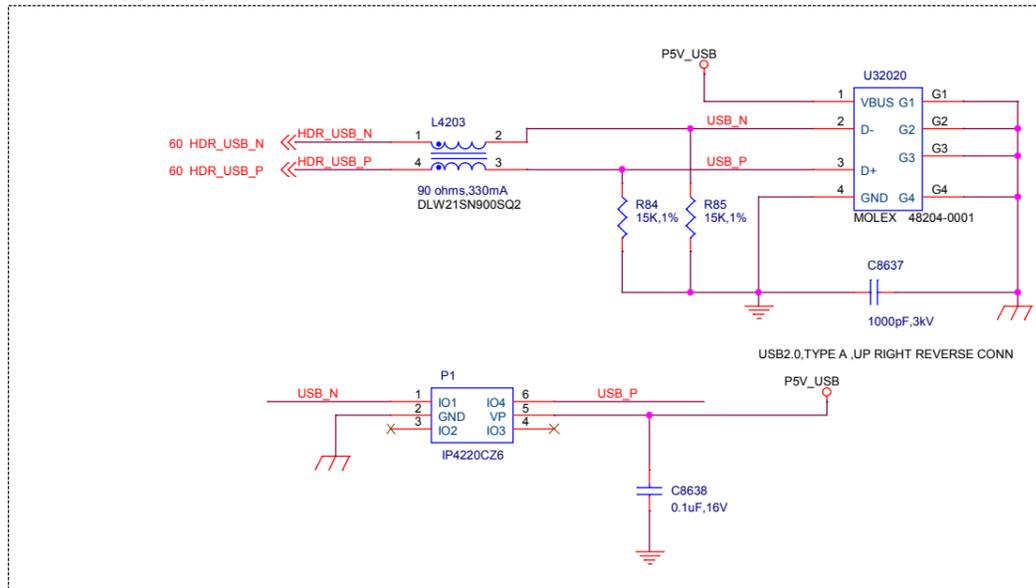
### PANEL UART TRANSEIVER



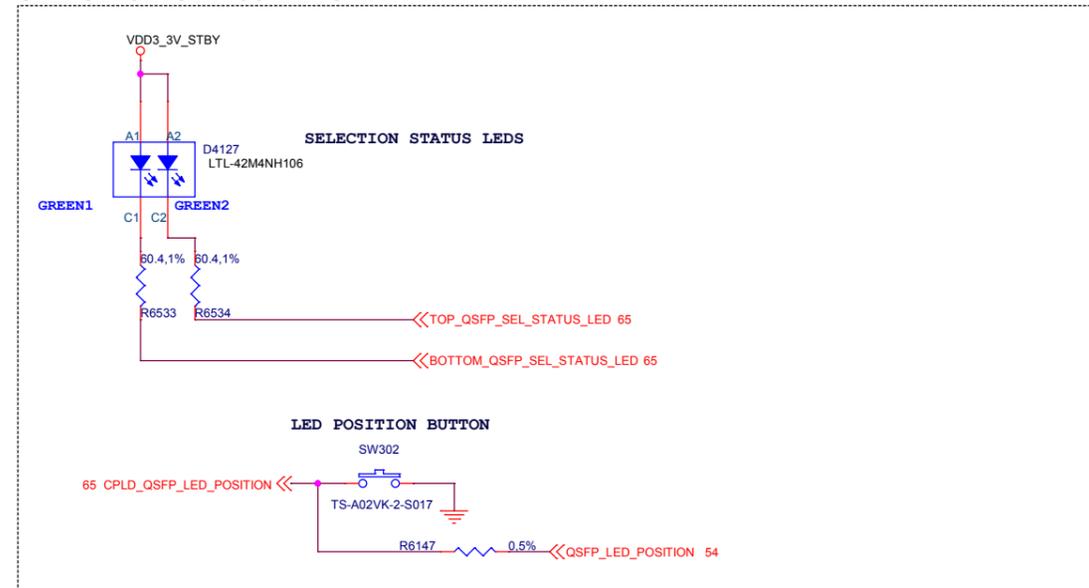
### MANAGEMENT PORT AND PANEL UART CONSOLE



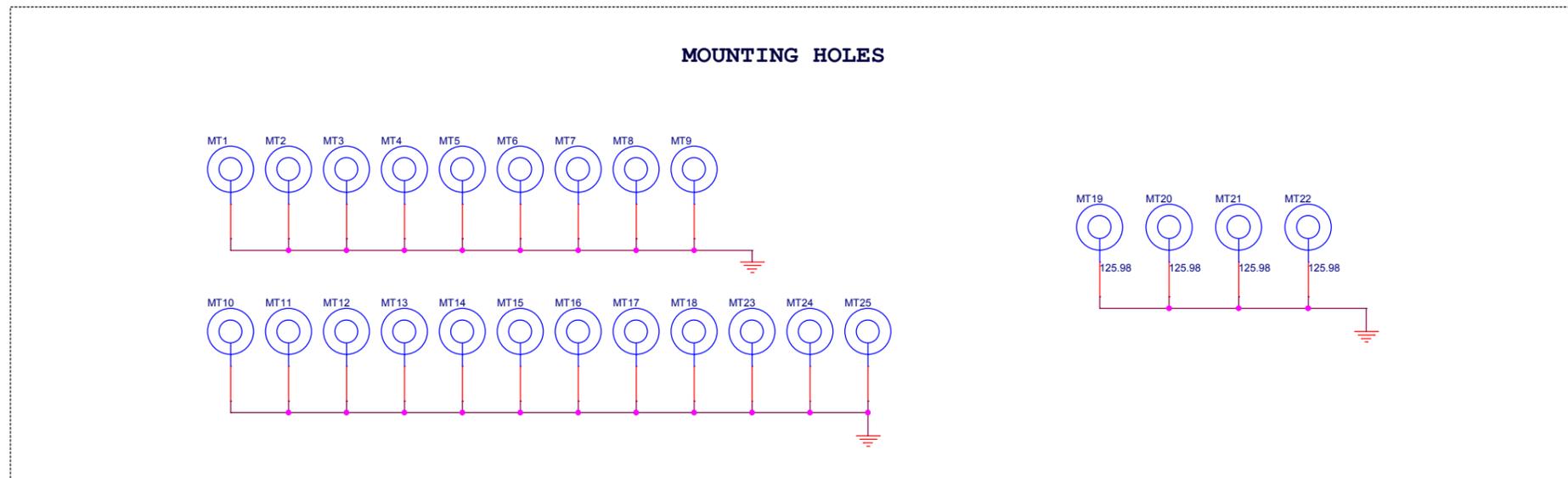
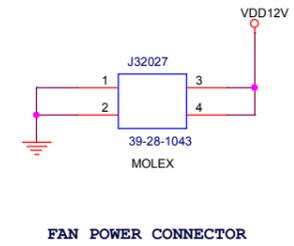
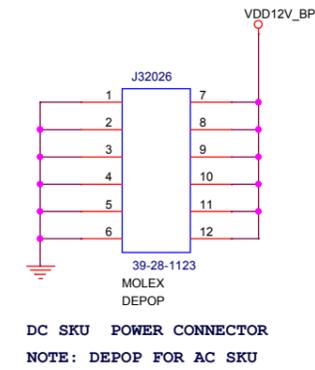
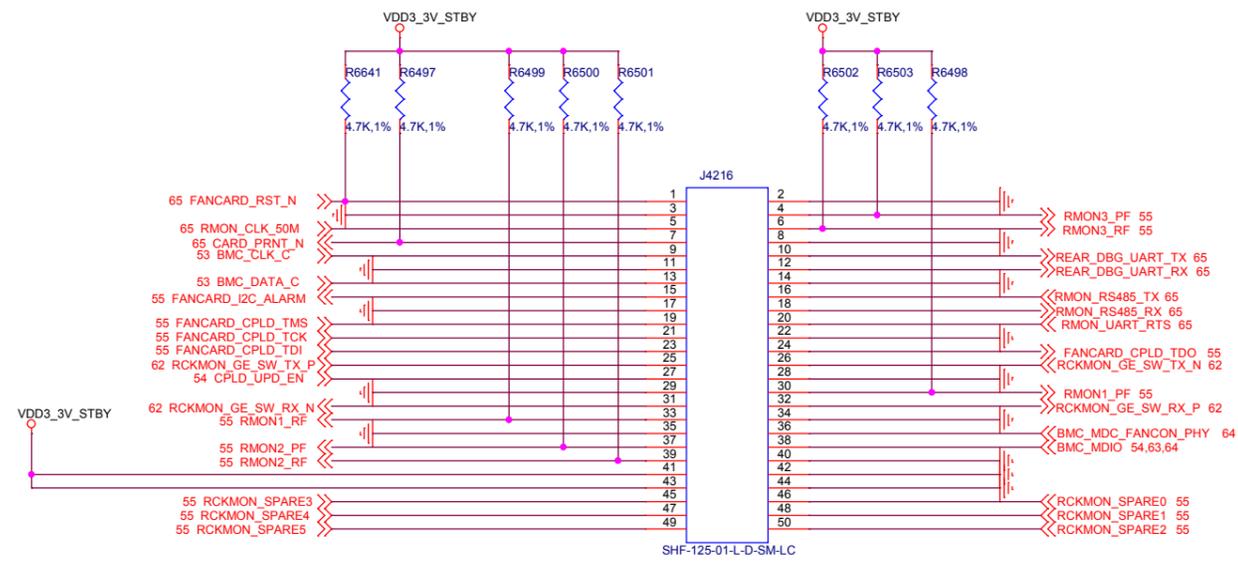
### TYPE A USB PORT



### SELECTION STATUS LEDES

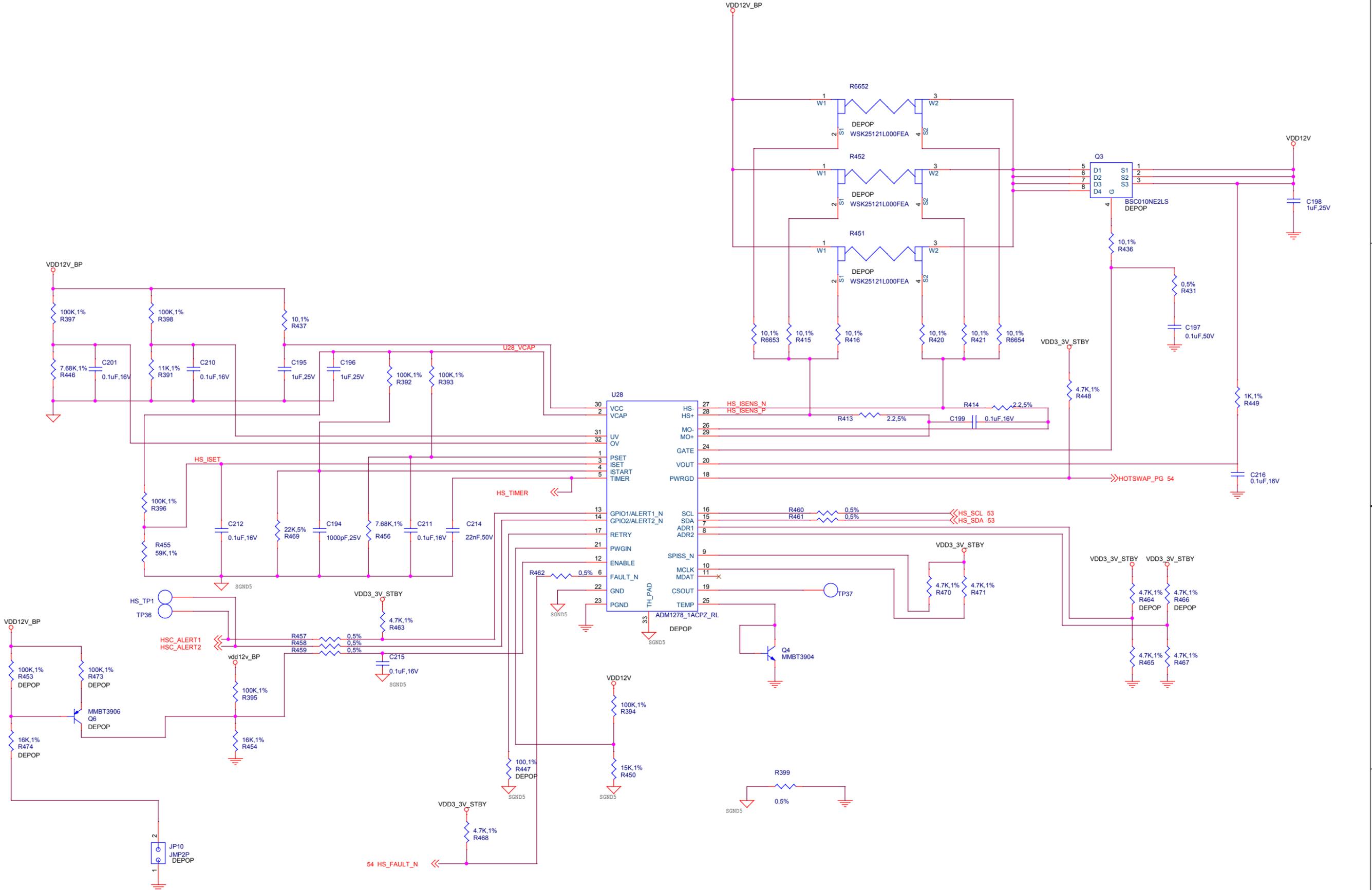


# FRONT PANEL CONNECTORS



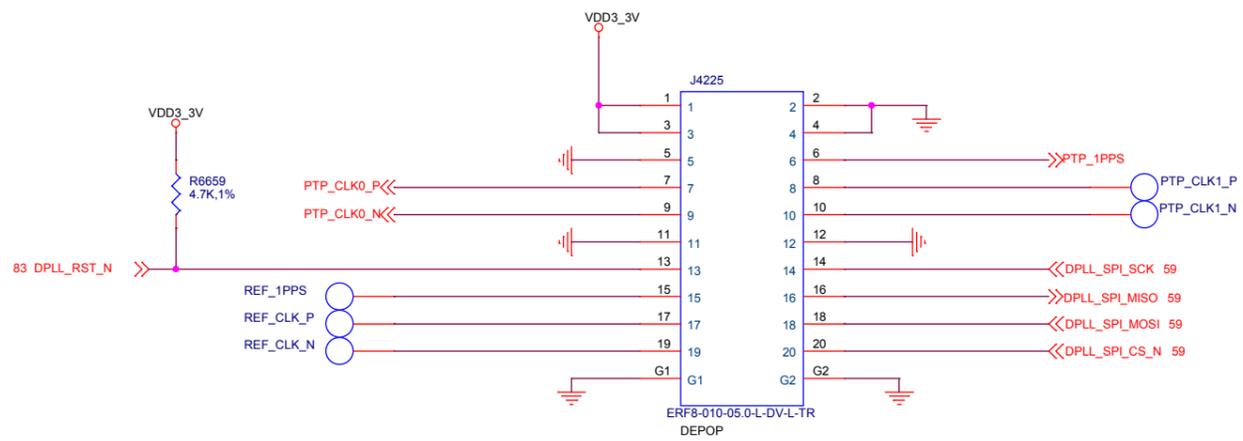
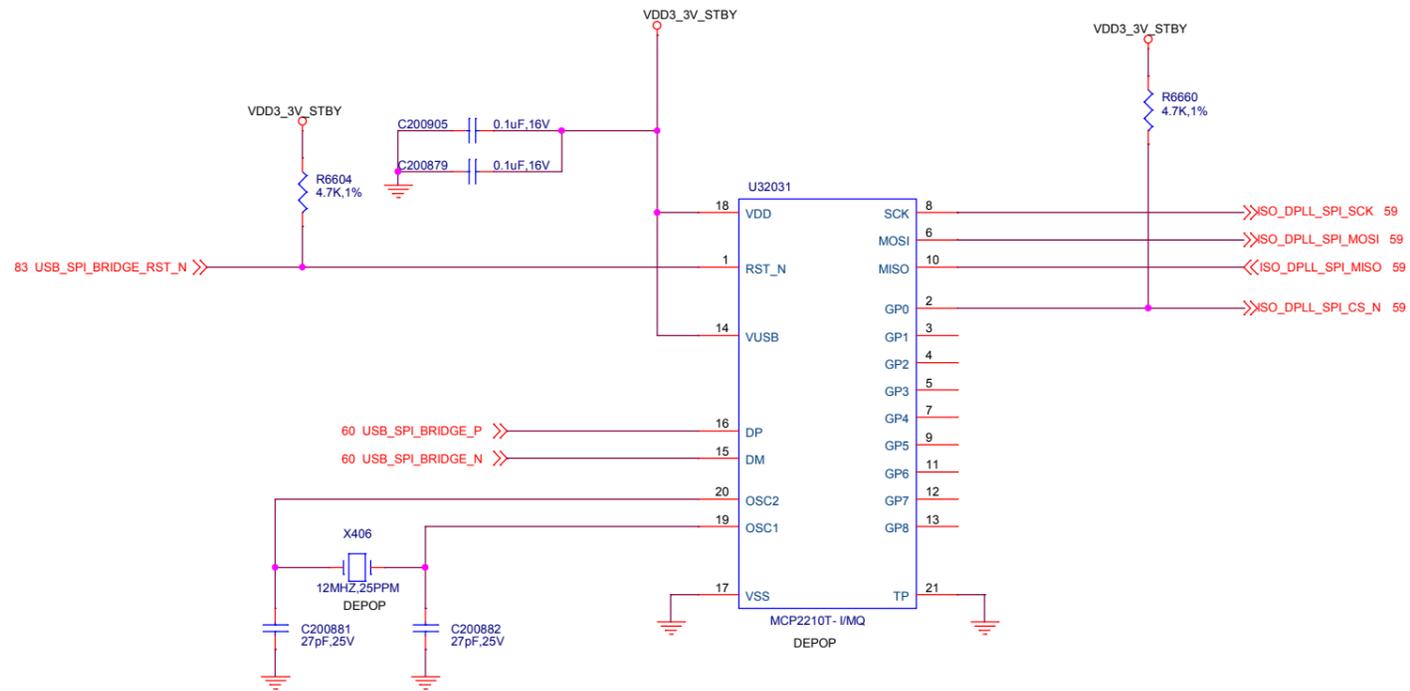
# RACKMON & FAN CONNECTOR

<b>CAVIUM</b>		
<b>WEDGE100C</b>		
Title		
Size	Document Number	Rev
C	80-00010-03	2.0
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# HOTSWAP CKT

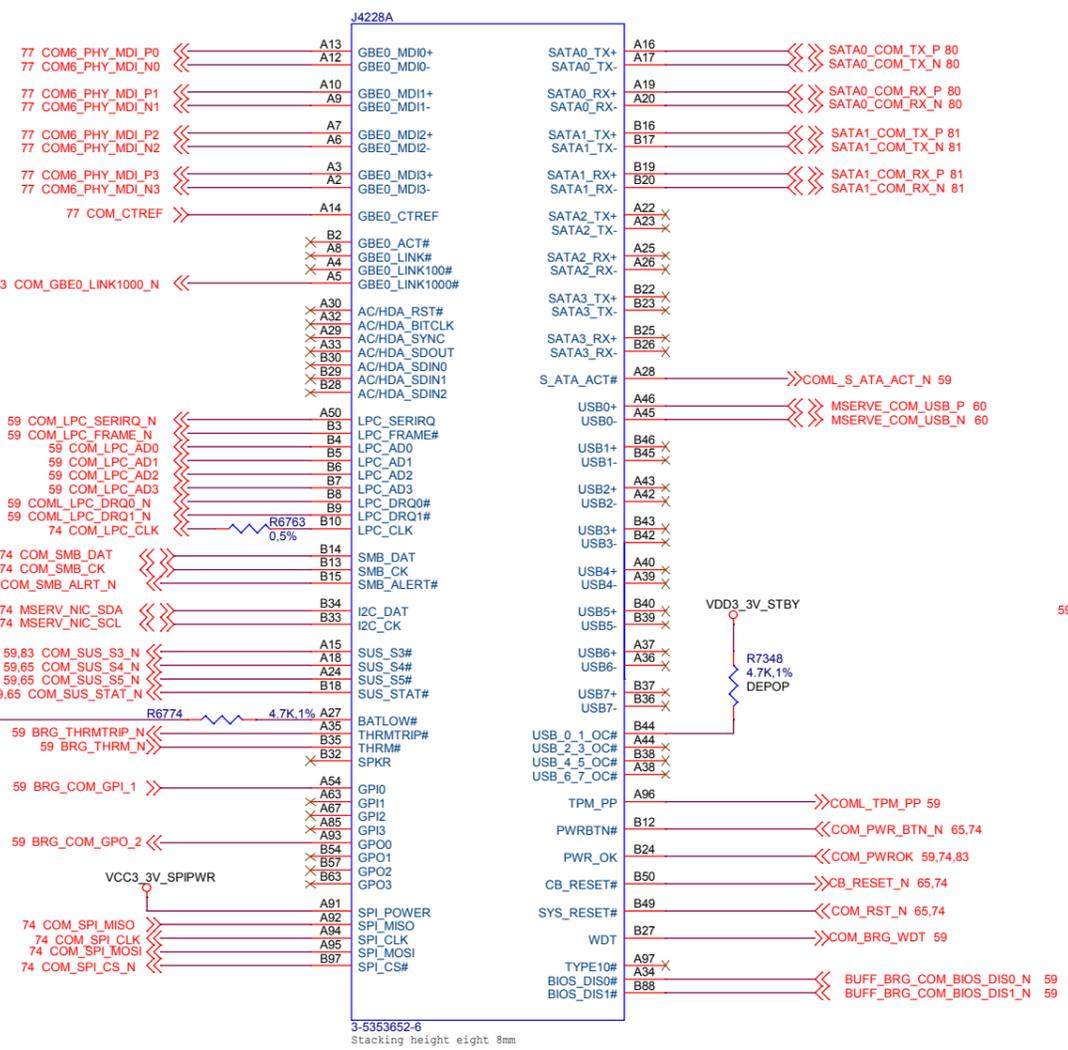
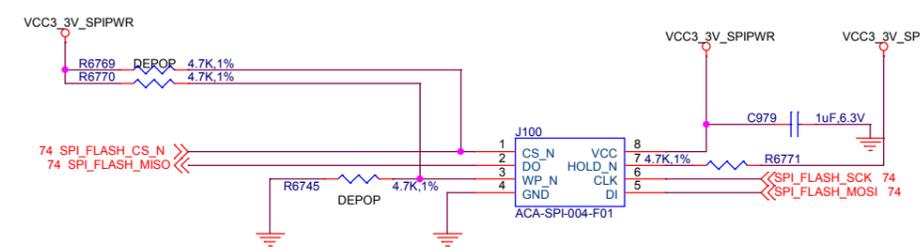
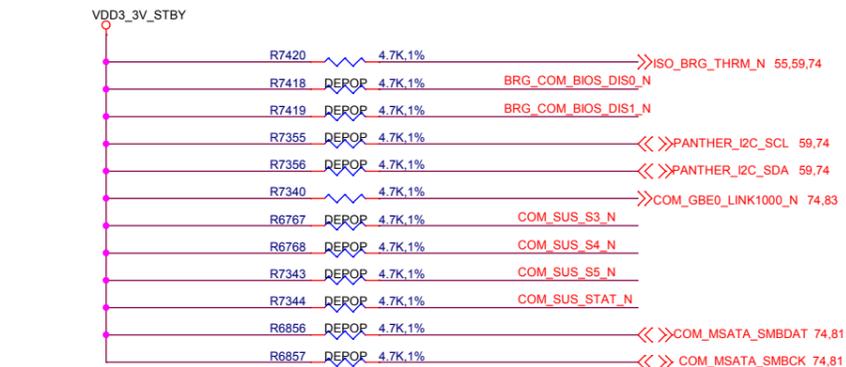
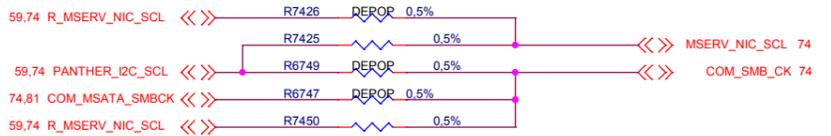
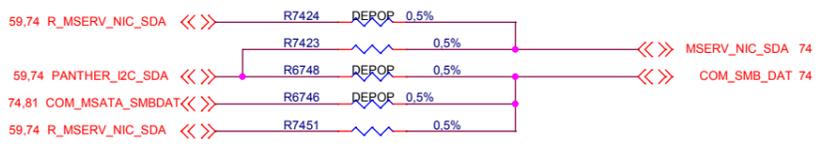
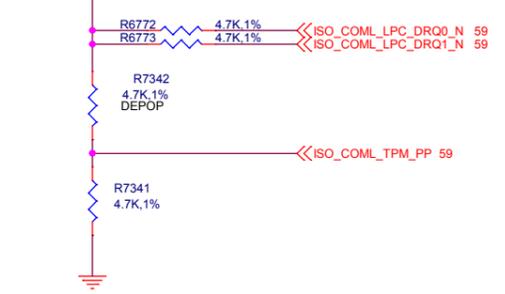
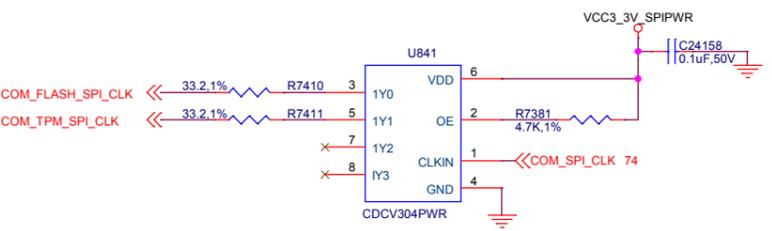
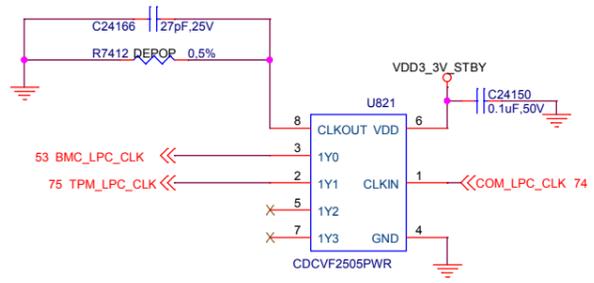
CAVIUM		
Title: WEDGE100C		
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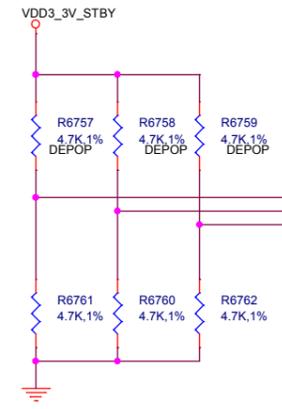
# DPLL CONN & SPI BRIDGE

CAVIUM		
Title <b>WEDGE100C</b>		
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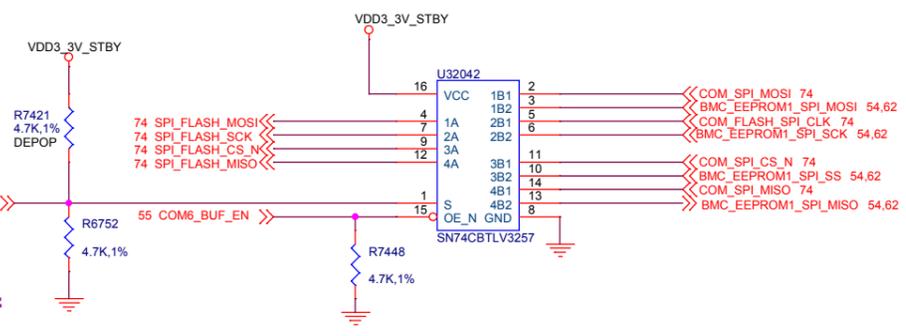
PLACE HOLDER TO ADJUST DELAY IF REQUIRED



3-5353652-6  
Stacking height eight 8mm



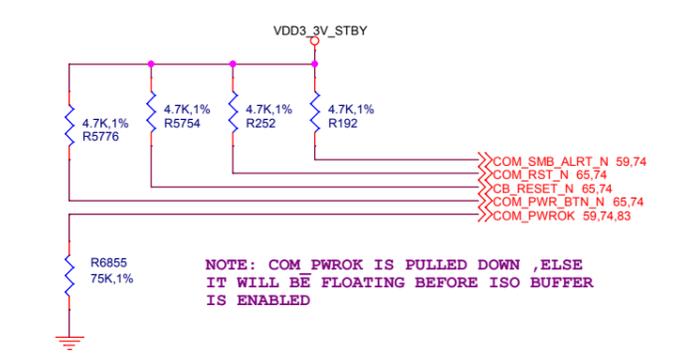
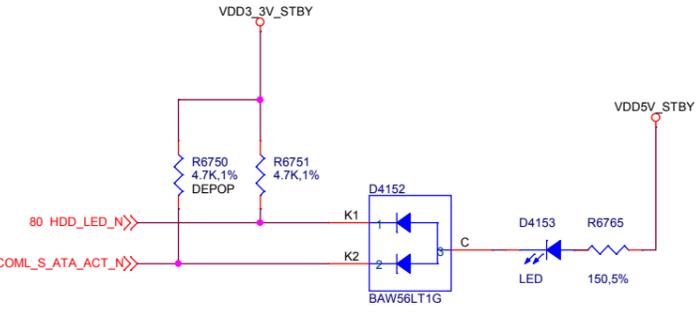
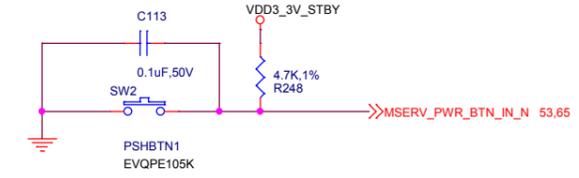
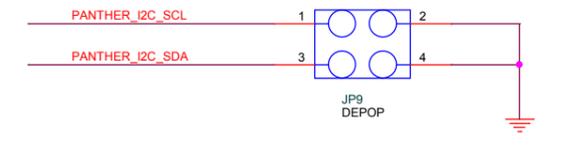
I2C ADDRESS=0X20



NOTE: COM SPI SEL AND SWITCH EEPROM1 WRT , SWITCH1 EEPROM1 WRT SHOULD NOT BE ENABLED AT SAME TIME BECAUSE SPI SIGNALS ARE SHARED



NOTE: SPI FLASH U99 NEED TO BE PLACED IN J100

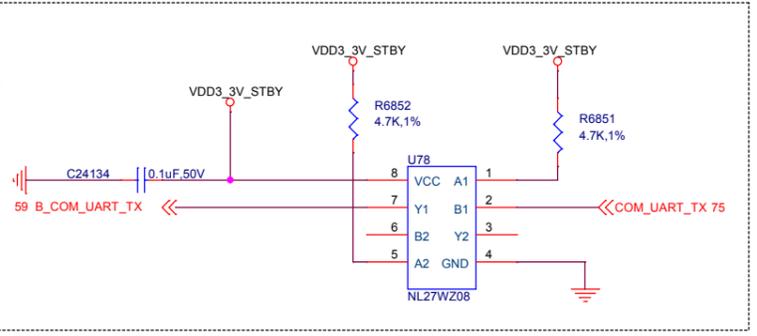
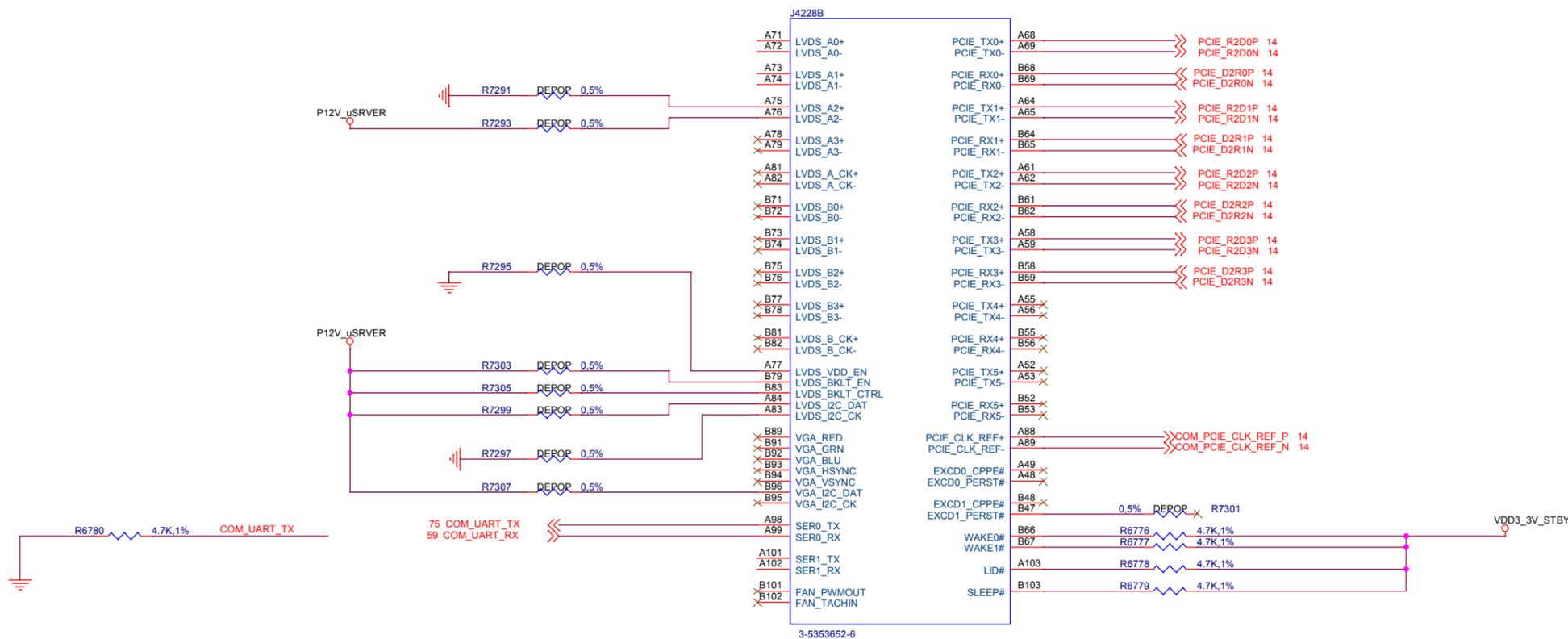


NOTE: COM PWROK IS PULLED DOWN , ELSE IT WILL BE FLOATING BEFORE ISO BUFFER IS ENABLED

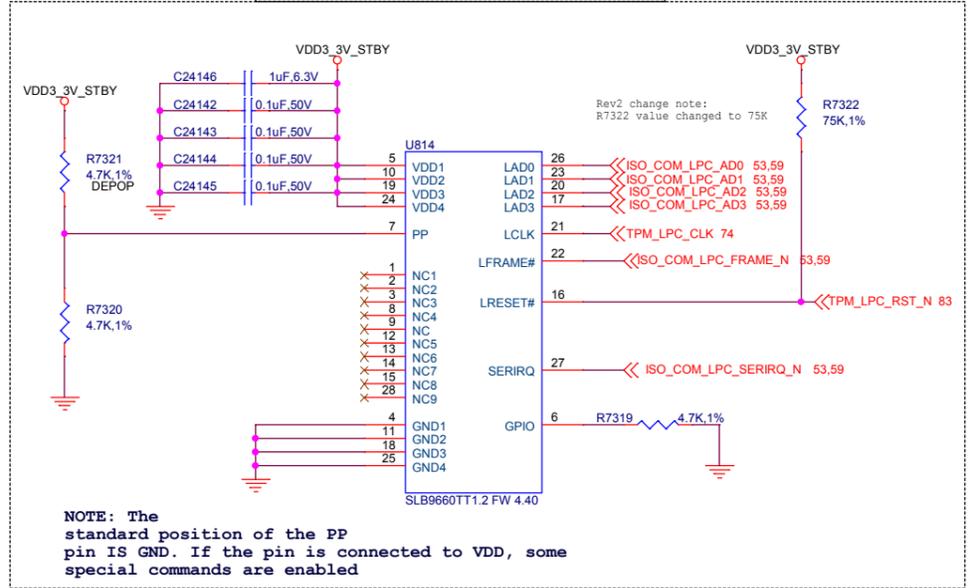
Rev2 change note:  
R6855 value changed to 75K

# COM6 CONNECTOR PAGE 1

CAVIUM	
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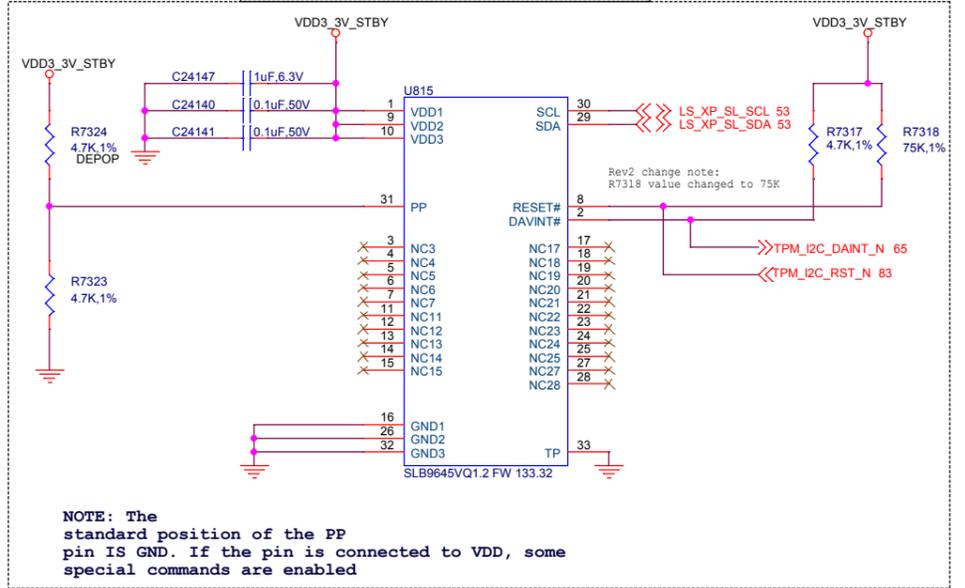


**TPM BASED LPC**



NOTE: The standard position of the PP pin IS GND. If the pin is connected to VDD, some special commands are enabled

**I2C BASED TPM**

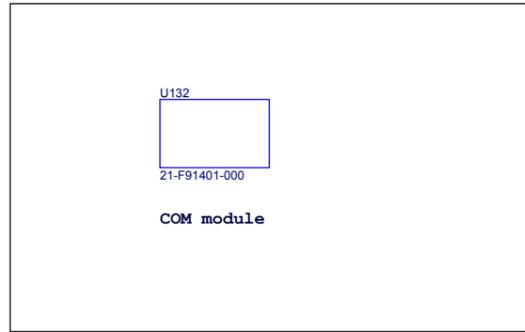
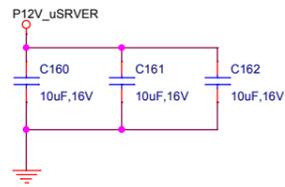


NOTE: The standard position of the PP pin IS GND. If the pin is connected to VDD, some special commands are enabled

COMe INTEGRATION CHANGE NOTE:  
MUX TO SELECT BMC OR COM SPI TO TPM MODULE DELETED

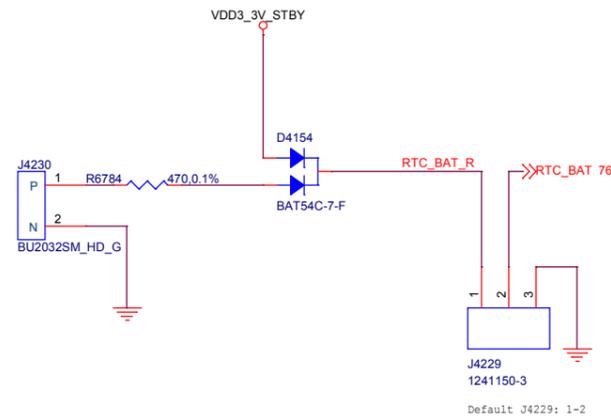
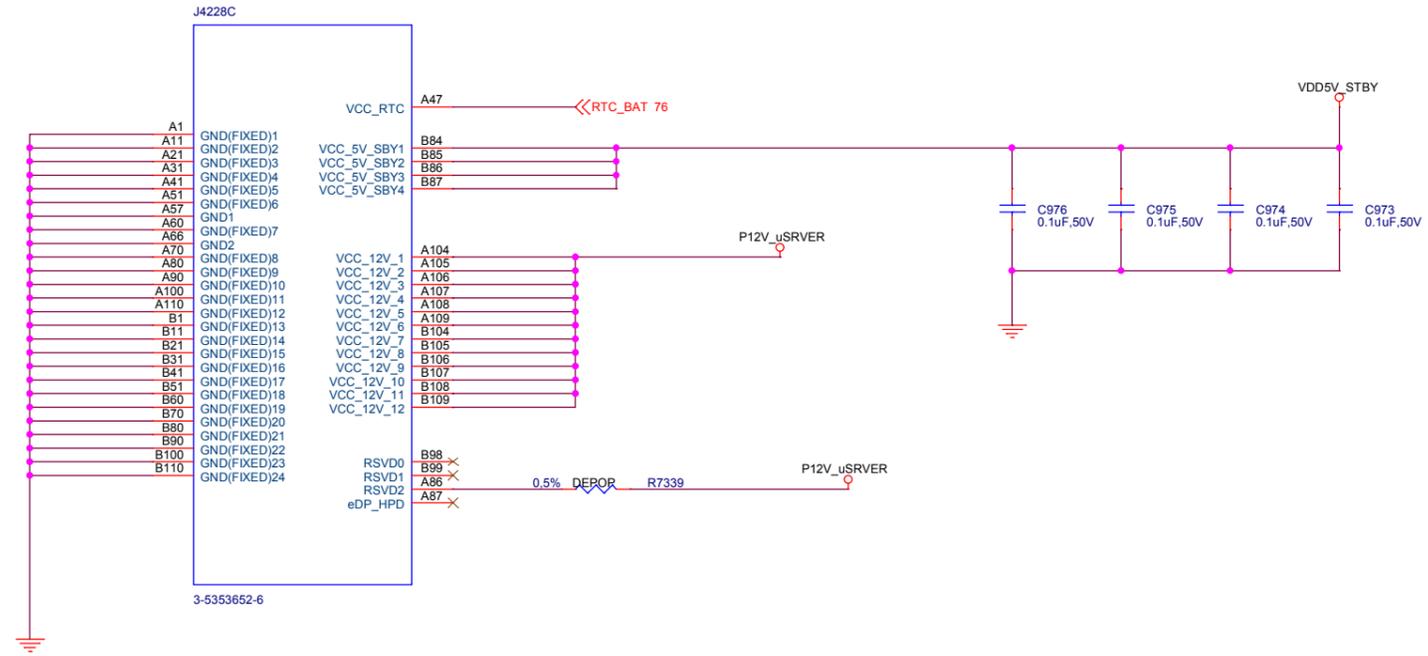
**COM6 CONNECTOR PAGE 2**

CAVIUM			
Title	WEDGE100C		
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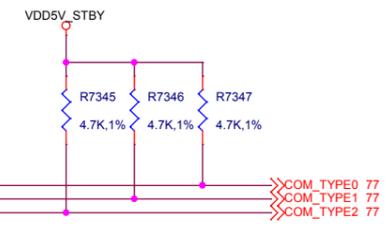
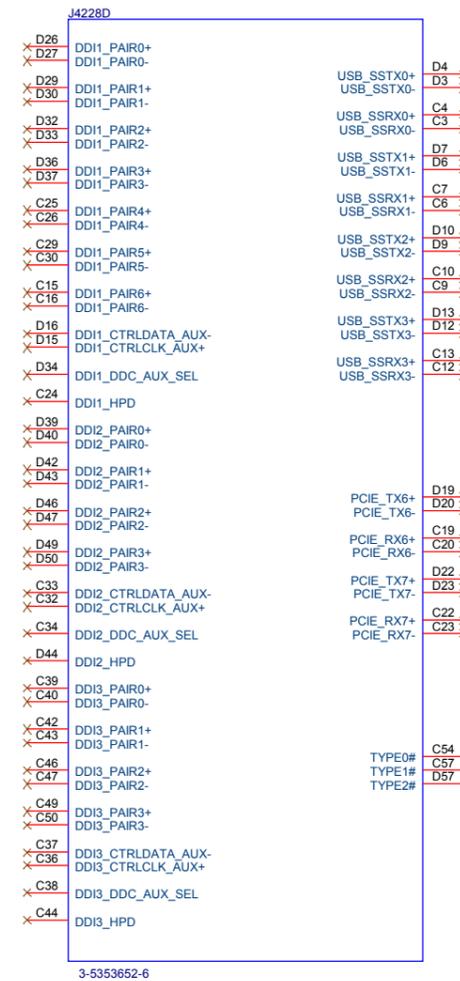
**PEM NUTS**

COMe INTEGRATION CHANGE NOTE:  
PEM NUTS FOR COMe MODULE ADDED

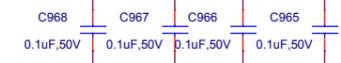
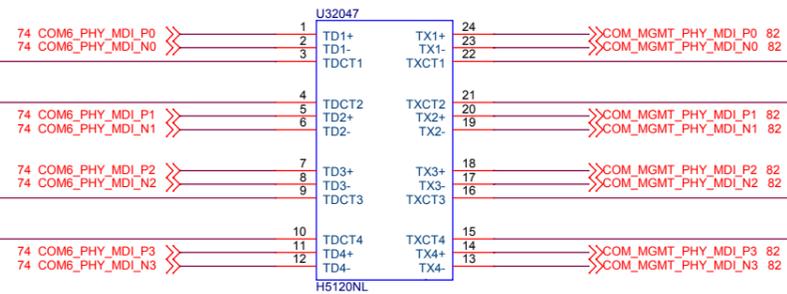
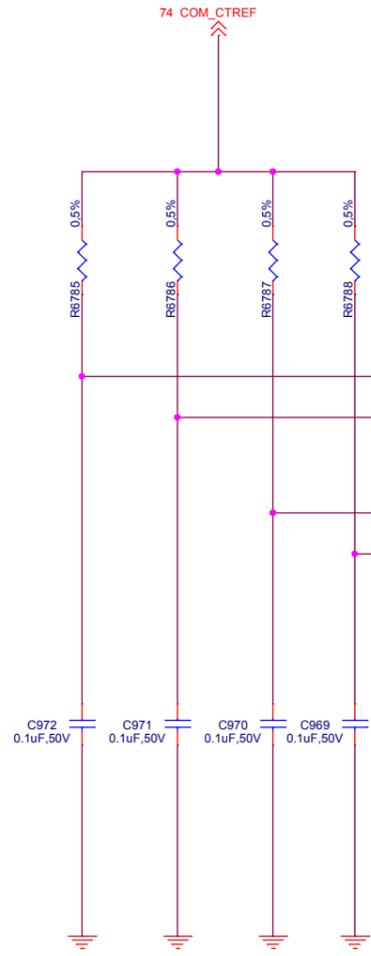
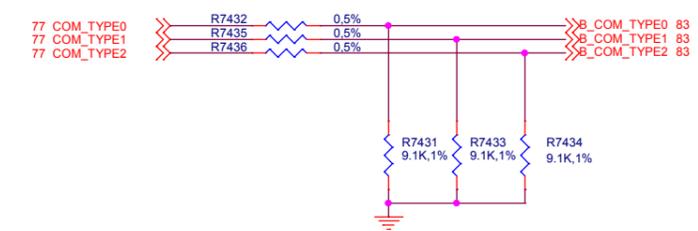


**COM6 CONNECTOR PAGE 3**

CAVIUM		
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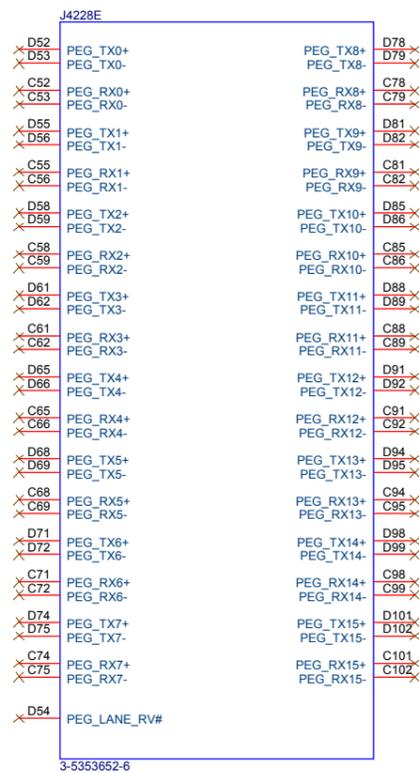


Pull up to 5V Standby and to CPLD with 5V protection. Decode TYPE0#, TYPE1#, and TYPE2# in CPLD and only power up the module 12V if it is Type 6 or Type 10



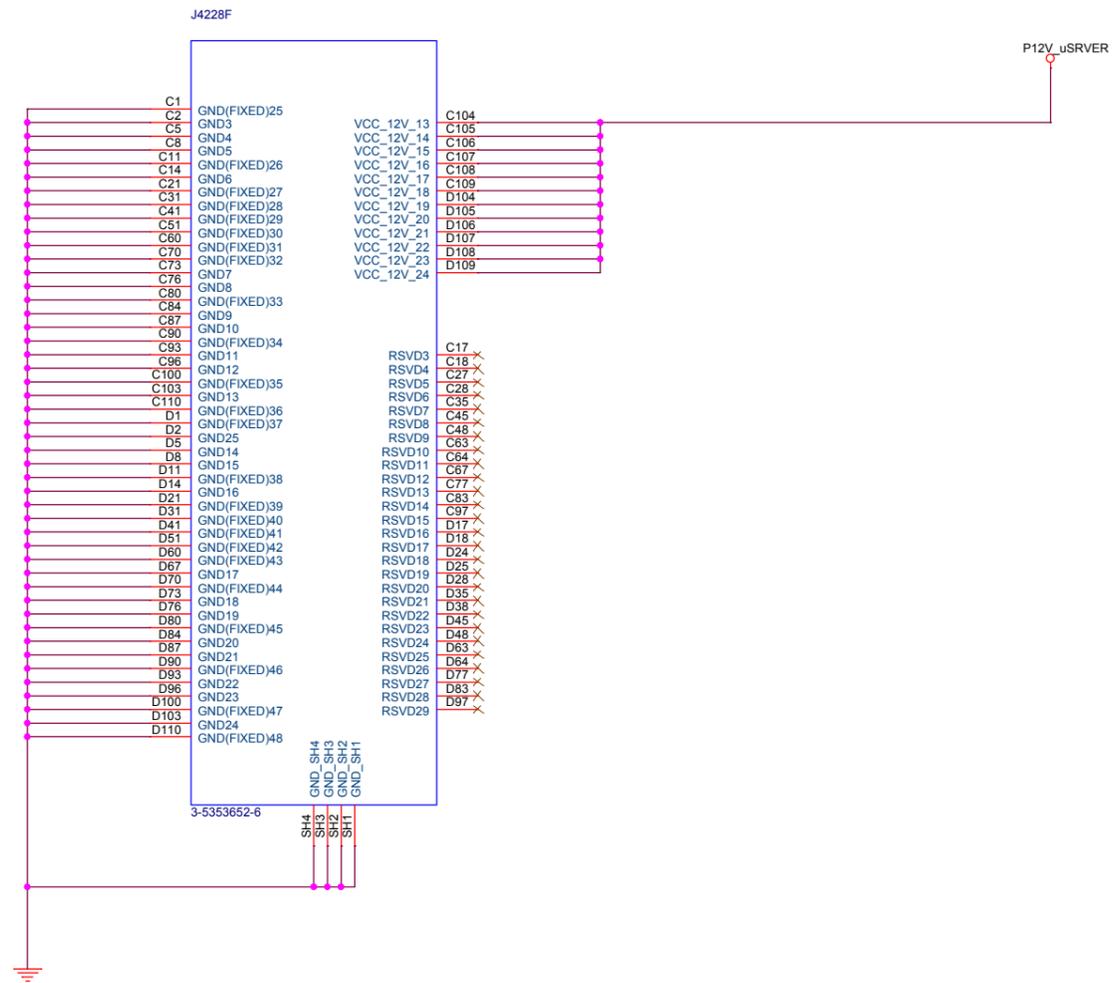
# COM6 CONNECTOR PAGE 4

CAVIUM		
Title	WEDGE100C	
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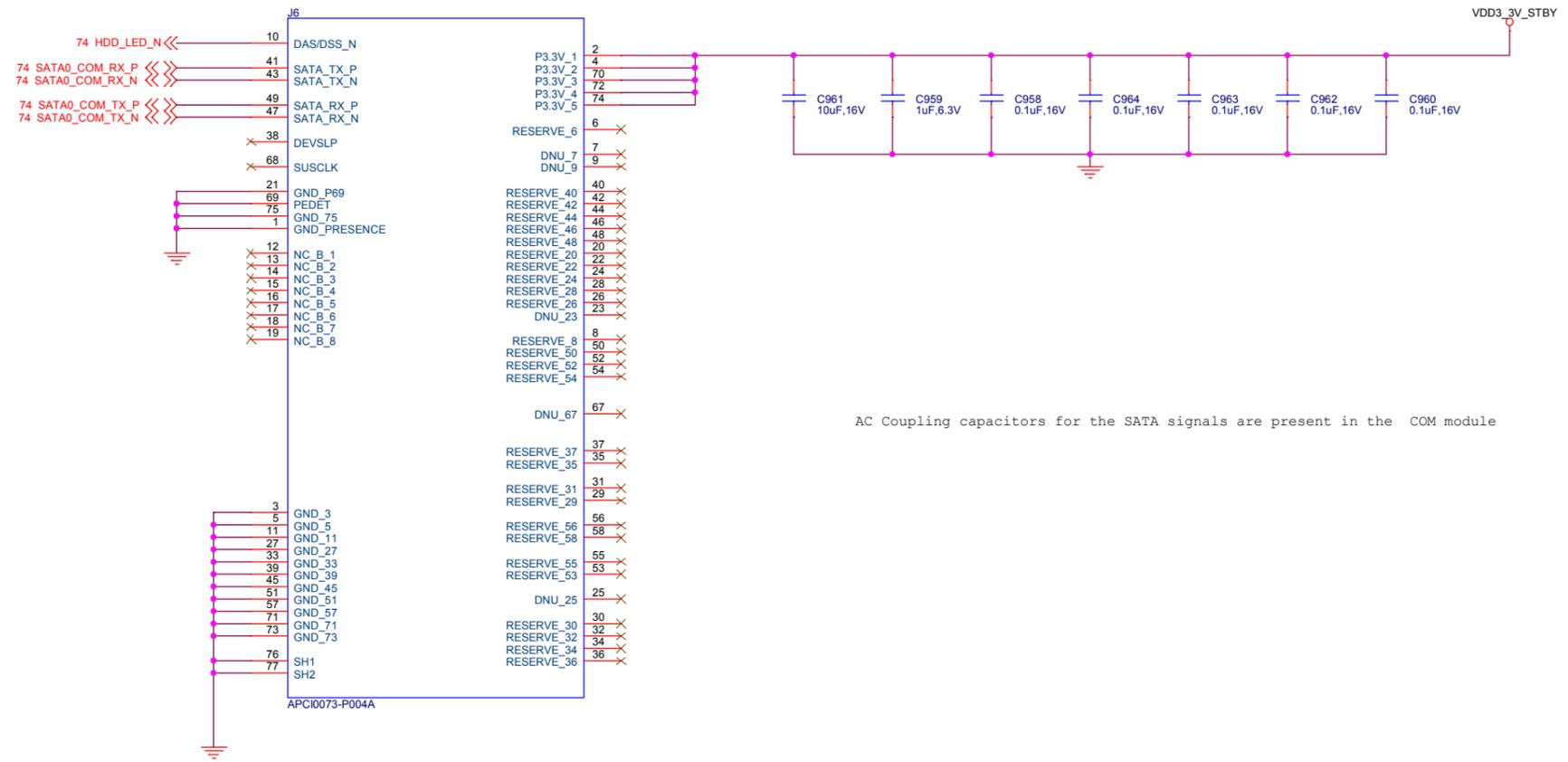
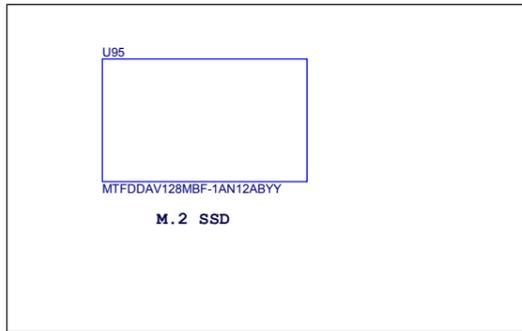
# COM6 CONNECTOR PAGE 5

Title			
CAVIUM			
WEDGE100C			
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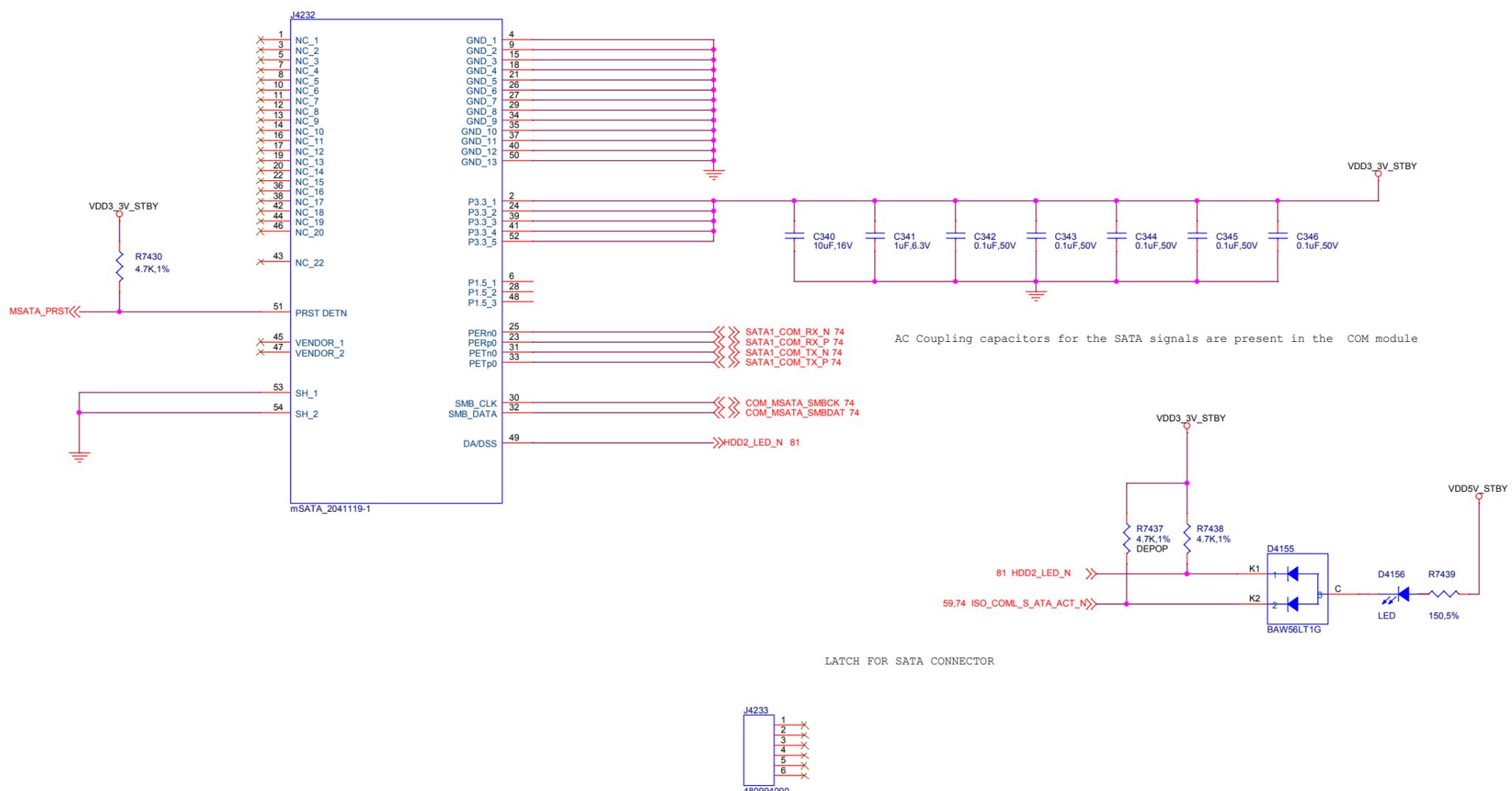
# COM6 CONNECTOR PAGE 6

CAVIUM			
Title: WEDGE100C			
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# M.2SSD CONNECTOR

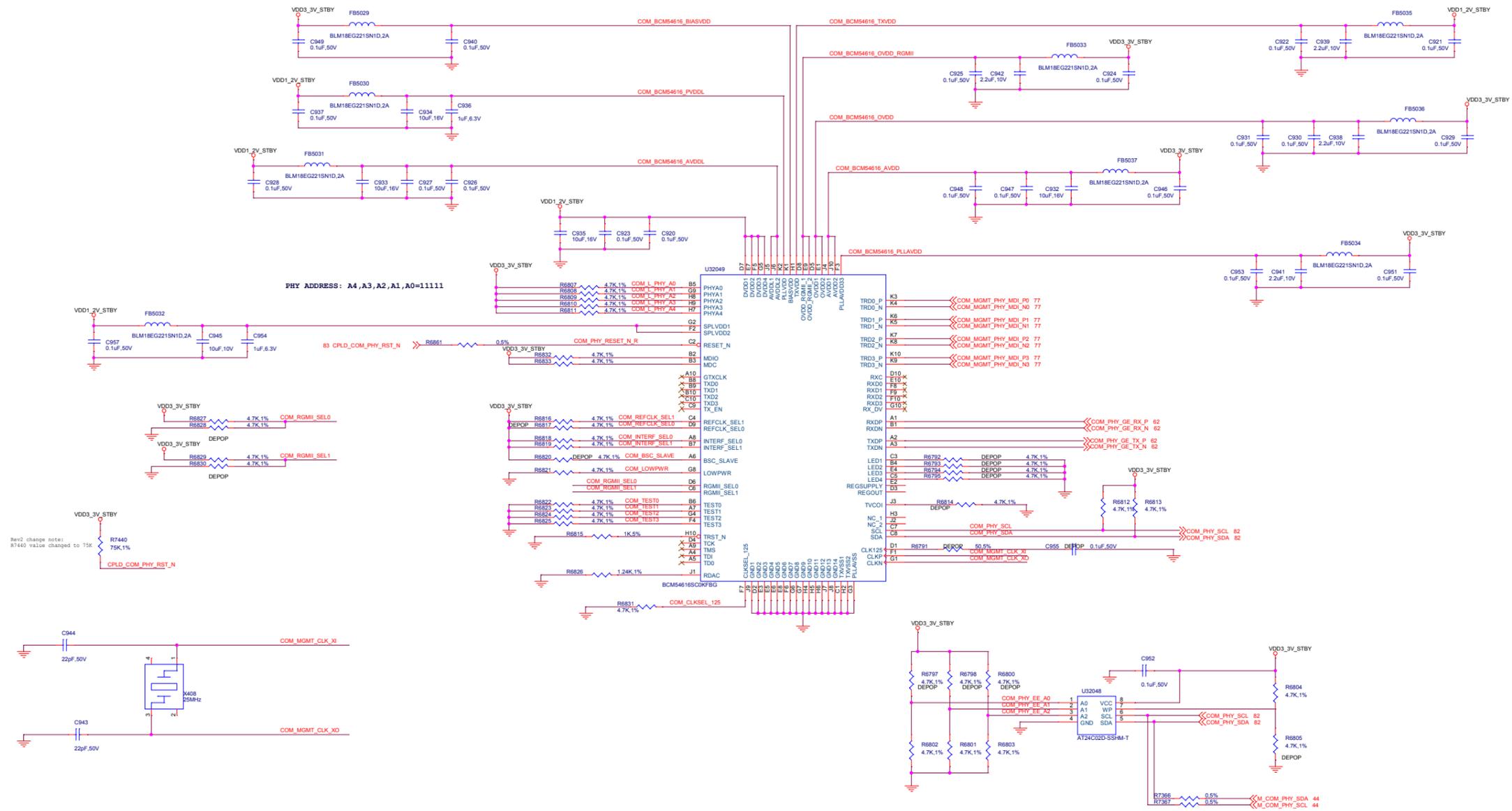
Title		
CAVIUM		
WEDGE100C		
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AC Coupling capacitors for the SATA signals are present in the COM module

# MSATA CONNECTOR

Title		
CAVIUM		
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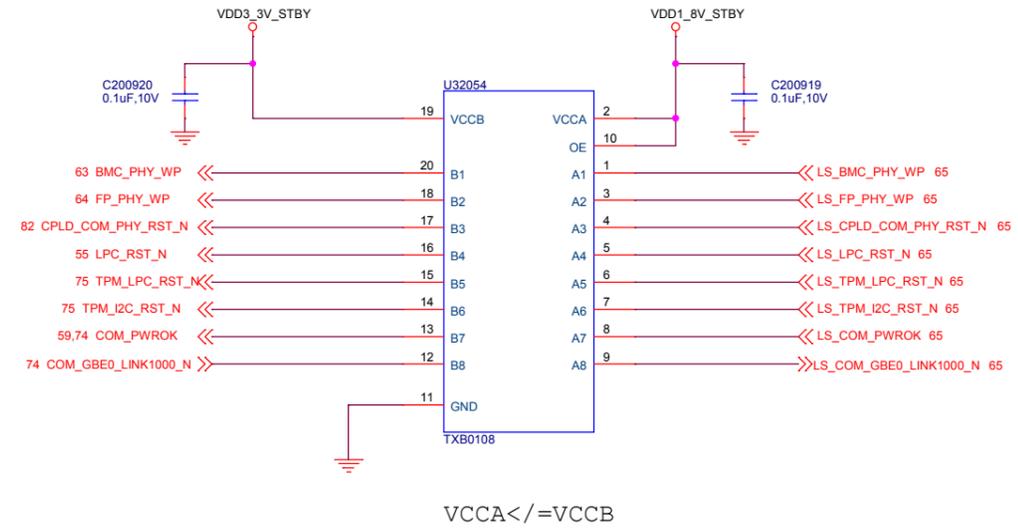
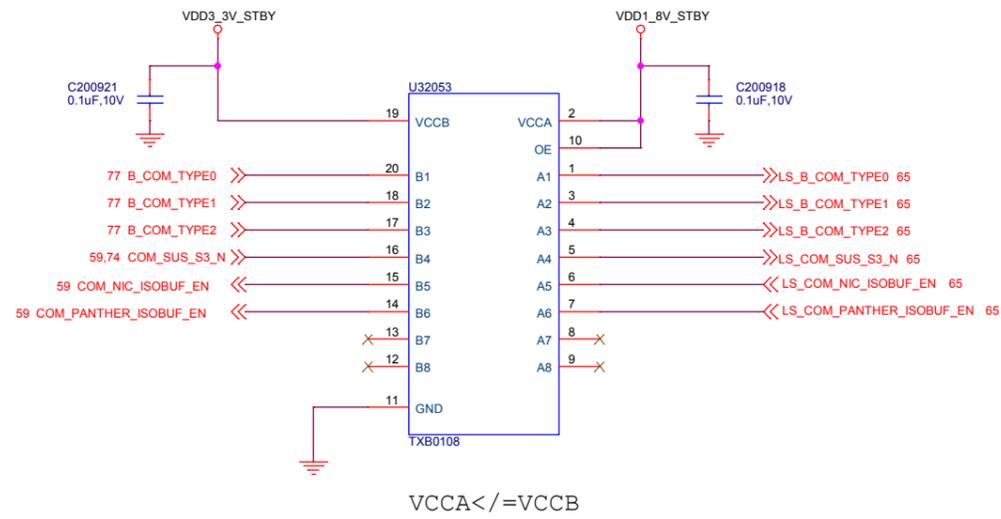
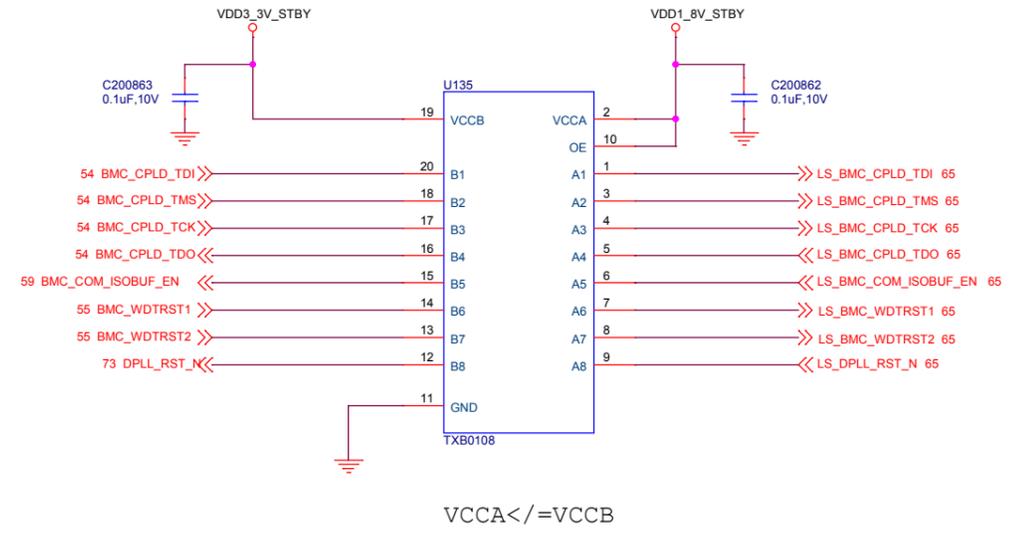
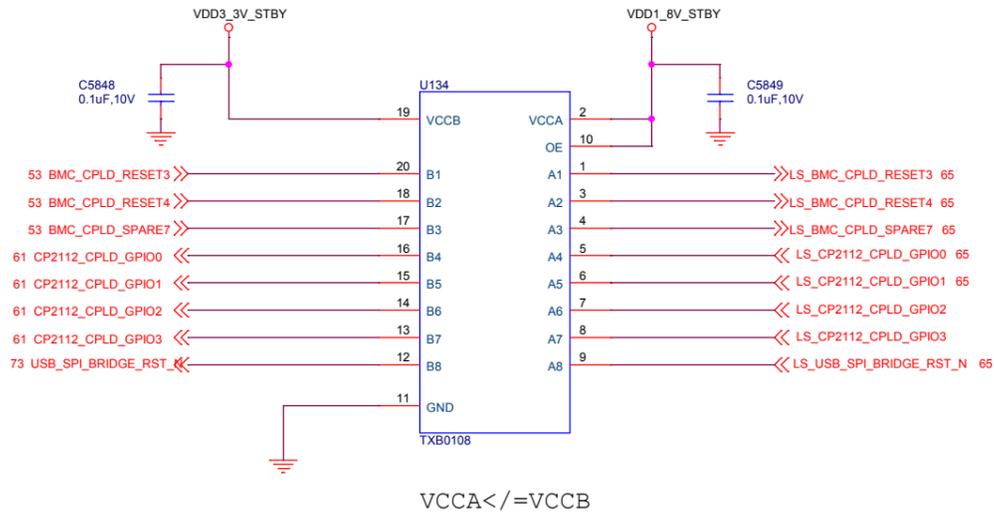
RGMII\_SEL[1:0]  
 00 = Reserved  
 01 = RGMII (2.5V)  
 10 = RGMII (1.8V)  
 \*11 = RGMII (3.3V)

REFCLK\_SEL [1:0]  
 00 = Select differential clock input  
 01 = Select single-ended CMOS  
 \*10 = Select XTAL input  
 11 = Not allowed

INTERF\_SEL [1:0]  
 00 = RGMII-Copper (Copper mode)  
 01 = RGMII-Fiber (Fiber mode)  
 10 = SGMII-Copper (SGMII mode)  
 \*11 = Serdes-Copper (Media Converter mode)

Rev2 change note:  
 R7440 value changed to 75K

### 3.3V to 1.8V Level Shifters



SI no	Changes	Page No.	REV
1	Deleted SMAs J4217,J4218,J4219,J4220,J4221,J4222,J8005,J8006	15,35	Rev1
2	SW1 part number changed to DNHF-04F-T-V from Dawning	17	Rev1
3	Changed C4015,C4016,C4017,C4018,C4019,C8355,C8356,C8357,C8358,C8359,C8360 C8361,C8362,C8363,C8364 with EEF-HX0E331R4 part from Panasonic	19	Rev1
4	Level Translator VCCA should be less than or equal to VCCB, to achieve this U180,U134,U135,U32053,U32054 schematics updated	65,83	Rev2
5	Resistor R1244 value changed to 1K	17	Rev2
6	Resistor R8197,1K newly added	14	Rev2
7	Resistors R4331,R5681,R6666,R6855,R7318,R7322,R7413,R7440,R7447 value changed to 75K	55,59,63,64,74,75,82	Rev2

## CHANGE TRACKER

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