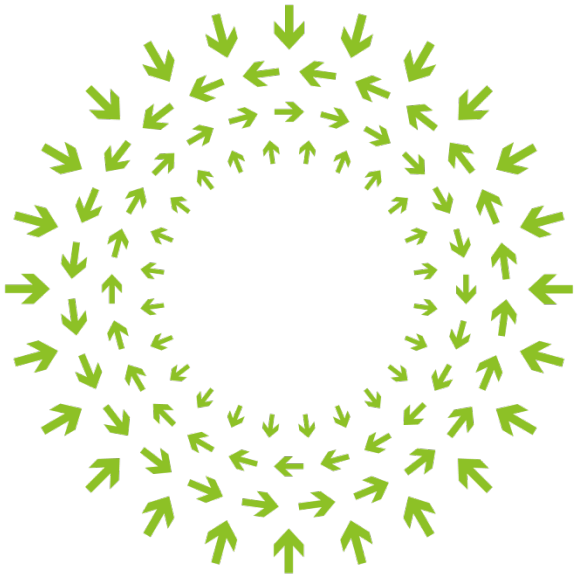

OPEN

Compute Project

Facebook, Inc.

MiniLake COM-Express Mezzanine Card Hardware Specification

Rev 1.6

1. Contents

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3. Introduction

3.1 COM-Express Mezzanine Card Overview

This document describes Minilake, a COM-Express mezzanine card (module) that is used inside Facebook's data center equipment. In this document:

Module: refers to Minilake

Carrier Board or System: refers to the system board that Minilake is installed.

Minilake conforms to PICMG COM Express Module Base Specification Revision 3.0 March 31, 2017.

Figure 3-1 shows the functional block diagram of an example COM-Express module.

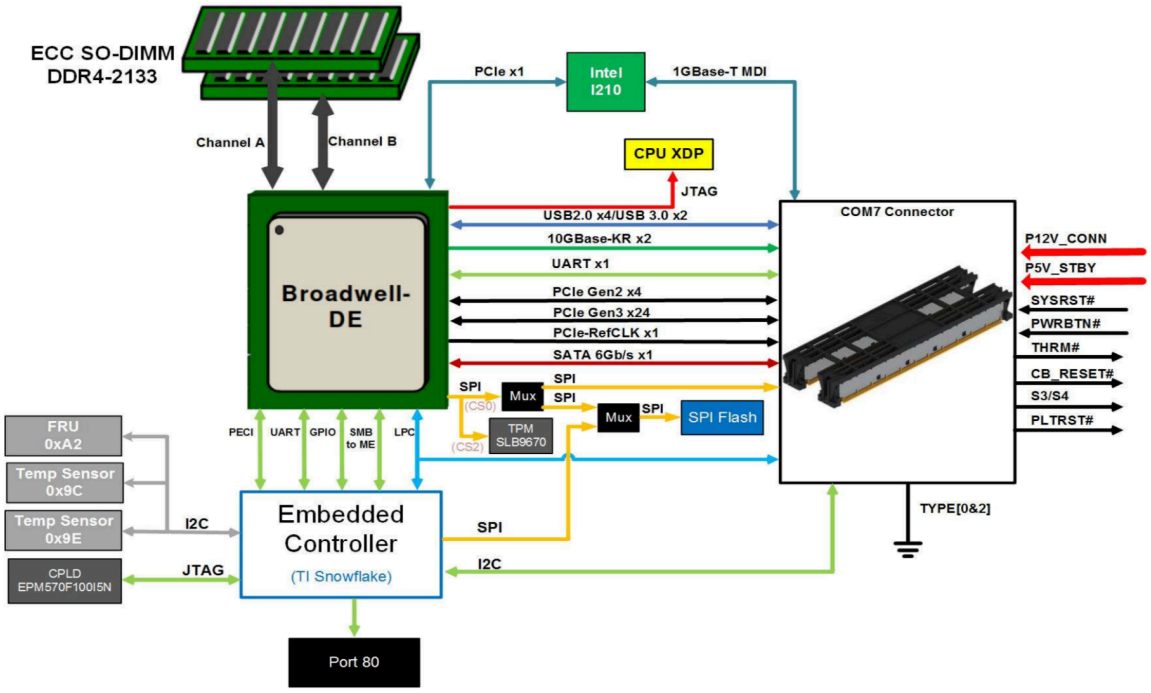

Figure 3-1 Example Block Diagram of COM-Express Module

4. Mechanical Design

4.1 Module Mechanical Outline

Minilake is with ***Basic*** (95x125mm) form factor. The components on the module including the CPU heatsink or heat spreader shall not protrude the profile shown below. Please note the profile is not exactly the same as what is specified by PICMG COM-Express

specification. Current mounting hole size is 2.5mm. prefer to use 3mm hole size for more standard size hardware.

Component and traces clearance also have been considered around the mounting hole area to allow M3 size standoff be used without creating a short to the PCBA.

Heatsink mounting force ensures it will not deform the PCB and create any damage on the PCBA.

No stress should apply to the PCB during DIMM insertion to the connector.

DIMM connector has positive latching to ensure DIMM will not walk out from the DIMM connector during operation/vibration.

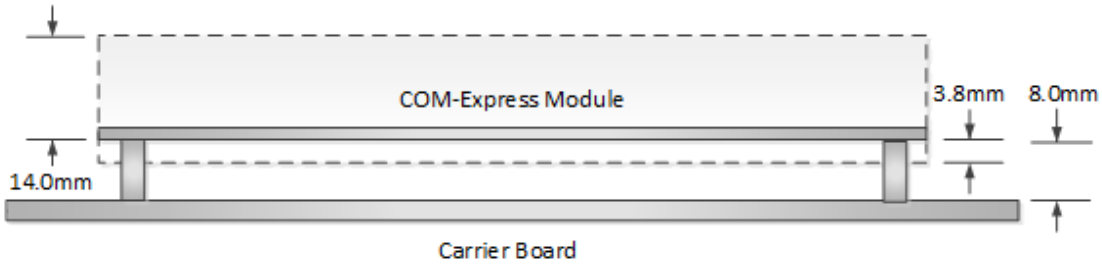

Figure 4-1 COM-Express Module Profile

5. Minilake Thermal Design

5.1 CPU Heatsink

Minilake vendor can design the heatsink for the CPU based on the system requirement. Heatsink design is following the concepts below:

- Heatsink design is optimized to minimize airflow requirement as well as adhere to system-level airflow restrictions (see paragraph below).
- Heatsink should not adversely impact cooling of DIMMs and other temperature-sensitive components on Minilake.
- Allowed pressure drop is about 30Pa.

The airflow direction when the module is mounted on the carrier board could be system specific, which implies that different heatsink designs may be needed for the same COM-Express module in different systems.

The CPU heatsink shall not protrude beyond the card mechanical outline specified in Section 4.1. It shall be designed in such a way that the SODIMM on the top side of the module can be replaced without removing the CPU heatsink.

5.2 Thermal Margin

Thermal margin is defined as the difference between the maximum theoretical safe temperature and actual operating temperature. A minimum of 10°C margin in junction or case temperatures is allowed for every component on Minilake.

5.3 Thermal Modeling

Minilake vendor is expected to provide a thermal model to assist system-level thermal design. The following information of key components should be provided for the purpose of heatsink selection and/or design.

- Detailed modeling of CPU, DIMMs, connectors and power delivery components
- Power consumption (TDP – Thermal Design Power)
- Thermal resistance (including that of thermal interface material)
- Junction or case temperature limit

5.4 Temperature and Power Sensors

Minilake have temperature sensors at key locations, and it have voltage sensors on major power rails. The module can sense the power consumption of key components as well.

Here is the list of sensors to be provided. Detailed table is listed in section 7.

- SoC junction temperature
- SoC core voltage
- DIMM temperature
- DRAM voltage

All sensor values must be readable by the BMC via the management sideband interface.

6. Electrical Interface

6.1 COM-Express Connector Pinout

Minilake follows ComE standard pinout Type 7, because it supports the built-in 10GbE NICs of Broadwell-DE SoC. In Facebook application not all the pins defined by PICMG COM.0 is used. The signals that are required in Facebook's application are listed in Table 6-1 and Table 5-2.

Table 6-1 COM Express Connector Pin Assignment

Row A			Row B		
Pin No.	**Pin name**	**Required?**	**Pin No.**	**Pin name**	**Required?**
A1	GND	Required	**B1**	GND	Required
A2	GBE0_MDI3-	Required	**B2**	GBE0_ACT#	Required
A3	GBE0_MDI3+	Required	**B3**	LPC_FRAME#	Required
A4	GBE0_LINK100#	Required	**B4**	LPC_AD0	Required
A5	GBE0_LINK1000#	Required	**B5**	LPC_AD1	Required
A6	GBE0_MDI2-	Required	**B6**	LPC_AD2	Required
A7	GBE0_MDI2+	Required	**B7**	LPC_AD3	Required

A8	GBE0_LINK#	Not Connected	**B8**	LPC_DRQ0#	Not Connected
A9	GBE0_MDI1-	Required	**B9**	LPC_DRQ1#	Not Connected
A10	GBE0_MDI1+	Required	**B10**	LPC_PCLK	Required
A11	GND	Required	**B11**	GND	Required
A12	GBE0_MDI0-	Required	**B12**	PWRBTN#	Required
A13	GBE0_MDI0+	Required	**B13**	SMB_CK	Not Connected
A14	GBE0_CTREF	Not Connected	**B14**	SMB_DAT	Not Connected
A15	SUS_S3#	Required if the module supports S3	**B15**	SMB_ALERT#	Not Connected
A16	SATA0_TX+	Required	**B16**	SATA1_TX+	Not Connected
A17	SATA0_TX-	Required	**B17**	SATA1_TX-	Not Connected
A18	SUS_S4#	Required if the module supports S4	**B18**	SUS_STAT#	Required
A19	SATA0_RX+	Required	**B19**	SATA1_RX+	Not Connected
A20	SATA0_RX-	Required	**B20**	SATA1_RX-	Not Connected
A21	GND	Required	**B21**	GND	Required
A22	PCIE_TX15+	Not Connected	**B22**	PCIE_RX15+	Not Connected
A23	PCIE_TX15-	Not Connected	**B23**	PCIE_RX15-	Not Connected
A24	SUS_S5#	Not Connected	**B24**	PWROK	Required
A25	PCIE_TX14+	Not Connected	**B25**	PCIE_RX14+	Not Connected
A26	PCIE_TX14-	Not Connected	**B26**	PCIE_RX14-	Not Connected
A27	BATLOW#	Required	**B27**	WDT	Required
A28	(S)ATA_ACT#	Not Connected	**B28**	RSVD	Not Connected
A29	RSVD	Not Connected	**B29**	RSVD	Not Connected
A30	RSVD	Not Connected	**B30**	RSVD	Not Connected
A31	GND	Required	**B31**	GND	Required
A32	RSVD	Not Connected	**B32**	RSVD	Not Connected
A33	RSVD	Not Connected	**B33**	I2C_CLK	Required
A34	BIOS_DIS0#	Required	**B34**	I2C_DAT	Required
A35	THRMTRIP#	Required	**B35**	THRM#	Required
A36	PCIE_TX13+	Not Connected	**B36**	PCIE_RX13+	Not Connected
A37	PCIE_TX13-	Not Connected	**B37**	PCIE_RX13-	Not Connected
A38	GND	Required	**B38**	GND	Required
A39	PCIE_TX12+	Not Connected	**B39**	PCIE_RX12+	Not Connected
A40	PCIE_TX12-	Not Connected	**B40**	PCIE_RX12-	Not Connected
A41	GND	Required	**B41**	GND	Required
A42	USB2-	Required	**B42**	USB3-	Required
A43	USB2+	Required	**B43**	USB3+	Required
A44	USB_2_3_OC#	Required	**B44**	USB_0_1_OC#	Required
A45	USB0-	Required	**B45**	USB1-	Required

A46	USB0+	Required	**B46**	USB1+	Required
A47	VCC_RTC	Required	**B47**	ESPI_EN#	Not Connected
A48	RSVD	Not Connected	**B48**	USB0_HOST_PRSNT#	Not Connected
A49	GBE0_SDP	Not Connected	**B49**	SYS_RESET#	Required
A50	LPC_SERIRQ	Required	**B50**	CB_RESET#	Required
A51	GND	Required	**B51**	GND	Required
A52	PCIE_TX5+	Optional	**B52**	PCIE_RX5+	Optional
A53	PCIE_TX5-	Optional	**B53**	PCIE_RX5-	Optional
A54	GPI0	Required	**B54**	PWRGD_PCH_PWROK	Powergood pin from SoC / PCH on ComE. 3.3V active high signal. The carrier board enables the isolation buffers when PWRGD_PCH_PWROK transitions to High.
A55	PCIE_TX4+	Optional	**B55**	PCIE_RX4+	Optional
A56	PCIE_TX4-	Optional	**B56**	PCIE_RX4-	Optional
A57	GND	Required	**B57**	GPO2	Ground
A58	PCIE_TX3+	Optional	**B58**	PCIE_RX3+	Optional
A59	PCIE_TX3-	Optional	**B59**	PCIE_RX3-	Optional
A60	GND	Required	**B60**	GND	Required
A61	PCIE_TX2+	Optional	**B61**	PCIE_RX2+	Optional
A62	PCIE_TX2-	Optional	**B62**	PCIE_RX2-	Optional
A63	RST_RTCRST_N_R	CMOS reset pin. Open drain input to the COMe. pull up resistor sitting on the ComE card. It clears the CMOS when pulled low.	**B63**	GPO3	Ground
A64	PCIE_TX1+	Optional	**B64**	PCIE_RX1+	Optional
A65	PCIE_TX1-	Optional	**B65**	PCIE_RX1-	Optional
A66	GND	Required	**B66**	WAKE0#	Not Connected
A67	GND	Required	**B67**	WAKE1#	Not Connected
A68	PCIE_TX0+	Optional	**B68**	PCIE_RX0+	Optional
A69	PCIE_TX0-	Optional	**B69**	PCIE_RX0-	Optional
A70	GND	Required	**B70**	GND	Required
A71	PCIE_TX8+	Required	**B71**	PCIE_RX8+	Required
A72	PCIE_TX8-	Required	**B72**	PCIE_RX8-	Required

A73	GND	Required	**B73**	GND	Required
A74	PCIE_TX9+	Required	**B74**	PCIE_RX9+	Required
A75	PCIE_TX9-	Required	**B75**	PCIE_RX9-	Required
A76	GND	Required	**B76**	GND	Required
A77	PCIE_TX10+	Required	**B77**	PCIE_RX10+	Required
A78	PCIE_TX10-	Required	**B78**	PCIE_RX10-	Required
A79	GND	Required	**B79**	GND	Required
A80	GND	Required	**B80**	GND	Required
A81	PCIE_TX11+	Required	**B81**	PCIE_RX11+	Required
A82	PCIE_TX11-	Required	**B82**	PCIE_RX11-	Required
A83	GND	Required	**B83**	GND	Required
A84	NCSI_TX_EN	Not Connected	**B84**	VCC_5V_SBY	Required
A85	GPI3	Not Connected	**B85**	VCC_5V_SBY	Required
A86	RSVD	Not Connected	**B86**	VCC_5V_SBY	Required
A87	GND	Ground	**B87**	VCC_5V_SBY	Required
A88	PCIE_CK_REF+	Required	**B88**	BIOS_DIS1#	Required / No Connected in Minilake
A89	PCIE_CK_REF-	Required	**B89**	NCSI_RX_ER	Not Connected
A90	GND	Required	**B90**	GND	Required
A91	SPI_POWER	Required	**B91**	NCSI_CLK_IN	Not Connected
A92	SPI_MISO	Required	**B92**	NCSI_RXD1	Not Connected
A93	GPO0	Required	**B93**	NCSI_RXD0	Not Connected
A94	SPI_CLK	Required	**B94**	NCSI_CRS_DV	Not Connected
A95	SPI_MOSI	Required	**B95**	NCSI_TXD1	Not Connected
A96	TPM_PP	Not Connected	**B96**	NCSI_TXD0	Not Connected
A97	TYPE10#	Required / No Connected in Minilake	**B97**	SPI_CS#	Required
A98	SER0_TX	Required	**B98**	NCSI_ARB_IN	Not Connected
A99	SER0_RX	Required	**B99**	NCSI_ARB_OUT	Not Connected
A100	GND	Required	**B100**	GND	Required
A101	SER1_TX	Not Connected	**B101**	FAN_PWNOUT	Not Connected
A102	SER1_RX	Not Connected	**B102**	FAN_TACHIN	Not Connected
A103	LID#	Not Connected	**B103**	SLEEP#	Not Connected
A104	VCC_12V	Required	**B104**	VCC_12V	Required
A105	VCC_12V	Required	**B105**	VCC_12V	Required
A106	VCC_12V	Required	**B106**	VCC_12V	Required
A107	VCC_12V	Required	**B107**	VCC_12V	Required
A108	VCC_12V	Required	**B108**	VCC_12V	Required
A109	VCC_12V	Required	**B109**	VCC_12V	Required
A110	GND	Required	**B110**	GND	Required

Table 6-2 COM Express Connector Pin Assignment

Row C			Row D		
Pin No.	**Signal**	**Required?**	**Pin No.**	**Signal**	**Required?**
C1	GND	Required	**D1**	GND	Required
C2	GND	Required	**D2**	GND	Required
C3	USB_SSRX0-	Required	**D3**	USB_SSTX0-	Required
C4	USB_SSRX0+	Required	**D4**	USB_SSTX0+	Required
C5	GND	Required	**D5**	GND	Required
C6	USB_SSRX1-	Required	**D6**	USB_SSTX1-	Required
C7	USB_SSRX1+	Required	**D7**	USB_SSTX1+	Required
C8	GND	Required	**D8**	GND	Required
C9	USB_SSRX2-	Not Connected	**D9**	USB_SSTX2-	Not Connected
C10	USB_SSRX2+	Not Connected	**D10**	USB_SSTX2+	Not Connected
C11	GND	Required	**D11**	GND	Required
C12	USB_SSRX3-	Not Connected	**D12**	USB_SSTX3-	Not Connected
C13	USB_SSRX3+	Not Connected	**D13**	USB_SSTX3+	Not Connected
C14	GND	Required	**D14**	GND	Required
C15	10G_PHY_MDC_SCL3	Not Connected	**D15**	10G_PHY_MDIO_SDA3	Not Connected
C16	10G_PHY_MDC_SCL2	Not Connected	**D16**	10G_PHY_MDIO_SDA2	Not Connected
C17	10G_SDP2	Not Connected	**D17**	10G_SDP3	Not Connected
C18	GND	Required	**D18**	GND	Required
C19	PCIE_RX6+	Optional	**D19**	PCIE_TX6+	Optional
C20	PCIE_RX6-	Optional	**D20**	PCIE_TX6-	Optional
C21	GND	Required	**D21**	GND	Required
C22	PCIE_RX7+	Optional	**D22**	PCIE_TX7+	Optional
C23	PCIE_RX7-	Optional	**D23**	PCIE_TX7-	Optional
C24	10G_INT2	Not Connected	**D24**	10G_INT3	Not Connected
C25	GND	Required	**D25**	GND	Required
C26	10G_KR_RX3+	Not Connected	**D26**	10G_KR_TX3+	Not Connected
C27	10G_KR_RX3-	Not Connected	**D27**	10G_KR_TX3-	Not Connected
C28	GND	Required	**D28**	GND	Required
C29	10G_KR_RX2+	Not Connected	**D29**	10G_KR_TX2+	Not Connected
C30	10G_KR_RX2-	Not Connected	**D30**	10G_KR_TX2-	Not Connected
C31	GND	Required	**D31**	GND	Required
C32	10G_SFP_SDA3	Not Connected	**D32**	10G_SFP_SCL3	Not Connected
C33	10G_SFP_SDA2	Not Connected	**D33**	10G_SFP_SCL2	Not Connected

C34	10G_PHY_RST_23	Not Connected	**D34**	10G_PHY_CAP_23	Not Connected
C35	10G_PHY_RST_01	Not Connected	**D35**	10G_PHY_CAP_01	Not Connected
C36	10G_LED_SDA	Not Connected	**D36**	RSVD	Not Connected
C37	10G_LED_SCL	Not Connected	**D37**	RSVD	Not Connected
C38	10G_SFP_SDA1	Not Connected	**D38**	10G_SFP_SCL1	Not Connected
C39	10G_SFP_SDA0	Not Connected	**D39**	10G_SFP_SCL0	Not Connected
C40	10G_SDP0	Not Connected	**D40**	10G_SDP1	Not Connected
C41	GND	Required	**D41**	GND	Required
C42	10G_KR_RX1+	Required	**D42**	10G_KR_TX1+	Required
C43	10G_KR_RX1-	Required	**D43**	10G_KR_TX1-	Required
C44	GND	Required	**D44**	GND	Required
C45	10G_PHY_MDC_SCL1	Optional	**D45**	10G_PHY_MDIO_SDA1	Optional
C46	10G_PHY_MDC_SCL0	Optional	**D46**	10G_PHY_MDIO_SDA0	Optional
C47	10G_INT0	Not Connected	**D47**	10G_INT1	Not Connected
C48	GND	Required	**D48**	GND	Required
C49	10G_KR_RX0+	Required	**D49**	10G_KR_TX0+	Required
C50	10G_KR_RX0-	Required	**D50**	10G_KR_TX0-	Required
C51	GND	Required	**D51**	GND	Required
C52	PCIE_RX16+	Required	**D52**	PCIE_TX16+	Required
C53	PCIE_RX16-	Required	**D53**	PCIE_TX16-	Required
C54	TYPE0#	Required	**D54**	RSVD	Not Connected
C55	PCIE_RX17+	Required	**D55**	PCIE_TX17+	Required
C56	PCIE_RX17-	Required	**D56**	PCIE_TX17-	Required
C57	TYPE1#	Required	**D57**	TYPE2#	Required
C58	PCIE_RX18+	Required	**D58**	PCIE_TX18+	Required
C59	PCIE_RX18-	Required	**D59**	PCIE_TX18-	Required
C60	GND	Required	**D60**	GND	Required
C61	PCIE_RX19+	Required	**D61**	PCIE_TX19+	Required
C62	PCIE_RX19-	Required	**D62**	PCIE_TX19-	Required
C63	GND	Required	**D63**	GND	Required
C64	GND	Required	**D64**	GND	Required
C65	PCIE_RX20+	Required	**D65**	PCIE_TX20+	Required
C66	PCIE_RX20-	Required	**D66**	PCIE_TX20-	Required
C67	GND	Required	**D67**	GND	Required
C68	PCIE_RX21+	Required	**D68**	PCIE_TX21+	Required
C69	PCIE_RX21-	Required	**D69**	PCIE_TX21-	Required
C70	GND	Required	**D70**	GND	Required
C71	PCIE_RX22+	Required	**D71**	PCIE_TX22+	Required
C72	PCIE_RX22-	Required	**D72**	PCIE_TX22-	Required

C73	GND	Required	**D73**	GND	Required
C74	PCIE_RX23+	Required	**D74**	PCIE_TX23+	Required
C75	PCIE_RX23-	Required	**D75**	PCIE_TX23-	Required
C76	GND	Required	**D76**	GND	Required
C77	GND	Required	**D77**	GND	Required
C78	PCIE_RX24+	Required	**D78**	PCIE_TX24+	Required
C79	PCIE_RX24-	Required	**D79**	PCIE_TX24-	Required
C80	GND	Required	**D80**	GND	Required
C81	PCIE_RX25+	Required	**D81**	PCIE_TX25+	Required
C82	PCIE_RX25-	Required	**D82**	PCIE_TX25-	Required
C83	GND	Required	**D83**	GND	Required
C84	GND	Required	**D84**	GND	Required
C85	PCIE_RX26+	Required	**D85**	PCIE_TX26+	Required
C86	PCIE_RX26-	Required	**D86**	PCIE_TX26-	Required
C87	GND	Required	**D87**	GND	Required
C88	PCIE_RX27+	Required	**D88**	PCIE_TX27+	Required
C89	PCIE_RX27-	Required	**D89**	PCIE_TX27-	Required
C90	GND	Required	**D90**	GND	Required
C91	PCIE_RX28+	Required	**D91**	PCIE_TX28+	Required
C92	PCIE_RX28-	Required	**D92**	PCIE_TX28-	Required
C93	GND	Required	**D93**	GND	Required
C94	PCIE_RX29+	Required	**D94**	PCIE_TX29+	Required
C95	PCIE_RX29-	Required	**D95**	PCIE_TX29-	Required
C96	GND	Required	**D96**	GND	Required
C97	GND	Required	**D97**	GND	Required
C98	PCIE_RX30+	Required	**D98**	PCIE_TX30+	Required
C99	PCIE_RX30-	Required	**D99**	PCIE_TX30-	Required
C100	GND	Required	**D100**	GND	Required
C101	PCIE_RX31+	Required	**D101**	PCIE_TX31+	Required
C102	PCIE_RX31-	Required	**D102**	PCIE_TX31-	Required
C103	GND	Required	**D103**	GND	Required
C104	VCC_12V	Required	**D104**	VCC_12V	Required
C105	VCC_12V	Required	**D105**	VCC_12V	Required
C106	VCC_12V	Required	**D106**	VCC_12V	Required
C107	VCC_12V	Required	**D107**	VCC_12V	Required
C108	VCC_12V	Required	**D108**	VCC_12V	Required
C109	VCC_12V	Required	**D109**	VCC_12V	Required
C110	GND	Required	**D110**	GND	Required

6.2 PCIe

Minilake supports up to Six PCIe x4 links of Gen 3 as table 5-1 and table 5-2. In the pin definition column, “Optional” means Minilake has this pin connected but the default setting does not use those channels. System designer can always reconfigure that.

- PCIE_TX0+/-, PCIE_RX0+/-
- PCIE_TX1+/-, PCIE_RX1+/-
- PCIE_TX2+/-, PCIE_RX2+/-
- PCIE_TX3+/-, PCIE_RX3+/-

- PCIE_TX4+/-, PCIE_RX4+/-
- PCIE_TX5+/-, PCIE_RX5+/-
- PCIE_TX6+/-, PCIE_RX6+/-
- PCIE_TX7+/-, PCIE_RX7+/-

- PCIE_TX16+/-, PCIE_RX16+/-
- PCIE_TX17+/-, PCIE_RX17+/-
- PCIE_TX18+/-, PCIE_RX18+/-
- PCIE_TX19+/-, PCIE_RX19+/-

- PCIE_TX20+/-, PCIE_RX20+/-
- PCIE_TX21+/-, PCIE_RX21+/-
- PCIE_TX22+/-, PCIE_RX22+/-
- PCIE_TX23+/-, PCIE_RX23+/-

- PCIE_TX24+/-, PCIE_RX24+/-
- PCIE_TX25+/-, PCIE_RX25+/-
- PCIE_TX26+/-, PCIE_RX26+/-
- PCIE_TX27+/-, PCIE_RX27+/-

- PCIE_TX28+/-, PCIE_RX28+/-
- PCIE_TX29+/-, PCIE_RX29+/-
- PCIE_TX30+/-, PCIE_RX30+/-
- PCIE_TX31+/-, PCIE_RX31+/-

- PCIE_CLK_REF+/-

Minilake also supports one PCIe x4 link of Gen 2 or above. It is on the following connector signals

- PCIE_TX8+/-, PCIE_RX8+/-
- PCIE_TX9+/-, PCIE_RX9+/-
- PCIE_TX10+/-, PCIE_RX10+/-
- PCIE_TX11+/-, PCIE_RX11+/-

6.3 SATA

Minilake supports one SATA interface at 6Gb/s.

- SATA0_TX+/-, SATA0_RX+/-

6.4 Ethernet

Minilake supports one 1000BASE-T interface as specified by PICMG COM.0. The 10GBASE-KR signals are on the following connector signals:

- 10G_KR_TX0+/-, 10G_KR_RX0+/-
- 10G_KR_TX1+/-, 10G_KR_RX1+/-

6.5 USB

Minilake supports four USB 2.0 and two USB 3.0 interfaces

USB 2.0 interface

- USB0+/-
- USB1+/-
- USB_0_1_OC#
- USB2+/-
- USB3+/-
- USB_2_3_OC#

USB 3.0 interface

- USBSSTX0+/-
- USBSSRX0+/-
- USBSSTX1+/-
- USBSSRX1+/-

6.6 Console

Minilake supports one UART port. Console re-direction shall be supported on at least one UART port, which shall be on:

- SER0_TX, SER0_RX

6.7 I2C and SMBus

The I2C interface of Minilake (I2C_CK, I2C_DAT) is connected to an embedded controller as the management entity on the module.

SMBUS pins directly go to the CPU is not connected to the ComE connector in Minilake.

There is a SMBUS between embedded controller and CPU.

6.8 LPC

Minilake has one LPC bus interface. System designer can specify the LPC devices on system side.

6.9 SPI

Minilake supports an off-module BIOS Flash through the SPI interface. The selection of the off-module BIOS Flash is controlled by BIOS_DIS0/1#.

6.10 Leakage Current Prevention

Leakage current scheme is defined by the carrier board. In Minilake, we propose system board to use pin B54 PWRGD_PCH_PWROK pin. The recommended behavior is to enable the isolation buffer to all possible pins that could cause leakage once this pin is high.

6.11 Intel ITP Support

Minilake has an XDP connector with keep out zones so we can connect Intel ITP debugger.

7. Power

Minilake can specify the power consumptions of the module on VCC_12V, VCC_5V_SBY, and VCC_RTC rails.

Minilake powers up the CPU when the power up sequence complies to PICMG COM.0 Rev3.0 Spec. Figure 6-1 and Table 6-1 is the copy of the figure in PICMG COM.0 spec. After the power is shut down according to the sequence mentioned above, the CPU is able to power up again when the power up sequence is re-applied to the module.

The module won't wait for the PWRBTN# signal from the carrier board to power up the CPU when the power is applied to the module. However, after the CPU is powered up, a long press on PWRBTN# (PWRBTN# being logic low for at least 4 seconds) will shut down the CPU. If PWRBTN# is toggled again, the CPU shall be powered up again. If PWRBTN# is not toggled, instead the module is powered down first then powered up again, the CPU shall be powered up again.

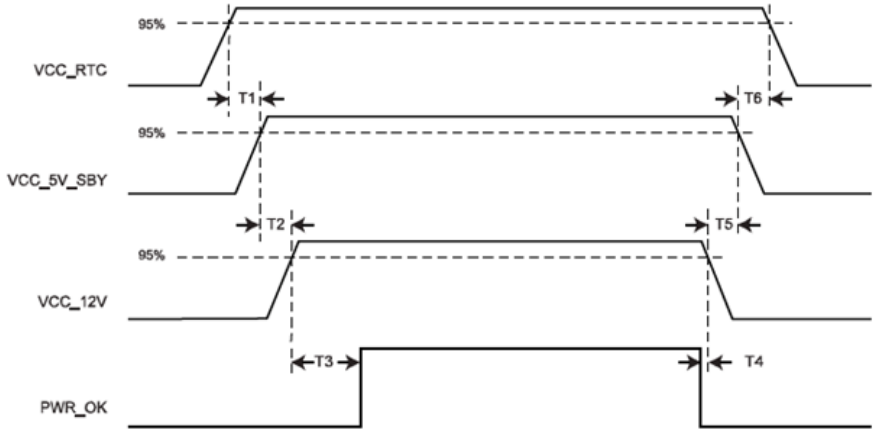

Figure 6-1 Power sequence requirement

Table 6-1 Power sequence timing requirement

T1	VCC_RTC rise to VCC_5V_SBY rise	≥ 0 ms
T2	VCC_5V_SBY rise to VCC_12V rise	≥ 0 ms
T3	VCC_12V rise to PWROK rise	≥ 0 ms
T4	PWR_OK fall to VCC_12V fall	≥ 0 ms
T5	VCC_12V fall to VCC_5V_SBY fall	≥ 0 ms
T6	VCC_5V_SBY fall to VCC_RTC fall	≥ 0 ms

8. Functional Requirements

8.1 Backward Compatibility

Minilake is based on Type-7 pinout with minor modifications, it shall be able to work in Facebook Wedge 100 switch, where the COM-Express socket is of modified Type-6 pinout. No 10GBASE-KR port is required in Wedge 100.

8.2 SOC

The CPU SoC is the key component on Minilake, and here are the requirements.

- The CPU on Minilake shall be in the Intel Broadwell-DE family with a TDP up to 45W.
- The CPU must support Intel TXT (Trusted Execution Technology).

8.3 Memory

Minilake supports at least two DDR4 SODIMM sockets with ECC. Each socket is connected to a different memory controller of the SoC. The DIMM capacity shall be 8GB (using 4Gb or 8Gb DRAM chip) or 16GB (using 8Gb DRAM chip), and the DIMM shall support the highest DDR4 interface speed supported by the SoC. These two sockets shall be placed on the top side of Minilake.

Additional DDR4 SODIMM sockets are preferred, and they can be located on the bottom side of the module. The additional sockets can share the memory controllers with the two sockets mentioned above.

8.4 NIC

For the 1000BASE-T MDI port, Minilake vendor shall specify the NIC vendor and model. The NIC shall be able to support IPv4 / Ipv6 UEFI PXE boot.

8.5 Storage

Minilake does not have any storage device on module.

8.6 TPM

Minilake has a TPM 2.0 module on SoC's LPC bus or the SPI bus, and it is soldered on the module PCB. Optionally, System designer can request it be de-populated when there is a LPC-based TPM module on the carrier board.

8.7 BIOS

The below features are supported in Minilake BIOS:

- Intel TXT support, and supporting Intel Dynamic Boot (DRTM – Dynamic Root of Trust for Measurements)
- UEFI compatible
- Configuration and features
  - Disable unused devices including video interfaces and GPU if supported by hardware
  - BIOS setup menu
  - SoC settings to allow tuning to achieve the optimal combination of performance and power consumption
- Default boot device priority
  - Network / PXE -> 1st off-module SATA -> Other removable devices
- PXE boot
  - Supports Ipv4 and Ipv6 UEFI PXE boot and provide the ability to modify the boot sequence. When PXE booting, the card first attempts to boot from the first Ethernet device (etho).
  - DHCP Discover will be retried four times. The four timeouts are 4, 8, 16, and 32 seconds respectively.
  - Supports UEFI mode
  - Supports both PXE boot over Ipv4 and Ipv6, and be able to boot from a PXE server on a different Ipv4 or Ipv6 subnet
- Other boot options
  - Also supports booting from SATA and USB interfaces
  - Provides the capability to select boot options
- UEFI-based BIOS settings tool
- UEFI-based BIOS update tool
- Linux-based BIOS settings tool
- Linux-based BIOS update tool
- Remote BIOS update
  - Scenario 1: Sample / audit BIOS settings
  - Scenario 2: Update BIOS with pre-configured set of BIOS settings
  - Scenario 3: BIOS / firmware update with a new revision
  - Update from CentOS over an ssh console
  - Can complete BIOS update or setup change with a single reboot (no PXE boot, no multiple reboots)
  - No user interaction (e.g., prompts)
  - BIOS updates and option changes do not take longer than five minutes to complete.
  - Can be scripted and propagated to multiple machines
- Event log
  - Implement SMBIOS Type 15 System Event Log per SMBIOS specification Rev 2.6
  - Hold more than 500 event records (assuming the maximum event record length is 24 bytes, then the size will be larger than 12KB)
  - Each event record includes enhanced information identifying the error source device's vendor ID, card slot ID, and device ID.
  - A system access interface and application software to retrieve and clear the event log from the BIOS

- Logged errors
  - Single-bit ECC error
  - Multi-bit ECC error
  - PCIe error
  - SATA error
  - POST error
- Error thresholds
  - Settings must be enabled for correctable errors.
  - Threshold for Memory Correctable ECC is 1000.
  - PCIe error threshold is 10.
- Console redirection to the serial ports
  - Console redirection shall be enabled whenever the CPU starts booting and kept enabled after the OS starts running.
- POST codes
  - To be provided on the serial console
  - To be provided on the LPC bus
- DMI
  - Model
  - Serial Number
  - Additional information if requested by Facebook
- ATA Security State 2
  - The BIOS shall not send out ATA "frozen" command to the SSDs attached to the SATA ports.
- Support AMI RuntimeMemoryHole eModule, so that we can avoid using the kernel module of SCELNX and AFULNX.
- Off-module BIOS Flash on the SPI interface of the COM-Express connector
  - The SoC will use the off-module BIOS when BIOS_DIS0# = 0
  - The SoC will use the on-module BIOS when BIOS_DIS0# = 0

8.8 System Management

The primary system management functions are provided by a BMC on the carrier board. The BMC on system board communicate with Minilake through the I2C interface. This section identifies the required information that must be accessible from the BMC.

1.1.1 Power Control

The BMC controls power on, off, and reset directly via the signals defined by PICMG COM.0 (PWRBTN#, SYS_RESET#). If VCC_12V to the card is lost and returns ("AC Lost"), the BIOS must be configurable to enable immediate or delayed power-on, or the last power state prior to the event.

1.1.2 Thermal Alerts and Throttle

Minilake provides a mechanism to provide thermal alerts and should accept thermal trip or throttle request from the BMC through THRMTRIP# and THRM# signal defined in COMe Spec Rev3.0. In some cases, an over-temp condition could also be triggered by CPU on minilake. In this case, minilake will shut down and the carrier board's BMC will be noticed through THRM#.

1.1.3 BMC Message Interface

Minilake supports a message interface between the SoC and the BMC on carrier board, so information like SDR (Sensor Data Record) and SEL (System Event Log) can be communicated. Minilake vendor shall specify what the stock BIOS supports, and the scope of work if BIOS customization is required to support such a message interface. The message interface can be the System Interfaces defined by IPMI 2.0 and Keyboard Controller Style (KCS) Interface.

1.1.4 Sensors and Embedded Controller Interface

Minilake specifies all the sensors (temperature, voltage, etc.) on the module, and how the BMC on carrier board can access the readings and alarms of those sensors.

The Embedded Controller (EC) provides an I2C slave interface on I2C_CK / I2C_DAT to the BMC on carrier board. One option of the EC interface to BMC is shown below, and the slave address shall be 0x40 (8-bit addressing, without the R/W# bit) in this case.

Table 8-1 Optional EC Interface to BMC

Register Address	Name	Size	Description
0X00	CPU Die Temperature Register	Byte	CPU die temperature, integer in binary
0X02	DIMM Upper Slot Temperature Register	2-byte	0x02 – Temperature MSB 0x03 – Temperature LSB Temperature = ((((MSB << 8) + LSB) >> 4) & 0xFF) * 1 + ((LSB >> 1) & 0x07) * 0.125
0X04	DIMM Lower Slot Temperature Register	2-byte	0x04 – Temperature MSB 0x05 – Temperature LSB Same temperature formula as above
0X10	Reserved	2-byte	Reserved
0X12	CPU Status Register	1-byte	Bit 0: '1' – CPU CatErr# asserted Bit 1: '1'- CPU Proc_Hot# asserted Bit 2 ~ 7: Read only '0'
0X15	HW Monitor Control Register	1-byte	Bit 1: '1' – Enable EC reading of DIMM temperature from SPD
0X1D	EC Version Register	3-byte	The ODM can use 0x1D, 0x1E, and 0x1F for storing EC version label.
0X20	CPU Vcore Register	2-byte	0x20 – Voltage MSB 0x21 – Voltage LSB Voltage =

			((MSB <<8) + LSB) / 341
0x22	3.3V Voltage Register	2-byte	0x22 – Voltage MSB 0x23 – Voltage LSB Same voltage formula as above
0x24	5V Voltage Register	2-byte	0x24 – Voltage MSB 0x25 – Voltage LSB Same voltage formula as above
0x2C	Build Date Register	3-byte	EC image build date: 0x2C – Year in binary (0 ~ 255 for 2000 ~ 2255) 0x2D – Month in binary (1 ~ 12) 0x2E – Day in binary (1 ~ 31)
0x30	12V Voltage Register	2-byte	0x30 – Voltage MSB 0x31 – Voltage LSB Voltage = ((MSB <<8) + LSB) / 341
0x32	DRAM Voltage Register	2-byte	0x32 – Voltage MSB 0x33 – Voltage LSB Same voltage formula as above
0x3C	Production Name Register	4-byte	ODM defined name in ASCII coding
0x4D	Customized Name Register	3-byte	ODM defined name in ASCII coding
0x50	MAC Address Register	6-byte	MAC address of the 1000BASE-T LAN
0x60	Serial Number Register	32-byte	Serial number of the module

9. Environmental Requirements

The full system with Minilake shall meet the following environmental requirements:

- Telcordia GR-63-CORE
- Operating temperature range: 0°C to +45°C
- Operating altitude with no de-rating up to 1000m (3300 feet)
- Relative humidity: 10% to 90% (non-condensing)
- Storage temperature range: -40°C to +70°C (long-term storage)
- Transportation temperature range: -40°C to +85°C (short-term storage)

9.1 Shock and Vibration

The system meets shock and vibration requirements according to Telcordia GR-63-CORE.

Table 9-1 Vibration and Shock Requirements

	Operating	Non-Operating
Vibration	N/A	Packaged equipment, 30 minutes on each of the 3 axes, per Table 5-13 and Figure 5-20 of GR-63-CORE Issue 4
Shock	N/A	Packaged and Un-packaged drop tests per GR-63-CORE

Table 9-2 Transportation Vibration Test Severity

Frequency Range (Hz)	Test Severity PSD Level
5–20	0.01 g^2/Hz (*1.0 m^2/sec^3*)
20–200	-3 dB/octave

10. Reliability and Quality

10.1 MTBF Requirements

Minilake shall have a minimum calculated MTBF of 300K hours at 90% confidence level at 45C ambient temperature. The motherboard shall also demonstrate the MTBF requirement above by running at full load and 50% of time and performing AC cycling test 50% of time at 45C.

Minilake shall have a minimum Service Life of 5 years (24 Hours / day, Full Load, at 45C system ambient temperature).

11. Prescribed Materials

11.1 Disallowed Components

The following components are not to be used in Minilake:

- Components disallowed by European Union's Restriction of Hazardous Substances Directive (RoHS 6)
- Trimmers and/or potentiometers

RoHS 6	
Lead	1000 ppm (or 0.1% by weight)
Mercury	1000 ppm (or 0.1% by weight)
Cadmium	100 ppm (or 0.01% by weight)
Hexavalent Chromium	1000 ppm (or 0.1% by weight)
PBB	1000 ppm (or 0.1% by weight)
PBDE	1000 ppm (or 0.1% by weight)

11.2 Materials of Concern

It is Facebook's goal to restrict the use of following materials of concern, in addition to the RoHS 6 requirement above. The table below also shows the compliance time lines that the vendors shall comply with.

HAZARDOUS SUBSTANCE	CONCENTRATION LIMIT OF INTEREST (FOR ALL HOMOGENOUS MATERIALS)	BEGIN PHASE-OUT (January 1)	COMPLIANCE DEADLINE (December 31)
Halogens (incl. PVC, BFRs/CFRs)	IEC 61249-2-21 definition of "halogen-free": 900 ppm for Br or Cl, or 1500 ppm combined	2016	2019
Phthalates (DEHP, DBP, DiBP, BBP)	1000 ppm (or 0.1% by weight)	2016	2019 (RoHS recast)
Arsenic	1000 ppm (or 0.1% by weight)	2017	2020

The vendors shall report to Facebook what materials of concern are in their products, and what their plan is to achieve compliance.

12. Labels and Markings

Minilake includes the following labels on the component side of the motherboard. The labels shall not be placed in a way, which may cause them to disrupt the functionality or the heat dissipation path of the module.

Description	Type	Barcode Required?
MAC Address for the SOC and/or the NIC.	Adhesive label	Yes
Vendor P/N, S/N, REV (Revision shall increment for any approved changes)	Adhesive label	Yes
Vendor Logo	Silk Screen	No
RoHS compliance	Silk Screen	No
WEEE symbol:  The module will have the crossed out wheeled bin symbol to indicate that it will be taken back by the Manufacturer for recycle at the end of its useful life. This is defined in the European Union Directive 2002/96/EC of January 27, 2003 on Waste Electrical and Electronic Equipment (WEEE) and any subsequent amendments.	Silk Screen	No

13. Revision History

Author	Description	Revision	Date
Xu Wang	▪ Initial draft	0.1	06/22/2015
Xu Wang	▪ Updated 7.5 BIOS requirements and 7.6 System Management ▪ Updated 5.1 COM-Express Connector Pinout	0.2	07/14/2015
Xu Wang	▪ Changed the SoC to Broadwell-DE	0.3	02/24/2016

	▪ General updates on Electrical Interface, Functional Requirements, and Environmental Requirements ▪ Added 9.2 Materials of Concern		
Xu Wang	▪ Added Intel TXT and DRTM support in 7.5 BIOS. ▪ Added 8 Hardware Validation ▪ Added 4.1 CPU Heatsink ▪ Updated 3.1 Module Mechanical Outline	0.4	03/16/2016
Xu Wang	▪ General update	0.5	05/22/2017
Xu Wang	▪ Merged the Spec Addendum Rev 0.1. ▪ Limited COM-Express Connector Pinout to Type 7 only ▪ Updated SoC SKU and DRAM requirements ▪ Updated PCIe and SMBus requirements	0.6	09/27/2017
John Fernandes	▪ Updated thermal requirements	0.7	10/08/2017
Jimmy Leung	▪ Updated mechanical requirements	0.8	10/09/2017
Xu Wang	▪ Updated PCIe and USB requirements ▪ Added TPM requirement ▪ Addded Wedge 100 backward compatibility requirement	0.9	10/16/2017
Xu Wang	▪ Updated PCIe, TPM, and EC interface requirements ▪ Added system-level channel budgeting information	1.0	12/06/2017
Xu Wang	▪ Marked SMBus as optional, and Intel At-Scale-Debug signals as reserved. Redefined GPI1 and GPO1 ▪ Clarified PXE timeout and error threshold requirements in 7.7 ▪ Updated system-level channel budgeting and topology information in 15	1.1	01/09/2018
Xu Wang	▪ Minor updates in 7.7 and 9.1	1.2	01/10/2018

Xu Wang	▪ Updated 15 ▪ Removed system reboot events, NMI, and sensor threshold crossing events from Logged errors in 7.7	1.3	02/08/2018
Xu Wang	▪ Updated the transportation temperature range to -40°C to +85°C.	1.4	03/01/2018
Hao Shen	▪ Update the PCIE link budget graph ▪ Update the Pin table	1.5	11/08/2019
Hao Shen	▪ Remove system related content	1.6	01/09/2019