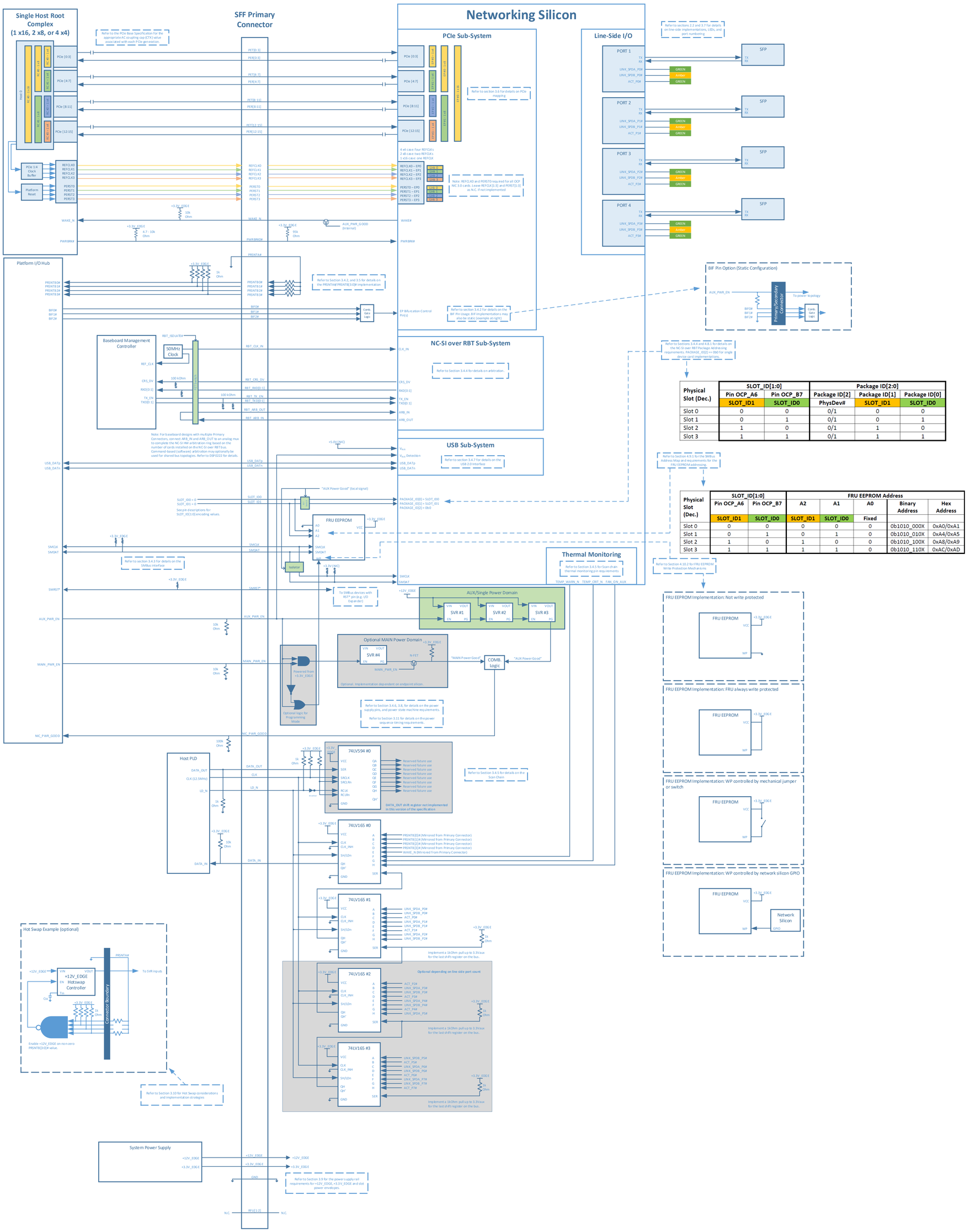
OCP NIC 3.0 SFF - Single Host Implementation Example (single, dual, quad link)



Physical Slot (Dec.)	SLOT_ID[1:0]		Package ID[2:0]		
	Pin OCP_A6	Pin OCP_B7	Package ID[2]	Package ID[1]	Package ID[0]
	SLOT_ID1	SLOT_ID0	PhysDev#	SLOT_ID1	SLOT_ID0
Slot 0	0	0	0/1	0	0
Slot 1	0	1	0/1	0	1
Slot 2	1	0	0/1	1	0
Slot 3	1	1	0/1	1	1

Physical Slot (Dec.)	SLOT_ID[1:0]		FRU EEPROM Address				
	Pin OCP_A6	Pin OCP_B7	A2	A1	A0	Binary Address	Hex Address
	SLOT_ID1	SLOT_ID0	SLOT_ID1	SLOT_ID0	Fixed		
Slot 0	0	0	0	0	0	0b1010_000X	0xA0/0xA1
Slot 1	0	1	0	1	0	0b1010_010X	0xA4/0xA5
Slot 2	1	0	1	0	0	0b1010_100X	0xA8/0xA9
Slot 3	1	1	1	1	0	0b1010_110X	0xAC/0xAD

Version, Date, Authors, Comments

0v91, 20190805b, MB/TN, Initial version for OCP NIC 3.0 WG review.

0v91, 20190815a, MB/TN, Clean up from initial round of comments.

0v92, 20191108a, TN, Change PCIe AC cap value to just state C_{TX} param, add note about hardware arbitration.