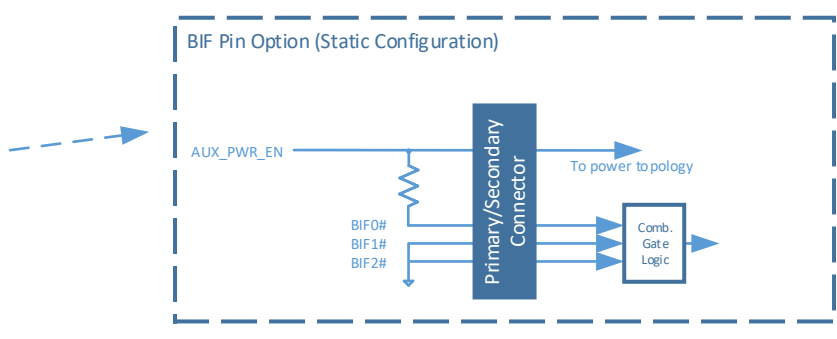
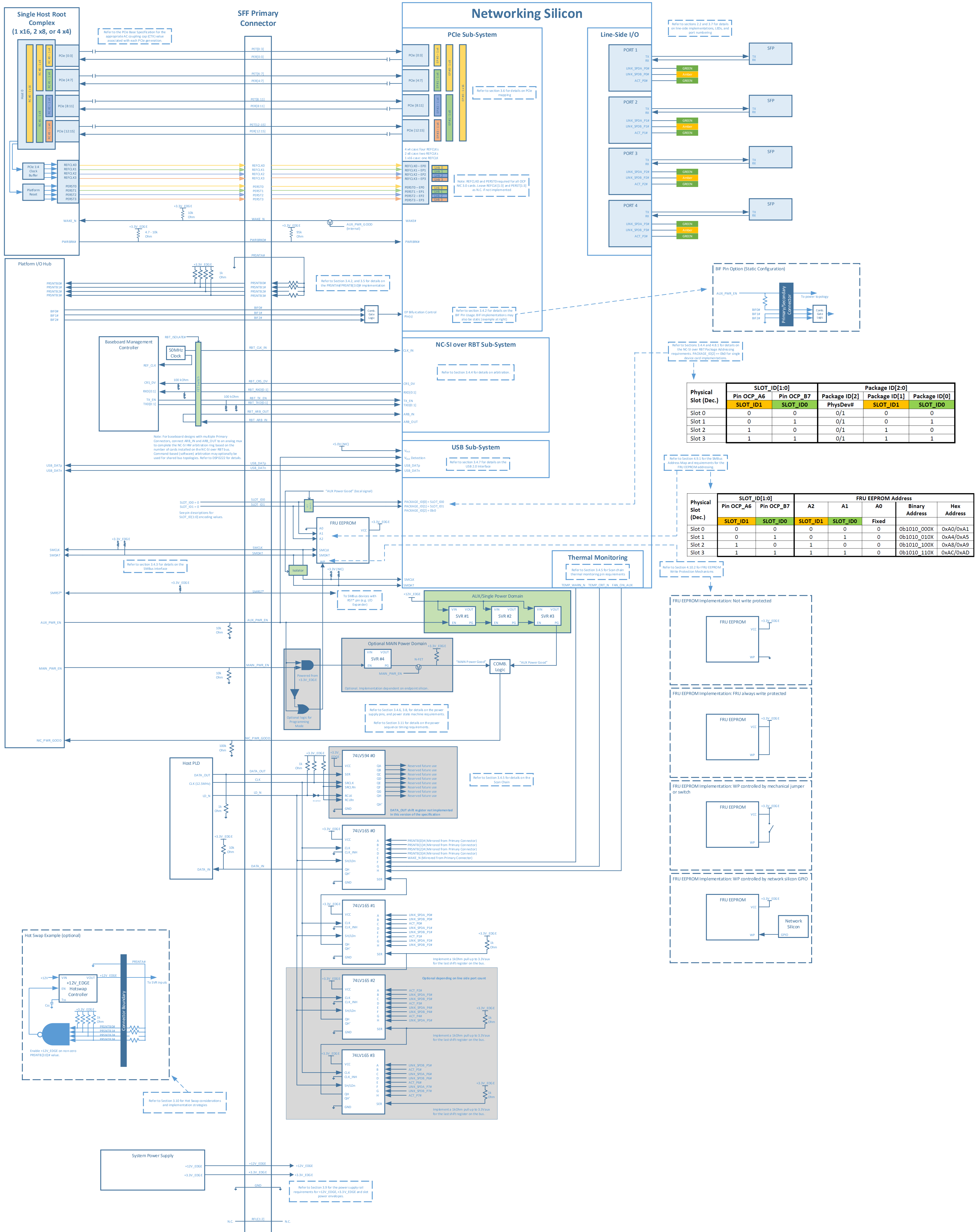
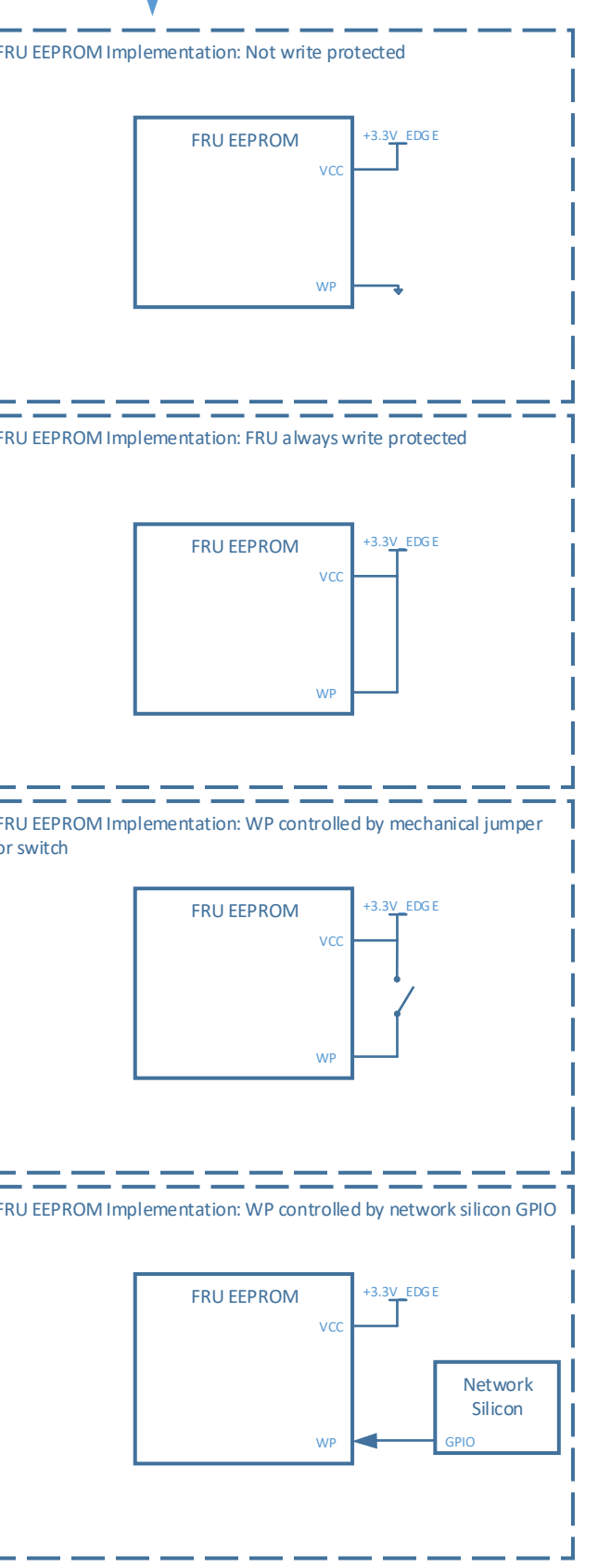


OCP NIC 3.0 SFF - Single Host Implementation Example (single, dual, quad link) with a 1x16 Option C card

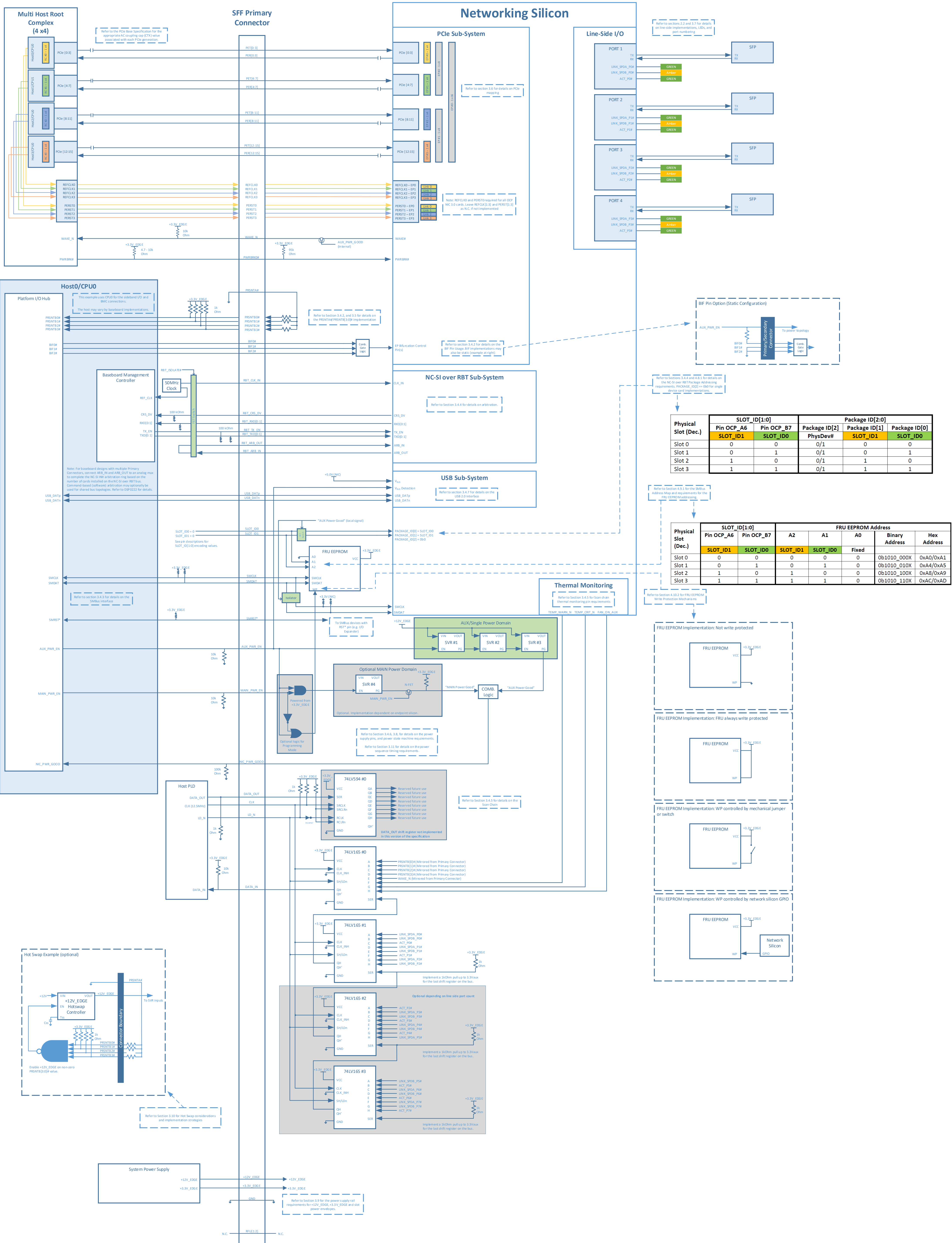


Physical Slot (Dec.)	SLOT_ID[1:0]		Package ID[2]		Package ID[1]		Package ID[0]	
	Pin OCP_A6	Pin OCP_B7	PhysDev#	SLOT_ID1	SLOT_ID0	SLOT_ID1	SLOT_ID0	
Slot 0	0	0	0/1	0	0	0	0	
Slot 1	0	1	0/1	0	1	0	1	
Slot 2	1	0	0/1	1	0	1	0	
Slot 3	1	1	0/1	1	1	1	1	

Physical Slot (Dec.)	SLOT_ID[1:0]		FRU EEPROM Address		Binary Address	Hex Address
	Pin OCP_A6	Pin OCP_B7	A2	A1		
Slot 0	0	0	0	0	0b1010_000X	0xA0/0xA1
Slot 1	0	1	0	1	0b1010_010X	0xA4/0xA5
Slot 2	1	0	1	0	0b1010_100X	0xA8/0xA9
Slot 3	1	1	1	1	0b1010_110X	0xAC/0xAD



OCP NIC 3.0 SFF – Quad Slot Implementation Example with a 1x16 Option C card



Refer to sections 3.2 and 3.7 for details on line side implementations, LEDs and port numbering.

Refer to section 3.4.2 and 3.5 for details on the physical layer implementation.

Refer to section 3.4.2 for details on the RBT Pin Usage. RBT implementations may also be used for power management.

Refer to section 3.4.4 for details on the NC-SI over RBT implementation.

Refer to section 3.4.7 for details on the USB 2.0 interface.

Refer to section 3.4.5 for details on the thermal monitoring pin requirements.

Refer to section 4.0.2 for FRU EEPROM write protection mechanisms.

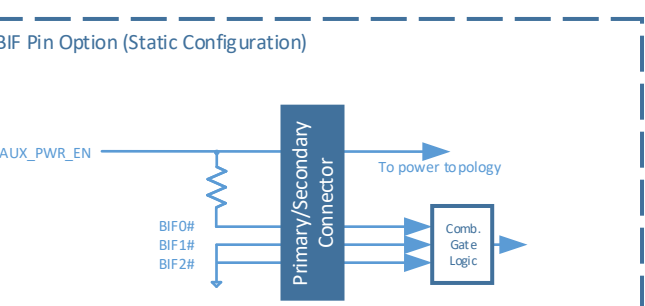
Refer to section 3.4.3 for details on the Host0/CPU0.

Refer to section 3.10 for the power supply pin requirements for +12V_EEDGE, +3.3V_EEDGE and hot power envelopes.

Refer to section 3.10 for the power supply pin requirements for +12V_EEDGE, +3.3V_EEDGE and hot power envelopes.

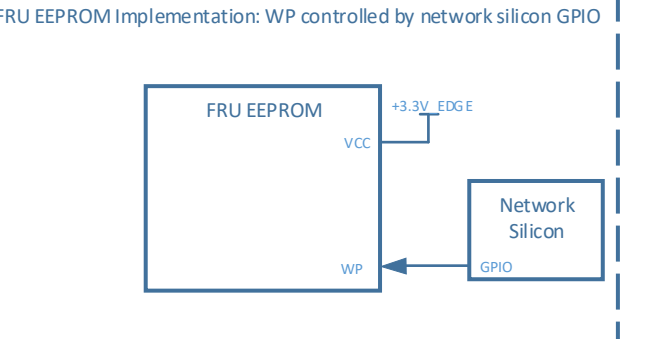
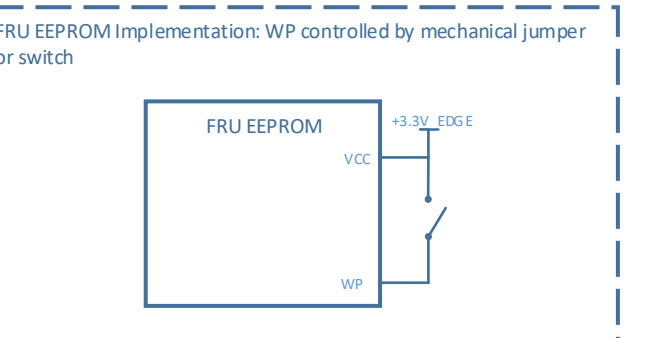
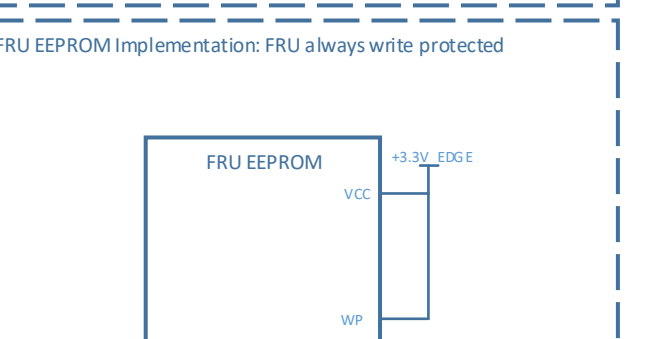
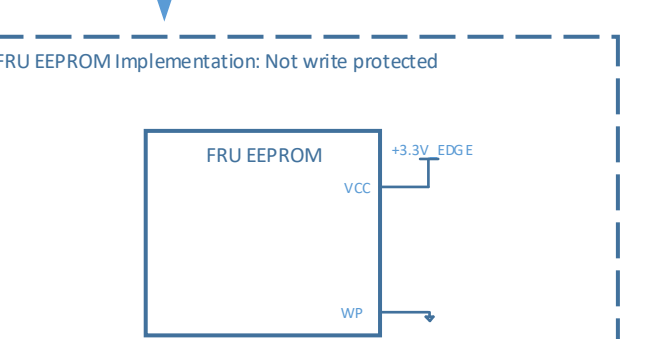
Refer to section 3.10 for the power supply pin requirements for +12V_EEDGE, +3.3V_EEDGE and hot power envelopes.

Refer to section 3.10 for the power supply pin requirements for +12V_EEDGE, +3.3V_EEDGE and hot power envelopes.



Physical Slot (Dec.)	SLOT_ID[1:0]		Package ID[2]	Package ID[1]		Package ID[0]
	Pin OCP_A6	Pin OCP_B7		SLOT_ID1	SLOT_ID0	
Slot 0	0	0	O/1	0	0	
Slot 1	0	1	O/1	0	1	
Slot 2	1	0	O/1	1	0	
Slot 3	1	1	O/1	1	1	

Physical Slot (Dec.)	SLOT_ID[1:0]		FRU EEPROM Address				
	Pin OCP_A6	Pin OCP_B7	A2	A1	A0	Binary Address	Hex Address
Slot 0	0	0	0	0	0	0b1010_000X	OxA0/OxA1
Slot 1	0	1	0	1	0	0b1010_010X	OxA4/OxA5
Slot 2	1	0	1	0	0	0b1010_100X	OxA8/OxA9
Slot 3	1	1	1	1	0	0b1010_110X	OxAC/OxAD



Version, Date, Authors, Comments

0v91, 20190805b, MB/TN, Initial version for OCP NIC 3.0 WG review.

0v91, 20190815a, MB/TN, Clean up from initial round of comments.

0v92, 20191108a, TN, Change PCIe AC cap value to just state C_{TX} param, add note about hardware arbitration.

0v92, 20191112a, MB/TN, Add multi-host implementation example to second page.