



OPEN
Compute Project

OCP NIC 3.0 Design Specification

Version 1.2.1 - DRAFT 1.2.0

Author: OCP Server Workgroup, OCP NIC subgroup

Table of Contents

| | | |
|----------|---|-----------------|
| 1 | Overview | 11 |
| 1.1 | License | 11 |
| 1.2 | Acknowledgements | 12 |
| 1.3 | References | 13 |
| 1.3.1 | Trademarks | 14 |
| 1.4 | Acronyms | 15 |
| 1.5 | Conventions | 16 |
| 1.6 | Background | 18 |
| 1.7 | Overview | 21 |
| 1.7.1 | Mechanical Form Factor Overview | 21 |
| 1.7.2 | Electrical Overview | 23 |
| 1.7.2.1 | Primary Connector | 23 |
| 1.7.2.2 | Secondary Connector | 24 |
| 1.8 | Non-NIC Use Cases | 24 |
| 2 | Mechanical Card Form Factor | 25 |
| 2.1 | Form Factor Options | 25 |
| 2.1.1 | SFF and TSFF Faceplate Configurations | 27 |
| 2.1.2 | LFF Faceplate Configurations | 31 |
| 2.2 | Line Side I/O Implementations | 35 |
| 2.3 | Top Level Assembly (SFF, TSFF and LFF) | 36 |
| 2.4 | Faceplate Subassembly (SFF, TSFF and LFF) | 38 |
| 2.4.1 | Faceplate Subassembly – Exploded View | 38 |
| 2.4.2 | Faceplate Subassembly – Bill of Materials (BOM) | 38 |
| 2.4.3 | SFF Generic I/O Faceplates | 41 |
| 2.4.4 | TSFF Generic I/O Faceplates | 42 |
| 2.4.5 | LFF Generic I/O Faceplate | 44 |
| 2.4.6 | Ejector Lever (SFF, TSFF) | 45 |
| 2.4.7 | Ejector Levers (LFF) | 46 |
| 2.4.8 | Ejector Lock (SFF, TSFF and LFF) | 47 |
| 2.4.9 | Clinch Nut (SFF and LFF) | 48 |
| 2.5 | Card Keep Out Zones | 49 |
| 2.5.1 | SFF Keep Out Zones | 49 |
| 2.5.2 | TSFF Keep Out Zones | 52 |
| 2.5.3 | LFF Keep Out Zones | 53 |
| 2.6 | Baseboard Keep Out Zones | 56 |
| 2.7 | Insulation Requirements | 57 |
| 2.7.1 | SFF, TSFF Insulator | 57 |
| 2.7.2 | LFF Insulator | 59 |
| 2.8 | Critical-to-Function (CTF) Dimensions (SFF, TSFF and LFF) | 62 |
| 2.8.1 | CTF Tolerances | 62 |
| 2.8.2 | SFF Pull Tab CTF Dimensions | 62 |
| 2.8.3 | SFF Ejector Latch CTF Dimensions | 64 |
| 2.8.4 | SFF Internal Lock CTF Dimensions | 65 |
| 2.8.5 | SFF Baseboard CTF Dimensions | 66 |
| 2.8.6 | TSFF Pull Tab CTF Dimensions | 7069 |
| 2.8.7 | TSFF Ejector Latch CTF Dimensions | 7069 |
| 2.8.8 | TSFF Internal Lock CTF Dimensions | 7069 |
| 2.8.9 | TSFF Baseboard CTF Dimensions | 7069 |
| 2.8.10 | LFF Ejector Latch CTF Dimensions | 7069 |
| 2.8.11 | LFF Baseboard CTF Dimensions | 7274 |
| 2.9 | Labeling Requirements | 7574 |
| 2.9.1 | General Guidelines for Label Contents | 7574 |
| 2.9.2 | MAC Address Labeling Requirements | 7675 |
| 2.9.2.1 | MAC Address Label Example 1 – Quad Port with Single Host, Single Managed Controller | 7776 |
| 2.9.2.2 | MAC Address Label Example 2 – Octal Port with Single Host, Dual Managed Controllers | 7776 |
| 2.9.2.3 | MAC Address Label Example 3 – Quad Port with Dual Hosts, Dual Managed Controllers | 7877 |
| 2.9.2.4 | MAC Address Label Example 4 – Single Port with Quad Host, Single Managed Controller | 7877 |

| | | |
|----------|---|---------------|
| 2.10 | Mechanical CAD Package Examples | 8079 |
| 3 | Electrical Interface Definition – Card Edge and Baseboard | 8180 |
| 3.1 | Card Edge Gold Finger Requirements | 8180 |
| 3.1.1 | Gold Finger Mating Sequence | 8382 |
| 3.2 | Baseboard Connector Requirements | 8786 |
| 3.2.1 | Right Angle Connector | 8786 |
| 3.2.2 | Right Angle Offset | 8887 |
| 3.2.3 | Straddle Mount Connector | 8887 |
| 3.2.4 | Straddle Mount Offset and PCB Thickness Options | 9089 |
| 3.2.5 | LFF Connector Locations | 9190 |
| 3.3 | Pin Definition | 9190 |
| 3.3.1 | Primary Connector | 9291 |
| 3.3.2 | Secondary Connector | 9493 |
| 3.4 | Signal Descriptions | 9594 |
| 3.4.1 | PCIe Interface Pins | 9594 |
| 3.4.2 | PCIe Present and Bifurcation Control Pins | 102401 |
| 3.4.3 | SMBus Interface Pins | 105404 |
| 3.4.4 | NC-SI over RBT Interface Pins | 106405 |
| 3.4.5 | Scan Chain Pins | 115413 |
| 3.4.6 | Power Supply Pins | 124422 |
| 3.4.7 | USB 2.0 (A68/A69) – Primary Connector Only | 129427 |
| 3.4.8 | UART (A68/A69) – Secondary Connector Only | 131429 |
| 3.4.9 | RFU[1:4] Pins | 132430 |
| 3.5 | PCIe Bifurcation Mechanism | 133431 |
| 3.5.1 | PCIe OCP NIC 3.0 Card to Baseboard Bifurcation Configuration (PRSN A #, PRSN T B[3:0]#) | 133431 |
| 3.5.2 | PCIe Baseboard to OCP NIC 3.0 Card Bifurcation Configuration (BIF[2:0]#) | 133431 |
| 3.5.3 | PCIe Bifurcation Decoder | 134432 |
| 3.5.4 | Bifurcation Detection Flow | 136434 |
| 3.5.5 | PCIe Bifurcation Examples | 137435 |
| 3.5.5.1 | Single Host (1 x16) Baseboard with a 1 x16 OCP NIC 3.0 Card (Single Controller) | 137435 |
| 3.5.5.2 | Single Host (2 x8) Baseboard with a 2 x8 OCP NIC 3.0 Card (Dual Controllers) | 138436 |
| 3.5.5.3 | Quad Host (4 x4) Baseboard with a 4 x4 OCP NIC 3.0 Card (Single Controller) | 139437 |
| 3.5.5.4 | Quad Host (4 x4) Baseboard with a 4 x4 OCP NIC 3.0 Card (Quad Controllers) | 140438 |
| 3.5.5.5 | Single Host (1 x16, no Bifurcation) Baseboard with a 2 x8 OCP NIC 3.0 Card (Dual Controller) | 141439 |
| 3.6 | PCIe REFCLK and PERST# Mapping | 142440 |
| 3.6.1 | SFF, TSFF PCIe REFCLK and PERST# Mapping | 143441 |
| 3.6.2 | LFF PCIe REFCLK and PERST# Mapping | 146444 |
| 3.6.3 | REFCLK and PERST# Mapping Expansion | 148446 |
| 3.7 | Port Numbering and LED Implementations | 149447 |
| 3.7.1 | OCP NIC 3.0 Port Naming and Port Numbering | 149447 |
| 3.7.2 | OCP NIC 3.0 Card LED Configuration | 149447 |
| 3.7.3 | OCP NIC 3.0 Card LED Ordering | 151449 |
| 3.7.4 | Baseboard LEDs Configuration over the Scan Chain | 152450 |
| 3.8 | Power State Machine | 154452 |
| 3.8.1 | NIC Power Off | 155453 |
| 3.8.2 | ID Mode | 155453 |
| 3.8.3 | Aux Power Mode | 156454 |
| 3.8.4 | Main Power Mode | 156454 |
| 3.8.5 | Programming Mode | 156454 |
| 3.9 | Power Supply Rail Requirements and Slot Power Envelopes | 158455 |
| 3.10 | Hot Swap Considerations for +12V_EDGE and +3.3V_EDGE Rails | 159456 |
| 3.11 | Power Sequence Timing Requirements | 160457 |
| 3.12 | Digital I/O Specifications | 164461 |
| 4 | Management and Pre-OS Requirements | 165462 |
| 4.1 | Sideband Management Interface and Transport | 165462 |
| 4.2 | NC-SI Traffic | 166463 |
| 4.3 | Management Controller (MC) MAC Address Provisioning | 166463 |
| 4.4 | ASIC Die Temperature Reporting | 169466 |

| | | |
|----------|--|--------------------------|
| 4.5 | Power Consumption Reporting | 171 168 |
| 4.6 | Pluggable Transceiver Module Status and Temperature Reporting | 172 169 |
| 4.7 | Management and Pre-OS Firmware Inventory and Update | 172 169 |
| 4.7.1 | Secure Firmware | 173 170 |
| 4.7.2 | Firmware Inventory | 173 170 |
| 4.7.3 | Firmware Inventory and Update in Multi-Host Environments..... | 173 170 |
| 4.8 | NC-SI Package Addressing and Hardware Arbitration Requirements | 174 171 |
| 4.8.1 | NC-SI over RBT Package Addressing..... | 174 171 |
| 4.8.2 | Arbitration Ring Connections..... | 174 171 |
| 4.9 | SMBus 2.0 Addressing Requirements | 174 171 |
| 4.9.1 | SMBus Address Map | 175 172 |
| 4.10 | FRU EEPROM..... | 175 172 |
| 4.10.1 | FRU EEPROM Addressing and Size | 175 172 |
| 4.10.2 | FRU EEPROM Write Protection..... | 177 174 |
| 4.10.3 | FRU EEPROM Content Requirements | 177 174 |
| 4.10.4 | FRU Template | 184 181 |
| 5 | Routing Guidelines and Signal Integrity Considerations | 185182 |
| 5.1 | NC-SI over RBT | 185 182 |
| 5.1.1 | SFF/TSFF Baseboard Requirements | 186 183 |
| 5.1.2 | LFF Baseboard Requirements | 187 184 |
| 5.1.3 | SFF/TSFF OCP NIC 3.0 Card Requirements..... | 187 184 |
| 5.1.4 | LFF OCP NIC 3.0 Card Requirements..... | 188 185 |
| 5.2 | SMBus 2.0 | 189 186 |
| 5.3 | PCIe..... | 189 186 |
| 5.3.1 | Channel Requirements | 189 186 |
| 5.3.1.1 | REFCLK requirements | 189 186 |
| 5.3.1.2 | Add-in Card Electrical Budgets | 189 186 |
| 5.3.1.3 | Baseboard Channel Budget | 190 187 |
| 5.3.1.4 | SFF-TA-1002 Connector Channel Budget | 190 187 |
| 5.3.1.5 | Differential Impedance (Informative) | 190 187 |
| 5.3.2 | Test Fixtures..... | 190 187 |
| 5.3.2.1 | Compliance Load Board (CLB) | 191 188 |
| 5.3.2.2 | Compliance Baseboard (CBB) | 192 189 |
| 5.3.3 | Test Methodology..... | 192 189 |
| 5.3.3.1 | Test Setup | 192 189 |
| 6 | Thermal and Environmental | 194191 |
| 6.1 | Airflow Direction..... | 194 191 |
| 6.1.1 | Hot Aisle Cooling..... | 194 191 |
| 6.1.2 | Cold Aisle Cooling | 195 192 |
| 6.2 | Thermal Design Guidelines | 196 193 |
| 6.2.1 | SFF Card ASIC Cooling – Hot Aisle | 196 193 |
| 6.2.2 | TSFF Card ASIC Cooling – Hot Aisle (TBD) | 200 197 |
| 6.2.3 | LFF Card ASIC Cooling – Hot Aisle | 200 197 |
| 6.2.4 | SFF Card ASIC Cooling – Cold Aisle | 202 199 |
| 6.2.5 | TSFF Card ASIC Cooling – Cold Aisle (TBD) | 205 202 |
| 6.2.6 | LFF Card ASIC Cooling – Cold Aisle | 205 202 |
| 6.3 | Thermal Simulation (CFD) Modeling..... | 207 204 |
| 6.4 | Thermal Test Fixture | 207 204 |
| 6.4.1 | Test Fixture for SFF Card | 208 205 |
| 6.4.2 | Test Fixture for TSFF Card (TBD) | 210 207 |
| 6.4.3 | Test Fixture for LFF Card | 210 207 |
| 6.4.4 | Test Fixture Airflow Direction | 212 209 |
| 6.4.5 | Thermal Test Fixture Candlestick Sensors..... | 212 209 |
| 6.5 | Card Sensor Requirements | 215 212 |
| 6.6 | Card Cooling Tiers | 215 212 |
| 6.7 | Non-Operational Shock & Vibration Testing..... | 217 214 |
| 6.7.1 | Shock & Vibe Test Fixture | 217 214 |
| 6.7.2 | Test Procedure | 218 215 |

| | | |
|----------|---|-------------------------------|
| 6.8 | Dye and Pull Test Method..... | 220 217 |
| 6.9 | Gold Finger Plating Requirements | 222 219 |
| 6.9.1 | Host Side Gold Finger Plating Requirements | 222 219 |
| 6.9.2 | Line Side Gold Finger Durability Requirements | 222 219 |
| 7 | Regulatory | 223 220 |
| 7.1 | Required Compliance..... | 223 220 |
| 7.1.1 | Required Environmental Compliance | 223 220 |
| 7.1.2 | Required EMC Compliance | 223 220 |
| 7.1.3 | Required Product Safety Compliance | 224 221 |
| 7.1.4 | Required Immunity (ESD) Compliance..... | 224 221 |
| 7.2 | Recommended Compliance | 224 221 |
| 7.2.1 | Recommended Environmental Compliance..... | 225 222 |
| 7.2.2 | Recommended EMC Compliance..... | 225 222 |
| 8 | Revision History | 226 223 |
| 8.1 | Document Revision History..... | 226 223 |
| 8.2 | FRU Content Revision History..... | 235 222 |

List of Figures

| | | |
|------------|--|----|
| Figure 1: | Representative SFF OCP NIC 3.0 Card with Dual QSFP Ports | 19 |
| Figure 2: | Representative TSFF OCP NIC 3.0 Card with Dual QSFP Ports | 19 |
| Figure 3: | Representative LFF OCP NIC 3.0 Card with Dual QSFP Ports and on-board DRAM..... | 20 |
| Figure 4: | SFF/TSFF and LFF Block Diagrams (not to scale) | 21 |
| Figure 5: | Primary Connector (4C+) and Secondary Connector (4C) (LFF) OCP NIC 3.0 Cards | 25 |
| Figure 6: | Primary Connector (4C+) Only (LFF) OCP NIC 3.0 Cards..... | 26 |
| Figure 7: | Primary Connector (4C+) with 4C and 2C (SFF) OCP NIC 3.0 Cards | 26 |
| Figure 8: | SFF/TSFF NIC Configuration Views..... | 28 |
| Figure 9: | SFF NIC Line Side 3D Views | 29 |
| Figure 10: | SFF NIC Chassis Mounted 3D Views | 30 |
| Figure 11: | LFF NIC Configuration Views | 32 |
| Figure 12: | LFF NIC Line Side 3D Views | 33 |
| Figure 13: | LFF NIC Chassis Mounted 3D Views | 34 |
| Figure 14: | PBA Exploded Views (SFF, TSFF and LFF)..... | 36 |
| Figure 15: | Faceplate Assembly Exploded Views (SFF, TSFF and LFF) | 38 |
| Figure 16: | SFF Generic I/O Faceplate – Pull Tab Version (2D View)..... | 41 |
| Figure 17: | SFF Generic I/O Faceplate – Ejector Version (2D View) | 41 |
| Figure 18: | SFF Generic I/O Faceplate – Internal Lock Version (2D View)..... | 42 |
| Figure 19: | TSFF Generic I/O Faceplate – Pull Tab Version (2D View)..... | 42 |
| Figure 20: | TSFF Generic I/O Faceplate – Ejector Version (2D View) | 43 |
| Figure 21: | TSFF Generic I/O Faceplate – Internal Lock Version (2D View)..... | 43 |
| Figure 22: | LFF Generic I/O Faceplate – Ejector Version (2D View) | 44 |
| Figure 23: | SFF I/O Faceplate – Ejector Lever (2D View) | 45 |
| Figure 24: | LFF I/O Faceplate – Ejector Lever (2D View) | 46 |
| Figure 25: | Ejector Lock..... | 47 |
| Figure 26: | Clinch Nut Option A | 48 |
| Figure 27: | Clinch Nut Option B..... | 48 |
| Figure 28: | SFF Keep Out Zone – Top View | 49 |
| Figure 29: | SFF Keep Out Zone – Top View – Detail A | 50 |
| Figure 30: | SFF Keep Out Zone – Bottom View | 50 |
| Figure 31: | SFF Keep Out Zone – Side View..... | 51 |
| Figure 32: | SFF Keep Out Zone – Side View – Detail D | 51 |
| Figure 33: | TSFF Keep Out Zone – Side View..... | 52 |
| Figure 34: | LFF Keep Out Zone – Top View | 53 |
| Figure 35: | LFF Keep Out Zone – Top View – Detail A | 54 |
| Figure 36: | LFF Keep Out Zone – Bottom View | 55 |
| Figure 37: | LFF Keep Out Zone – Side View | 55 |

| | |
|---|-------------------|
| Figure 38: LFF Keep Out Zone – Side View – Detail D | 56 |
| Figure 39: SFF, TSFF Bottom Side Insulator (3D View) | 57 |
| Figure 40: SFF, TSFF Bottom Side Insulator (Top and Side View) | 58 |
| Figure 41: SFF, TSFF Bottom Side Insulator (alternate) (Top and Side View) | 59 |
| Figure 42: LFF Bottom Side Insulator (3D View) | 59 |
| Figure 43: LFF Bottom Side Insulator (Top and Side View) | 60 |
| Figure 44: LFF Bottom Side Insulator (alternate) (Top and Side View) | 61 |
| Figure 45: SFF OCP NIC 3.0 Card with Pull Tab CTF Dimensions (Top View) | 62 |
| Figure 46: SFF OCP NIC 3.0 Card with Pull Tab CTF Dimensions (Front View)..... | 63 |
| Figure 47: SFF OCP NIC 3.0 Card with Pull Tab CTF Dimensions (Side View) | 63 |
| Figure 48: SFF OCP NIC 3.0 Card with Ejector Latch CTF Dimensions (Top View) | 64 |
| Figure 49: SFF OCP NIC 3.0 Card with Ejector CTF Dimensions (Front View) | 64 |
| Figure 50: SFF OCP NIC 3.0 Card with Ejector CTF Dimensions (Side View) | 65 |
| Figure 51: SFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Top View) | 65 |
| Figure 52: SFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Front View)..... | 66 |
| Figure 53: SFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Side View) | 66 |
| Figure 54: SFF Baseboard Chassis CTF Dimensions (Rear View) | 66 |
| Figure 55: SFF Baseboard Chassis to Card Thumb Screw CTF Dimensions (Side View)..... | 67 |
| Figure 56: SFF Baseboard Chassis to Ejector lever Card CTF Dimensions (Side View) | 67 |
| Figure 57: SFF Baseboard Chassis CTF Dimensions (Rear Rail Guide View) | 67 |
| Figure 58: SFF Baseboard Chassis CTF Dimensions (Rail Guide Detail) – Detail C | 68 |
| Figure 59: TSFF OCP NIC 3.0 Card with Pull Tab CTF Dimensions (Top View) | 7069 |
| Figure 60: TSFF OCP NIC 3.0 Card with Ejector Latch CTF Dimensions (Top View) | 7069 |
| Figure 61: TSFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Top View) | 7069 |
| Figure 62: TSFF Baseboard Chassis CTF Dimensions (Rear View)..... | 7069 |
| Figure 63: LFF OCP NIC 3.0 Card with Ejector Latch CTF Dimensions (Top View) | 7170 |
| Figure 64: LFF OCP NIC 3.0 Card with Ejector CTF Dimensions (Front View) | 7170 |
| Figure 65: LFF OCP NIC 3.0 Card with Ejector CTF Dimensions (Side View) | 7271 |
| Figure 66: LFF Baseboard Chassis CTF Dimensions (Rear View)..... | 7271 |
| Figure 67: LFF Baseboard Chassis CTF Dimensions (Side View) | 7372 |
| Figure 68: LFF Baseboard Chassis CTF Dimensions (Rail Guide View) | 7372 |
| Figure 69: LFF Baseboard Chassis CTF Dimensions (Rail Guide – Detail C) | 7372 |
| Figure 70: SFF, TSFF Label Area Example | 7574 |
| Figure 71: MAC Address Label Example 1 – Quad Port with Single Host, Single Managed Controller | 7776 |
| Figure 72: MAC Address Label Example 2 – Octal Port with Single Host, Dual Managed Controller | 7877 |
| Figure 73: MAC Address Label Example 3 – Quad Port with Dual Hosts, Dual Managed Controllers | 7877 |
| Figure 74: MAC Address Label Example 4 – Single Port with Quad Host, Single Managed Controller | 7978 |
| Figure 75: MAC Address Label Example 5 – Octal Port with Single Host, Octal Managed Controller | 7978 |
| Figure 76: SFF, TSFF Primary Connector Gold Finger Dimensions – x16 – Top Side (“B” Pins) | 8180 |
| Figure 77: SFF, TSFF Primary Connector Card Profile Dimensions | 8281 |
| Figure 78: SFF, TSFF Primary Connector Gold Finger - Detail D | 8281 |
| Figure 79: LFF Gold Finger Dimensions – x32 – Top Side (“B” Pins)..... | 8382 |
| Figure 80: LFF Gold Finger Dimensions – x32 – Bottom Side (“A” Pins)..... | 8382 |
| Figure 81: 168-pin Base Board Primary Connector – Right Angle..... | 8786 |
| Figure 82: 140-pin Base Board Secondary Connector – Right Angle..... | 8887 |
| Figure 83: OCP NIC 3.0 Card and Host Offset for Right Angle Connectors..... | 8887 |
| Figure 84: 168-pin Base Board Primary Connector – Straddle Mount | 8988 |
| Figure 85: 140-pin Base Board Secondary Connector – Straddle Mount..... | 8988 |
| Figure 86: OCP NIC 3.0 Card and Baseboard PCB Thickness Options for Straddle Mount Connectors..... | 9089 |
| Figure 87: 0 mm Offset (Coplanar) for 0.062” Thick Baseboards..... | 9089 |
| Figure 88: 0.3 mm Offset for 0.076” Thick Baseboards | 9190 |
| Figure 89: Primary and Secondary Connector Locations for LFF Support with Right Angle Connectors | 9190 |
| Figure 90: Primary and Secondary Connector Locations for LFF Support with Straddle Mount Connectors | 9190 |
| Figure 91: PCIe Present and Bifurcation Control Pins (Baseboard Controlled BIF[2:0]#)..... | 104403 |
| Figure 92: PCIe Present and Bifurcation Control Pins (Static BIF[2:0]#)..... | 104403 |
| Figure 93: Example SMBus Connections | 106405 |
| Figure 94: NC-SI over RBT Connection Example – Single Primary Connector | 113411 |
| Figure 95: NC-SI over RBT Connection Example – Dual Primary Connectors..... | 114412 |

| | |
|---|--------|
| Figure 96: Scan Chain Timing Diagram Example 1 | 117145 |
| Figure 97: Scan Chain Timing Diagram Example 2 | 117145 |
| Figure 98: Scan Chain Connection Example | 123121 |
| Figure 99: Example Power Supply Topology | 128126 |
| Figure 100: USB 2.0 Connection Example – Basic Connectivity | 130128 |
| Figure 101: USB 2.0 Connection Example – USB-Serial / USB-JTAG Connectivity | 130128 |
| Figure 102: UART Connection Example | 132130 |
| Figure 103: Single Host (1 x16) and 1 x16 OCP NIC 3.0 Card (Single Controller)..... | 137135 |
| Figure 104: Single Host (2 x8) and 2 x8 OCP NIC 3.0 Card (Dual Controllers) | 138136 |
| Figure 105: Quad Hosts (4 x4) and 4 x4 OCP NIC 3.0 Card (Single Controller) | 139137 |
| Figure 106: Quad Hosts (4 x4) and 4 x4 OCP NIC 3.0 Card (Quad Controllers) | 140138 |
| Figure 107: Single Host with no Bifurcation (1 x16) and 2 x8 OCP NIC 3.0 Card (Dual Controllers)..... | 141139 |
| Figure 108: SFF/TSFF PCIe REFCLK Mapping – Single Host – 1, 2 and 4 links | 143141 |
| Figure 109: SFF/TSFF PCIe REFCLK Mapping – Dual Host – 2 and 4 links | 144142 |
| Figure 110: SFF/TSFF PCIe REFCLK Mapping – Quad Host – 4 Links | 145143 |
| Figure 111: LFF PCIe REFCLK Mapping – Single Host – 1, 2 and 4 links | 146144 |
| Figure 112: LFF PCIe REFCLK Mapping – Dual Host – 2 and 4 links | 147145 |
| Figure 113: LFF PCIe REFCLK Mapping – Quad Host – 4 Links | 148146 |
| Figure 114: Port and LED Ordering – Example SFF Link/Activity and Speed LED Placement | 152150 |
| Figure 115: Baseboard Power States | 154152 |
| Figure 116: Power-Up Sequencing – Normal Operation | 160157 |
| Figure 117: Power-Down Sequencing – Normal Operation | 161158 |
| Figure 118: Programming Mode Sequencing..... | 162159 |
| Figure 119: FRU EEPROM Writes with Double Byte Addressing | 176173 |
| Figure 120: FRU EEPROM Reads with Double Byte Addressing | 176173 |
| Figure 121: FRU Update Flow | 177174 |
| Figure 122: NC-SI over RBT Timing Budget Topology | 186183 |
| Figure 123: NC-SI over RBT Propagation Delay Matching for Two Target ASICs – No Clock Buffer | 188185 |
| Figure 124: NC-SI over RBT Propagation Delay Matching for Two Target ASICs – Clock Buffer..... | 188185 |
| Figure 125: PCIe Load Board Test Fixture for OCP NIC 3.0 SFF/TSFF | 191188 |
| Figure 126: PCIe Base Board Test Fixture for OCP NIC 3.0 SFF/TSFF..... | 192189 |
| Figure 127: Airflow Direction for Hot Aisle Cooling (SFF/TSFF and LFF) | 194191 |
| Figure 128: Airflow Direction for Cold Aisle Cooling (SFF/TSFF and LFF) | 195192 |
| Figure 129: ASIC Supportable Power for Hot Aisle Cooling – SFF | 196193 |
| Figure 130: OCP NIC 3.0 SFF Reference Design and CFD Geometry..... | 197194 |
| Figure 131: Server System Airflow Capability – SFF Card Hot Aisle Cooling | 198195 |
| Figure 132: Server System Airflow Capability – SFF Card Hot Aisle Cooling in Aux Power Mode | 199196 |
| Figure 133: ASIC Supportable Power for Hot Aisle Cooling – LFF Card | 200197 |
| Figure 134: OCP NIC 3.0 LFF Reference Design and CFD Geometry..... | 200197 |
| Figure 135: Server System Airflow Capability – LFF Card Hot Aisle Cooling..... | 202199 |
| Figure 136: ASIC Supportable Power for Cold Aisle Cooling – SFF Card..... | 203200 |
| Figure 137: Server System Airflow Capability – SFF Cold Aisle Cooling | 204201 |
| Figure 138: ASIC Supportable Power Comparison – SFF Card | 204201 |
| Figure 139: ASIC Supportable Power for Cold Aisle Cooling – LFF Card..... | 205202 |
| Figure 140: Server System Airflow Capability – LFF Cold Aisle Cooling..... | 206203 |
| Figure 141: ASIC Supportable Power Comparison – LFF Card..... | 206203 |
| Figure 142: SFF Thermal Test Fixture Preliminary Design | 208205 |
| Figure 143: SFF Thermal Test Fixture Preliminary Design – Cover Removed | 209206 |
| Figure 144: SFF Card Thermal Test Fixture PCB | 209206 |
| Figure 145: LFF Card Thermal Test Fixture Design | 210207 |
| Figure 146: LFF Card Thermal Test Fixture Design – Cover Removed | 210207 |
| Figure 147: LFF Card Thermal Test Fixture PCB | 211208 |
| Figure 148: Thermal Test Fixture Airflow Direction | 212209 |
| Figure 149: External Thermocouple Placement for Cold Aisle Inlet Temperature Measurement | 213210 |
| Figure 150: SFF Fixture, Hot Aisle Flow – Candlestick Air Velocity vs. Volume Flow..... | 214211 |
| Figure 151: TSFF Fixture, Hot Aisle Flow – Candlestick Air Velocity vs. Volume Flow (TBD)..... | 214211 |
| Figure 152: LFF Fixture, Hot Aisle Flow – Candlestick Air Velocity vs. Volume Flow..... | 214211 |
| Figure 153: Graphical View of Card Cooling Tiers | 216213 |

Open Compute Project • OCP NIC 3.0

Version ~~1.2.1 - DRAFT~~ 2.0

Figure 154: Typical Operating Range for Hot Aisle Configurations ~~216~~213

Figure 155: Typical Operating Range for Cold Aisle Configurations ~~217~~214

Figure 156: SFF/TSFF Shock and Vibe Fixture ~~218~~215

Figure 157: LFF Shock and Vibe Fixture ~~218~~215

Figure 158: Dye and Pull Type Locations ~~221~~218

Figure 159: Dye Coverage Percentage ~~221~~218

List of Tables

| | |
|---|--------------------|
| Table 1: Acknowledgements – Current Contributors – By Company..... | 12 |
| Table 2: Acronyms | 15 |
| Table 3: OCP NIC 3.0 Form Factor Dimensions | 22 |
| Table 4: Baseboard to OCP NIC Form Factor Compatibility Chart | 22 |
| Table 5: Example Non-NIC Use Cases | 24 |
| Table 6: OCP NIC 3.0 Card Definitions..... | 27 |
| Table 7: OCP NIC 3.0 Line Side I/O Implementations..... | 35 |
| Table 8: Line Side I/O Cross Reference to Industry Standards | 35 |
| Table 9: Bill of Materials for the SFF and LFF Faceplate Assemblies..... | 39 |
| Table 10: CTF Default Tolerances (SFF, TSFF and LFF OCP NIC 3.0) | 62 |
| Table 11: MAC Address Label Example 1 – Quad Port with Single Host, Single Managed Controller..... | 77 76 |
| Table 12: MAC Address Label Example 2 – Octal Port with Single Host, Dual Managed Controller | 77 76 |
| Table 13: MAC Address Label Example 3 – Quad Port with Dual Hosts, Dual Managed Controller..... | 78 77 |
| Table 14: MAC Address Label Example 4 – Single Port with Quad Host, Single Managed Controller..... | 79 78 |
| Table 15: MAC Address Label Example 5 – Octal Port with Single Host, Octal Managed Controller | 79 78 |
| Table 16: NIC Implementation Examples and 3D CAD..... | 80 79 |
| Table 17: Contact Mating Positions for the Primary Connector | 83 82 |
| Table 18: Contact Mating Positions for the Secondary Connector | 85 84 |
| Table 19: Right Angle Connector Options..... | 87 86 |
| Table 20: Straddle Mount Connector Options | 88 87 |
| Table 21: Primary Connector Pin Definition (x16) (4C+) | 92 91 |
| Table 22: Secondary Connector Pin Definition (x16) (4C) | 94 93 |
| Table 23: Pin Descriptions – PCIe..... | 96 95 |
| Table 24: Pin Descriptions – PCIe Present and Bifurcation Control Pins..... | 102 101 |
| Table 25: Pin Descriptions – SMBus..... | 105 104 |
| Table 26: RBT_ISOLATE# Truth Table..... | 106 105 |
| Table 27: Pin Descriptions – NC-SI over RBT | 108 106 |
| Table 28: Pin Descriptions – Scan Chain | 115 113 |
| Table 29: Scan Chain Timing Requirements – Baseboard Side | 117 115 |
| Table 30: Scan Chain Timing Requirements – OCP NIC 3.0 Card Side | 117 115 |
| Table 31: Pin Descriptions – Scan Chain DATA_OUT Bit Definition..... | 118 116 |
| Table 32: Pin Descriptions – Scan Chain DATA_IN Bit Definition | 119 116 |
| Table 33: Pin Descriptions – Power..... | 124 122 |
| Table 34: Pin Descriptions – USB 2.0 – Primary Connector only..... | 129 127 |
| Table 35: Pin Descriptions – UART – Secondary Connector Only..... | 131 129 |
| Table 36: Pin Descriptions – RFU[1:4]..... | 132 130 |
| Table 37: PCIe Bifurcation Decoder for x32, x16, x8, x4, x2 and x1 Card Widths..... | 135 133 |
| Table 38: PCIe REFCLK and PERST Associations | 142 140 |
| Table 39: SFF, TSFF PCIe Link / REFCLKn / PERSTn mapping for 1, 2 and 4 Links | 142 140 |
| Table 40: LFF PCIe Link / REFCLKn / PERSTn mapping for 1, 2, 4 and 8 Links..... | 142 140 |
| Table 41: OCP NIC 3.0 Card LED Configuration with Two Physical LEDs per Port | 150 148 |
| Table 42: Available Card Functions per Power State | 155 153 |
| Table 43: Baseboard Power Supply Rail Requirements – Slot Power Envelopes | 158 155 |
| Table 44: Power Sequencing Parameters | 162 159 |
| Table 45: Digital I/O DC specifications | 164 161 |
| Table 46: Digital I/O AC specifications | 164 161 |
| Table 47: OCP NIC 3.0 Management Implementation Definitions..... | 165 162 |
| Table 48: Sideband Management Interface and Transport Requirements..... | 165 162 |
| Table 49: NC-SI Traffic Requirements | 166 163 |
| Table 50: MC MAC Address Provisioning Requirements | 166 163 |
| Table 51: Threshold Severity Level vs Example Threshold Values | 169 166 |
| Table 52: Temperature Reporting Requirements | 170 167 |
| Table 53: Power Consumption Reporting Requirements..... | 171 168 |
| Table 54: Pluggable Module Status Reporting Requirements | 172 169 |
| Table 55: Management and Pre-OS Firmware Inventory and Update Requirements | 172 169 |
| Table 56: Slot_ID[1:0] to Package ID[2:0] Mapping | 174 171 |
| Table 57: FRU EEPROM Address Map | 175 172 |

Open Compute Project • OCP NIC 3.0
Version ~~1.2.1 - DRAFT~~ 2.0

| | |
|---|--------------------|
| Table 58: FRU EEPROM Record – OEM Record 0xC0, Offset 0x00..... | 178 175 |
| Table 59: NC-SI over RBT Timing Parameters | 185 182 |
| Table 60: PCIe Electrical Budgets | 189 186 |
| Table 61: PCIe Test Fixtures for OCP NIC 3.0 | 190 187 |
| Table 62: Hot Aisle Air Temperature Boundary Conditions | 195 192 |
| Table 63: Hot Aisle Airflow Boundary Conditions | 195 192 |
| Table 64: Cold Aisle Air Temperature Boundary Conditions..... | 195 192 |
| Table 65: Cold Aisle Airflow Boundary Conditions..... | 196 193 |
| Table 66: Reference OCP NIC 3.0 SFF Card Geometry | 197 194 |
| Table 67: Reference OCP NIC 3.0 LFF Card Geometry | 201 198 |
| Table 68: Card Cooling Tier Definitions (LFM)..... | 215 212 |
| Table 69: Random Vibration Testing 1.88 G _{RMS} Profile | 219 216 |
| Table 70: FCC Class A Radiated and Conducted Emissions Requirements Based on Geographical Location..... | 223 220 |
| Table 71: Safety Requirements | 224 221 |
| Table 72: Immunity (ESD) Requirements | 224 221 |

1 Overview

1.1 License

As of January 23rd, 2018, the following persons or entities have made this Specification available under the Open Compute Project Hardware License (Permissive) Version 1.0 (OCPHL-P)

- OCP NIC Subgroup

An electronic copy of the OCPHL-P is available at:

<https://www.opencompute.org/documents/ocphl-permissive-v10>

Your use of this Specification may be subject to other third-party rights. THIS SPECIFICATION IS PROVIDED "AS IS." The contributors expressly disclaim any warranties (express, implied, or otherwise), including implied warranties of merchantability, non-infringement, fitness for a particular purpose, or title, related to the Specification. The Specification implementer and user assume the entire risk as to implementing or otherwise using the Specification. IN NO EVENT WILL ANY PARTY BE LIABLE TO ANY OTHER PARTY FOR LOST PROFITS OR ANY FORM OF INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES OF ANY CHARACTER FROM ANY CAUSES OF ACTION OF ANY KIND WITH RESPECT TO THIS SPECIFICATION OR ITS GOVERNING AGREEMENT, WHETHER BASED ON BREACH OF CONTRACT, TORT (INCLUDING NEGLIGENCE), OR OTHERWISE, AND WHETHER OR NOT THE OTHER PARTY HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

1.2 Acknowledgements

The OCP NIC 3.0 specification was created under a collaboration from many OCP member companies and facilitated by the OCP NIC Subgroup under the OCP Server Workgroup.

The OCP NIC Subgroup would like to acknowledge the following member companies for their current contributions to the OCP NIC 3.0 specification:

Table 1: Acknowledgements – Current Contributors – By Company

| | |
|------------------------------------|--|
| Amphenol Corporation | Marvell Semiconductor, Inc. |
| Broadcom Inc. | Molex LLC |
| Dell, Inc. | Netronome Systems, Inc. |
| Facebook, Inc. | NVIDIA Corporation |
| Hewlett Packard Enterprise Company | Quanta Computer Inc. |
| Intel Corporation | TE Connectivity Corporation |
| Keysight Technologies | University of New Hampshire InterOperability Lab |
| Lenovo Group Ltd | |

1.3 References

- DMTF Standard. *DSP0222, Network Controller Sideband Interface (NC-SI) Specification*. Distributed Management Task Force (DMTF), Rev 1.1.0, September 23rd, 2015.
- DMTF Standard. *DSP0222, Network Controller Sideband Interface (NC-SI) Specification*. Distributed Management Task Force (DMTF), Rev 1.2.0, Work-In-Progress.
- DMTF Standard. *DSP0236, Management Component Transport Protocol (MCTP) Base Specification*. Distributed Management Task Force (DMTF), Rev 1.3.0, November 24th, 2016.
- DMTF Standard. *DSP0237, Management Component Transport Protocol (MCTP) SMBus/I2C Transport Binding Specification*. Distributed Management Task Force (DMTF), Rev 1.1.0, May 21st, 2017.
- DMTF Standard. *DSP0238, Management Component Transport Protocol (MCTP) PCIe VDM Transport Binding Specification*. Distributed Management Task Force (DMTF), Rev 1.0.2, December 7th, 2014.
- DMTF Standard. *DSP0239, MCTP IDs and Codes Specification*. Distributed Management Task Force (DMTF), Rev 1.5.0, December 17th, 2017.
- DMTF Standard. *DSP0240, Platform Level Data Model (PLDM) Base Specification*. Distributed Management Task Force (DMTF), Rev 1.0.0, April 23rd, 2009.
- DMTF Standard. *DSP0240, Platform Level Data Model (PLDM) over MCTP Binding Specification*. Distributed Management Task Force (DMTF), Rev 1.0.0, April 23rd, 2009.
- DMTF Standard. *DSP0245, Platform Level Data Model (PLDM) IDs and Codes Specification*. Distributed Management Task Force (DMTF), Rev 1.2.0, November 24th, 2016.
- DMTF Standard. *DSP0248, Platform Level Data Model (PLDM) for Platform Monitoring and Control Specification*. Distributed Management Task Force (DMTF), Rev 1.1.1, January 10th, 2017.
- DMTF Standard. *DSP0249, Platform Level Data Model (PLDM) State Sets Specification*. Distributed Management Task Force (DMTF), Rev 1.0.0, March 16th, 2009.
- DMTF Standard. *DSP0261, NC-SI over MCTP Binding Specification*. Distributed Management Task Force (DMTF), Rev 1.2.0, August 26th, 2017.
- DMTF Standard. *DSP0267, Platform Level Data Model (PLDM) for Firmware Update Specification*. Distributed Management Task Force (DMTF), Rev 1.0.1, March 28th, 2018.
- DMTF Standard. *DSP0254, PLDM NIC Modeling*. Distributed Management Task Force (DMTF), Rev 1.0.0, December 18th, 2019.
- EDSFF. *Enterprise and Datacenter SSD Form Factor Connector Specification*. Enterprise and Datacenter SSD Form Factor Working Group, Rev 0.9 (draft), August 2nd 2017.
- IPC. *IPC-TM-650 Test Methods Manual number 2.4.53. Dye and Pull Test Method (Formerly Known as Dye and Pry)*, Association Connecting Electronics Industries, August 2017.
- IPMI Platform Management FRU Information Storage Definition, v1.0 Document Revision 1.3, March 24th, 2015.
- National Institute of Standards and Technology (NIST). *Special Publication 800-193, Platform Firmware Resiliency Guidelines*, May 2018.
- NXP Semiconductors. *I²C-bus specification and user manual*. NXP Semiconductors, Rev 6, April 4th, 2014.

- Open Compute Project. *OCP NIC Subgroup*. Online. <http://www.opencompute.org/wiki/Server/Mezz>
- PCI-SIG®. *PCI Express® Base Specification*, Revision 3.0 December 7th, 2015.
- PCI-SIG®. *PCI Express® Base Specification*, Revision 4.0 Version 1.0, October 5th, 2017.
- PCI-SIG®. *PCI Express® Card Electromechanical Specification*, Revision 3.0, July 21st, 2013.
- PCI-SIG®. *PCI Express® Card Electromechanical Specification*, Revision 4.0 (draft).
- SMBus Management Interface Forum. *System Management Bus (SMBus) Specification*. System Management Interface Forum, Inc, Version 2.0, August 3rd, 2000.
- SNIA. SFF-TA-1002, Specification for Protocol Agnostic Multi-Lane High Speed Connector. SNIA SFF TWG Technology Affiliate, Rev 1.2, April 3rd, 2019.
- UEFI Specification Version 2.5, <http://www.uefi.org/sites/default/files/resources/UEFI%202.5.pdf>, April 2015.
- USB Implementers Forum. *Universal Serial Bus Specification*, Revision 2.0, April 27th, 2000.

1.3.1 Trademarks

Names and brands may be claimed as trademarks by their respective companies.

I²C® is a trademark of NXP Semiconductor.

PCIe® and PCI Express® are the registered trademarks of PCI-SIG.

1.4 Acronyms

For the purposes of the OCP NIC 3.0 specification, the following acronyms apply:

Table 2: Acronyms

| Acronym | Definition |
|---------|---|
| AIC | Add-in Card |
| ASIC | Application Specific Integrated Circuit |
| BGA | Ball Grid Array |
| BMC | Baseboard Management Controller |
| BOM | Bill of Materials |
| CAD | Computer Aided Design |
| CBB | Compliance Base Board |
| CEM | Card Electromechanical |
| CFD | Computational Fluid Dynamics |
| CFM | Cubic Feet per Minute |
| CLB | Compliance Load Board |
| CTD | Chain of Trust for Detection |
| CTF | Critical to Function |
| CTU | Chain of Trust for Update |
| DMTF | Distributed Management Task Force |
| DRAM | Dynamic Random Access Memory |
| EDSFF | Enterprise and Datacenter SSD Form Factor |
| EMI | Electro Magnetic Interference |
| ESD | Electrostatic Discharge |
| EU | European Union |
| FCC | Federal Communications Commission |
| FRU | Field Replaceable Unit |
| I/O | Input / Output |
| I2C | Inter-Integrated Circuit - two wire serial protocol |
| IEC | International Electrotechnical Commission |
| IPC | Institute for Printed Circuits |
| IPMI | Intelligent Platform Management Interface |
| ISO | International Organization for Standardization |
| LED | Light Emitting Diode |
| LFF | Large Form Factor |
| LFM | Linear Feet per Minute |
| MAC | Media Access Control |
| MC | Management Controller |
| MCTP | Management Component Transport Protocol |
| ME | Management Entity |
| MSA | Multi-source Agreement |
| NC | No Connect |
| NC-SI | Network Controller Sideband Interface |
| NEBS | Network Equipment Building-System |
| NIC | Network Interface Card |
| OCP | Open Compute Project |

| Acronym | Definition |
|----------|--|
| ODM | Original Design Manufacturer |
| OEM | Original Equipment Manufacturer |
| OSFP-RHS | Octal Small Form Factor Pluggable Riding Heat Sink |
| PBA | Printed Board Assembly |
| PCB | Printed Circuit Board |
| PCI™ | Peripheral Component Interconnect |
| PCIe® | PCI Express® |
| PDR | Platform Descriptor Record |
| PLDM | Platform Level Data Model |
| QSFP | Quad Small Form Factor Pluggable |
| QSFP-DD | Quad Small Form Factor Pluggable Double Density |
| QZ | Quiet Zone |
| RA | Right Angle |
| RBT | RMII Based Transport |
| REACH | Registration, Evaluation, Authorization and Restriction of Chemicals |
| RFU | Reserved Future Use |
| RJ45 | Registered Jack 45 (IEC 60603-7 8P8C connector) |
| RoHS | Restriction of Hazardous Substances Directive |
| RSVD | Reserved |
| RTU | Root of Trust for Update |
| SFF | Small Form Factor |
| SFP | Small Form Factor Pluggable |
| SMBus | System Management Bus |
| SMT | Surface Mount Technology |
| TBD | To be Determined |
| TDP | Thermal Design Power |
| TSFF | Tall Small Form Factor |
| UART | Universal Asynchronous Receiver-Transmitter |
| UDID | Unique Device Identifier for each SMBus device. Refer to the SMBus 2.0 specification for the field definition. |
| UEFI | Unified Extensible Firmware Interface |
| USB | Universal Serial Bus |
| VDM | Vendor Defined Messages |
| WEEE | Waste Electrical and Electronic Equipment |

1.5 Conventions

The OCP NIC 3.0 specification adopts the following convention for numerical representations:

- Hexadecimal numbers are written with a 0x prefix with the most significant byte first – such as 0xFFFF
- Binary numbers are written with a 0b prefix with the most significant bit first – such as 0b0101
- Decimal numbers are indicated without any prefix (such as 25)

The unit representations are implemented per the Bureau International des Poids et Mesures (BIPM). The value and unit are separated by a space. The SI symbol and appropriate SI prefix are used (such as 50 °C, 15 A and 200 kΩ).

1.6 Background

The OCP NIC 3.0 specification is a follow-on to the OCP Mezz 2.0 rev 1.00 design specification. The OCP NIC 3.0 specification supports three basic card sizes: Small Form Factor (SFF), Tall Small Form Factor (TSFF) and Large Form Factor (LFF). The SFF and TSFF allows for up to 16 PCIe® lanes on the card edge while the LFF supports up to 32 PCIe lanes. The SFF and TSFF share the same board footprint. The TSFF has a taller faceplate to accommodate a taller heatsink and board level components. Compared to the OCP Mezz Card 2.0 Design Specification, the updated OCP NIC 3.0 specification provides a broader solution space for the NIC and system vendors to support the following use case scenarios:

- NICs with a higher Thermal Design Power (TDP)
- Power delivery supports up to 80 W to a single connector (SFF, TSFF) card, and up to 150 W to a dual connector (LFF) card
 - Note: Baseboard vendors need to evaluate if there is sufficient airflow to thermally cool the OCP NIC 3.0 card. Refer to Section 6 for additional details.
- Supports up to PCIe Gen 4 (16 GT/s) on the baseboard and OCP NIC 3.0 card
 - Connector is electrically compatible with PCIe Gen 5 (32 GT/s)
- Support for up to 32 lanes of PCIe per OCP NIC 3.0 card
- Support for single host, multi-root complex, and multi-host environments
- Supports a greater board area for more complex OCP NIC 3.0 card designs
- Support for Smart NIC implementations with on-board DRAM and accelerators
- Simplification of FRU installation and removal while reducing overall down time

A representative SFF OCP NIC 3.0 card is shown in Figure 1. A representative TSFF is shown in Figure 2 and a LFF is shown in Figure 3.

Figure 1: Representative SFF OCP NIC 3.0 Card with Dual QSFP Ports

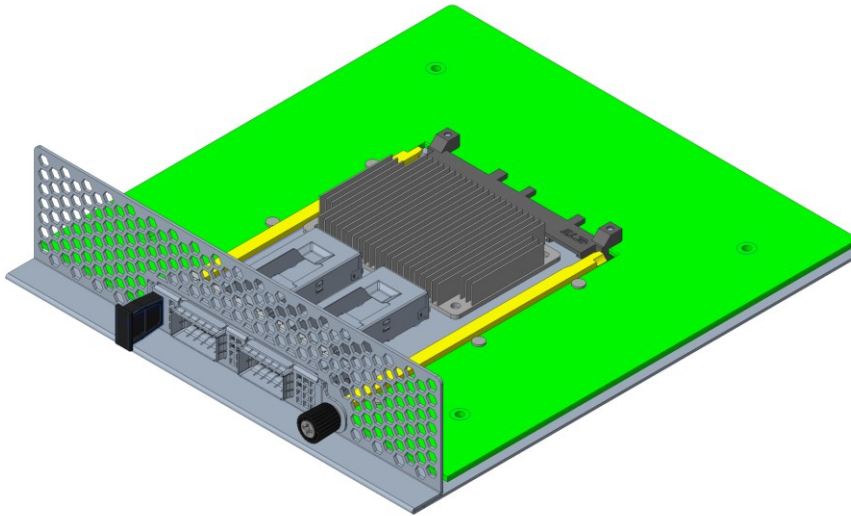


Figure 2: Representative TSFF OCP NIC 3.0 Card with Dual QSFP Ports

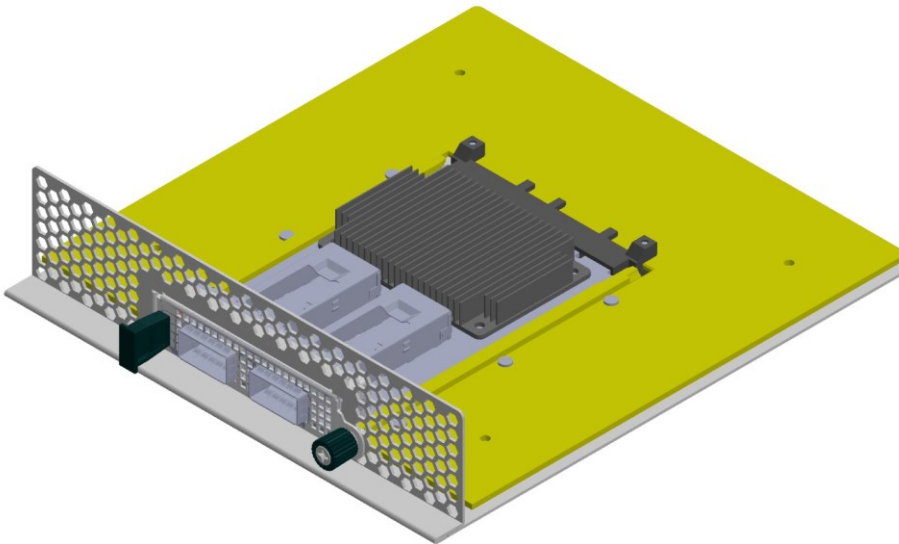
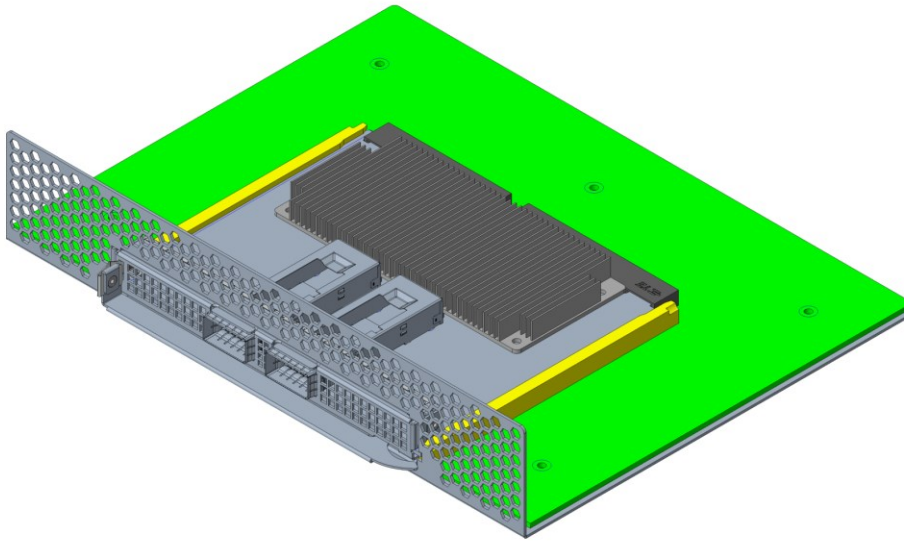


Figure 3: Representative LFF OCP NIC 3.0 Card with Dual QSFP Ports and on-board DRAM



In order to achieve the features outlined in this specification, OCP NIC 3.0 compliant cards are not backwards compatible with OCP Mezz 2.0 cards.

This specification is created under OCP Server workgroup – OCP NIC subgroup. An electronic copy of this specification can be found on the Open Compute Project and the OCP Marketplace websites:

http://www.opencompute.org/wiki/Server/Mezz#Specifications_and_Designs

<https://www.opencompute.org/contributions?query=OCP%20NIC%203.0>

1.7 Overview

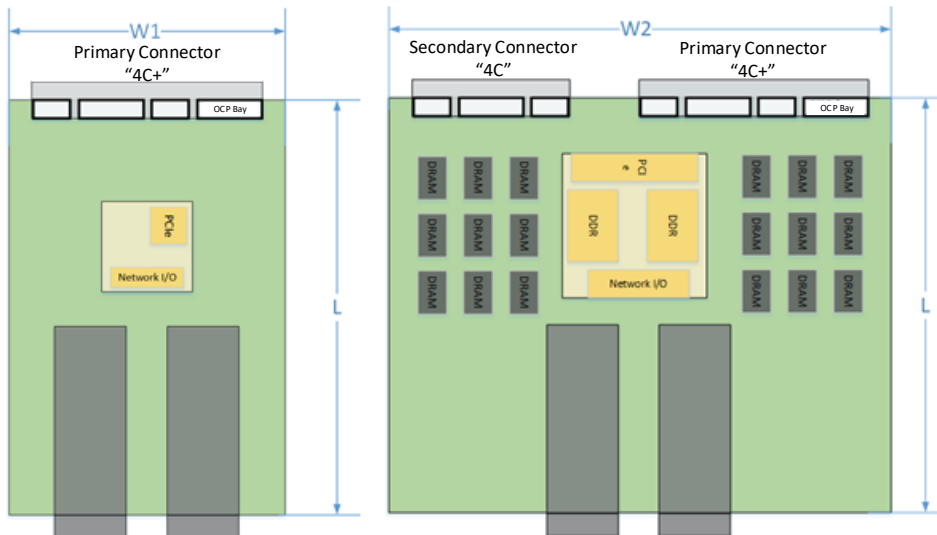
1.7.1 Mechanical Form Factor Overview

The OCP NIC 3.0 specification defines a ~~third-generation~~ **third-generation** mechanical form factor that allows for interoperability between compliant baseboards and OCP NIC 3.0 cards.

OCP NIC 3.0 cards have three form factors – SFF, TSFF and LFF. These cards are shown in Figure 4 below. The components shown in the figures are for illustrative purposes. The SFF and TSFF uses one connector (Primary Connector) on the baseboard. The LFF uses one or two connectors (Primary Connector only or both the Primary and Secondary Connectors) on the baseboard.

Both the Primary and Secondary Connectors and card edge gold fingers are defined in and compliant to SFF-TA-1002. The Primary Connector is the “4C+” variant, the Secondary Connector is the “4C” version. On the OCP NIC 3.0 card side, the card edge is implemented with gold fingers. The SFF and TSFF gold finger area only occupies the Primary Connector area for up to 16 PCIe lanes. The LFF gold finger area may occupy both the Primary and Secondary Connectors for up to 32 PCIe lanes, or optionally just the Primary Connector for up to 16 PCIe lane implementations.

Figure 4: SFF/TSFF and LFF Block Diagrams (not to scale)



The two form factor dimensions are shown in Table 3.

Table 3: OCP NIC 3.0 Form Factor Dimensions

| Form Factor | Width | Depth | Max Z-height | Primary Connector | Secondary Connector | Typical Use Case |
|-------------|-------------|--------|--------------|-------------------|---------------------|---|
| SFF | 76 mm (W1) | 115 mm | 11.50 mm | “4C+” 168 pins | N/A | Low profile and NIC with a similar profile as an OCP NIC 2.0 card; up to 16 PCIe lanes. |
| TSFF | 76 mm (W1) | 115 mm | 14.20 mm | “4C+” 168 pins | N/A | Higher thermal dissipation compared to SFF cards with the additional Z-height. |
| LFF | 139 mm (W2) | 115 mm | 11.50 mm | “4C+” 168 pins | “4C” 140 pins | Larger PCB width to support additional NICs; up to 32 PCIe lanes. |

The OCP NIC 3.0 design allows downward compatibility between the three card sizes. Table 4 shows the compatibility between the baseboard and NIC combinations. A SFF baseboard slot may only accept a SFF sized NIC. A LFF baseboard slot may mechanically accept a SFF or LFF NIC using a guide rail adapter, and a TSFF baseboard slot may mechanically accept a TSFF or SFF NIC, however, these combinations are outside the scope of the specification.

Table 4: Baseboard to OCP NIC Form Factor Compatibility Chart

| Baseboard Slot Size | NIC Size / Supported PCIe Width | |
|---------------------|---------------------------------|---------------------|
| | SFF | LFF |
| SFF | Up to 16 PCIe lanes | Not Supported |
| TSFF | Up to 16 PCIe lanes | Not Supported |
| LFF | Up to 16 PCIe lanes | Up to 32 PCIe lanes |

There are two baseboard connector mounting options available for system designers: straddle mount and right angle (RA). The straddle mount connector option allows the OCP NIC and baseboard to exist in a co-planer position. To achieve this, a cutout exists on the baseboard and is defined in this specification. Alternatively, the right angle option allows the OCP NIC to be installed on top of the baseboard. A baseboard cutout is not required for the right angle connector. The right angle option allows the baseboard to use this area for additional routing or backside component placement. The straddle mount and right angle connectors are shown in Section 3.2.

For both the baseboard and OCP NIC 3.0 card, this specification defines the component and routing keep out areas. Refer to Section 2.5 for details.

Both the straddle mount and right angle implementations shall accept the same OCP NIC 3.0 card and shall be supported in the baseboard chassis regardless of the baseboard connector selection (right angle or straddle mount) so long as the baseboard slot and OCP NIC 3.0 card sizes are a supported combination as shown in Table 4.

This specification defines the form factor at the OCP NIC 3.0 card level for the SFF, TSFF and LFF, including the front panel, latching mechanism and card guide features.

More details about the card form factor is shown in Section 2.

1.7.2 Electrical Overview

This specification defines the electrical interface between baseboard and the OCP NIC 3.0 card. The electrical interface is implemented with a right angle or straddle mount connector on baseboard and gold finger on the OCP NIC 3.0 card. As previously noted in the mechanical overview, each card may implement a Primary Connector or Primary + Secondary Connector. Cards using only the Primary Connector are suitable for SFF, TSFF and LFF and may support up to 16 lanes of PCIe. The Secondary Connector, when used in conjunction with the Primary Connector, allows LFF implementations and may support up to 32 lanes of PCIe.

1.7.2.1 Primary Connector

The Primary Connector provides all OCP specific management functions as well as up to 16 lanes of PCIe between the OCP NIC and the system motherboard. The Primary Connector is a 4C+ as defined in SFF-TA-1002 and consists of an OCP Bay for management and sideband signals, and a 4C region.

Management Function Overview (OCP Bay):

- DMTF DSP0222 compliant Network Controller Sideband Interface (NC-SI) RMII Based Transport (RBT) Physical Interface
- Power management and status reporting
 - Power Brake for emergency power reduction
 - State change control
- Control / status serial bus
 - NIC-to-Host status
 - Port LED Link/Activity
 - Environmental Indicators
 - Host-to-NIC configuration Information
- Multi-host PCIe support signals (2x PCIe resets, 2x reference clocks)
 - The OCP bay provides PERST2#, PERST3#, REFCLK2 and REFCLK3. This enables support for up to four hosts when used in conjunction with PERST0#, PERST1#, REFCLK0 and REFCLK1 in the Primary 4C region.
- PCIe Wake signal

See Section 3.4 for a complete list of pin and function descriptions for the OCP Bay portion of the Primary Connector. The OCP Bay pins are prefixed with “OCP_” in the pin location column.

Interface Overview (4C region):

- 16x differential transmit/receive pairs
 - Up to PCIe Gen 5 (32 GT/s) support
- 2x 100 MHz differential reference clocks
- Control signals
 - 2x PCIe Resets
 - Link Bifurcation Control
 - Card power disable/enable

- SMBus 2.0
- USB 2.0 interface
- Power
 - +12V_EDGE
 - +3.3V_EDGE
 - Power distribution between the aux and main power domains is up to the baseboard vendor

See Section 3.4 for a complete list of pin and function descriptions for the 4C+ connector.

1.7.2.2 Secondary Connector

The Secondary Connector provides an additional 16 lanes of PCIe and their respective control signals. The Secondary Connector is a 4C as defined in SFF-TA-1002.

Interface Overview (4C Connector):

- 16x differential transmit/receive pairs
 - Up to PCIe Gen 5 (32 GT/s) support
- 2x 100 MHz differential reference clocks
- Control signals
 - 2x PCIe Resets
 - Link Bifurcation Control
 - Card power disable/enable
- SMBus 2.0
- UART (transmit and receive)
- Power
 - +12V_EDGE
 - +3.3V_EDGE
 - Power distribution between the aux and main power domains is up to the baseboard vendor

See Section 3.4 for a complete list of pin and function descriptions for the 4C connector.

1.8 Non-NIC Use Cases

The OCP NIC 3.0 specification is mainly targeted for Network Interface Card applications. It is possible to use the same OCP NIC 3.0 card form factor, baseboard interface and mechanical design to enable non-NIC use cases. These non-NIC use cases use the same baseboard/OCP NIC 3.0 card interface as defined in Section 3. The non-NIC use cases are not covered in the current revision of the OCP NIC 3.0 specification. Example non-NIC use cases implement various external I/O interfaces and are shown in Table 5.

Table 5: Example Non-NIC Use Cases

| Example Use Case | Card External I/O Interface(s) |
|-------------------------|---|
| PCIe Retimer Card | PCIe |
| Accelerator Card | N/A |
| NVMe Card | N/A |
| Storage HBA / RAID Card | I/O Interface to be determined in future specification release. |

2 Mechanical Card Form Factor

2.1 Form Factor Options

OCP NIC 3.0 provides three fundamental form factor options: SFF (76 mm x 115 mm x 11.50 mm), TSFF (76 mm x 115 mm x 14.20 mm) and LFF (139 mm x 115 mm x 11.50 mm).

These form factors support a Primary Connector and optionally, a Secondary Connector. The Primary Connector is defined to be a SFF-TA-1002 compliant 4C+ connector. The 4C+ connector is a 4C compliant implementation plus a 28-pin “OCP bay” for OCP NIC 3.0 specific pins. The Secondary Connector is the 4C connector as defined in SFF-TA-1002. The 4C specification supports up to 32 differential pairs for a x16 PCIe connection per connector. For host platforms, the 28-pin OCP bay is required for all Primary Connector implementations.

The SFF uses the Primary 4C+ connector to provide up to a x16 PCIe interface to the host. The additional 28-pin OCP bay carries sideband management interfaces as well as OCP NIC 3.0 specific control signals for multi-host PCIe support. The SFF card provides sufficient faceplate area to accommodate up to 2x QSFP modules, 4x SFP modules, or 4x RJ45 for BASE-T operation. The SFF and TSFF supports up to 80 W of delivered power to the card edge. Actual cooling capacity for a SFF and TSFF card is dependent on the ambient conditions over the NIC. An example SFF is shown in Figure 1. An Example TSFF is shown in Figure 2.

The LFF uses the Primary 4C+ connector to provide the same functionality as the SFF along with an additional Secondary 4C connector to provide up to a x32 PCIe interface. The LFF Card may utilize both the Primary and Secondary Connectors, or just the Primary Connector for lower PCIe lane count applications. Table 6 summarizes the LFF permutations. The LFF supports higher power envelopes and provides additional board area for more complex designs. The LFF supports up to 150 W of delivered power to the card edge across the two connectors. Actual cooling capacity for the LFF is dependent on the ambient conditions over the NIC. An example LFF is shown in Figure 3.

For LFF Cards, implementations may use both the Primary and Secondary Connector (as shown in Figure 5), or may use the Primary Connector only (as shown in Figure 6) for the card edge gold fingers.

Figure 5: Primary Connector (4C+) and Secondary Connector (4C) (LFF) OCP NIC 3.0 Cards

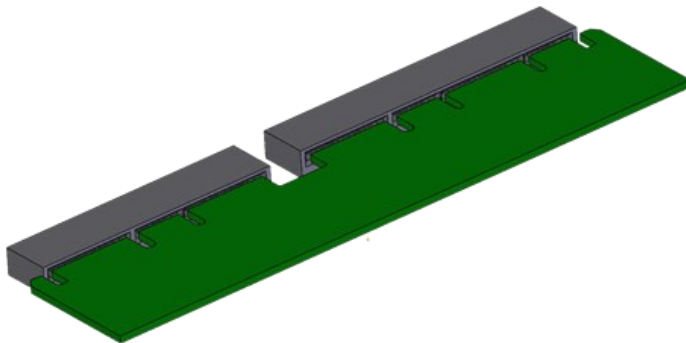
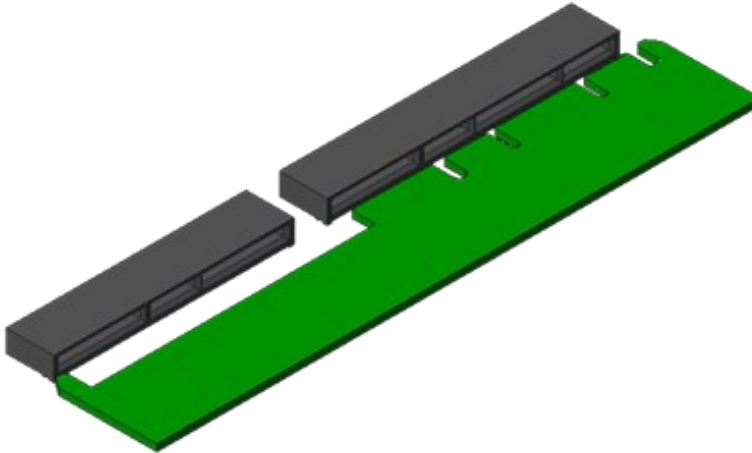


Figure 6: Primary Connector (4C+) Only (LFF) OCP NIC 3.0 Cards



For both form factors, an OCP NIC 3.0 card may optionally implement a subset of pins to support less than a x16 PCIe connection. This may be implemented using a 2C+ card edge per SFF-TA-1002. The baseboard Primary Connector shall use a 4C+ in all cases. Figure 7 illustrates the supported 4C+ and 2C+ card edge configurations on a 4C+ Primary Connector.

Figure 7: Primary Connector (4C+) with 4C and 2C (SFF) OCP NIC 3.0 Cards

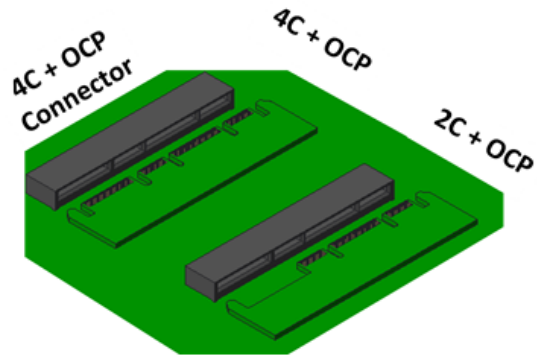


Table 6 summarizes the supported card form factors. SFF and TSFF cards support the Primary Connector and up to 16 PCIe lanes. LFF cards support implementations with both the Primary and Secondary Connectors and up to 32 PCIe lanes, or a Primary Connector only implementation with up to 16 PCIe lanes.

Table 6: OCP NIC 3.0 Card Definitions

| OCP NIC 3.0 Card Size and PCIe Lane Count | Baseboard Secondary Connector (4C) | Baseboard Primary Connector (4C+) | |
|---|------------------------------------|-----------------------------------|---------|
| | x16 PCIe | x16 PCIe | OCF Bay |
| SFF, TSFF (x8) | Not used with SFF 2C+ Card Edge | x8 (Lanes 7:0) PCIe | OCF Bay |
| SFF, TSFF (x16) | Not used with SFF 4C+ Card Edge | x16 (Lanes 15:0) PCIe | OCF Bay |
| LFF (x8) | Not used with LFF 2C+ Card Edge | x8 (Lanes 7:0) PCIe | OCF Bay |
| LFF (x16) | Not used with LFF 4C+ Card Edge | x16 (Lanes 15:0) PCIe | OCF Bay |
| LFF (x32) | x16 (Lanes 31:16) PCIe | x16 (Lanes 15:0) PCIe | OCF Bay |

All mechanical board assemblies shall meet the safety requirements described in Section 7.1.3.

2.1.1 SFF and TSFF Faceplate Configurations

The SFF and TSFF configuration views are shown below. Three different faceplates are each available for the SFF and TSFF – pull tab, ejector latch and internal lock. The same SFF and TSFF OCP NIC 3.0 PBA accepts up to six faceplate types depending on the end application. Faceplates are attached to the PCBA at the time of manufacture. A TSFF faceplate may be used on a SFF PBA. The drawings shown in Figure 8 below illustrates representative ~~¾~~-three-quarter views of the SFF only, front, side and top views of SFF and TSFF implementations.

Note: The TSFF implementation uses the same PCB outline as SFF. The faceplate and top-side Z-height envelope grows to 14.20 mm. Additional I/O connector options are available with the TSFF.

Where space is permitted on the faceplate, square vents sized to a maximum of 3.0 mm x 3.0 mm may be added to help optimize airflow while maintaining the integrity of the faceplate structure. EMI mitigation should also be considered during the design process. Refer to the images shown in Figure 9 for example square vent configurations depending on the line side I/O connectors.

Depending on the OCP NIC 3.0 card implementation, I/O connectors may be placed anywhere within the allowable connector keep in regions as defined by the SFF and TSFF PBA mechanical drawings and faceplate drawings of Section 2.5.1 and Section 2.5.2.

The OCP NIC 3.0 outline provides an optional feature to lock the card into the chassis. This is accomplished with two notches – one on each side of the card guide rail. A baseboard may choose to use one or both notches for the internal locking mechanism. The OCP NIC 3.0 outline provides a notch location on both guide rails to provide flexible configurations to baseboard vendors. If a locking feature is implemented on the baseboard, the OCP NIC 3.0 card may only be inserted or removed after actuating the internal locking mechanism. The PCB retention notches are compatible with all chassis implementations. Please refer to the SFF dimensions in Section 2.5.1 for details. The internal locking mechanism is not available on LFF cards.

Note: The OCP NIC 3.0 card supplier may add port identification on the faceplate assembly that meet their manufacturing and customer requirements.

All of the OCP NIC 3.0 CAD files are available for download and use on the OCP NIC 3.0 Wiki site:
<http://www.opencompute.org/wiki/Server/Mezz>

Figure 8: SFF/TSFF NIC Configuration Views

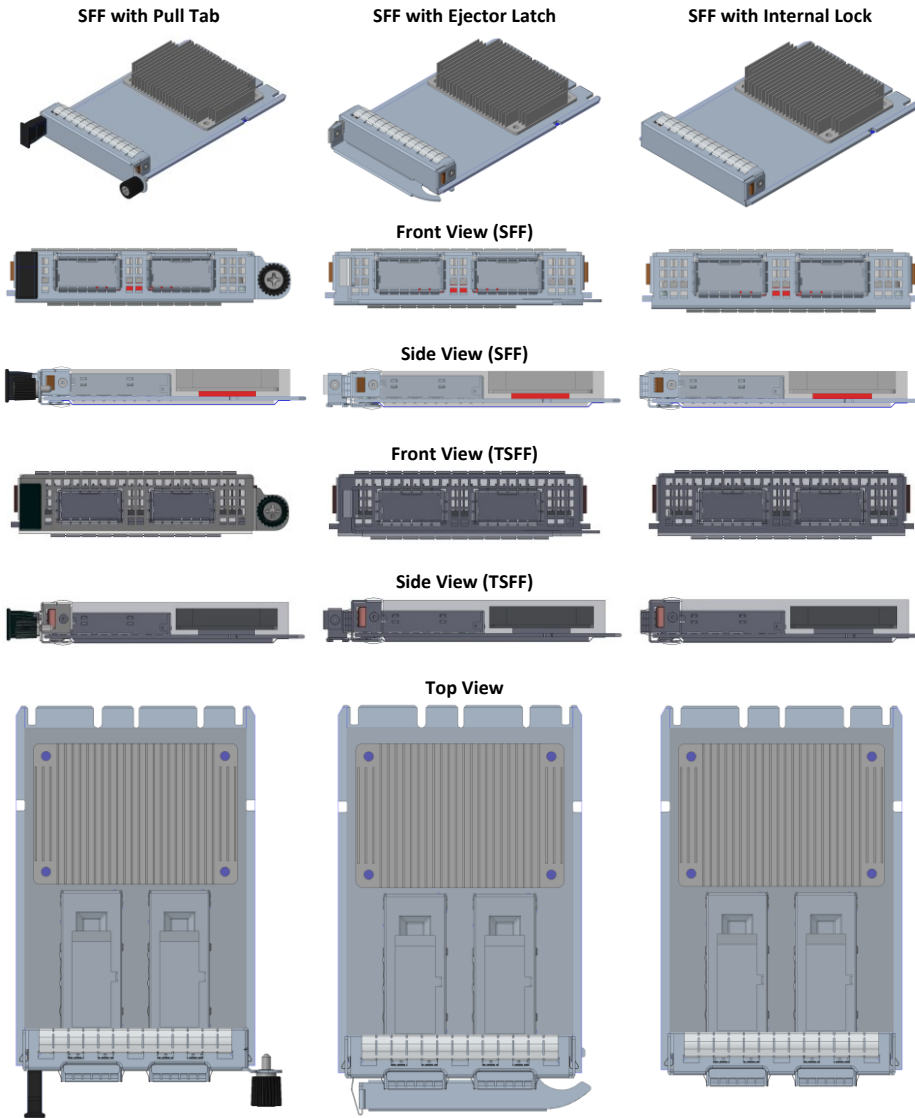


Figure 9 illustrates example SFF 3D views for the supported line side I/O implementations. The line side I/O implementations are discussed in Section 2.2. TSFF implementations are similar but have a taller faceplate.

Figure 9: SFF NIC Line Side 3D Views

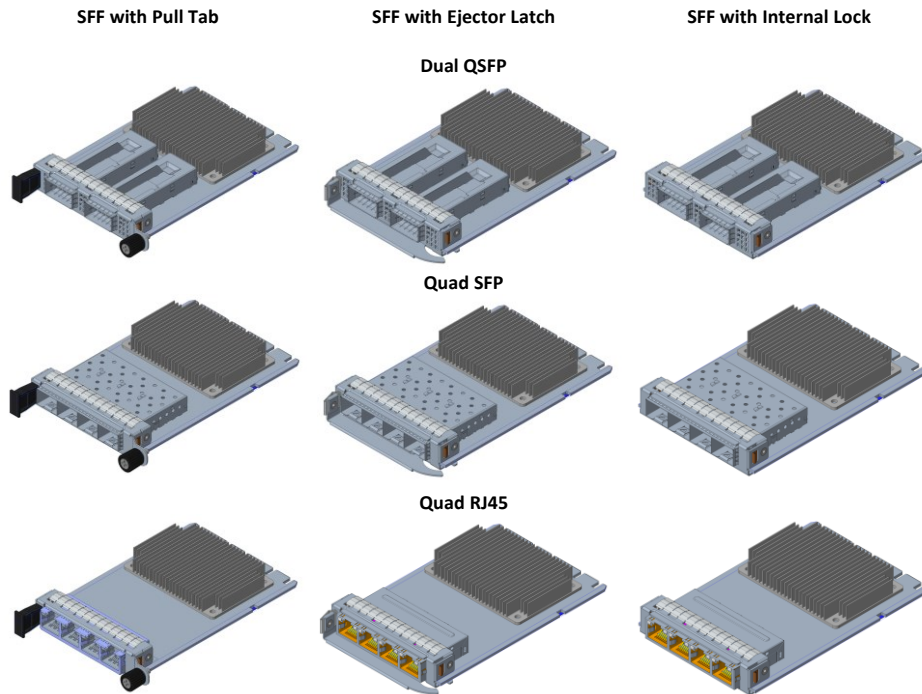


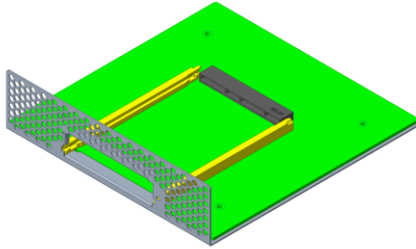
Figure 10 illustrates example SFF 3D views of the pull tab and ejector latch assemblies mounted in a chassis utilizing a straddle mount connector and a right-angle connector. The baseboard connector options are discussed in Section 3.2. The SFF OCP NIC 3.0 card is identical for both chassis connector options.

The OCP NIC 3.0 card provides a notch on each side of the card rail edge. This feature is used in conjunction with a baseboard's internal locking mechanism to prevent card insertion and removal. The internal locking mechanism is a baseboard vendor's optional feature and is not shown in the views below.

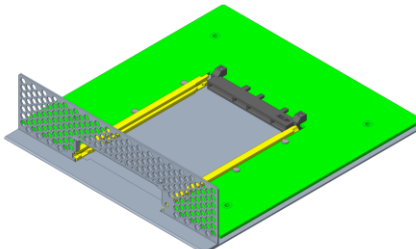
On the internal lock variation only, a 5.4 kg force with a 1 second ramp may be applied to the heatsink during NIC ejection. The mechanical and thermal solution shall be implemented such that the thermal performance is maintained for 10 force cycles (i.e., the NIC still passes all functional tests). If there exists a minimum of (10 mm x 10 mm x 10 mm) of space behind the line side connectors, then each connector shall be able to sustain the same 5.4 kg force with a 1 second ramp.

Figure 10: SFF NIC Chassis Mounted 3D Views

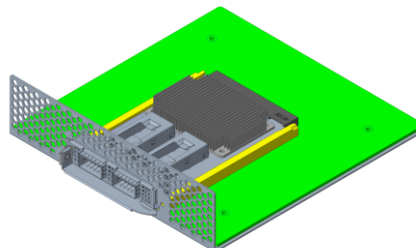
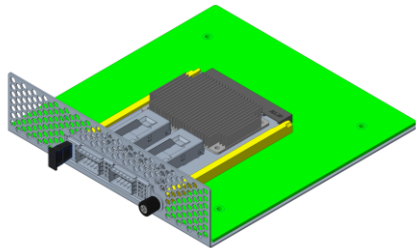
SFF with Pull Tab



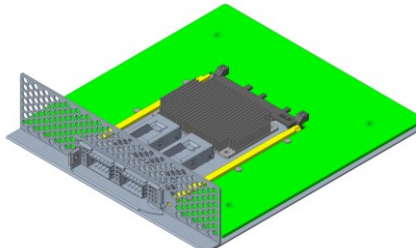
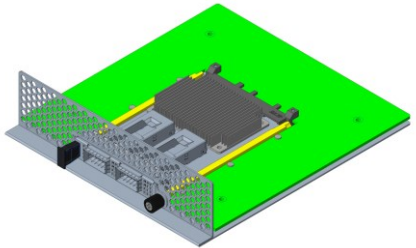
SFF with Ejector Latch



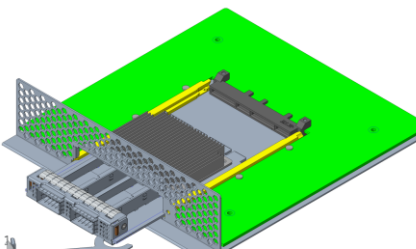
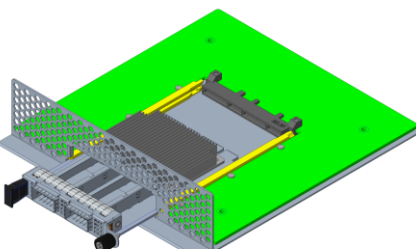
Right Angle vs Straddle Mount Chassis Configuration



Right Angle Baseboard Connector



Straddle Mount Baseboard Connector



NIC Insertion / Removal (Shown with a Straddle Mount Connector)

2.1.2 LFF Faceplate Configurations

The LFF configuration views are shown below. A single faceplate implementation is available for the LFF – with a single ejector latch. The long ejector is the default configuration, however, a short ejector version is available for non-shadowed front I/O configurations and is being considered for future development. Like the SFF and TSFF, if additional LFF faceplate implementations become available, the same LFF OCP NIC 3.0 PBA accepts up to three faceplate types depending on the end application. Faceplates are attached to the PCBA at the time of manufacture. The drawings shown in Figure 11 below illustrate a representative front, side and top views of the LFF.

Where space is permitted on the faceplate, square vents sized to a maximum of 3.0 mm x 3.0 mm may be added to help optimize airflow while maintaining the integrity of the faceplate structure. EMI considerations should also be considered during the design process. Refer to the images shown in Figure 12 for example square vent configurations depending on the line side I/O connectors.

Depending on the OCP NIC 3.0 card implementation, I/O connectors may be placed anywhere within the allowable connector keep in regions as defined by the PBA mechanical drawings and faceplate drawings of Section 2.5

Note: The OCP NIC 3.0 card supplier shall add port identification on the faceplate assembly that meet their manufacturing and customer requirements.

All of the OCP NIC 3.0 CAD files are available for download and use on the OCP NIC 3.0 Wiki site:
<http://www.opencompute.org/wiki/Server/Mezz>

Figure 11: LFF NIC Configuration Views
LFF with Ejector Latch

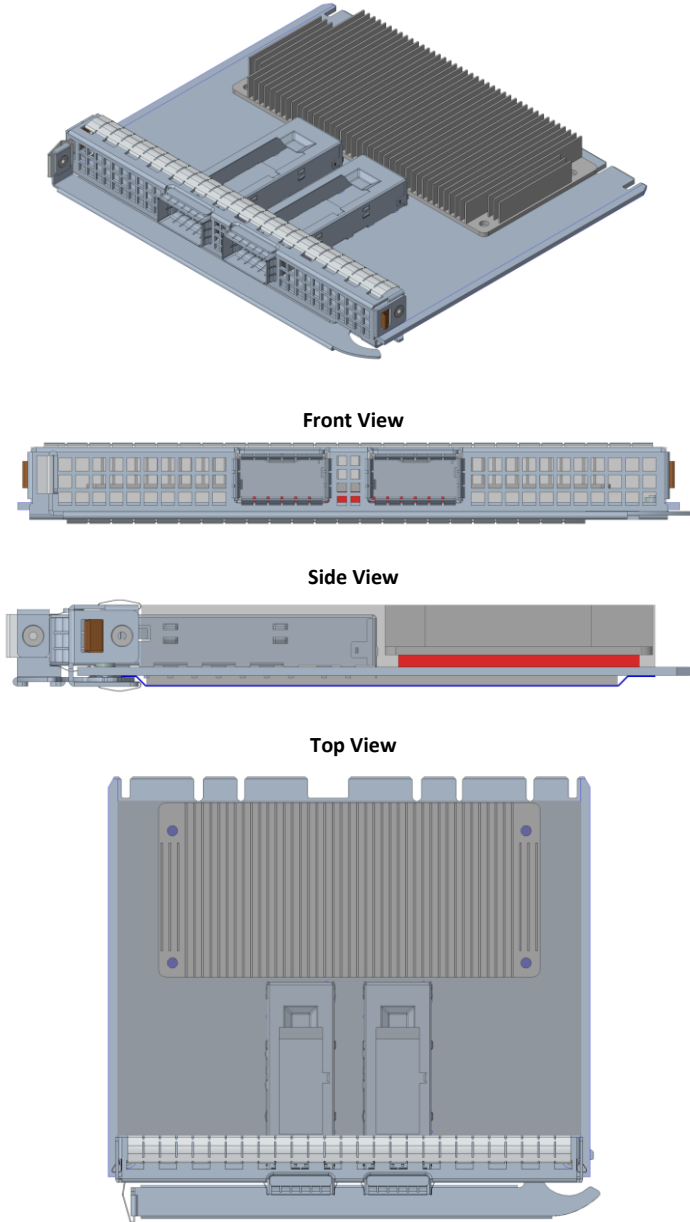


Figure 12 illustrates example LFF 3D views for the supported line side I/O implementations. The line side I/O implementations are discussed in Section 2.2.

Figure 12: LFF NIC Line Side 3D Views

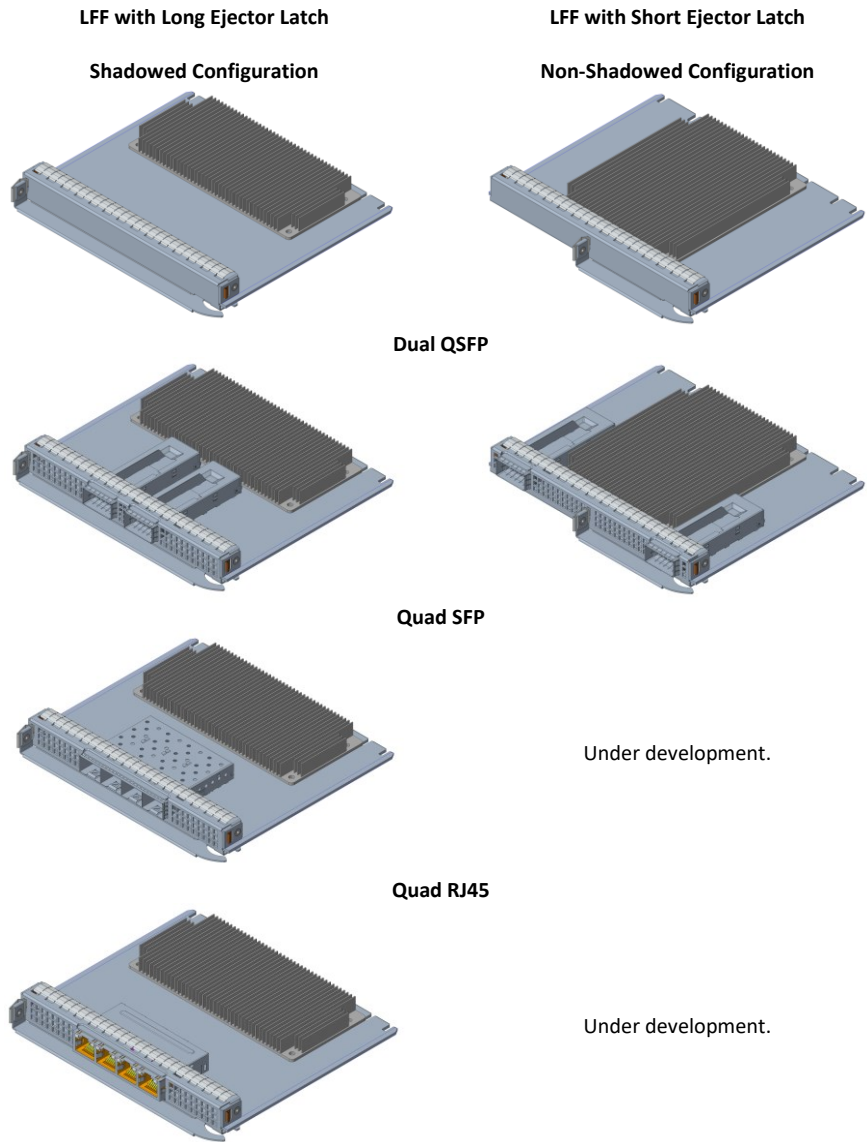
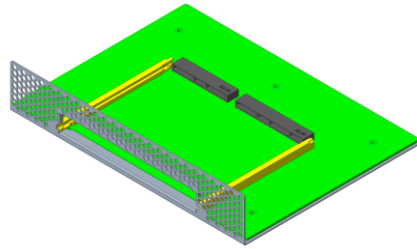
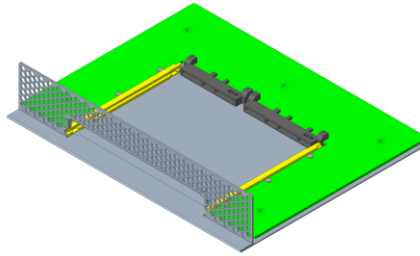


Figure 13 illustrates example LFF 3D views of the ejector latch assembly mounted in a chassis utilizing a straddle mount connector and a right-angle connector. The baseboard connector options are discussed in Section 3.2. The LFF OCP NIC 3.0 card is identical for both chassis connector options.

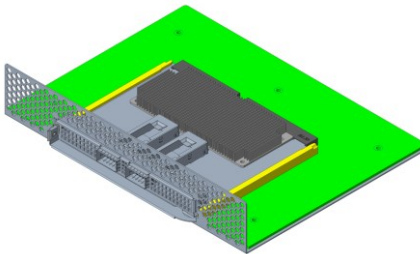
Figure 13: LFF NIC Chassis Mounted 3D Views



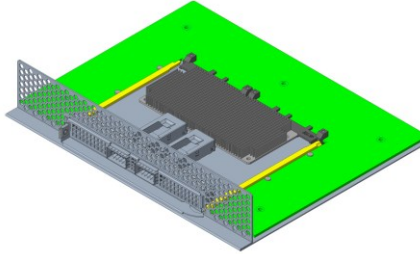
Right Angle Baseboard Connector



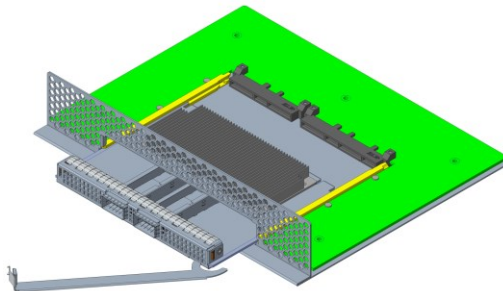
Straddle Mount Baseboard Connector



NIC Installed in Baseboard with Right Angle



NIC Installed in Baseboard with Straddle Mount



NIC Insertion / Removal (As shown with a Straddle Mount Connector)

2.2 Line Side I/O Implementations

At the time of this writing, the SFF, TSFF and LFF implementations have been optimized to support the standard line side I/O implementations shown in Table 7. OCP NIC 3.0 cards may implement a subset of line side connectors and shall stay within the allowed I/O area as depicted in Section 2.4.3 for SFF, Section 2.4.4 for TSFF and Section 2.4.5 for LFF.

Table 7: OCP NIC 3.0 Line Side I/O Implementations

| Form Factor | Max Topology Connector Count |
|-------------|------------------------------|
| SFF, TSFF | 2x QSFP+/QSFP28/QSFP-DD |
| SFF, TSFF | 4x SFP+/SFP28 |
| SFF, TSFF | 4x RJ45 |
| TSFF | 1x OSFP-RHS |
| LFF | 2x QSFP+/QSFP28 |
| LFF | 4x SFP+/SFP28 |
| LFF | 4x RJ45 |

Table 7 lists typical connectors that fit into the card form-factors. Additional connectors not listed in this table may be used if the connector keep-in heights are not exceeded. Please refer to Section 2.5 for details.

Note: For brevity, references to QSFP+, and QSFP28 shall be referred to as QSFP for the remainder of this document. Similarly, references to SFP+, and SFP28 shall be referred to as SFP.

The following specifications may be used to cross reference the associated line side I/O form-factor and module management specifications. This is not an exhaustive list. Refer to Table 3-1 in SFF-8024 – SFF Cross Reference to Industry Products for additional details.

Table 8: Line Side I/O Cross Reference to Industry Standards

| Form Factor | Pluggable Form-Factor Specification | Common Management Specification |
|-------------|-------------------------------------|---|
| SFP | INF-8074 (MSA) | SFF-8472 |
| SFP+ | SFF-8084 | SFF-8472 |
| SFP28 | SFF-8402 | SFF-8472 |
| OSFP-RHS | OSFP MSA | OSFP management Interface Specification |
| QSFP | INF-8438 (MSA) | SFF-8636 |
| QSFP+ | SFF-8436 | SFF-8636 |
| QSFP28 | SFF-8665 | SFF-8636 |
| QSFP-DD | QSFP-DD MSA | CMIS 5.0 |

SFP and QSFP cables come in passive and active variants. An active cable contains equalization or optical transceiver components. For cards that support active cables, appropriate thermal considerations shall be made per Section 6. A passive direct-attach, or RJ45 cable are purely passive elements.

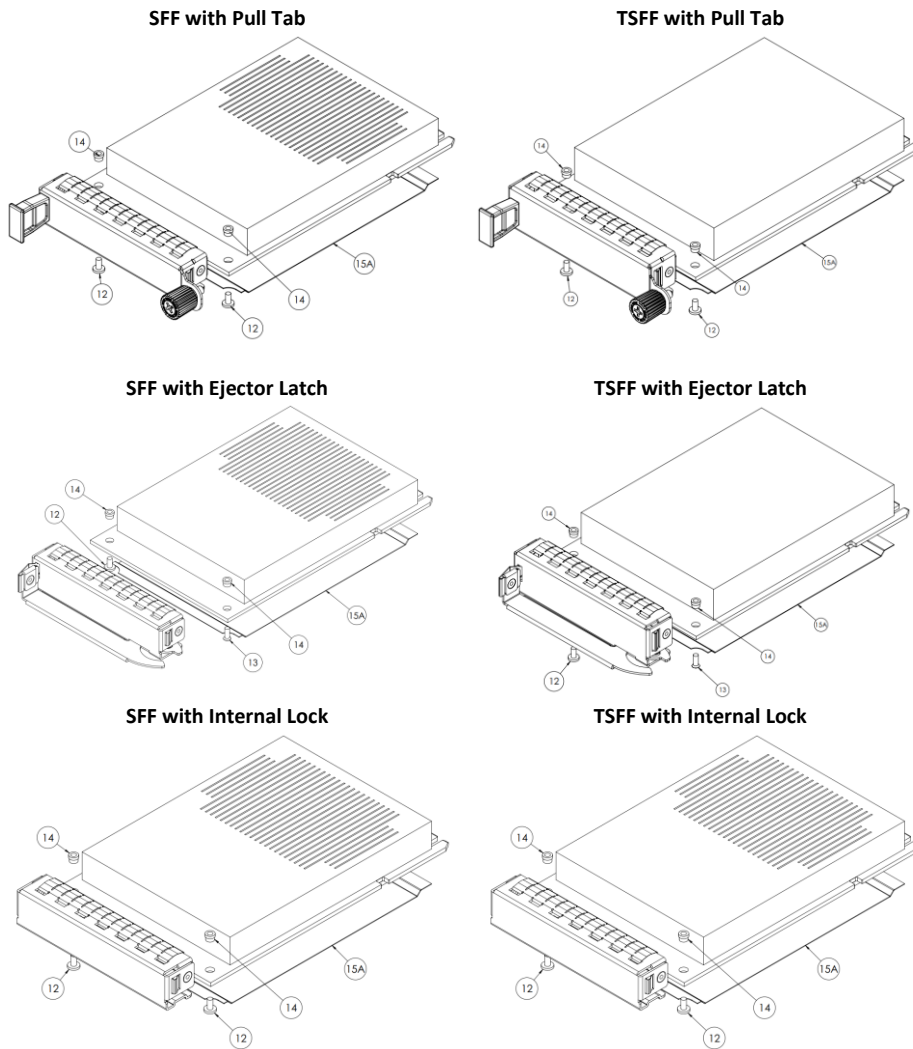
Additional combinations and connector types are permissible as I/O form factor technologies and thermal capabilities evolve.

2.3 Top Level Assembly (SFF, TSFF and LFF)

The images in Figure 14 illustrate the exploded top-level assemblies for SFF, TSFF and LFF.

Note: The TSFF implementation uses the same PCB outline as SFF. The faceplate and top-side Z-height envelope grows to 14.20 mm. Refer to the faceplate subassembly drawings in Section 2.4 for more details.

Figure 14: PBA Exploded Views (SFF, TSFF and LFF)



LFF with Ejector Latch

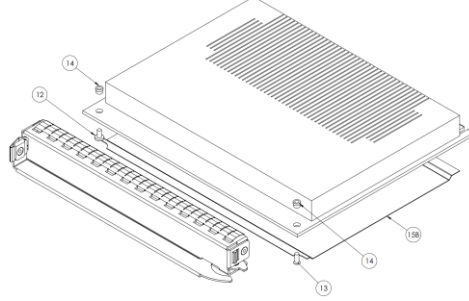


Diagram callouts #12 through #15 are installed at the NIC assembly level:

Item #12 & #13 – Screws used to attach the faceplate assembly to the OCP NIC 3.0 PBA.

Item #14 – 2x SMT nuts installed on to the PBA assembly using the reflow process.

Item #15 – Insulator is located on the secondary side and is installed on the PBA prior to the faceplate.

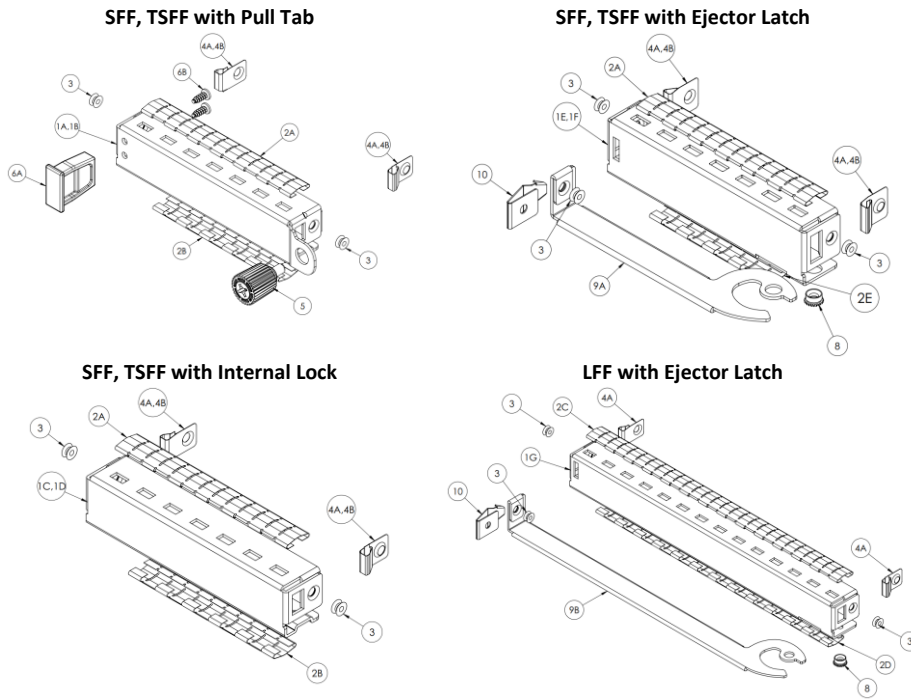
2.4 Faceplate Subassembly (SFF, TSFF and LFF)

The following section define the generic SFF, TSFF and LFF faceplates.

2.4.1 Faceplate Subassembly – Exploded View

The images in Figure 15 illustrate the three faceplates subassemblies as exploded views. The bill of materials is shown in Section 2.4.2.

Figure 15: Faceplate Assembly Exploded Views (SFF, TSFF and LFF)



2.4.2 Faceplate Subassembly – Bill of Materials (BOM)

Table 9 shows the bill of materials for the SFF, TSFF and LFF assemblies. Item number call outs align with the SFF, TSFF and LFF numbering of Figure 15.

Note: Dimensionally identical equivalent parts and equivalent materials may be substituted in the assembly. Substituted parts and materials shall meet or exceed the tolerances and requirements specified by the supplier part numbers of Table 9. Refer to the 3D CAD files for hardware specifics not covered by this table.

Table 9: Bill of Materials for the SFF and LFF Faceplate Assemblies

| Item # | Item description | Part Number / Drawing | Supplier |
|--|-------------------------------------|--|---|
| 1A 1B 1C 1D 1E 1F 1G | Faceplate | See Section 2.4.3: 1A NIC_OCPv3_SFF_Faceplate_Pulltab_20190303.pdf 1B NIC_OCPv3_TSFF_Faceplate_Pulltab_20210527.pdf 1C NIC_OCPv3_SFF_Faceplate_Latch_20190719.pdf 1D NIC_OCPv3_TSFF_Faceplate_Latch_20210527.pdf 1E NIC_OCPv3_SFF_Faceplate_IntLatch_20190303.pdf 1F NIC_OCPv3_TSFF_Faceplate_IntLatch_20210527.pdf See Section 2.4.4: 1G NIC_OCPv3_LFF_Faceplate_Latch_20190719.pdf | Custom |
| 2A 2B 2C 2D 2E | Top and Bottom EMI Fingers | 2A LT18CJ1921 – 13 fingers (Laird) TF187VE32F11-2.41-08 (Tech-Etch) 2B LT18CJ1920 – 11 fingers (Laird) TF187VE32F11-2.04-08 (Tech-Etch) 2C LT18CJ1923 – 27 fingers (Laird) TF187VE32F11-5.03-08 (Tech-Etch) 2D LT18CJ1922 – 25 fingers (Laird) TF187VE32F11-4.66-08 (Tech-Etch) 2E LT18CJ4430 – 9 fingers (Laird) TF187VE32F11-1.67-08 (Tech-Etch) | Laird, Tech-ETCH |
| 3 | Rivet | 1-AC-2424-01 | Dong Guan KSETT Hardware Technology |
| 4A 4B | Side EMI Fingers | 4A LT18DP1911 (for SFF, LFF) 4B LT21DP2320 (for TSFF) | Laird |
| 5 | Thumbscrew | 4C-99-343-K081 | Southco, Inc. |
| 6A 6B | Pull tab w/2x screws | CN-99-459 | Southco, Inc. |
| 8 | Clinch Nut | See Section 2.4.9 and drawing NIC_OCPv3_ClinchNut_20190719.pdf | Custom |
| 9A 9B | Ejector Handle | SFF Ejector: See Section 2.4.6 and drawing 9A NIC_OCPv3_EjectorHandle_Short_20190719.pdf Note: The SFF ejector is also used on the LFF non-shadowed I/O faceplate configuration. LFF Ejector: See Section 2.4.7 & Drawing 9B NIC_OCPv3_EjectorHandle_Long_20190719.pdf | Custom |
| 10 | Ejector Lock | See Section 2.4.8 and drawing NIC_OCPv3_EjectorLock_20190719.pdf | Custom |
| 12* | Screw for securing faceplate to NIC | Phillips screw: ICMMS200403N Torx screw: ITMMAE200402X | WUJIANG Screw Tech Precision Industry |

Open Compute Project • OCP NIC 3.0

Version ~~1.2.1 - DRAFT~~ 1.2.0

| Item # | Item description | Part Number / Drawing | Supplier |
|------------|--|--|---------------------------------------|
| 13* | Screw for attaching faceplate and ejector to NIC | Phillips screw: FCMMQ200503N Torx screw: FTMMC200502X | WUJIANG Screw Tech Precision Industry |
| 14 | SMT nut (on NIC) | 82-950-22-010-05-RL | Fivetech Technology Inc. |
| 15A 15B | Insulator | Refer to Section 2.7 for the SFF (15A) and LFF (15B) insulator mechanical requirements | Custom |

Note: * Phillips and Torx screws are allowed. Head types should not be mixed on the same assembly.

2.4.3 SFF Generic I/O Faceplates

Figure 16 shows the standard SFF I/O bracket with a thumbscrew and pull-tab assembly.

Figure 16: SFF Generic I/O Faceplate – Pull Tab Version (2D View)

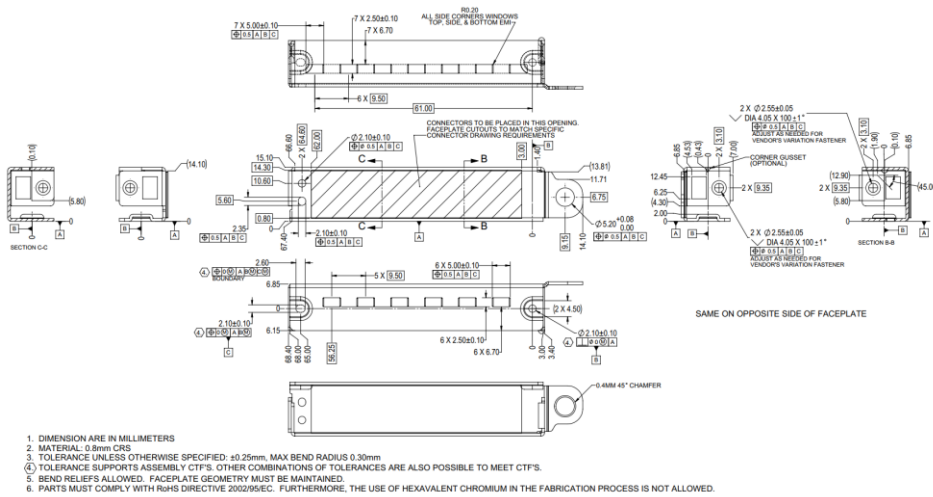


Figure 17: SFF Generic I/O Faceplate – Ejector Version (2D View)

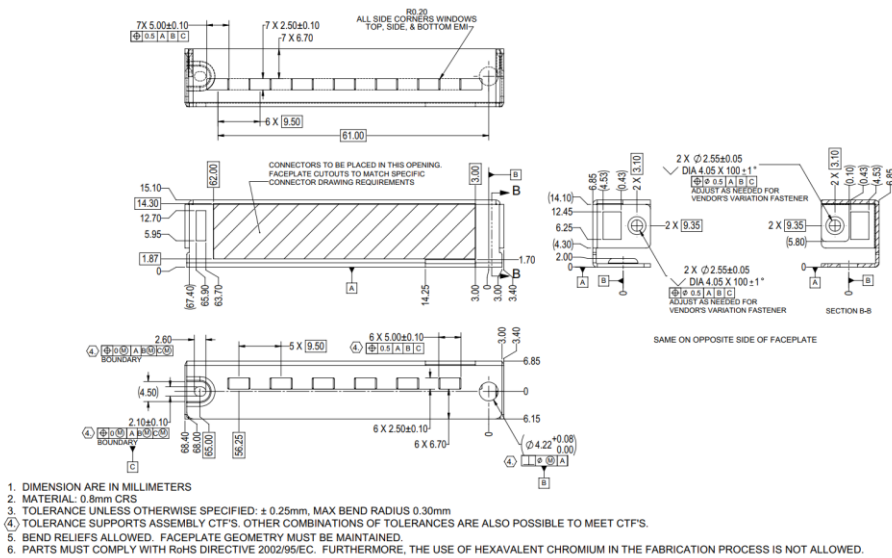
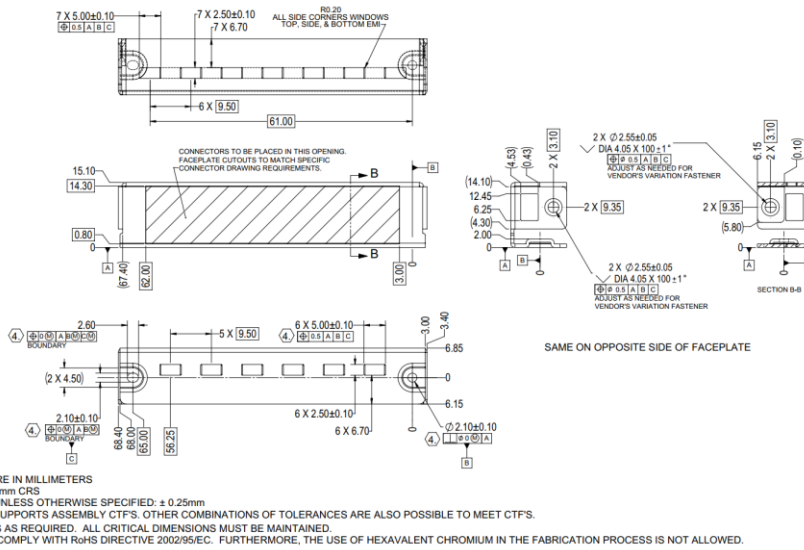


Figure 18: SFF Generic I/O Faceplate – Internal Lock Version (2D View)



2.4.4 TSFF Generic I/O Faceplates

The TSFF diagrams call out the deltas from the SFF diagrams. Refer to the SFF diagrams in Section 2.4.3 for the remaining details.

Figure 19: TSFF Generic I/O Faceplate – Pull Tab Version (2D View)

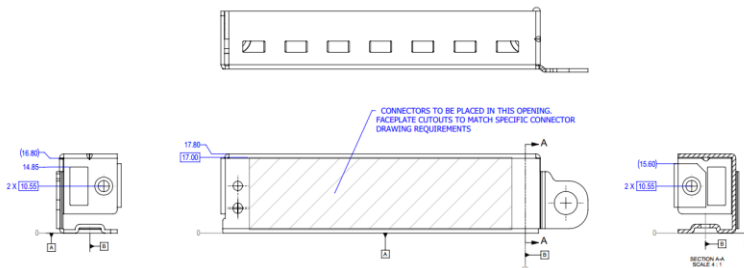


Figure 20: TSFF Generic I/O Faceplate – Ejector Version (2D View)

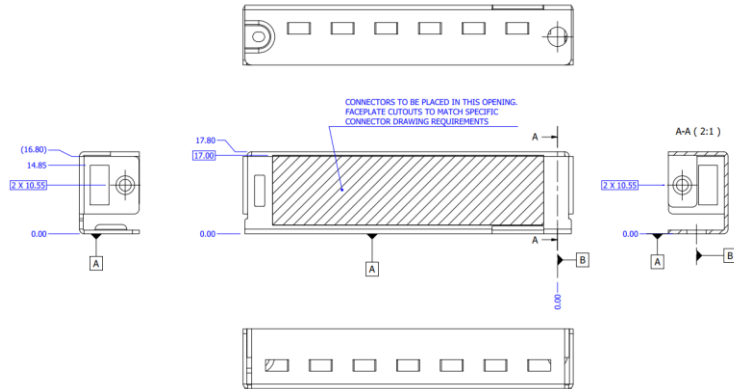
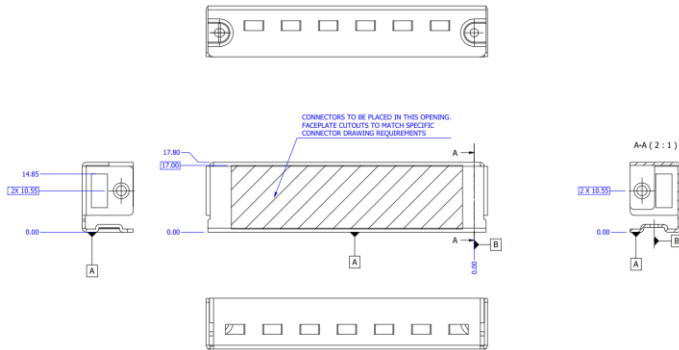
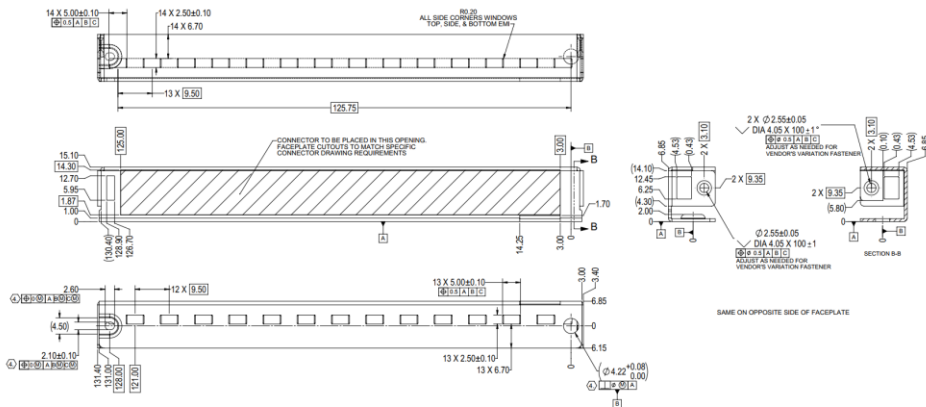


Figure 21: TSFF Generic I/O Faceplate – Internal Lock Version (2D View)



2.4.5 LFF Generic I/O Faceplate

Figure 22: LFF Generic I/O Faceplate – Ejector Version (2D View)

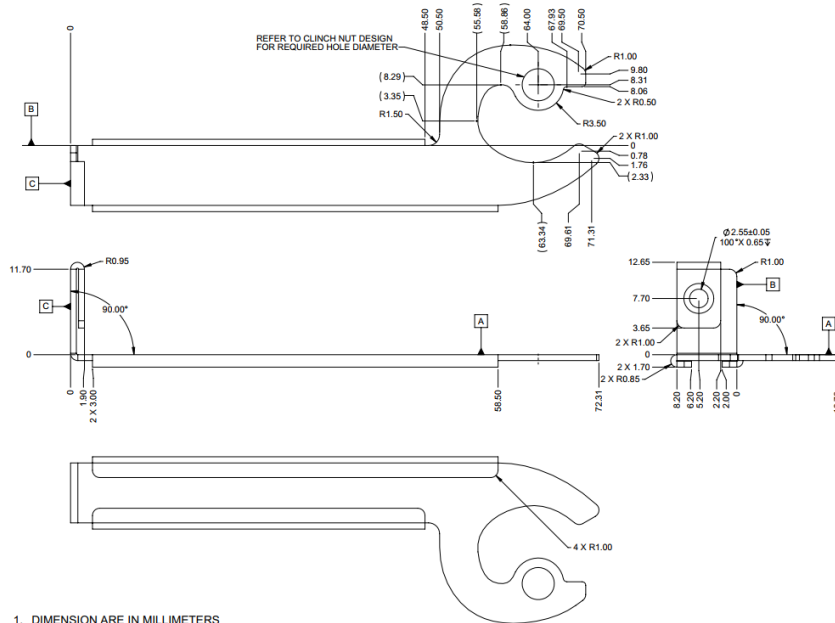


1. DIMENSION ARE IN MILLIMETER
2. MATERIAL: 0.8mm CRS
3. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.25mm. MAX BEND RADIUS 0.30mm
4. TOLERANCE SUPPORTS ASSEMBLY CTF'S. OTHER COMBINATIONS OF TOLERANCES ARE ALSO POSSIBLE TO MEET CTF'S.
5. BEND RELIEFS ALLOWED. FACEPLATE GEOMETRY MUST BE MAINTAINED. ANY DEVIATIONS MUST BE APPROVED.
6. PARTS MUST COMPLY WITH RoHS DIRECTIVE 2002/95/EC. FURTHERMORE, THE USE OF HEXAVALENT CHROMIUM IN THE FABRICATION PROCESS IS NOT ALLOWED.

2.4.6 Ejector Lever (SFF, TSFF)

This section defines the SFF lever dimensions. Note: this SFF ejector lever is also used on the non-shadowed LFF faceplate configuration.

Figure 23: SFF I/O Faceplate – Ejector Lever (2D View)

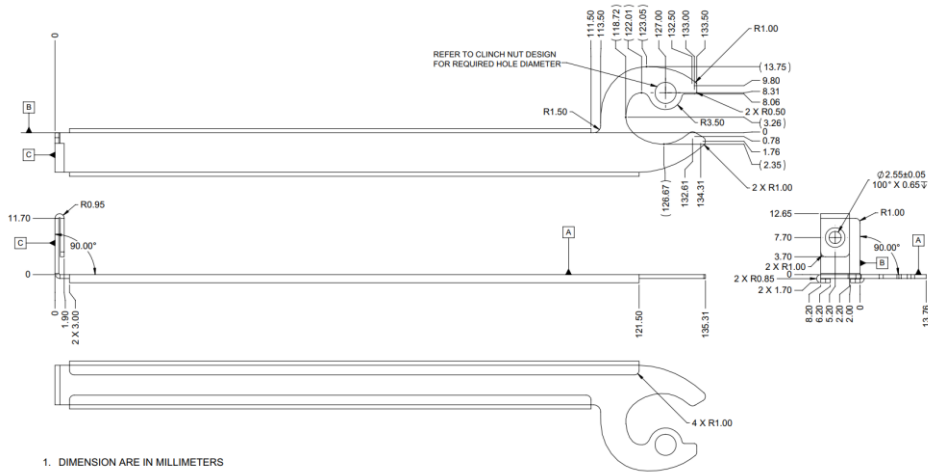


1. DIMENSION ARE IN MILLIMETERS
2. MATERIAL: 0.8mm 301 SS 1/4 HARD
3. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.25mm, ± 1.0°
4. PARTS MUST COMPLY WITH RoHS DIRECTIVE 2002/95/EC. FURTHERMORE, THE USE OF HEXAVALENT CHROMIUM IN THE FABRICATION PROCESS IS NOT ALLOWED.

2.4.7 Ejector Levers (LFF)

This section defines the LFF ejector lever dimensions.

Figure 24: LFF I/O Faceplate – Ejector Lever (2D View)

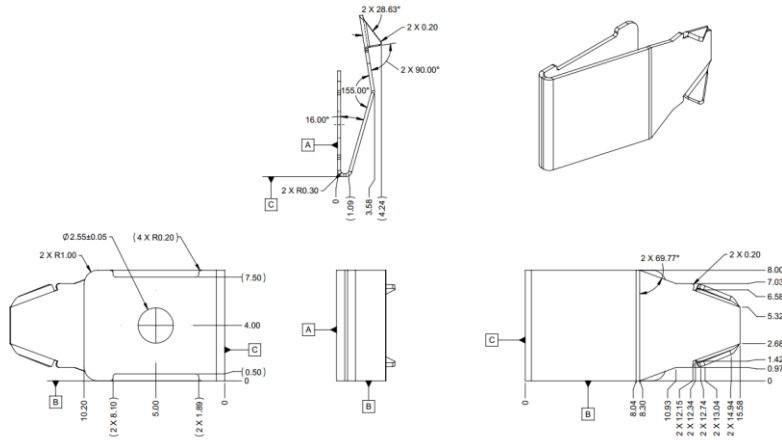


1. DIMENSION ARE IN MILLIMETERS
2. MATERIAL: 0.8mm 301 SS 1/4 HARD
3. TOLERANCE UNLESS OTHERWISE SPECIFIED: $\pm 0.25\text{mm}$, $\pm 1.0^\circ$
4. PARTS MUST COMPLY WITH RoHS DIRECTIVE 2002/95/EC. FURTHERMORE, THE USE OF HEXAVALENT CHROMIUM IN THE FABRICATION PROCESS IS NOT ALLOWED.

2.4.8 Ejector Lock (SFF, TSFF and LFF)

The SFF and LFF ejector uses a locking mechanism at the end of the handle to retain the lever position. This is shown in Figure 25.

Figure 25: Ejector Lock



1. DIMENSION ARE IN MILLIMETERS
2. MATERIAL: 0.3mm-301 SS 1/2 HARD
3. TOLERANCE UNLESS OTHERWISE SPECIFIED: $\pm 0.25\text{mm}$, $\pm 1.0^\circ$
4. PARTS MUST COMPLY WITH RoHS DIRECTIVE 2002/95/EC. FURTHERMORE, THE USE OF HEXAVALENT CHROMIUM IN THE FABRICATION PROCESS IS NOT ALLOWED.

2.4.9 Clinch Nut (SFF and LFF)

The SFF/TSFF and LFF card ejector handle uses a clinch nut as a spacer and rotation anchor. The clinch nut binds the ejector handle to the faceplate. Two clinch nut options are available to accommodate supplier manufacturing processes. These are shown in Figure 26 and Figure 27.

Figure 26: Clinch Nut Option A

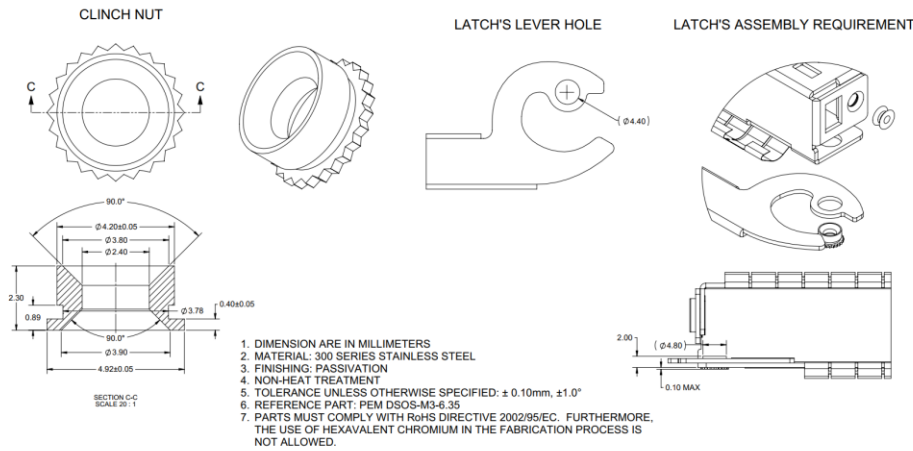
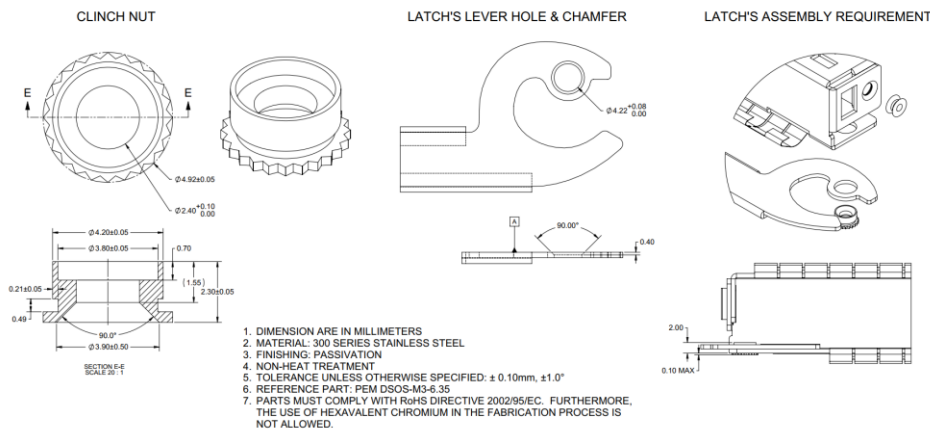


Figure 27: Clinch Nut Option B

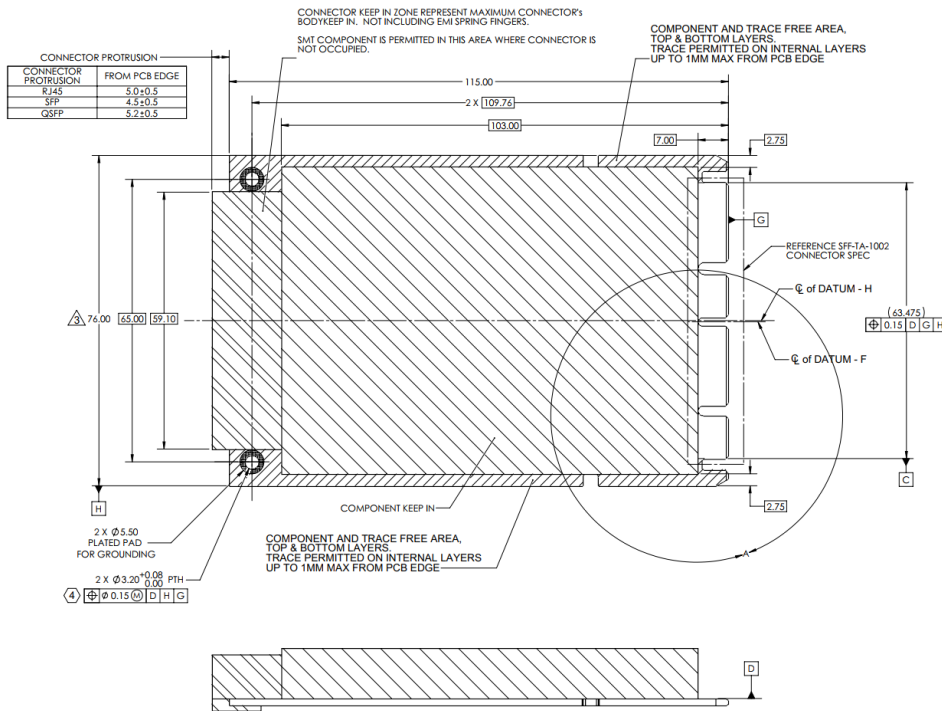


2.5 Card Keep Out Zones

2.5.1 SFF Keep Out Zones

Note: The SFF top, detail and bottom view keep out zones are also applicable to the TSFF.

Figure 28: SFF Keep Out Zone – Top View



- NOTES:
- UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETERS
 - TOLERANCE UNLESS OTHERWISE SPECIFIED: ±0.13, ±1°
 - ANY BREAK OFF FEATURE MUST ADHERE TO THE SPECIFIED DIMENSION EXCEPT THAT THE TOLERANCE IS +0.13/-0.23. THE SUM OF THE EDGE LENGTHS OF ALL BREAK OFF FEATURES CANNOT EXCEED 40 MM PER SIDE
 - TOLERANCE SUPPORTS ASSEMBLY CTF'S. OTHER COMBINATIONS OF TOLERANCES ARE ALSO POSSIBLE.

Figure 29: SFF Keep Out Zone – Top View – Detail A

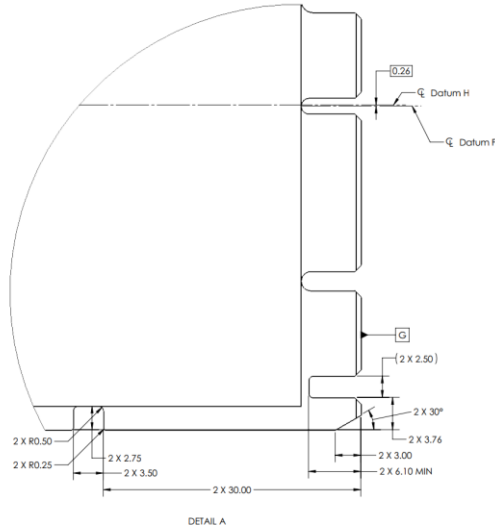


Figure 30: SFF Keep Out Zone – Bottom View

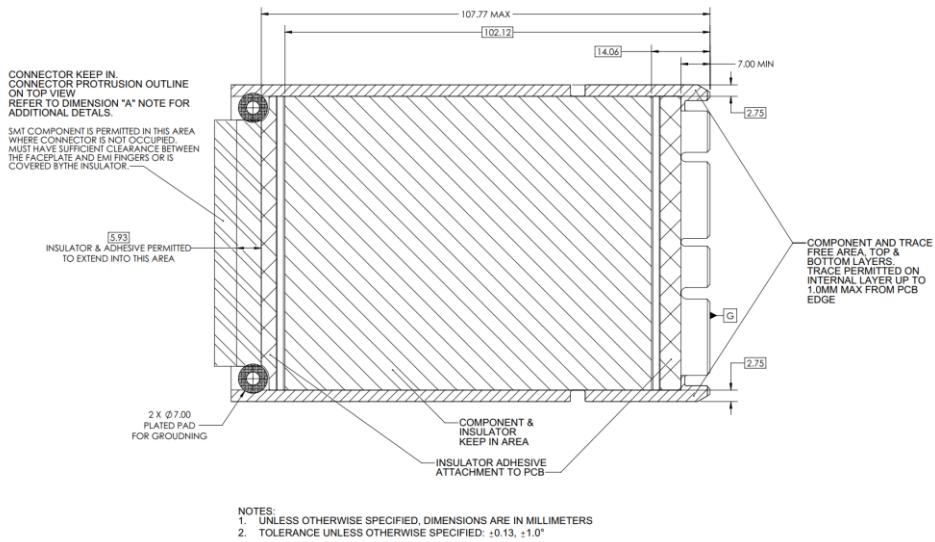
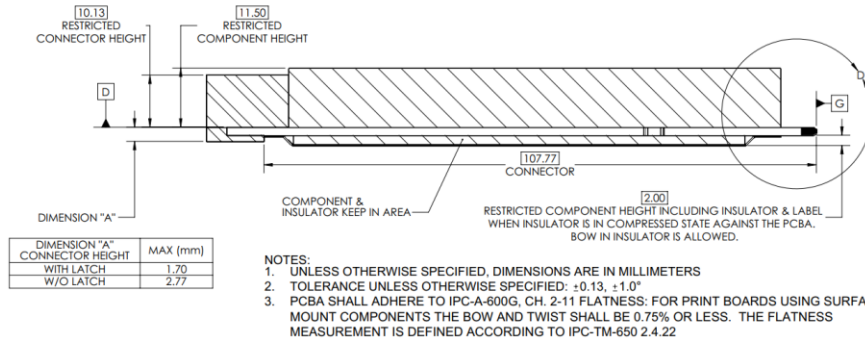
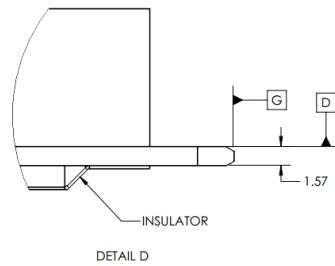


Figure 31: SFF Keep Out Zone – Side View



Note: The area defined by DIMENSION "A" is between the faceplate and the primary side of the board. Grounded through-hole mounting pins are permitted but should avoid making contact with the latching mechanism and EMI fingers. Signal pins are not permitted in this area.

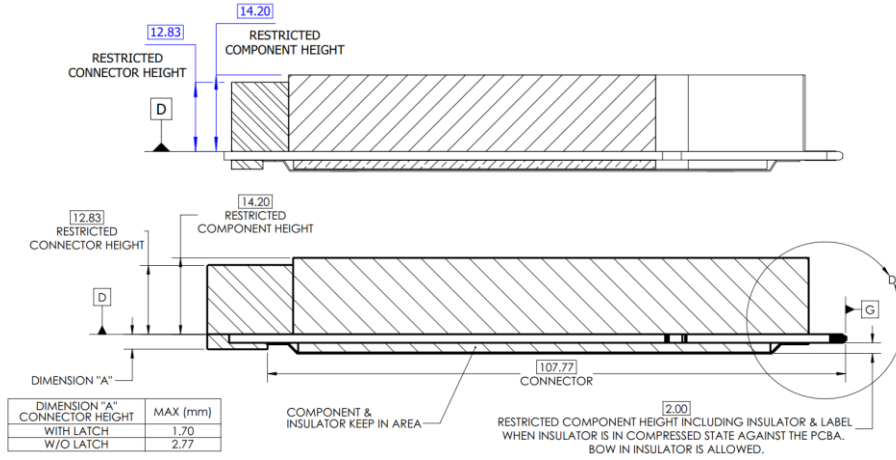
Figure 32: SFF Keep Out Zone – Side View – Detail D



2.5.2 TSFF Keep Out Zones

The TSFF keep out zones are identical to the SFF except for the side view. This is shown in Figure 33. Refer to the SFF keep out zone in Section 2.5.1 for the remaining details.

Figure 33: TSFF Keep Out Zone – Side View



NOTES:

1. UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETERS
2. TOLERANCE UNLESS OTHERWISE SPECIFIED: $-0.13, \pm 1.0^\circ$
3. PCBA SHALL ADHERE TO IPC-A-600G, CH. 2-11 FLATNESS: FOR PRINT BOARDS USING SURFACE MOUNT COMPONENTS THE BOW AND TWIST SHALL BE 0.75% OR LESS. THE FLATNESS MEASUREMENT IS DEFINED ACCORDING TO IPC-TM-650 2.4.22

2.5.3 LFF Keep Out Zones

Figure 34: LFF Keep Out Zone – Top View

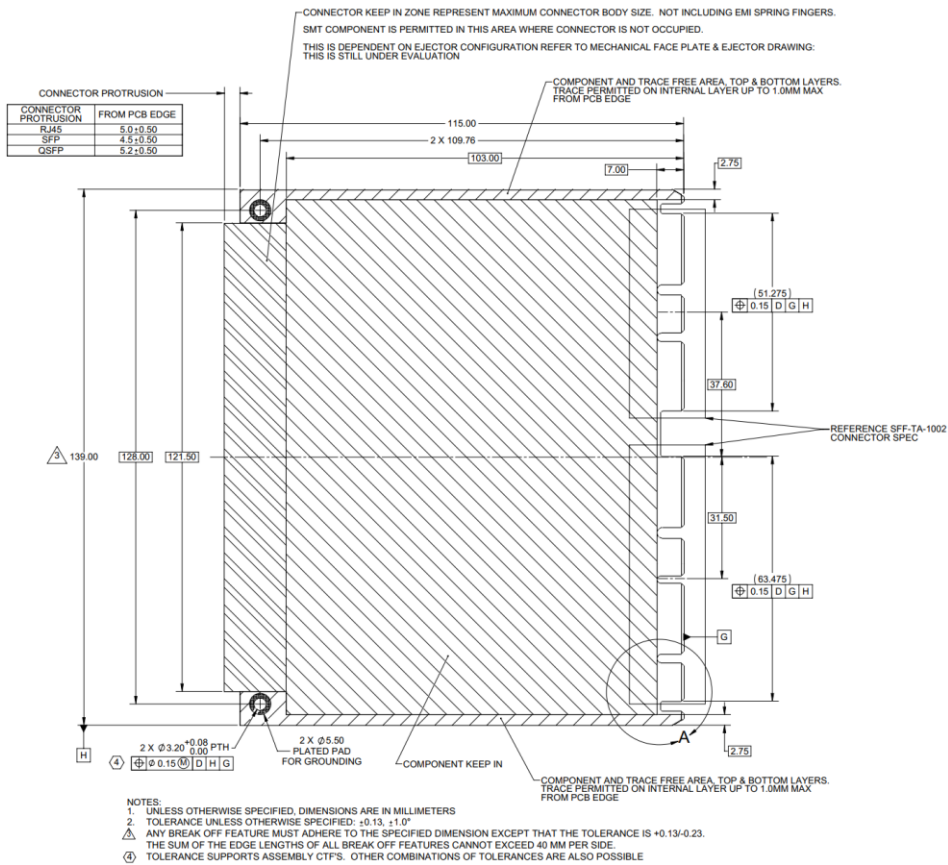


Figure 35: LFF Keep Out Zone – Top View – Detail A

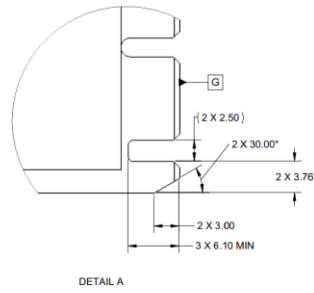


Figure 36: LFF Keep Out Zone – Bottom View

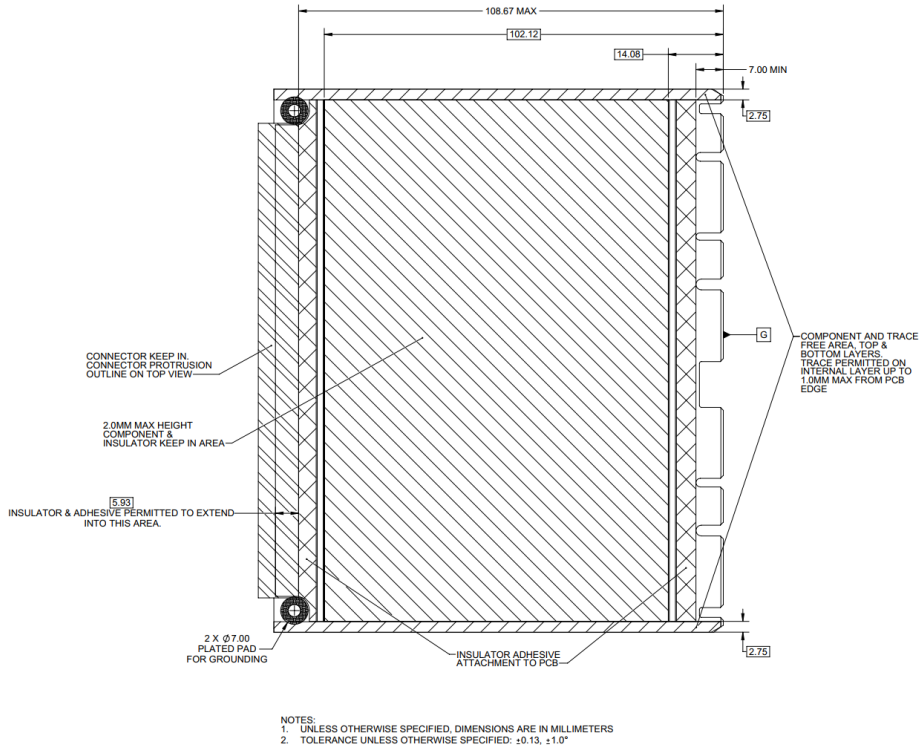


Figure 37: LFF Keep Out Zone – Side View

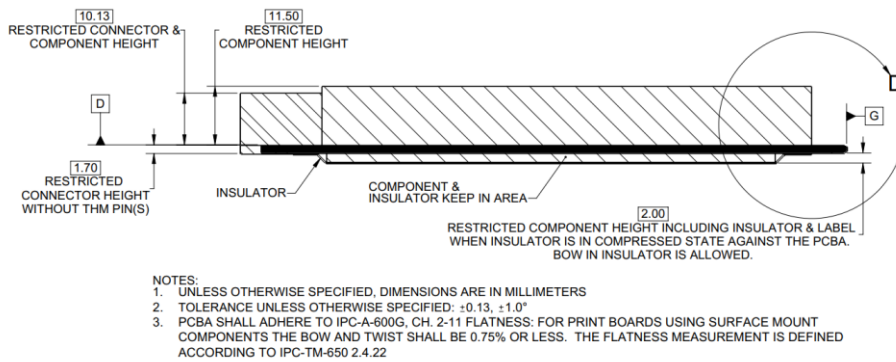
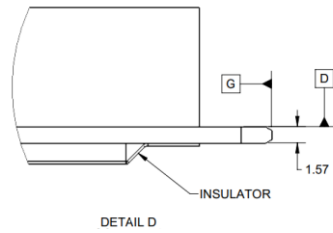


Figure 38: LFF Keep Out Zone – Side View – Detail D



2.6 Baseboard Keep Out Zones

Refer to the 3D CAD files for the baseboard keep out zones for the SFF, TSFF and LFF designs. The 3D CAD files are available for download on the OCP NIC 3.0 Wiki:

<http://www.opencompute.org/wiki/Server/Mezz>

2.7 Insulation Requirements

All OCP NIC 3.0 cards shall implement an insulator to prevent the bottom side card components from shorting out to the baseboard chassis. The recommended insulator thickness is 0.25 mm and shall reside within the following mechanical envelopes for the SFF, TSFF and LFF. An alternate insulator thickness of 0.127 mm is permitted. The total stack up height of the secondary side components, insulator and the labels shall not exceed the 2 mm keep-in dimension as shown in Section 2.7.1 and 2.7.2.

A maximum of four circular holes with a 4 mm maximum diameter are permitted for access to mechanical retention components. Any components exposed by these holes must be non-conductive.

2.7.1 SFF, TSFF Insulator

Figure 39: SFF, TSFF Bottom Side Insulator (3D View)

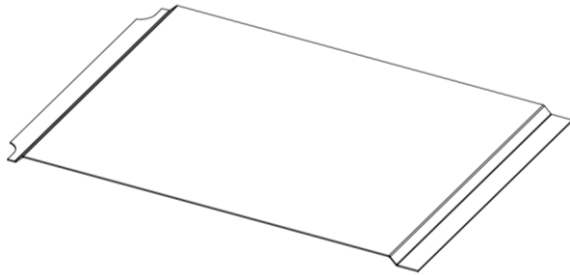
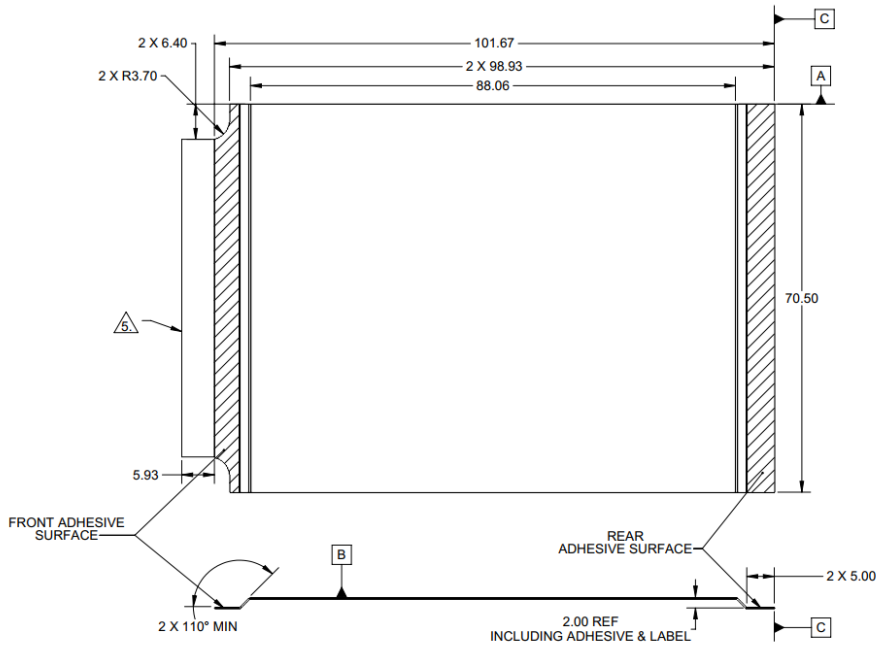


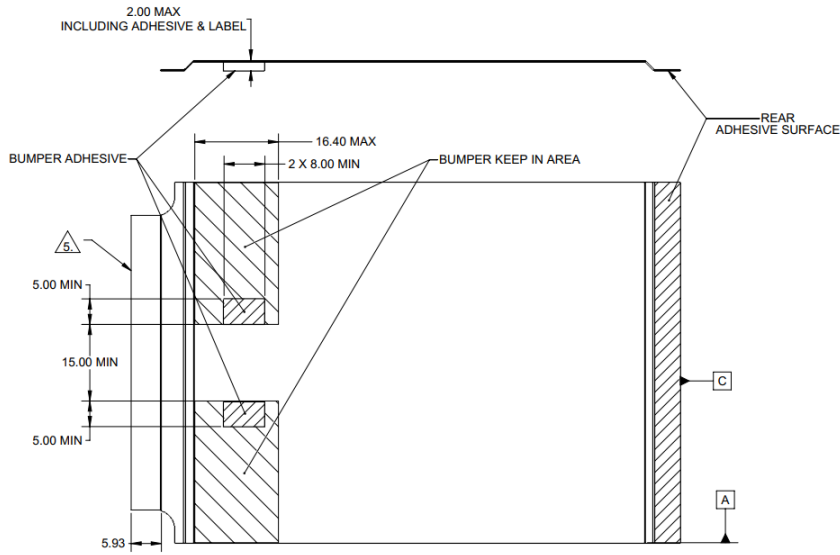
Figure 40: SFF, TSFF Bottom Side Insulator (Top and Side View)



1. DIMENSIONS ARE IN MILLIMETERS
2. MATERIAL:
 1. FORMEX GK-10BK or FORMEX N3 (HALOGEN FREE, BLACK OR NATURAL), 0.25mm THICKNESS
 2. FORMEX GK-5BK (HALOGEN FREE, BLACK), 0.127mm THICKNESS
3. MATERIAL SHALL CONFORM TO 94VTM-0
4. ADHESIVE 3M 467MP 0.05mm THICKNESS
5. FRONT EDGE OF INSULATOR AND ADHESIVE MAY EXTEND TO 107.60MM IF NECESSARY TO PROTECT LEADS ON SECONDARY SIDE OF PCBA.
6. TOLERANCE UNLESS OTHERWISE SPECIFIED: $\pm 0.30\text{mm}$, $\pm 1.0^\circ$

Figure 41: SFF, TSFF Bottom Side Insulator (alternate) (Top and Side View)

ALTERNATE OPTION USING BUMPER & ADHESIVE FOR ATTACHING THE INSULATOR TO PCB INSTEAD OF USING FRONT ADHESIVE SURFACE.
ENSURE CORRESPONDING SURFACE ON THE PCB IS FLAT.



2.7.2 LFF Insulator

Figure 42: LFF Bottom Side Insulator (3D View)

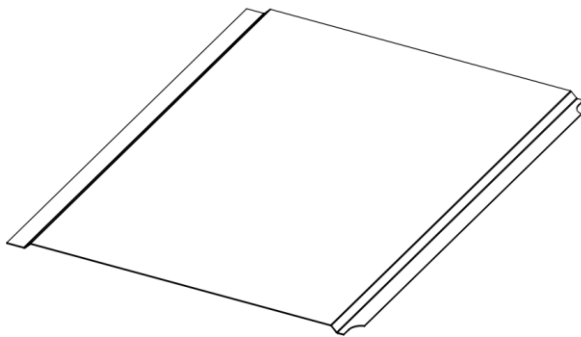
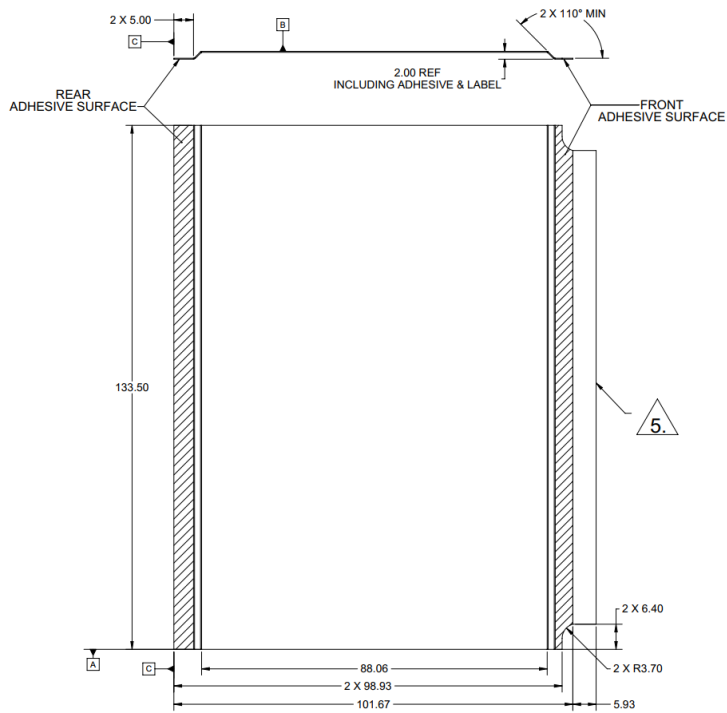


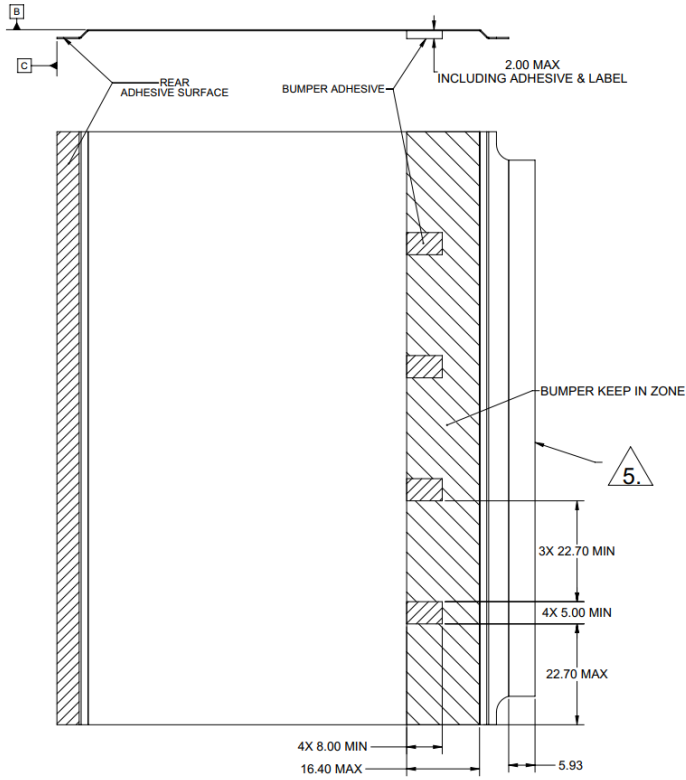
Figure 43: LFF Bottom Side Insulator (Top and Side View)



1. DIMENSION ARE IN MILLIMETERS
2. MATERIAL: FORMEX GK-10BK; FORMEX N3 (HALOGEN FREE, BLACK OR NATURAL), 0.25mm THICKNESS
3. MATERIAL SHALL CONFORM TO 94VTM-0
4. ADHESIVE 3M 467MP 0.05mm THICKNESS
5. FRONT EDGE OF INSULATOR AND ADHESIVE MAY EXTEND TO 107.60MM IF NECESSARY TO PROTECT LEADS ON SECONDARY SIDE OF PCBA.
6. TOLERANCE UNLESS OTHERWISE SPECIFIED: $\pm 0.30\text{mm}$, $\pm 1.0^\circ$

Figure 44: LFF Bottom Side Insulator (alternate) (Top and Side View)

ALTERNATE OPTION USING BUMPER & ADHESIVE FOR ATTACHING THE INSULATOR TO PCB INSTEAD OF USING FRONT ADHESIVE SURFACE.
ENSURE CORRESPONDING SURFACE ON PCB IS FLAT



2.8 Critical-to-Function (CTF) Dimensions (SFF, TSFF and LFF)

2.8.1 CTF Tolerances

The following CTF tolerances are used in this section and are the same for the SFF, TSFF and LFF.

Table 10: CTF Default Tolerances (SFF, TSFF and LFF OCP NIC 3.0)

| CTF DEFAULT TOLERANCES | |
|------------------------|--------------------------|
| DIMENSION RANGE | TOLERANCE |
| | TWO PLACE DECIMALS: X.XX |
| LINEAR: | ± 0.30 |
| ANGULAR: | ± 1.00 DEGREES |
| HOLE DIAMETER: | ± 0.13 |

2.8.2 SFF Pull Tab CTF Dimensions

The following dimensions are considered critical-to-function (CTF) for each SFF OCP NIC 3.0 card with a pull tab and thumbscrew. The CTF default tolerances are shown in Section 2.8.1.

Figure 45: SFF OCP NIC 3.0 Card with Pull Tab CTF Dimensions (Top View)

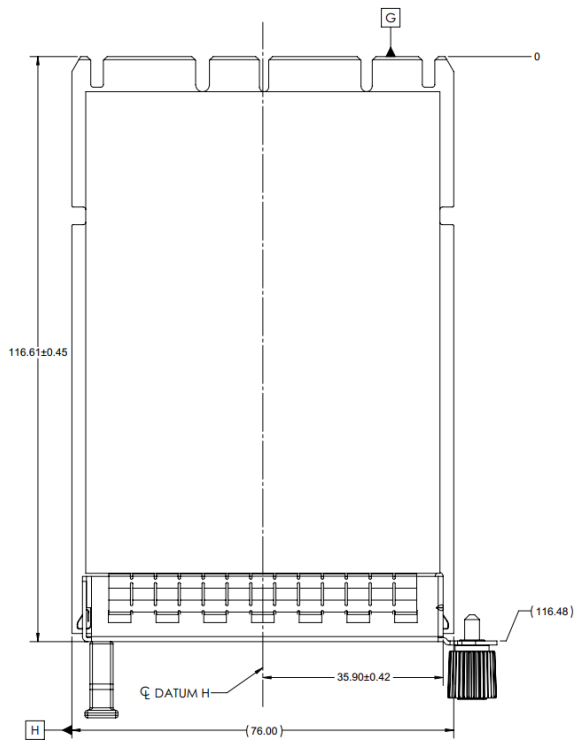


Figure 46: SFF OCP NIC 3.0 Card with Pull Tab CTF Dimensions (Front View)

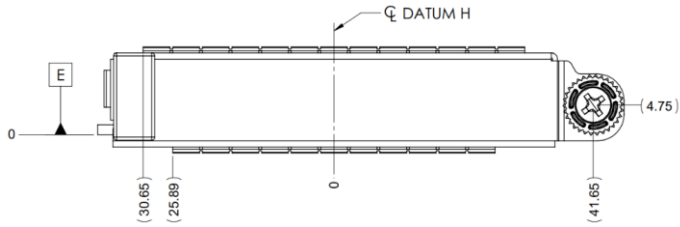
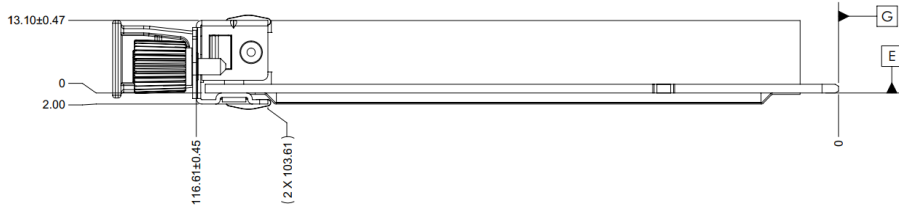


Figure 47: SFF OCP NIC 3.0 Card with Pull Tab CTF Dimensions (Side View)



2.8.3 SFF Ejector Latch CTF Dimensions

The following dimensions are considered critical-to-function (CTF) for each SFF OCP NIC 3.0 card with an ejector latch. The CTF default tolerances are shown in Section 2.8.1.

Figure 48: SFF OCP NIC 3.0 Card with Ejector Latch CTF Dimensions (Top View)

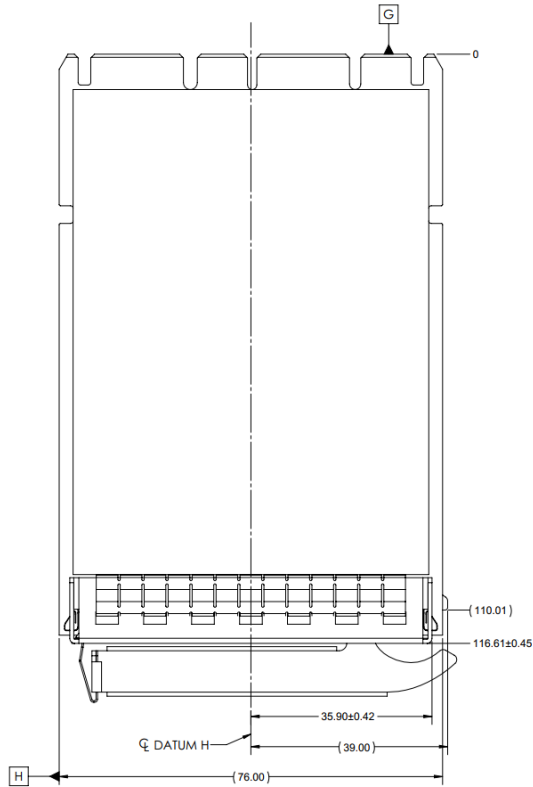


Figure 49: SFF OCP NIC 3.0 Card with Ejector CTF Dimensions (Front View)

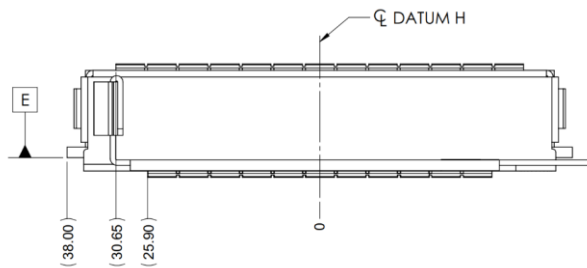
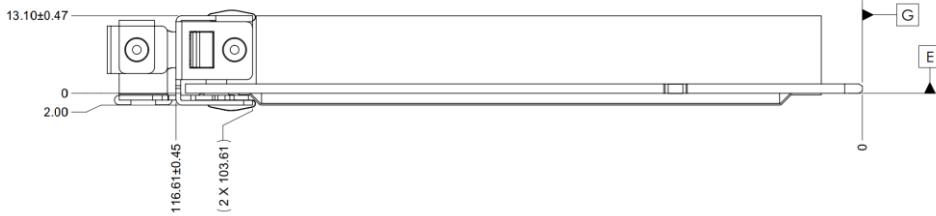


Figure 50: SFF OCP NIC 3.0 Card with Ejector CTF Dimensions (Side View)



2.8.4 SFF Internal Lock CTF Dimensions

The following dimensions are considered critical-to-function (CTF) for each SFF OCP NIC 3.0 card with an internal lock. The CTF default tolerances are shown in Section 2.8.1.

Figure 51: SFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Top View)

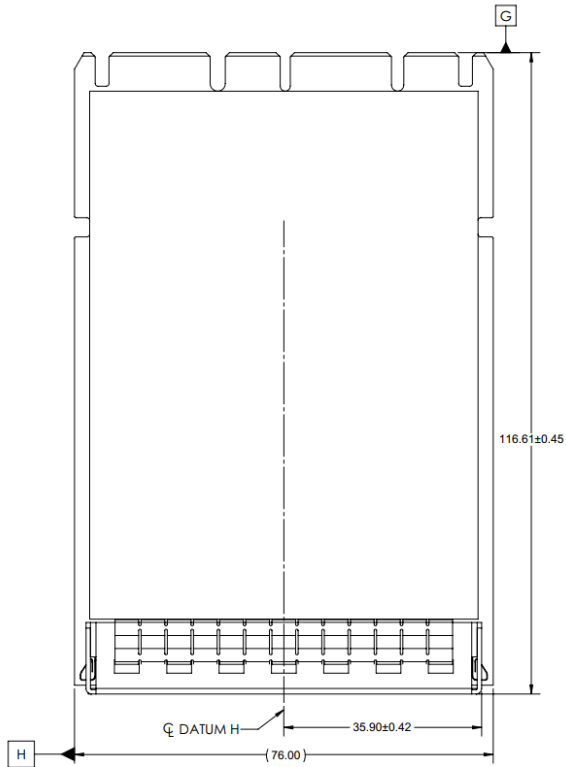


Figure 52: SFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Front View)

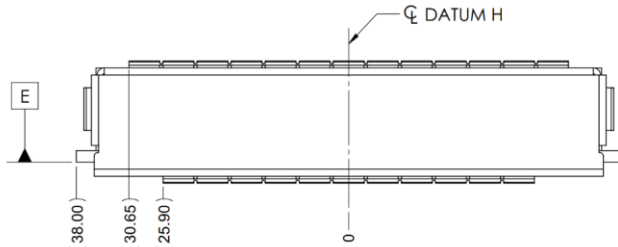
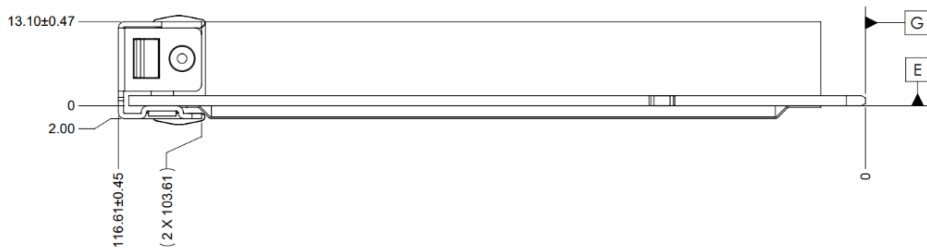


Figure 53: SFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Side View)



2.8.5 SFF Baseboard CTF Dimensions

The following dimensions are considered critical-to-function (CTF) for each SFF baseboard chassis. The CTF default tolerances are shown in Section 2.8.1.

Note: The SFF baseboard CTF dimensions are applicable to both the right angle and straddle mount connector configurations. The faceplate opening relative to the baseboard changes due to the connector vertical offset, but all CTF dimensions remain identical.

Figure 54: SFF Baseboard Chassis CTF Dimensions (Rear View)

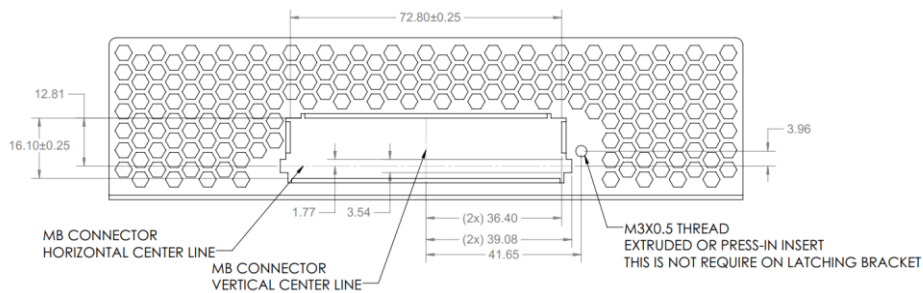


Figure 55: SFF Baseboard Chassis to Card Thumb Screw CTF Dimensions (Side View)

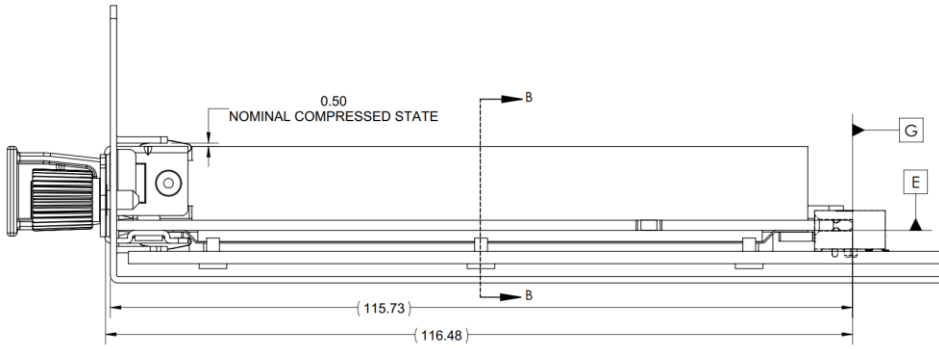


Figure 56: SFF Baseboard Chassis to Ejector lever Card CTF Dimensions (Side View)

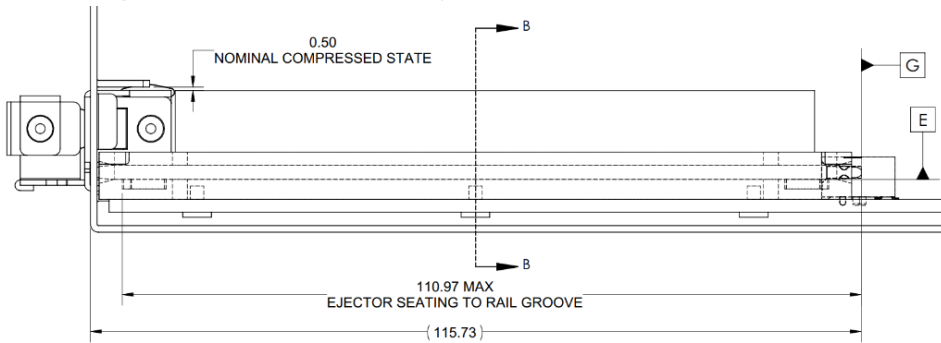


Figure 57: SFF Baseboard Chassis CTF Dimensions (Rear Rail Guide View)

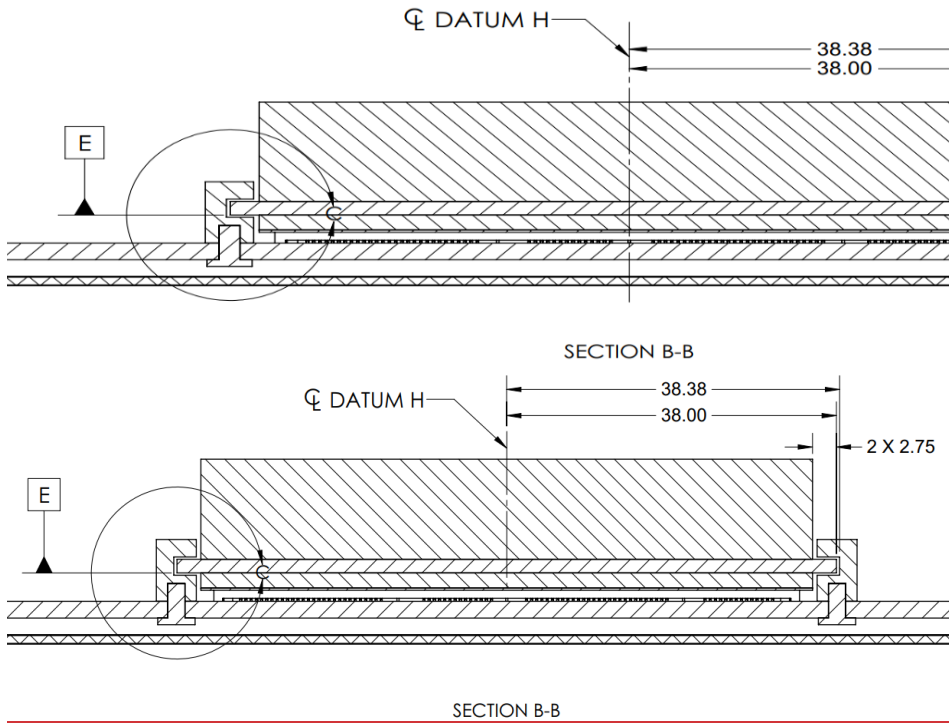
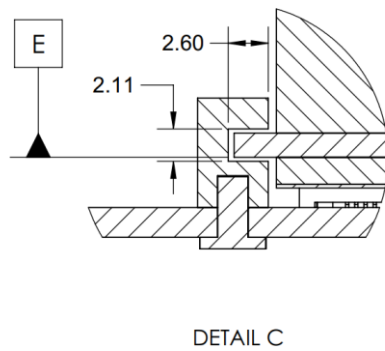


Figure 58: SFF Baseboard Chassis CTF Dimensions (Rail Guide Detail) – Detail C



Open Compute Project • OCP NIC 3.0

Version ~~1.2.1 - DRAFT~~ 2.0

The right angle and straddle mount card guides are identical between the SFF and LFF cards. The card guide model is included in the 3D CAD packages and may be downloaded from the OCP NIC 3.0 Wiki site: <http://www.opencompute.org/wiki/Server/Mezz>.

2.8.6 TSFF Pull Tab CTF Dimensions

The TSFF CTF dimensions only differ for the Z-height envelope and are noted below. Refer to the corresponding SFF drawing for the remaining dimensions.

Figure 59: TSFF OCP NIC 3.0 Card with Pull Tab CTF Dimensions (Top View)



2.8.7 TSFF Ejector Latch CTF Dimensions

The TSFF CTF dimensions only differ for the Z-height envelope and are noted below. Refer to the corresponding SFF drawing for the remaining dimensions.

Figure 60: TSFF OCP NIC 3.0 Card with Ejector Latch CTF Dimensions (Top View)



2.8.8 TSFF Internal Lock CTF Dimensions

The TSFF CTF dimensions only differ for the Z-height envelope and are noted below. Refer to the corresponding SFF drawing for the remaining dimensions.

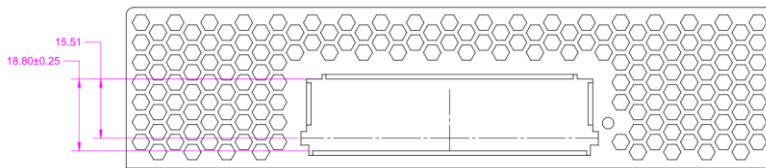
Figure 61: TSFF OCP NIC 3.0 Card with Internal Lock CTF Dimensions (Top View)



2.8.9 TSFF Baseboard CTF Dimensions

The TSFF CTF dimensions only differ for the Z-height envelope and are noted below. Refer to the corresponding SFF drawing for the remaining dimensions.

Figure 62: TSFF Baseboard Chassis CTF Dimensions (Rear View)



2.8.10 LFF Ejector Latch CTF Dimensions

The following dimensions are considered critical-to-function (CTF) for each LFF OCP NIC 3.0 card. The CTF default tolerances are shown in Section 2.8.1.

Figure 63: LFF OCP NIC 3.0 Card with Ejector Latch CTF Dimensions (Top View)

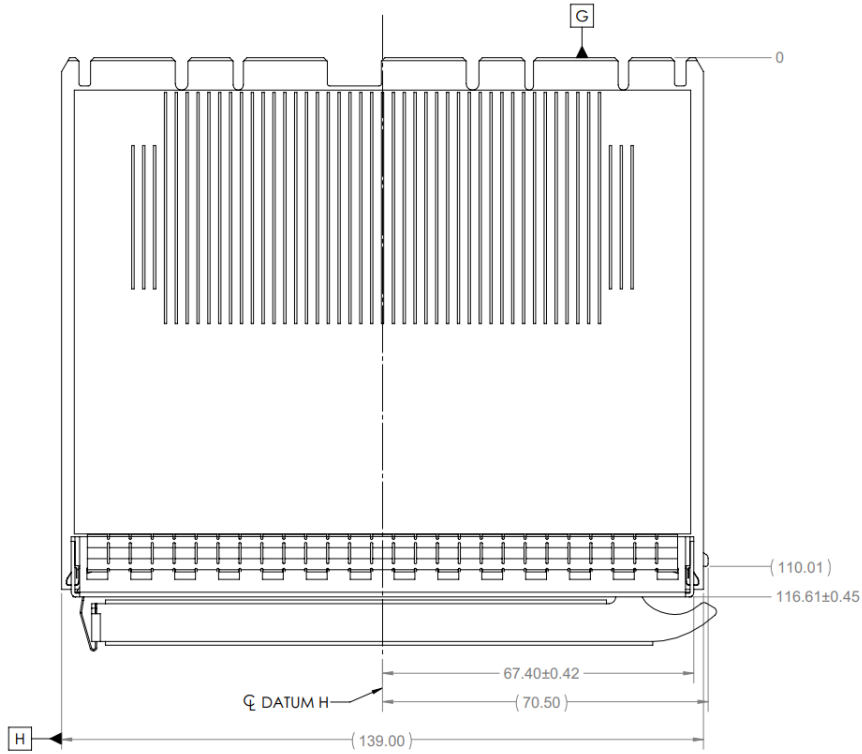


Figure 64: LFF OCP NIC 3.0 Card with Ejector CTF Dimensions (Front View)

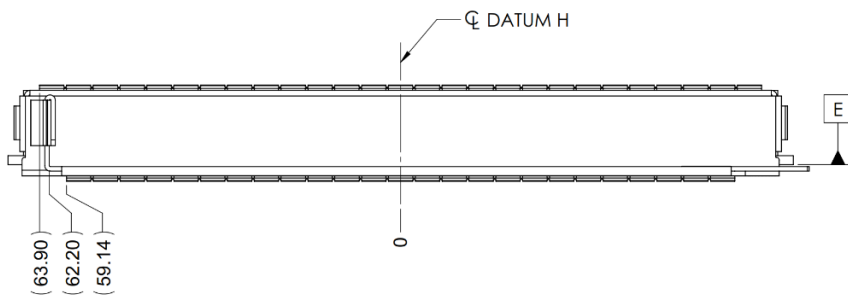
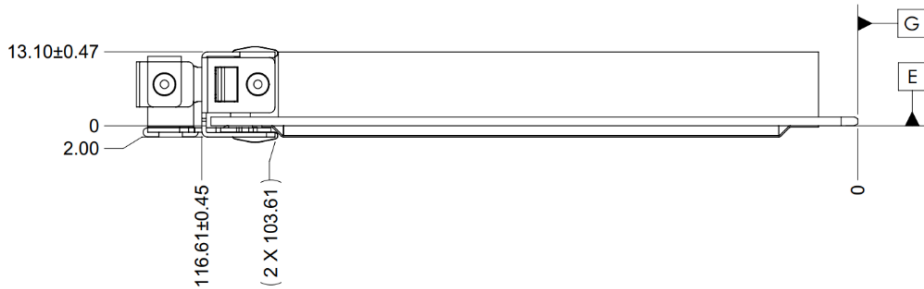


Figure 65: LFF OCP NIC 3.0 Card with Ejector CTF Dimensions (Side View)



2.8.11 LFF Baseboard CTF Dimensions

The following dimensions are considered critical-to-function (CTF) for each LFF baseboard chassis. The CTF default tolerances are shown in Section 2.8.1.

Note: The LFF baseboard CTF dimensions are applicable to both the right angle and straddle mount connector configurations. The faceplate opening relative to the baseboard changes due to the connector vertical offset, but all CTF dimensions remain identical.

Figure 66: LFF Baseboard Chassis CTF Dimensions (Rear View)

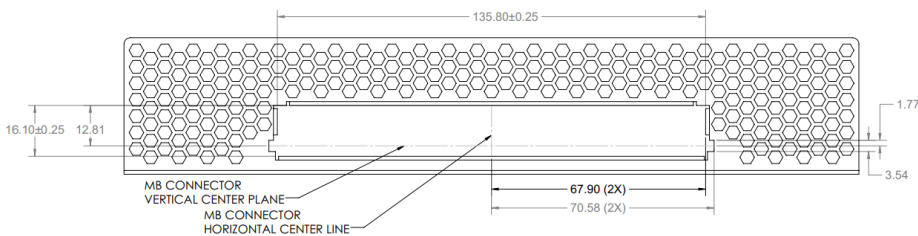


Figure 67: LFF Baseboard Chassis CTF Dimensions (Side View)

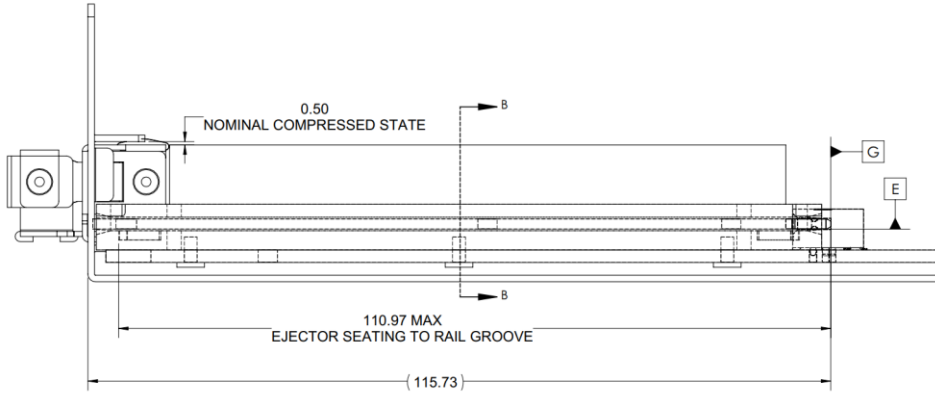
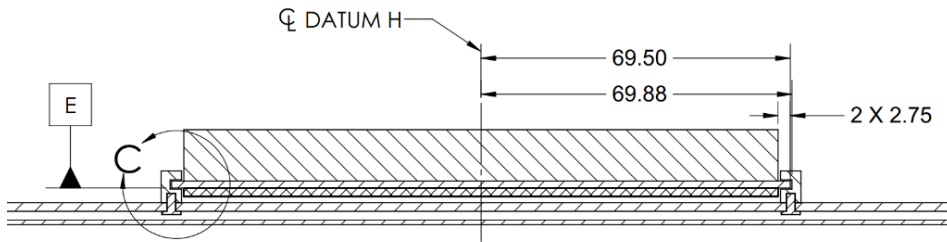
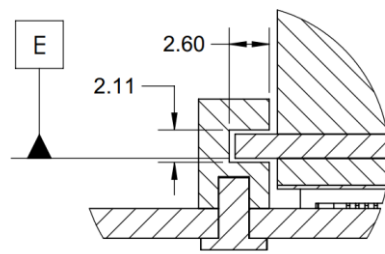


Figure 68: LFF Baseboard Chassis CTF Dimensions (Rail Guide View)



SECTION B-B

Figure 69: LFF Baseboard Chassis CTF Dimensions (Rail Guide – Detail C)



DETAIL C

Open Compute Project • OCP NIC 3.0

Version ~~1.2.1 - DRAFT~~ 2.0

The right angle and straddle mount card guides are identical between the SFF, TSFF and LFF. The card guide models are included in the 3D CAD packages and may be downloaded from the OCP NIC 3.0 Wiki site: <http://www.opencompute.org/wiki/Server/Mezz>.

2.9 Labeling Requirements

OCP NIC 3.0 cards shall implement all (or a subset of) label items listed below as required by each customer. All labels shall be placed on the exposed face of the insulator and within their designated zones. All labels shall be placed within the insulator edge and insulator bend lines to prevent labels from peeling or interfering with the faceplate, chassis card guides and card gold finger edge.

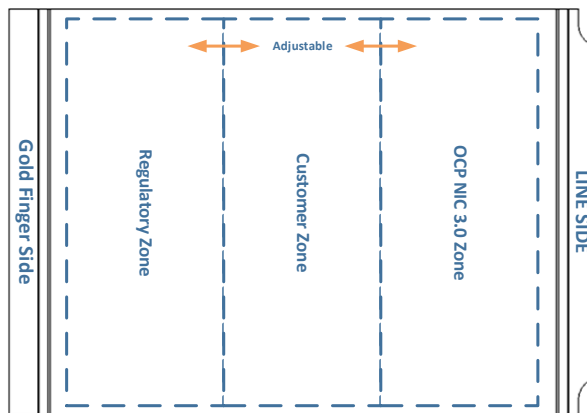
The insulator shall be divided into three different zones:

- **Regulatory Zone** – Used for all regulatory markings and filing numbers
- **Customer Zone** – Used for manufacturer markings or any ODM specific labels
- **OCP NIC 3.0 Zone** – Used for MAC addresses, part number labels and optionally the board serial number label if there are no manufacturer requirements to place it on the primary side

Notes:

- Some NIC vendor(s) may require serial number labels to be placed on the primary side of the PBA. This is permitted but it is up to the NIC vendor(s) to find the appropriate location(s) to affix the label. If a label is to be adhered to the PCB, then the label must be ESD safe as defined by ANSI/ESD S541-2008 (between $10^4 \Omega$ and $10^{11} \Omega$).
- Regulatory marks may be printed on the insulator or affixed via a label
- Each zone size shall be adjustable to accommodate each vendor's labeling requirements
- All labels shall be oriented and readable in the same direction. The readable direction should be with the line side I/O interfaces facing "up"
- Additional labels may be placed on the primary side or on the PCB itself. This is up to the NIC vendor(s) to find the appropriate location(s)

Figure 70: SFF, TSFF Label Area Example



2.9.1 General Guidelines for Label Contents

Each board shall have a unique label for identification. The label information shall be both in human readable and machine readable formats (linear or 2D data matrix). The labels may include:

- Serial number
- Part Number
- MAC Address
- Manufacturing Date
- Manufacturing Site Information

Barcode Requirements

- Linear Barcodes
- Code 93, Code 128 Auto or Code 128 Subset B
- Minimum narrow bar width $X \geq 5$ mil (0.127 mm)
- 2D data matrix
- Data matrix shall use ECC200 error correction
- Minimum cell size $X \geq 10$ mil (0.254 mm)
- All linear barcode and data matrix labels shall meet the contrast and print growth requirements per ISO/IEC 16022
- All linear barcode and data matrix labels shall have a quality level C or higher per ISO/IER 15415
- All linear barcode and data matrix labels shall define a minimum Quiet Zone (QZ) to ensure the label is correctly registered by the scanner per ISO/IEC 15415
- Linear barcode labels shall use a QZ that is 10 times the width of the narrowest bar or 1/8th inch, whichever is greater
- Data matrix labels shall have a Quiet Zone (QZ) that is at least one module (in the X-dimension) around the perimeter of the data matrix
- Multiple Serial Numbers, MAC address may exist in one 2D data matrix, each separated by a comma

Human Readable Font

- Arial or printer font equivalent
- Minimum 5 point font size. 3 point font is acceptable when using 600 DPI printers
- Text must be easily legible under normal lighting 6-to-8 inches away

The label size and typeface may vary based on each vendor and/or customer's label content and requirements.

2.9.2 MAC Address Labeling Requirements

For an OCP NIC 3.0 card with m line side interfaces and n RBT management interfaces, the MAC address label shall list the MAC addresses in sequential order starting with line side port 1 to port m followed by the controller #0 MAC address to controller n . For cards that support multi-host configurations, the label shall associate each MAC address with a host number. The examples below show the MAC addresses presented as a single column, for labels with many MAC addresses, the label may also be formatted in multiple columns for greater readability. Labels may optionally use ellipses for the human readable text to individually indicate a range of Port and ME MAC addresses. In all cases, the 2D data matrix shall include all the card assigned MAC addresses.

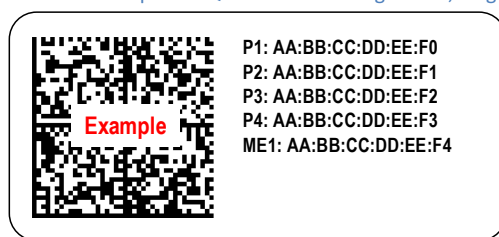
2.9.2.1 MAC Address Label Example 1 – Quad Port with Single Host, Single Managed Controller

As an example, the label content of a quad SFP OCP NIC 3.0 card with a single management MAC address shall be constructed to show human readable data per the Label Data column of Table 11. The constructed label is shown in Figure 71. For each human readable line, there is a MAC prefix “Px:” for a line side Port, or “MEx:” for a managed controller instance, followed by the MAC address. The port/controller association for each row is shown in the far right column.

Table 11: MAC Address Label Example 1 – Quad Port with Single Host, Single Managed Controller

| Label Data | MAC Prefix | MAC Address | Association |
|------------------------|------------|-------------------|---------------|
| P1: AA:BB:CC:DD:EE:F0 | P1: | AA:BB:CC:DD:EE:F0 | Port 1 |
| P2: AA:BB:CC:DD:EE:F1 | P2: | AA:BB:CC:DD:EE:F1 | Port 2 |
| P3: AA:BB:CC:DD:EE:F2 | P3: | AA:BB:CC:DD:EE:F2 | Port 3 |
| P4: AA:BB:CC:DD:EE:F3 | P4: | AA:BB:CC:DD:EE:F3 | Port 4 |
| ME1: AA:BB:CC:DD:EE:F4 | ME1: | AA:BB:CC:DD:EE:F4 | Controller #0 |

Figure 71: MAC Address Label Example 1 – Quad Port with Single Host, Single Managed Controller



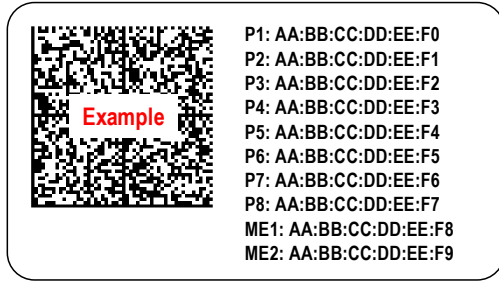
2.9.2.2 MAC Address Label Example 2 – Octal Port with Single Host, Dual Managed Controllers

As a second example, the label content of an octal port (2xQSFP with “breakout” support) OCP NIC 3.0 card with two managed silicon instances is constructed per Table 12. The constructed label is shown in Figure 72. The MAC address label shall also list the four MAC addresses associated with QSFP lanes [1:4] for QSFP connectors that allow “breakout” modes. The Host-MAC address presentation may also be formatted horizontally for easier readability.

Table 12: MAC Address Label Example 2 – Octal Port with Single Host, Dual Managed Controller

| Label Data | MAC Prefix | MAC Address | Association |
|------------------------|------------|-------------------|---------------|
| P1: AA:BB:CC:DD:EE:F0 | P1: | AA:BB:CC:DD:EE:F0 | QSFP1, Port 1 |
| P2: AA:BB:CC:DD:EE:F1 | P2: | AA:BB:CC:DD:EE:F1 | QSFP1, Port 2 |
| P3: AA:BB:CC:DD:EE:F2 | P3: | AA:BB:CC:DD:EE:F2 | QSFP1, Port 3 |
| P4: AA:BB:CC:DD:EE:F3 | P4: | AA:BB:CC:DD:EE:F3 | QSFP1, Port 4 |
| P5: AA:BB:CC:DD:EE:F4 | P5: | AA:BB:CC:DD:EE:F4 | QSFP2, Port 5 |
| P6: AA:BB:CC:DD:EE:F5 | P6: | AA:BB:CC:DD:EE:F5 | QSFP2, Port 6 |
| P7: AA:BB:CC:DD:EE:F6 | P7: | AA:BB:CC:DD:EE:F6 | QSFP2, Port 7 |
| P8: AA:BB:CC:DD:EE:F7 | P8: | AA:BB:CC:DD:EE:F7 | QSFP2, Port 8 |
| ME1: AA:BB:CC:DD:EE:F8 | ME1: | AA:BB:CC:DD:EE:F8 | Controller #0 |
| ME2: AA:BB:CC:DD:EE:F9 | ME2: | AA:BB:CC:DD:EE:F9 | Controller #1 |

Figure 72: MAC Address Label Example 2 – Octal Port with Single Host, Dual Managed Controller



2.9.2.3 MAC Address Label Example 3 – Quad Port with Dual Hosts, Dual Managed Controllers

For multi-host implementations, each MAC address shall be prefixed with the host association “Hx” prior to the port number, where x represents the host number. An example of this is shown in Table 13 and Figure 73.

Table 13: MAC Address Label Example 3 – Quad Port with Dual Hosts, Dual Managed Controller

| Label Data | Host | MAC Prefix | MAC Address | Association |
|------------------------|------|------------|-------------------|---------------|
| P1: AA:BB:CC:DD:EE:F0 | H1 | P1: | AA:BB:CC:DD:EE:F0 | Port 1 |
| P2: AA:BB:CC:DD:EE:F1 | H1 | P2: | AA:BB:CC:DD:EE:F1 | Port 2 |
| P3: AA:BB:CC:DD:EE:F2 | H2 | P3: | AA:BB:CC:DD:EE:F2 | Port 3 |
| P4: AA:BB:CC:DD:EE:F3 | H2 | P4: | AA:BB:CC:DD:EE:F3 | Port 4 |
| ME1: AA:BB:CC:DD:EE:F4 | n/a | ME1: | AA:BB:CC:DD:EE:F4 | Controller #0 |
| ME2: AA:BB:CC:DD:EE:F5 | n/a | ME2: | AA:BB:CC:DD:EE:F5 | Controller #1 |

Figure 73: MAC Address Label Example 3 – Quad Port with Dual Hosts, Dual Managed Controllers



2.9.2.4 MAC Address Label Example 4 – Single Port with Quad Host, Single Managed Controller

The following example shows a single port device with quad hosts. To conserve space on the MAC address label, this example only shows the MAC addresses for Port 1 through Port 4. The MAC address for each managed host is P_x+1. This is shown in Table 14 and Figure 74.

Table 14: MAC Address Label Example 4 – Single Port with Quad Host, Single Managed Controller

| Label Data | Host | MAC Prefix | MAC Address | Association |
|------------------------|------|------------|-------------------|-------------|
| P1: AA:BB:CC:DD:EE:F0 | H1 | P1: | AA:BB:CC:DD:EE:F0 | Port 1 |
| ME1: AA:BB:CC:DD:EE:F1 | ME1 | P1: | AA:BB:CC:DD:EE:F1 | Port 1 |
| P2: AA:BB:CC:DD:EE:F2 | H2 | P1: | AA:BB:CC:DD:EE:F2 | Port 1 |
| ME2: AA:BB:CC:DD:EE:F3 | ME2 | P1: | AA:BB:CC:DD:EE:F3 | Port 1 |
| P3: AA:BB:CC:DD:EE:F4 | H3 | P1: | AA:BB:CC:DD:EE:F4 | Port 1 |
| ME3: AA:BB:CC:DD:EE:F5 | ME3 | P1: | AA:BB:CC:DD:EE:F5 | Port 1 |
| P4: AA:BB:CC:DD:EE:F6 | H4 | P1: | AA:BB:CC:DD:EE:F6 | Port 1 |
| ME4: AA:BB:CC:DD:EE:F7 | ME4 | P1: | AA:BB:CC:DD:EE:F7 | Port 1 |

Figure 74: MAC Address Label Example 4 – Single Port with Quad Host, Single Managed Controller

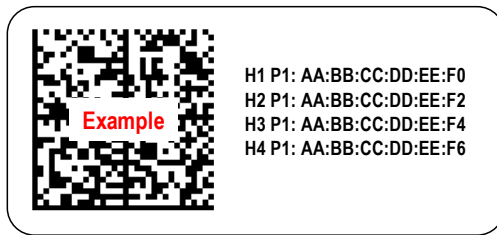


Table 15: MAC Address Label Example 5 – Octal Port with Single Host, Octal Managed Controller

| Label Data | MAC Prefix | MAC Address | Association |
|------------------------|------------|-------------------|-------------|
| P1: AA:BB:CC:DD:EE:F0 | P1: | AA:BB:CC:DD:EE:F0 | Port 1 |
| P8: AA:BB:CC:DD:EE:F7 | P8: | AA:BB:CC:DD:EE:F7 | Port 8 |
| ME1: AA:BB:CC:DD:EE:F8 | ME1: | AA:BB:CC:DD:EE:F8 | P1 |
| ME8: AA:BB:CC:DD:EE:FF | ME8: | AA:BB:CC:DD:EE:FF | P8 |

Figure 75: MAC Address Label Example 5 – Octal Port with Single Host, Octal Managed Controller



Figure 75 illustrates the use of ellipses in the human readable text to individually indicate a range of Port and Management MAC addresses. In this example, the 2D data matrix shall contain all 16 MAC addresses.

2.10 Mechanical CAD Package Examples

Typical OCP NIC 3.0 implementation examples are included in the 3D CAD package. The purpose of these examples is to demonstrate the implementation feasibility. Additional use cases beyond the implementation examples are possible as long they adhere to the OCP NIC 3.0 specification.

Note: For brevity, references to QSFP+, and QSFP28 shall be referred to as QSFP in this document. Similarly, references to SFP+, and SFP28 shall be referred to as SFP.

The 3D CAD files may be obtained from the OCP NIC 3.0 Wiki:
<http://www.opencompute.org/wiki/Server/Mezz>

Table 16: NIC Implementation Examples and 3D CAD

| Implementation Example | 3D CAD File name |
|---------------------------------|---|
| SFF Single/Dual QSFP ports | 01_nic_v3_sff2q_1tab_asm.stp 01_nic_v3_sff2q_latch_asm.stp |
| SFF Single/Dual SFP ports | N/A |
| SFF Quad SFP ports | 01_nic_v3_sff4s_1tab_asm.stp 01_nic_v3_sff4s_latch_asm.stp |
| SFF Quad 10GBASE-T ports | 01_nic_v3_sff4r_1tab_asm.stp 01_nic_v3_sff4r_latch_asm.stp |
| TSFF generic faceplate assembly | TSFF_Pull_Tab_20210527.stp TSFF_Latch_20210527.stp TSFF_Internal_Latch_20210527.Stp |
| LFF Single/Dual QSFP ports | 01_nic_v3_lff2q_asm.stp |
| LFF Single/Dual SFP ports | N/A |
| LFF Quad SFP ports | 01_nic_v3_lff4s_asm.stp |
| LFF Quad 10GBASE-T ports | 01_nic_v3_lff4r_asm.stp |

3 Electrical Interface Definition – Card Edge and Baseboard

3.1 Card Edge Gold Finger Requirements

The OCP NIC 3.0 cards are compliant to the SFF-TA-1002 specification with respect to the gold fingers and connectors.

SFF and TSFF cards fit in the Primary Connector. Primary Connector compliant cards are 76 mm x 115 mm and may implement the full 168-pins. The Primary Connector cards may optionally implement a subset of gold finger pins if there is a reduced PCIe width requirement (such as 1 x8 and below). In this case, the card edge gold finger may implement a 2C+ design. The overall board thickness is 1.57 mm. The gold finger dimensions for the Primary Connector compliant cards are shown below.

LFF cards support up to a x32 PCIe implementation and may use both the Primary 4C+and Secondary 4C Connectors. LFF cards may implement a reduced PCIe lane count and optionally implement only the Primary Connector.

Note: The “B” pins on the connector are associated with the top side of the OCP NIC 3.0 card. The “A” pins on the connector are associated with the bottom side of the OCP NIC 3.0 card. The A and B side pins are physically on top of each other with zero x-axis offset.

Figure 76: SFF, TSFF Primary Connector Gold Finger Dimensions – x16 – Top Side (“B” Pins)

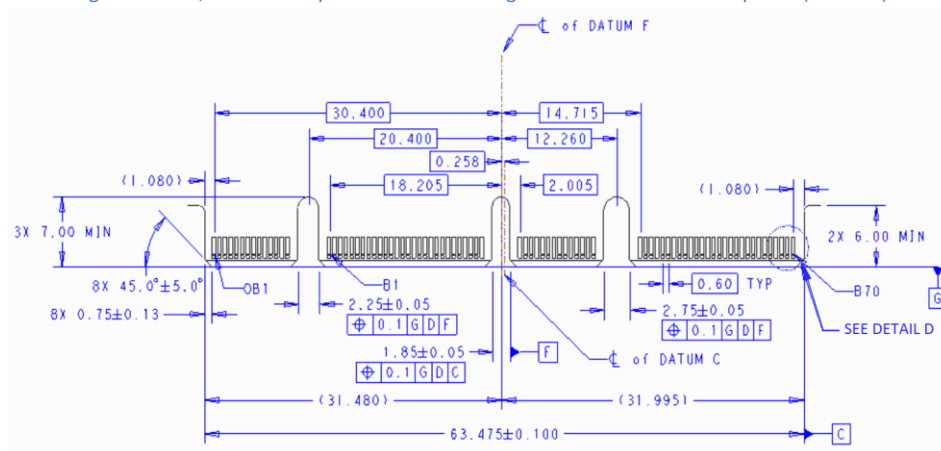


Figure 77: SFF, TSFF Primary Connector Card Profile Dimensions

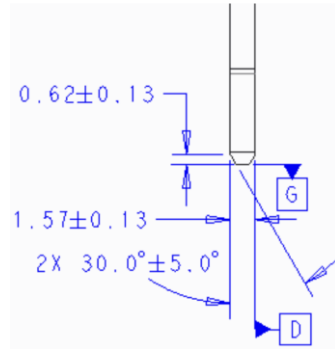


Figure 78: SFF, TSFF Primary Connector Gold Finger - Detail D

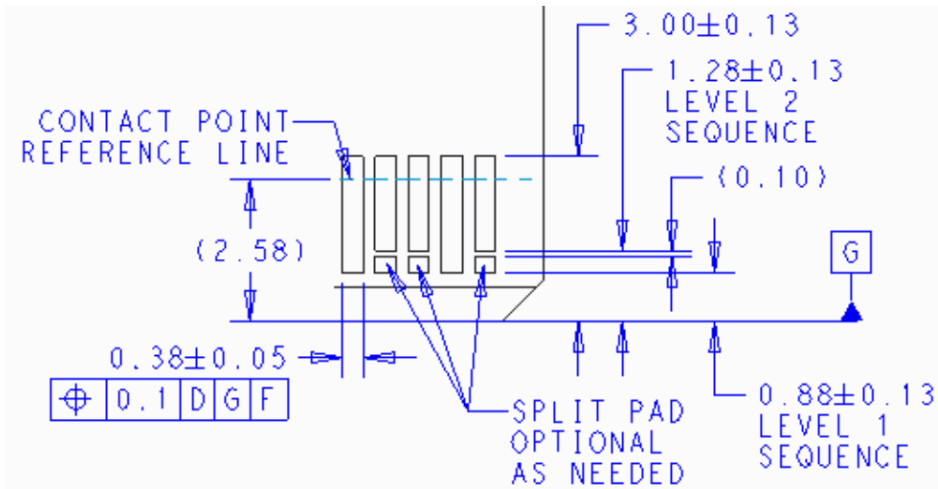


Figure 79: LFF Gold Finger Dimensions – x32 – Top Side (“B” Pins)

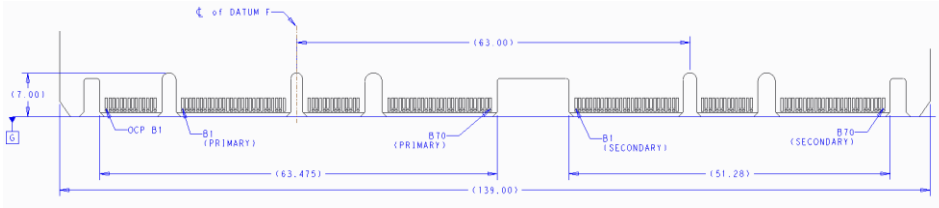
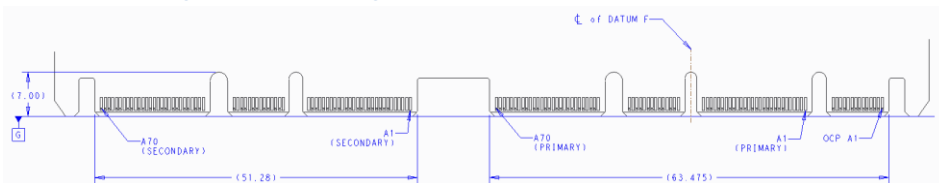


Figure 80: LFF Gold Finger Dimensions – x32 – Bottom Side (“A” Pins)



3.1.1 Gold Finger Mating Sequence

Per the SFF-TA-1002 specification, the Primary and Secondary Connectors are protocol agnostic and are optimized for high speed differential pairs. For use in the OCP NIC 3.0 application, some pin locations are used for single ended control nets or power and would benefit from a shorter pin length for staggering. As such, the required OCP NIC 3.0 card gold finger staging is shown in Table 17 and Table 18 for a two stage, first-mate, last-break functionality. The two-stage finger length is a normative requirement for the OCP NIC 3.0 card. The host connectors have a single stage mating and do not implement different pin lengths.

The AIC Plug (Free) side refers to the OCP NIC 3.0 card gold fingers; the receptacle (Fixed) side refers to the physical connector on the host platform. This table is based on the SFF-TA-1002 Table A-1 with modifications for OCP NIC 3.0. Refer to the mechanical drawings for pin the first-mate and second-mate lengths.

Note: Pin names in Table 17 and Table 18 are used for first mate/second mate reference only. Full pin definitions are described in Sections 3.3 and 3.4.

Table 17: Contact Mating Positions for the Primary Connector

| Side B | | | Side A | | | |
|-------------------------|----------------------|--------------------|-------------------------|----------------------|--------------------|--|
| Gold Finger Side (Free) | | Receptacle (Fixed) | Gold Finger Side (Free) | | Receptacle (Fixed) | |
| 2 nd Mate | 1 st Mate | | 2 nd Mate | 1 st Mate | | |
| OCB B1 | NIC_PWR_GOOD | | OCB A1 | PERST2# | | |
| OCB B2 | MAIN_PWR_EN | | OCB A2 | PERST3# | | |
| OCB B3 | SCAN_LD# | | OCB A3 | WAKE# | | |
| OCB B4 | SCAN_DATA_IN | | OCB A4 | RBT_ARB_IN | | |
| OCB B5 | SCAN_DATA_OUT | | OCB A5 | RBT_ARB_OUT | | |
| OCB B6 | SCAN_CLK | | OCB A6 | SLOT_ID1 | | |
| OCB B7 | SLOT_ID0 | | OCB A7 | RBT_TX_EN | | |
| OCB B8 | RBT_RXD1 | | OCB A8 | RBT_TXD1 | | |
| OCB B9 | RBT_RXD0 | | OCB A9 | RBT_TXD0 | | |
| OCB B10 | GND | | OCB A10 | GND | | |
| OCB B11 | REFCLKn2 | | OCB A11 | REFCLKn3 | | |
| OCB B12 | REFCLKp2 | | OCB A12 | REFCLKp3 | | |

| Side B | | | | Side A | | | |
|-------------------------|----------------------|--|-----------------------|-------------------------|----------------------|--|-----------------------|
| Gold Finger Side (Free) | | | Receptacle (Fixed) | Gold Finger Side (Free) | | | Receptacle (Fixed) |
| 2 nd Mate | 1 st Mate | | | 2 nd Mate | 1 st Mate | | |
| OCP B13 | GND | | | OCP A13 | GND | | |
| OCP B14 | RBT_CRS_DV | | | OCP A14 | RBT_CLK_IN | | |
| Mechanical Key | | | | | | | |
| B1 | +12V_EDGE | | | A1 | GND | | |
| B2 | +12V_EDGE | | | A2 | GND | | |
| B3 | +12V_EDGE | | | A3 | GND | | |
| B4 | +12V_EDGE | | | A4 | GND | | |
| B5 | +12V_EDGE | | | A5 | GND | | |
| B6 | +12V_EDGE | | | A6 | GND | | |
| B7 | BIF0# | | | A7 | SMCLK | | |
| B8 | BIF1# | | | A8 | SMDAT | | |
| B9 | BIF2# | | | A9 | SMRST# | | |
| B10 | PRSTO# | | | A10 | PRSNTA# | | |
| B11 | +3.3V_EDGE | | | A11 | PRST1# | | |
| B12 | AUX_PWR_EN | | | A12 | PRSNTB2# | | |
| B13 | GND | | | A13 | GND | | |
| B14 | REFCLKn0 | | | A14 | REFCLKn1 | | |
| B15 | REFCLKp0 | | | A15 | REFCLKp1 | | |
| B16 | GND | | | A16 | GND | | |
| B17 | PETn0 | | | A17 | PERn0 | | |
| B18 | PETp0 | | | A18 | PERp0 | | |
| B19 | GND | | | A19 | GND | | |
| B20 | PETn1 | | | A20 | PERn1 | | |
| B21 | PETp1 | | | A21 | PERp1 | | |
| B22 | GND | | | A22 | GND | | |
| B23 | PETn2 | | | A23 | PERn2 | | |
| B24 | PETp2 | | | A24 | PERp2 | | |
| B25 | GND | | | A25 | GND | | |
| B26 | PETn3 | | | A26 | PERn3 | | |
| B27 | PETp3 | | | A27 | PERp3 | | |
| B28 | GND | | | A28 | GND | | |
| Mechanical Key | | | | | | | |
| B29 | GND | | | A29 | GND | | |
| B30 | PETn4 | | | A30 | PERn4 | | |
| B31 | PETp4 | | | A31 | PERp4 | | |
| B32 | GND | | | A32 | GND | | |
| B33 | PETn5 | | | A33 | PERn5 | | |
| B34 | PETp5 | | | A34 | PERp5 | | |
| B35 | GND | | | A35 | GND | | |
| B36 | PETn6 | | | A36 | PERn6 | | |
| B37 | PETp6 | | | A37 | PERp6 | | |
| B38 | GND | | | A38 | GND | | |
| B39 | PETn7 | | | A39 | PERn7 | | |
| B40 | PETp7 | | | A40 | PERp7 | | |
| B41 | GND | | | A41 | GND | | |
| B42 | PRSNTB0# | | | A42 | PRSNTB1# | | |
| Mechanical Key | | | | | | | |
| B43 | GND | | | A43 | GND | | |
| B44 | PETn8 | | | A44 | PERn8 | | |
| B45 | PETp8 | | | A45 | PERp8 | | |
| B46 | GND | | | A46 | GND | | |
| B47 | PETn9 | | | A47 | PERn9 | | |
| B48 | PETp9 | | | A48 | PERp9 | | |
| B49 | GND | | | A49 | GND | | |
| B50 | PETn10 | | | A50 | PERn10 | | |
| B51 | PETp10 | | | A51 | PERp10 | | |
| B52 | GND | | | A52 | GND | | |
| B53 | PETn11 | | | A53 | PERn11 | | |
| B54 | PETp11 | | | A54 | PERp11 | | |
| B55 | GND | | | A55 | GND | | |
| B56 | PETn12 | | | A56 | PERn12 | | |
| B57 | PETp12 | | | A57 | PERp12 | | |
| B58 | GND | | | A58 | GND | | |
| B59 | PETn13 | | | A59 | PERn13 | | |
| B60 | PETp13 | | | A60 | PERp13 | | |
| B61 | GND | | | A61 | GND | | |
| B62 | PETn14 | | | A62 | PERn14 | | |
| B63 | PETp14 | | | A63 | PERp14 | | |

| Side B | | | | Side A | | | |
|-------------------------|----------------------|--|--------------------|-------------------------|----------------------|--|--------------------|
| Gold Finger Side (Free) | | | Receptacle (Fixed) | Gold Finger Side (Free) | | | Receptacle (Fixed) |
| 2 nd Mate | 1 st Mate | | | 2 nd Mate | 1 st Mate | | |
| B64 | GND | | A64 | GND | | | |
| B65 | PETn15 | | A65 | PERn15 | | | |
| B66 | PETp15 | | A66 | PERp15 | | | |
| B67 | GND | | A67 | GND | | | |
| B68 | RFU1, N/C | | A68 | USB_DATn | | | |
| B69 | RFU2, N/C | | A69 | USB_DATp | | | |
| B70 | PRSNB3# | | A70 | PWRBRK0# | | | |

Table 18: Contact Mating Positions for the Secondary Connector

| Side B | | | | Side A | | | |
|-------------------------|----------------------|--|--------------------|-------------------------|----------------------|--|--------------------|
| Gold Finger Side (Free) | | | Receptacle (Fixed) | Gold Finger Side (Free) | | | Receptacle (Fixed) |
| 2 nd Mate | 1 st Mate | | | 2 nd Mate | 1 st Mate | | |
| B1 | +12V_EDGE | | A1 | GND | | | |
| B2 | +12V_EDGE | | A2 | GND | | | |
| B3 | +12V_EDGE | | A3 | GND | | | |
| B4 | +12V_EDGE | | A4 | GND | | | |
| B5 | +12V_EDGE | | A5 | GND | | | |
| B6 | +12V_EDGE | | A6 | GND | | | |
| B7 | BIF0# | | A7 | SMCLK | | | |
| B8 | BIF1# | | A8 | SMDAT | | | |
| B9 | BIF2# | | A9 | SMRST# | | | |
| B10 | PERST4# | | A10 | PRNSTA# | | | |
| B11 | +3.3V_EDGE | | A11 | PERST5# | | | |
| B12 | AUX_PWR_EN | | A12 | PRSNB2# | | | |
| B13 | GND | | A13 | GND | | | |
| B14 | REFCLKn4 | | A14 | REFCLKn5 | | | |
| B15 | REFCLKp4 | | A15 | REFCLKp5 | | | |
| B16 | GND | | A16 | GND | | | |
| B17 | PETn16 | | A17 | PERn16 | | | |
| B18 | PETp16 | | A18 | PERp16 | | | |
| B19 | GND | | A19 | GND | | | |
| B20 | PETn17 | | A20 | PERn17 | | | |
| B21 | PETp17 | | A21 | PERp17 | | | |
| B22 | GND | | A22 | GND | | | |
| B23 | PETn18 | | A23 | PERn18 | | | |
| B24 | PETp18 | | A24 | PERp18 | | | |
| B25 | GND | | A25 | GND | | | |
| B26 | PETn19 | | A26 | PERn19 | | | |
| B27 | PETp19 | | A27 | PERp19 | | | |
| B28 | GND | | A28 | GND | | | |
| Mechanical Key | | | | | | | |
| B29 | GND | | A29 | GND | | | |
| B30 | PETn20 | | A30 | PERn20 | | | |
| B31 | PETp20 | | A31 | PERp20 | | | |
| B32 | GND | | A32 | GND | | | |
| B33 | PETn21 | | A33 | PERn21 | | | |
| B34 | PETp21 | | A34 | PERp21 | | | |
| B35 | GND | | A35 | GND | | | |
| B36 | PETn22 | | A36 | PERn22 | | | |
| B37 | PETp22 | | A37 | PERp22 | | | |
| B38 | GND | | A38 | GND | | | |
| B39 | PETn23 | | A39 | PERn23 | | | |
| B40 | PETp23 | | A40 | PERp23 | | | |
| B41 | GND | | A41 | GND | | | |
| B42 | PRSNB0# | | A42 | PRSNB1# | | | |
| Mechanical Key | | | | | | | |
| B43 | GND | | A43 | GND | | | |
| B44 | PETn24 | | A44 | PERn24 | | | |
| B45 | PETp24 | | A45 | PERp24 | | | |
| B46 | GND | | A46 | GND | | | |
| B47 | PETn25 | | A47 | PERn25 | | | |
| B48 | PETp25 | | A48 | PERp25 | | | |
| B49 | GND | | A49 | GND | | | |
| B50 | PETn26 | | A50 | PERn26 | | | |
| B51 | PETp26 | | A51 | PERp26 | | | |
| B52 | GND | | A52 | GND | | | |

| Side B | | | Side A | | | |
|-------------------------|----------------------|-----------------------|-------------------------|----------------------|-----------------------|--|
| Gold Finger Side (Free) | | Receptacle (Fixed) | Gold Finger Side (Free) | | Receptacle (Fixed) | |
| 2 nd Mate | 1 st Mate | | 2 nd Mate | 1 st Mate | | |
| B53 | PETn27 | | A53 | PERn27 | | |
| B54 | PETp27 | | A54 | PERp27 | | |
| B55 | GND | | A55 | GND | | |
| B56 | PETn28 | | A56 | PERn28 | | |
| B57 | PETp28 | | A57 | PERp28 | | |
| B58 | GND | | A58 | GND | | |
| B59 | PETn29 | | A59 | PERn29 | | |
| B60 | PETp29 | | A60 | PERp29 | | |
| B61 | GND | | A61 | GND | | |
| B62 | PETn30 | | A62 | PERn30 | | |
| B63 | PETp30 | | A63 | PERp30 | | |
| B64 | GND | | A64 | GND | | |
| B65 | PETn31 | | A65 | PERn31 | | |
| B66 | PETp31 | | A66 | PERp31 | | |
| B67 | GND | | A67 | GND | | |
| B68 | RFU3, N/C | | A68 | UART_RX | | |
| B69 | RFU4, N/C | | A69 | UART_TX | | |
| B70 | PRSNB3# | | A70 | PWRBRK1# | | |

3.2 Baseboard Connector Requirements

The OCP NIC 3.0 connectors are compliant to the 4C+ and 4C connectors as defined in the SFF-TA-1002 specification for a right angle or straddle mount form factor. The Primary Connector is a 4C+ implementation with 168-pins. The Secondary Connector is a 4C implementation with 140-pins. Both the Primary and Secondary Connectors includes support for up to 32 differential pairs to support a x16 PCIe connection. Each connector also provides 6 pins of +12V_EDGE, and 1 pin of +3.3V_EDGE for power. This implementation is common between both the Primary and Secondary Connectors. In addition, the 4C+ implementation of the Primary Connector has a 28-pin OCP Bay used for management and support for up to a 4 x2 and 4 x4 multi-host configurations on the Primary Connector. The Primary and Secondary Connector drawings are shown below.

All diagram units are in mm unless otherwise noted.

3.2.1 Right Angle Connector

The following offset and height options are available for the right-angle Primary and Secondary Connectors.

Table 19: Right Angle Connector Options

| Name | Pins | Style and Baseboard Thickness | Offset (mm) |
|--------------------------|----------|-------------------------------|-------------|
| Primary Connector – 4C+ | 168 pins | Right Angle | 4.05 mm |
| Secondary Connector – 4C | 140 pins | Right Angle | 4.05 mm |

Figure 81: 168-pin Base Board Primary Connector – Right Angle

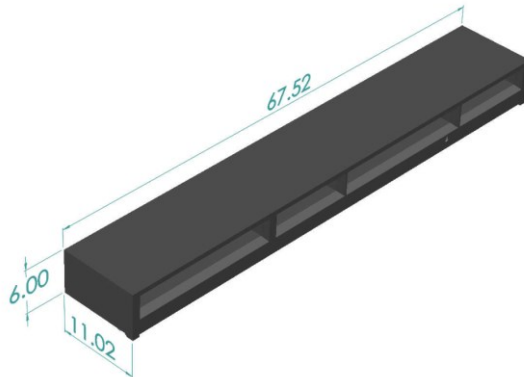
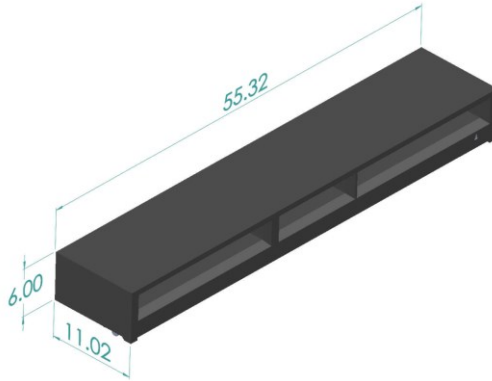


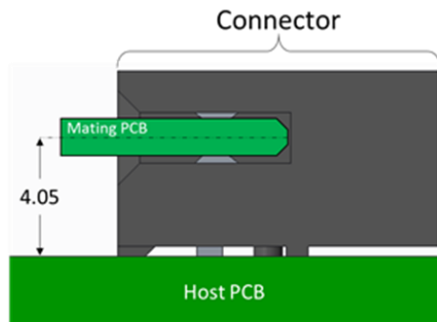
Figure 82: 140-pin Base Board Secondary Connector – Right Angle



3.2.2 Right Angle Offset

The OCP NIC 3.0 right angle connectors have a 4.05 mm offset from the baseboard. This is shown in Figure 83.

Figure 83: OCP NIC 3.0 Card and Host Offset for Right Angle Connectors



3.2.3 Straddle Mount Connector

The following offset and height options are available for the straddle mount Primary and Secondary Connectors.

Table 20: Straddle Mount Connector Options

| Name | Pins | Style and Baseboard Thickness | Offset (mm) |
|--------------------------|----------|-------------------------------|-----------------|
| Primary Connector – 4C+ | 168 pins | Straddle Mount for 0.062" | Coplanar (0 mm) |
| Primary Connector – 4C+ | 168 pins | Straddle Mount for 0.076" | -0.3 mm |
| Primary Connector – 4C+ | 168 pins | Straddle Mount for 0.093" | Coplanar (0 mm) |
| Secondary Connector – 4C | 140 pins | Straddle Mount for 0.062" | Coplanar (0 mm) |
| Secondary Connector – 4C | 140 pins | Straddle Mount for 0.076" | -0.3 mm |
| Secondary Connector – 4C | 140 pins | Straddle Mount for 0.093" | Coplanar (0 mm) |

Figure 84: 168-pin Base Board Primary Connector – Straddle Mount

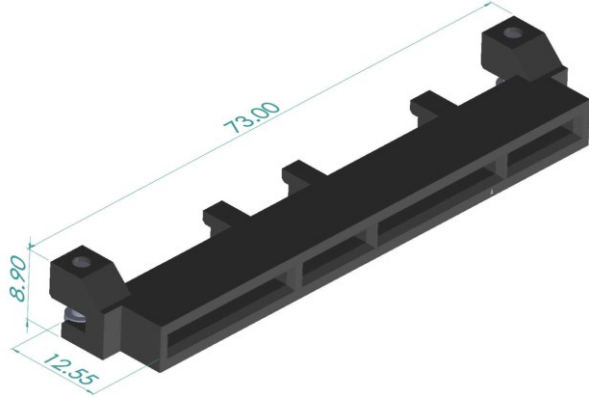
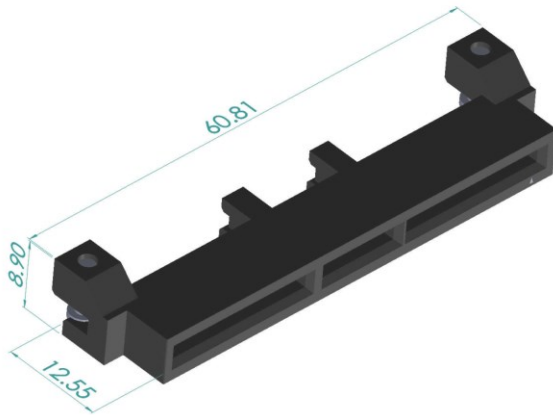


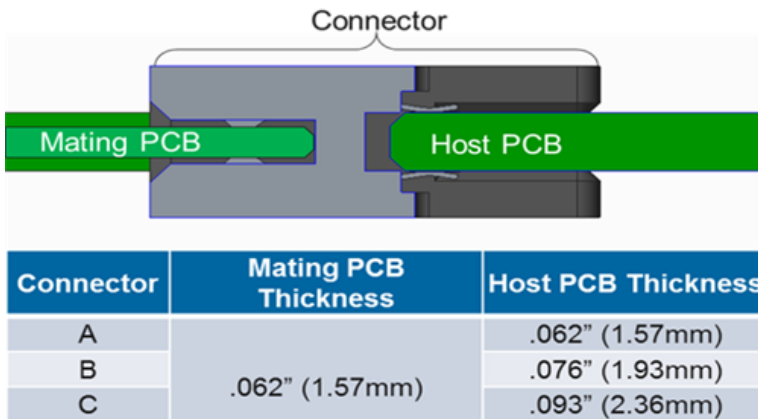
Figure 85: 140-pin Base Board Secondary Connector – Straddle Mount



3.2.4 Straddle Mount Offset and PCB Thickness Options

The OCP NIC 3.0 straddle mount connectors have three baseboard PCB thicknesses they can accept. The available options are shown in Figure 86. The thicknesses are 0.062", 0.076", and 0.093". These PCBs must be controlled to a thickness of $\pm 10\%$. These are available for both the Primary and Secondary Connector locations. At the time of this writing, the most used part is expected to be the 0.076" baseboard thickness.

Figure 86: OCP NIC 3.0 Card and Baseboard PCB Thickness Options for Straddle Mount Connectors



The connectors are capable of being used coplanar as shown in Figure 87. Additionally, the connectors are also capable of having a 0.3 mm offset from the centerline of the host board as shown in Figure 88.

Figure 87: 0 mm Offset (Coplanar) for 0.062" Thick Baseboards

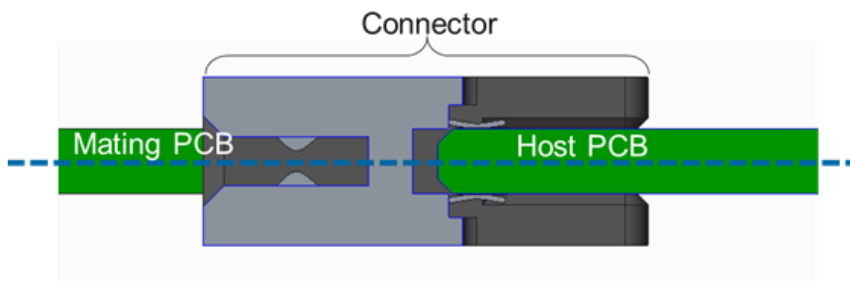
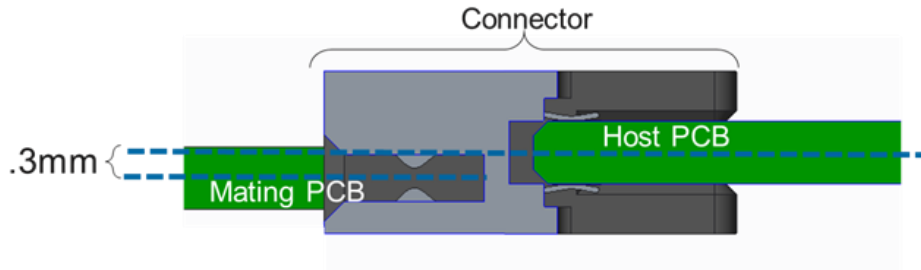


Figure 88: 0.3 mm Offset for 0.076" Thick Baseboards



3.2.5 LFF Connector Locations

In order to support the LFF, systems must locate the Primary and Secondary Connectors per the mechanical drawing shown in Figure 89 and Figure 90.

Figure 89: Primary and Secondary Connector Locations for LFF Support with Right Angle Connectors

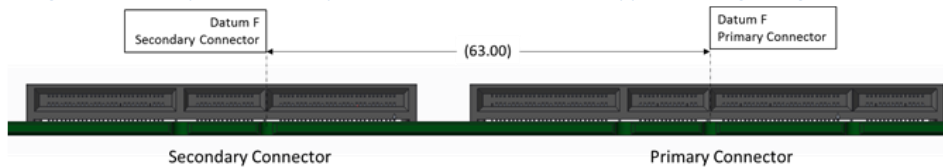
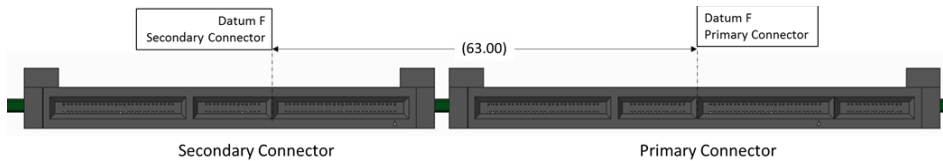


Figure 90: Primary and Secondary Connector Locations for LFF Support with Straddle Mount Connectors



3.3 Pin Definition

The pin definitions of an OCP NIC 3.0 card with up to a x32 PCIe interface are shown in Table 21 and Table 22. All signal directions are shown from the perspective of the baseboard.

A baseboard system may provide a combination of Primary Connectors only, or Primary and Secondary Connectors to support multiple sizes of OCP NIC 3.0 cards. Both connectors share common functionality with power, SMBus 2.0, x16 PCIe and bifurcation control. The Primary Connector 4C+ definition has an additional OCP Bay (pins OCP_A[1:14], OCP_B[1:14]) with additional REFCLKs for supporting up to four PCIe hosts, NC-SI over RBT connectivity and a Scan Chain for information exchange between the host and card. The NIC is required to implement the Scan Chain, while the baseboard may choose to optionally implement it. Depending on the baseboard form factor, multiple OCP NIC 3.0 compliant cards may be designed into the system.

The Primary and Secondary Connectors pins are shown in Section 3.4. The OCP Bay pins on the Primary Connector only are explicitly called out with the “OCP_” prefix in the pin location column.

Cards or systems that do not require the use of a PCIe x16 connection may optionally implement a subset of electrical connections as applicable to the design. For example, a x8 (or smaller) card using the first 8 PCIe lanes that is compliant with the Primary Connector pinout. Refer to Sections 3.1 and 3.2 for mechanical details. For these cases, the Primary Connector matches the 2C dimensions as defined in SFF-TA-1002.

In all cases, the physical baseboard connectors shall support x16 PCIe widths and must be implemented with the Primary (4C+) and Secondary (4C) connectors.

3.3.1 Primary Connector

Table 21: Primary Connector Pin Definition (x16) (4C+)

| Side B | | Side A | |
|----------------|---------------|-------------|---------|
| OCP_B1 | NIC_PWR_GOOD | PERST2# | OCP_A1 |
| OCP_B2 | MAIN_PWR_EN | PERST3# | OCP_A2 |
| OCP_B3 | SCAN_LD# | WAKE# | OCP_A3 |
| OCP_B4 | SCAN_DATA_IN | RBT_ARB_IN | OCP_A4 |
| OCP_B5 | SCAN_DATA_OUT | RBT_ARB_OUT | OCP_A5 |
| OCP_B6 | SCAN_CLK | SLOT_ID1 | OCP_A6 |
| OCP_B7 | SLOT_ID0 | RBT_TX_EN | OCP_A7 |
| OCP_B8 | RBT_RXD1 | RBT_TXD1 | OCP_A8 |
| OCP_B9 | RBT_RXD0 | RBT_TXD0 | OCP_A9 |
| OCP_B10 | GND | GND | OCP_A10 |
| OCP_B11 | REFCLKn2 | REFCLKn3 | OCP_A11 |
| OCP_B12 | REFCLKp2 | REFCLKp3 | OCP_A12 |
| OCP_B13 | GND | GND | OCP_A13 |
| OCP_B14 | RBT_CRS_DV | RBT_CLK_IN | OCP_A14 |
| Mechanical Key | | | |
| B1 | +12V_EDGE | GND | A1 |
| B2 | +12V_EDGE | GND | A2 |
| B3 | +12V_EDGE | GND | A3 |
| B4 | +12V_EDGE | GND | A4 |
| B5 | +12V_EDGE | GND | A5 |
| B6 | +12V_EDGE | GND | A6 |
| B7 | BIF0# | SMCLK | A7 |
| B8 | BIF1# | SMDAT | A8 |
| B9 | BIF2# | SMRST# | A9 |
| B10 | PERSTO# | PRSNTA# | A10 |
| B11 | +3.3V_EDGE | PERST1# | A11 |
| B12 | AUX_PWR_EN | PRSNB2# | A12 |
| B13 | GND | GND | A13 |
| B14 | REFCLKn0 | REFCLKn1 | A14 |
| B15 | REFCLKp0 | REFCLKp1 | A15 |
| B16 | GND | GND | A16 |
| B17 | PETn0 | PERn0 | A17 |
| B18 | PETp0 | PERp0 | A18 |
| B19 | GND | GND | A19 |
| B20 | PETn1 | PERn1 | A20 |
| B21 | PETp1 | PERp1 | A21 |
| B22 | GND | GND | A22 |

Primary Connector (4C+, x16, 168-pin OCP NIC 3.0 card with OCP Bay)

Primary Connector (2C+, x8, 112-pin OCP NIC 3.0 card with OCP bay)

| Side B | | Side A | |
|-----------------------|-----------|----------|-----|
| B23 | PETn2 | PERn2 | A23 |
| B24 | PETp2 | PERp2 | A24 |
| B25 | GND | GND | A25 |
| B26 | PETn3 | PERn3 | A26 |
| B27 | PETp3 | PERp3 | A27 |
| B28 | GND | GND | A28 |
| Mechanical Key | | | |
| B29 | GND | GND | A29 |
| B30 | PETn4 | PERn4 | A30 |
| B31 | PETp4 | PERp4 | A31 |
| B32 | GND | GND | A32 |
| B33 | PETn5 | PERn5 | A33 |
| B34 | PETp5 | PERp5 | A34 |
| B35 | GND | GND | A35 |
| B36 | PETn6 | PERn6 | A36 |
| B37 | PETp6 | PERp6 | A37 |
| B38 | GND | GND | A38 |
| B39 | PETn7 | PERn7 | A39 |
| B40 | PETp7 | PERp7 | A40 |
| B41 | GND | GND | A41 |
| B42 | PRSNB0# | PRSNB1# | A42 |
| Mechanical Key | | | |
| B43 | GND | GND | A43 |
| B44 | PETn8 | PERn8 | A44 |
| B45 | PETp8 | PERp8 | A45 |
| B46 | GND | GND | A46 |
| B47 | PETn9 | PERn9 | A47 |
| B48 | PETp9 | PERp9 | A48 |
| B49 | GND | GND | A49 |
| B50 | PETn10 | PERn10 | A50 |
| B51 | PETp10 | PERp10 | A51 |
| B52 | GND | GND | A52 |
| B53 | PETn11 | PERn11 | A53 |
| B54 | PETp11 | PERp11 | A54 |
| B55 | GND | GND | A55 |
| B56 | PETn12 | PERn12 | A56 |
| B57 | PETp12 | PERp12 | A57 |
| B58 | GND | GND | A58 |
| B59 | PETn13 | PERn13 | A59 |
| B60 | PETp13 | PERp13 | A60 |
| B61 | GND | GND | A61 |
| B62 | PETn14 | PERn14 | A62 |
| B63 | PETp14 | PERp14 | A63 |
| B64 | GND | GND | A64 |
| B65 | PETn15 | PERn15 | A65 |
| B66 | PETp15 | PERp15 | A66 |
| B67 | GND | GND | A67 |
| B68 | RFU1, N/C | USB_DATn | A68 |
| B69 | RFU2, N/C | USB_DATp | A69 |
| B70 | PRSNB3# | PWRBRK0# | A70 |

3.3.2 Secondary Connector

Table 22: Secondary Connector Pin Definition (x16) (4C)

| Side B | | Side A | | Secondary Connector (4C, x16, 140-pin OCP NIC 3.0 card) | |
|-----------------------|------------|----------|-----|---|--|
| B1 | +12V_EDGE | GND | A1 | | |
| B2 | +12V_EDGE | GND | A2 | | |
| B3 | +12V_EDGE | GND | A3 | | |
| B4 | +12V_EDGE | GND | A4 | | |
| B5 | +12V_EDGE | GND | A5 | | |
| B6 | +12V_EDGE | GND | A6 | | |
| B7 | BIFO# | SMCLK | A7 | | |
| B8 | BIF1# | SMDAT | A8 | | |
| B9 | BIF2# | SMRST# | A9 | | |
| B10 | PERST4# | PRSNTA# | A10 | | |
| B11 | +3.3V_EDGE | PERST5# | A11 | | |
| B12 | AUX_PWR_EN | PRSNTB2# | A12 | | |
| B13 | GND | GND | A13 | | |
| B14 | REFCLKn4 | REFCLKn5 | A14 | | |
| B15 | REFCLKp4 | REFCLKp5 | A15 | | |
| B16 | GND | GND | A16 | | |
| B17 | PETn16 | PERn16 | A17 | | |
| B18 | PETp16 | PERp16 | A18 | | |
| B19 | GND | GND | A19 | | |
| B20 | PETn17 | PERn17 | A20 | | |
| B21 | PETp17 | PERp17 | A21 | | |
| B22 | GND | GND | A22 | | |
| B23 | PETn18 | PERn18 | A23 | | |
| B24 | PETp18 | PERp18 | A24 | | |
| B25 | GND | GND | A25 | | |
| B26 | PETn19 | PERn19 | A26 | | |
| B27 | PETp19 | PERp19 | A27 | | |
| B28 | GND | GND | A28 | | |
| Mechanical Key | | | | | |
| B29 | GND | GND | A29 | | |
| B30 | PETn20 | PERn20 | A30 | | |
| B31 | PETp20 | PERp20 | A31 | | |
| B32 | GND | GND | A32 | | |
| B33 | PETn21 | PERn21 | A33 | | |
| B34 | PETp21 | PERp21 | A34 | | |
| B35 | GND | GND | A35 | | |
| B36 | PETn22 | PERn22 | A36 | | |
| B37 | PETp22 | PERp22 | A37 | | |
| B38 | GND | GND | A38 | | |
| B39 | PETn23 | PERn23 | A39 | | |
| B40 | PETp23 | PERp23 | A40 | | |
| B41 | GND | GND | A41 | | |
| B42 | PRSNTB0# | PRSNTB1# | A42 | | |
| Mechanical Key | | | | | |
| B43 | GND | GND | A43 | | |
| B44 | PETn24 | PERn24 | A44 | | |
| B45 | PETp24 | PERp24 | A45 | | |
| B46 | GND | GND | A46 | | |
| B47 | PETn25 | PERn25 | A47 | | |
| B48 | PETp25 | PERp25 | A48 | | |
| B49 | GND | GND | A49 | | |

| | Side B | Side A | |
|-----|-----------|----------|-----|
| B50 | PETn26 | PERn26 | A50 |
| B51 | PETp26 | PERp26 | A51 |
| B52 | GND | GND | A52 |
| B53 | PETn27 | PERn27 | A53 |
| B54 | PETp27 | PERp27 | A54 |
| B55 | GND | GND | A55 |
| B56 | PETn28 | PERn28 | A56 |
| B57 | PETp28 | PERp28 | A57 |
| B58 | GND | GND | A58 |
| B59 | PETn29 | PERn29 | A59 |
| B60 | PETp29 | PERp29 | A60 |
| B61 | GND | GND | A61 |
| B62 | PETn30 | PERn30 | A62 |
| B63 | PETp30 | PERp30 | A63 |
| B64 | GND | GND | A64 |
| B65 | PETn31 | PERn31 | A65 |
| B66 | PETp31 | PERp31 | A66 |
| B67 | GND | GND | A67 |
| B68 | RFU3, N/C | UART_RX | A68 |
| B69 | RFU4, N/C | UART_TX | A69 |
| B70 | PRSNB3# | PWRBRK1# | A70 |

3.4 Signal Descriptions

The pins shown in this section are common for both the Primary and Secondary Connectors unless otherwise noted. Pins that exist only for the Primary Connector OCP Bay are explicitly called out in the pin location column with the prefix “OCP_xxx”. USB is only defined on the Primary Connector. UART is only defined on the secondary connector. All pin directions are from the perspective of the baseboard.

Note 1: The OCP NIC 3.0 card shall implement protection methods to prevent leakage or low impedance paths between the V_{AUX} and V_{MAIN} power domains if a powered-down NIC is physically present in a powered-up baseboard. This specification provides example isolation implementations in the signal description text and appropriate figures. OCP NIC 3.0 implementers may choose to do a different implementation as long as the isolation requirements are met and the same result is achieved.

Note 2: The terms Aux Power Mode and Main Power Mode are used within this specification and define the corresponding ACPI power states of the system.

- Aux Power Mode corresponds to the S5 ACPI power state and may also include ACPI power states S3 or S4 depending on the implementation. In Aux Power Mode, AUX_PWR_EN==1, and MAIN_PWR_EN==0.
- Main Power Mode corresponds to the S0 ACPI power state on the system and may also correspond to ACPI power state S1 depending on the implementation. In Main Power Mode, AUX_PWR_EN==1, and MAIN_PWR_EN==1.

3.4.1 PCIe Interface Pins

This section provides the pin assignments for the PCIe interface signals. The PCIe signals have unique names on the Primary and Secondary connector. The Primary Connector uses the REFCLK[0:3], TX/RX[0:15], PERST[0:3] indices. The Secondary Connector uses the REFCLK[4:5], TX/RX[16:31] and

PERST[4:5] indices. Where applicable, the Primary/Secondary connector naming convention is shown as a pair. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0. Example connection diagrams for are shown in Section 3.6.

Table 23: Pin Descriptions – PCIe

| Signal Name (Primary / Secondary) | Pin # | Baseboard Direction | Signal Description |
|---|--------------------|------------------------|--|
| REFCLKn0/REFCLKn4 REFCLKp0/REFCLKp4 | B14 B15 | Output | PCIe compliant differential reference clocks. 100MHz reference clocks are used for the OCP NIC 3.0 card PCIe core logic. |
| REFCLKn1/REFCLKn5 REFCLKp1/REFCLKp5 | A14 A15 | Output | |
| REFCLKn2 REFCLKp2 | OCP_B11 OCP_B12 | Output | REFCLK0 is always available to all OCP NIC 3.0 cards. The card should not assume REFCLK1, REFCLK2 or REFCLK3 are available until the bifurcation negotiation process is complete. |
| REFCLKn3 REFCLKp3 | OCP_A11 OCP_A12 | Output | <p>For baseboards, the REFCLK0, REFCLK1, REFCLK2 and REFCLK3 signals shall be available at the Primary Connector for supported designs. REFCLK2 and REFCLK3 are only available on the Primary connector in the OCP Bay. REFCLK4 and REFCLK5 are available on the Secondary connector.</p> <ul style="list-style-type: none"> REFCLK0 is required for all designs. REFCLK1, REFCLK2 and REFCLK3 are required for designs that support 2 xn, and 4 xn bifurcation implementations. <p>For baseboard implementations that use REFCLK[1:3], the baseboard should disable the appropriate REFCLKs not used by the OCP NIC 3.0 card.</p> <p>The baseboard shall not advertise the corresponding bifurcation modes if REFCLK[1:3] are not implemented.</p> <p>REFCLK4 and REFCLK5 are only available on the Secondary Connector and are not defined for use this specification release.</p> <p>For OCP NIC 3.0 cards, the required REFCLKs shall be connected per the endpoint datasheet. Unused REFCLKs on the OCP NIC 3.0 card shall be left as a no connect.</p> |

| Signal Name (Primary / Secondary) | Pin # | Baseboard Direction | Signal Description |
|---|------------|------------------------|--|
| | | | <p>Note: For cards that only support 1 x16, REFCLK0 is used. For cards that support 2 x8, REFCLK0 is used for the first eight PCIe lanes, and REFCLK1 is used for the second eight PCIe lanes. REFCLK2 and REFCLK3 are only used for cards that only support a four link PCIe bifurcation mode.</p> <p>Refer to Section 2.1 in the PCIe CEM Specification, Rev 4.0 for electrical details.</p> |
| PETn0 / PETn16 PETp0 / PETp16 | B17 B18 | Output | <p>Transmitter differential pairs [0:15] (Primary Connector), and differential pairs [16:31] (Secondary Connector). These pins are connected from the baseboard transmitter differential pairs to the receiver differential pairs on the OCP NIC 3.0 card.</p> <p>The PCIe transmit pins shall be AC coupled on the baseboard with capacitors. The AC coupling capacitor value shall use the C_{TX} parameter value specified in the PCIe Base Specification Rev 4.0 Section 8.3.9.</p> <p>For baseboards, the PET[0:15] signals are required at the Primary Connector for the SFF and TSFF slots. PET[0:15] and PET[16:31] are required for a LFF slot.</p> <p>For SFF and TSFF OCP NIC 3.0 cards, the required PET[0:15] signals shall be connected to the endpoint silicon. For silicon that uses less than a x16 connection, the appropriate PET[0:15] signals shall be connected per the endpoint datasheet.</p> <p>For LFF implementations, PET[0:15] are assigned to the Primary Connector, and PET[16:31] are assigned to the Secondary Connector.</p> <p>Refer to Section 6.1 in the PCIe CEM Specification, Rev 4.0 for details.</p> |
| PETn1 / PETn17 PETp1 / PETp17 | B20 B21 | Output | |
| PETn2 / PETn18 PETp2 / PETp18 | B23 B24 | Output | |
| PETn3 / PETn19 PETp3 / PETp19 | B26 B27 | Output | |
| PETn4 / PETn20 PETp4 / PETp20 | B30 B31 | Output | |
| PETn5 / PETn21 PETp5 / PETp21 | B33 B34 | Output | |
| PETn6 / PETn22 PETp6 / PETp22 | B36 B37 | Output | |
| PETn7 / PETn23 PETp7 / PETp23 | B39 B40 | Output | |
| PETn8 / PETn24 PETp8 / PETp24 | B44 B45 | Output | |
| PETn9 / PETn25 PETp9 / PETp25 | B47 B48 | Output | |
| PETn10 / PETn26 PETp10 / PETp26 | B50 B51 | Output | |
| PETn11 / PETn27 PETp11 / PETp27 | B53 B54 | Output | |
| PETn12 / PETn28 PETp12 / PETp28 | B56 B57 | Output | |
| PETn13 / PETn29 PETp13 / PETp29 | B59 B60 | Output | |
| PETn14 / PETn30 PETp14 / PETp30 | B62 B63 | Output | |
| PETn15 / PETn31 PETp15 / PETp31 | B65 B66 | Output | |
| PERn0 / PERn16 PERp0 / PERp16 | A17 A18 | Input | <p>Receiver differential pairs [0:15] (Primary Connector), and differential pairs [16:31] (Secondary Connector). These pins are connected</p> |
| PERn1 / PERn17 | A20 | Input | |

| Signal Name (Primary / Secondary) | Pin # | Baseboard Direction | Signal Description |
|--|--------------------------------|------------------------|--|
| PERp1 / PERp17 | A21 | | from the OCP NIC 3.0 card transmitter differential pairs to the receiver differential pairs on the baseboard. |
| PERn2 / PERn18 PERp2 / PERp18 | A23 A24 | Input | |
| PERn3 / PERn19 PERp3 / PERp19 | A26 A27 | Input | The PCIe receive pins shall be AC coupled on the OCP NIC 3.0 card with capacitors. The AC coupling capacitor value shall use the C _{TX} parameter value specified in the PCIe Base Specification Rev 4.0 Section 8.3.9. |
| PERn4 / PERn20 PERp4 / PERp20 | A30 A31 | Input | |
| PERn5 / PERn21 PERp5 / PERp21 | A33 A34 | Input | |
| PERn6 / PERn22 PERp6 / PERp22 | A36 A37 | Input | |
| PERn7 / PERn23 PERp7 / PERp23 | A39 A40 | Input | For baseboards, the PER[0:15] signals are required at the Primary Connector for the SFF and TSFF slots. PER[0:15] and PER[16:31] are required for a LFF slot. |
| PERn8 / PERn24 PERp8 / PERp24 | A44 A45 | Input | |
| PERn9 / PERn25 PERp9 / PERp25 | A47 A48 | Input | For SFF and TSFF OCP NIC 3.0 cards, the required PER[0:15] signals shall be connected to the endpoint silicon. For silicon that uses less than a x16 connection, the appropriate PER[0:15] signals shall be connected per the endpoint datasheet. |
| PERn10 / PERn26 PERp10 / PERp26 | A50 A51 | Input | |
| PERn11 / PERn27 PERp11 / PERp27 | A53 A54 | Input | |
| PERn12 / PERn28 PERp12 / PERp28 | A56 A57 | Input | For LFF implementations, PER[0:15] are assigned to the Primary Connector, and PER[16:31] are assigned to the Secondary Connector. |
| PERn13 / PERn29 PERp13 / PERp29 | A59 A60 | Input | |
| PERn14 / PERn30 PERp14 / PERp30 | A62 A63 | Input | Refer to Section 6.1 in the PCIe CEM Specification, Rev 4.0 for details. |
| PERn15 / PERn31 PERp15 / PERp31 | A65 A66 | Input | |
| PERST0# / PERST4# PERST1# / PERST5# PERST2# PERST3# | B10 A11 OCP_A1 OCP_A2 | Output | <p>PCIe Reset #[0:5]. Active low.</p> <p>When PERSTn# is deasserted, the signal shall indicate the power state is already in Main Power Mode and is within tolerance and stable for the OCP NIC 3.0 card to bring up the PCIe link.</p> <p>PERST# shall be deasserted at least 1s after the NIC_PWR_GOOD assertion to Main Power Mode. This ensures the card power rails are within the operating limits. This value is longer than the minimum value specified in the PCIe CEM Specification. The PCIe REFCLKs shall also become stable within this period of time.</p> |

| Signal Name (Primary / Secondary) | Pin # | Baseboard Direction | Signal Description |
|---|--------|------------------------|---|
| | | | <p>PERST[0:5]# shall be asserted low on the baseboard until the platform is ready to deassert reset.</p> <p>For baseboards that support bifurcation, the PERST[0:3]# signals are required at the Primary Connector, PERST[4:5]# are required at the Secondary Connector.</p> <p>For OCP NIC 3.0 cards, the required PERST[0:5]# signals shall be connected to the endpoint silicon. Unused PERST[0:5]# signals shall be left as a no connect.</p> <p>Note: For cards that only support 1 x16, PERST0# is used. For cards that support 2 x8, PERST0# is used for the first eight PCIe lanes, and PERST1# is used for the second eight PCIe lanes. PERST2# and PERST3# are only used for cards that support a four link PCIe bifurcation mode.</p> <p>PERST0# is always available to all OCP NIC 3.0 cards. The card should not assume PERST[1:5]# are available until the bifurcation negotiation process is complete.</p> <p>For hosts with unused PERST[1:5]# signals, a 10 kΩ pull down resistor shall be provided by the baseboard for each unused pin.</p> <p>Refer to Section 2.2 in the PCIe CEM Specification, Rev 4.0 for details.</p> |
| WAKE# | OCP_A3 | Input, OD | <p>WAKE#. Open drain. Active low.</p> <p>This signal shall be driven by the OCP NIC 3.0 card to notify the baseboard to restore PCIe link. For OCP NIC 3.0 cards that support multiple WAKE# signals, their respective WAKE# pins may be tied together as the signal is open-drain to form a wired-OR. For multi-homed host configurations, the WAKE# signal assertion shall wake all nodes.</p> <p>For baseboards, this signal shall be pulled up to +3.3V_EDGE on the baseboard with a 10 kΩ resistor. This signal shall be connected to the system WAKE# signal.</p> |

| Signal Name (Primary / Secondary) | Pin # | Baseboard Direction | Signal Description |
|-----------------------------------|-------|---------------------|---|
| | | | <p>For OCP NIC 3.0 cards, this signal shall be connected between the endpoint silicon WAKE# pin(s) and the card edge through an isolation buffer. The WAKE# signal shall not assert until the PCIe card is in the D3 state according to the PCIe CEM specification to prevent false WAKE# events. For OCP NIC 3.0, the WAKE# pin shall be buffered or otherwise isolated from the host until the aux voltage source is present. Examples of this are shown in Section 3.5.5 by gating via an on-board “AUX_PWR_GOOD” signal to indicate all the NIC Aux power rails are stable. The PCIe CEM specification also shows an example in the WAKE# signal section.</p> <p>This pin shall be left as a no connect if WAKE# is not supported by the silicon.</p> <p>Refer to Section 2.3 in the PCIe CEM Specification, Rev 4.0 for details.</p> |
| PWRBRK0# / PWRBRK1# | A70 | Output, OD | <p>Power Brake. Active low, open drain.</p> <p>This signal shall be pulled up to +3.3V_EDGE on the OCP NIC 3.0 card with 95 kΩ or larger resistance. A baseboard that supports this function must provide a stronger pull up on PWRBRK#. A baseboard pull up value between 4.7 kΩ and 10 kΩ is recommended. The pull up shall meet the T_{PWRBRK} timing parameter as shown in the PCIe CEM Specification.</p> <p>When this signal is driven low by the baseboard, the Emergency Power Reduction State is requested. The OCP NIC 3.0 card shall move to a lower power consumption state.</p> <p>For baseboards, the PWRBRK0# pin shall be implemented and available on the Primary Connector for the SFF and TSFF slots. In addition, the PWRBRK1# pin shall be implemented on the Secondary connector for LFF slots.</p> <p>For OCP NIC 3.0 cards, the PWRBRK[0:1]# pin usage is optional. If used, the PWRBRK0# on the Primary</p> |

| Signal Name (Primary / Secondary) | Pin # | Baseboard Direction | Signal Description |
|---|-------|------------------------|---|
| | | | <p>Connector should be connected to the network silicon to enable reduced power state. If not used, the PWRBRK0# signals shall be left as a no connect. PWRBRK1# on the Secondary Connector is reserved for future use cases and shall be left as a no connect.</p> <p>Note: The PWRBRK[0:1]# pins are only available for OCP NIC 3.0 cards that implement a SFF/TSFF 4C+ edge connector or a LFF. For SFF/TSFF cards that implement at 2C+ edge connection, the PWRBRK[0:1]# functionality is not available.</p> |

3.4.2 PCIe Present and Bifurcation Control Pins

This section provides the pin assignments for the PCIe present and bifurcation control signals. The AC/DC specifications are defined in Section 3.11. Example connection diagrams are shown in Figure 91 and Figure 92.

The PRSNTA#/PRSNTB[3:0]# state shall be used to determine if a card has been physically plugged in. The BIF[2:0]# pins shall be asserted by the baseboard along with the rising edge of AUX_PWR_EN. The BIF[2:0]# pins shall be latched by the OCP NIC 3.0 card when AUX_PWR_EN=1 and NIC_PWR_GOOD=1 to ensure the correct values are detected by the OCP NIC 3.0 card. Changing the pin states after this timing window is not allowed. Refer to the AC timing diagram in Section 3.11 for details.

PRSNTB[3:0]# pins are available to each connector and are independent of each other. For the SFF and TSFF, the baseboard shall only read the Primary Connector PRSNTB[3:0]# to determine the card type. For the LFF, the baseboard shall read both the Primary and Secondary connector PRSNTB[3:0]# pins to determine the card type. The card type matrix is discussed in Section 3.5.

Table 24: Pin Descriptions – PCIe Present and Bifurcation Control Pins

| Signal Name | Pin # | Baseboard Direction | Signal Description |
|--|--------------------------|---------------------|---|
| PRSNTA# | A10 | Output | <p>Present A is used for OCP NIC 3.0 card presence and PCIe capabilities detection.</p> <p>For baseboards, this pin shall be directly connected to GND.</p> <p>For OCP NIC 3.0 cards, this pin shall be directly connected to the PRSNTB[3:0]# pins.</p> |
| PRSNTB0# PRSNTB1# PRSNTB2# PRSNTB3# | B42 A42 A12 B70 | Input | <p>Present B [3:0]# are used for OCP NIC 3.0 card presence and PCIe capabilities detection.</p> <p>For baseboards, these pins shall be connected to the I/O hub and pulled up to +3.3V_EDGE using 1 kΩ resistors.</p> <p>For OCP NIC 3.0 cards, these pins shall be strapped to PRSNTA# per the encoding definitions described in Section 3.5. The card series resistor values shall be in the range of 0 Ω to ~200 Ω to protect the baseboard logic.</p> <p><u>When no OCP NIC 3.0 card is installed, the baseboard shall see this value as PRSNTB[3:0]#=0b1111.</u></p> <p>Note: PRSNTB3# is located at the bottom of the 4C connector and is only applicable for OCP NIC 3.0 cards with a PCIe width of x16 (or greater). OCP NIC 3.0 cards that implement a 2C card edge do not use</p> |

| Signal Name | Pin # | Baseboard Direction | Signal Description |
|-------------------------|----------------|---------------------|---|
| | | | the PRSNTB3# pin for capabilities or present detection. |
| BIF0# BIF1# BIF2# | B7 B8 B9 | Output | <p>Bifurcation [2:0]# pins allow the baseboard to force configure the OCP NIC 3.0 card bifurcation.</p> <p>For baseboards, the BIF[2:0]# pins shall be driven from the baseboard I/O hub on the rising edge of AUX_PWR_EN. This allows the baseboard to force the OCP NIC 3.0 card bifurcation. The baseboard may optionally pull the BIF[2:0]# signals to AUX_PWR_EN or to ground per the definitions described in Section 3.5 if no dynamic bifurcation configuration is required. The BIF[2:0]# pins shall be low until AUX_PWR_EN is asserted. The BIF[2:0]# pins shall remain static after AUX_PWR_EN is asserted. The pins are not allowed to change states when the OCP NIC 3.0 card is powered on.</p> <p>For baseboards that allow dynamic bifurcation, the BIF[2:0] pins are driven low prior to AUX_PWR_EN. The state of the BIF[2:0] pins are driven with the rising edge of AUX_PWR_EN when bifurcation is requested. Refer to Figure 91 for an example configuration.</p> <p>For baseboards with static bifurcation, the BIF pins that are intended to be a logical '1' shall be connected to a pull up to AUX_PWR_EN. BIF pins that are a logical '0' may be directly tied to ground. Refer to Figure 92 for an example configuration.</p> <p>For OCP NIC 3.0 cards, these signals shall connect to the endpoint bifurcation pins if it is supported. The BIF[2:0]# signals shall be left as no connects if endpoint bifurcation is not supported. The value of the BIF[2:0]# pins are latched by the OCP NIC 3.0 card upon entering Aux Power Mode (when AUX_PWR_EN=1 and NIC_PWR_GOOD=1).</p> <p>Note: the required combinatorial logic output for endpoint bifurcation is dependent on the specific silicon and is not defined in this specification.</p> |

Figure 91: PCIe Present and Bifurcation Control Pins (Baseboard Controlled BIF[2:0]#)

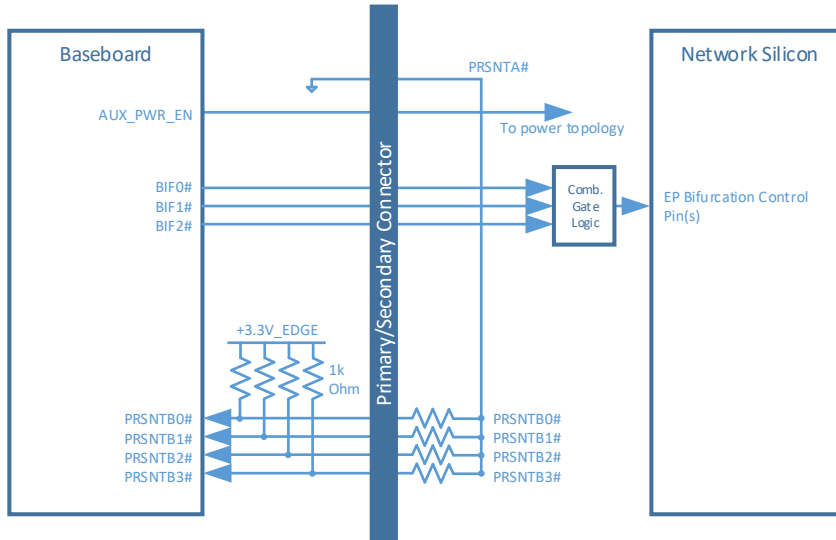
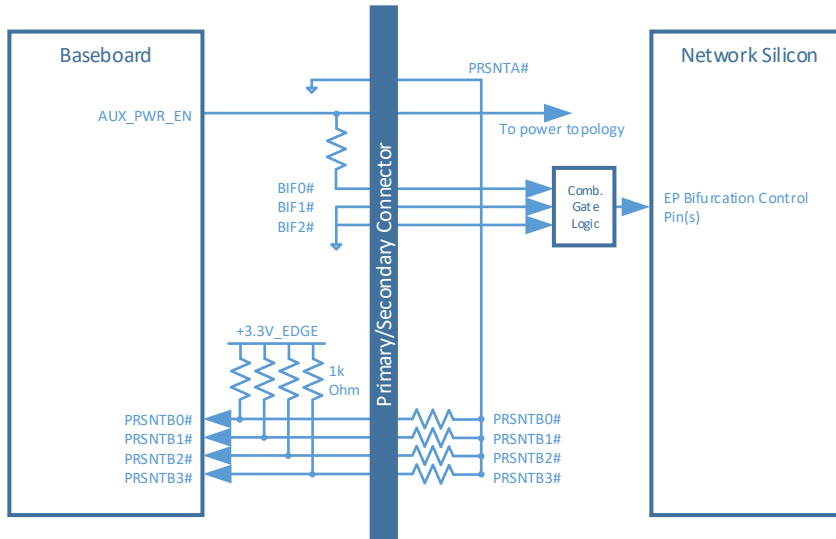


Figure 92: PCIe Present and Bifurcation Control Pins (Static BIF[2:0]#)



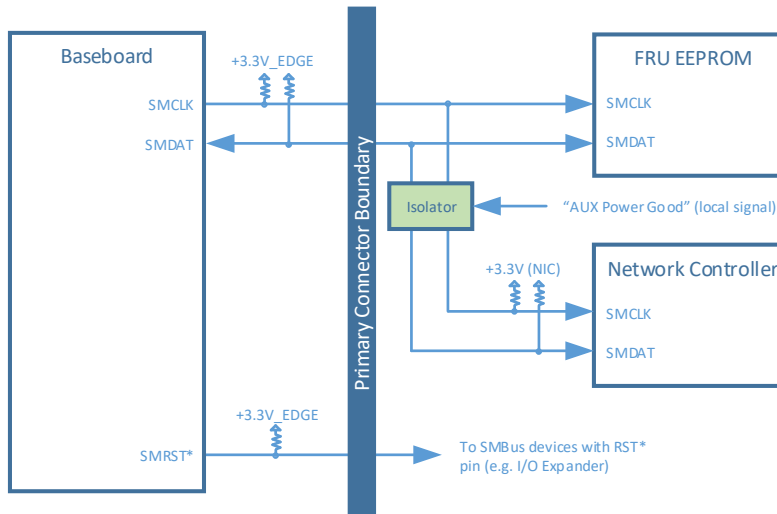
3.4.3 SMBus Interface Pins

This section provides the pin assignments for the SMBus interface signals. The AC/DC specifications are defined in the SMBus 2.0 specification. The SMBus interface is pinned out on the Primary and Secondary Connectors. For SFF, TSFF and LFF OCP NIC 3.0 card implementations, FRU and MCTP over SMBus transactions shall use the Primary Connector only. SMBus on the Secondary Connector may be a separate bus and is reserved for a future use case. An example connection diagram is shown in Figure 93.

Table 25: Pin Descriptions – SMBus

| Signal Name | Pin # | Baseboard Direction | Signal Description |
|-------------|-------|---------------------|--|
| SMCLK | A7 | Output, OD | <p>SMBus clock. Open drain, pulled up to +3.3V_EDGE on the baseboard.</p> <p>For baseboards, the SMCLK from the platform SMBus master shall be connected to the connector.</p> <p>For OCP NIC 3.0 cards, the SMCLK from the endpoint silicon shall be connected to the card edge gold fingers.</p> |
| SMDAT | A8 | Input / Output, OD | <p>SMBus Data. Open drain, pulled up to +3.3V_EDGE on the baseboard.</p> <p>For baseboards, the SMDAT from the platform SMBus master shall be connected to the connector.</p> <p>For OCP NIC 3.0 cards, the SMDAT from the endpoint silicon shall be connected to the card edge gold fingers.</p> |
| SMRST# | A9 | Output, OD | <p>SMBus reset. Open drain.</p> <p>For baseboards, this pin shall be pulled up to +3.3V_EDGE. The SMRST pin may be used to reset optional downstream SMBus devices (such as temperature sensors). The SMRST# implementation shall be mandatory for baseboard implementations.</p> <p>For OCP NIC 3.0 cards, SMRST# is optional and is dependent on the OCP NIC 3.0 card implementation. If used, the SMRST# is on the +3.3V_EDGE power domain. Isolation logic may be required if the target device(s) exist on a different power domain to prevent a leakage path. The SMRST# signal shall be left as a no connect if it is not used on the OCP NIC 3.0 card.</p> |

Figure 93: Example SMBus Connections



3.4.4 NC-SI over RBT Interface Pins

This section provides the pin assignments for the NC-SI over RBT interface signals on the Primary Connector OCP bay. The AC/DC specifications for NC-SI over RBT are defined in the DMTF DSP0222 NC-SI specification. Example connection diagrams are shown in Figure 94 and Figure 95.

~~Note: The baseboard shall possess the ability to isolate the RBT pins, including RBT_CLK_IN, must provide the ability to be isolated on the baseboard side, when AUX_PWR_EN=0 or when (AUX_PWR_EN=1 and NIC_PWR_GOOD=0). The isolation logic shall be controlled with a baseboard generated signal called RBT_ISOLATE#. This signal is not pinned out on the Primary or Secondary Connectors. RBT_ISOLATE# shall be low when AUX_PWR_EN=0 or before the card side supplies have been fully enabled (AUX_PWR_EN=1 and NIC_PWR_GOOD=0). RBT_ISOLATE# shall become high when The RBT pins shall remain isolated until the power state machine has transitioned to Aux Power Mode (AUX_PWR_EN=1 and or to Main Power Mode along with a the valid indication rising edge of NIC_PWR_GOOD=1 (upon entering Aux Power Mode). RBT_ISOLATE# shall remain high during the transition to Main Power Mode when the NIC_PWR_GOOD signal is in the don't care state. RBT_ISOLATE# shall be high when (AUX_PWR_EN=1, MAIN_PWR_EN=1 and NIC_PWR_GOOD=1). The truth table that describes the RBT_ISOLATE# behavior is illustrated in Table 26 and shown in Figure 116. This prevents a leakage path through unpowered silicon. The RBT_REF_CLK must also be disabled until AUX_PWR_EN=1 and NIC_PWR_GOOD=1. Example buffering implementations are shown in Figure 94 and Figure 95. The isolator shall be controlled on the baseboard with a signal called RBT_ISOLATE#. The RBT_ISOLATE# signal shall remain asserted even when the NIC_PWR_GOOD signal is in the don't care state. This is illustrated in Figure 116.~~

Table 26: RBT_ISOLATE# Truth Table

| AUX_PWR_EN | MAIN_PWR_EN | NIC_PWR_GOOD | RBT_ISOLATE# |
|------------|-------------|--------------|--------------|
|------------|-------------|--------------|--------------|

| | | | |
|----------|----------|---|----------|
| <u>0</u> | <u>X</u> | <u>X</u> | <u>0</u> |
| <u>1</u> | <u>X</u> | <u>0</u> | <u>0</u> |
| <u>1</u> | <u>X</u> | <u>Rising edge on entering Aux Power Mode</u> | <u>1</u> |
| <u>1</u> | <u>1</u> | <u>X</u> | <u>1</u> |

Isolation prevents a leakage path through unpowered silicon. Example buffering implementations are shown in Figure 94 and Figure 95.

RBT reference clock buffers are permitted on the OCP NIC for multi-endpoint implementations if the NIC timing budget is not violated. Refer to the signal integrity requirements in Section 5.1 for timing budget details.

Command-based (software) arbitration is also permissible per DSP0222. Baseboards may choose to use the Select Package and Deselect Package commands to allow a network controller to transmit on the shared bus when more than one device is present.

Table 27: Pin Descriptions – NC-SI over RBT

| Signal Name | Pin # | Baseboard Direction | Signal Description |
|----------------------|------------------|---------------------|--|
| RBT_REF_CLK_IN | OCP_A14 | Output | <p>Reference clock input. Synchronous clock reference for receive, transmit and control interface. The clock shall have a typical frequency of 50MHz ±50 ppm.</p> <p>For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the Primary Connector OCP bay. The RBT_REF_CLK_IN shall not be driven until the card has transitioned into Aux Power Mode. The RBT_REF_CLK_IN shall be continuous once it has started <u>and while RBT_ISOLATE# is high</u>.</p> <p>If the baseboard does not support NC-SI over RBT, then this pin shall be terminated to ground through a 100 kΩ pull down resistor.</p> <p>For OCP NIC 3.0 cards, this pin shall be connected between the card gold finger and the endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.</p> |
| RBT_CRS_DV | OCP_B14 | Input | <p>Carrier sense/receive data valid. This signal is used to indicate to the baseboard that the carrier sense/receive data is valid.</p> <p>For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor on the baseboard between the BMC and the RBT isolator to prevent the signal from floating when no card is installed.</p> <p>If the baseboard does not support NC-SI over RBT, then this pin shall be terminated to ground through a 100 kΩ pull down resistor.</p> <p>For OCP NIC 3.0 cards, this pin shall be connected between the card gold finger and the endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.</p> |
| RBT_RXD0 RBT_RXD1 | OCP_B9 OCP_B8 | Input | <p>Receive data. Data signals from the network controller to the BMC.</p> |

| Signal Name | Pin # | Baseboard Direction | Signal Description |
|----------------------|------------------|---------------------|--|
| | | | <p>For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor to GND on the baseboard between the BMC and the RBT isolator to prevent the signal from floating when no card is installed.</p> <p>If the baseboard does not support NC-SI over RBT, then this pin shall be terminated to GND through a 100 kΩ pull down.</p> <p>For OCP NIC 3.0 cards, this pin shall be connected between the card gold fingers and the RBT_RXD[0:1] pins on endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.</p> |
| RBT_TX_EN | OCP_A7 | Output | <p>Transmit enable.</p> <p>For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor to ground on the baseboard between the RBT isolator and the OCP connector to prevent the card-side signals from floating when the RBT signals are isolated.</p> <p>If the baseboard does not support NC-SI over RBT, then this pin shall be terminated to ground through a 100 kΩ pull down.</p> <p>For OCP NIC 3.0 cards, this pin shall be connected between the card gold finger and the endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.</p> |
| RBT_TXD0 RBT_TXD1 | OCP_A9 OCP_A8 | Output | <p>Transmit data. Data signals from the BMC to the network controller.</p> <p>For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor to GND on the baseboard between the RBT isolator and the OCP connector to prevent the card-side signals from floating when the RBT signals are isolated.</p> |

| Signal Name | Pin # | Baseboard Direction | Signal Description |
|-------------|--------|---------------------|---|
| | | | <p>If the baseboard does not support NC-SI over RBT, then this pin shall be terminated to GND through a 100 kΩ pull down.</p> <p>Note: Some BMC vendors use the RBT_TXD[0:1] pins as hardware configuration straps. A 4.7 kΩ to 10 kΩ pull up/pull down resistor is permitted between the BMC and the RBT isolator for this purpose. The resulting network will not violate the NC-SI V_{HMIN} of 2.0V.</p> <p>For OCP NIC 3.0 cards, this pin shall be connected between the card gold fingers and the RBT_TXD[0:1] pins on the endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.</p> |
| RBT_ARB_OUT | OCP_A5 | Output | <p>NC-SI hardware arbitration output.</p> <p>If the baseboard supports multiple OCP NIC 3.0 cards connected to the same RBT interface, it shall implement logic that connects the RBT_ARB_OUT pin of the first populated OCP NIC 3.0 card to its RBT_ARB_IN pin if it is the only card present or to the RBT_ARB_IN pin of the next populated card and so on sequentially for all cards on the specified RBT bus to ensure the arbitration ring is complete. This logic shall bypass slots that are not populated, powered off, or in ID mode. A two OCP NIC 3.0 card example using an analog mux is shown in Figure 95.</p> <p>If the baseboard does not support NC-SI over RBT or implements only one OCP NIC 3.0 interface, this signal shall be directly connected to the RBT_ARB_IN pin to complete the hardware arbitration ring on the OCP NIC 3.0 card.</p> <p>For OCP NIC 3.0 cards that support hardware arbitration, this pin shall be connected between the card gold finger and the RBT_ARB_IN pin on the endpoint silicon. If the card implements two controllers, both must be connected internally to complete the ring, see Figure 95. If hardware arbitration is not supported, then this pin shall be directly connected to the card edge RBT_ARB_IN pin. This allows the hardware arbitration signals to pass through in a multi-Primary Connector baseboard.</p> |
| RBT_ARB_IN | OCP_A4 | Input | NC-SI hardware arbitration input. |

| Signal Name | Pin # | Baseboard Direction | Signal Description | | | | | | | | | | | | | | | |
|-------------------------|------------------|---------------------|---|-------------------------|-----------------|-----------------|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | <p>If the baseboard supports multiple OCP NIC 3.0 cards connected to the same RBT interface, it shall implement logic that connects the RBT_ARB_IN pin of the first populated OCP NIC 3.0 card to its RBT_ARB_OUT pin if it is the only card present or to the RBT_ARB_OUT pin of the next populated card and so on sequentially for all cards on the specified RBT bus to ensure the arbitration ring is complete. This logic shall bypass slots that are not populated, powered off, or in ID mode. A two OCP NIC 3.0 card example using an analog mux is shown in Figure 95.</p> <p>If the baseboard does not support NC-SI over RBT or implements only one OCP NIC 3.0 interface, this signal shall be directly connected to the RBT_ARB_OUT pin to complete the hardware arbitration ring on the OCP NIC 3.0 card.</p> <p>For OCP NIC 3.0 cards that support hardware arbitration, this pin shall be connected between the card gold finger and the RBT_ARB_OUT pin on the endpoint silicon. If the card implements two controllers, both must be connected internally to complete the ring, see Figure 95. If hardware arbitration is not supported, then this pin shall be directly connected to the card edge RBT_ARB_OUT pin. This allows the hardware arbitration signals to pass through in a multi-Primary Connector baseboard.</p> | | | | | | | | | | | | | | | |
| SLOT_ID0 SLOT_ID1 | OCP_B7 OCP_A6 | Output | <p>NC-SI / FRU EEPROM Address 0/1.</p> <p>For baseboards, the SLOT_ID[1:0] pins shall be connected to GND through a 100 Ω pull down or to +3.3V_EDGE through a 4.7 kΩ pull up. The SLOT[1:0] values are based on the following mapping on a per slot basis:</p> <table border="1"> <thead> <tr> <th>Physical Slot (Decimal)</th> <th>SLOT_ID1 OCP_A6</th> <th>SLOT_ID0 OCP_B7</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>3</td> <td>1</td> <td>1</td> </tr> </tbody> </table> | Physical Slot (Decimal) | SLOT_ID1 OCP_A6 | SLOT_ID0 OCP_B7 | 0 | 0 | 0 | 1 | 0 | 1 | 2 | 1 | 0 | 3 | 1 | 1 |
| Physical Slot (Decimal) | SLOT_ID1 OCP_A6 | SLOT_ID0 OCP_B7 | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | | | | | | | | | | | | | | | | |
| 2 | 1 | 0 | | | | | | | | | | | | | | | | |
| 3 | 1 | 1 | | | | | | | | | | | | | | | | |

| Signal Name | Pin # | Baseboard Direction | Signal Description |
|-------------|-------|---------------------|---|
| | | | <p>For OCP NIC 3.0 cards, the SLOT_ID[1:0] pins shall be used to set the RBT Package ID and the FRU EEPROM address on the OCP NIC 3.0 card. The OCP NIC 3.0 card may optionally implement weak pull up or pull down resistors (>47 kΩ) to prevent the silicon pins from floating prior to the local silicon “Aux power good.”</p> <p>For OCP NIC 3.0 cards, SLOT_ID0 shall be connected to the endpoint device GPIO associated with Package ID[0]. SLOT_ID1 shall be associated with Package ID[1]. Refer to Section 4.8.1 and the device datasheet for details.</p> <p>For OCP NIC 3.0 cards with multiple endpoint devices, Package ID[2] shall be used to identify a second physical RBT capable controller on the same physical card.</p> <p>For Package ID addressing, the SLOT_ID[1:0] pins shall be buffered on NIC side with a FET switch (or a similar implementation) to prevent a leakage path when the OCP NIC 3.0 card is in ID mode. The SLOT_ID[1:0] buffers shall isolate the signals to the network silicon until an “Aux Power Good” is generated locally from the NIC. This indication shall be generated from an on-board voltage monitor or similar logic. OCP NIC 3.0 designers may omit isolation logic for the Package ID addressing if the target silicon properly isolates the signals when it is unpowered.</p> <p>For FRU EEPROM addressing, the SLOT_ID0 pin shall be directly connected to the EEPROM A1 address pin; SLOT_ID1 shall be connected to the EEPROM A2 address pin. No isolation shall be used for the FRU EEPROM connections.</p> <p>For endpoint devices without NC-SI over RBT support, these pins shall only be connected to the FRU EEPROM as previously described.</p> |

Figure 94: NC-SI over RBT Connection Example – Single Primary Connector

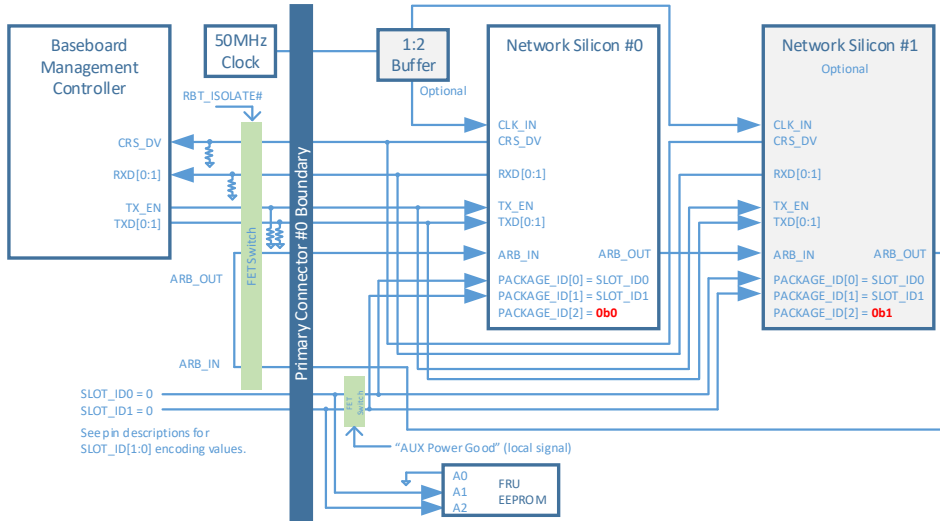
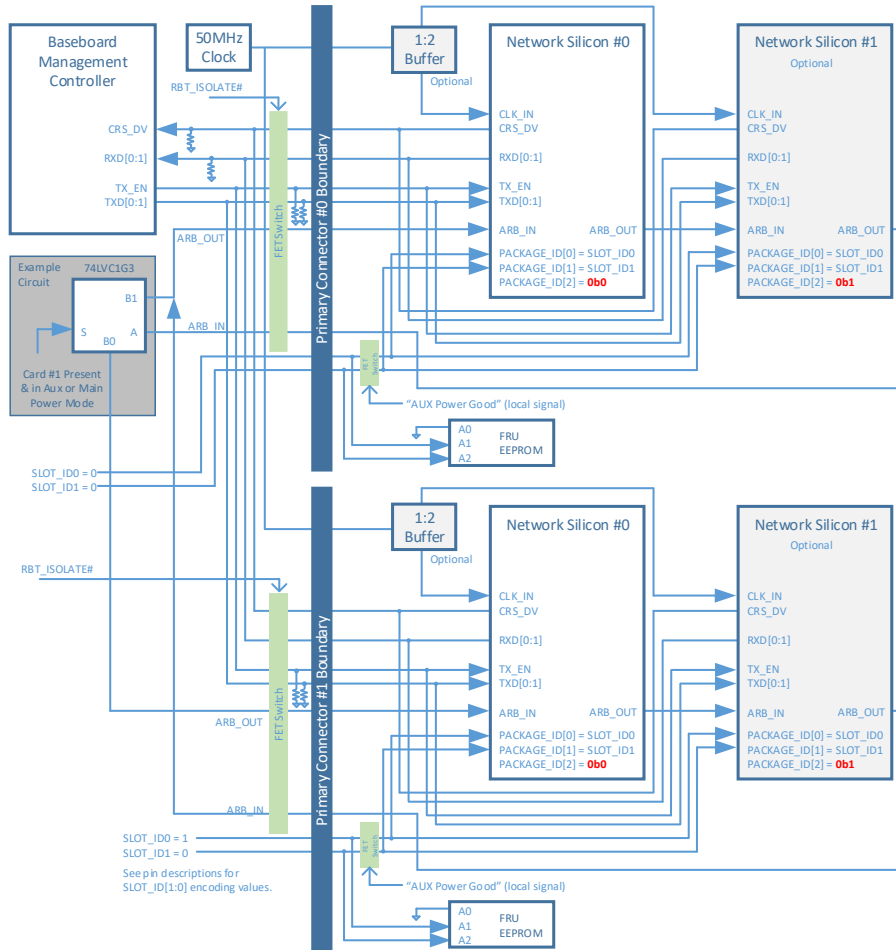


Figure 95: NC-SI over RBT Connection Example – Dual Primary Connectors



Note 1: For baseboard designs with a single Primary Connector, connect ARB_IN to ARB_OUT to complete the NC-SI hardware arbitration ring. For designs with multiple Primary Connectors, connect ARB_IN and ARB_OUT to an analog mux to complete the NC-SI arbitration ring based on the number of cards installed in the system. An example dual Primary Connector implementation is shown in Figure 95.

Note 2: For baseboard implementations having two or more RBT busses, the baseboard hardware arbitration rings shall remain within their respective bus and shall not cross RBT bus domains.

Note 3: The baseboard implementation shall maintain the arbitration ring integrity when there exists one or more cards that are not present, plugged in but are powered off, or in ID Mode.

Note 4: For OCP NIC 3.0 cards with two discrete endpoint silicon, the Package ID[2] bit shall be statically set based on the silicon instance. For example, the figure above shows Network Silicon #0 and Network Silicon #1. Network Silicon #0 has Package ID[2] = 0b0, Network Silicon #1 has Package ID[2] = 0b1.

Note 5: Designs that implement a clock fan out buffer will affect the RBT timing budget. Careful analysis of the timing budget is required. Refer to Section 5.1 for RBT signal integrity and timing budget considerations.

3.4.5 Scan Chain Pins

This section provides the pin assignments for the Scan Chain interface signals on the Primary Connector OCP Bay. The scan chain is a point-to-point bus on a per OCP slot basis. The scan chain consists of two unidirectional busses, a common clock and a common load signal. The SCAN_DATA_OUT signal serially shifts control signals from the baseboard to the OCP NIC 3.0 card. The SCAN_DATA_IN signal serially shifts bits from the OCP NIC 3.0 card to the baseboard. The SCAN_DATA_OUT and SCAN_DATA_IN chains are independent of each other. The scan chain SCAN_CLK is driven from the baseboard. The SCAN_LD# pin, when asserted by the baseboard, allows loading of the data on to the shift registers. An example timing diagram is shown in Figure 96. An example connection diagram is shown in Figure 98.

Note: The SCAN_DATA_OUT chain is provisioned, but is not used on OCP NIC 3.0 cards for this revision of the specification.

Table 28: Pin Descriptions – Scan Chain

| Signal Name | Pin # | Baseboard Direction | Signal Description |
|----------------------|--------|---------------------|---|
| <u>SCAN_CLK</u> | OCP_B6 | Output | <p>Scan clock. The <u>SCAN_CLK</u> is an output pin from the baseboard to the OCP NIC 3.0 card. The <u>SCAN_CLK</u> may run up to 12.5MHz.</p> <p>For baseboard implementations, the <u>SCAN_CLK</u> pin shall be connected to the Primary Connector. The <u>SCAN_CLK</u> pin shall be tied directly to GND if the scan chain is not used.</p> <p>For NIC implementations, the <u>SCAN_CLK</u> pin shall be connected to Shift Registers 0 & 1, and optionally connected to Shift Registers 2 & 3 (if implemented) as defined in the text and Figure 98, below. The <u>SCAN_CLK</u> pin shall be pulled up to +3.3V_EDGE through a 1 kΩ resistor.</p> |
| <u>SCAN_DATA_OUT</u> | OCP_B5 | Output | <p>Scan data output from the baseboard to the OCP NIC 3.0 card. This bit stream is used to shift configuration data out to the NIC.</p> |

| Signal Name | Pin # | Baseboard Direction | Signal Description |
|------------------------------|--------|---------------------|--|
| | | | <p>For baseboard implementations, the SCAN_DATA_OUT pin shall be connected to the Primary Connector. The SCAN_DATA_OUT pin shall be pulled down to GND through a 1 kΩ resistor if the scan chain is not used.</p> <p>For NIC implementations, the SCAN_DATA_OUT pin shall be pulled down to GND on the OCP NIC 3.0 card through a 10 kΩ resistor.</p> |
| SCAN_DATA_IN | OCP_B4 | Input | <p>Scan data input to the baseboard. This bit stream is used to shift out NIC status bits to the baseboard.</p> <p>For baseboard implementations, the SCAN_DATA_IN pin shall be pulled up to +3.3V_EDGE through a 10 kΩ resistor to prevent the input signal from floating if a card is not installed. This pin may be left as a no connect if the scan chain is not used.</p> <p>For NIC implementations, the SCAN_DATA_IN scan chain is required. The SCAN_DATA_IN pin shall be connected to Shift Register 0, as defined in the text and Figure 98.</p> |
| SCAN_LD# | OCP_B3 | Output | <p>Scan shift register load. Used to latch configuration data on the OCP NIC 3.0 card.</p> <p>For baseboard implementations, the SCAN_LD# pin shall be pulled up to +3.3V_EDGE through a 1 kΩ resistor if the scan chain is not used to prevent the OCP NIC 3.0 card from erroneous data latching.</p> <p>For NIC implementations, the SCAN_LD# pin implementation is required. The SCAN_LD# pin shall be connected to Shift Registers 0 & 1, and optionally connected to Shift Registers 2 & 3 (if implemented) as defined in the text and Figure 98. The SCAN_LD# pin shall be pulled up to +3.3V_EDGE through a 10 kΩ resistor.</p> |

Two possible examples for the Scan Chain timing diagram are shown in Figure 96 and Figure 97. The specific timing parameters guaranteed by the Baseboard are shown in [Table 29](#)~~Table-28~~ and timing parameters guaranteed by the OCP NIC 3.0 card are shown in [Table 30](#)~~Table-29~~. The parameters assume operation with a 15 pF load between 0 °C and 85 °C. The values are relaxed when compared to the 74LV165 datasheet and allows system implementers to use alternate implementations (such as a CPLD) instead of discrete logic parts. If the waveform in Figure 96 is implemented, the first [SCAN_DATA_IN](#) bit (bit 7 on Byte 0) shall be sampled before the first rising edge of the clock that follows [SCAN_LD#](#) signal rising edge. If the waveform in Figure 97 is implemented, the first [SCAN_DATA_IN](#) bit shall be latched by

the baseboard on the falling edge of the clock. For both examples, each subsequent SCAN_DATA_IN bit shall be latched by the baseboard on the falling edge of the clock. SCAN_DATA_OUT shall be driven by the baseboard such that sufficient setup/hold time is assured to the OCP NIC 3.0 card. Note that the first bit that is shifted on SCAN_DATA_IN is 0.7 (bit 7 on the least significant Byte) while the first bit that is shifted on SCAN_DATA_OUT is 3.7 (bit 7 on the most significant Byte).

Figure 96: Scan Chain Timing Diagram Example 1

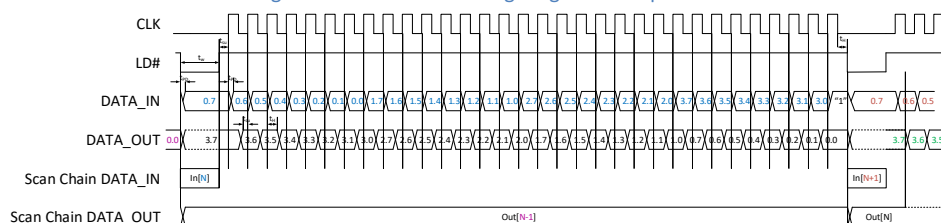


Figure 97: Scan Chain Timing Diagram Example 2

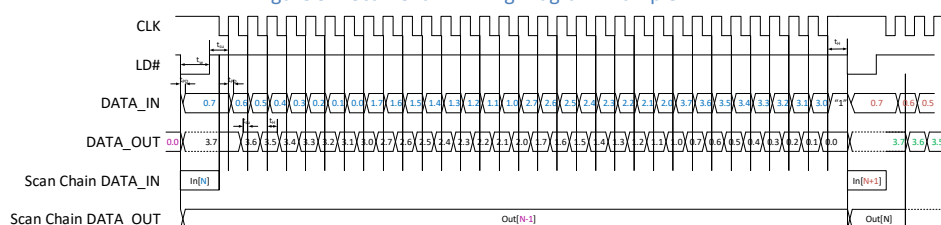


Table 29: Scan Chain Timing Requirements – Baseboard Side

| Parameter | Test Condition | Min | Max | Unit |
|-------------------------------|--|-----------------|------|------|
| t _w Pulse Duration | <u>SCAN</u> _LD# low | 15 ¹ | - | ns |
| t _{su} Setup Time | <u>SCAN</u> _LD# high before <u>SCAN</u> _CLK↑ | 10 | - | ns |
| | <u>SCAN</u> _DATA_OUT valid before <u>SCAN</u> _CLK↑ | | | |
| t _h Hold Time | <u>SCAN</u> _LD# high after <u>SCAN</u> _CLK↑ | 5 | - | ns |
| | <u>SCAN</u> _LD# high after <u>SCAN</u> _CLK↓ | | | |
| | <u>SCAN</u> _DATA_OUT valid after <u>SCAN</u> _CLK↑ | | | |
| f _{max} | <u>SCAN</u> _CLK frequency | - | 12.5 | MHz |

Table 30: Scan Chain Timing Requirements – OCP NIC 3.0 Card Side

| Parameter | From (Input) | To (Output) | Max | Unit |
|-----------------------------------|-------------------------------|----------------------|-----|------|
| t _{pd} Propagation Delay | <u>SCAN</u> _CLK ² | <u>SCAN</u> _DATA_IN | 30 | ns |
| | <u>SCAN</u> _LD# ³ | <u>SCAN</u> _DATA_IN | 30 | ns |

Note 1: When t_w < t_{pd} then SCAN_DATA_IN may only be valid after SCAN_LD# rising edge.

Note 2: Applies when SCAN_LD# is high.

Note 3: When SCAN_LD# is low, the SCAN_CLK signal is ignored by the Scan Chain SCAN_DATA_IN.

The Scan Chain provides sideband status indication between the OCP NIC 3.0 card and the baseboard. The Scan Chain bit definition is defined in the two tables below. The Scan Chain data stream is 32-bits in length for both the `SCAN_DATA_OUT` and the `SCAN_DATA_IN` streams. The Scan Chain implementation is optional on the host, but its implementation is mandatory per [Table 31](#) and [Table 32](#) on all OCP NIC 3.0 cards. The Scan Chain components operates on the +3.3V_EDGE power domain.

The Scan Chain `SCAN_DATA_OUT` bus is an output from the host. The Scan Chain `SCAN_DATA_OUT` bus provides initial configuration options to the OCP NIC 3.0 card. At the time of this writing, the Scan Chain `SCAN_DATA_OUT` bus is not used. All baseboard systems that implement the Scan Chain shall connect `SCAN_DATA_OUT` between the platform and the Primary Connector for subsequent revisions of this specification. The `SCAN_DATA_OUT` data stream shall shift out all 0's prior to `AUX_PWR_EN` assertion to prevent leakage paths into unpowered silicon.

Table 31: Pin Descriptions – Scan Chain `SCAN_DATA_OUT` Bit Definition

| Byte.bit | <code>SCAN_DATA_OUT</code> Field Name | Default Value | Description |
|----------|---------------------------------------|---------------|---------------------------------|
| 0.[0..7] | Reserved | 0h00 | Reserved. Byte 0 value is 0h00. |
| 1.[0..7] | Reserved | 0h00 | Reserved. Byte 1 value is 0h00. |
| 2.[0..7] | Reserved | 0h00 | Reserved. Byte 2 value is 0h00. |
| 3.[0..7] | Reserved | 0h00 | Reserved. Byte 3 value is 0h00. |

The Scan Chain `SCAN_DATA_IN` bus is an input to the host and provides NIC status indication. The default implementation is completed with two 8-bit 74LV165 parallel into serial out shift registers in a cascaded implementation. Up to four shift registers may be implemented to provide additional NIC status indication to the host platform. Alternatively, an OCP NIC 3.0 card vendor may choose to implement this chain using an active device (such as a microcontroller or CPLD), as long as it implements the function of the 74LV165, supporting circuitry for the Scan Chain and meets all of the timing specifications given in this specification. For active device implementations, there is an associated device start-up time. Refer to Section 3.11 for details on the +3.3V_EDGE stable to the first data valid read in ID Mode.

The Scan Chain `SCAN_DATA_IN` shift register 0 shall be mandatory for scan chain implementations for the card present, `WAKE_N` and thermal threshold features. Scan Chain `SCAN_DATA_IN` shift registers 1, 2 & 3 are optional depending on the line side I/O and LED fields being reported to the host. Dual port LED applications require shift register 1. Quad port LED applications require shift registers 1 & 2. Octal port applications require shift registers 1, 2 & 3.

The host should read the Scan Chain `SCAN_DATA_IN` bus multiple times to qualify the incoming data stream. The number of data qualification reads is dependent on the baseboard implementation.

On the OCP NIC 3.0 card, a 1 kΩ pull up resistor shall be connected to the `SER` input of the last `SCAN_DATA_IN` shift register. Doing so ensures the default bit value of 0b1 for implementations using less than four shift registers.

Table 32: Pin Descriptions – Scan Chain SCAN_DATA_IN Bit Definition

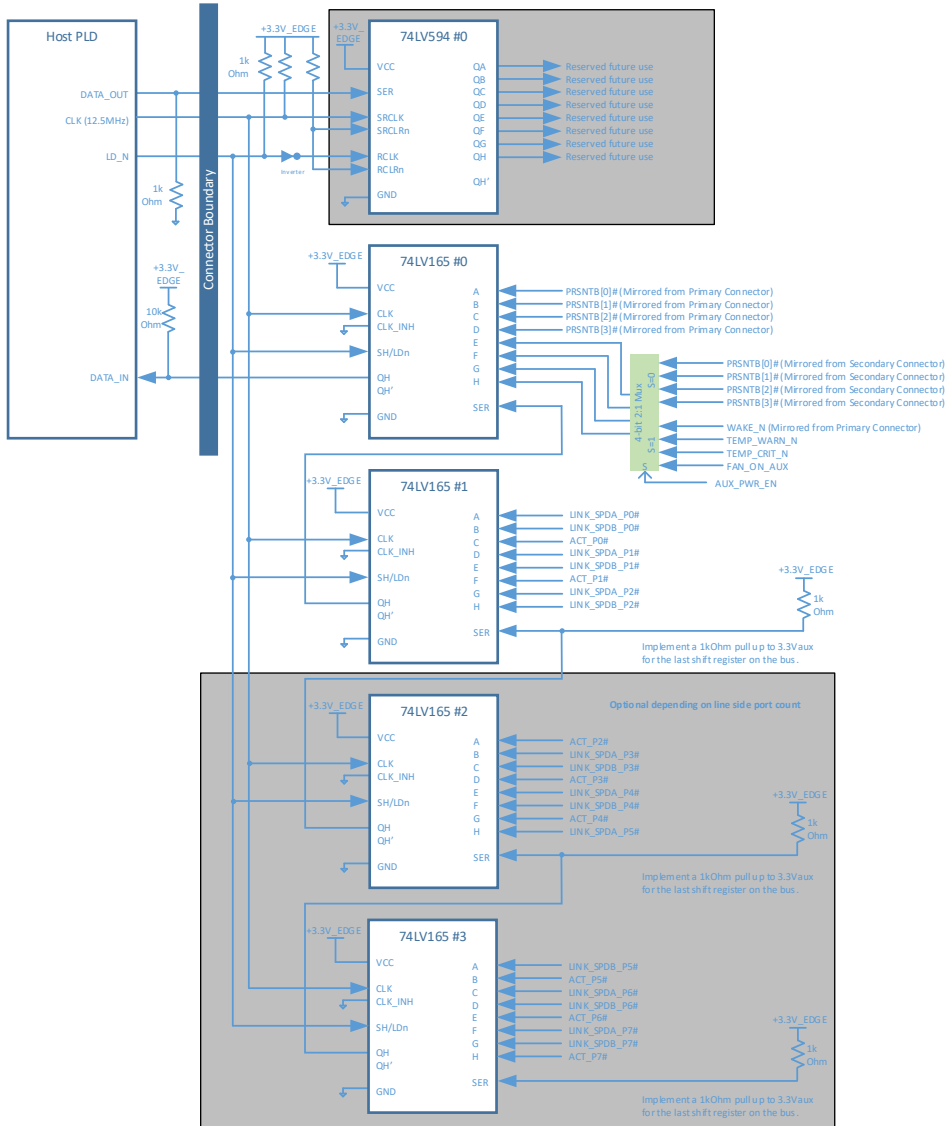
| Byte.bit | SCAN_DATA_IN Field Name | Default Value | Description |
|----------|----------------------------|---------------|---|
| 0.0 | PRSNTB[0]_P# | 0bX | PRSNTB[3:0]# bits shall reflect the same state as the signals on the Primary Connector. Connect these scan chain signals directly to the OCP NIC 3.0 card edge PRSNTB[3:0]# pins. The OCP NIC 3.0 implementer may alternatively choose to locally populate pull up and pull down resistors to these scan chain inputs as long as the PRSNTB[3:0]# values are the same on the scan chain and card edge. |
| 0.1 | PRSNTB[1]_P# | 0bX | |
| 0.2 | PRSNTB[2]_P# | 0bX | |
| 0.3 | PRSNTB[3]_P# | 0bX | |
| 0.4 | WAKE_N / PRSNTB[0]_S# | 0bX / 0bX | <p>PCIe WAKE_N signal shall reflect the same state as the signal on the Primary Connector.</p> <p>For LFF designs, this bit shall also serve as the PRSNTB[0]# signal from the Secondary Connector when the card is in ID Mode (AUX_PWR_EN==0). Multiplexing between the two functions shall be controlled via AUX_PWR_EN. Refer to Figure 98 for details.</p> |
| 0.5 | TEMP_WARN_N / PRSNTB[1]_S# | 0b1 / 0bX / | <p>Temperature monitoring pin from the on-card thermal solution. This pin shall be asserted low when the network silicon or transceiver module temperature sensors exceed the temperature warning threshold.</p> <p>For cards that do not require temperature reporting, the TEMP_WARN_N value shall be statically set to 0b1. Refer to Section 4.4 for details on temperature reporting.</p> <p>For LFF designs, this bit shall also serve as the PRSNTB[1]# signal from the Secondary Connector when the card is in ID Mode (AUX_PWR_EN==0). Multiplexing between the two functions shall be controlled via AUX_PWR_EN. Refer to Figure 98 for details.</p> |
| 0.6 | TEMP_CRIT_N / PRSNTB[2]_S# | 0b1 / 0bX | <p>Temperature monitoring pin from the on-card thermal solution. This pin shall be asserted low when the network silicon or transceiver module temperature sensors exceed the temperature critical threshold.</p> <p>For cards that do not require temperature reporting, the TEMP_CRIT_N value shall be</p> |

| Byte.bit | SCAN_DATA_IN Field Name | Default Value | Description |
|----------|-----------------------------|---------------|--|
| | | | <p>statically set to 0b1. Refer to Section 4.4 for details on temperature reporting.</p> <p>For LFF designs, this bit shall also serve as the PRSNTB[2]# signal from the Secondary Connector when the card is in ID Mode (AUX_PWR_EN==0). Multiplexing between the two functions shall be controlled via AUX_PWR_EN. Refer to Figure 98 for details.</p> |
| 0.7 | FAN_ON_AUX / PRSNTB[3]_S# / | 0b0 / 0bX | <p>When high, FAN_ON_AUX shall request the system fan to be enabled for extra cooling in Aux Power Mode.</p> <p>The FAN_ON_AUX bit shall be asserted when the network silicon or transceiver module cooling requested threshold has been exceeded. The temperature at which this assertion occurs is device dependent.</p> <p>The FAN_ON_AUX bit shall deassert when the network silicon or transceiver module temperature is at least 5 °C below the assertion threshold.</p> <p>0b0 – The system fan is not requested/off in Aux Power Mode. 0b1 – The system fan is requested/on in Aux Power Mode.</p> <p>For cards that do not require temperature reporting, the FAN_ON_AUX value shall be statically set to 0b0. Refer to Section 4.4 for details on temperature reporting.</p> <p>For LFF designs, this bit shall also serve as the PRSNTB[3]# signal from the Secondary Connector when the card is in ID Mode (AUX_PWR_EN==0). Multiplexing between the two functions shall be controlled via AUX_PWR_EN. Refer to Figure 98 for details.</p> |
| 1.0 | LINK_SPDA_P0# | 0b1 | <p>Port 0 link and speed A indication (max speed). Active low.</p> <p>0b0 – Link LED is illuminated on the host platform. 0b1 – Link LED is not illuminated on the host platform.</p> |

| Byte.bit | SCAN_DATA_IN Field Name | Default Value | Description |
|----------|-------------------------|---------------|---|
| | | | <p>On = link is detected on the port and is at the maximum speed. Off = the physical link is down, the link is not operating at the maximum speed or the port is disabled.</p> <p>Note: The link and speed A LED may also be blinked for use as port identification.</p> |
| 1.1 | LINK_SPDB_P0# | 0b1 | <p>Port 0 link and speed B indication (not max speed). Active low.</p> <p>0b0 – Link LED is illuminated on the host. 0b1 – Link LED is not illuminated on the host.</p> <p>On = link is detected on the port and is not at the maximum speed. Off = the physical link is down, the link is operating at the maximum speed, or the port is disabled.</p> <p>Note: The link and speed B LED may also be blinked for use as port identification.</p> |
| 1.2 | ACT_P0# | 0b1 | <p>Port 0 activity indication. Active low.</p> <p>0b0 – ACT LED is illuminated on the host. 0b1 – ACT LED is not illuminated on the host.</p> <p>Blinking = activity is detected on the port. The LED should blink at the rate of ½ Hz to 5 Hz. Off = no activity is detected on the port.</p> |
| 1.3 | LINK_SPDA_P1# | 0b1 | Port 1 link and speed A indication (max speed). Active low. |
| 1.4 | LINK_SPDB_P1# | 0b1 | Port 1 link and speed B indication (not max speed). Active low. |
| 1.5 | ACT_P1# | 0b1 | Port 1 activity indication. Active low. |
| 1.6 | LINK_SPDA_P2# | 0b1 | Port 2 link and speed A indication (max speed). Active low. |
| 1.7 | LINK_SPDB_P2# | 0b1 | Port 2 link and speed B indication (not max speed). Active low. |
| 2.0 | ACT_P2# | 0b1 | Port 2 activity indication. Active low. |
| 2.1 | LINK_SPDA_P3# | 0b1 | Port 3 link and speed A indication (max speed). Active low. |
| 2.2 | LINK_SPDB_P3# | 0b1 | Port 3 link and speed B indication (not max speed). Active low. |

| Byte.bit | SCAN_DATA_IN Field Name | Default Value | Description |
|----------|-------------------------|---------------|---|
| 2.3 | ACT_P3# | 0b1 | Port 3 activity indication. Active low. |
| 2.4 | LINK_SPDA_P4# | 0b1 | Port 4 link and speed A indication (max speed). Active low. |
| 2.5 | LINK_SPDB_P4# | 0b1 | Port 4 link and speed B indication (not max speed). Active low. |
| 2.6 | ACT_P4# | 0b1 | Port 4 activity indication. Active low. |
| 2.7 | LINK_SPDA_P5# | 0b1 | Port 5 link and speed A indication (max speed). Active low. |
| 3.0 | LINK_SPDB_P5# | 0b1 | Port 5 link and speed B indication (not max speed). Active low. |
| 3.1 | ACT_P5# | 0b1 | Port 5 activity indication. Active low. |
| 3.2 | LINK_SPDA_P6# | 0b1 | Port 6 link and speed A indication (max speed). Active low. |
| 3.3 | LINK_SPDB_P6# | 0b1 | Port 6 link and speed B indication (not max speed). Active low. |
| 3.4 | ACT_P6# | 0b1 | Port 6 activity indication. Active low. |
| 3.5 | LINK_SPDA_P7# | 0b1 | Port 7 link and speed A indication (max speed). Active low. |
| 3.6 | LINK_SPDB_P7# | 0b1 | Port 7 link and speed B indication (not max speed). Active low. |
| 3.7 | ACT_P7# | 0b1 | Port 7 activity indication. Active low. |

Figure 98: Scan Chain Connection Example



3.4.6 Power Supply Pins

This section provides the pin assignments for the power supply interface signals. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0 and amended in Section 3.9. An example connection diagram is shown in Figure 99.

Table 33: Pin Descriptions – Power

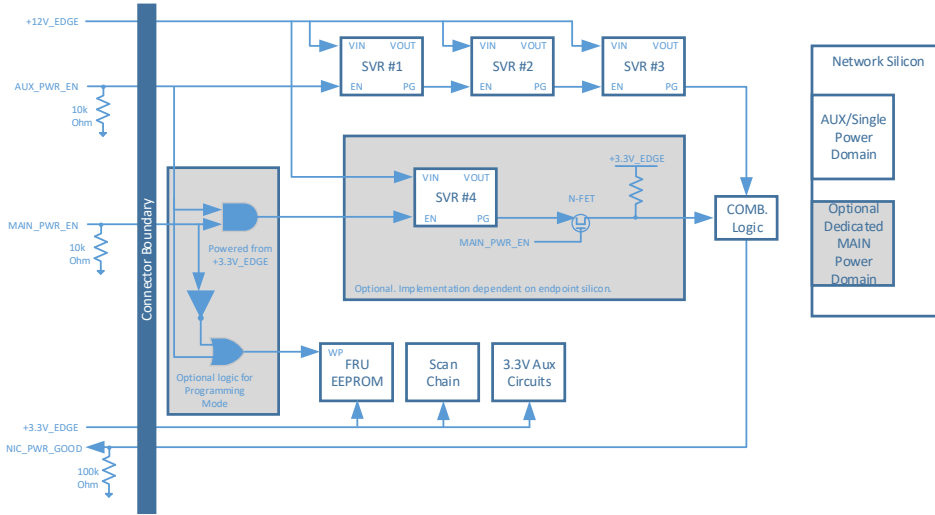
| Signal Name | Pin # | Baseboard Direction | Signal Description |
|-------------|------------------------|---------------------|--|
| GND | Various | GND | Ground return; a total of 46 ground pins are on the main 140-pin connector area. Additionally, a total of 4 ground pins are in the OCP bay area. Refer to Section 3.3 for details. |
| +12V_EDGE | B1, B2, B3, B4, B5, B6 | Power | <p>+12 V main or +12 V aux power; total of 6 pins per connector. The +12V_EDGE pins shall be rated to 1.1 A per pin with a maximum derated power delivery of 80 W.</p> <p>The +12V_EDGE power pins shall be within the rail tolerances as defined in Section 3.9 when the PWR_EN pin is driven high by the baseboard.</p> <p>The OCP NIC 3.0 card may optionally implement a fuse on +12V_EDGE to protect against electrical faults.</p> |
| +3.3V_EDGE | B11 | Power | <p>+3.3 V main or +3.3 V aux power; total of 1 pin per connector. The +3.3V_EDGE pin shall be rated to 1.1 A for a maximum derated power delivery of 3.63 W.</p> <p>The +3.3V_EDGE power pin shall be within the rail tolerances as defined in Section 3.9 when the PWR_EN pin is driven high by the baseboard.</p> <p>The OCP NIC 3.0 card may optionally implement a fuse on +3.3V_EDGE to protect against electrical faults.</p> |
| AUX_PWR_EN | B12 | Output | <p>Aux Power enable. Active high.</p> <p>This pin indicates that the baseboard +12V_EDGE and +3.3V_EDGE power are supplied per the Aux Power Mode requirements described in Section 3.9. Additionally, this signal notifies the OCP NIC 3.0 card to enable any power supplies that run only in the Aux Power Mode.</p> <p>AUX_PWR_EN is pinned out on both the Primary and Secondary Connector. For SFF, TSFF and LFF OCP NIC 3.0 cards, the AUX_PWR_EN connection shall be implemented on the Primary Connector only. The</p> |

| Signal Name | Pin # | Baseboard Direction | Signal Description |
|-------------|--------|---------------------|--|
| | | | <p>AUX_PWR_EN connection on the Secondary Connector is reserved for a future use case.</p> <p>This signal shall be pulled down to GND through a 10 kΩ resistor on the baseboard. This ensures the OCP NIC 3.0 card power is disabled until instructed to turn on by the baseboard.</p> <p>When low, the OCP NIC 3.0 card supplies running on aux power shall be disabled.</p> <p>When high, the OCP NIC 3.0 card supplies running on aux power shall be enabled.</p> <p>For OCP NIC 3.0 cards that do not use a separate “main power” domain circuitry (or can operate in a single power domain), the AUX_PWR_EN signal serves as the primary method to enable all the card power supplies.</p> <p>For OCP NIC 3.0 cards that support the Programming Mode power state, the condition <code>AUX_PWR_EN==0</code> and <code>MAIN_PWR_EN==1</code> shall prevent the aux power supplies from being enabled. An example of this logic is shown in Figure 99.</p> <p>It is expected that a baseboard will not drive signals other than SMBus and the Scan Chain to the OCP NIC 3.0 card when this signal is low.</p> |
| MAIN_PWR_EN | OCP_B2 | Output | <p>Main Power Enable. Active high.</p> <p>This pin indicates that the baseboard +12V_EDGE and +3.3V_EDGE power are supplied per the Main Power Mode requirements described in Section 3.9. Additionally, this signal notifies the OCP NIC 3.0 card to enable any power supplies that run only in the Main Power Mode.</p> <p>The MAIN_PWR_EN pin is driven by the baseboard for normal operation and may only be asserted when AUX_PWR_EN is already asserted. The MAIN_PWR_EN pin must be implemented on baseboard systems, but may optionally be used to control main power rail power supplies by the OCP NIC 3.0 card depending on the end point silicon implementation. Depending on the silicon vendor, end point devices may be able to</p> |

| Signal Name | Pin # | Baseboard Direction | Signal Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------|-------------|-------------------------------|---|------------------------------------|-------------|-------------------------------|--------------|------------|---|---|-----|---|---------|---|---|-----|---|----------------|---|---|-----|---|------------------|---|---|-----|---|-----------------|---|---|----|---|------------------------------------|---|---|----|---|------------------------------------|
| | | | <p>operate in a single power domain, or may require separate power domains to function.</p> <p>For OCP NIC 3.0 cards that support the Programming Mode power state, the condition AUX_PWR_EN == 0 and MAIN_PWR_EN == 1 shall prevent the main power supplies from being enabled. An example of this gating logic is shown in Figure 99.</p> <p>For baseboard implementations, this signal shall be pulled down to GND through a 10 kΩ resistor on the baseboard. This ensures the OCP NIC 3.0 card power is disabled until instructed to turn on by the baseboard.</p> <p>When low, the OCP NIC 3.0 card supplies running on main power shall be disabled.</p> <p>When high, the OCP NIC 3.0 card supplies running on main power shall be enabled.</p> <p>This pin may be left as a no connect for OCP NIC 3.0 cards that do not use a separate “main power” domain SVR circuitry.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| NIC_PWR_GOOD | OCP_B1 | Input | <p>NIC Power Good. Active high. This signal is driven by the OCP NIC 3.0 card.</p> <p>The NIC_PWR_GOOD signal is used to indicate when the aux power domain, and main power domain rails are within operational tolerances.</p> <p>The truth table shows the expected NIC_PWR_GOOD state for power up sequencing. This is dependent on the values of AUX_PWR_EN, MAIN_PWR_EN and the enabled power domains operating within design tolerances.</p> <table border="1"> <thead> <tr> <th>AUX_PWR_EN</th> <th>MAIN_PWR_EN</th> <th>Enabled Power domains nominal</th> <th>NIC_PWR_GOOD</th> <th>State Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>N/A</td> <td>0</td> <td>ID Mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>Yes</td> <td>1</td> <td>Aux Power Mode</td> </tr> <tr> <td>0</td> <td>1</td> <td>N/A</td> <td>0</td> <td>Programming Mode</td> </tr> <tr> <td>1</td> <td>1</td> <td>Yes</td> <td>1</td> <td>Main Power Mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>No</td> <td>0</td> <td>Transition state (non-operational)</td> </tr> <tr> <td>1</td> <td>1</td> <td>No</td> <td>0</td> <td>Transition state (non-operational)</td> </tr> </tbody> </table> | AUX_PWR_EN | MAIN_PWR_EN | Enabled Power domains nominal | NIC_PWR_GOOD | State Name | 0 | 0 | N/A | 0 | ID Mode | 1 | 0 | Yes | 1 | Aux Power Mode | 0 | 1 | N/A | 0 | Programming Mode | 1 | 1 | Yes | 1 | Main Power Mode | 1 | 0 | No | 0 | Transition state (non-operational) | 1 | 1 | No | 0 | Transition state (non-operational) |
| AUX_PWR_EN | MAIN_PWR_EN | Enabled Power domains nominal | NIC_PWR_GOOD | State Name | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | N/A | 0 | ID Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Yes | 1 | Aux Power Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | N/A | 0 | Programming Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Yes | 1 | Main Power Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | No | 0 | Transition state (non-operational) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | No | 0 | Transition state (non-operational) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Signal Name | Pin # | Baseboard Direction | Signal Description |
|-------------|-------|---------------------|--|
| | | | <p>Refer to the power up and power down sequencing diagrams (Figure 116 and Figure 117) for timing details.</p> <p>Where appropriate, designs that have a separate Main Power domain should also connect to the main power good indication to the NIC_PWR_GOOD signal via a FET to isolate the domains. Refer to Figure 99 for an example implementation.</p> <p>When low, this signal shall indicate that the OCP NIC 3.0 card power supplies are not yet within nominal tolerances or are in a fault condition after the power ramp times (T_{APL} and T_{MPL}) have expired.</p> <p>For cards that support the Programming Mode power state, the NIC_PWR_GOOD signal shall remain low when the OCP NIC 3.0 card is in Programming Mode as both the Aux Power Mode and Main Power Mode power supplies are disabled. Programming Mode shall only be used on OCP NIC 3.0 cards that advertise that the Programming Mode power state is supported per Section 4.10.3.</p> <p>For baseboards, this pin may be connected to the platform I/O hub as a NIC power health status indication. This signal shall be pulled down to ground with a 100 kΩ resistor on the baseboard to prevent a false power good indication if no OCP NIC 3.0 card is present.</p> <p>For OCP NIC 3.0 cards this signal shall indicate the OCP NIC 3.0 card power is “good” for the given power mode. This signal may be implemented by combinatorial logic, a cascaded power good tree or a discrete power good monitor output.</p> <p>When high, this signal should be treated as V_{REF} is available for NC-SI communications. Refer to timing parameter T4 in the DMTF DSP0222 specification for details.</p> |

Figure 99: Example Power Supply Topology



3.4.7 USB 2.0 (A68/A69) – Primary Connector Only

This section provides the pin assignments for the USB 2.0 interface signals. USB 2.0 is only defined for operation on the Primary Connector. USB 2.0 may be used for applications with end point silicon that requires a USB connection to the baseboard. Implementations may also allow for a USB-Serial or USB-JTAG translator for serial or JTAG applications. If multiple USB devices are required, an optional USB hub may be implemented on the OCP NIC 3.0 card. Downstream device discovery is completed as part of the bus enumeration per the USB 2.0 specification. A basic example connection diagram is shown in Figure 100. An example depicting USB-Serial and USB-JTAG connectivity with an USB hub is shown in Figure 101.

Table 34: Pin Descriptions – USB 2.0 – Primary Connector only

| Signal Name | Pin # | Baseboard Direction | Signal Description |
|----------------------|------------|---------------------|--|
| USB_DATn USB_DATp | A68 A69 | Bi-directional | <p>USB 2.0 Differential Pair – Primary Connector Only.</p> <p>A baseboard implementation shall provide a USB connection to the OCP NIC 3.0 primary connector.</p> <p>NIC implementations that require USB shall connect the bus to the end point silicon. This pin shall be left as a no connect if it is not used on the OCP NIC 3.0 card.</p> <p>The USB pins shall be directly connected between the end point silicon or USB device and the card gold fingers.</p> <p>The USB interface shall be based on a $V_{BUS} = 5\text{ V}$ per the USB specification. Both the baseboard and NIC device shall be capable of driving a differential signal using 3.3 V logic. Differential termination (V_{TERM}) pull-up values on the D+ line, if implemented, shall also be 3.3V compliant. The OCP NIC 3.0 card may implement protection diodes and is up to the adapter vendor for placement.</p> <p>To prevent leakage paths, a baseboard shall not use USB pull up resistors on the USB_DATp/n lines to indicate the bus data transmission rate. If used, pull up resistors shall only exist on the NIC side.</p> <p>The AUX_PWR_EN signal may be used for downstream USB devices that require a V_{BUS} detection indication. Designers would have to ensure the V_{BUS} detection threshold supports 3.3V signaling. Examples of this may include USB-serial converting devices.</p> |

Figure 100: USB 2.0 Connection Example – Basic Connectivity

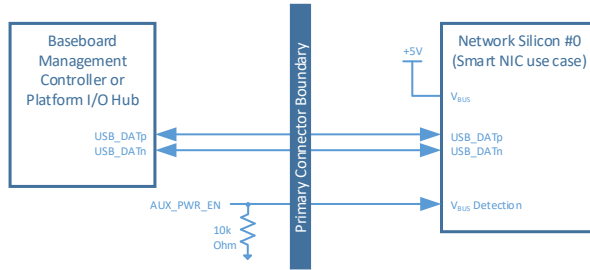
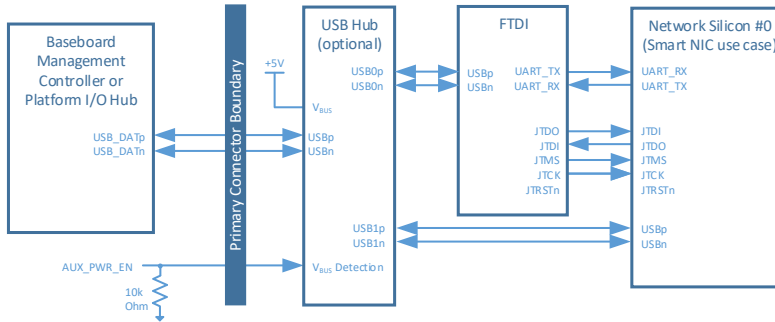


Figure 101: USB 2.0 Connection Example – USB-Serial / USB-JTAG Connectivity



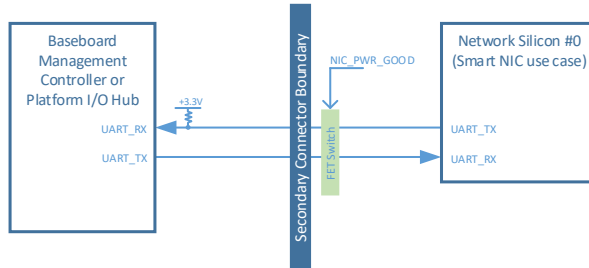
3.4.8 UART (A68/A69) – Secondary Connector Only

This section provides the pin assignments for the UART interface signals. UART is only defined for operation on the Secondary Connector. The UART pins may be used with end point silicon that require console redirection over the baseboard – such as LFF SmartNICs. An example connection diagram is shown in Figure 102.

Table 35: Pin Descriptions – UART – Secondary Connector Only

| Signal Name | Pin # | Baseboard Direction | Signal Description |
|-------------|-------|---------------------|---|
| UART_RX | A68 | Input | <p>UART Receive. +3.3 V signaling levels. Secondary Connector Only.</p> <p>A baseboard implementation shall provide a UART receive connection from the OCP NIC 3.0 connector. The UART_RX pin shall be pulled up to +3.3 V_{AUX} on the baseboard to prevent erroneous data reception when the OCP NIC 3.0 card is powered off or not present.</p> <p>NIC implementations that require a UART shall connect the network silicon UART_RX pin to the UART_TX pin on the OCP NIC 3.0 connector. This pin shall be left as a no connect if it is not used on the OCP NIC 3.0 card.</p> <p>The UART_RX pin shall be buffered on the NIC to prevent a leakage path into unpowered silicon when the card is in ID Mode. The buffer may be controlled via a local “Power Good” indicator.</p> |
| UART_TX | A69 | Output | <p>UART Transmit. +3.3 V signaling levels. Secondary Connector Only.</p> <p>A baseboard implementation shall provide a UART transmit connection to the OCP NIC 3.0 connector.</p> <p>NIC implementations that require a UART shall connect the UART_TX pin from the OCP NIC 3.0 connector to the target silicon UART_RX pin. This pin shall be left as a no connect if it is not used on the OCP NIC 3.0 card.</p> <p>The UART_TX pin shall be buffered on the NIC to prevent a leakage path into unpowered silicon when the card is in ID Mode. The buffer may be controlled via a local “Power Good” indicator.</p> |

Figure 102: UART Connection Example



3.4.9 RFU[1:4] Pins

This section provides the pin assignments for the RFU[1:4] interface signals.

Table 36: Pin Descriptions – RFU[1:4]

| Signal Name (Primary / Secondary) | Pin # | Baseboard Direction | Signal Description |
|-----------------------------------|-------|---------------------|--|
| RFU1 / RFU3, N/C | B68 | Input / Output | Reserved future use pins. These pins shall be left as no connect. These pins may also be used as a differential pair for future implementations. In this release of the OCP NIC 3.0 specification, the RFU[1:2] pins are defined on the Primary Connector. RFU[3:4] are defined on the Secondary Connector. A total of two reserved pins are available for the SFF and TSFF; a total of four reserved pins are available for the LFF. |
| RFU2 / RFU4, N/C | B69 | | |

3.5 PCIe Bifurcation Mechanism

OCP NIC 3.0 baseboards and OCP NIC 3.0 cards support multiple bifurcation combinations. Single socket baseboards with a single or multiple root ports, as well as a multi-socket baseboards with a single or multiple root ports are supported. The bifurcation mechanism also supports OCP NIC 3.0 cards with a single or multiple end points. These features are accomplished via I/O pins on the Primary and Secondary Connector:

- PRSNTA#, PRSNTB[3:0]#. The PRSNTA# pin shall connect to the PRSNTB# pins as a hard coded value on the OCP NIC 3.0 card. The encoding of the PRSNTB[3:0]# pins allows the baseboard to determine the PCIe Links available on the OCP NIC 3.0 card. PRSNTA# and PRSNTB[3:0]# pins exist for each connector. For the SFF and TSFF, a baseboard shall read the pins associated with the Primary Connector to determine the card type. For the LFF, a baseboard shall read the pins associated with both the Primary and Secondary Connector to determine the card type.
- BIF[2:0]#. The BIF# pin states shall be controlled by the baseboard to allow the baseboard to override the default end point bifurcation for silicon that support bifurcation. Additional combinatorial logic is required and is specific to the card silicon. The combinatorial logic is not covered in this specification. The BIF[2:0]# pins may optionally be hardcoded for baseboards that do not require a dynamic bifurcation override. BIF[2:0]# pins exist on each connector.

A high-level bifurcation connection diagram is shown in Figure 91.

3.5.1 PCIe OCP NIC 3.0 Card to Baseboard Bifurcation Configuration (PRSNTA#, PRSNTB[3:0]#)

The OCP NIC 3.0 card to baseboard configuration mechanism consists of four dual use pins (PRSNTB[3:0]#) on the OCP NIC 3.0 card and a grounded PRSNTA# pin on the baseboard per connector. For the SFF and TSFF, a baseboard shall read the pins associated with the Primary Connector to determine the card type. For the LFF, a baseboard shall read the pins associated with both the Primary and Secondary Connector to determine the card type. These pins provide card presence detection as well as mechanism to notify the baseboard of the pre-defined PCIe lane width capabilities. The PRSNTB[3:0]# pins are pulled up to +3.3V_EDGE on the baseboard and are active low signals. A state of 0b1111 indicates that no card is present in the connector(s). Depending on the capabilities of the OCP NIC 3.0 card, a selection of PRSNTB[3:0]# signals may be strapped to the PRSNTA# signal and is pulled low by the baseboard. The encoding of the PRSNTB[3:0]# bits is shown in ~~Table 37~~ **Table 36** for x32, x16 and x8 PCIe cards. While SFF and LFF cards are allowed in an LFF compliant slot, the condition where the Primary Connector PRSNTB[3:0]# equals 0b1111 and the Secondary Connector PRSNTB[3:0]# pins is not equal to 0b1111 is invalid.

3.5.2 PCIe Baseboard to OCP NIC 3.0 Card Bifurcation Configuration (BIF[2:0]#)

Three signals (BIF[2:0]#) are driven by the baseboard to notify requested bifurcation on the OCP NIC 3.0 card silicon. This allows the baseboard to set the lane configuration on the OCP NIC 3.0 card that supports multiple bifurcation options. BIF[2:0]# pins exist on each connector. For the SFF and TSFF, the BIF[2:0]# pins associated with the Primary Connector are used. For the LFF, the BIF[2:0]# pins associated with both the Primary and Secondary Connector are used to determine the requested bifurcation.

For example, a baseboard that has four separate hosts that support a 4 x4 connection, should appropriately drive the BIF[2:0]# pins per ~~Table 37~~ [Table 36](#) and indicate to the SFF/TSFF OCP NIC 3.0 card silicon to setup a 4 x4 configuration.

As previously noted, the BIF[2:0]# signals require additional combinatorial logic to decode the BIF[2:0]# value and appropriately apply it to the end-point silicon. The combinatorial logic is not covered in the specification as its implementation is specific to the vendor silicon used.

3.5.3 PCIe Bifurcation Decoder

The combination of the PRSNTB[3:0]# and BIF[2:0]# pins deterministically sets the PCIe lane width for a given combination of baseboard and OCP NIC 3.0 cards. ~~Table 37~~ [Table 36](#) shows the resulting number of PCIe links and its width for known combinations of baseboards and OCP NIC 3.0 cards. A copy of this bifurcation decoder, along with a detailed PCIe lane, PERST# and REFCLK assignments is available on the OCP NIC 3.0 Wiki site. Please refer to: <https://www.opencompute.org/wiki/Server/Mezz>.

Note 1: Baseboard vendors do not have to support the full complement of cases enumerated in the bifurcation table. Instead, baseboard vendors may choose to support only a subset of cases that is applicable to their hardware topology.

Note 2: The baseboard must disable PCIe lanes during the initialization phase if the number of detected PCIe links are greater than what is supported on the baseboard to prevent a nondeterministic solution. For example, if the baseboard only supports a 1 x16 connection, and the OCP NIC 3.0 card only supports a 2 x8 connection, the baseboard must disable PCIe lanes 8-15 to prevent any potential LTSSM issues during the discovery phase.

Note 3: Due to separate PCIe REFCLKs and power state timing differences in multi-host configurations, ~~Table 37~~ [Table 36](#) shows the expected resulting links for a given baseboard and OCP NIC 3.0 card combination.

3.5.4 Bifurcation Detection Flow

The following detection flow shall be used to determine the resulting link count and lane width based on the baseboard and OCP NIC 3.0 card configurations.

1. The baseboard shall read the state of the PRSNTB[3:0]# pins for the Primary Connector and Secondary Connector (if applicable). An OCP NIC 3.0 card is present in the system if the resulting value is not 0b1111 on the Primary Connector.
2. Firmware determines the OCP NIC 3.0 card PCIe lane width capabilities per ~~Table 37~~Table 36 by reading the PRSNTB[3:0]# pins.
3. The baseboard reconfigures the PCIe bifurcation on its ports to match the highest common lane width and lowest common link count on the card.
4. For cases where the baseboard request a link count override (such as requesting a 4-host baseboard requesting 4 x4 operation on a supported card that would otherwise default to a 2 x8 case), the BIF[2:0]# pins shall be asserted as appropriate. Asserting the BIF[2:0]# pins assumes the OCP NIC 3.0 card supports the requested link override.
 - o Note: For cards that are already powered up, BIF[2:0]# reconfiguration requires a transition back to ID Mode. During this transition, the card power rails are inactive and manageability links may be briefly lost due to the RBT isolation state.
5. The BIF[2:0]# pins must be in their valid states upon the assertion of AUX_PWR_EN. The BIF[2:0]# pins shall remain static after AUX_PWR_EN is asserted. The pins are not allowed to change states when the OCP NIC 3.0 card is powered on.
6. AUX_PWR_EN is asserted. An OCP NIC 3.0 card is allowed a max ramp time T_{APL} between AUX_PWR_EN assertion and NIC_PWR_GOOD assertion.
7. MAIN_PWR_EN is asserted. An OCP NIC 3.0 card is allowed a max ramp time T_{MPL} between MAIN_PWR_EN assertion and NIC_PWR_GOOD reassertion. For cards that do not have a separate Aux and Main power domain, this state is an unconditional transition to NIC_PWR_GOOD.
8. The PCIe REFCLK shall become valid a minimum of 100 μ s before the deassertion of PERST#.
9. PERST# shall be deasserted >1 s after NIC_PWR_GOOD assertion as defined in Figure 116. Refer to Section 3.11 for timing details.

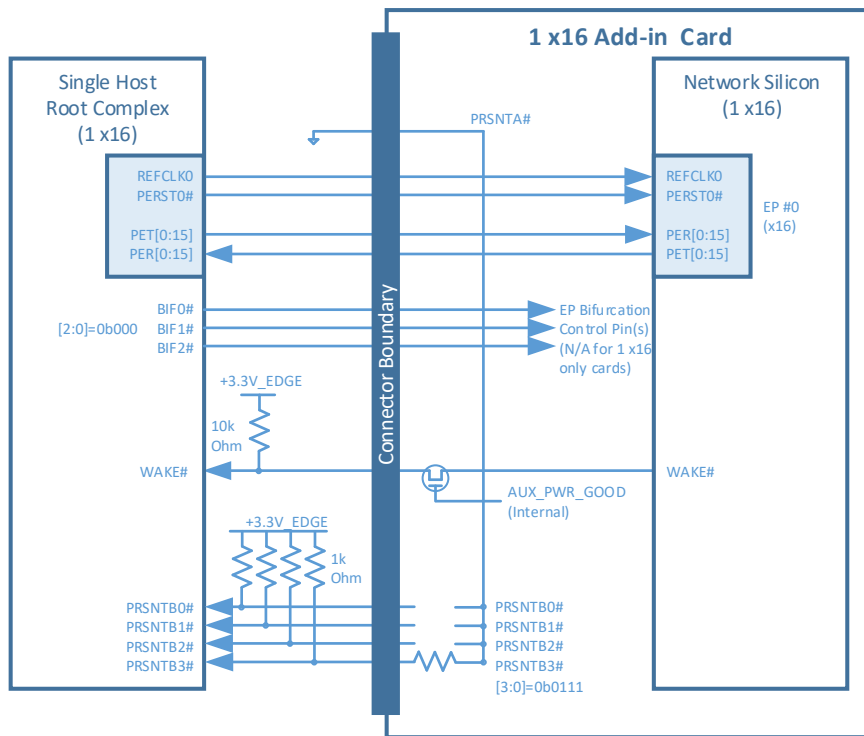
3.5.5 PCIe Bifurcation Examples

For illustrative purposes, the following figures show several common bifurcation permutations using a SFF.

3.5.5.1 Single Host (1 x16) Baseboard with a 1 x16 OCP NIC 3.0 Card (Single Controller)

Figure 103 illustrates a single host baseboard that supports x16 with a single controller OCP NIC 3.0 card that also supports x16. The `PRSTNB[3:0]#` state is 0b0111. The `BIF[2:0]#` state is 0b000 to set the card as a 1x16 for bifurcation capable controllers. For controllers without bifurcation support, the `BIF[2:0]` pin connections are not required on the card. The `PRSTNB` encoding notifies the baseboard that this card is only capable of 1 x16. The single host baseboard determines that it is also capable of supporting 1 x16. The resulting link width is 1 x16.

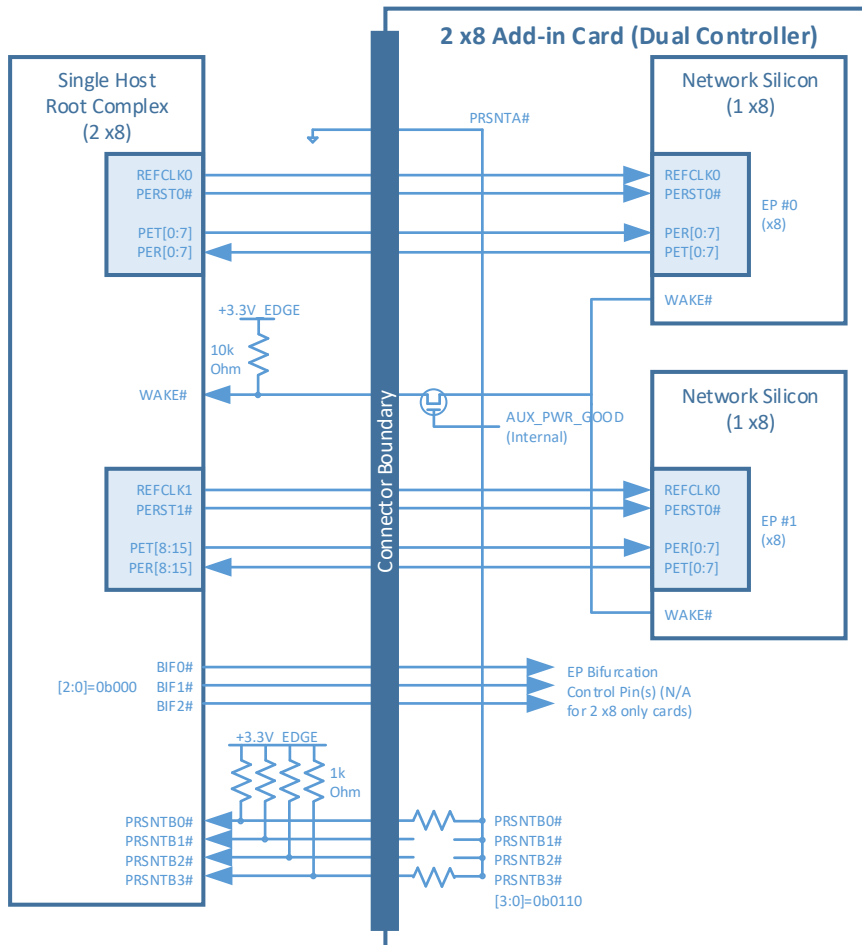
Figure 103: Single Host (1 x16) and 1 x16 OCP NIC 3.0 Card (Single Controller)



3.5.5.2 Single Host (2 x8) Baseboard with a 2 x8 OCP NIC 3.0 Card (Dual Controllers)

Figure 104 illustrates a single host baseboard that supports 2 x8 with a dual controller OCP NIC 3.0 card that also supports 2 x8. The PRSNTB[3:0]# state is 0b0110. The BIF[2:0]# state is 0b000 in this example because the network card only supports a 2x8. The PRSNTB encoding notifies the baseboard that this card is only capable of 2 x8. The single host baseboard determines that it is also capable of supporting 2 x8. The resulting link width is 2 x8.

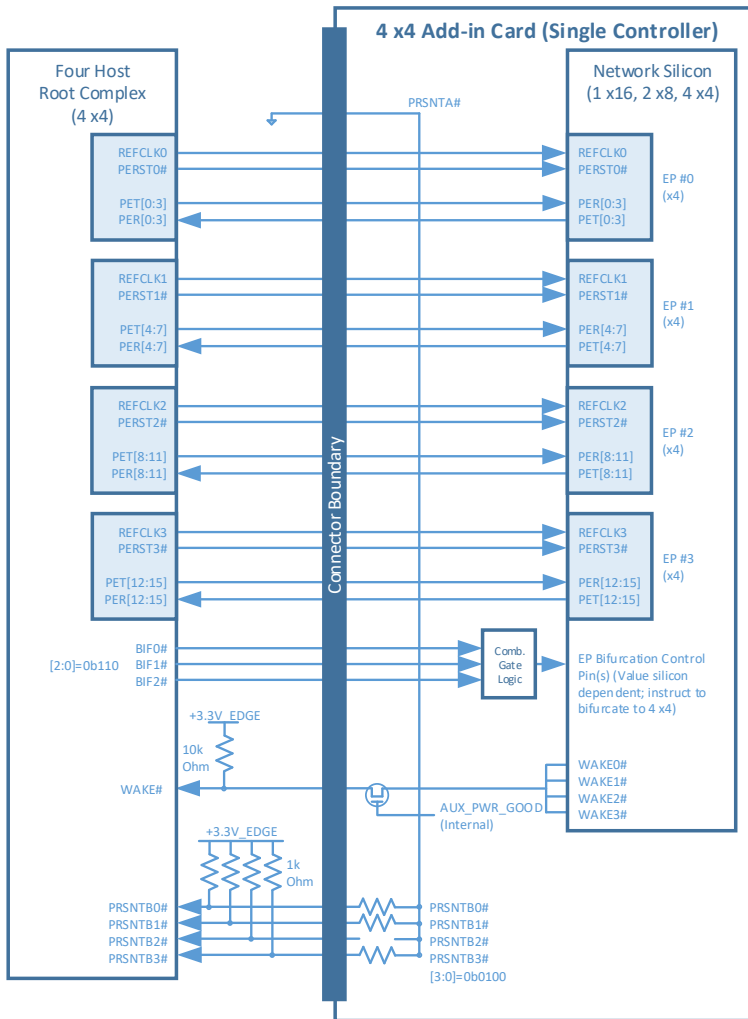
Figure 104: Single Host (2 x8) and 2 x8 OCP NIC 3.0 Card (Dual Controllers)



3.5.5.3 Quad Host (4 x4) Baseboard with a 4 x4 OCP NIC 3.0 Card (Single Controller)

Figure 105 illustrates a quad host baseboard that supports 4 x4 with a single controller OCP NIC 3.0 card that supports 1 x16, 2 x8 and 4 x4. The PRSNTB[3:0]# state is 0b0100. The BIF[2:0]# state in this example is 0b110 as the end point network controller is forced to bifurcate to 4 x4. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16, 2 x8 and 4 x4. The quad host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

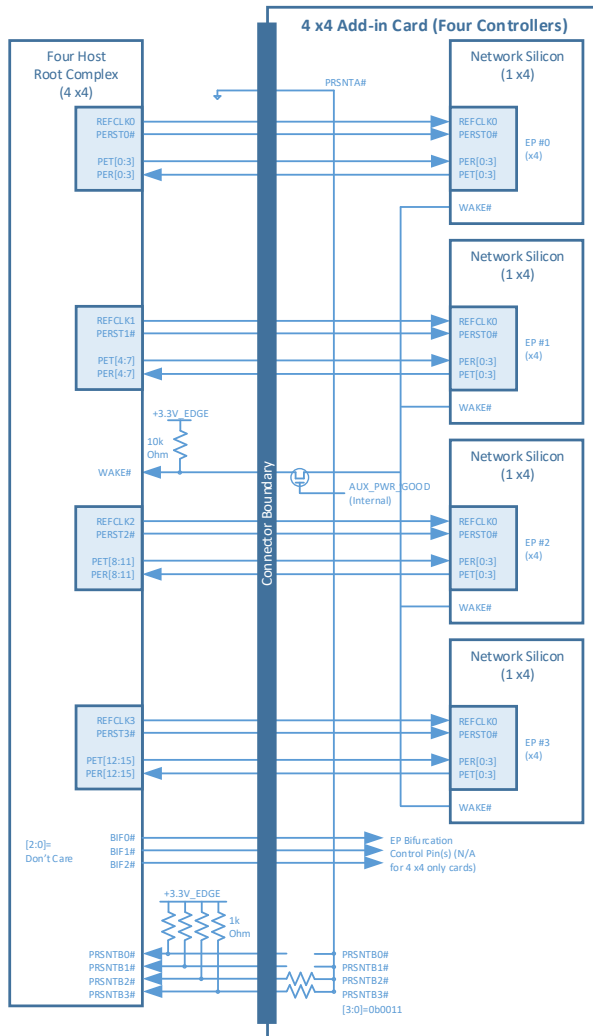
Figure 105: Quad Hosts (4 x4) and 4 x4 OCP NIC 3.0 Card (Single Controller)



3.5.5.4 Quad Host (4 x4) Baseboard with a 4 x4 OCP NIC 3.0 Card (Quad Controllers)

Figure 106 illustrates a quad host baseboard that supports 4 x4 with a quad controller OCP NIC 3.0 card that supports 4 x4. The PRSNTB[3:0]# state is 0b0011. The BIF[2:0]# state is a don't care value as there is no need to instruct the end-point network controllers to a specific bifurcation (each controller only supports 1x4 in this example). The PRSNTB encoding notifies the baseboard that this card is only capable of 4 x4. The quad host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

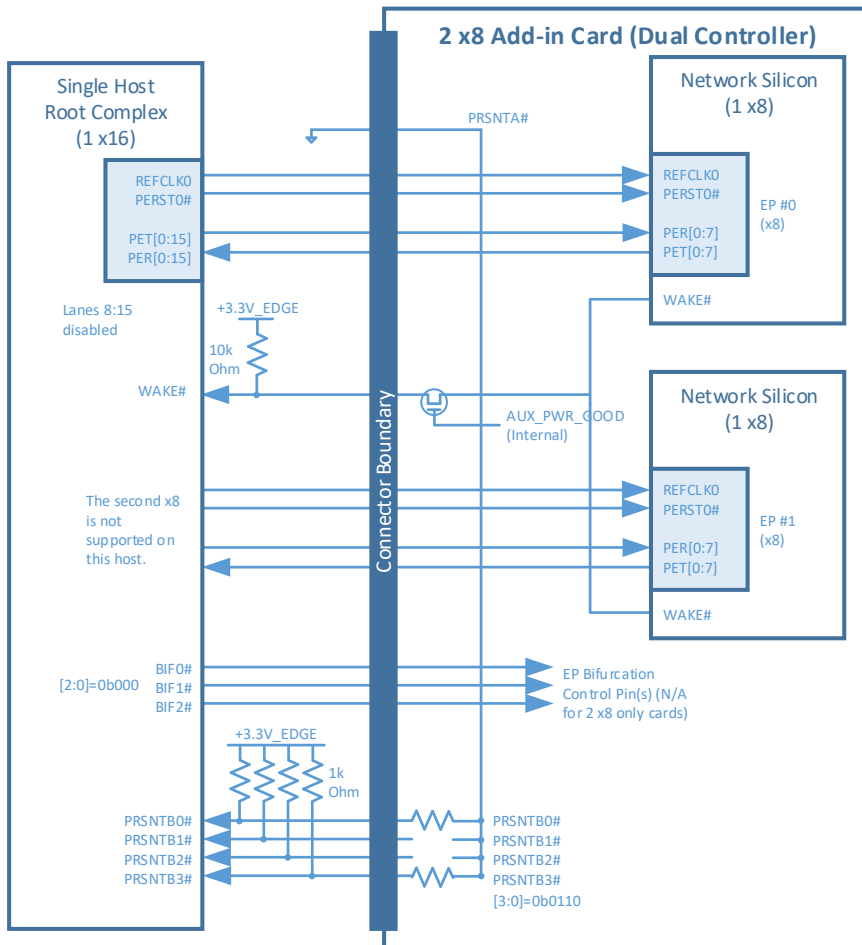
Figure 106: Quad Hosts (4 x4) and 4 x4 OCP NIC 3.0 Card (Quad Controllers)



3.5.5.5 Single Host (1 x16, no Bifurcation) Baseboard with a 2 x8 OCP NIC 3.0 Card (Dual Controller)

Figure 107 illustrates a single host baseboard that supports 1 x16 with a dual controller OCP NIC 3.0 card that supports 2 x8. The PRSNTB[3:0]# state is 0b0110. The BIF[2:0]# state is 0b000 as each silicon instance only supports 1x8. The PRSNTB encoding notifies the baseboard that this card is only capable of 2 x8. The quad host baseboard determines that it is capable of 1x 16, but down shifts to 1 x8. The resulting link width is 1 x8 and only on endpoint 0.

Figure 107: Single Host with no Bifurcation (1 x16) and 2 x8 OCP NIC 3.0 Card (Dual Controllers)



3.6 PCIe REFCLK and PERST# Mapping

The OCP NIC 3.0 specification allows for up to four PCIe REFCLKs and PERST# signals on the Primary Connector and up to two PCIe REFCLKs and PERST# signals on the Secondary Connector. The association of each REFCLK and PERST# is based on the card PCIe Link number and is shown in [Table 38](#)[Table 37](#). Cards that implement both the Primary and Secondary Connectors have a total of up to 6 available REFCLKs and 6 PERST# signals.

REFCLK[0:3] and PERST[0:3]# are defined for use in this release of the specification. REFCLK[4:5] and PERST[4:5]# are not currently defined for use. The following tables enumerate the REFCLK and PERST# mapping for SFF and TSFF cards for 1, 2 and 4 links; LFF cards for 1, 2, 4 and 8 links. For a LFF 8 link scenario, the lower x4 “link-a” and upper x4 “link-b” of each x8 lanes are expected to use the same REFCLK and PERST (see [Table 40](#)[Table 39](#)). A 1:2 clock driver circuit is expected on the OCP NIC 3.0 card in this case.

For multi-host use cases, the baseboard may require a multiplexer circuit to direct the Host 1, Host 2 PCIe reference clock to the connector REFCLK1 signal to maintain proper REFCLK associations for a card with two links. Refer to the diagrams in Sections 3.6.1 and 3.6.2.

Table 38: PCIe REFCLK and PERST Associations

| REFCLK # | PERST # | Description | Availability (Connector) |
|----------|---------|-------------------------|---------------------------|
| REFCLK0 | PERST0# | Associated with Link 0. | Primary Connector only. |
| REFCLK1 | PERST1# | Associated with Link 1. | Primary Connector only. |
| REFCLK2 | PERST2# | Associated with Link 2. | Primary Connector only. |
| REFCLK3 | PERST3# | Associated with Link 3. | Primary Connector only. |
| REFCLK4 | PERST4# | Not used. | Secondary Connector only. |
| REFCLK5 | PERST5# | Not used. | Secondary Connector only. |

Table 39: SFF, TSFF PCIe Link / REFCLKn / PERSTn mapping for 1, 2 and 4 Links

| Primary Connector | | | |
|--------------------------------|-------------------------------|-------------------------------|-------------------------------|
| Lanes [0:3] | Lanes [4:7] | Lanes [8:11] | Lanes [12:15] |
| Link 0 – x16, REFCLK0, PERST0# | | | |
| Link 0 – x8, REFCLK0, PERST0# | | Link 1 – x8, REFCLK1, PERST1# | |
| Link 0 – x4, REFCLK0, PERST0# | Link 1 – x4, REFCLK1, PERST1# | Link 2 – x4, REFCLK2, PERST2# | Link 3 – x4, REFCLK3, PERST3# |

Table 40: LFF PCIe Link / REFCLKn / PERSTn mapping for 1, 2, 4 and 8 Links

| Primary Connector | | | | Secondary Connector | | | |
|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|
| Lanes [0:3] | Lanes [4:7] | Lanes [8:11] | Lanes [12:15] | Lanes [16:19] | Lanes [20:23] | Lanes [24:27] | Lanes [28:31] |
| Link 0 – x32, REFCLK0, PERST0# | | | | Link 2 – x16, REFCLK2, PERST2# | | | |
| Link 0 – x8, REFCLK0, PERST0# | | Link 1 – x8, REFCLK1, PERST1# | | Link 2 – x8, REFCLK2, PERST2# | | Link 3 – x8 REFCLK3, PERST3# | |
| Link 0a – x4, REFCLK0, PERST0# | Link 0b – x4, REFCLK0, PERST0# | Link 1a – x4, REFCLK1, PERST1# | Link 1b – x4, REFCLK1, PERST1# | Link 2a – x4, REFCLK2, PERST2# | Link 2b – x4, REFCLK2, PERST2# | Link 3a – x4, REFCLK3, PERST3# | Link 3b – x4, REFCLK3, PERST3# |

3.6.1 SFF, TSFF PCIe REFCLK and PERST# Mapping

The following figures show the Link n, REFCLKn, PERSTn mapping for the SFF/TSFF with 1, 2 and 4 links as single, dual and quad host configurations. For clarity, the PCIe sideband signals are not illustrated in this section. Please refer to the signal descriptions and associated diagrams for connectivity requirements.

Figure 108: SFF/TSFF PCIe REFCLK Mapping – Single Host – 1, 2 and 4 links

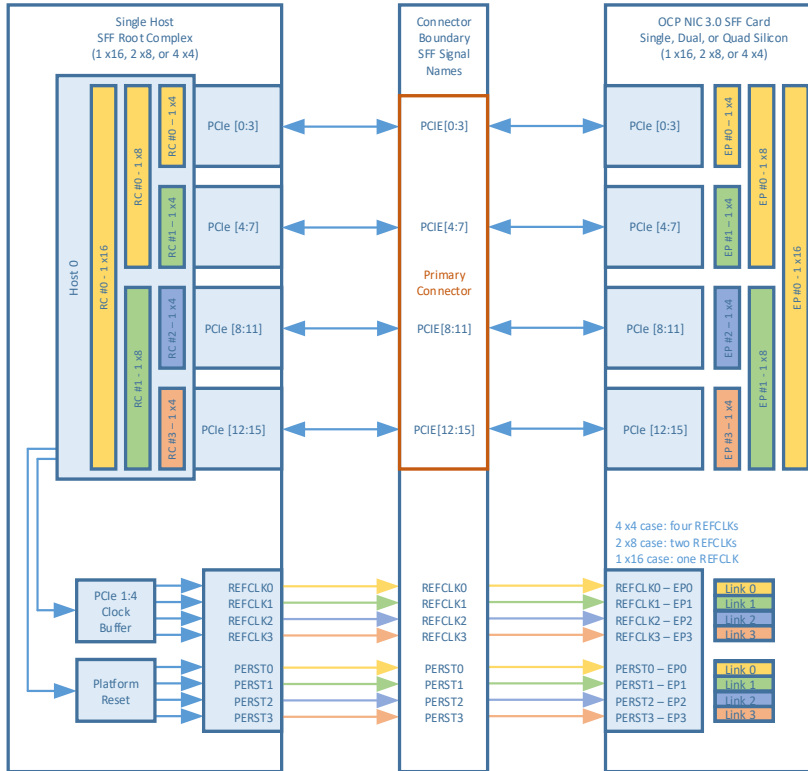
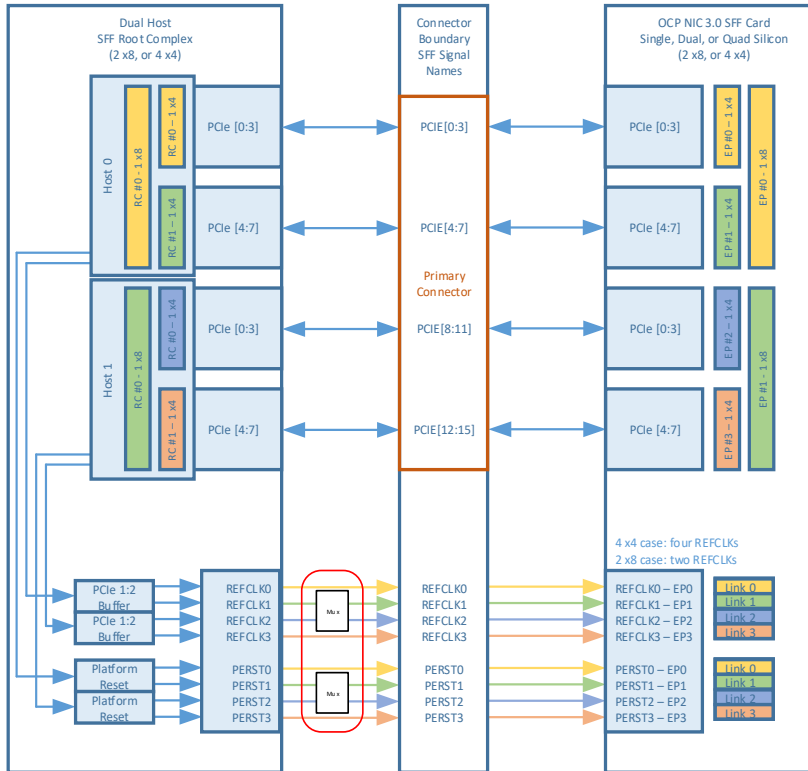
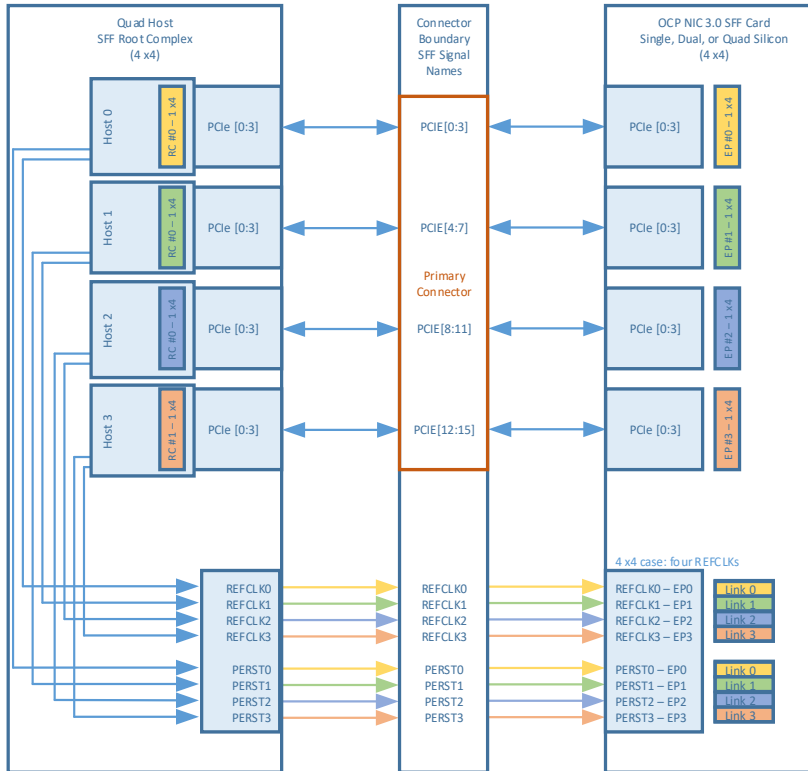


Figure 109: SFF/TSFF PCIe REFCLK Mapping – Dual Host – 2 and 4 links



Note: For dual host applications that connect to a two-link endpoint, the baseboard Host 1 REFCLK0 and PERST0 signal needs to be multiplexed to the REFCLK1 and PERST1 pins of the OCP NIC 3.0 card edge. This ensures the mandated Link n, REFCLKn and PERSTn mappings are maintained.

Figure 110: SFF/TSFF PCIe REFCLK Mapping – Quad Host – 4 Links



Note: For quad host applications that connect to a two link endpoint, the baseboard Host 2 REFCLK and PERST signal needs to be multiplexed to the REFCLK1 and PERST1 pins of the OCP NIC 3.0 card edge. This ensures the mandated Link n, REFCLKn and PERSTn mappings are maintained.

3.6.2 LFF PCIe REFCLK and PERST# Mapping

The following figures show the Link n, REFCLKn, PERSTn mapping for the LFF with 1, 2 and 4 links as single, dual and quad host configurations. For clarity, the PCIe sideband signals are not illustrated this section. Please refer to the signal descriptions and associated diagrams for connectivity requirements.

Figure 111: LFF PCIe REFCLK Mapping – Single Host – 1, 2 and 4 links

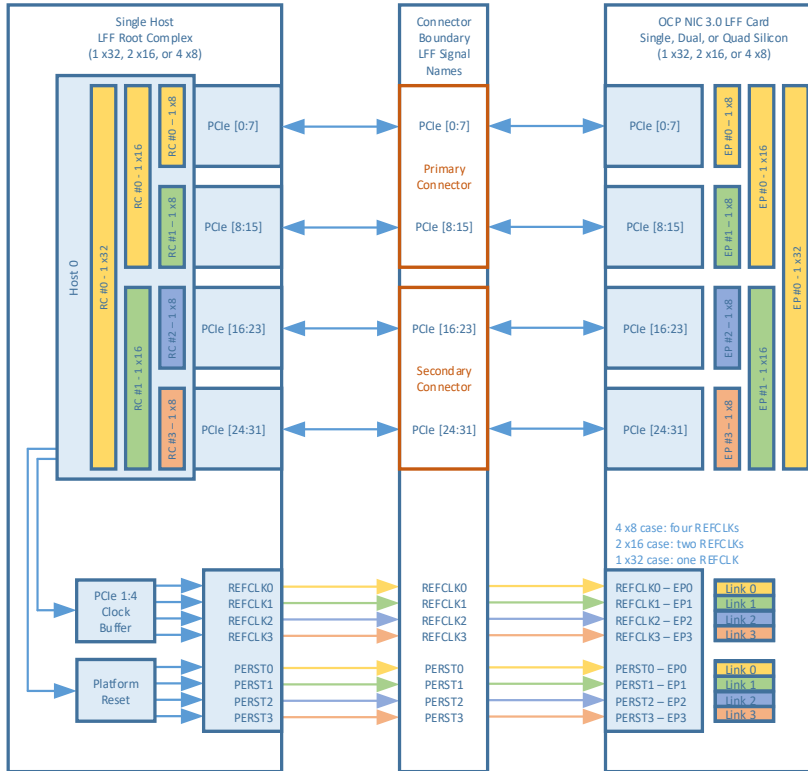
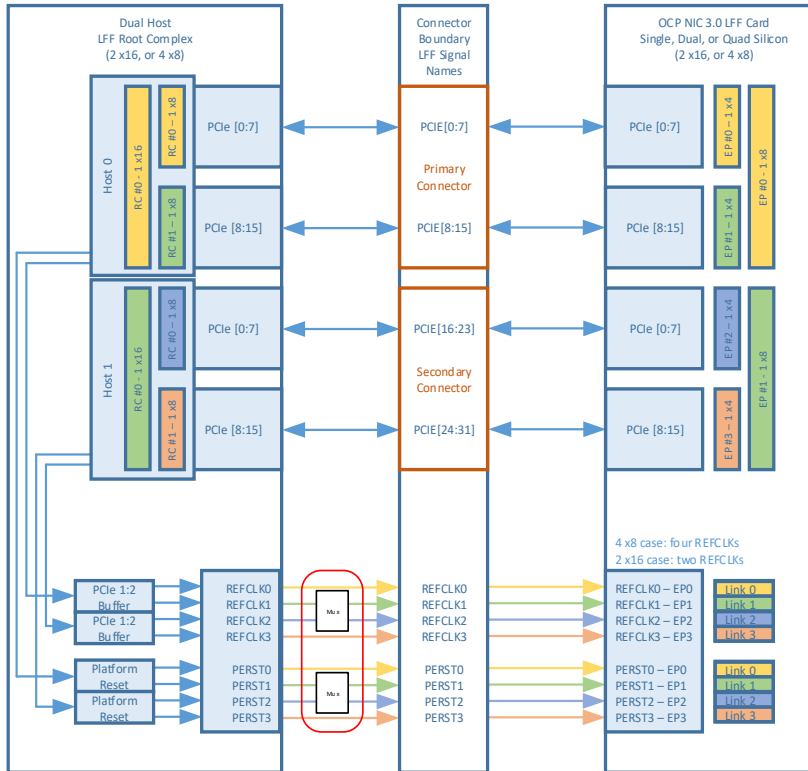
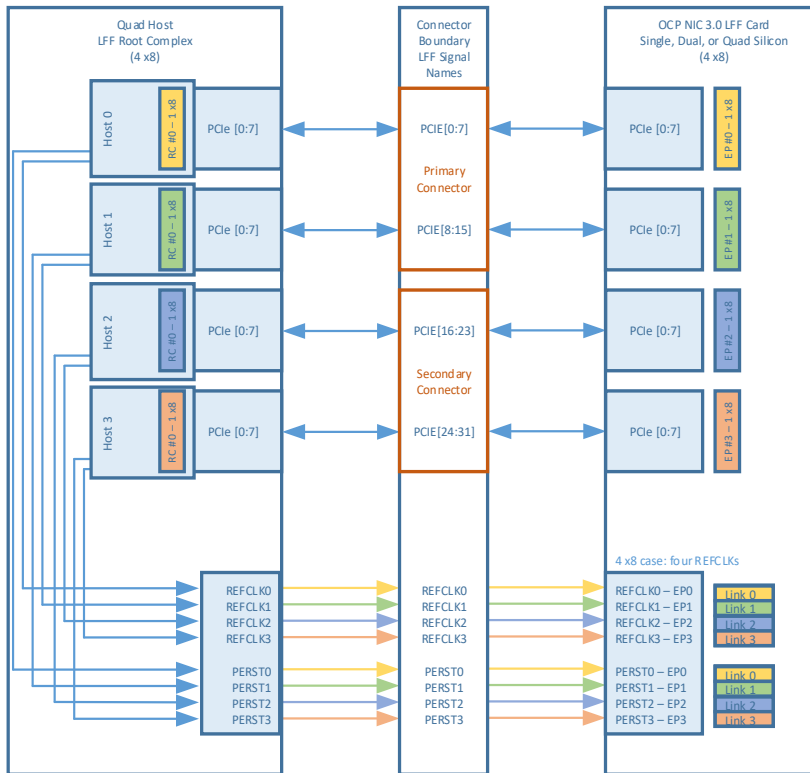


Figure 112: LFF PCIe REFCLK Mapping – Dual Host – 2 and 4 links



Note: For dual host applications that connect to a two link endpoint, the baseboard Host 1 REFCLK0 and PERST0 signal needs to be multiplexed to the REFCLK1 and PERST1 pins of the OCP NIC 3.0 card edge. This ensures the mandated Link n, REFCLKn and PERSTn mappings are maintained.

Figure 113: LFF PCIe REFCLK Mapping – Quad Host – 4 Links



Note: For quad host applications that connect to a two link endpoint, the baseboard Host 2 REFCLK and PERST signal needs to be multiplexed to the REFCLK1 and PERST1 pins of the OCP NIC 3.0 card edge. This ensures the mandated Link n , REFCLK n and PERST n mappings are maintained.

3.6.3 REFCLK and PERST# Mapping Expansion

For cases where bifurcation are permissible on the baseboard and OCP NIC 3.0 card, an expanded PCIe Bifurcation spreadsheet is available on the OCP Wiki site:

<https://www.opencompute.org/wiki/Server/Mezz>.

Implementers shall use the spreadsheet version that is aligned with this version of the OCP NIC 3.0 specification.

The spreadsheet enumerates ~~all of all~~ the ~~supported~~ PCIe link, lane and REFCLK mappings for each supported configuration. The bifurcation decoder is shown in Section 3.5.3.

3.7 Port Numbering and LED Implementations

The OCP NIC 3.0 I/O bracket shall provide port labeling for user identification.

LEDs shall be implemented on the OCP NIC 3.0 I/O bracket when there is sufficient space for local indication. LEDs are typically placed on the primary side. LEDs may be optionally implemented on the secondary side of the card for space constrained implementations. LEDs may be remotely implemented on the card Scan Chain (as defined in Section 3.4.5) for link/activity indication on the baseboard. LED configurations for the local and remote cases are described in the sections below. In all cases, the actual link rate may be directly queried through the management interface.

3.7.1 OCP NIC 3.0 Port Naming and Port Numbering

The numbering of all OCP NIC 3.0 external ports shall start from Port 1. When oriented with the primary side components facing up and viewing directly into the port, Port 1 shall be located on the left-hand side. The port numbers shall sequentially increase to the right. Refer to Figure 114 as an example implementation.

3.7.2 OCP NIC 3.0 Card LED Configuration

For low I/O count SFF/TSFF cards without built in light pipes (such as 1x QSFP, 2x QSFP, 2x SFP, or 2x RJ45), or LFF cards, where additional I/O bracket area is available, the card shall locally implement on-board link/activity indications. The card may additionally implement LEDs on the optional Scan Chain data stream.

For 4x SFP, a permissible LED implementation may include right angle SMT mount LEDs placed on the secondary side of the OCP NIC 3.0 card. The LEDs shall be located below the line side I/O cages.

A QSFP typically operates in a single port mode, but may be optionally configured to operate in dual or quad port modes. The LED definition extends to these modes to indicate the overall operating status of the cage.

Note: Depending on the end faceplate implementation (e.g., with an ejector latch), the secondary side LED implementation may be obstructed and biased to the left to prevent interference with the ejector cam mechanism.

The recommended local (on-card) LED implementation uses two physical LEDs (a bicolored Speed A/Speed B Link LED and a discrete Activity LED). ~~Table 41~~Table 40 describes the OCP NIC 3.0 card LED implementations.

The LEDs shall be uniformly illuminated across the indicator surface. LED surfaces with a diffusion treatment are preferred. For ease of indication within the operating environment, all OCP NIC 3.0 cards shall implement measures to prevent bleed-through between LED indicators and their surrounding chassis components.

Table 41: OCP NIC 3.0 Card LED Configuration with Two Physical LEDs per Port

| LED Pin | LED Color | Description |
|---------|-----------|---|
| Link | Green | <p>Active low. The LED is illuminated when the signal is low. Bicolor multifunction LED.</p> <p>This LED shall be used to indicate link.</p> <p>When the link is up, then this LED shall be lit and solid. This indicates that the link is established, there are no local or remote faults, and the link is ready for data packet transmission/reception.</p> <p>For all single port cage implementations (SFP, QSFP and BASE-T), the LED indication shall operate as follows:</p> <ul style="list-style-type: none"> • The LED is Green when the port is linked at its maximum speed. • The LED is Amber when the port is linked but not operating at the highest speed. • The LED is off when no link is present. <p>When a multi-lane cage is configured for dual port or quad port operation (e.g., QSFP breakout), the LED indication shall operate as follows:</p> <ul style="list-style-type: none"> • The LED is Green when all ports of the multi-lane cage are linked at its maximum speed. • The LED is Amber when one or more ports of the multi-lane cage are linked, but not operating at the highest speed, or one or more ports are down. • The LED is off when no link is present on all ports of the multi-lane cage. <p>For silicon with limited I/O, the Amber LED may be omitted. In this case, the Green LED shall simply indicate link is up at any configured speed.</p> <p>The illuminated Link LED indicator may be blinked and used for port identification through vendor specific link diagnostic software.</p> <p>The Link LED shall be located on the left-hand side or located on the top for each port when the OCP NIC 3.0 card is viewed in the horizontal plane.</p> <p>For serviceability, green LEDs shall emit light at a wavelength between 513 nm and 537 nm while amber LEDs shall emit light at a wavelength between 580 nm and 589 nm.</p> |
| | Amber | |
| | Off | |

| LED Pin | LED Color | Description |
|----------|--------------|--|
| | | <p>For uniformity across OCP NIC 3.0 products, all link LEDs should have their luminous intensity measured in millicandelas (mcd) with an average value between 12 mcd to 18 mcd.</p> <p>A recommended measurement methodology is a work-in-progress by the OCP NIC 3.0 electrical subgroup and will be added in a future release.</p> |
| Activity | Green Off | <p>Active low. The LED is illuminated when the signal is low.</p> <p>For all single port cage implementations (SFP, QSFP and BASE-T), the LED indication shall operate as follows:</p> <ul style="list-style-type: none"> • The LED is off when there is no activity. • <u>The LED should blink at the rate of ½ Hz to 5 Hz when there is activity.</u> • <u>The LED shall not blink when the link state is down.</u> <p>When a multi-lane cage is configured for dual port or quad port operation (e.g., QSFP breakout), the LED indication shall operate as follows:</p> <ul style="list-style-type: none"> • The LED is off when there is no activity on all ports of the multi-lane cage. • <u>The LED should blink at the rate of ½ Hz to 5 Hz when there is activity on one or more ports of the multi-lane cage.</u> • <u>The LED shall not blink when the link state is down for all ports of the multi-lane cage.</u> <p>The activity LED shall be located on the right-hand side or located on the bottom for each port when the OCP NIC 3.0 card is viewed in the horizontal plane.</p> <p>For serviceability, green LEDs shall emit light at a wavelength between 513 nm and 537 nm.</p> <p>For uniformity across OCP NIC 3.0 products, all activity LEDs should have their luminous intensity measured in millicandelas (mcd) with an average value between 12 mcd and 18 mcd.</p> <p>A recommended measurement methodology is a work-in-progress by the OCP NIC 3.0 electrical subgroup and will be added in a future release.</p> |

3.7.3 OCP NIC 3.0 Card LED Ordering

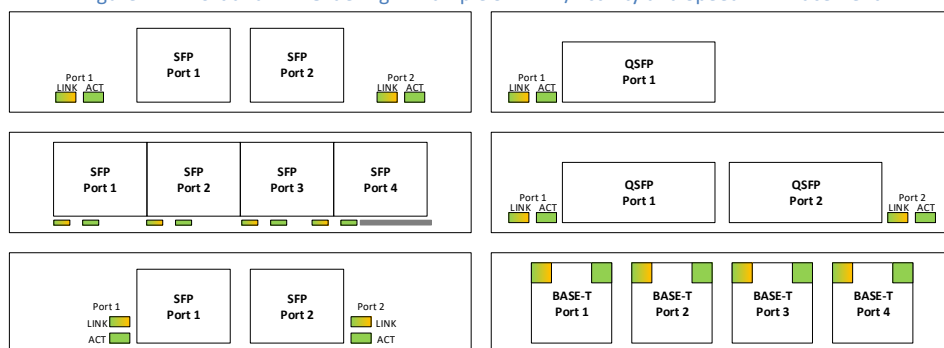
For all OCP NIC 3.0 card use cases, each port shall implement the green/amber Link LED and a green activity LED. For I/O limited silicon, the amber LED may be omitted.

When the OCP NIC 3.0 card is viewed from the horizontal position, and with the primary component side facing up, the Link LED shall be located on the left side and the activity LED shall be located on the right. The LED placement may also make use of a stacked LED assembly, or light pipe in the vertical axis. In this case, the Link Activity LED shall be on the top of the stack, and the Activity LED shall be on the bottom of the stack when viewed from the horizontal position. In all cases, the port ordering shall increase from left to right when viewed from the same horizontal position.

The actual placement of the Link and Activity LEDs on the faceplate may be left up to the discretion of the OCP NIC 3.0 card designer. The LED port association should be clearly labeled on the OCP NIC 3.0 card if the space allows. Similarly, the LED for link and the LED for Activity indication should also be marked on the faceplate. Vendors shall use the largest text permissible for increased readability.

For 4xSFP configurations, the LEDs may be placed on the secondary side of the card using right-angle SMT components. OCP NIC 3.0 designers may opt to use the scan chain LEDs instead or in addition to the on-card indicators.

Figure 114: Port and LED Ordering – Example SFF Link/Activity and Speed LED Placement



Note 1: The example port and LED ordering diagrams shown in Figure 114 are viewed with the card in the horizontal position and the primary side is facing up.

Note 2: The 4xSFP LED implementation is biased to the left to allow clearance for the ejector latch cam.

Note 3: For TSFF, there may be sufficient space to place LEDs above the port depending on the I/O configuration. Light pipes may be used in this configuration at the discretion of the OCP NIC 3.0 card designer.

3.7.4 Baseboard LEDs Configuration over the Scan Chain

A SFF OCP NIC 3.0 card with a fully populated I/O bracket (2x QSFP, 4x SFP or 4x RJ45) does not have sufficient space for primary-side discrete on-board (faceplate) LED indicators. Section 3.7.2 presents an implementation for placing LEDs on the secondary side.

In this scenario, the line side link and activity LED indicators are implemented on the baseboard system via the Scan Chain for remote indication. The Scan Chain bit stream is defined in Section 3.4.5.

The baseboard LED implementation uses two discrete LEDs – a green/amber Link LED and a discrete green Activity. The physical baseboard LED implementation is left up to the baseboard vendor and is not defined in this specification. The LED implementation is optional for baseboards.

For serviceability, green LEDs shall emit light at a wavelength between 513 nm and 537 nm while amber LEDs shall emit light at a wavelength between 580 nm and 589 nm.

At the time of this writing, the Scan Chain definition allows for up to two link and one activity LED per port. A total of up to 8 ports are supported in the Scan Chain. The bit stream defines the LEDs to be active low (on). The Scan Chain LED implementation allows the NIC LED indicators to be remotely located on the OCP NIC 3.0 compliant chassis (e.g., front LED indicators with rear I/O cards).

3.8 Power State Machine

There are four permissible power states for normal operation of the card: NIC Power Off, ID Mode, Aux Power Mode, and Main Power Mode. These four power states are mandatory for each OCP NIC 3.0 card. An optional fifth power state is Programming Mode and allows the FRU EEPROM to be updated in the field under the baseboard control. The normal transition order for these states is shown in Figure 115 and described in detail in the sections below. For simplicity, only the signal transitions resulting in a state change are shown. The available functions per power state are defined in [Table 42](#) [Table 41](#). The minimum transition time between power states is defined in Section 3.11.

Figure 115: Baseboard Power States

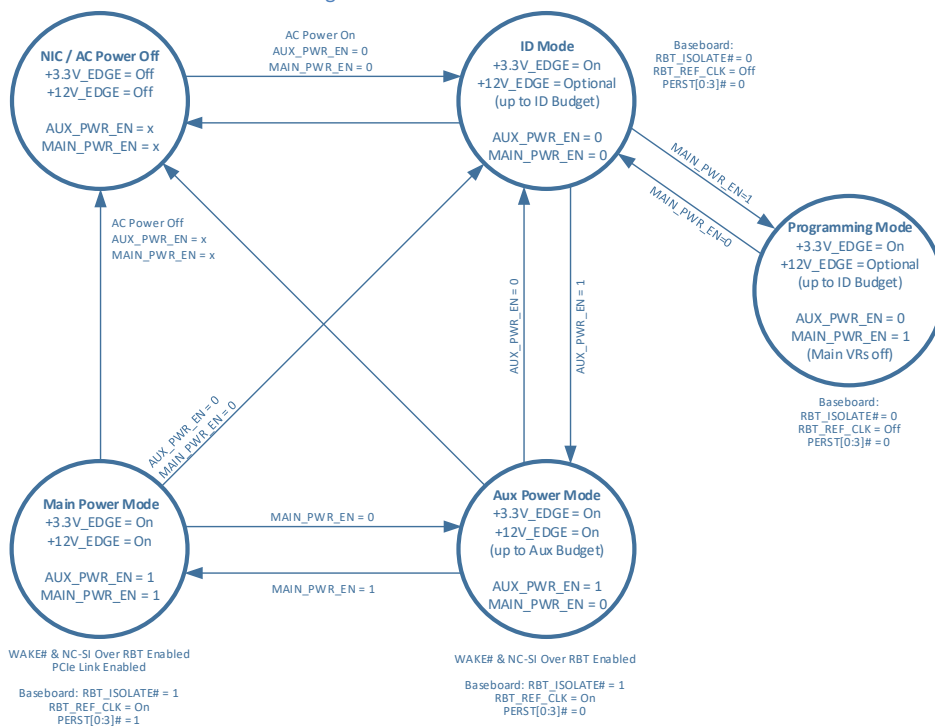


Table 42: Available Card Functions per Power State

| Power State | AUX_PWR_EN | MAIN_PWR_EN | PERSTn | FRU | Scan Chain | WAKEn | RBT Link | PCIe Link | +3.3V_EDGE | +12V_EDGE |
|------------------|------------|-------------|--------|-----------------------|-----------------------|----------|----------|-----------|------------|-----------------------|
| NIC Power Off | Low | Low | Low | | | | | | | |
| ID Mode | Low | Low | Low | <u>M</u> * | <u>M</u> ¹ | | | | <u>M</u> | <u>O</u> ² |
| Programming Mode | Low | High | Low | <u>M</u> ⁴ | | | | | <u>M</u> | <u>O</u> ² |
| Aux Power Mode | High | Low | Low | <u>M</u> | <u>M</u> | <u>M</u> | <u>M</u> | | <u>M</u> | <u>M</u> ³ |
| Main Power Mode | High | High | High | <u>M</u> | <u>M</u> | <u>M</u> | <u>M</u> | <u>M</u> | <u>M</u> | <u>M</u> |

M = Mandatory. Function is required in the designated power state.
O = Optional. Function is optionally supported in the designated power state.

Note 1: Only the PRSNTB[3:0]# scan chain signals are valid in ID mode as the OCP NIC 3.0 card power rails have not yet been enabled via the AUX_PWR_EN/MAIN_PWR_EN signals.

Note 2: The +12V_EDGE rail ~~may be optionally disabled by the baseboard at this time~~ during this power state, but the max permissible leakage is up to the ID Mode / Programming Mode current limit defined in Section 3.9. The NIC shall not rely on +12V_EDGE power in this state and shall not malfunction if +12V_EDGE is present or absent.

Note 3: The +12V_EDGE rail is on, but the max permissible current draw is up to the Aux Power Mode current limit defined in Section 3.9.

Note 4: The FRU EEPROM WP pin is low (not write protected) to enable programming using any of the defined methods for controlling the EEPROM WP signal. Refer to the FRU Write Protection Mechanism field in Section 4.10.3.

3.8.1 NIC Power Off

In NIC Power Off mode, all power delivery has been turned off or the card is not physically plugged into the baseboard. Transition to this state can be from any other state.

3.8.2 ID Mode

In the ID Mode, only +3.3V_EDGE is available for powering up the FRU EEPROM and the Scan Chain devices. All OCP NIC 3.0 cards must enter the ID Mode state for FRU EEPROM and scan chain queries immediately following the NIC Power Off state. An OCP NIC 3.0 card shall transition to this mode when AUX_PWR_EN=0 and MAIN_PWR_EN=0.

The baseboard queries the EEPROM and determines the OCP NIC 3.0 device capabilities. The FRU EEPROM content requirements are defined in Section 4.10.3. Only the card PRSNTB[3:0]# bits are valid on the scan chain in this mode as the OCP NIC 3.0 card power rails have not yet been enabled via the AUX_PWR_EN and MAIN_PWR_EN signals. The WAKE#, TEMP_WARN#, TEMP_CRIT#, Link and Activity bits are invalid and should be masked by the baseboard in ID Mode.

Baseboards may disable +12V_EDGE in this power state. OCP NIC 3.0 cards are not intended to use +12V_EDGE in ID Mode, however leakage current may be present. If +12V_EDGE is not provided by the baseboard and leakage is present, the max voltage leakage from the OCP NIC 3.0 card to the baseboard

shall be limited to 300 mV when a 1 k Ω bleed resistor is present on the baseboard. The baseboard bleed resistor is optional if the baseboard can tolerate leakage. If +12V_EDGE is present in ID Mode, the max current is defined in Section 3.9.

3.8.3 Aux Power Mode

The Aux Power Mode provides both +3.3V_EDGE as well as +12V_EDGE is available. +12V_EDGE in Aux mode may be used to deliver power to the OCP NIC 3.0 card, but only up to the Aux mode budget as defined in ~~Table 43~~Table 42. An OCP NIC 3.0 card shall transition to this mode when AUX_PWR_EN=1, MAIN_PWR_EN=0, NIC_PWR_GOOD=1 and the duration (T_{APL}) has passed for the ID-Aux Power Mode ramp. This guarantees the ID mode to Aux Power Mode transition (as shown in Figure 116) has completed and all Aux Power Mode rails are within operating tolerances. The WAKE#, TEMP_WARN#, and TEMP_CRIT# bits shall not be sampled until these conditions are met.

For OCP NIC 3.0, Aux Power Mode corresponds to ACPI power state S5 on the system. This could also correspond to ACPI power state S3 or S4 depending on the implementation.

3.8.4 Main Power Mode

The Main Power Mode provides both +3.3V_EDGE and +12V_EDGE across the OCP connector. The OCP NIC 3.0 card operates in full capacity. Up to 80 W may be delivered on +12V_EDGE for a SFF/TSFF Card and up to 150 W for a LFF Card. Additionally, up to 3.63 W is delivered on each +3.3V_EDGE pin. An OCP NIC 3.0 card shall transition to this mode when AUX_PWR_EN=1, MAIN_PWR_EN=1, NIC_PWR_GOOD=1 and the duration (T_{MPL}) has passed for the Aux-Main Power Mode ramp. This guarantees the Aux Power Mode to Main Power Mode transition (as shown in Figure 116) has completed and all Main Power Mode rails are within operating tolerances. The WAKE#, TEMP_WARN#, and TEMP_CRIT# bits shall not be sampled until these conditions are met.

For OCP NIC 3.0, Main Power Mode corresponds to ACPI power state S0 on the system. This could also correspond to ACPI power state S1 depending on the implementation.

3.8.5 Programming Mode

The Programming Mode provides +3.3V_EDGE for powering up the FRU EEPROM. This is an optional state that disables the FRU EEPROM write protection mechanism via combinatorial logic and allows the baseboard to reprogram the FRU EEPROM. This state shall only be entered from ID mode if the FRU EEPROM advertises support for this power state as defined in Section 4.10.3.

Baseboards may disable +12V_EDGE in this power state. OCP NIC 3.0 cards are not intended to use +12V_EDGE in Programming Mode, however leakage current may be present. If +12V_EDGE is not provided by the baseboard and leakage is present, the max voltage leakage from the OCP NIC 3.0 card to the baseboard shall be limited to 300 mV when a 1 k Ω bleed resistor is present on the baseboard. The baseboard bleed resistor is optional if the baseboard can tolerate leakage. If +12V_EDGE is present in Programming Mode, the max current is defined in Section 3.9.

Additionally, the Aux Power Mode and Main Power Mode SVRs need to remain disabled and NIC_PWR_GOOD shall remain low while the card is in this state. An example discrete logic circuit to accomplish this gating is shown in Figure 99. NIC vendors may implement their own gating circuitry if the same result is achieved.

Devices which use GPIO, NC-SI or PLDM for FRU EEPROM WP control may allow programming of the FRU EEPROM when in operating in the Aux Power or Main Power Modes. Usage of the GPIO signal, NC-SI or PLDM to control the WP mechanism are implementation specific and is outside the scope of this specification.

3.9 Power Supply Rail Requirements and Slot Power Envelopes

The baseboard provides +3.3V_EDGE and +12V_EDGE to both the Primary and Secondary Connectors. The rail requirements are leveraged from the PCIe CEM 4.0 specification. For OCP NIC 3.0 implementations, there are six total power envelopes. Five are defined for SFF/TSFF, and one is defined for LFF. The max current draw is defined in ~~Table 43~~Table 42 for each state and power envelope and is inclusive of the line side transceivers installed on the card. The slot power values are the max supportable power delivered to the card for each slot type. This is independent of the +3.3V_EDGE and +12V_EDGE rails deviating from their nominal values.

Table 43: Baseboard Power Supply Rail Requirements – Slot Power Envelopes

| Power Rail | 15 W Slot SFF/TSFF | 25 W Slot SFF/TSFF | 35 W Slot SFF/TSFF | 50 W Slot SFF/TSFF | 80 W Slot SFF/TSFF | 150 W LFF |
|-------------------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|---------------|
| +3.3V_EDGE | | | | | | |
| Voltage Tolerance | ±9% (max) | ±9% (max) | ±9% (max) | ±9% (max) | ±9% (max) | ±9% (max) |
| Supply Current | | | | | | |
| ID Mode | 100 mA (max) | 100 mA (max) | 100 mA (max) | 100 mA (max) | 100 mA (max) | 100 mA (max) |
| Programming Mode | 100 mA (max) | 100 mA (max) | 100 mA (max) | 100 mA (max) | 100 mA (max) | 100 mA (max) |
| Aux Power Mode | 1.1 A (max) | 1.1 A (max) | 1.1 A (max) | 1.1 A (max) | 1.1 A (max) | 2.2 A (max) |
| Main Power Mode | 1.1 A (max) | 1.1 A (max) | 1.1 A (max) | 1.1 A (max) | 1.1 A (max) | 2.2 A (max) |
| Capacitive Load | 150 µF (max) | 150 µF (max) | 150 µF (max) | 150 µF (max) | 150 µF (max) | 300 µF (max) |
| +12V_EDGE | | | | | | |
| Voltage Tolerance | +8/-12% (max) | +8/-12% (max) | +8/-12% (max) | +8/-12% (max) | +8/-12% (max) | +8/-12% (max) |
| Supply Current | | | | | | |
| ID Mode ⁵ | 50 mA (max) | 50 mA (max) | 50 mA (max) | 50 mA (max) | 50 mA (max) | 50 mA (max) |
| Programming Mode ⁵ | 50 mA (max) | 50 mA (max) | 50 mA (max) | 50 mA (max) | 50 mA (max) | 50 mA (max) |
| Aux Power Mode | 0.7 A (max) | 1.1 A (max) | 1.5 A (max) | 2.1 A (max) | 3.3 A (max) | 6.3 A (max) |
| Main Power Mode | 1.25 A (max) | 2.1 A (max) | 2.9 A (max) | 4.1 A (max) | 6.6 A (max) | 12.5 A (max) |
| Capacitive Load ³ | 500 µF (max) | 500 µF (max) | 500 µF (max) | 1200 µF (max) | 2000 µF (max) | 2000 µF (max) |

Note 1: While cards may draw up to the published power ratings, the baseboard vendor shall evaluate its cooling capacity for each slot power envelope to determine if a transition to Aux Power Mode is allowed.

Note 2: The maximum slew rate for each OCP NIC 3.0 card shall be no more than 0.1 A/µs per the PCIe CEM specification.

Note 3: Each OCP NIC 3.0 card shall limit the bulk capacitance to the max published values.

Note 4: For systems that implement hot plug, the baseboard shall limit the voltage slew rate such that the instantaneous inrush current shall not exceed the specified max current. The equation is defined in the PCIe CEM specification and is $dV/dt = I/C$; where:

$$I = \text{max allowed current (A)}$$

$$C = \text{max allowed bulk capacitance (F)}$$

$$dV/dt = \text{maximum allowed voltage slew rate (V/s)}$$

Note 5: +12V_EDGE may optionally be disabled during ID Mode and Programming mode. Refer to Section 3.8 for details.

The OCP NIC 3.0 FRU definition provides a record for the max power consumption of the card. This value shall be used to aid in determining if the card may be enabled for a given OCP slot. Refer to Section 4.10.3 for the available FRU records.

Additionally, the baseboard shall advertise its slot power limits to aid in the overall board power budget allocation to prevent a high-power card from being enabled in a lower power class slot. This is implemented via the Slot Power Limit Control mechanism as defined in the PCIe Base Specification. The end point silicon will power up in a low power state until power is negotiated.

3.10 Hot Swap Considerations for +12V_EDGE and +3.3V_EDGE Rails

Hot plug and hot swap support is optional for baseboard implementers. However, the OCP NIC 3.0 form factor lends itself to potential hot plug and removal events while the baseboard is powered on. These events need to be carefully orchestrated with the operating system and system management entity to prevent a system hang. A surprise extraction may occur in some instances when resources have not been quiesced and the card is removed. Many aspects of the system are involved in processing such an event in both cases. The current scope of this specification does not define an overall hardware or software system architecture to support hot plug. Instead, this specification only highlights the hardware elements that can be utilized to support hot plug for implementations.

The system implementer shall consider the use of hot swap controllers on both the +12V_EDGE and +3.3V_EDGE pins to prevent damage to the baseboard or the OCP NIC 3.0 card. Hot swap controllers limit the in-rush current while also providing overcurrent, undervoltage and overvoltage protection capabilities.

The hot swap controller may gate the +12V_EDGE and +3.3V_EDGE based on the PRSNTB[3:0]# value. Per Section 3.5.3, a card is present in the system when the encoded value is not 0b1111. The PRSNTB[3:0]# may be AND'ed together and connected to the hot swap controller to accomplish this result. Per the OCP NIC 3.0 mechanical definition (Section 3.1.1), the present pins are short pins and engage only when the card is positively seated.

The PRSNTB[3:0]# pins are used to detect an OCP 3.0 NIC card insertion and removal event. The card type detection is described in Section 3.5. Using in-band signaling, the PCIe link may be enabled to periodically train when a card is plugged in. Similarly, the signals may be used to detect a card removal. The card type is determined by querying the FRU data over the SMBus.

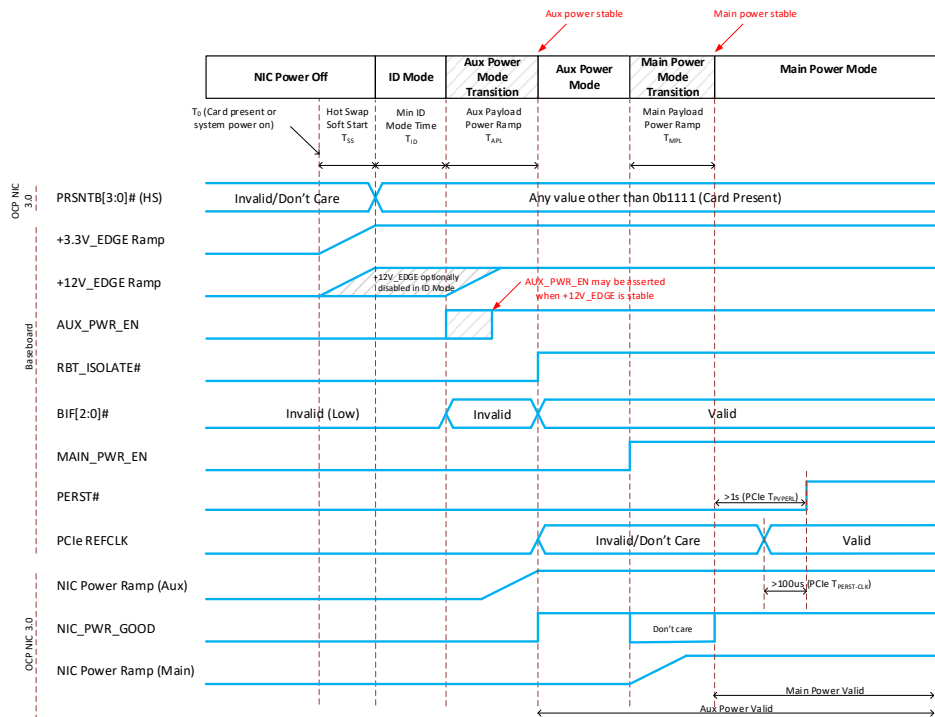
At the time of this writing, the DSP0222 Network Controller Sideband Interface (NC-SI) Specification 1.1 and 1.2 does not define a mechanism to discover hot-plug support. Future work is needed for supporting this feature on NCSI over RBT interfaces.

Baseboards that do not support hot insertion, or hot extractions may opt to not implement these features.

3.11 Power Sequence Timing Requirements

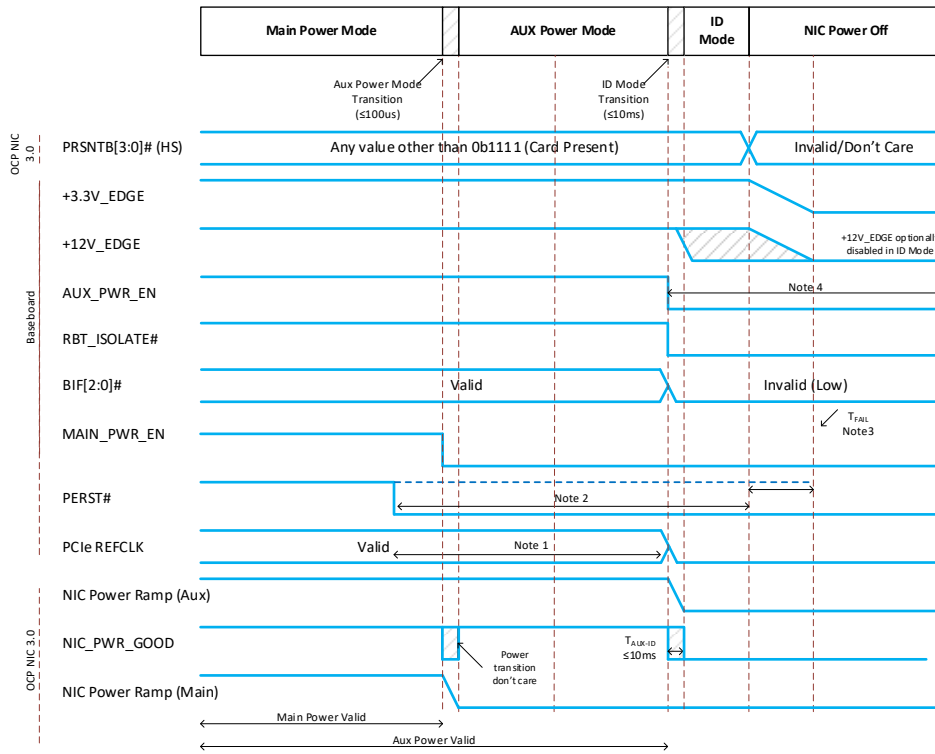
The following figure shows the power sequence of PRSNTB[3:0]#, +3.3V_EDGE, +12V_EDGE relative to AUX_PWR_EN, RBT_ISOLATE#, BIF[2:0]#, MAIN_PWR_EN, PERSTn*, and PCIe REFCLK stable on the baseboard. Additionally, the OCP NIC 3.0 card power ramp, and NIC_PWR_GOOD are shown. Please refer to Section 3.4.6 for the NIC_PWR_GOOD definition. Refer to DMTF DSP0222 for details on the NC-SI controller and clock startup requirements.

Figure 116: Power-Up Sequencing – Normal Operation



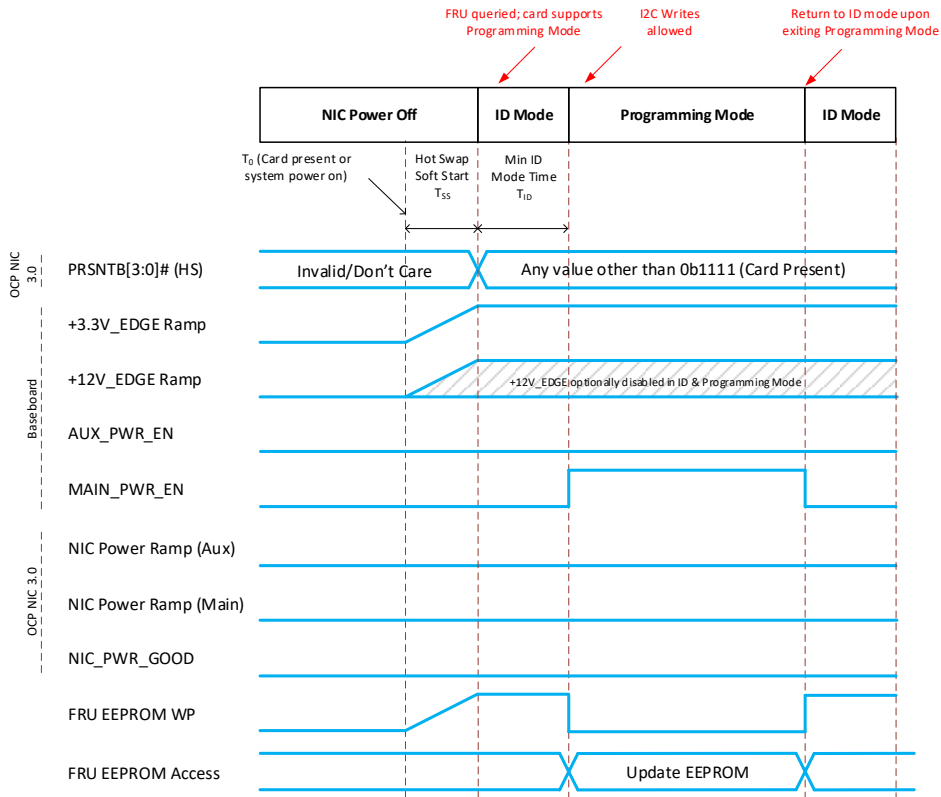
Note 1: The RBT isolation state is controlled with the baseboard RBT_ISOLATE# signal. This controls the baseboard RBT isolator.
Note 2: For NC-SI over RBT, the rising edge of NIC_PWR_GOOD shall be treated as V_{REF} is available for NC-SI communication. Refer to timing parameter T4 in the DMTF DSP0222 specification for details.

Figure 117: Power-Down Sequencing – Normal Operation



- Note 1: REFCLK go inactive after PERST# goes active. (PCIe CEM Section 2.2.3)
- Note 2: PERST# goes active before the power on the connector is removed. (PCIe CEM Section 2.2.3)
- Note 3: In the case of a surprise power down, PERST# goes active T_{FAIL} after power is no longer stable.
- Note 4: The baseboard shall have a minimum delay of T_{CYCLE_SFF} and T_{CYCLE_LFF} for the respective form-factors between AUX_PWR_EN deassertion (power off) and subsequent AUX_PWR_EN assertion (power on) to prevent powering up into a pre-biased condition.

Figure 118: Programming Mode Sequencing



Note 1: All other signals are electrically low and are not shown.

Table 44: Power Sequencing Parameters

| Parameter | Value | Units | Description |
|-----------------------|-------|-------|---|
| T _{SS} | 20 | ms | Maximum time between system +3.3V_EDGE and +12V_EDGE ramp to power stable. This parameter is only applicable to hot swap controller-based implementations. For non-hot swap applications, the +3.3V_EDGE and +12V_EDGE ramp is system dependent. |
| T _{SCAN_RDY} | 1 | ms | Minimum time required between +3.3V_EDGE stable to the first scan chain data valid read. |
| T _{ID} | 20 | ms | Minimum time per spec to spend in ID mode. |

| Parameter | Value | Units | Description |
|------------------------|-------|-------|---|
| T _{APL} | 50 | ms | Maximum time between AUX_PWR_EN assertion and NIC_PWR_GOOD assertion. |
| T _{MPL} | 50 | ms | Maximum time between MAIN_PWR_EN assertion and NIC_PWR_GOOD assertion. |
| T _{PVPERL} | 1 | s | Minimum time between NIC_PWR_GOOD assertion in Main Power Mode and PERST# deassertion. For OCP NIC 3.0 applications, this value is >1 second. This is longer than the minimum value specified in the PCIe CEM Specification, Rev 4.0. |
| T4 | 2 | s | Maximum time interval from when the network controller NC-SI over RBT interface is able to respond to commands. The parameter T4 is defined in the DSP0222 specification and is measured from when V _{REF} becomes available. For OCP NIC 3.0, the value T4 is measured from the deassertion of RBT_ISOLATE#. |
| T _{PERST-CLK} | 100 | μs | Minimum Time PCIe REFCLK is stable before PERST# inactive. |
| T _{FAIL} | 500 | ns | In the case of a surprise power down, PERST# goes active at minimum T _{FAIL} after power is no longer stable. |
| T _{AUX-ID} | 10 | ms | Maximum time from AUX_PWR_EN deassertion to NIC_PWR_GOOD deassertion. |
| T _{CYCLE_SFF} | 30 | ms | Minimum time between AUX_PWR_EN deassertion to AUX_PWR_EN reassertion for SFF/TSFF cards. Delay time allows for OCP NIC 3.0 card capacitors to discharge and prevent reapplying power into a pre-biased condition. |
| T _{CYCLE_LFF} | 60 | ms | Minimum time between AUX_PWR_EN deassertion to AUX_PWR_EN reassertion for LFF cards. Delay time allows for OCP NIC 3.0 card capacitors to discharge and prevent reapplying power into a pre-biased condition. |

3.12 Digital I/O Specifications

This section is for informative reference only. All digital I/O pins on the connector boundary are +3.3 V signaling levels. ~~Table 44~~The following tables provide the absolute max levels. Refer to the appropriate specifications for the RBT, PCIe and SMBus DC/AC specifications for any superseded values.

Table 45: Digital I/O DC specifications

| Symbol | Parameter | Min | Max | Units | Note(s) |
|------------------|---------------------|-----|-----|-------|---------|
| V _{OH} | Output voltage | | 3.6 | V | |
| V _{OL} | Output low voltage | | 0.8 | V | |
| I _{OH} | Output high current | | | mA | |
| I _{OL} | Output low current | | | mA | |
| V _{IH1} | Input voltage | 2.0 | 3.6 | V | 1, 3, 4 |
| V _{IL1} | Input low voltage | - | 0.8 | V | 1, 3, 4 |
| V _{IH2} | Input voltage | 2.1 | 3.6 | V | 2 |
| V _{IL2} | Input low voltage | - | 0.8 | V | 2 |
| V _{IH2} | Input voltage | 2.1 | 3.6 | V | 5 |
| V _{IL2} | Input low voltage | - | 1.0 | V | 5 |
| I _{OH} | Input current | | | mA | |

Table 46: Digital I/O AC specifications

| Symbol | Parameter | Min | Max | Units | Note(s) |
|-----------------|------------------|-----|-----|-------|---------|
| T _{OR} | Output rise time | | | ns | |
| T _{OF} | Output fall time | | | ns | |

Note 1: Applies to PCIe CEM signals PERST[5:0]#, WAKE#, PWRBRK[1:0]#.

Note 2: Applies to SMBus signals SMCLK, SMDAT and SMRST#.

Note 3: Applies to RBT signals defined by DSP0222.

Note 4: Applies to OCP NIC 3.0 card edge signals (AUX_PWR_EN, MAIN_PWR_EN, SLOT_ID[1:0], NIC_PWR_GOOD, BIF[2:0]#, PRSNTB[3:0]#).

Note 5: Applies to scan chain shift register signals (SCAN_LD#, SCAN_DATA_IN, SCAN_DATA_OUT, SCAN_CLK).

4 Management and Pre-OS Requirements

OCP NIC 3.0 card management is an important aspect to overall system management. This section specifies a common set of management requirements for OCP NIC 3.0 implementations. There are three types of implementations (RBT+MCTP Type, RBT Type, and MCTP Type) depending on the physical sideband management interfaces, transports, and traffic supported over different transports. An OCP NIC 3.0 implementation shall support at least one type of implementation for card management. For a given type of implementation, an OCP NIC 3.0 card shall support type specific requirements described in Sections 4.1 through 4.7.

Table 47: OCP NIC 3.0 Management Implementation Definitions

| Management Type | Definition |
|-----------------|---|
| RBT Type | The RBT Type management interface is exclusive to the Reduced Media Independent Interface (RMII) Based Transport (RBT). The NIC card is required to support the DSP0222 Network Controller Sideband Interface (NC-SI) Specification for this management |
| RBT+MCTP Type | The RBT+MCTP management interface supports both the RBT and MCTP standards, specifically the DSP0222 Network Controller Sideband Interface (NC-SI) Specification, DSP0236 Management Component Transport Protocol (MCTP) Base Specification, and the associated binding specifications. This is the preferred management implementation for baseboard NIC cards. See MCTP Type below for more details |
| MCTP Type | The MCTP management interface supports MCTP standards specifically the DSP0236 Management Component Transport Protocol (MCTP) Base Specification and the associated binding specifications. |

4.1 Sideband Management Interface and Transport

OCP NIC 3.0 sideband management interfaces are used by a Management Controller (MC) or Baseboard Management Controller (BMC) to communicate with the OCP NIC 3.0 card. ~~Table 48~~Table 47 summarizes the sideband management interface and transport requirements.

Table 48: Sideband Management Interface and Transport Requirements

| Requirement | RBT+MCTP Type | RBT Type | MCTP Type |
|--|---------------|----------|-----------|
| NC-SI compliant RMII Based Transport (RBT) including physical interface defined in Section 10 of DMTF DSP0222 | Required | Required | N/A |
| I ² C compliant physical interface for FRU EEPROM | Required | Required | Required |
| SMBus 2.0 compliant physical interface | Required | N/A | Required |
| Management Component Transport Protocol (MCTP) Base (DSP0236 compliant) over MCTP/SMBus Binding (DSP0237 compliant) | Required | N/A | Required |
| PCIe VDM compliant physical interface | Optional | N/A | Optional |
| Management Component Transport Protocol (MCTP) Base (DSP0236 compliant) over MCTP/PCIe VDM Binding (DSP0238 compliant) | Optional | N/A | Optional |

4.2 NC-SI Traffic

DMTF DSP0222 defines two types of NC-SI traffic: Pass-Through and Control. ~~Table 49~~Table 48 summarizes the NC-SI traffic requirements.

Table 49: NC-SI Traffic Requirements

| Requirement | RBT+MCTP Type | RBT Type | MCTP Type |
|---|---------------|----------|-----------|
| NC-SI Control over RBT (DMTF DSP0222 compliant) | Required | Required | N/A |
| NC-SI Control over MCTP (DMTF DSP0261 compliant) | Required | N/A | Required |
| NC-SI Pass-Through over RBT (DMTF DSP0222 compliant) | Required | Required | N/A |
| NC-SI Pass-Through over MCTP (DMTF DSP0261 compliant) | Optional | N/A | Optional |

Note: A Management Controller (MC) is allowed to use NC-SI Control traffic only without enabling NC-SI pass-through.

4.3 Management Controller (MC) MAC Address Provisioning

An OCP NIC 3.0 compliant card that supports NC-SI pass-through shall provision one or more MAC addresses per Package (refer to the Package definition as detailed in the DMTF DSP0222 specification) for Out-Of-Band (OOB) management traffic. The number of MC MAC addresses provisioned is implementation dependent. These MAC addresses are not exposed to the host(s) as available MAC addresses. The MC is not required to use these provisioned MAC addresses. ~~Table 50~~Table 49 summarizes the MC MAC address provisioning requirements. A MAC address algorithm calculator is provided on the OCP NIC 3.0 wiki page and may be downloaded from: <http://www.opencompute.org/wiki/Server/Mezz>

Table 50: MC MAC Address Provisioning Requirements

| Requirement | RBT+MCTP Type | RBT Type | MCTP Type |
|---|---------------|----------|-----------|
| <p>One or more MAC Addresses per package shall be provisioned for the MC.</p> <p>The OCP NIC 3.0 platform may choose to use the NIC vendor allocated MAC addresses for the BMC.</p> <p>The usage of provisioned MAC addresses are BMC implementation specific and is outside the scope of this specification.</p> <p>The recommended MAC address allocation scheme is stated below. This algorithm assumes all of the port MAC addresses are sequentially allocated first, followed by the BMC MAC addresses. For multi-host capable cards, the MAC addresses shall be provisioned for the maximum number of supported hosts.</p> <p>Assumptions:</p> | Required | Required | Optional |

| Requirement | RBT+MCTP Type | RBT Type | MCTP Type |
|---|---------------|----------|-----------|
| <p>1. The number of BMCs or virtual BMCs is the same as the number of hosts (1:1 relationship between each host and the BMC).</p> <p>2. The maximum number of partitions on each port is the same.</p> <p>Variables:</p> <ul style="list-style-type: none"> • <code>num_ports</code> – Number of Ports on the OCP NIC 3.0 card • <code>max_parts</code> – Maximum number of partitions on a port per host • <code>num_hosts</code> – Number of hosts supported by the NIC • <code>first_addr</code> – The MAC address of the first host for the first partition on the first port • <code>host_addr[i]</code> – base MAC address of i^{th} host ($0 \leq i \leq \text{num_hosts}-1$) • <code>bmc_addr[i]</code> – base MAC address of i^{th} BMC ($0 \leq i \leq \text{num_hosts}-1$) <p>Formula:</p> <ul style="list-style-type: none"> • $\text{host_addr}[i] = \text{first_addr} + i * \text{num_ports} * \text{max_parts}$ • The assignment of MAC address used by i^{th} host on port j for the partition k is out of the scope of this specification. • $\text{bmc_addr}[i] = \text{first_addr} + \text{num_ports} * \text{max_parts} * \text{num_hosts} + i * \text{num_ports}$ • The MAC address used by i^{th} BMC on port j, where $0 \leq i \leq \text{num_hosts}-1$ and $0 \leq j \leq \text{num_ports} - 1$ is $\text{bmc_addr}[i] + j$ | | | |
| <p>For multi-host capable OCP NIC 3.0 cards, the MAC addresses shall be provisioned for the maximum number of supported hosts.</p> <p>This algorithm assumes each host and port MAC address combination shall have a corresponding BMC MAC address allocated in sequential order.</p> <p>Variables:</p> | Required | Required | Required |

| Requirement | RBT+MCTP Type | RBT Type | MCTP Type |
|--|---------------|----------|-----------|
| <ul style="list-style-type: none"> num_ports – Number of Ports on the OCP NIC 3.0 card max_parts – Maximum number of partitions on a port per host num_hosts – Number of hosts supported by the NIC first_addr – The MAC address of the first host for the first partition on the first port host_addr[i][j] – base MAC address of ith host for the jth port bmc_addr[i][j] – base MAC address of ith BMC for the jth port i is the host number ($0 \leq i \leq \text{num_hosts}-1$) j is the port number ($0 \leq j \leq \text{num_ports}-1$) k is the partition number ($0 \leq k \leq \text{max_parts}-1$) <p>Formula:</p> <ul style="list-style-type: none"> host_addr[i][j] = first_addr + i*(max_parts+1)*num_ports + j bmc_addr[i][j] = first_addr + i*(max_parts+1)*num_ports + max_parts*num_ports + j The assignment of MAC address used by ith host on port j for the partition k is out of the scope of this specification. | | | |
| <p>Support at least one of the following mechanisms for provisioned MC MAC Address retrieval:</p> <ul style="list-style-type: none"> NC-SI Control/RBT (DMTF DSP0222 compliant) NC-SI Control/MCTP (DMTF DSP0261 compliant) <p>Note: This capability is planned to be included in revision 1.2 of the DSP0222 NC-SI specification.</p> <p>For DMTF DSP0222 1.1 compliant OCP NIC 3.0 implementations, MC MAC address retrieval shall be supported using NC-SI OEM commands. An OCP NIC 3.0 implementation, that is compliant with DMTF DSP0222 that defines standard NC-SI commands for MC MAC address retrieval, shall support those NC-SI commands.</p> | Required | Required | Optional |

4.4 ASIC Die Temperature Reporting

An OCP NIC 3.0 implementation can have several silicon components including one or more ASICs implementing NIC functions. For the system management, it is important that the die temperatures of these ASIC components can be retrieved over sideband interfaces. The ASIC die temperature reporting requirements of this section are independent of the transceiver module temperature reporting discussed in Section 4.6.

The temperature reporting interface shall be accessible in Aux Power Mode, and Main Power Mode. ~~Table 52~~ ~~Table 54~~ summarizes temperature reporting requirements. These requirements improve the system thermal management and allow the baseboard management device to access key component temperatures on an OCP NIC 3.0 card. When the temperature reporting function is implemented, it is required that the temperature reporting accuracy is within ± 3 °C.

As an example, the assumed hysteresis value for any threshold deassertion is 2 °C. For the three upper severity levels (Warning, Critical and Fatal), the thresholds shall be no less than the reporting accuracy of the temperature sensor (± 3 °C) plus the hysteresis value. Therefore, the minimum temperature delta between thresholds should be 5 °C. Larger temperature deltas between severity levels are permitted.

- The Fatal threshold should be set to the temperature at which the silicon may experience permanent failures.
- The Critical threshold should be set to the temperature at which degraded performance or transient errors may occur for the silicon. The life span of the product may be impacted. At minimum, the Critical threshold shall be at least 5 °C below Fatal.
- The Warning threshold should be set to at least 5 °C below Critical and set accordingly to the NIC vendor to give an early indication that the server needs to take remedial action to increase cooling capacity.

To illustrate this concept, the following example shows a silicon device with an operating T_j of 105 °C per the device datasheet and card temperature reporting accuracy of ± 3 °C. The Upper Fatal threshold is fix to the upper device temperature before immediate physical damage is incurred. This threshold values can be adjusted when the card temperature sensor reporting accuracy is better than ± 3 °C.

Table 51: Threshold Severity Level vs Example Threshold Values

| Threshold Severity Level | Example Threshold Value (°C) |
|--------------------------|------------------------------|
| Upper Fatal | 115 |
| Upper Critical | 105 |
| Upper Warning | 100 |

For the severity levels above, each baseboard shall ensure the card fatal thermal limit is not exceeded. In ID Mode, baseboard shall determine if the card present in the OCP NIC 3.0 slot is thermally supportable for the thermal tier as defined in the FRU contents.

Table 52: Temperature Reporting Requirements

| Requirement | RBT+MCTP Type | RBT Type | MCTP Type |
|--|---------------|-------------|-------------|
| ASIC die temperature reporting for a component with TDP ≥ 5 W | Required | Required | Required |
| ASIC die temperature reporting for a component with TDP < 5 W | Recommended | Recommended | Recommended |
| When the temperature sensor reporting function is implemented, the OCP NIC 3.0 card shall support PLDM for Platform Monitoring and Control (DSP0248 compliant) for temperature reporting. Additionally, refer to DSP2054 for the PLDM NIC Modeling scheme. | Required | Required | Required |
| When the temperature sensor reporting function is implemented, the OCP NIC 3.0 card shall report upper warning, upper critical, and upper fatal thresholds for PLDM numeric sensors. Note: Refer to DSP0248 for definitions of the upper warning, upper critical, and upper fatal thresholds. Additionally, refer to DSP2054 for the PLDM NIC Modeling scheme. | Required | Required | Required |
| When the temperature reporting function is implemented using PLDM numeric sensors, the temperature tolerance shall be reported as part of the sensor Platform Descriptor Record (PDR) format. | Required | Required | Required |
| Support for self-shutdown. The purpose of the self-shutdown feature is to “self-protect” the NIC ASIC from permanent damage due to high operating temperatures. The NIC may accomplish this by reducing the power consumed by the ASIC. A BMC may continuously monitor the NIC ASIC temperature and shutdown the NIC ASIC as soon as the temperature reaches a threshold value. There may be scenarios and implementations where the OCP NIC ASIC may be required to self-shutdown without depending on an external entity like the BMC. For those scenarios and implementations, the self-shutdown feature is a final effort in preventing permanent damage to the NIC ASIC at the expense of potential data loss. If the self-shutdown feature is implemented, the NIC ASIC shall monitor its temperature and shutdown itself as soon as the self-shutdown threshold value is reached. The value of the self-shutdown threshold is implementation specific. It is recommended that the self-shutdown threshold value is | Optional | Optional | Optional |

| Requirement | RBT+MCTP Type | RBT Type | MCTP Type |
|---|---------------|----------|-----------|
| <p>higher than the maximum junction temperature of the ASIC implementing the NIC function. It is also recommended that the self-shutdown threshold value is between the critical and fatal temperature thresholds of the ASIC.</p> <p>If the self-shutdown feature is implemented, care shall be taken to ensure that the board power down state is latched and the board does not autonomously resume normal operation.</p> <p>The OCP NIC 3.0 card does not need to know the reason for the NIC ASIC self-shutdown threshold crossing (e.g., fan failure). After the NIC ASIC enters the self-shutdown state, the OCP NIC 3.0 card may not be operational. This might cause the system with the OCP NIC 3.0 card to become unreachable via the NIC.</p> <p>In order to recover the NIC ASIC from the self-shutdown state, the OCP NIC 3.0 card shall go through the NIC ID Mode state as described in Section 3.8.1.</p> <p>If the self-shutdown feature is implemented, the implementation shall provide a mechanism to enable/disable the feature.</p> <p>Note: It is assumed that a system management function will prevent a component from reaching its fatal threshold temperature.</p> | | | |

4.5 Power Consumption Reporting

An OCP NIC 3.0 implementation may be able to report the power consumed at the board level. It is important for the system management that the information about the power consumption can be retrieved over sideband interfaces. ~~Table 53~~Table-52 summarizes the power consumption reporting requirements.

Table 53: Power Consumption Reporting Requirements

| Requirement | RBT+MCTP Type | RBT Type | MCTP Type |
|--|---------------|----------|-----------|
| Board Only Estimated Power Consumption Reporting. The value of this field is encoded into the FRU EEPROM contents. This field reports the board max power consumption value without transceivers plugged into the line side receptacles. | Required | Required | Required |
| Pluggable Transceiver Module Power Reporting. The pluggable transceivers plugged into the line side receptacles | Required | Required | Required |

| Requirement | RBT+MCTP Type | RBT Type | MCTP Type |
|---|---------------|----------|-----------|
| shall be inventoried (via an EEPROM query) and the Power Class of the module shall be reported. | | | |
| Board Runtime Power Consumption Reporting. This value shall be optionally reported over the management binding interface. The runtime power value shall report the card edge power. | Optional | Optional | Optional |
| PLDM for Platform Monitoring and Control (DSP0248 compliant) shall be used for transceiver and board power consumption reporting. | Required | Required | Required |

4.6 Pluggable Transceiver Module Status and Temperature Reporting

A pluggable transceiver module is a compact, hot-pluggable transceiver used to connect the OCP 3.0 NIC to an external physical medium. It is important for proper system operation to know the presence and temperature of pluggable transceiver modules. [Table 54](#) summarizes pluggable module status reporting requirements. The transceiver temperature is always reported and is independent of the ASIC die temperature reporting requirements as discussed in Section 4.4. The temperature reporting interface shall be accessible in Aux Power Mode, and Main Power Mode.

Table 54: Pluggable Module Status Reporting Requirements

| Requirement | RBT+MCTP Type | RBT Type | MCTP Type |
|--|---------------|----------|-----------|
| Pluggable Transceiver modules Presence Status and Temperature Reporting | Required | Required | Required |
| PLDM for Platform Monitoring and Control (DSP0248 compliant) for reporting the pluggable transceiver module presence status and pluggable transceiver module temperature | Required | Required | Required |

4.7 Management and Pre-OS Firmware Inventory and Update

An OCP NIC 3.0 implementation can have different types of firmware components for data path, control path, and management path operations. It is desirable that OCP NIC 3.0 implementations support an OS-independent mechanism for the management firmware update. It is desirable that the management firmware update does not require a system reboot for the new firmware image to become active. [Table 55](#) summarizes the firmware inventory and update requirements.

Table 55: Management and Pre-OS Firmware Inventory and Update Requirements

| Requirement | RBT+MCTP Type | RBT Type | MCTP Type |
|---|---------------|-------------|-----------|
| Network boot in UEFI driver (supporting both IPv4 and IPv6 addressing for network boot) | Required | Required | Required |
| UEFI secure boot for UEFI drivers | Required | Required | Required |
| UEFI Firmware Management Protocol (FMP) | Required | Required | Required |
| PLDM for Firmware Update (DSP0267 compliant) | Required | Recommended | Required |

4.7.1 Secure Firmware

It is highly recommended that an OCP NIC 3.0 card supports a secure firmware feature. In the future versions of the OCP NIC 3.0 specification, the secure firmware feature is intended to be required. When the secure firmware feature is enabled and where export compliance permits, the OCP NIC 3.0 card shall verify firmware components prior to the execution, execute only signed and verified firmware components, and only allow authenticated firmware updates. Where applicable, an OCP NIC 3.0 implementation shall use the guidelines provided in NIST SP 800-193 Platform Resiliency Guidelines for the following secure firmware functions:

- Signed Firmware Updates
- Ensure only valid/authenticated firmware updates can be applied. Refer to: NIST 800-193 Section 3.5 Firmware Update Mechanisms, and 4.1.2 Root of Trust for Update (RTU) and Chain of Trust for Update (CTU)
- Ensure authentication mechanisms cannot be bypassed. Refer to NIST 800-193 Section 4.2 Protection.
- Secure Boot
- Only boot trusted/authenticated firmware: NIST 800-193 4.1.3 Root of Trust for Detection (RTD) and Chain of Trust for Detection (CTD), and Section 4.3 Detection
- Recovery mechanism in case of boot failure: NIST 800-193 Section 4.4 Recovery

4.7.2 Firmware Inventory

The OCP NIC 3.0 card shall allow queries to obtain the firmware component versions, device model, and device ID via in-band and out-of-band interfaces without impacting NIC function and performance of said paths.

4.7.3 Firmware Inventory and Update in Multi-Host Environments

A multi-host capable OCP NIC 3.0 card shall gracefully handle concurrent in-band queries from multiple hosts and out-of-band access from the BMC for firmware component versions, device model, and device ID information.

A multi-host capable OCP NIC 3.0 card shall only permit one entity to perform write accesses to NIC firmware at a time, without creating contention.

A multi-host capable OCP NIC 3.0 card shall gracefully handle exceptions when more than one entity attempts to perform concurrent NIC firmware writes.

4.8 NC-SI Package Addressing and Hardware Arbitration Requirements

NC-SI over RBT is implemented via RMII pins between the MC and the OCP NIC 3.0 card. Protocol and implementation details of NC-SI over RBT can be found in the DMTF DSP0222 standard.

4.8.1 NC-SI over RBT Package Addressing

NC-SI over RBT capable OCP NIC 3.0 cards shall use a unique Package ID per ASIC when multiple ASICs share the single NC-SI physical interconnect to ensure there are no addressing conflicts.

Baseboards use the Slot_ID[1:0] values on the Primary Connector for this identification. The value of Slot_ID[1:0] is determined by the encoding shown in [Table 56](#)~~Table 55~~. Slot_ID[1:0] is statically set high or low on the baseboard and is available on the OCP Bay portion of the Primary Connector.

Table 56: Slot_ID[1:0] to Package ID[2:0] Mapping

| Physical Slot (Dec.) | SLOT_ID[1:0] | | Package ID[2:0] | | |
|----------------------|--------------|------------|-----------------|---------------|---------------|
| | Pin OCP_A6 | Pin OCP_B7 | Package ID[2] | Package ID[1] | Package ID[0] |
| | SLOT_ID1 | SLOT_ID0 | PhysDev# | SLOT_ID1 | SLOT_ID0 |
| Slot 0 | 0 | 0 | 0/1 | 0 | 0 |
| Slot 1 | 0 | 1 | 0/1 | 0 | 1 |
| Slot 2 | 1 | 0 | 0/1 | 1 | 0 |
| Slot 3 | 1 | 1 | 0/1 | 1 | 1 |

Package ID[2:0] is a 3-bit field and is encoded in the NC-SI Channel ID as bits [7:5]. SLOT_ID1 is associated with Package ID[1]. SLOT_ID0 is associated with Package ID[0]. The Package ID[2] value is based on the silicon instance on the same physical OCP NIC 3.0 card. Package ID[2]==0b0 is assigned for physical controller #0. Package ID[2]==0b1 is assigned for physical controller #1. In this case, physical controller #1 on the same card is at an address offset of +0x4. Refer to the specific endpoint device datasheet for details on the Package ID configuration options.

Note: The Package ID[2] field is optionally configurable in the NC-SI specification. If the target silicon hard codes this bit to 0b0, then a card must only implement a single silicon instance to prevent addressing conflicts.

Refer to the DMTF DSP0222 standard for more information on package addressing and Package ID.

4.8.2 Arbitration Ring Connections

For baseboards that implement two or more Primary Connectors, the NC-SI over RBT arbitration ring shall be connected to each other. The arbitration ring shall support operation with one card, or multiple cards installed. Figure 95 shows an example connection with dual Primary Connectors.

4.9 SMBus 2.0 Addressing Requirements

The SMBus provides a low speed management bus for the OCP NIC 3.0 card. The FRU EEPROM is directly connected to the OCP NIC 3.0 card edge on this bus and can be read by the baseboard in the ID Mode, Aux Power Mode and Main Power Mode. Network controllers may utilize the SMBus 2.0 interface for MCTP communications. OCP NIC 3.0 does not support MCTP over I²C due to the use of specific SMBus 2.0 addressing. Proper power domain isolation shall be implemented on the NIC.

4.9.1 SMBus Address Map

OCN NIC 3.0 cards shall support the SMBus Address Resolution Protocol (ARP). This allows for dynamic assignment of slave device addresses. This method automatically resolves address conflicts and eliminates the need for manual address configuration. The SMBus address type can be either a Dynamic and Persistent Address or a Dynamic and Volatile Address. Refer to the SMBus 2.0 specification and Section 6.11 of DSP0237 for details on SMBus address assignment. Due to the prevalent use of SMBus muxes in many baseboard designs, the OCP NIC 3.0 card is discouraged from sending unsolicited messages, which includes the optional “Notify ARP Master” command.

A baseboard implementation may choose to only use fixed addresses for OCP NIC 3.0 cards. The assignment of these fixed addresses is system dependent and is outside the scope of this specification. When fixed addresses are used, then the OCP NIC 3.0 card shall be a “Fixed and Discoverable” SMBus device. Refer to the SMBus 2.0 specification for more details.

All predefined SMBus addresses for OCP NIC 3.0 are shown in ~~Table 57~~Table 56. Baseboard and OCP NIC 3.0 card designers must ensure additional devices do not conflict. The addresses shown are in 8-bit format and represent the read/write address pair.

Table 57: FRU EEPROM Address Map

| Physical Slot (Dec.) | SLOT_ID[1:0] | | FRU EEPROM Address | | | | |
|----------------------|--------------|------------|--------------------|----------|-------|----------------|-------------|
| | Pin OCP_A6 | Pin OCP_B7 | A2 | A1 | A0 | Binary Address | Hex Address |
| | SLOT_ID1 | SLOT_ID0 | SLOT_ID1 | SLOT_ID0 | Fixed | | |
| Slot 0 | 0 | 0 | 0 | 0 | 0 | 0b1010_000X | 0xA0/0xA1 |
| Slot 1 | 0 | 1 | 0 | 1 | 0 | 0b1010_010X | 0xA4/0xA5 |
| Slot 2 | 1 | 0 | 1 | 0 | 0 | 0b1010_100X | 0xA8/0xA9 |
| Slot 3 | 1 | 1 | 1 | 1 | 0 | 0b1010_110X | 0xAC/0xAD |

4.10 FRU EEPROM

4.10.1 FRU EEPROM Addressing and Size

A FRU EEPROM is implemented on the OCP NIC 3.0 cards and is used by the baseboard to determine the card type and capabilities. The FRU EEPROM is directly connected to the SMBus on the card edge. Only one EEPROM is required for a single physical OCP NIC 3.0 card regardless of the PCIe width or number of physical card edge connectors it occupies. The FRU EEPROM is mandatory and shall be connected to the Primary Connector SMBus.

The FRU EEPROM is readable in all four power states: ID mode, Programming mode, Aux Power Mode, and Main Power Mode.

The permissible EEPROM addresses are indicated in ~~Table 57~~Table 56. The write/read pair is presented in 8-bit format. The EEPROM shall use double byte addressing and, at minimum, shall be of sufficient size to hold the base FRU contents and any vendor specific information. The double byte write and read accesses are shown in 119 and Figure 120. Refer to the I²C specification for timing details.

Figure 119: FRU EEPROM Writes with Double Byte Addressing

Byte Write



Page Write

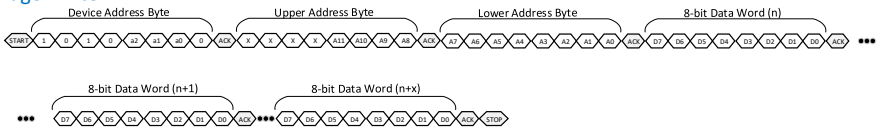
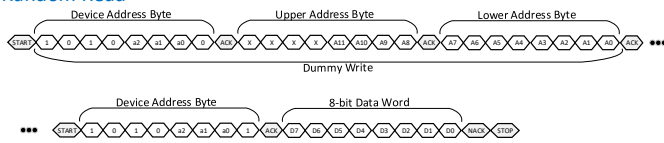


Figure 120: FRU EEPROM Reads with Double Byte Addressing

Random Read



Current Address Read



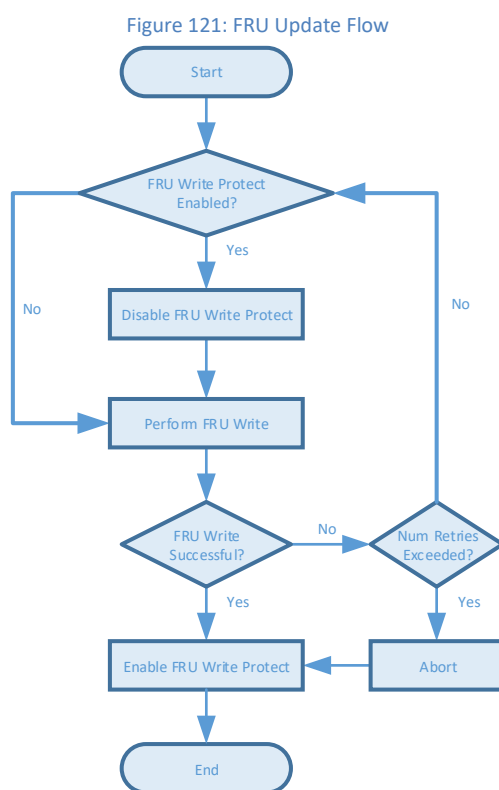
Current Sequential Read



4.10.2 FRU EEPROM Write Protection

The FRU EEPROM should be write protected for production cards. The FRU write protection may optionally be overridden for field updates via the use of a mechanical jumper or switch, a GPIO, controlled via a NC-SI or PLDM based mechanism, or the Programming Mode Power state. An OCP NIC 3.0 card may implement one or more of these write protection implementations. The definitions of these mechanisms are outside the scope of this specification. The NIC vendor write protection mechanism(s) shall be noted in the OEM Record. The FRU shall be writable for Programming mode power state, manufacturing test and during the card development cycle.

The FRU update flow is shown in Figure 121.



4.10.3 FRU EEPROM Content Requirements

The FRU EEPROM shall follow the data format specified in Section 1 of the IPMI Platform Management FRU Information Storage Definition specification. For OCP NIC 3.0, the FRU Information Device shall, at a minimum, contain the Common Header, Board Info Area, Product Info Area and a MultiRecord Area for storing the OEM record. These fields shall be populated in the FRU EEPROM. Where applicable, fields

common to the Board Info and Product Info records shall be populated with the same values so they are consistent.

The OEM record 0xC0 is used to store specific records for the OCP NIC 3.0 and is stored in the MultiRecord area of the FRU layout. For an OCP NIC 3.0 card, the FRU EEPROM OEM record content based on the format defined in [Table 58](#) shall be populated.

Note: [Table 58](#) only shows a portion of the OEM record. The complete record includes a Common Header and valid record checksum as defined in the IPMI Platform Management FRU Information Storage Definition specification.

Table 58: FRU EEPROM Record – OEM Record 0xC0, Offset 0x00

| Offset | Length | Description |
|--------|--------|---|
| 0 | 3 | <p>Manufacturer ID.</p> <p>For OCP NIC 3.0 compliant cards, the value of this field shall be set to the OCP IANA assigned number. This value is 42623 in decimal or 0x00A67F in hexadecimal. The least significant byte (0x7F) is first at offset 0 and the most significant byte (0x00) is at offset 2.</p> |
| 3 | 1 | <p>OCP NIC 3.0 FRU OEM Record Version.</p> <p>This field indicates the card OEM Record Version. Baseboards shall read this field to determine the OEM Record format. OCP NIC 3.0 cards compliant to this version of the specification shall be set the field to 0x01. Future changes to the OEM Record format will result in an additional record version value added to this list.</p> <p>0x00 – Reserved 0x01 – OCP NIC 3.0 card FRU record released with version 0.90 0x02 – OCP NIC 3.0 card FRU record released with version 1.1 0x03 – 0xFF – Reserved</p> |
| 4 | 1 | <p>Card Max power (in Watts) in Main Power Mode.</p> <p>The encoded value is the calculated max power of the OCP NIC 3.0 card in the Main Power Mode only and does not include the consumed power by transceivers plugged into the line side receptacle(s).</p> <p>0x00 – 0xFE – Card power rounded up to the nearest Watt for fractional values. 0xFF – Unknown</p> |
| 5 | 1 | <p>Card Max power (in Watts) in Aux Power Mode.</p> <p>The encoded value is the calculated max power of the OCP NIC 3.0 card in the Aux Power Mode only and does not include the consumed power by transceivers plugged into the line side receptacle(s).</p> <p>0x00 – 0xFE – Card power rounded up to the nearest Watt for fractional values. 0xFF – Unknown</p> |
| 6 | 1 | <p>Hot Aisle Card Cooling Tier with Passive Cables or RJ45.</p> <p>The encoded value reports the OCP NIC 3.0 Card Hot Card Cooling Tier as defined in Section 6.6 for cards with passive pluggable cables or with RJ45 for the line side I/O.</p> |

| Offset | Length | Description |
|--------|--------|--|
| | | 0x00 – Reserved 0x01 – Hot Aisle Cooling Tier 1 0x02 – Hot Aisle Cooling Tier 2 0x03 – Hot Aisle Cooling Tier 3 0x04 – Hot Aisle Cooling Tier 4 0x05 – Hot Aisle Cooling Tier 5 0x06 – Hot Aisle Cooling Tier 6 0x07 – Hot Aisle Cooling Tier 7 0x08 – Hot Aisle Cooling Tier 8 0x09 – Hot Aisle Cooling Tier 9 0x0A – Hot Aisle Cooling Tier 10 0x0B – Hot Aisle Cooling Tier 11 0x0C – Hot Aisle Cooling Tier 12 0x0D – 0xFE – Reserved 0xFF – Unknown |
| 7 | 1 | Cold Aisle Card Cooling Tier with Passive Cables or RJ45. The encoded value reports the OCP NIC 3.0 Card Cold Aisle Cooling Tier as defined in Section 6.6 for cards with passive pluggable cables or with RJ45 for the line side I/O. 0x00 – Reserved 0x01 – Cold Aisle Cooling Tier 1 0x02 – Cold Aisle Cooling Tier 2 0x03 – Cold Aisle Cooling Tier 3 0x04 – Cold Aisle Cooling Tier 4 0x05 – Cold Aisle Cooling Tier 5 0x06 – Cold Aisle Cooling Tier 6 0x07 – Cold Aisle Cooling Tier 7 0x08 – Cold Aisle Cooling Tier 8 0x09 – Cold Aisle Cooling Tier 9 0x0A – Cold Aisle Cooling Tier 10 0x0B – Cold Aisle Cooling Tier 11 0x0C – Cold Aisle Cooling Tier 12 0x0D – 0xFE – Reserved 0xFF – Unknown |
| 8 | 1 | Card active/passive cooling. This byte defines if the card has passive cooling (there is no fan on the card) or active cooling (a fan is located on the card). 0x00 – Passive Cooling 0x01 – Active Cooling 0x02 – 0xFE – Reserved 0xFF – Unknown |
| 9 | 2 | Hot aisle standby airflow requirement with Active Cables. The encoded value represents the amount of airflow, in LFM, required to cool the card in Aux Power Mode with active cables while operating in a hot aisle environment with an approach air temperature of 45 °C. Refer to Section 6 for more information about the thermal and environmental requirements. Byte 9 is the least significant byte, byte 10 is the most significant byte. 0x0000 – Card only supports passive cables (e.g., Direct Attached Cables or RJ45) |

| Offset | Length | Description |
|--------|--------|---|
| | | 0x0001 – 0xFFFE – LFM required for cooling card in Hot Aisle Operation. 0xFFFF – Unknown. |
| 11 | 2 | <p>Cold aisle standby airflow requirement with Active Cables.</p> <p>The encoded value represents the amount of airflow, in LFM, required to cool the card in Aux Power Mode with active cables while operating in a cold aisle environment with an approach air temperature of 35 °C. Refer to Section 6 for more information about the thermal and environmental requirements.</p> <p>Byte 11 is the least significant byte, byte 12 is the most significant byte.</p> <p>0x0000 – Card only supports passive cables (e.g., Direct Attached Cables or RJ45)</p> <p>0x0001 – 0xFFFE – LFM required for cooling card in Cold Aisle Operation. 0xFFFF – Unknown.</p> |
| 13 | 1 | <p>UART Configuration 1 – Secondary Connector.</p> <p>This byte denotes the UART configuration 1. A value 0x00 means no serial connection is implemented on the Secondary Connector card edge.</p> <p>Bits [2:0] denotes the UART baud rate per the encoding table below. If implemented, the encoded field value defines the default baud rate of the OCP NIC 3.0 card serial port.</p> <p>0b000 – No serial connection 0b001 – 115200 baud 0b010 – 57600 baud 0b011 – 38400 baud 0b100 – 19200 baud 0b101 – 9600 baud 0b110 – 4800 baud 0b111 – 2400 baud</p> <p>Bits [4:3] denotes the number of data bits.</p> <p>0b00 – No serial connection 0b01 – 7 data bits 0b10 – 8 data bits 0b11 – Reserved</p> <p>Bits [7:5] denotes the parity bit character.</p> <p>0b000 – No serial connection 0b001 – None (N) 0b010 – Odd (O) 0b011 – Even (E) 0b100 – Mark (M) 0b101 – Space (S) 0b110 – Reserved 0b111 – Reserved</p> |
| 14 | 1 | <p>UART Configuration 2 – Secondary Connector.</p> <p>This byte denotes the UART configuration 2. A value 0x00 means no serial connection is implemented on the Secondary Connector card edge.</p> <p>Bits [1:0] denotes the number of stop bits.</p> <p>0b00 – No serial connection 0b01 – 1 stop bit 0b10 – 1.5 stop bits 0b11 – 2 stop bits</p> |

| Offset | Length | Description |
|--------|--------|--|
| | | <p>Bits [3:2] denotes the flow control method.</p> <p>0b00 – No serial connection</p> <p>0b01 – Software handshaking</p> <p>0b10 – No handshaking</p> <p>0b11 – Reserved</p> <p>Bits [7:4] are reserved and shall be encoded to a value of 0b0000.</p> |
| 15 | 1 | <p>USB Present – Primary Connector.</p> <p>This byte denotes a USB 2.0 connection is implemented on the Primary Connector card edge.</p> <p>0x00 – No USB 2.0 is present or is not implemented on the card edge.</p> <p>0x01 – A USB 2.0 connection is implemented on the card edge.</p> <p>0x02 – 0xFE – Reserved for future use</p> <p>0xFF – Unknown</p> |
| 16 | 1 | <p>Manageability Type.</p> <p>This byte denotes the card manageability type and interface used.</p> <p>0x00 – No manageability</p> <p>0x01 – RBT Type</p> <p>0x02 – MCTP Type</p> <p>0x03 – RBT + MCTP Type</p> <p>0x04-0xFE – Reserved for future use</p> <p>0xFF – Unknown</p> |
| 17 | 1 | <p>FRU Write Protection Mechanism.</p> <p>This byte defines the FRU write protection mechanism implemented on the OCP NIC 3.0 card. Multiple FRU write projection mechanisms may be simultaneously supported on the OCP NIC 3.0 card. Refer to Section 4.10.2 for details.</p> <p>Bit 0 – FRU EEPROM is not write protected.</p> <p>Bit 1 – FRU EEPROM is statically write protected. No field updates permissible.</p> <p>Bit 2 – FRU EEPROM is write protected via a mechanical jumper or switch.</p> <p>Bit 3 – FRU EEPROM write protection is controlled via network silicon GPIO.</p> <p>Bit 4 – FRU EEPROM write protection is controlled via an NC-SI or PLDM based mechanism.</p> <p>Bit 5 – FRU EEPROM write protection is controlled by the Programming Mode power state.</p> <p>Bits [6:7] – Reserved for future use.</p> <p>0xFF – Unknown.</p> |
| 18 | 1 | <p>Programming Mode Power State supported.</p> <p>This byte defines support for the Programming Mode power state. If supported, the FRU EEPROM write protect mechanism is disabled for field updates. Refer to Section 3.8 for details on the Programming Mode power state.</p> <p>0x00 – Programming Mode power state not supported.</p> <p>0x01 – Programming Mode power state supported.</p> <p>0x02 – 0xFE – Reserved for future use.</p> <p>0xFF – Unknown.</p> |
| 19 | 1 | <p>Hot Aisle Card Cooling Tier with Active Cables.</p> |

| Offset | Length | Description |
|--------|--------|---|
| | | <p>The encoded value reports the OCP NIC 3.0 Card Hot Aisle Card Cooling Tier as defined in Section 6.6 for cards with active pluggable cables for the line side I/O.</p> <p>0x00 – Card only supports passive cables (e.g., Direct Attached Cables or RJ45) 0x01 – Hot Aisle Cooling Tier 1 0x02 – Hot Aisle Cooling Tier 2 0x03 – Hot Aisle Cooling Tier 3 0x04 – Hot Aisle Cooling Tier 4 0x05 – Hot Aisle Cooling Tier 5 0x06 – Hot Aisle Cooling Tier 6 0x07 – Hot Aisle Cooling Tier 7 0x08 – Hot Aisle Cooling Tier 8 0x09 – Hot Aisle Cooling Tier 9 0x0A – Hot Aisle Cooling Tier 10 0x0B – Hot Aisle Cooling Tier 11 0x0C – Hot Aisle Cooling Tier 12 0x0D – 0xFE – Reserved 0xFF – Unknown</p> |
| 20 | 1 | <p>Cold Aisle Card Cooling Tier with Active Cables.</p> <p>The encoded value reports the OCP NIC 3.0 Card Cold Aisle Card Cooling Tier as defined in Section 6.6 for cards with active pluggable cables for the line side I/O.</p> <p>0x00 – Card only supports passive cables (e.g., Direct Attached Cables or RJ45) 0x01 – Cold Aisle Cooling Tier 1 0x02 – Cold Aisle Cooling Tier 2 0x03 – Cold Aisle Cooling Tier 3 0x04 – Cold Aisle Cooling Tier 4 0x05 – Cold Aisle Cooling Tier 5 0x06 – Cold Aisle Cooling Tier 6 0x07 – Cold Aisle Cooling Tier 7 0x08 – Cold Aisle Cooling Tier 8 0x09 – Cold Aisle Cooling Tier 9 0x0A – Cold Aisle Cooling Tier 10 0x0B – Cold Aisle Cooling Tier 11 0x0C – Cold Aisle Cooling Tier 12 0x0D – 0xFE – Reserved 0xFF – Unknown</p> |
| 21 | 1 | <p>Transceiver Reference Power Level.</p> <p>The encoded value denotes the reference power envelope for active transceivers that was used to determine the card thermal tier. The active cable power class is defined in the respective module management interface specifications:</p> <p>SFF-8472 for SFP modules – Power level 1 through 3. SFF-8636 for QSFP modules – Power Classes 1 through 8.</p> <p>0x00 – Passive Cable 0x01 – QSFP Active cable Power Class 1 (1.5 W max) / SFP Level 1 (1.0 W max) 0x02 – QSFP Active cable Power Class 2 (2.0 W max) / SFP Level 2 (1.5 W max) 0x03 – QSFP Active cable Power Class 3 (2.5 W max) / SFP Level 3 (2.0 W max)</p> |

| Offset | Length | Description |
|--------|--------|---|
| | | <p>0x04 – QSFP Active cable Power Class 4 (3.5 W max) 0x05 – QSFP Active cable Power Class 5 (4.0 W max) 0x06 – QSFP Active cable Power Class 6 (4.5 W max) 0x07 – QSFP Active cable Power Class 7 (5.0 W max) 0x08 – QSFP Active cable Power Class 8 (10.0 W max) 0x09 – 0xFE – Reserved 0xFF – Unknown</p> |
| 22 | 1 | <p>Transceiver Reference Temperature Level. The encoded value denotes the reference active transceiver temperature limit, in degrees Celsius, that was used to determine the card thermal tier. 0x00 – Passive Cable 0x01 – 0xFE – Transceiver max operating temperature 0xFF – Unknown</p> |
| 23 | 1 | <p>Card Thermal Tier with Local Fan Fail. The encoded value denotes the required thermal tier when the OCP NIC 3.0 active cooling fails. 0x00 – Card requires the same thermal tier when the active cooling fan fails or the OCP NIC 3.0 card uses passive cooling. 0x01 – Card requires Cooling Tier 1 with card fan failure 0x02 – Card requires Cooling Tier 2 with card fan failure 0x03 – Card requires Cooling Tier 3 with card fan failure 0x04 – Card requires Cooling Tier 4 with card fan failure 0x05 – Card requires Cooling Tier 5 with card fan failure 0x06 – Card requires Cooling Tier 6 with card fan failure 0x07 – Card requires Cooling Tier 7 with card fan failure 0x08 – Card requires Cooling Tier 8 with card fan failure 0x09 – Card requires Cooling Tier 9 with card fan failure 0x0A – Card requires Cooling Tier 10 with card fan failure 0x0B – Card requires Cooling Tier 11 with card fan failure 0x0C – Card requires Cooling Tier 12 with card fan failure 0x0D – 0xFE – Reserved 0xFF – Unknown</p> |
| 24 | 1 | <p>Aux Power Supported Ports Each bit indicates if the corresponding port can be active in Aux Power Mode. This is a bit map representation. The LSB represents Port 1, the MSB represents Port 8. Refer to Section 3.7.1 for the port numbering nomenclature. Examples: 0b00000000 – Configuration unknown. 0b00000001 – Only Port 1 can be active in Aux Power Mode. 0b00000010 – Only Port 2 can be active in Aux Power Mode. 0b00000011 – Ports 1 and 2 can be active in Aux Power Mode. Etc.</p> |
| 25 | 2 | <p>Hot aisle standby airflow requirement with Passive Cables or RJ45. The encoded value represents the amount of airflow, in LFM, required to cool the card in Aux Power Mode with passive cables or RJ45 while operating in a hot aisle environment with an approach air temperature of 45 °C. Refer to Section 6 for more information about the thermal and environmental requirements.</p> |

| Offset | Length | Description |
|---------|--------|---|
| | | Byte 25 is the least significant byte, byte 26 is the most significant byte. 0x0000-0xFFFF – LFM required for cooling card in Hot Aisle Operation. 0xFFFF – Unknown. |
| 27 | 2 | Cold aisle standby airflow requirement with Passive Cables or RJ45. The encoded value represents the amount of airflow, in LFM, required to cool the card in Aux Power Mode with passive cables or RJ45 while operating in a cold aisle environment with an approach air temperature of 35 °C. Refer to Section 6 for more information about the thermal and environmental requirements. Byte 27 is the least significant byte, byte 28 is the most significant byte. 0x0000-0xFFFF – LFM required for cooling card in Cold Aisle Operation. 0xFFFF – Unknown. |
| 29:30 | 2 | Reserved for future use. Set each byte to 0xFF for this version of the specification. |
| 31 | 1 | Number of Physical Controllers (N). This byte denotes the number of SMBus connected physical controllers on the OCP NIC 3.0 card. If N=0, no controllers exist on this OCP NIC 3.0 card and this is the last byte in the FRU OEM Record. If N≥1, then the controller UDID records below shall be included for each controller N. |
| 32:47 | 16 | Controller 1 UDID (if applicable). This field reports the Controller 1 Unique Device Identifier (UDID) and is used to aid in the dynamic slave address assignment over the SMBus Address Resolution Protocol. The format of the UDID string is defined in the SMBus 2.0 specification. This field shall list the most significant byte first (to align the FRU order to the reported UDID order on the SMBus). This field is populated with the UDID for Controller 1. This field is omitted and is of zero length if controller 1 is not present. |
| 48:63 | 16 | Controller 2 UDID (if applicable). See Controller 1 UDID description above. |
| 64:79 | 16 | Controller 3 UDID (if applicable). See Controller 1 UDID description above. |
| 80:95 | 16 | Controller 4 UDID (if applicable). See Controller 1 UDID description above. |
| 96:111 | 16 | Controller 5 UDID (if applicable). See Controller 1 UDID description above. |
| 112:127 | 16 | Controller 6 UDID (if applicable). See Controller 1 UDID description above. |

4.10.4 FRU Template

A FRU template is provided as a baseline implementation example. This FRU template contains the IPMI Platform Management FRU Information Storage Definition Product Info, Board Info records as well as the OEM record for OCP NIC 3.0.

The FRU template file may be downloaded from the OCP NIC 3.0 Wiki site:

<http://www.opencompute.org/wiki/Server/Mezz>.

5 Routing Guidelines and Signal Integrity Considerations

5.1 NC-SI over RBT

The NC-SI over RBT requirements in this section apply to the SFF, TSFF and LFF OCP NIC 3.0 cards. Designers shall use the appropriate SFF, TSFF or LFF timing parameters for the design calculations. The SFF and TSFF timing parameters are equivalent since the same card and baseboard PBA may be used.

The overall end-to-end timing budget is computed by the formula below. The values of each parameter are shown in ~~Table 59~~Table 58 and in DSP0222. The overall BMC pad to ASIC pad timing budget is 3 ns assuming the values shown. This value is inclusive of the RBT isolation buffer on the baseboard, propagation delay through the OCP connector, clock jitter or any clock buffers that may be implemented on the OCP NIC 3.0 card. The addition of these components subtracts from the total available budget.

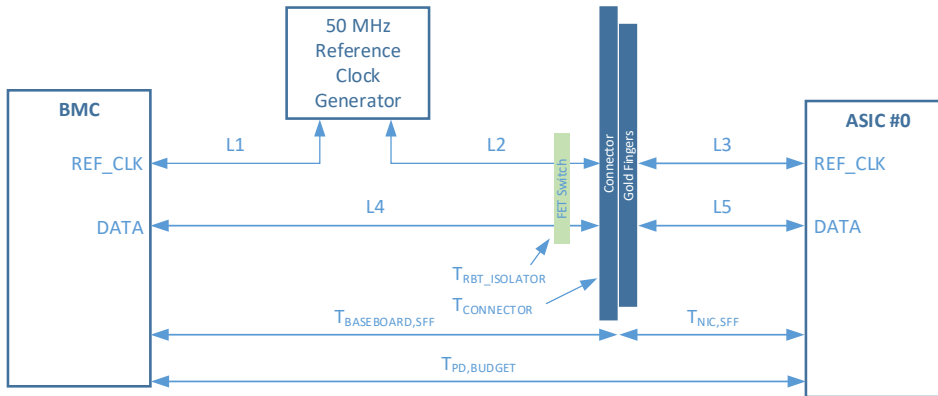
$$\begin{aligned}
 \text{Total timing budget} &= T_{\text{CLK}} - T_{\text{CO}(\text{max})} - T_{\text{SU}(\text{min})} - T_{\text{SKEW}(\text{max})} \\
 &= 20 \text{ ns} - 12.5 \text{ ns} - 3 \text{ ns} - 1.5 \text{ ns} \\
 &= 3 \text{ ns}
 \end{aligned}$$

Table 59: NC-SI over RBT Timing Parameters

| Parameter | Value | Description |
|--|---------|--|
| $T_{\text{PD,BUDGET}}$ | 3000 ps | Total propagation delay budget between BMC and the target ASIC. |
| $T_{\text{BASEBOARD,SFF}}$ | 2100 ps | Max permissible propagation delay on a SFF/TSFF baseboard. |
| $T_{\text{BASEBOARD,LFF}}$ | 1650 ps | Max permissible propagation delay on a LFF baseboard. |
| $T_{\text{NIC,SFF}}$ | 900 ps | Max permissible propagation delay for a SFF/TSFF OCP NIC 3.0 card. |
| $T_{\text{NIC,LFF}}$ | 1350 ps | Max permissible propagation delay for a LFF OCP NIC 3.0 card. |
| T_{CLK} | 20 ns | 50 MHz RBT REF_CLK_IN frequency period. |
| $T_{\text{CO}(\text{max})}$ | 12.5 ns | Clock-to-out value per DSP0222 |
| $T_{\text{SU}(\text{min})}$ | 3 ns | RBT single ended signal data setup to REF_CLK RBT_CLK_IN rising edge |
| $T_{\text{SKEW}(\text{max})}$ | 1.5 ns | Max permissible clock REF_CLK RBT_CLK_IN skew between any two devices in the system – BMC and target NIC ASIC(s). |
| $T_{\text{RBT_ISOLATOR}(\text{max})}$ | - | Baseboard RBT isolator propagation delay. Value is dependent on device selection. Baseboard implementers shall include this value in the timing budget calculations. |
| $T_{\text{CONNECTOR,STRADDLE}}$ | 110 ps | OCP NIC 3.0 straddle mount connector propagation delay. This value is the assumed worst case value for all straddle mount connector configurations. |
| $T_{\text{CONNECTOR,RA}}$ | 130 ps | OCP NIC 3.0 right angle connector propagation delay. This value is the assumed worst case value for all right angle connector configurations. |
| $T_{\text{CLK_BUF}(\text{max})}$ | - | OCP NIC 3.0 clock buffer propagation delay. Value is dependent on device selection. OCP NIC 3.0 implementers shall include this value in the timing budget calculations. |

| Parameter | Value | Description |
|-------------------------|-------|--|
| T _{JITTER_REF} | - | Baseboard reference clock generator cycle-to-cycle clock jitter. Value is dependent on device selection. Baseboard implementers shall include this value in the timing budget calculations. |
| T _{JITTER_NIC} | - | OCP NIC 3.0 clock buffer cycle-to-cycle clock jitter (if implemented on the NIC). Value is dependent on device selection. OCP NIC 3.0 implementers shall include this value in the timing budget calculations. |

Figure 122: NC-SI over RBT Timing Budget Topology



The following sections define the portion of the overall propagation delay budget allocated to the baseboard and to the OCP NIC 3.0 card, as well as additional requirements for each. Baseboard and NIC implementers shall analyze their design to ensure the timing budget is not violated.

The traces shall be implemented as 50 Ω ±15% impedance-controlled nets. Baseboard and NIC designers are encouraged to follow the guidelines defined in the RMII and NC-SI specifications for physical routing. Refer to Section 3.4.4 and the DSP0222 specification for example interconnect topologies.

5.1.1 SFF/TSFF Baseboard Requirements

The SFF/TSFF baseboard is allocated a maximum propagation time of 2100 ps between the BMC and the connector edge. NC-SI over RBT isolation buffers are required on the baseboard. The requirements for additional add-in card loading are reduced. The available timing budget for the SFF/TSFF baseboard is computed by the formula below.

$$T_{BASEBOARD,SFF} = 2100 \text{ ps} - T_{RBT_ISOLATOR} - T_{CONNECTOR}$$

The skew requirement defines the max permissible clock skew (T_{SKEW}) between any two system devices. The T_{SKEW} calculation is computed by the formula below. This applies to both the devices on the baseboard and the NIC. L1 is the **REF_CLK** **RBT_CLK_IN** segment from the baseboard 50 MHz reference clock generator to the BMC. L2 is the **REF_CLK** **RBT_CLK_IN** segment between the baseboard clock

generator to the OCP NIC 3.0 connector and L3 is the segment between the SFF/TSFF OCP NIC 3.0 card gold fingers and the target ASIC. Refer to Figure 122 for details. The max permissible value of L3 is $T_{NIC,SFF} = 900$ ps as discussed in Section 5.1.3. Baseboard vendors shall take this value into consideration when analyzing the available timing budget.

$$T_{SKEW(max)} \leq |L1 - (L2 + T_{CONNECTOR} + L3)|$$

5.1.2 LFF Baseboard Requirements

The LFF baseboard is allocated a maximum propagation time of 1650 ps between the BMC and the connector edge. NC-SI over RBT isolation buffers are required on the baseboard. The requirements for additional add-in card loading are reduced. The available timing budget for the LFF baseboard is computed by the formula below.

$$T_{BASEBOARD,LFF} = 1650 \text{ ps} - T_{RBT_ISOLATOR} - T_{CONNECTOR}$$

Similar to the SFF/TSFF implementation, the LFF clock skew parameter $T_{SKEW(max)}$ must not be exceeded. The max permissible value of L3 is $T_{NIC,LFF} = 1350$ ps. Refer to Section 5.1.1 for the skew computation requirements.

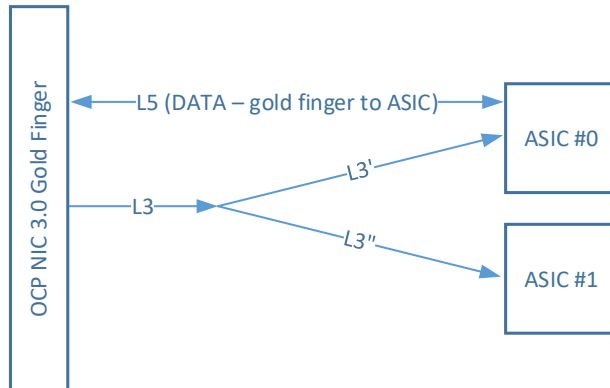
5.1.3 SFF/TSFF OCP NIC 3.0 Card Requirements

The SFF/TSFF OCP NIC 3.0 card is allocated a maximum propagation time of $T_{NIC,SFF} = 900$ ps between the card gold finger and the ASIC pad for both the clock and data signals. The total card propagation delay from the RBT clock input towards the card to the RBT outputs from the card shall be less than 14.3 ns ($T_{CO(max)} + 2 \times T_{NIC,SFF}$) when measured at the corresponding SFF/TSFF OCP NIC 3.0 gold fingers. This can be achieved by using an ASIC with the worst case Clock-to-Out ($T_{CO,MAX}$) value of 12.5 ns specified by DSP0222, and each SFF/TSFF OCP NIC 3.0 card-side RBT signal not exceeding a max propagation time of 900 ps.

This propagation delay is equivalent to a max length of 5.1 inches assuming standard FR4 material with a propagation delay of 175 ps/in. Additional trace length may be achieved with the use of a higher propagation velocity material (e.g., material with a lower dielectric constant) on the baseboard and OCP NIC 3.0 card or simultaneously using both BMC and ASIC devices with an improved timing from Clock-to-Out ($T_{CO,MAX}$) value compared to the published value of 12.5 ns in DSP0222. For NIC implementations with clock buffers, the propagation delay of the buffer needs to be included in this timing budget (i.e., $L3 + T_{CLK_BUF} + L3' + T_{CO,MAX} + L5$ shall be less than 14.3 ns) as shown in Figure 124.

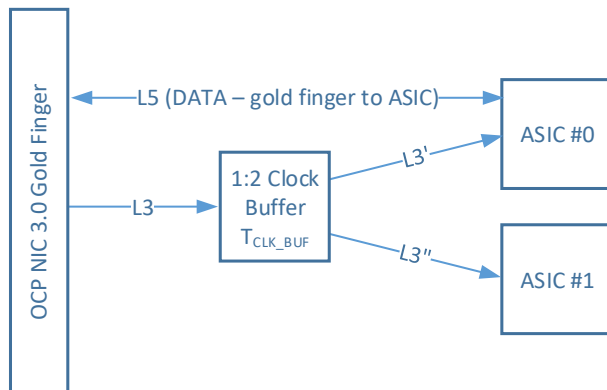
If multiple ASICs are utilized, the RBT_CLK_IN signal may be routed with a T-topology as shown in Figure 123. The trace length would be calculated as the delay summation of segment L3 + L3' for ASIC #0 and L3 + L3'' for ASIC #1. The data path delay to the ASIC is L5.

Figure 123: NC-SI over RBT Propagation Delay Matching for Two Target ASICs – No Clock Buffer



A clock buffer is optionally permitted if the NIC timing budget is not violated. This is shown in Figure 124. In this case, the trace length would be calculated as the delay summation of trace segment L3 + T_{CLK_BUF} + L3' for ASIC #0, and L3 + T_{CLK_BUF} + L3'' for ASIC #1.

Figure 124: NC-SI over RBT Propagation Delay Matching for Two Target ASICs – Clock Buffer



5.1.4 LFF OCP NIC 3.0 Card Requirements

Similar to the SFF/TSFF, a LFF OCP NIC 3.0 Card is allocated a maximum propagation time of $T_{NIC,LFF} = 1350$ ps between the card gold finger and the ASIC pad for both the clock and data signals. The segment L3 between the LFF OCP NIC 3.0 card gold fingers and the ASIC shall not exceed this propagation delay for a single and multi-ASIC target implementations. Refer to Section 5.1.3 for computation and topology considerations.

5.2 SMBus 2.0

For the SMBus 2.0 interface, both the baseboard and OCP NIC 3.0 designers shall follow the applicable requirements found in the SMBus, PCIe CEM specifications. This applies to the routing guidelines, SI considerations, bus operational speed range, capacitive loading, and range of pull up resistance values. Doing so allows the baseboard suppliers to design a SMBus interface that is compatible with OCP NIC 3.0 products.

5.3 PCIe

OCP NIC 3.0 card suppliers shall follow the PCIe routing specifications. Refer to the PCIe CEM and PCIe Base specifications for end-to-end channel signal integrity considerations.

5.3.1 Channel Requirements

The OCP NIC 3.0 PCIe channel requirements for PCI Express® Gen 4.0 align with the electrical budget and constraints as detailed in the PCI Express® CEM 4.0 Rev 1.0 and PCI Express Base Specification Rev 4.0. Exceptions or clarifications to the referenced specifications are noted in the sections below. The OCP NIC 3.0 PCIe channel requirements for PCI Express® Gen 5.0 differ from the PCI Express® CEM 5.0 Rev 0.7 for Insertion Loss Values as the loss was reduced on the OCP NIC 3.0 to allow the baseboard additional margin for SFF/TSFF implementations. The OCP NIC 3.0 LFF aligns with the specification. Refer to Section 5.3.1.2 for details.

5.3.1.1 REFCLK requirements

REFCLK requirements are detailed in the PCI Express CEM 5.0 Rev 0.7 Section 2.1.

5.3.1.2 Add-in Card Electrical Budgets

This section defines the OCP NIC 3.0 card channel budget from the gold finger edge to the end point silicon. The values listed below are shown for reference and mirrors that of the PCIe CEM 4.0 specification.

Table 60: PCIe Electrical Budgets

| Parameter | PCIe CEM 4.0 Rev 1.0 Specification Section | PCIe CEM 5.0 Rev 0.7 Specification Section |
|---|--|---|
| AC coupling capacitors | Section 4.7.1 | PCIe Base Specification 5.0 Section 8.3.9 Symbol C_{TX} |
| Insertion Loss Values (Voltage Transfer Function) | Section 4.7.2 and Appendix A. Section 4.7.10 for 16 GT/s | Section 4.7.2 and Appendix A. -7.0 dB at 16 GHz for SFF/TSFF ¹ Section 4.7.11 for LFF |
| Jitter Values | Section 4.7.3 for 8 GT/s and 16 GT/s. Also refer to the PCIe Base Specification 4.0 Section 8.3.5 | Section 4.7.3 for 8 GT/s, 16 GT/s and 32 GT/s. Also refer to the PCIe Base Specification 5.0 Section 8.3.5 |
| Crosstalk | Section 4.7.4 | Section 4.7.4 |
| Lane-to-lane skew (S_A) for Add-in cards | Section 4.7.5 | Section 4.7.5 |
| Transmitter Equalization | Section 4.7.6 and PCIe Base Spec Chapter 9 | Section 4.7.6 and PCIe Base Spec Chapter 9 |

| Parameter | PCIe CEM 4.0 Rev 1.0 Specification Section | PCIe CEM 5.0 Rev 0.7 Specification Section |
|---|--|--|
| Skew within a differential pair | Section 4.7.7 | Section 4.7.7 |
| Differential data trace impedance | Section 4.7.8 | Section 4.7.8 |
| Differential data trace propagation delay | Section 4.7.9 | Section 4.7.9 |

Note 1: OCP NIC 3.0 SFF/TSFF deviates from the PCIe CEM specification on Insertion Loss Values at PCIe Gen5 speeds (32GT/s only).

5.3.1.3 Baseboard Channel Budget

The baseboard channel budget directly follows the PCI Express CEM 4.0 Rev 1.0 specification. Details of the budget are outside of the scope of this specification.

5.3.1.4 SFF-TA-1002 Connector Channel Budget

Reference the SFF-TA-1002 Revision 1.1 or later.

5.3.1.5 Differential Impedance (Informative)

For PCIe transmit and receive differential pairs, the target impedance is 85 Ω \pm 10%.

For the PCIe REFCLKs, the target impedance is 100 Ω \pm 10%.

5.3.2 Test Fixtures

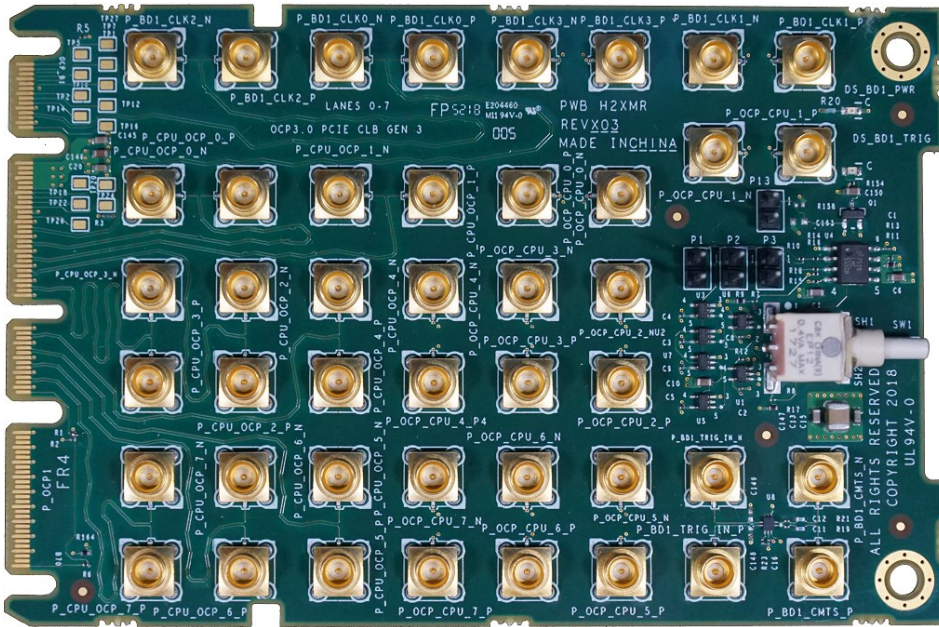
Test Fixtures are designed using the PCIe CEM CLB and CBB. The fixtures host interface has been modified to the OCP connector standard and there are three versions of the fixtures for both the SFF/TSFF and LFF OCP NIC 3.0 cards for Gen 3, Gen 4 and Gen 5 PCIe rates. Careful attention has been placed on these fixtures to help ensure that standard test equipment automation should work without significant modification. PCIe Gen 5 automation scripts may need to be modified as the OCP NIC 3.0 insertion loss budget differs from the PCIe CEM 5.0 32GT/s values.

Table 61: PCIe Test Fixtures for OCP NIC 3.0

| Test Fixture | PCIe Generation | PCB Material |
|--------------|-----------------|-------------------|
| Load Board | Gen 3 | TU863 |
| | Gen 4 | TU883 |
| | Gen 5 | TBD |
| Base Board | Gen 3 | TU863 |
| | Gen 4 | TBD (+vISI board) |
| | Gen 5 | TBD |

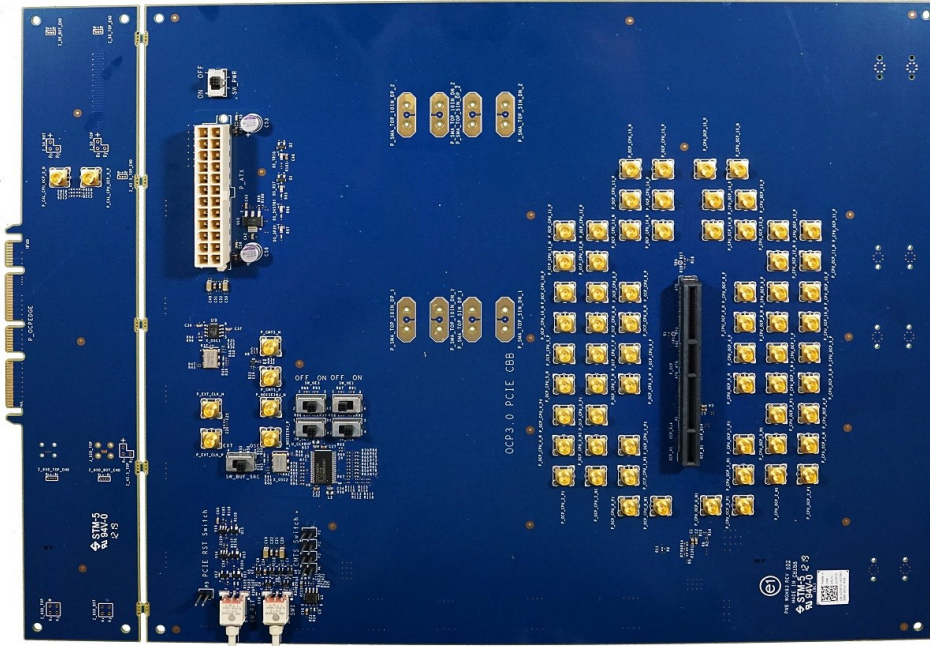
5.3.2.1 Compliance Load Board (CLB)

Figure 125: PCIe Load Board Test Fixture for OCP NIC 3.0 SFF/TSFF



5.3.2.2 Compliance Baseboard (CBB)

Figure 126: PCIe Base Board Test Fixture for OCP NIC 3.0 SFF/TSFF



5.3.3 Test Methodology

OCP NIC 3.0 is compliant to the applicable PCIe specifications. The electrical interface may be tested against the PCI Express® Architecture PHY Test Specification Revision 4.0, providing that the appropriate test fixtures from Section 5.3.2 are used.

For PCIe Gen 5.0, OCP NIC 3.0 modifies the insertion loss budget on the SFF/TSFF as shown in [Table 60](#) and the test methodology may need to be adjusted to compensate for this difference. The electrical interface may be tested against the PCI Express® Architecture PHY Test Specification Revision 5.0, providing that the appropriate test fixtures from Section 5.3.2 are used and the insertion loss difference is compensated.

5.3.3.1 Test Setup

This section is a work-in-progress by the OCP NIC 3.0 SI Subgroup. The following information will be added in a future document release:

- Description of the OCP NIC 3.0 CLB and CBB test figure for use in the PCIe Architecture PHY Test Specifications.
- A user guide is in development through UNH at the time of publication.

- The test procedure is based on the PCIe procedures. The differences between the procedures for PCIe Adapters and OCP NIC 3.0 cards will be documented in the user guide.

6 Thermal and Environmental

6.1 Airflow Direction

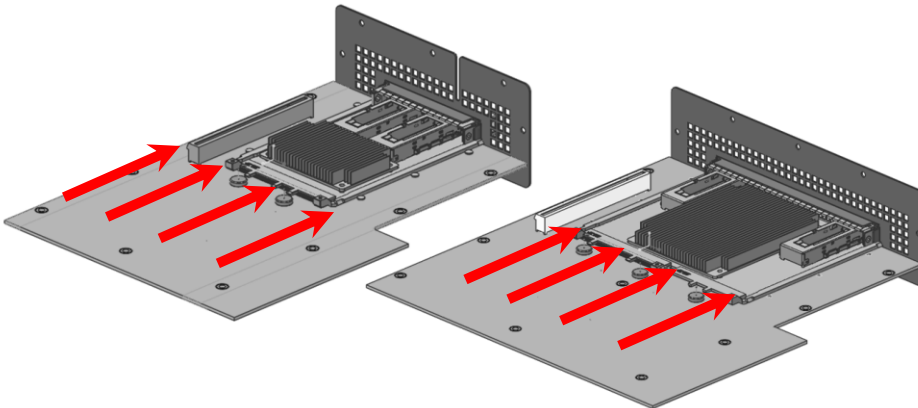
The OCP NIC 3.0 card is designed to operate in either of two different airflow directions which are referred to as Hot Aisle and Cold Aisle. In both Hot Aisle and Cold Aisle configurations all airflow is directed over the topside of the card. Component placement must assume that there will be no airflow on the bottom side of the card. The local approach air temperature and velocity to the card is dependent on the capability of the system adopting OCP NIC 3.0 card. These parameters may be impacted by the operational altitude and relative humidity in Hot Aisle or Cold Aisle configurations. Design boundary conditions for Hot Aisle and Cold Aisle cooling are included below in Sections 6.1.1 and 6.1.2 respectively.

The two airflow directions of the Hot and Cold Aisle cases should not result in multiple thermal solutions to separately satisfy the varying thermal boundary conditions. Ideally, any specific OCP NIC 3.0 card design should function in systems with either Hot Aisle or Cold Aisle cooling. Thermal analysis in support of this specification have shown the Hot Aisle configuration to be more challenging than Cold Aisle but card vendors should make that determination for each card that is developed.

6.1.1 Hot Aisle Cooling

The airflow in typical server systems will approach from the card edge or heatsink side of the card. This airflow direction is referred to as Hot Aisle cooling and is illustrated below in Figure 127. The term Hot Aisle refers to the card being located at the rear of the system where the local inlet airflow is preheated by the upstream system components (e.g., HDD, CPU, DIMM, etc.).

Figure 127: Airflow Direction for Hot Aisle Cooling (SFF/TSFF and LFF)



The boundary conditions for Hot Aisle cooling are shown below in [Table 62](#)~~Table 61~~ and [Table 63](#)~~Table 62~~. The low temperature is listed at 5 °C and assumes fresh air could be ducted to the back of the system from the front. More typically the inlet temperature to the OCP NIC 3.0 card will be in the same range as PCIe cards located at the back of the system (55 °C local inlet temperature). Depending on the system design, power density, and airflow the inlet temperature to the OCP NIC 3.0 card may be as high as 60 °C or 65 °C. The airflow velocities listed in [Table 63](#)~~Table 62~~ represent the airflow velocities typical

in mainstream servers. Higher airflow velocities are available within the Hot Aisle cooling tiers listed in [Table 68](#)~~Table 67~~ but card designers must be sure to understand the system level implications of such high card LFM requirements.

Table 62: Hot Aisle Air Temperature Boundary Conditions

| | Low | Typical | High | Max |
|-----------------------------|------------------------|---------|-------|-------|
| Local Inlet air temperature | 5 °C (system inlet) | 55 °C | 60 °C | 65 °C |

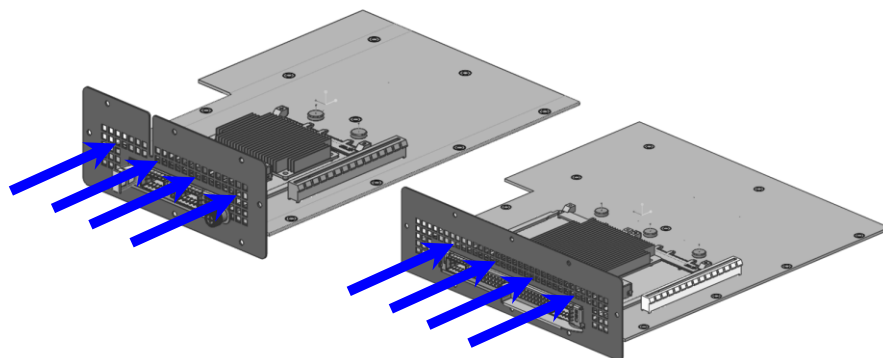
Table 63: Hot Aisle Airflow Boundary Conditions

| | Low | Typical | High | Max |
|--------------------------|--------|-------------|---------|---------------------|
| Local inlet air velocity | 50 LFM | 100-200 LFM | 300 LFM | System Dependent |

6.1.2 Cold Aisle Cooling

When installed in the front of a server the airflow will approach from the I/O connector (e.g., SFP, QSFP or RJ45) side of the card. This airflow direction is referred to as Cold Aisle cooling and is illustrated below in Figure 128. The term Cold Aisle refers to the card being located at the front of the system where the local inlet airflow is assumed to be the same temperature as the system inlet airflow.

Figure 128: Airflow Direction for Cold Aisle Cooling (SFF/TSFF and LFF)



The boundary conditions for Cold Aisle cooling are shown below in [Table 64](#)~~Table 63~~ and [Table 65](#)~~Table 64~~. The temperature values listed in [Table 64](#)~~Table 63~~ assume the inlet temperature to the OCP NIC 3.0 card to be the same as the system inlet. The low, typical, high, and max temperatures listed align with the ASHRAE A1, A2, A3, and A4 environmental classes. Depending on the system, the supported ASHRAE class may limit the maximum temperature to the OCP 3.0 NIC card. However, for more broad industry support, cards should be designed to the upper end of the ASHRAE classes (e.g., class A4).

Table 64: Cold Aisle Air Temperature Boundary Conditions

| | Low | Typical | High | Max |
|-----------------------------|------|--------------------------|--------------------|--------------------|
| Local Inlet Air Temperature | 5 °C | 25-35 °C ASHRAE A1/A2 | 40 °C ASHRAE A3 | 45 °C ASHRAE A4 |

Table 65: Cold Aisle Airflow Boundary Conditions

| Local Inlet Air Velocity | Low | Typical | High | Max |
|--------------------------|--------|---------|---------|------------------|
| | 50 LFM | 100 LFM | 200 LFM | System Dependent |

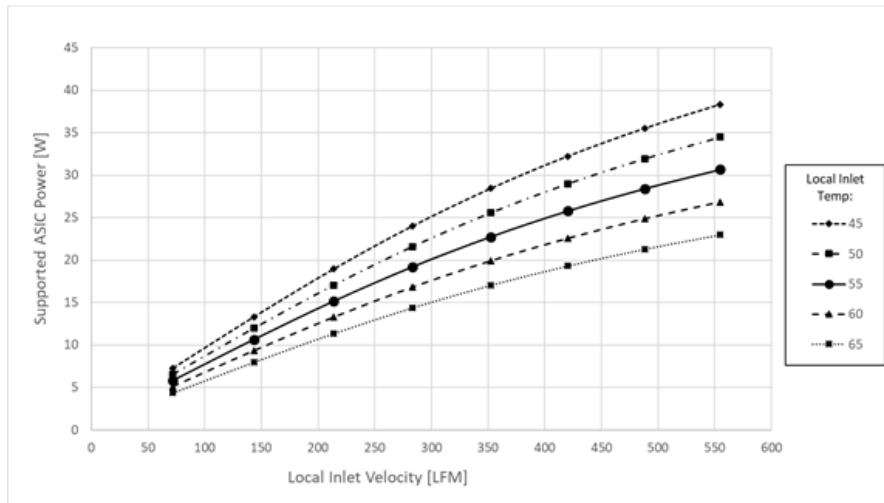
6.2 Thermal Design Guidelines

The information in this section is intended to serve as a quick reference guide for OCP NIC 3.0 designers early in the design process. The information should be used as a reference for upfront thermal design and feasibility and should not replace detailed card thermal design analysis. The actual cooling capability of the card shall be defined based on the testing with the OCP NIC 3.0 thermal test fixture as defined in Section 6.4.

6.2.1 SFF Card ASIC Cooling – Hot Aisle

The ASIC or controller chip is typically the highest power component on the card. Thus, as OCP NIC 3.0 cards are developed it is important to understand the ASIC cooling capability. Figure 129 below provides an estimate of the maximum ASIC power that can be supported as a function of the local inlet velocity for the SFF card in a hot aisle cooling configuration. Each curve in Figure 129 represents a different local inlet air temperature from 45 °C to 65 °C.

Figure 129: ASIC Supportable Power for Hot Aisle Cooling – SFF



The curves shown in Figure 129 were obtained using CFD analysis of a reference OCP NIC 3.0 SFF card. The reference card has a 20 mm x 20 mm ASIC with two QSFP connectors. Figure 130 shows a comparison of the 3D CAD and CFD model geometry for the reference OCP NIC 3.0 card. Additional card geometry parameters and boundary conditions used in the reference CFD analysis are summarized in [Table 66](#) ~~Table 65~~. The OCP NIC 3.0 simulation was conducted within a virtual version of the test fixture defined in Section 6.4.

Figure 130: OCP NIC 3.0 SFF Reference Design and CFD Geometry

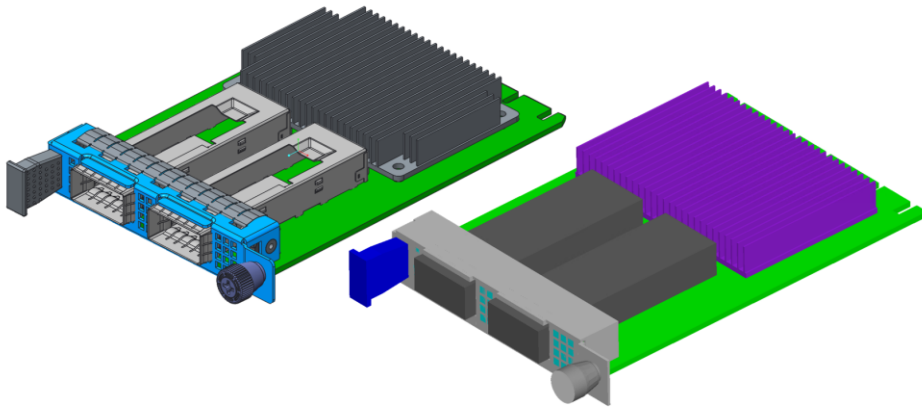


Table 66: Reference OCP NIC 3.0 SFF Card Geometry

| OCP NIC 3.0 Form Factor | SFF Card |
|-------------------------------|-----------------------|
| Heatsink Width | 65 mm |
| Heatsink Length | 45 mm |
| Heatsink Height | 9.24 mm |
| Heatsink Base Thickness | 1.5 mm |
| Fin Count/Thickness | 28/0.5 mm |
| Heatsink Material | Extruded Aluminum |
| ASIC Width | 20 |
| ASIC Length | 20 |
| ASIC Height | 2.26 |
| ASIC Theta-JC | 0.17 C/W |
| ASIC Theta-JB | 10 C/W |
| OCP PCB In-Plane Conductivity | 34 W/mK |
| OCP PCB Normal Conductivity | 0.33 W/mK |
| ASIC Max T-case | 95 °C |
| OCP NIC 3.0 I/O Connectors | Two QSFP @ 3.5 W each |

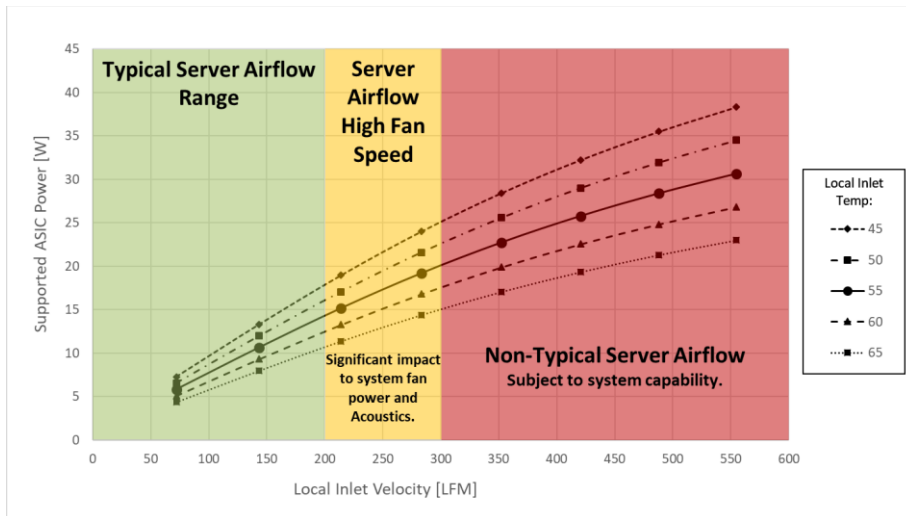
An increase in the supported ASIC power or a decrease in the required airflow velocity may be achieved through heatsink size and material changes. For example, a larger heatsink or a heatsink made out of copper could improve ASIC cooling and effectively shift up the supportable power curves shown in Figure 129.

It is important to point out that the curves shown in Figure 129 represent only the maximum ASIC power that can be supported vs. the supplied inlet velocity. Other heat loads on the card may require airflow velocities above and beyond that required to cool the ASIC. SFP or QSFP optical transceivers located downstream of the ASIC will in many cases pose a greater cooling challenge than the ASIC cooling.

Cooling the optical transceivers becomes even more difficult as the ASIC power is increased due to additional preheating of the air as it moves through the ASIC heatsink. OCP NIC 3.0 designers must consider all heat sources early in the design process to ensure the card thermal solution is sufficient for the feature set. In addition, OCP NIC 3.0 designers must consider all power modes in the design process – including Main Power Mode and Aux Power Mode. For both modes, the card designer must provide the airflow requirements in the OEM FRU record as described in Section 4.10.3.

Card designers must also consider the airflow capability of the server systems that the cards are targeted for use within. Figure 131 below shows the SFF ASIC supportable power curves with an overlay of three server airflow capability ranges. Designers must ensure that their thermal solutions and resulting card airflow requirements fall within the range of supportable system airflow velocity. Cards that are under-designed (e.g., require airflow greater than the system capability) will have thermal issues when deployed into the server system. Card designers are advised to work closely with system vendors to ensure they target the appropriate airflow and temperature boundary conditions.

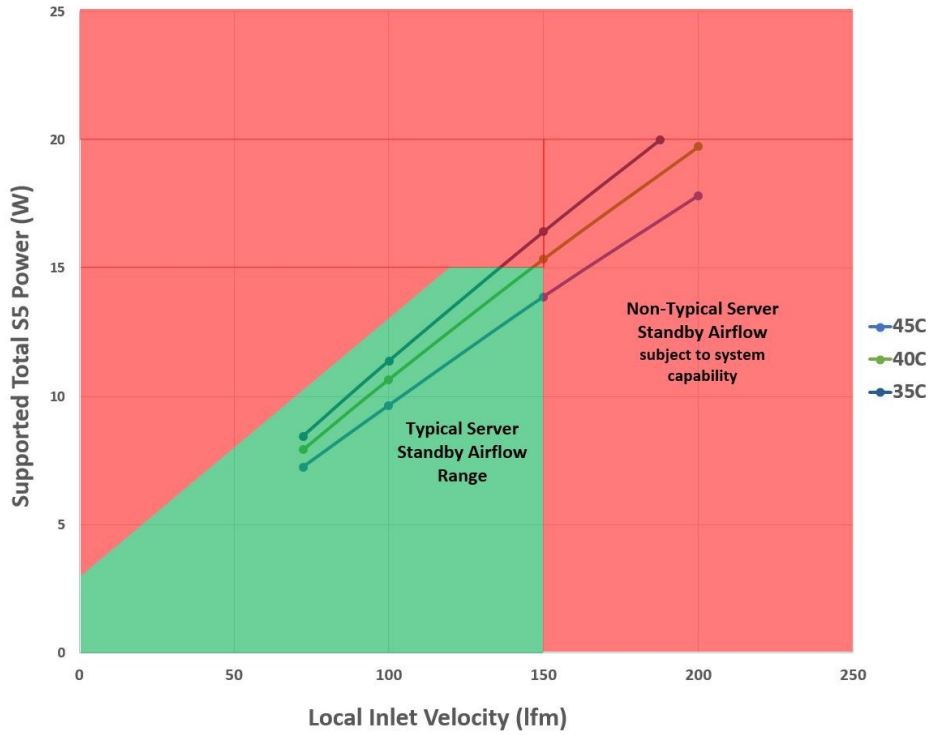
Figure 131: Server System Airflow Capability – SFF Card Hot Aisle Cooling



The server airflow capability is typically more restrictive when the OCP card is operating in Aux Power Mode. The airflow available from the system cooling solution is often more restrictive due to limited power budget available in Aux Power Mode. The graph below emphasizes that though the local OCP NIC 3.0 air temperature is typically lower in Main Power Mode (since preheating from upstream components should be greatly reduced while in standby), the upper bound of local air velocity is a fraction of what can be generated when the system is in Main Power Mode. Card vendors must test for these conditions, making sure that the provided cooling is sufficient for both the ASIC and any installed transceivers (which will still be receiving preheat from the ASIC in Aux Power Mode).

The NIC vendor shall provide the required LFM during for Aux Power Mode in the FRU EEPROM (see Section 4.10.3). The cold aisle should be tested at 35 °C; the hot aisle should be tested at 45 °C.

Figure 132: Server System Airflow Capability – SFF Card Hot Aisle Cooling in Aux Power Mode



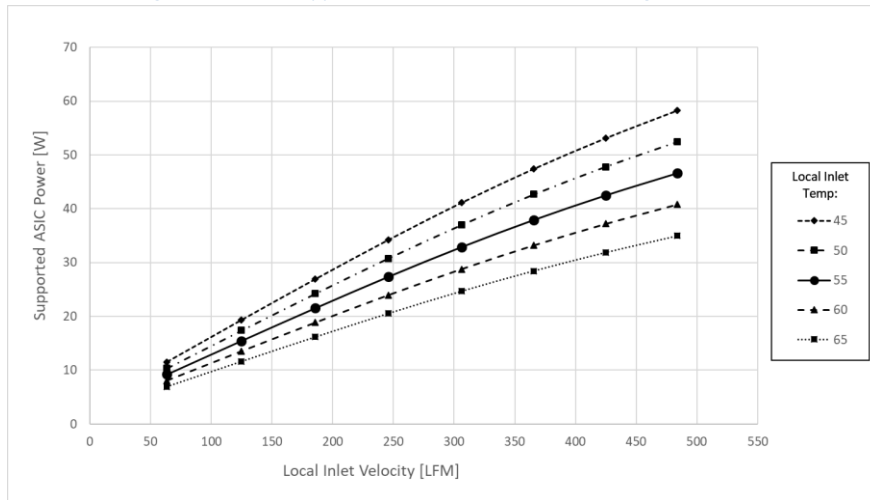
6.2.2 TSFF Card ASIC Cooling – Hot Aisle (TBD)

This section is a work in progress.

6.2.3 LFF Card ASIC Cooling – Hot Aisle

Figure 133 below provides an estimate of the maximum ASIC power that can be supported as a function of the local inlet velocity for the LFF card in a hot aisle cooling configuration. Each curve in Figure 133 represents a different local inlet air temperature from 45 °C to 65 °C.

Figure 133: ASIC Supportable Power for Hot Aisle Cooling – LFF Card



The curves shown in Figure 133 were obtained using CFD analysis of the reference OCP NIC 3.0 LFF card. The reference card has a 45 mm x 45 mm ASIC with two QSFP connectors. Additional card geometry parameters and boundary conditions used in the reference CFD analysis are summarized in [Table 67](#) and [Table 66](#). Figure 134 shows a comparison of the 3D CAD and CFD model geometry for the reference OCP NIC 3.0 card.

Figure 134: OCP NIC 3.0 LFF Reference Design and CFD Geometry

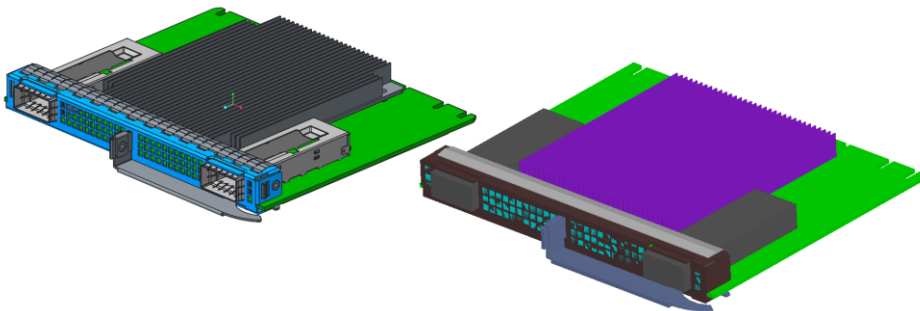


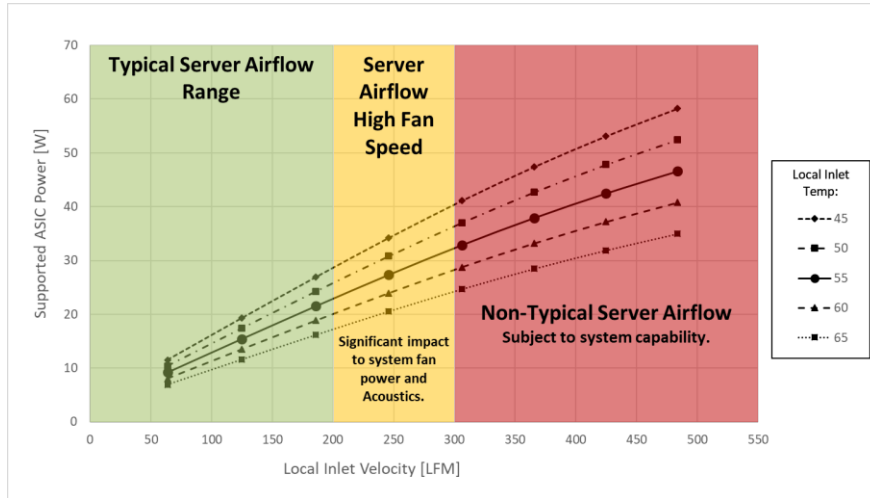
Table 67: Reference OCP NIC 3.0 LFF Card Geometry

| OCP NIC 3.0 Form Factor | LFF Card |
|-------------------------------|-----------------------|
| Heatsink Width | 75 mm |
| Heatsink Length | 85 mm |
| Heatsink Height | 9.3 mm |
| Heatsink Base Thickness | 1.5 mm |
| Fin Count/Thickness | 33/0.5 mm |
| Heatsink Material | Extruded Aluminum |
| ASIC Width | 45 |
| ASIC Length | 45 |
| ASIC Height | 2.13 |
| ASIC Theta-JC | 0.17 C/W |
| ASIC Theta-JB | 10 C/W |
| OCP PCB In-Plane Conductivity | 34 W/mK |
| OCP PCB Normal Conductivity | 0.33 W/mK |
| ASIC T-case Max | 95 °C |
| OCP NIC 3.0 I/O Connectors | Two QSFP @ 3.5 W each |

It is important to note that the supportable power for the LFF card is considerably higher than for the SFF card due to the increased size of the ASIC heatsink. In addition, optics module cooling on the LFF card will also be considerably improved due to the arrangement of the optics in parallel to the ASIC heatsink rather than in series. These thermal advantages are key drivers for the LFF card geometry. The OCP NIC 3.0 simulation was conducted within a virtual version of the LFF card test fixture defined in Section 6.4. In addition, OCP NIC 3.0 designers must consider all power modes in the design process – including Main Power Mode and Aux Power Mode. For both modes, the card designer must provide the airflow requirements in the OEM FRU record as described in Section 4.10.3.

Figure 135 below shows the LFF ASIC supportable power curves with an overlay of three server airflow capability ranges. Designers must ensure that their thermal solutions and resulting card airflow requirements fall within the range of supportable system airflow velocity. Cards that are under-designed (e.g., require airflow greater than the system capability) will have thermal issues when deployed into the server system. Card designers are advised to work closely with system vendors to ensure they target the appropriate airflow and temperature boundary conditions.

Figure 135: Server System Airflow Capability – LFF Card Hot Aisle Cooling

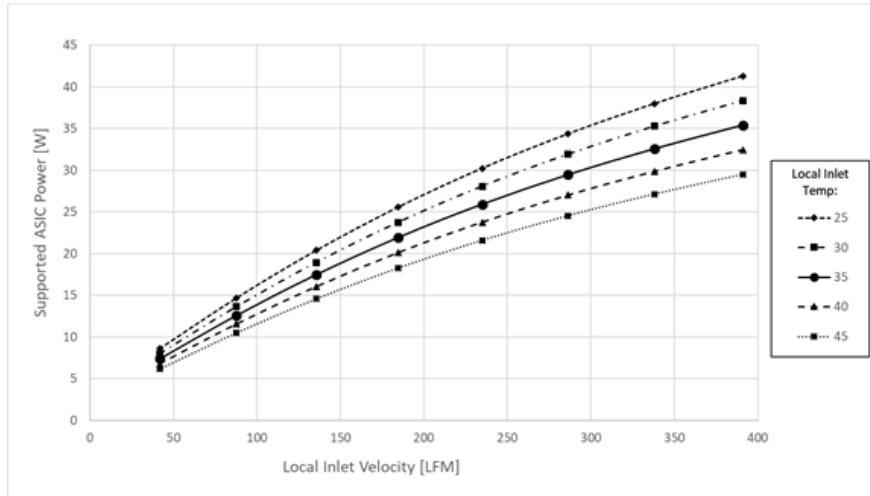


6.2.4 SFF Card ASIC Cooling – Cold Aisle

Compared to the Hot Aisle cooling configuration, there are several key differences for Cold Aisle ASIC cooling. With Cold Aisle cooling the airflow is pulled from the I/O connector side of the card. The I/O connectors and faceplate venting may affect the airflow through the ASIC heatsink. The I/O connectors may also preheat the airflow by some amount. In a Cold Aisle cooling configuration, other parallel airflow paths may result in less airflow passing over and through the OCP NIC 3.0 card compared to the Hot Aisle.

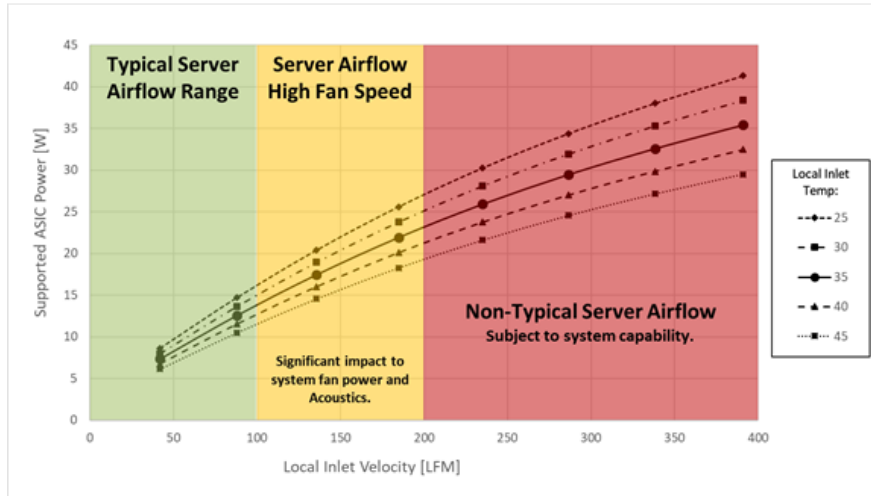
The ASIC cooling analysis for the SFF Card in the Cold Aisle configuration was conducted utilizing the same geometry and boundary conditions described in Figure 130 and ~~Table 66~~ ~~Table 65~~ with airflow moving from I/O connector to ASIC (opposite to the Hot Aisle analysis). Figure 136 below shows the results of this analysis for the Cold Aisle cooling configuration. Each curve in Figure 136 represents a different system inlet air temperature from 25 °C to 45 °C.

Figure 136: ASIC Supportable Power for Cold Aisle Cooling – SFF Card



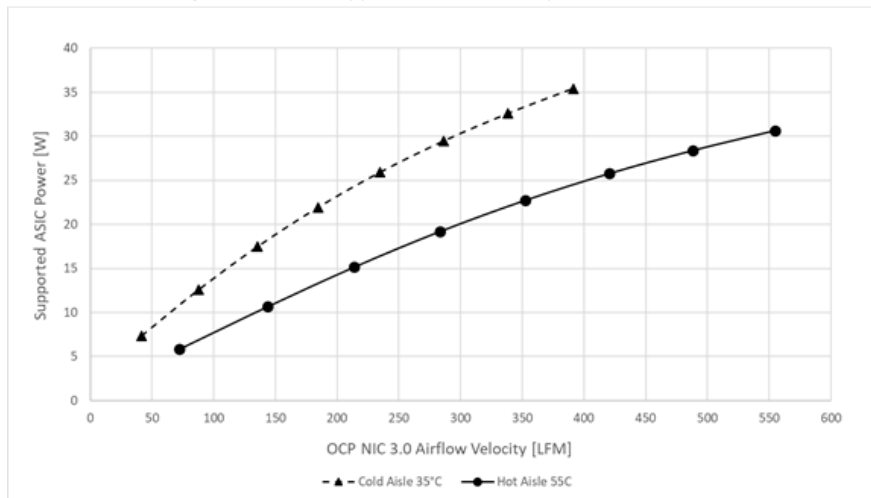
Similar to Figure 131 for Hot Aisle cooling, Figure 137 below shows the ASIC supportable power curves with an overlay of three Cold Aisle server airflow capability ranges. Designers must ensure that their thermal solutions and resulting card airflow requirements fall within the range of supportable Cold Aisle system airflow velocity. Cards that are under-designed (e.g., require airflow greater than the system capability) will have thermal issues when deployed into the server system. Similar to the Hot Aisle cases, cooling of the optical transceivers need to be taken into consideration even though they are not preheated by the ASIC in the Cold Aisle case. OCP NIC 3.0 designers must consider all power modes in the design process – including Main Power Mode and Aux Power Mode. For both modes, the card designer must provide the airflow requirements in the OEM FRU record as described in Section 4.10.3. Card designers are advised to work closely with system vendors to ensure they target the appropriate airflow and temperature boundary conditions for both Hot and Cold Aisle cooling.

Figure 137: Server System Airflow Capability – SFF Cold Aisle Cooling



A comparison of Hot Aisle (55 °C) and Cold Aisle (35 °C) SFF ASIC cooling capability curves is shown below in Figure 138. The comparison shows the Hot Aisle ASIC cooling capability at 12 W at 150 LFM while the cold Aisle cooling capability shows support for 19 W at 150 LFM. In general, based on the reference geometry, the Cold Aisle cooling configuration allows for higher supported ASIC power at lower velocities due primarily to the lower inlet temperatures local to the OCP NIC 3.0 card when in the Cold Aisle cooling configuration.

Figure 138: ASIC Supportable Power Comparison – SFF Card



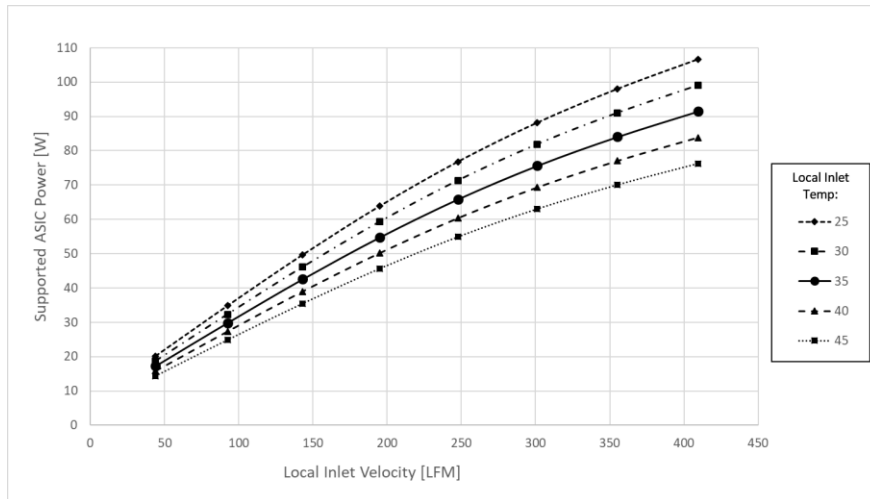
6.2.5 TSFF Card ASIC Cooling – Cold Aisle (TBD)

This section is a work in progress.

6.2.6 LFF Card ASIC Cooling – Cold Aisle

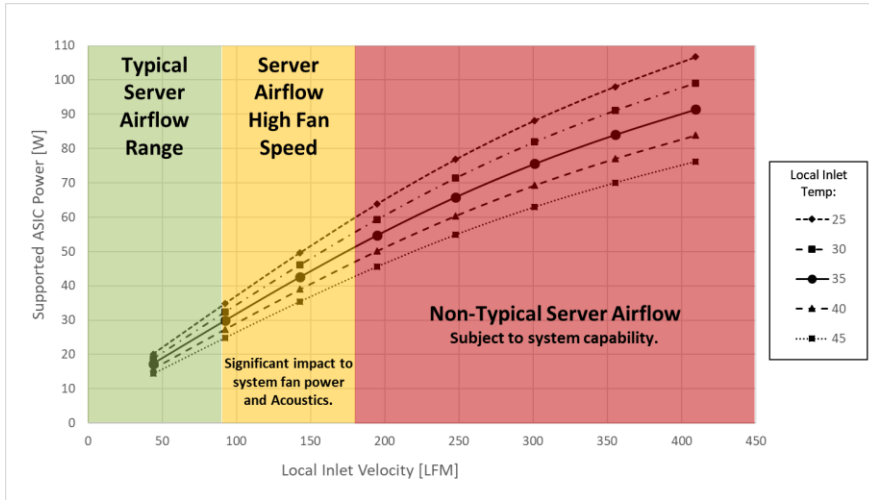
The ASIC cooling analysis for the LFF card in Cold Aisle configuration was conducted utilizing the same geometry and boundary conditions described in Figure 134 and Table 67 Table 66 with airflow moving from I/O connector to ASIC (opposite to the Hot Aisle analysis). Figure 139 below shows the results of this analysis for the Cold Aisle cooling configuration. Each curve in Figure 139 represents a different system inlet air temperature from 25 °C to 45 °C.

Figure 139: ASIC Supportable Power for Cold Aisle Cooling – LFF Card



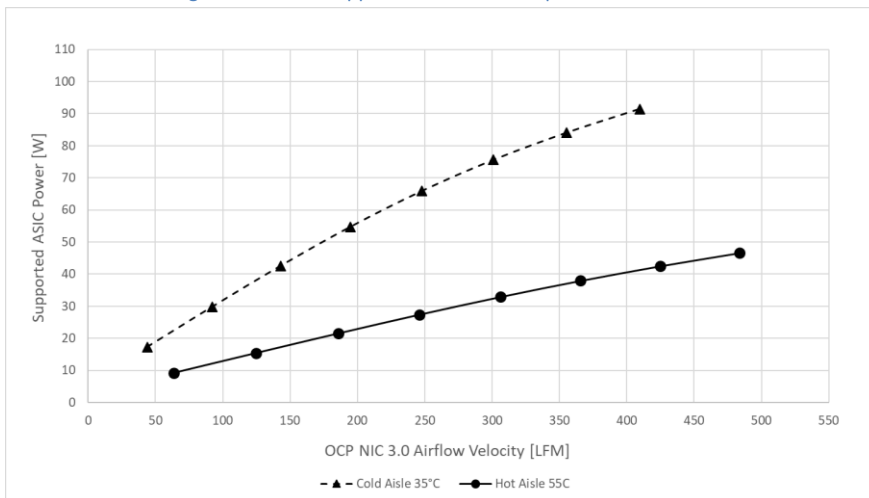
Similar to Figure 137 for LFF Hot Aisle cooling, Figure 140 below shows the LFF ASIC supportable power curves with an overlay of three Cold Aisle server airflow capability ranges. Designers must ensure that their thermal solutions and resulting card airflow requirements fall within the range of supportable Cold Aisle system airflow velocity. Cards that are under-designed (e.g., require airflow greater than the system capability) will have thermal issues when deployed into the server system. Similar to the Hot Aisle cases, cooling of the optical transceivers need to be taken into consideration even though they are not preheated by the ASIC in the Cold Aisle case. OCP NIC 3.0 designers must consider all power modes in the design process – including Main Power Mode and Aux Power Mode. For both modes, the card designer must provide the airflow requirements in the OEM FRU record as described in Section 4.10.3. Card designers are advised to work closely with system vendors to ensure they target the appropriate airflow and temperature boundary conditions for both Hot and Cold Aisle cooling.

Figure 140: Server System Airflow Capability – LFF Cold Aisle Cooling



A comparison of Hot Aisle (55 °C) and Cold Aisle (35 °C) LFF ASIC cooling capability curves is shown below in Figure 141. The comparison shows the Hot Aisle ASIC cooling capability at 19 W at 150 LFM while the cold Aisle cooling capability shows support for 42 W at 150 LFM. In general, based on the reference geometry, the Cold Aisle cooling configuration allows for higher supported ASIC power at lower velocities due primarily to the lower inlet temperatures local to the OCP NIC 3.0 card when in the Cold Aisle cooling configuration.

Figure 141: ASIC Supportable Power Comparison – LFF Card



6.3 Thermal Simulation (CFD) Modeling

CFD models of the SFF, TSFF and LFF cards developed for the analysis detailed in Section 6.2 are available for download on the OCP NIC 3.0 Wiki: <http://www.opencompute.org/wiki/Server/Mezz>

Commented [TN1]: Confirm this is going to be available!

The thermal models available on the wiki site are in Icepak format. CAD step file exports from those models are also available to aid in re-creation of the models in other CFD software tools. Note that the geometry utilized in the CFD models is based on the OCP NIC 3.0 thermal test fixture detailed in Section 6.4.

Thermal simulation of OCP NIC 3.0 cards using the provided CFD models is recommended. Ideally, vendors developing OCP NIC 3.0 cards would perform CFD analysis to validate card thermal solutions using the provided CFD models prior to building card prototypes. Once prototypes are available, vendors would then perform thermal testing on the functional cards using the thermal test fixtures detailed in Section 6.4.

6.4 Thermal Test Fixture

Thermal test fixtures have been developed for SFF, TSFF and LFF OCP NIC 3.0 cards. The test fixtures are intended to provide a common thermal test platform for card vendors, server vendors, and other industry groups planning to develop or utilize the OCP NIC 3.0 card form factors. Details of the thermal test fixtures are as follows:

- Sheet metal side walls, base, faceplate, and top cover
- Thumbscrew top cover access
- PCB sandwiched between base and side walls
- Intended for attachment to wind tunnel or flow bench such as those available at: <http://www.fantester.com/>
- Allows for thermal testing of functional OCP NIC 3.0 cards in a metered airflow environment
- Input power from external power supplies allows for OCP NIC 3.0 card power measurement
- SFF, TSFF fixture power connections for 3.3 V, GND, GND, 12 V
- LFF fixture power connections for 3.3 V, GND, GND, GND, 12 V, 12 V
- RJ45 connector for NC-SI pass-through
- USB Type-C connector for microprocessor connectivity and Micro-B to the USB pins on the primary connector
- Functions as a remote PCIe extension with intent to position host server under the fixture for connection to system PCIe slot
- Single x16 connection to server host on bottom side of the fixture PCB (SFF, TSFF)
- Dual x16 connection to server host on bottom side of the fixture PCB (LFF)
- Predefined locations for fixture airflow/temperature sensors on fixture PCB silkscreen. Quantity 3x per SFF/TSFF board and quantity 4x for LFF – see [Figure 147](#)

- Candlestick style sensors are available at:
<https://www.qats.com/Products/Instruments/Temperature-and-Velocity-Measurement/Sensors/Candlestick-Sensor>
- Candlestick sensors must be procured separately, not integrated with fixture PCB
- Low profile PCIe card serves as blockage above OCP NIC 3.0 card to mimic system geometry and prevent airflow bypass
- LFF fixture uses a sheet metal obstruction built into the top cover

CAD Files for the current revision of the test fixture are available for download on the OCP NIC 3.0 Wiki:
<http://www.opencompute.org/wiki/Server/Mezz>.

6.4.1 Test Fixture for SFF Card

Images of the SFF thermal test fixture are shown in Figure 142 and Figure 143. The SFF fixture PCB is shown in Figure 144. Note the three candlestick sensor locations directly next to the OCP NIC 3.0 connectors.

Figure 142: SFF Thermal Test Fixture Preliminary Design

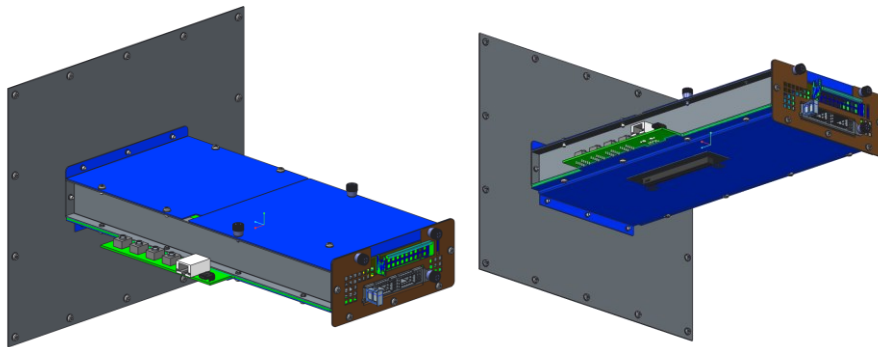


Figure 143: SFF Thermal Test Fixture Preliminary Design – Cover Removed

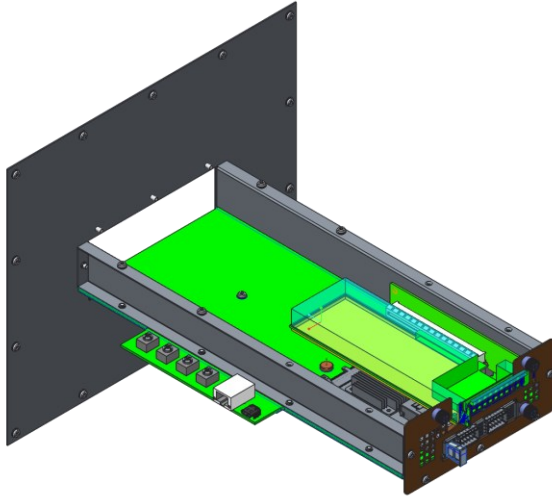
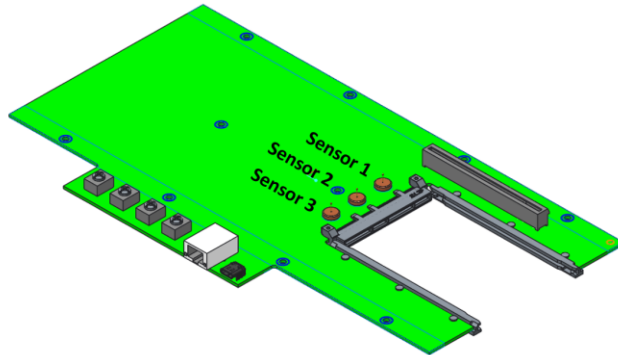


Figure 144: SFF Card Thermal Test Fixture PCB



6.4.2 Test Fixture for TSFF Card (TBD)

This section is a work in progress.

6.4.3 Test Fixture for LFF Card

Images of the LFF thermal test fixture are shown in Figure 145 and Figure 146. The LFF fixture PCB is shown in ~~Figure 147~~ Figure 147. Note the three candlestick sensor locations directly next to the OCP NIC 3.0 connectors.

Figure 145: LFF Card Thermal Test Fixture Design

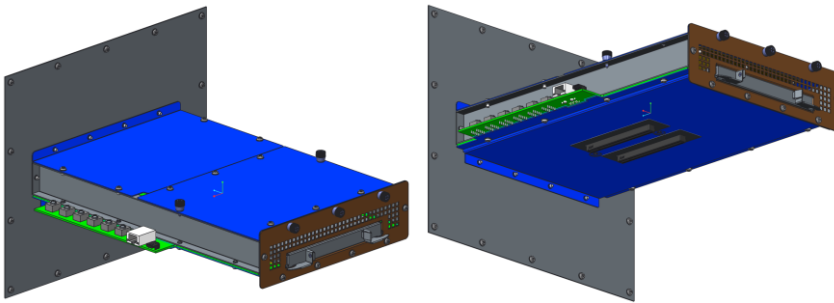


Figure 146: LFF Card Thermal Test Fixture Design – Cover Removed

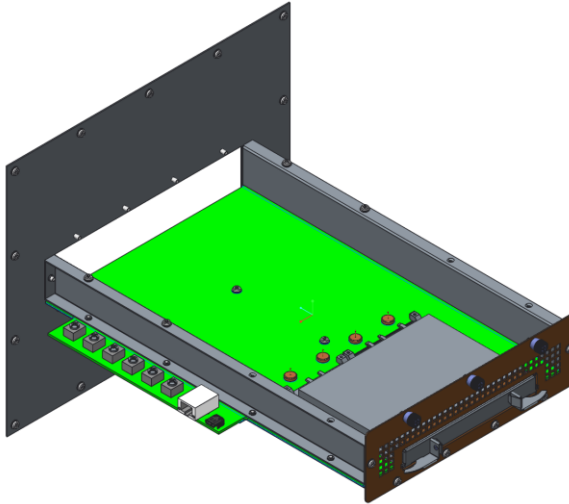
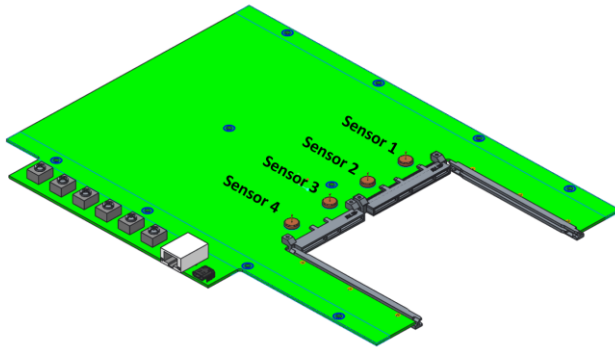


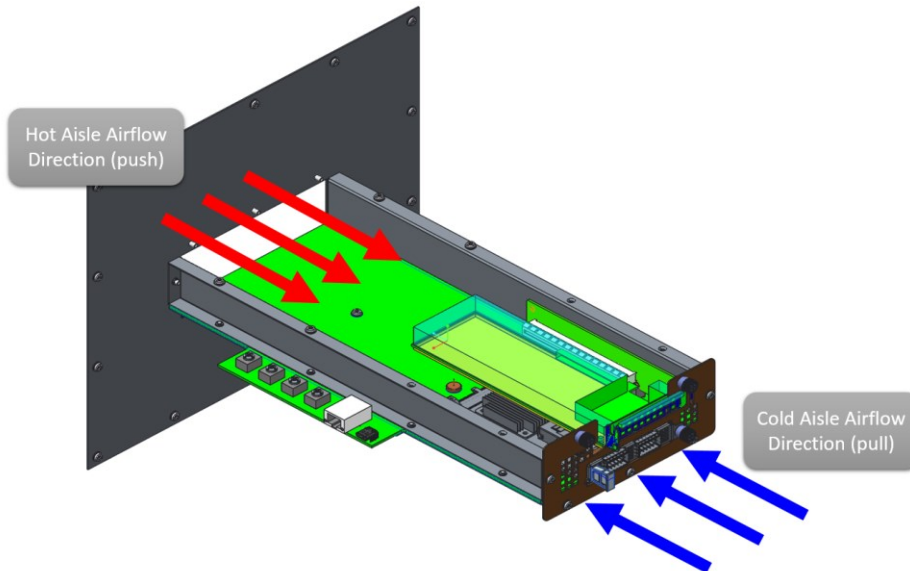
Figure 147: LFF Card Thermal Test Fixture PCB



6.4.4 Test Fixture Airflow Direction

When utilizing the OCP NIC 3.0 thermal test fixture, the wind tunnel or flow bench must be configured to push airflow for Hot Aisle cooling or to pull airflow for Cold Aisle cooling as shown in Figure 148.

Figure 148: Thermal Test Fixture Airflow Direction



6.4.5 Thermal Test Fixture Candlestick Sensors

As noted previously, candlestick sensor locations are included on the fixture PCB silkscreen. These candlestick sensors provide point measurements for both airflow velocity (LFM) and air temperature. The airflow at the inlet to the OCP NIC 3.0 will differ from the fixture mean velocity due to the obstructions above the OCP NIC 3.0 cards within the fixture. Thus, the fixture flow rate and cross-sectional area should not be used to determine the local velocity at the OCP NIC 3.0 card. Instead, the candlestick velocity/temperature sensors should be utilized to directly measure the local inlet velocity to the cards for hot aisle cooling.

When measuring the cold aisle inlet temperature, a separate thermocouple in front of the faceplate should be used instead of using the candlestick sensors on-board the thermal test fixture. The thermocouple should be centered on the faceplate area and placed 25 ± 2 mm away from the surface. This method is more representative of the cold aisle inlet temperature compared to using the on-board thermal-test fixture candlestick sensors which may be affected by the heat dissipated from the ASIC.

Figure 149: External Thermocouple Placement for Cold Aisle Inlet Temperature Measurement

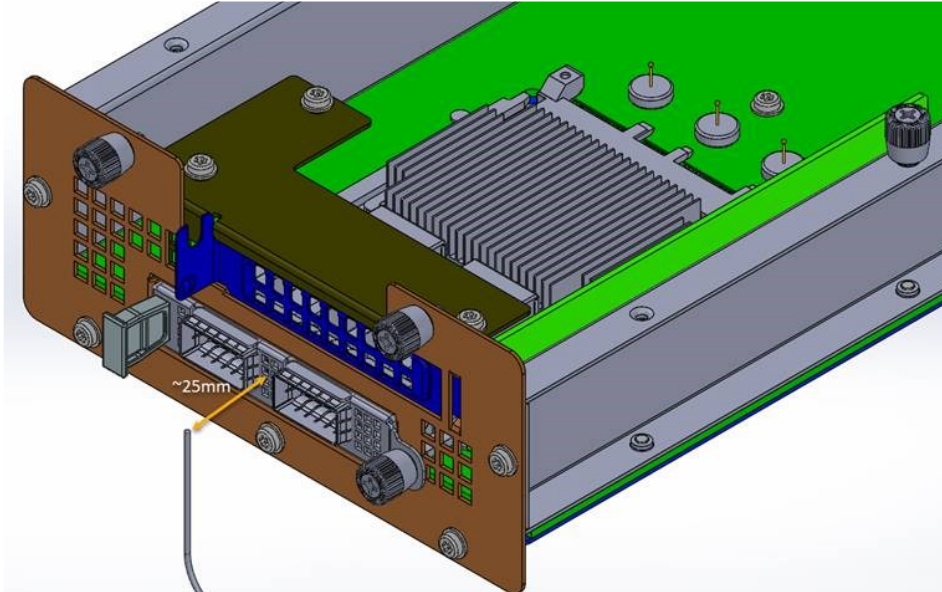


Figure 150, Figure 151 and Figure 152 ~~below~~ show the air velocity at each sensor location vs. the total fixture flow rate in CFM. The curves shown in these figures are based on the data collected from the CFD models discussed in Section 6.3. Note the error between the velocities obtained from the sensor locations vs. the velocity based on the duct cross-sectional area.

Figure 150: SFF Fixture, Hot Aisle Flow – Candlestick Air Velocity vs. Volume Flow

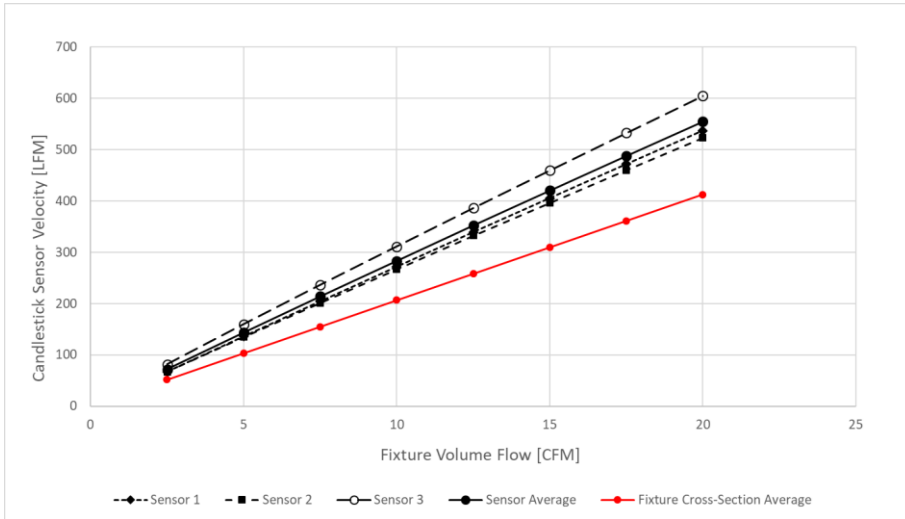
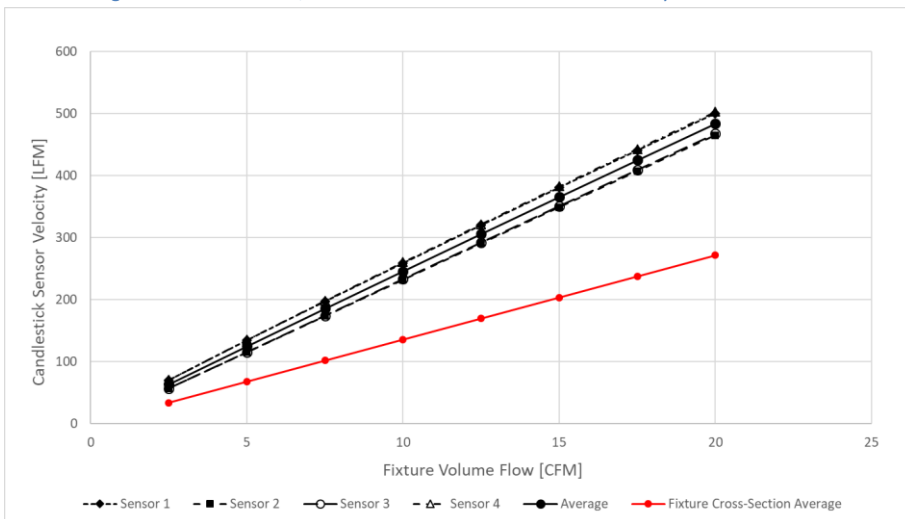


Figure 151: TSFF Fixture, Hot Aisle Flow – Candlestick Air Velocity vs. Volume Flow (TBD)

This section is a work in progress

Figure 152: LFF Fixture, Hot Aisle Flow – Candlestick Air Velocity vs. Volume Flow



6.5 Card Sensor Requirements

See Sections 4.4 to 4.6 for information relating to temperature sensor and reporting requirements.

6.6 Card Cooling Tiers

Section 4.10.3 defines several FRU fields that may be read by the baseboard management controller (BMC). Two of these fields provide the Hot Aisle and Cold Aisle Card Cooling Tiers that may be used for open loop fan speed control. The Card Cooling Tiers relate the card local inlet temperature to the required local inlet velocity in linear feet per minute (LFM) which allows the system to set fan speeds according to the cooling requirements of the card.

The Card Cooling Tier FRU fields are particularly useful for systems that do not implement temperature sensor monitoring (open loop fan control). The FRU fields may also be used as a backup for systems that implement fan control based on temperature sensor monitoring (closed loop control).

Card Cooling Tiers for Hot and Cold Aisle Cooling configurations are defined in [Table 68](#)~~Table 67~~. The values in the table are listed with units shown in LFM. Future releases of this specification will provide more detail to the Card Cooling Tier curve definition.

Table 68: Card Cooling Tier Definitions (LFM)

| OCP NIC 3.0 Local Inlet Temperature [°C] | Target Operating Region | | | | Server Airflow High Fan Speed | | Non-Typical Server Airflow - Subject to System Capability | | | | | |
|--|-------------------------|--------|--------|--------|-------------------------------|--------|---|--------|--------|---------|---------|---------|
| | Tier 1 | Tier 2 | Tier 3 | Tier 4 | Tier 5 | Tier 6 | Tier 7 | Tier 8 | Tier 9 | Tier 10 | Tier 11 | Tier 12 |
| 5 | 0 | 100 | 100 | 100 | 100 | 100 | 110 | 150 | 200 | 255 | 320 | 395 |
| 10 | 0 | 100 | 100 | 100 | 100 | 100 | 118 | 159 | 211 | 271 | 341 | 426 |
| 15 | 0 | 100 | 100 | 100 | 100 | 105 | 128 | 170 | 226 | 291 | 366 | 461 |
| 20 | 0 | 100 | 100 | 100 | 100 | 109 | 137 | 181 | 241 | 311 | 391 | 496 |
| 25 | 0 | 100 | 100 | 100 | 100 | 114 | 147 | 198 | 260 | 337 | 420 | 532 |
| 30 | 0 | 100 | 100 | 100 | 110 | 130 | 167 | 215 | 283 | 363 | 453 | 578 |
| 35 | 0 | 100 | 100 | 100 | 120 | 146 | 186 | 236 | 308 | 393 | 488 | 623 |
| 40 | 0 | 100 | 100 | 111 | 139 | 172 | 212 | 260 | 335 | 430 | 525 | 673 |
| 45 | 0 | 100 | 100 | 125 | 161 | 200 | 242 | 290 | 370 | 472 | 575 | 736 |
| 50 | 0 | 100 | 110 | 155 | 198 | 243 | 288 | 335 | 425 | 530 | 645 | 838 |
| 55 | 0 | 100 | 150 | 200 | 250 | 300 | 350 | 400 | 500 | 625 | 750 | 1000 |
| 60 | 0 | 150 | 200 | 255 | 315 | 380 | 450 | 525 | 643 | 796 | 936 | 1241 |
| 65 | 0 | 200 | 260 | 330 | 410 | 500 | 600 | 710 | 850 | 1025 | 1200 | 1550 |

A graphical view of the Card Cooling Tiers is shown in Figure 153. The Tiers range from 0 LFM to as high as 1000 LFM at 55 °C local inlet temperature. It is important to understand that the cooling tiers extend well beyond the airflow range of most server systems. As noted in Section 6.2, card designers must consider the airflow capability of the systems that the cards are to be used in when designing the card thermal solution and component placement. Figure 154 and Figure 155 below show the range of typical system capability for Hot Aisle and Cold Aisle configurations. Cards designed to these typical ranges (Tiers 1-6) will be low risk to support in most if not all server systems. Alternatively, cards that require Tier 7 or greater may still work in many server systems but may require extra validation testing, specific system slot location requirements, and potentially ambient temperature and hardware restrictions.

Figure 153: Graphical View of Card Cooling Tiers

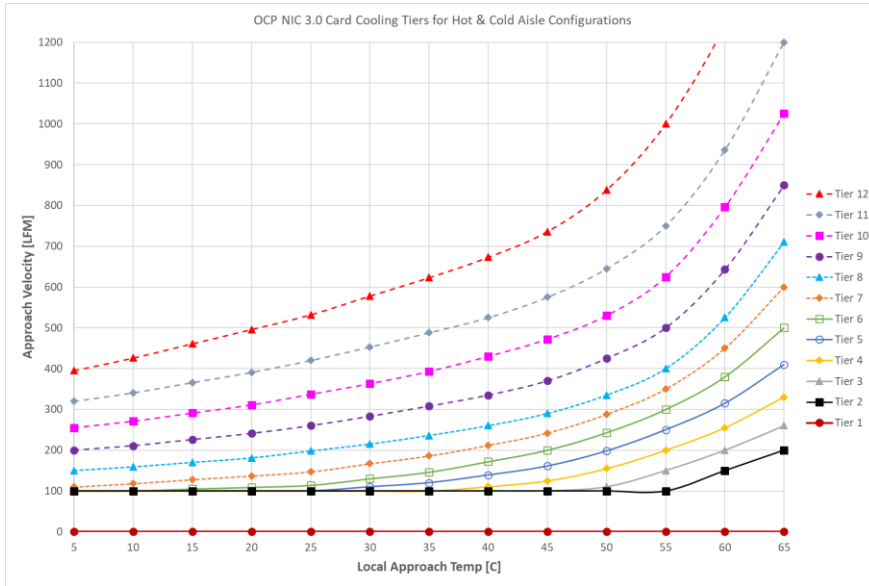


Figure 154: Typical Operating Range for Hot Aisle Configurations

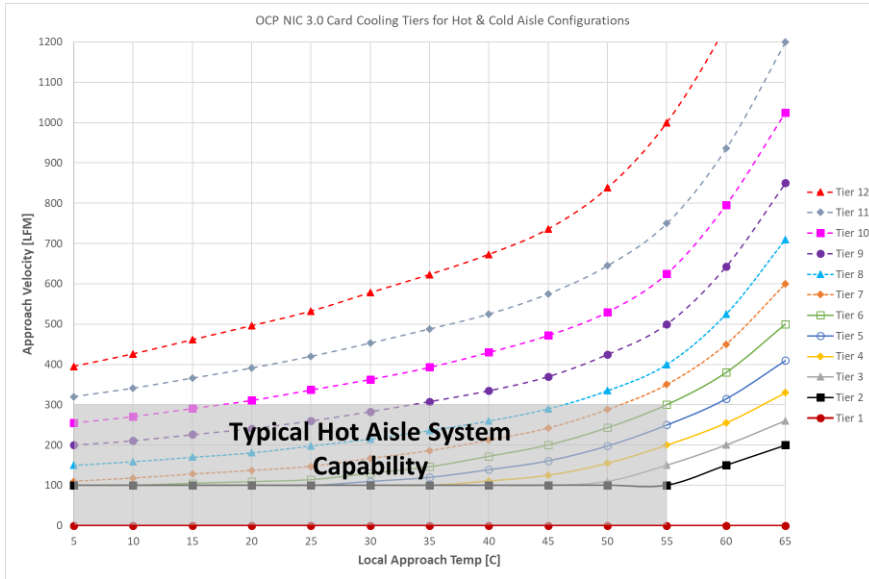
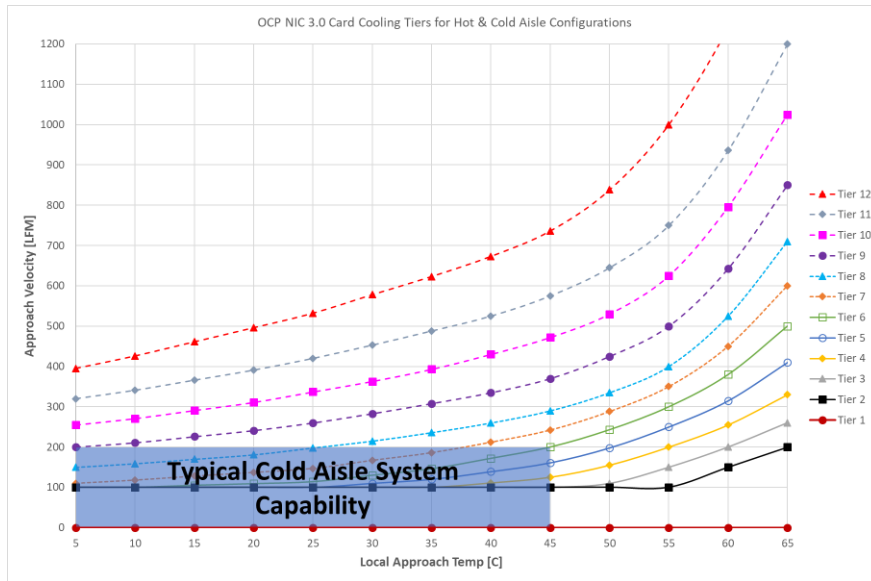


Figure 155: Typical Operating Range for Cold Aisle Configurations



6.7 Non-Operational Shock & Vibration Testing

OCP NIC 3.0 components are deployed in various environments. As such, all OCP NIC 3.0 cards shall be subjected to shock and vibration testing to ensure products do not sustain damage during normal operational or transportation conditions. While end customer deployments may require an additional final system level test, this section sets the minimum shock and vibration requirements for an OCP NIC 3.0 card that must also be considered.

Shock and vibration testing shall be done in accordance with the procedures listed below. The tests shall be conducted using a vertical shock table. The OCP NIC 3.0 card shall be secured in the standard test fixture as described in Section 6.7.1.

6.7.1 Shock & Vibe Test Fixture

The OCP NIC 3.0 shock and vibe fixture supports simultaneous testing of up to four SFF/TSFF, or four LFF cards. The SFF/TSFF fixture accepts card configurations that utilize the pull tab, ejector lever and internal lock mechanisms. The LFF fixture only accepts the single latch faceplate.

The fixture is comprised of a universal baseplate that allows for attaching SFF/TSFF or LFF rail guides and simulated chassis faceplates. The baseplate includes an industry standard vibration table hole pattern for securing the UUT for test. Figure 156 and Figure 157 show the SFF/TSFF and LFF fixtures, respectively.

CAD files for the current revision of the test fixture are available for download from the OCP NIC 3.0 wiki: <http://www.opencompute.org/wiki/Server/Mezz>.

Figure 156: SFF/TSFF Shock and Vibe Fixture

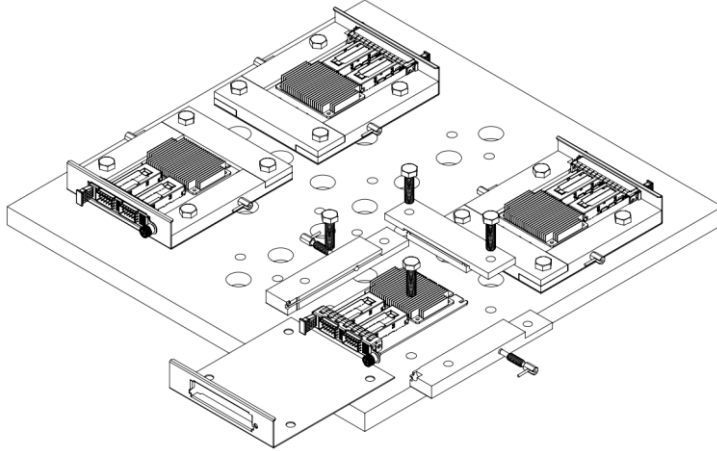
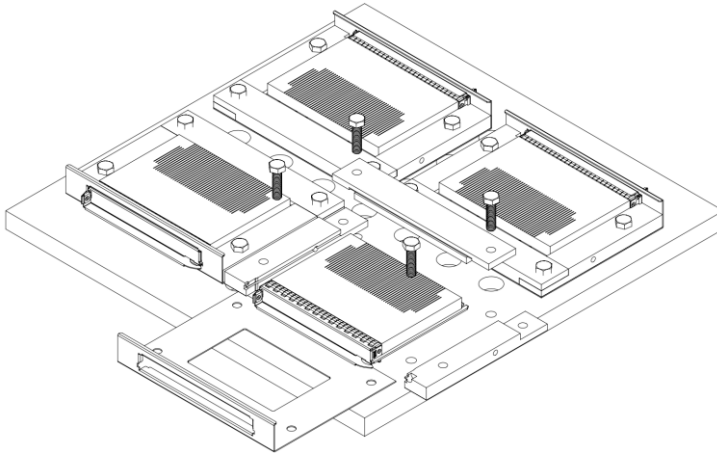


Figure 157: LFF Shock and Vibe Fixture



6.7.2 Test Procedure

The following procedures shall be followed for the shock and vibration testing:

- A minimum sample size of three OCP NIC 3.0 cards shall be subjected to shock and vibration. Each sample shall be subjected to testing in the order listed below.
- All samples shall be verified for functionality prior to test.

- The OCP NIC 3.0 card shall be fixtured to simulate how the card will be mounted within a system. For example, the OCP NIC 3.0 card may be fixtured in the horizontal plane with the primary component side facing up for certain chassis configurations.
- The fixture shall be tested on all 6 sides. Each side shall be clearly labeled as 1-6 for test identification purposes. Testing shall be performed in the vertical axis only. The fixture shall be rotated until all six sides have been tested as the product may be dropped from any orientation during handling. Testing shall not be conducted on a three axis slip table.
- Non-operational vibration testing is performed at 1.88 G_{RMS} for a duration of 15 minutes per side per ~~Table 69~~ [Table 68](#).

Table 69: Random Vibration Testing 1.88 G_{RMS} Profile

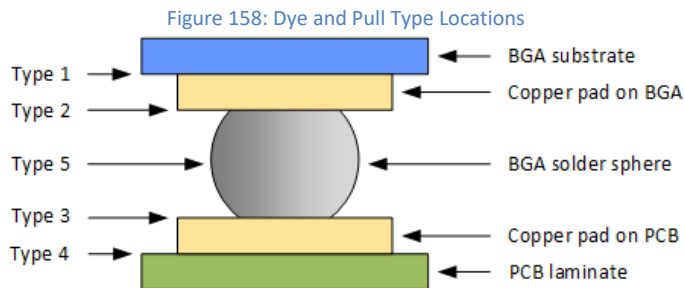
| Frequency (Hz) | G ² /Hz |
|----------------|--------------------|
| 10 | 0.13 |
| 20 | 0.13 |
| 70 | 0.004 |
| 130 | 0.004 |
| 165 | 0.0018 |
| 500 | 0.0018 |

- Non-operational half-sine shock test at 71 G ±10% with a 2 ms duration per surface.
- Non-operational trapezoidal wave shock test at 50 G ±10% at a rate of 170 inches/sec per surface.
- All cards shall be checked for proper operation after the shock and vibration tests have been conducted. All three samples must be in full operating order to consider the product as a pass.

6.8 Dye and Pull Test Method

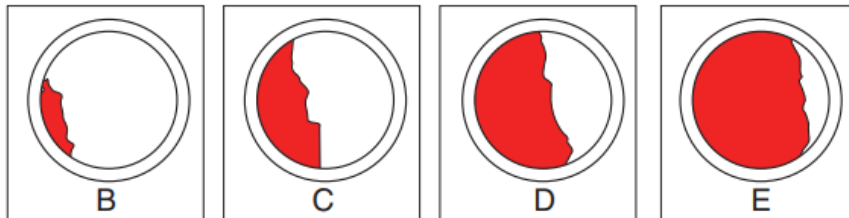
All Dye and Pull test methods shall be implemented per the IPC-TM-650 method 2.4.53 (Dye and Pull Test Method – formerly known as Dye and Pry). The Dye and Pull test uses a colored dye penetrant to visually indicate cracked solder joints on BGA devices. The test shall only be conducted after the Shock and Vibration testing has been conducted on the test samples. The Dye and Pull Test Method is a destructive test.

- A minimum sample size of three OCP NIC 3.0 cards shall be subjected to the Dye and Pull Test Method.
- All samples shall be first subjected to the Shock and Vibration testing outlined in Section 6.7.
- All samples shall be subjected to the preparation and test procedures of IPC-TM-650 method 2.4.53.
- Following the pull-test operation, the board sample shall be examined for dye indication at the target BGA area. Separation locations are categorized in to the following five areas:
 - Type 1 – Separation between the BGA copper pad and the BGA substrate.
 - Type 2 – Separation between the BGA copper pad and the BGA solder sphere.
 - Type 3 – Separation between the BGA solder sphere and the copper pad on the PCB.
 - Type 4 – Separation between the copper pad on the PCB and the PCB laminate.
 - Type 5 – Separation of the BGA solder sphere.



- Samples shall be subjected to the following failure criteria:
 - Dye coverage of >50% (“D” and “E” in Figure 159) of any Type 2 or Type 3 BGA cracks are present in the test sample.
 - One or more Type 1 or Type 4 BGA cracks are present in the test sample.

Figure 159: Dye Coverage Percentage



The following exceptions are allowed:

- For “via-in-pad” designs, dye is allowed on the laminate surface (under the pad), as long as the dye has not entered the inner-via laminate area, or is found on the separated via-barrel wall.
- Allowances for dye indications on mechanical (non-electrical) BGA corner locations or multiple use locations (grounds, powers) may be determined by the appropriate Engineering Team.

6.9 Gold Finger Plating Requirements

This section defines the minimum plating/quality requirements for the OCP NIC 3.0 gold fingers.

6.9.1 Host Side Gold Finger Plating Requirements

Per Section 6.4 (Environmental Requirements) of the PCIe CEM specification, the minimum host side gold finger plating is 30 microinches of gold over 50 microinches of nickel. OCP NIC 3.0 card vendors shall individually evaluate the minimum plating required.

The recommendation for OCP NIC 3.0 is to 30 microinches of gold over 150 microinches of nickel.

6.9.2 Line Side Gold Finger Durability Requirements

The line side connectors must be designed to support a minimum of 250 error free insertion cycles. In order to accomplish this, it is required that the minimum contact plating be as follows:

- SFP and QSFP connectors: 30 microinches of gold over 50 microinches of nickel
- RJ45 connectors have a minimum of 50 microinches of gold over 50 microinches of nickel

7 Regulatory

7.1 Required Compliance

An OCP NIC 3.0 card shall meet the following Environmental, EMC and safety requirements.

Note: Emissions and immunity tests in Section 7.1.4 are to be completed at the system level. The OCP NIC 3.0 vendors should work with the system vendors to achieve the applicable requirements listed in this section.

7.1.1 Required Environmental Compliance

- China RoHS Directive
- **EU RoHS 2 Directive (2011/65/EU)** aims to reduce the environmental impact of electronic and electrical equipment (EEE) by restricting the use of certain hazardous materials. The substances banned under RoHS are lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls, polybrominated diphenyl ether, and four phthalates.
- **EU REACH Regulation (EC) No 1907/2006** addresses the production and use of chemical substances and their potential impact on human health and the environment.
- **EU Waste Electrical and Electronic Equipment (“WEEE”) Directive (2012/19/EU)** – mandates the treatment, recovery and recycling of EEE.
- **The Persistent Organic Pollutants Regulation (EC) No. 850/2004** bans production, placing on the market and use of certain persistent organic pollutants.
- **The California Safe Drinking Water and Toxic Enforcement Act of 1986 (“Proposition 65”)** sets forth a list of regulated chemicals that require warnings in the State of California.
- **The Packaging and Packaging Waste Directive 94/62/EC** limits certain hazardous substances in the packaging materials
- **Batteries Directive 2006/66/EC** regulates the manufacture and disposal of all batteries and accumulators, including those included in appliances.

7.1.2 Required EMC Compliance

- Radiated and Conducted Emissions requirements are based on deployed geographical locations. Refer to [Table 70](#) ~~Table 69~~ for details.

Table 70: FCC Class A Radiated and Conducted Emissions Requirements Based on Geographical Location

| Targeted Geography | Applicable Specifications |
|--------------------|--|
| USA | FCC, 47 CFR Part 15, Class A digital device (USA) |
| Canada | ICES-003, class A (CAN) |
| EU | EN 55032: 2015+AC:2016 Class A Radiated and Conducted Emissions requirements for European Union EN 55035: 2017 Immunity requirements for the European Union (EU) EN 55024: 2010+A1:2015 Immunity requirements for European Union (EU) may alternatively be reported. |

| Targeted Geography | Applicable Specifications |
|-----------------------|---|
| | Note: EN55024 is scheduled to be superseded by EN55035. OCP NIC 3.0 implementors are encouraged to test to EN55035 to avoid recertifying their product when EN55024 is withdrawn. |
| Australia/New Zealand | AS/NZS CISPR 32:2015 Class A CISPR 32:2015 for Radiated and Conducted Emissions requirements |
| Japan | VCCI 32-1 Class A Radiated and Conducted Emissions requirements |
| Korea | KN32 – Radiated and Conducted Emissions KN35- Immunity |
| Taiwan | BSMI CNS13438: 2006 (complete) Class A Radiated and Conducted Emissions requirements |

- **CE** – Equipment must pass the CE specification
- All technical requirements covered under **EMC Directive (2014/30/EU)**

7.1.3 Required Product Safety Compliance

- Safety – requirements are listed in [Table 71](#)~~Table 70~~.

Table 71: Safety Requirements

| Targeted Category | Applicable Specifications |
|-------------------|--|
| Safety | UL 62368-1 and CAN/CSA C22.2 No. 62368-1-14, 3 rd Edition. Audio/video, information and communication technology equipment Part 1: Safety requirements, dated 2019/12/13. |

7.1.4 Required Immunity (ESD) Compliance

The OCP NIC 3.0 card shall meet or exceed the following ESD immunity requirements listed in [Table 72](#)~~Table 71~~.

Table 72: Immunity (ESD) Requirements

| Targeted Category | Applicable Specifications |
|-------------------------|---|
| Immunity (ESD) | EN 55035 2017, and IEC 61000-4-2 2008 for ESD. EN 55024 may alternatively be reported. Required ±4 kV contact discharge and ±8 kV air discharge. Note: EN55024 is scheduled to be superseded by EN55035. OCP NIC 3.0 implementors are encouraged to test to EN55035 to avoid recertifying their product when EN55024 is withdrawn. |
| NEBS Level 3 (optional) | Optionally test devices to NEBS Level 3 – Required ±8 kV contact discharge and ±15 kV air discharge with interruptions not greater than 2 seconds. The device shall self-recover without operator intervention. Note: NEBS compliance is part of the system level testing. The OCP NIC 3.0 specification is providing a baseline minimum recommendation for ESD immunity. |

7.2 Recommended Compliance

All OCP NIC 3.0 cards are required to meet the requirements specified in Section 7.1. Card vendors should also consider meeting the requirements below.

7.2.1 Recommended Environmental Compliance

- **Halogen Free:** IEC 61249-2-21 Definition of halogen free: 900ppm for Bromine or Chlorine, or 1500ppm combined total halogens.
- **Arsenic:** 1000 ppm (or 0.1% by weight)
- **Emerging: US Conflict Minerals law: section 1502 of the Dodd-Frank Act** requires companies using tin, tantalum, tungsten, and gold (“3TG”) in their products to verify and disclose the mineral source. While this does not apply to products that are used to provide services, such as Infrastructure hardware products, the OCP NIC Subgroup is considering voluntarily reporting of this information.

7.2.2 Recommended EMC Compliance

- FCC, 47 CFR Part 15, Subpart B Class A digital device (USA) with 10dB margin. Refer to the baseline requirements shown in Section 7.1.2 for details.

8 Revision History

8.1 Document Revision History

| Author | Description | Revision | Date |
|----------------------|---|----------|------------|
| OCP NIC 3.0 Subgroup | Initial public review. | 0.70 | 01/25/2018 |
| OCP NIC 3.0 Subgroup | <ul style="list-style-type: none"> - Implemented comments from 0.70 review. - LED implementation updated. - Gold finger lengths updated. All pins are full length except for PCIe TX/RX, REFCLKS and PRSNT pins. | 0.71 | 02/06/2018 |
| OCP NIC 3.0 Subgroup | - Updates to Section 4.x per the working group session. | 0.72 | 02/21/2018 |
| OCP NIC 3.0 Subgroup | <ul style="list-style-type: none"> - Change NC-SI over RBT RXD/TXD pins to a pull-up instead of a pull down. - Update power sequencing diagram. REFCLK is disabled before silicon transitions to Aux Power Mode. - Merge pinout sections 3.4 and 3.5 together for structural clarity. - Add text to gate WAKE# signal on AUX_PWR_GOOD (internal) assertion; updated diagrams with WAKE# signals to reflect implementation. - Add initial signal integrity outline to document (WIP) - Add Initial draft of the Shock and Vibration, and Dye and Pull test requirements. - Rearrange Section 2 for structure; changed section name to Mechanical Card Form Factor - Move non-NIC use cases to Section 1.5. - Moved Port numbering and LED definitions to Section 3.8. - Add secondary side LED placement for 4x SFP and 2x QSFP implementations in Section 3.8. - Revised labeling section (Section 2.9). - Optimize the scan chain LED bit stream for dual port applications. - Add SLOT_ID[1]. Updated text and diagrams for mapping SLOT_ID[1:0] to Package ID[2:0] and FRU EEPROM A[2:0] fields. - Reduce ID Mode power consumption on +12V_EDGE | 0.73 | 05/01/2018 |
| OCP NIC 3.0 Subgroup | <ul style="list-style-type: none"> - Text clean up. All minor / generally agreed upon items within the OCP NIC 3.0 Workgroup have been accepted. - Clarify PCIe bifurcation is on a per-slot basis. Add 1x32 and 2x16 implementation examples for a Large Form Factor card. - Removed reference to a x24 PCIe width LFF card from Table 5 – OCP NIC 3.0 Card Definitions. - Move SLOT_ID[1] to OCP_A6 for immediate power on indication of the card physical location for RBT and FRU EEPROM addressing. Updated RBT addressing and Scan Chain definition to match. - Updated diagrams and text in Section 6.x based on feedback from the OCP NIC 3.0 Thermal Workgroup. - Updated diagrams and text in Section 2.0 based on feedback received from the OCP NIC 3.0 Mechanical Workgroup. | 0.74 | 06/04/2018 |
| OCP NIC 3.0 Subgroup | 0v80 public release | 0.80 | 06/04/2018 |
| OCP NIC 3.0 Subgroup | <p>0v81 public release. Changes are as follows:</p> <ul style="list-style-type: none"> - Section 1.3 – Update Figure 1 with latest thumbscrew design. - Section 2.4.2 – Mechanical corrections to BOM items 5, 6A/B, 8 & 11. - Section 3.4.3 – Add statement to isolate SMRST# if target device voltage is not powered from +3.3V_EDGE. | 0.81 | 07/06/2018 |

| Author | Description | Revision | Date |
|----------------------|--|----------|------------|
| | <ul style="list-style-type: none"> - Section 3.4.4 – Clarified the RBT_ARB_IN and RBT_ARB_OUT pin descriptions. - Section 3.4.4 – Clarified SLOT_ID[1:0] description and example diagrams; move SLOT_ID[1:0] isolation to NIC and use direct connection to FRU EEPROM. - Section 3.4.5 – DATA_IN bit PRSNTB[3:0] definition to optionally use pull up/down to match PRSNTB[3:0]# card edge connections. - Section 3.4.7 – Add USB 2.0 definition to the Primary Connector. - Section 3.4.8 – Add UART definition to the Secondary Connector. - Section 3.4.9 – Changed Miscellaneous pins to RFU[1:2] pins. - Section 3.8 – Clarified LED placement. - Section 3.9.x – Clarified ID-Aux and Aux-Main Power Mode transition requirements to prevent sampling health status pins until cards have fully entered into Aux and Main Power Modes to prevent false indication. - Section 3.11 – Updated hot swap consideration text to highlight available hot swap mechanisms. Actual hot swap design is outside the scope of this specification. - Section 4 – Update MCTP Type management description. - Section 4.9 – Clarified the FRU EEPROM is directly connected to the card edge. No isolation is used for the FRU EEPROM. | | |
| OCP NIC 3.0 Subgroup | <ul style="list-style-type: none"> - Minor editorial changes. - Changed names to “SFF” and “LFF” when referencing the two board form factors for uniformity. - Section 3.4.1 – Changed PERST[3:0]# to be asserted low until the platform is ready to bring cards out of reset. - Section 3.5.3 – Corrected typos in the PCIe Bifurcation Decoder (Table 31) for hosts that implement 4 x2 links on the first 8 lanes when using a 4 x4 OCP NIC 3.0 card. - Section 3.5.5.3 & 3.5.5.4 – Corrected the BIF[2:0] values in the diagrams. - Section 3.7 – Corrected typos in the PCIe Bifurcation result and REFCLK mapping (Table 38 and Table 41) for single host/quad host cases with PCIe on the first 8 lanes. This change was due to propagating corrections from Table 31 from Section 3.5.3. - Section 3.8.3 – Changed faceplate LED placement for 2xQSFP to primary side. - Section 4.10.2 – Added FRU field to identify the card manageability type. | 0.82 | 08/03/2018 |
| OCP NIC 3.0 Subgroup | <ul style="list-style-type: none"> - Section 5.3.4 – Removed subheadings for the PCIe test methodology. Replaced with reference text to the PCIe test specifications. | 0.83 | 08/29/2018 |
| OCP NIC 3.0 Subgroup | <ul style="list-style-type: none"> - Editorial changes. - Add appropriate trademarks per entity usage guidelines - Section 1.x – Reorganized section, added list of acronyms. - Section 1.5, 2.x – Mechanical updates from ME team. Updates to Vendor PN, pull tab/thumbscrew color. - Section 3.1.x – Add card edge gold finger Detail D and profile dimensions. - Section 3.1.1 – Change gold finger lengths to align with SFF-TA-1002 and SFF-TA-1009. All ground pins mate first; power, single ended and differential pairs mate second. - Section 3.4.1, Section 3.5.x – Updated for LFF and applications with 32 lanes of PCIe. Included TX/RX lane indices for lanes[16:31], REFCLK[4:5], PERST[4:5]# and PWRBRK1 on the Secondary Connector. - Section 3.4.2 – Clarified BIF[2:0]# assertion timing. | 0.84 | 11/13/2018 |

| Author | Description | Revision | Date |
|----------------------|---|----------|------------|
| | <ul style="list-style-type: none"> - Section 3.4.4 – Clarified RBT isolation state with respect to AUX_PWR_EN and NIC_PWR_GOOD assertion. - Section 3.4.5 – Clarified that the scan chain shift registers may also be implemented with a CPLD as long as the logic is equivalent. Clarified the FAN_ON_AUX bit. - Section 3.4.9 – Changed RFU[1:2] to RFU[3:4] for the Secondary Connector. - Section 3.7 – Removed bifurcation expansion tables. Redirected readers to the pinout/bifurcation spreadsheet on the OCP Mezz Wiki site instead. - Section 3.6 and Section 3.7 – Merged together as they both discuss PCIE REFCLK mapping. Add new diagrams depicting single, dual and quad host implementations with 1, 2, and 4 links. Diagrams show association of the link to the REFCLK and PERST signals. Update bifurcation table color codes to differentiate SFF (2C+ / 4C+) implementations from LFF implementations. - Section 3.11 – Add RBT_ISOLATE# to the power up/down sequencing diagrams. Changed BIF[2:0]# pins to ‘low’ state when AUX_PWR_EN is deasserted. Add timing value “T4” from DSP0222 to power up diagram and sequencing parameters table. Add T_{CYCLE_SFF} / T_{CYCLE_LFF} parameters to power down sequencing to prevent a pre-biased output condition when power cycling cards. - Section 4.4 – Clarified requirements for self-shutdown if the optional feature is implemented on the card. - Section 4.9 – Cleaned up SMBus 2.0 Address Map text. Add text to discourage the use of unsolicited SMBus messages including the optional ‘Notify ARP Master’ command. - Section 4.10.2 – Clarified FRU data format requirements per the IPMI Platform Management FRU Information Storage Definition. List minimum FRU content requirements. - Section 5.1.x – Clarified NC-SI over RBT physical routing and length matching requirements. - Section 7.1.4 – Corrected typo on NEBS air discharge value for ESD testing. Changed from 16 kV to 15 kV. | 0.85 | 11/20/2018 |
| OCP NIC 3.0 Subgroup | November release with all 0.84 subgroup changes | 0.85 | 11/20/2018 |
| OCP NIC 3.0 Subgroup | <ul style="list-style-type: none"> - December Hot fix release. Minor text corrections and clarifications. - Section 2.4.2 – Update faceplate and ejector handle drawing filenames - Sections 2.4.3, 2.4.4, and 2.7.x – Mechanical drawing updates. Fixed typos and updated critical dimension text. - Section 2.8.x – Mechanical drawing updates. Changed bottom of PCB datum from H to J. - Section 3.4.5 – Clarified the default scan chain pin states for TEMP_WARN_N, TEMP_CRIT_N and FAN_ON_AUX when temperature reporting is not required. - Section 3.4.7 – Clarified USB text on differential signaling voltage, termination voltage and V_{BUS} detection indication. Updated USB figures to include V_{BUS} and V_{BUS} detection inputs. - Section 3.8 – Updated power state machine. +12V_EDGE clarified as being “on, but limited up to the ID Mode budget.” This clarification aligns with the existing text. Added clarification notes to Table 37 for permissible +12V_EDGE current draw in the ID Mode and Aux Power Mode states. | 0.85b | 12/14/2018 |
| OCP NIC 3.0 Subgroup | <ul style="list-style-type: none"> - Section 1.2 – Change Cavium entity name to Marvell Semiconductor, Inc. - Section 1.3 – Added DSP0267 reference | 0.86 | 04/02/2019 |

| Author | Description | Revision | Date |
|----------------------|---|----------|------------|
| | <ul style="list-style-type: none"> - Sections 1.5, 2.1.x – All 3D renderings have been updated - Section 2.4.2 – Mechanical BOM updated. Added notes for Phillips + Torx screw heads. - Sections 2.4.3, 2.4.4, 2.5.x, 2.7.x, 2.8.2 – Mechanical 2D drawings updated. - Section 2.7 – Added insulator note regarding the use of 0.127 mm material for constrained regions; 4x 4mm diameter holes permitted for non-metallic mechanical retention pin cutouts - Section 3.1 – Gold finger figure updated to clarify dimension from center of pad. - Section 3.4.4 – Add note that RBT clock buffers are permitted so long as the card timing budget is not violated. Clarify permitted baseboard and OCP NIC 3.0 side pull up/pull down implementations on SLOT_ID[1:0]. - Sections 3.4.5, 3.7.2 – Scan Chain LED definition updated. Activity LED is OFF when “idle” - Section 3.4.7 – USB figures now shown as a BMC or Platform I/O hub connectivity instead of just the BMC. - Section 3.4.8 – UART figures now shown as a BMC or Platform I/O hub connectivity instead of just the BMC. - Section 3.6 – Clarify REFCLK/PERST mapping for LFF (Table 35). - Section 4.4 – Temperature Reporting clarified as ASIC die temp reporting. Also clarified die temp reporting is independent of the transceiver temp reporting. - Section 4.6 – Transceiver module temperature reporting is always required and is independent of the network ASIC TDP 5W threshold. - Section 4.10.1 – Add double byte FRU EEPROM access diagrams for clarity. FRU EEPROM WP mechanism may optionally be over written in the field to allow for field updates. - Section 5.1 – Re-wrote NC-SI over RBT SI recommendations. Broke up into three sections: common, baseboard, and OCP NIC 3.0 requirements. - Section 5.2 – Reference SMBus and PCIe CEM specifications for SI, routing and signal requirements. - Sections 6.2.x – Add notes to consider airflow requirements in Aux and Main Power Modes for SFF & LFF in Hot & Cold Aisle implementations. - Section 6.7 – Non-operational shock fixture – CAD files on wiki. Updated test procedure requirements. | | |
| OCP NIC 3.0 Subgroup | <ul style="list-style-type: none"> - Section 1.1 – Update OCPHL-P license link due to opencompute.org site restructuring. - Section 1.3 – Update NIST Special Publication 800-193 to May 2018 release - Section 1.3.1 – Add I²C as a trademark of NXP Semiconductor. - Section 2.1 – Add safety requirement text and cross reference Section 7.1.3. - Section 2.1.1 – Add requirement regarding maximum extraction force on heatsink for internal lock implementations. - Section 2.x – Update Mechanical 2D drawings from WG notes - Section 2.7 – Clarify insulator access hole requirements. - Section 3.4.1 – Clarify PWRBRK[0:1]# card pull up resistor value as 95kΩ or larger and must meet the T_{PWRBRK} timing parameter per PCIe CEM. Provided recommended Baseboard value between 4.7 kΩ and 10 kΩ. - Section 3.4.4 – Updated NC-SI over RBT signal list pull down requirements. TX_EN and TXD[1:0] pull downs moved between RBT isolation circuit and OCP NIC 3.0 connector to prevent NIC side signals | 0.90 | 06/20/2019 |

| Author | Description | Revision | Date |
|----------------------|---|----------|------------|
| | <p>from floating when RBT_ISOLATE# is asserted. Updated NC-SI diagrams to depict this change. Clarify HW ARB_IN / ARB_OUT ring integrity requirements for baseboards with multiple OCP NIC 3.0 slots.</p> <ul style="list-style-type: none"> - Section 3.4.6 – Clarify +12V_EDGE and +3.3V_EDGE requirements when AUX_PWR_EN and MAIN_PWR_EN are asserted. - Section 3.4.6, 3.8.x, 3.9, 4.10.1 – Add optional Programming Mode power state. Add state of NIC_PWR_GOOD when in Programming Mode. Update Power state diagram with Programming Mode. - Section 3.5.3 – Bifurcation decoder table updated to align with bifurcation spreadsheet. - Section 3.8 – Rename section from “Power Capacity and Power Delivery” to “Power State Machine.” Add text about Programming Power State. Clarify normal power state flow. - Section 3.11 – Add Programming Mode sequencing diagram detailing transition from ID Mode to Programming Mode and back to ID Mode. - Section 4.10.2 – Move FRU write protection mechanism to a dedicated section heading. - Section 4.10.3 – Modify OEM Record Offsets for supporting FRU write protection, Programming Mode power state, and thermal requirements. <p>Offset 03 – Values now advertise compliance to specification 0v90. Offset 06/07 – Changed Hot/Cold Aisle tier for use with passive cables. Offset 17 – advertise FRU write protection mechanism. Offset 18 – advertise if the Programming Mode Power State is supported. Offset 19/20 – Add Hot/Cold Aisle tier for use with active cables. Offset 21/22 – Add Reference module power and temperature level. Offset 23 – Add reference active cooling fan fail tier requirement. Offset 31 – Defined “controller” as a SMBus connected device in the context of the FRU UDID.</p> <ul style="list-style-type: none"> - Section 5.1, 5.1.2, 5.1.4 – Add NC-SI over RBT requirements for LFF - Section 6.4 – Update thermal test fixture feature list. - Section 6.6 – Update card cooling tiers. Combined Hot Aisle and Cold Aisle airflow definition. - Section 6.7.2 – Clarified Shock and Vibe testing shall be tested in the order noted in the specification. | | |
| OCP NIC 3.0 Subgroup | <ul style="list-style-type: none"> - Section 2.2 – Clarified line side implementations may be a subset of I/O listed in Table 7. - Section 2.x – Update ejector lever and faceplate to support a clinch nut implementation. <p>Updated Figure 13 & Figure 14 with new ejector lever diagrams Updated Table 9 with updated drawing & clinch nut. Removed bushing and wave washer from BOM. Updated Figures 16, 18 generic I/O plate for ejector clinch nut Updated Figures 19, 20 with Ejector Lever clinch nut updates. Updated Figure 21 with Ejector lock design. Renamed Section 2.4.8 (was Ejector Bushing, now Clinch Nut), Removed Section 2.4.9 (was Ejector Wave washer)</p> <ul style="list-style-type: none"> - Section 3.4.1, 3.4.3 and 3.4.6 – Clarified the PWRBRK[0:1]#, SMBus and AUX_PWR_EN of SFF and LFF. These pins are defined on both the Primary and Secondary Connectors. SFF and LFF cards shall use the Primary Connector pin. The Secondary Connector pin is reserved for a future use case. | 0.91 | 07/24/2019 |

| Author | Description | Revision | Date |
|----------------------|---|----------|------------|
| OCP NIC 3.0 Subgroup | <ul style="list-style-type: none"> - Section 4.3 – Clarified MC MAC address provisioning requirements for multi-host capable cards as the maximum number of supported hosts. - Section 3.2.4 – Figure 77 was inadvertently changed to include an “Option D” straddle mount connector for a host PCB thickness of 0.105”. This was an error and has been removed. - Section 3.4.3 – Add “AUX Power Good (local signal)” to the isolator figure. - Section 3.5.3 – Add implementation note to state baseboard vendors only need to implement PCIe bifurcation options applicable to their topology. - Section 3.10 – Clarified that RBT hot-plug is not supported in DSP0222 version 1.1 and 1.2. This is feature would be dependent on future revisions of the DSP0222 specification. - Section 3.11 – Change the max T_{APL} / T_{MPL} (AUX_PWR_EN to NIC_PWR_GOOD and MAIN_PWR_EN to NIC_PWR_GOOD) parameters from 25ms to 50ms. - Section 4.10.3 – Changed offset three to state “OCP NIC 3.0 card FRU record released with version 0.90”. The same FRU Record field may be used with incremental revisions of the specification. - Section 7.1.2, 7.1.4 – Add text for co-reporting testing for EN 55024 and EN 55035. | 0.92 | 11/22/2019 |
| OCP NIC 3.0 Subgroup | <ul style="list-style-type: none"> - Section 2.1.1 – Update max permissible heatsink force applied for internal lock variant. - Section 2.3 – Removed faceplate callout #8 (wave washer), and #11 (no longer used) from the text under Figure 13 and from Table 9. - Section 2.4.3 – Update SFF Generic I/O faceplate – Figures 15-17 - Section 2.4.4 – Update LFF Generic I/O faceplate – Figure 18 - Section 2.4.8 – Update Clinch nut drawings – Figures 22 and 23 - Section 2.5.x – Update Keep Out zone drawings – Figures 24-33 - Section 2.7.1 – Update SFF insulator drawings – Figures 35 and 36 - Section 2.7.2 – Update LFF insulator drawings – Figures 38 and 39 - Section 2.8.2 – Update SFF Pull Tab CTF dimensions – Figures 40-42 - Section 2.8.3 – Update SFF Ejector latch CTF dimensions – Figs 43-45 - Section 2.8.4 – Update SFF Internal latch CTF dimensions – Figs 46-48 - Section 2.8.5 – Update SFF Baseboard CTF dimensions – Figs 50-53 - Section 2.8.6 – Update LFF Ejector latch CTF dimensions – Figs 54-56 - Section 2.8.7 – Update LFF Baseboard CTF dimensions – Figs 58-60 - Section 3.1 – Update SFF-TA-1002 card edge drawings – Figs 67-69 - Section 3.4.5 – For LFF, multiplex scan chain thermal pins (TEMP_WARN, TEMP_CRIT, FAN_ON_AUX) and WAKEn for PRSNTB[3:0] from the secondary connector. - Section 3.4.5 – Add NIC and baseboard timing requirement tables for the Scan Chain. - Section 3.7.2 – Update line side LED luminance range and add statement regarding the measurement methodology as a WIP. - Section 4.3 – Add second Management Controller MAC Address Algorithm. Add link to OCP NIC 3.0 wiki to download MAC Address algorithm calculator spreadsheet. - Section 4.10.3 – Offset 3 – Rearranged sentences for the OEM Record Format description. Technical content remains the same. Offset 15 – Add USB Present – Primary Connector field value 0x02-0xFE as Reserved for future use, and 0xFF as Unknown for consistency. Offset 16 – Change Manageability Type field value 0x04-0xFE as Reserved for future use, and 0xFF as Unknown for consistency. Offsets 17, 18, 21, 22, 23 – Change value 0xFF as Unknown instead of Reserved for consistency with offsets 0-16. | 0.99 | 12/18/2019 |

| Author | Description | Revision | Date |
|----------------------|---|----------|------------|
| OCP NIC 3.0 Subgroup | Document release – version R1v00 | 1.00 | 12/19/2019 |
| OCP NIC 3.0 Subgroup | <ul style="list-style-type: none"> - General – Fixed Power Sequence Timing Requirements as Heading 2 (was incorrectly changed to Heading 3). Fixed index order for BIF pins as [2:0]. Previous versions of this document had mixed indexes represented as BIF[0:2], and incorrectly as BIF[3:0] in some instances. Fixed index order for PRSNTB pins as [3:0]. - General – Uniformly changed references for Aux Power Mode and Main Power Mode. Removed references to ACPI power states S5 and S0. Added additional text to Section 3.8.3 and 3.8.4 for the included ACPI power states. - Section 1.2 – Acknowledgements section updated. Company name updates. - Section 1.5 – Add Conventions section to define numerical representation in binary and hexadecimal radix. Standardized unit representations per the Bureau International des Poids et Mesures (BIPM). The number and unit are always separated with a space (example: for temperature “5 °C.” Units, where applicable, have been changed to their SI symbol. Most notably, “Ohm” is now represented with the uppercase letter omega “Ω”. - Section 1.7.2.1, 1.7.2.2 – Minor update to clarify Primary connector is a 4C+ as defined in SFF-TA-1002 and consists of an “OCP Bay” and a “4C” region. - Section 2.5.1, 2.5.2 – Figure 24 & 29 – Update PCB break off note #3 to include feature max tolerances. - Section 2.8.2 – Figure 40 – Updated dimension notation with parenthesis and add center line labeled as CL DATUM H for consistency across form-factor figures. - Section 2.8.3 – Figure 43 – Add center line labeled as CL DATUM H for consistency across form-factor figures. - Section 2.8.4 – Figure 46 – Add center line labeled as CL DATUM H for consistency across form-factor figures. - Section 3. 4 – Add clarification statement for Aux Power Mode and Main Power Mode in relation to ACPI power states. - Section 3.4.2 – Add recommendation on the PRSNTB[0:3] strapping resistors values as 0 Ω to 200 Ω. - Section 3.4.5 – Scan Chain text clarification and diagram updates. - Section 3.4.6 – Clarified the state of NIC_PWR_GOOD in relation to AUX_PWR_EN, MAIN_PWR_EN and the enabled power domain signals within operational tolerances in the truth table. - Section 3.8 – Power state machine diagram updated - +12V_EDGE in ID Mode and Programming Mode marked as optional. - Section 3.8.3 – Clarified that Aux Power Mode includes ACPI power states S3, S4 and S5 as they are equivalent from a power delivery and sequencing perspective. - Section 3.8.2, 3.8.5 – Clarifications to +12V_EDGE in ID/Programming mode. +12V_EDGE is now marked as optional in these two states. A max permissible leakage voltage is stated and the baseboard has an optional a bleed resistor. - Section 3.9 – Clarification on the slot power envelope definition (assuming that is the same path the PCI SIG is going). Add 50W power class. Increased +12V_EDGE capacitance limits on 50W, 80W and 150W power class cards. - Section 3.10.1 – Changed +12V_EDGE on normal power up sequence and programming mode power sequence diagrams to optional. | 1.0.9 | 10/28/2020 |

| Author | Description | Revision | Date |
|----------------------|---|----------|------------|
| | <ul style="list-style-type: none"> - Section 4.1 – Change PCIe VDM and MCTP Base over MCTP/PCIe VDM to N/A for RBT Type cards. - Section 4.4 – Add Warning/Critical/Fatal temperature threshold example text as discussed in the June NIC 3.0 monthly meeting. Define Warning, Critical and Fatal criteria. - Section 4.10.3 – Modify FRU OEM Record. Offset 3 – Add new FRU record version for spec version 1.1. Offset 9 – Clarified this is the Hot aisle standby air flow requirements when using active cables. Defined value 0x0000 for card only supporting passive cables – similar to offset 19. Offset 11 – Clarified this is the Cold aisle standby air flow requirements when using active cables. Defined value 0x0000 for card only supporting passive cables – similar to offset 19. Offset 21 – Add QSFP Power Class 8 (10.0 W transceivers). Offset 24 – Add definition on which ports are supported in Aux Power Mode. Offset 25 – Add definition for Hot aisle standby air flow requirements when using passive cables or RJ45. Offset 27 – Add definition for Cold aisle standby air flow requirements when using passive cables or RJ45. - Section 5.3.x – Add PCIe Gen5 text/fixture/test methodology updates. PCIe Gen5 for SFF uses a max -7.0 dB insertion loss at 16 GHz. - Section 6.4.4 – Add thermocouple notes for cold-aisle inlet temperature measurements. | | |
| OCP NIC 3.0 Subgroup | Document release – version R1.1.0 | 1.1.0 | 10/29/2020 |
| OCP NIC 3.0 Subgroup | <ul style="list-style-type: none"> - General – Changed “SFF” references to “SFF/TSFF” where applicable. - General – Format all tables with repeated headers when they span multiple pages - Section 1.2 – Added Molex to the acknowledgements section. Changed NVIDIA to NVIDIA Corporation. - Section 1.4 – Added TSFF, OSFP-RHS and QSFP-DD to the acronyms section. - Section 1.6, 2.1.1 – Added text for TSFF and clarify TSFF shares the same mechanical outline as SFF. Add representative TSFF diagram. - Section 1.7.1 – Added TSFF to the OCP NIC 3.0 Form Factor Dimensions table; add Max Z-height information. Added note that SFF may fit in TSFF slot and in LFF slot, but the combination (and support mechanisms) are outside of the scope of the current specification. - Section 1.7.2.x – Updated text “Up to PCIe Gen 5 (32 GT/s) support” - Section 2.1 - Add TSFF. Add notes that actual cooling capacity for a SFF/TSFF/LFF card is dependent on the ambient conditions over the NIC. - Section 2.1.x – Clarified that faceplates are attached to the PCBA at the time of manufacture. - Section 2.1.1 – Add TSFF faceplate views to Figure 7. - Section 2.2 – Add QSFP-DD, OSFP-RHS in Line side implementation table. Add QSFP-DD, OSFP to standards cross reference table. - Section 2.3 – Add TSFF PBA exploded views to Figure 13. - Section 2.4.1, 2.4.2 – Updated faceplate subassembly drawing and BOM callouts for SFF/TSFF. - Section 2.4.4 – Added TSFF generic faceplate drawings. Drawings only contain dimensional deltas from SFF. - Section 2.5.2 – Added TSFF keep out zones. Drawings only contain dimensional deltas from SFF. - Section 2.8.5 - Replaced Figure 56 - SFF Baseboard Chassis CTF | 1.2.0 | 09/13/2021 |

| Author | Description | Revision | Date |
|--------|---|----------|------|
| | <p>dimensions (Rear Rail Guide View) as it was clipped in the previous release.</p> <ul style="list-style-type: none">- Section 2.8.6, 2.8.7, 2.8.8, 2.8.9 – Added TSFF CTF dimensions for pull tab, ejector and internal lock board dimensions. Add TSFF baseboard CTF dimensions. Drawings only contain dimensional deltas from SFF.- Section 2.10 – Added TSFF Generic faceplate assembly CAD.- Section 3.4.1 – Clarified that hosts with unused PERST[1:5]# signals shall implement at 10kOhm pull down on the baseboard to prevent floating nets.- Section 3.4.2, 3.5.4 – Clarified that the BIF[2:0]# pins shall not change states after AUX_PWR_EN is asserted.- Section 3.4.4 – Clarified that the RBT_ISOLATE# signal shall not change state even when the NIC_PWR_GOOD signal is in the don't care state.- Section 3.7.3 – Added note regarding the use of light pipes above I/O cage assemblies for TSFF and cage implementations.- Section 3.11 – Clarified power down sequencing diagram - +12V_EDGE may optionally be disabled in ID Mode. This mirrors the same behavior for the power up sequencing diagram.- Section 5.1 – Added note stating the SFF and TSFF timing parameters are the same since the cards may share the same PBA.- Section 6.2.2, 6.2.5 – Added placeholder headings for the hot and cold aisle cooling graphs for TSFF.- Section 6.4.2 – Added placeholder heading for the TSFF thermal test fixture.- Section 6.4.5 – Added placeholder figure headings for the TSFF candlestick air velocity vs volume flow graphs.- Section 7.1.3 – Updated Safety requirements. 60950-1 was withdrawn as of 12/20/2020. 62368-1 replaced 60950-1. <p>Document release version R1.2.0</p> | | |

8.2 FRU Content Revision History

The following table summarizes the FRU content revision history and maps it against specification releases.

| Date | Change Description | Released with Spec Version |
|------------|---|----------------------------|
| 01/25/2018 | - Initial FRU contents. | 0.70 |
| 06/04/2018 | - Offset 4, 5 – Clarified that the Card Max Power in Main Power Mode and the Card Max Power in Aux Power Mode do not include the power consumed by transceivers plugged into the line side receptacle(s). - Offset 8 – Corrected Card active/passive cooling) as a byte value (not bitwise). - Offset 13, 14 – Removed ASIC temperature target; replaced with UART Configuration 1 and UART Configuration 2. - Offset 15 – Added USB Present. - Offset 32-127 – Explicitly called out UDID offset ranges for controllers 1 through 6. | 0.80 |
| 07/06/2018 | - Offset 13, 14 – Clarified these offsets are only applicable to the Secondary Connector (LFF designs) - Offset 15 – Clarified this offset is only applicable to the Primary Connector (SFF designs) | 0.81 |
| 11/20/2018 | - Offset 3 – Corrected Manufacturer ID as 0x00A67F. - Offset 9, 10 – Clarified hot aisle standby airflow LSB, MSB byte order. - Offset 11, 12 – Clarified cold aisle standby airflow LSB, MSB byte order. - Offset 16 – Add card manageability type. | 0.85 |
| 04/02/2019 | - Offset 32-127 – Add note declaring the controller UDID fields may be omitted and left as zero length if no corresponding controller is present on the card. | 0.86 |
| 06/20/2019 | - Offset 3 – Updated FRU OEM Record Version compliance. Cards complaint to spec version 0x90 shall use the value 0x01. All other values reserved. - Offset 6 – Clarified Hot Aisle Card Cooling Tier offset is applicable to passive cable or RJ-45 implementations. - Offset 7 – Clarified Cold Aisle Card Cooling Tier offset is applicable to passive cable or RJ-45 implementations. - Offset 9, 10 – Clarified hot aisle standby airflow requirement with an approach air temperature of 45 °C. - Offset 11, 12 – Clarified cold aisle standby airflow requirement with an approach air temperature of 35 °C. - Offset 17 – Add FRU Write Protection Mechanism indication. - Offset 18 – Add Programming Mode Power State indication. - Offset 19 – Add Hot Aisle Cooling Tier with Active Cables indication. - Offset 20 – Add Cold Aisle Card Cooling Tier with Active Cables indication. - Offset 21 – Add Transceiver Reference Power Level indication. - Offset 22 – Add Transceiver Reference Temperature Level indication. - Offset 23 – Add Card Thermal Tier with local Fan Fail indication. - Offset 31 – Clarify Number of Physical Controllers as the number of SMBus connected controllers on the OCP NIC 3.0 card. | 0.90 |
| 11/08/2019 | - Offset 3 – Changed FRU OEM Record Version definition to declare “this FRU record is released with version x.xx” of the specification. This prevents revising the field to match future specification releases when no FRU changes have been made. | 0.92 |
| 12/8/2019 | - Offset 15 – Add USB Present – Primary Connector field value 0x02-0xFE as Reserved for future use, and 0xFF as Unknown for consistency within the OEM record. - Offset 16 – Change Manageability Type field value 0x04-0xFE as Reserved for future use, and 0xFF as Unknown for consistency within the OEM record. - Offsets 17, 18, 21, 22, 23 – Change value 0xFF as Unknown instead of Reserved for consistency with offsets 0-16. | 0.99 |
| 10/28/2020 | - Offset 3 - Add new FRU record version for spec version 1.1. | 1.1.0 |

| Date | Change Description | Released with Spec Version |
|------|---|----------------------------|
| | <ul style="list-style-type: none">- Offset 9 – Clarified this is the Hot aisle standby air flow requirements when using active cables. Defined value 0x0000 for card only supporting passive cables - similar to offset 19.- Offset 11 – Clarified this is the Cold aisle standby air flow requirements when using active cables. Defined value 0x0000 for card only supporting passive cables - similar to offset 19.- Offset 21 – Add QSFP Power Class 8 (10.0 W transceivers).- Offset 24 – Add definition on which ports are supported in Aux Power Mode.- Offset 25 – Add definition for Hot aisle standby air flow requirements when using passive cables or RJ45.- Offset 27 – Add definition for Cold aisle standby air flow requirements when using passive cables or RJ45. | |