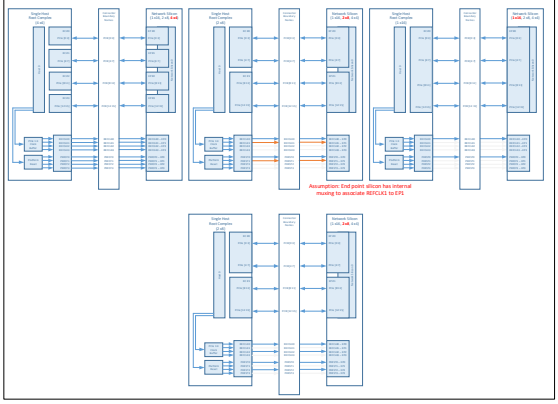
These diagrams are up for discussion – do not include in the specification yet. - 20181008a_TN

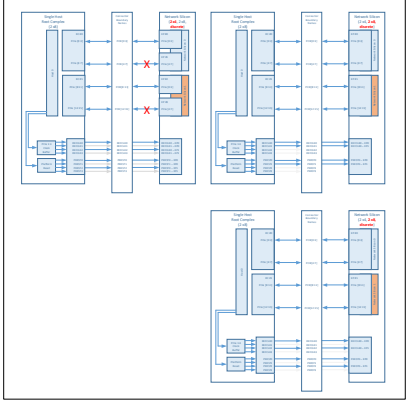
PROPOSED DIAGRAMS (and associated text update in spec)

Diagram for discussion…

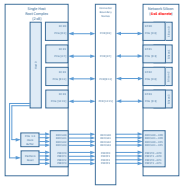
Single Host 1x16 / 2x8 / 4x4; Configurable Network Silicon 1x16 / 2x8 / 4x4



Single Host 2x8; Two discrete network silicon 2x8 / 4x4



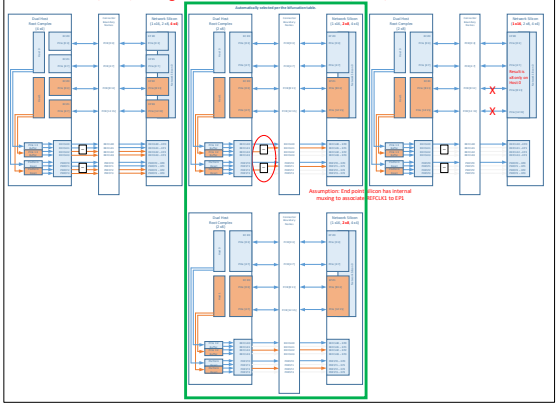
Single Host 4x4; Four discrete network silicon 4x4.



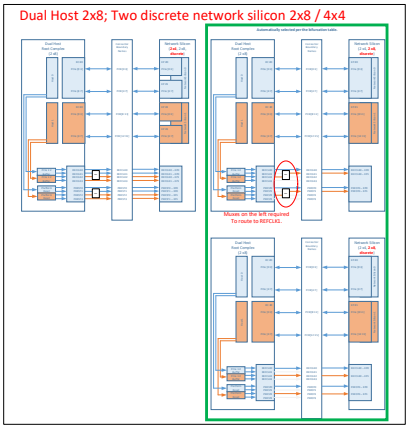
PROPOSED DIAGRAMS (and associated text update in spec)

Diagram for discussion…

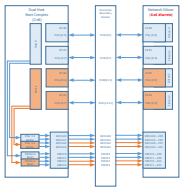
Dual Host 2x8 / 4x4; Configurable Network Silicon 1x16 / 2x8 / 4x4



Dual Host 2x8; Two discrete network silicon 2x8 / 4x4



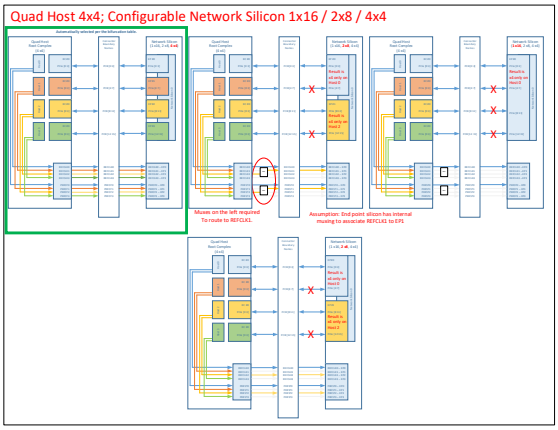
Dual Host 4x4; Four discrete network silicon 4x4.



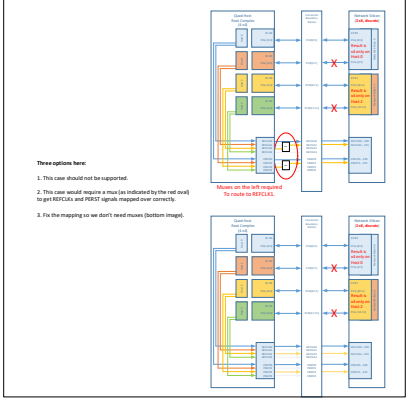
PROPOSED DIAGRAMS (and associated text update in spec)

Diagram for discussion…

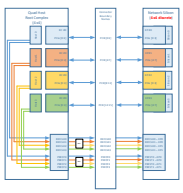
Quad Host 4x4; Configurable Network Silicon 1x16 / 2x8 / 4x4

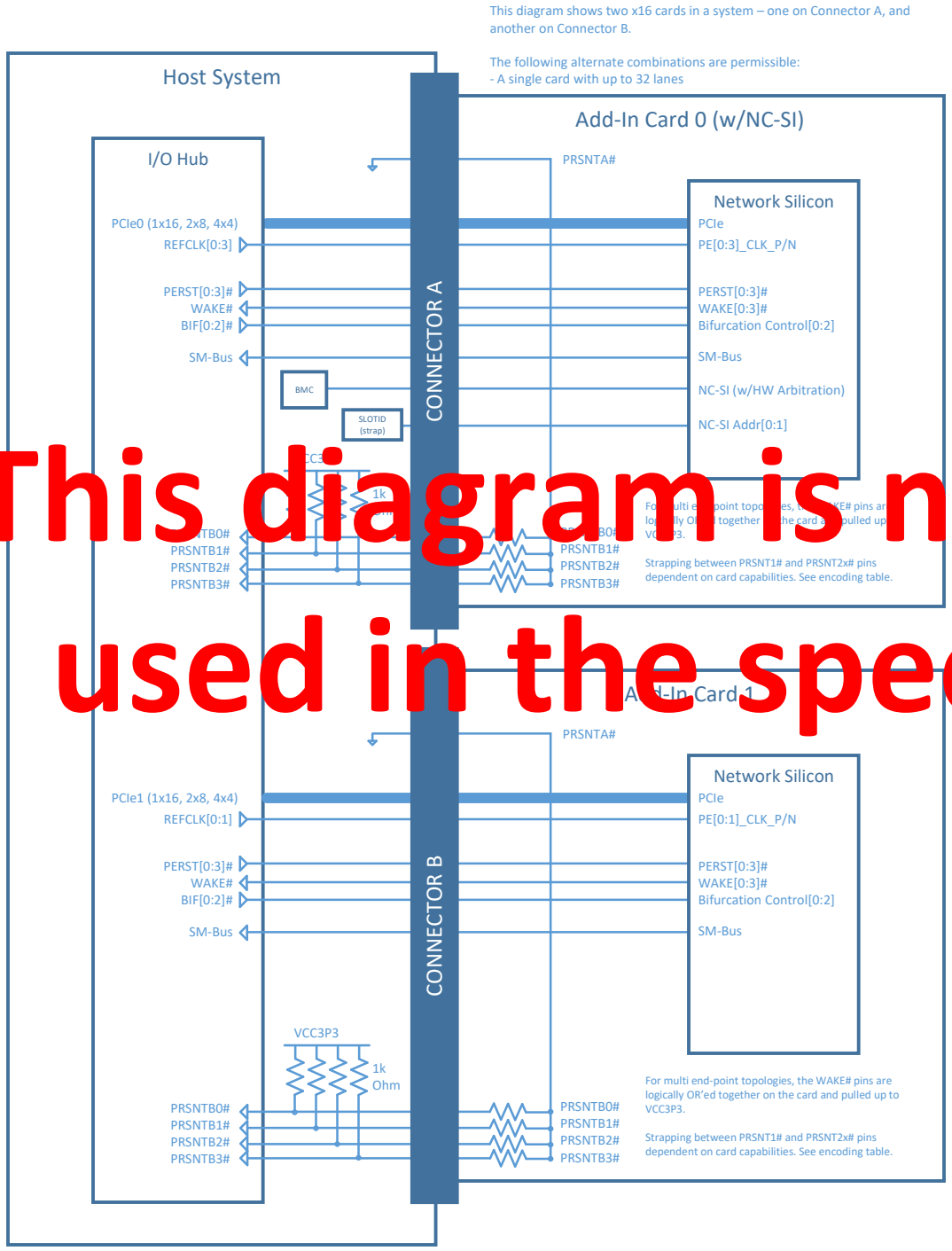


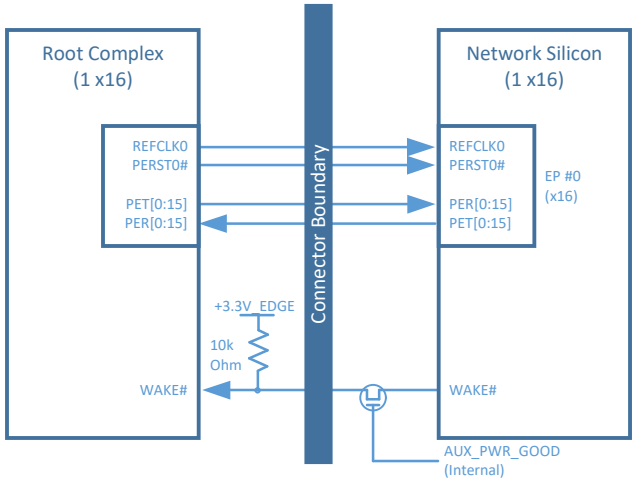
Quad Host 4x4; Two discrete network silicon 2x8

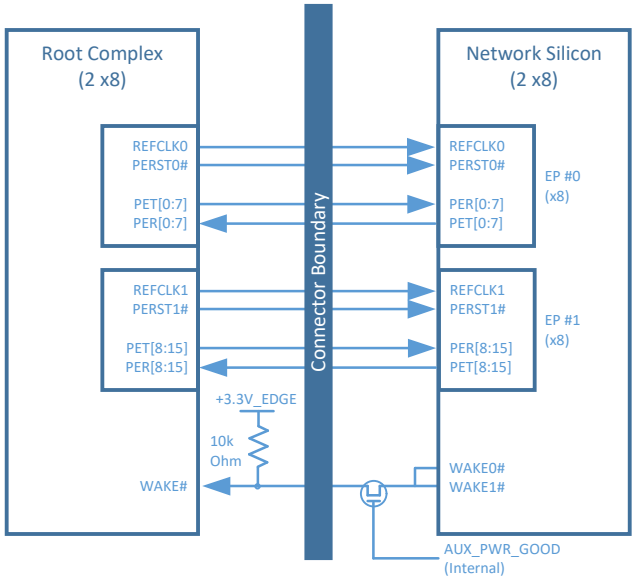


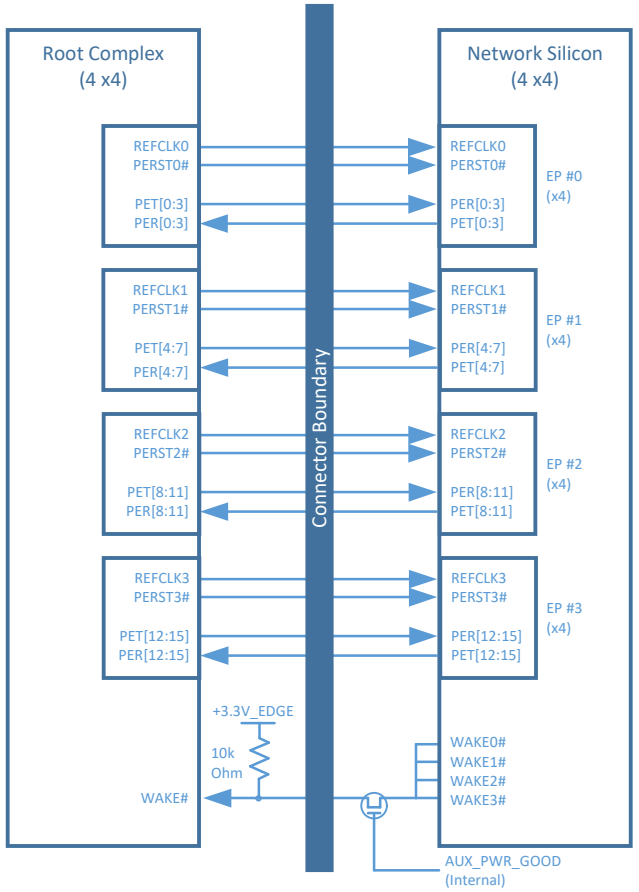
Quad Host 4x4; Four discrete network silicon 4x4.









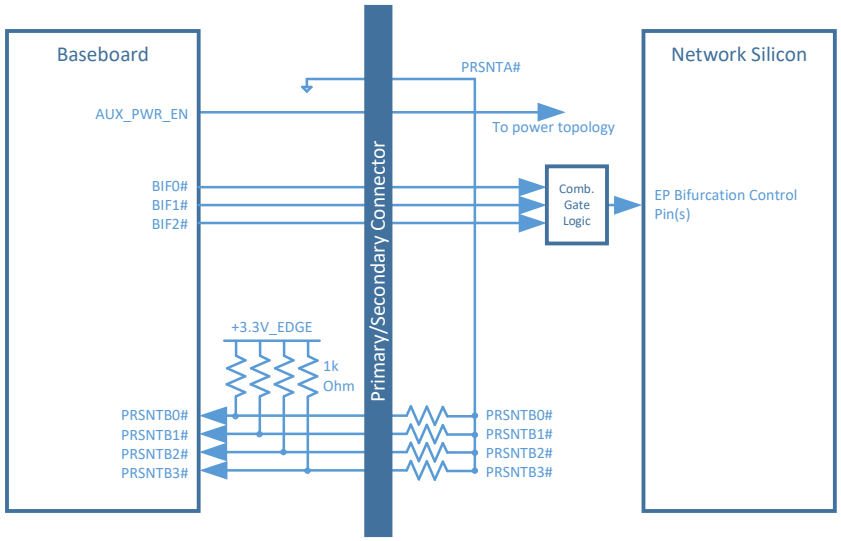


Updated 20180409a-TN – Diagram copied into the 0v73 specification
- added WAKE# gating via the AUX_PWR_EN signal to prevent WAKE# assertion prior to D3 state

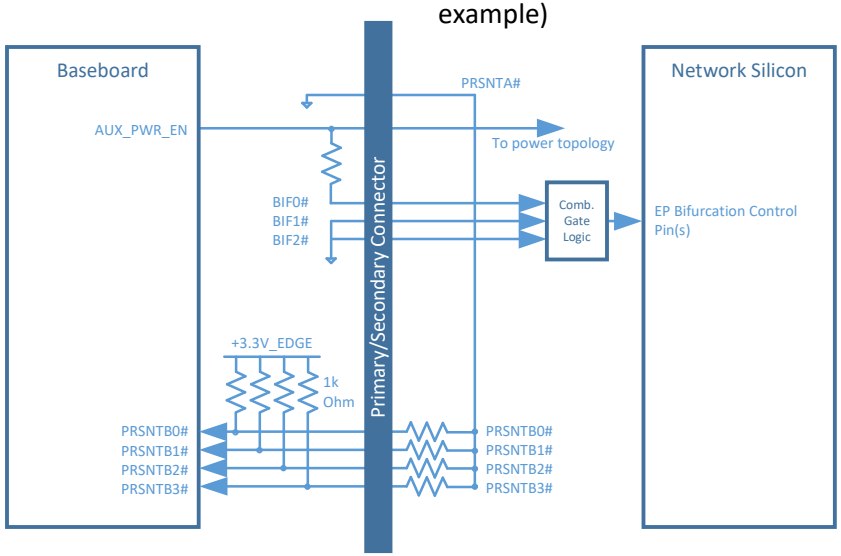
Updated 20180508b-TN – Diagrams copied into the 0v73 20180508b spec
- Changed WAKE# to being gated by an internal (on-card) AUX_PWR_GOOD signal instead of AUX_PWR_EN

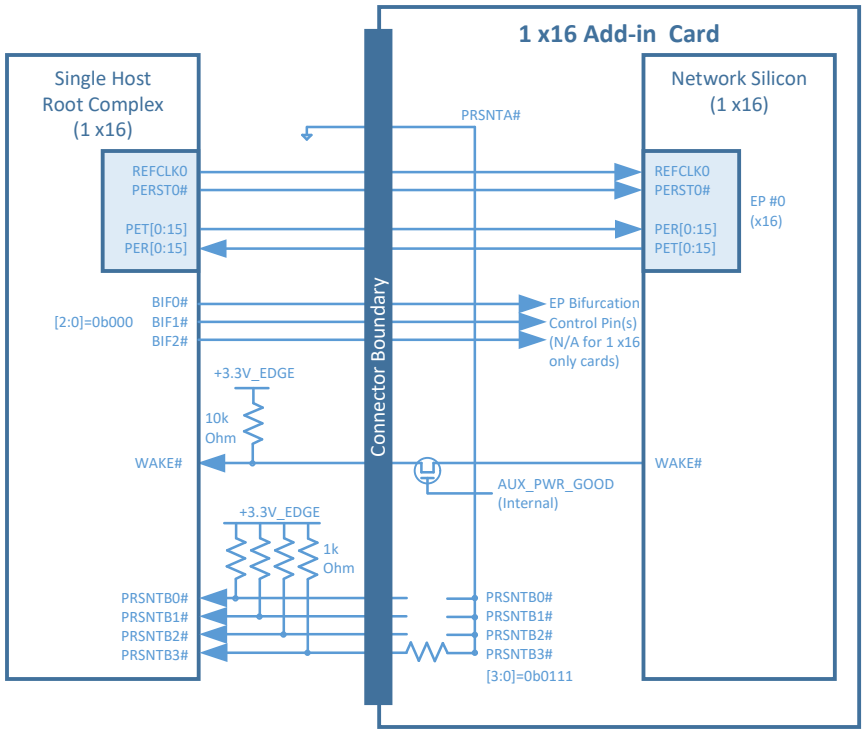
Updated 20180409a-TN – Diagram copied into the 0v73 specification
- added static BIF configuration (forced by baseboard, not configurable). BIF high values tied to AUX_PWR_EN.

PCIe Present and Bifurcation Control Pins (Baseboard **Controlled** BIF[0:2]#)

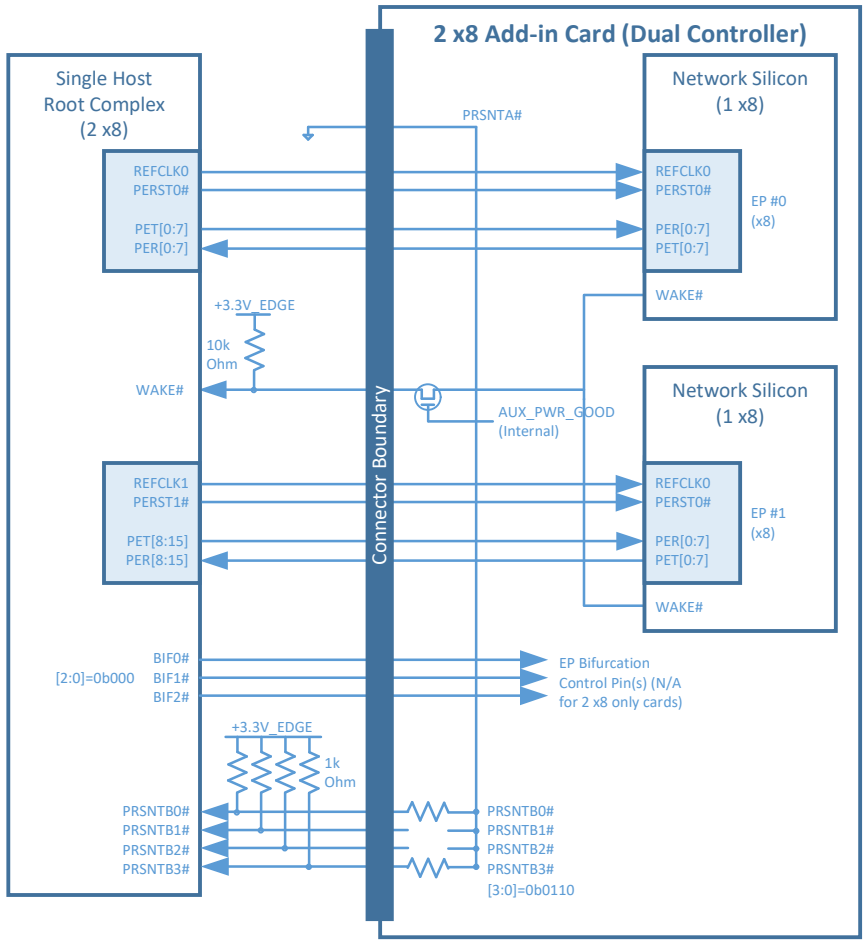


PCIe Present and Bifurcation Control Pins (Baseboard **Forced** BIF[0:2]# = 0b100, example)

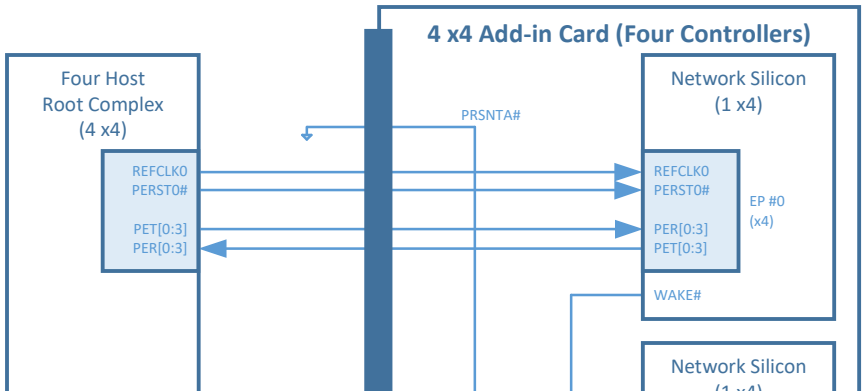


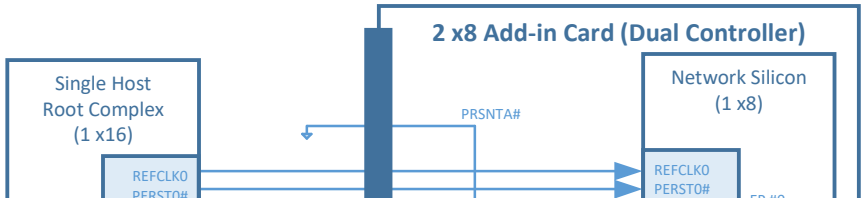


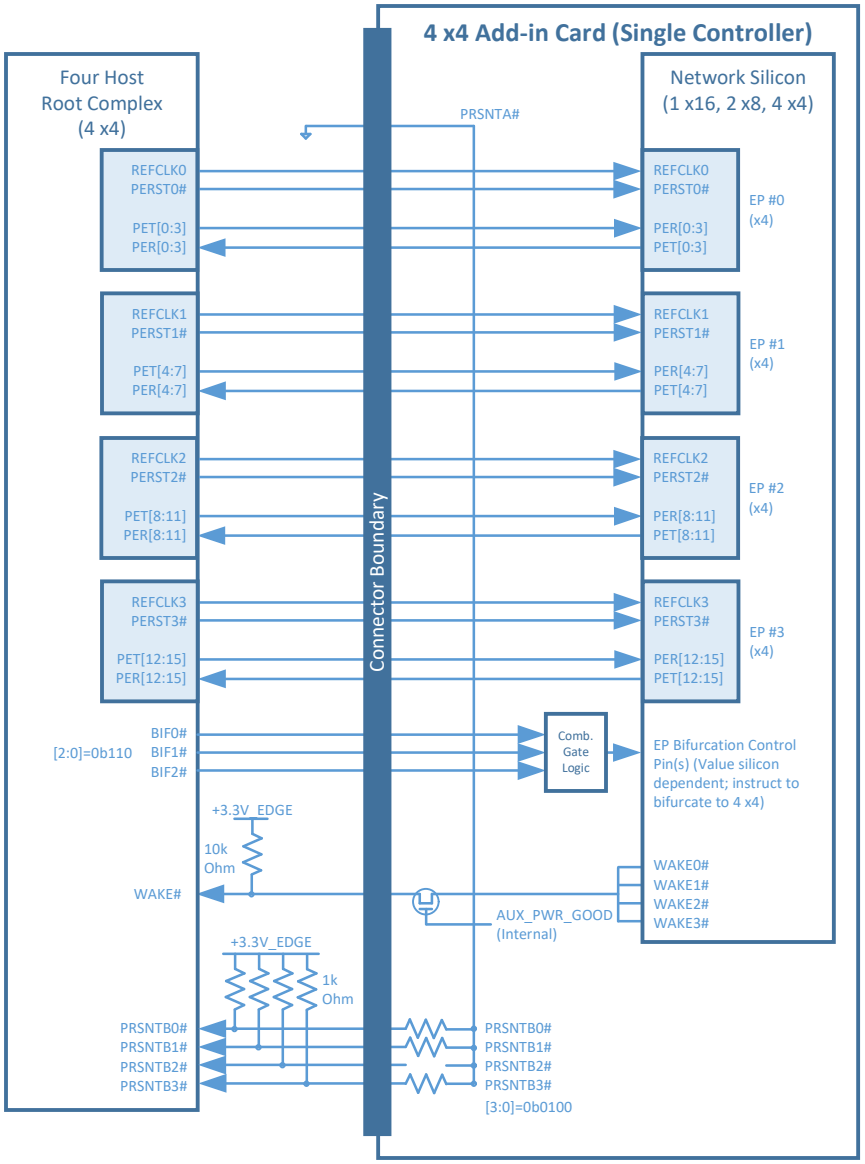
Single Host (1 x16) and 1x16 Add-in card



Single Host (2 x8) and Type 2 Add-in Card (Dual Controllers, 2 x8 only)



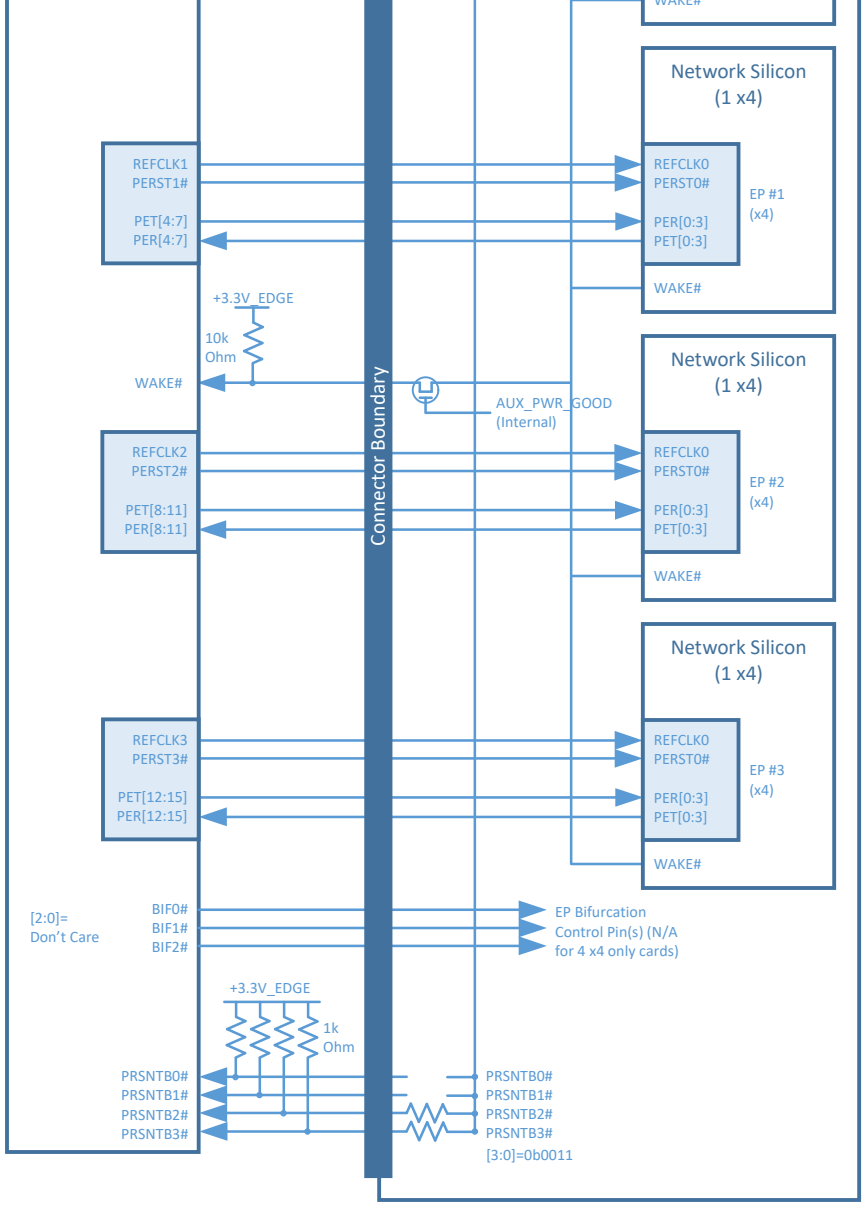




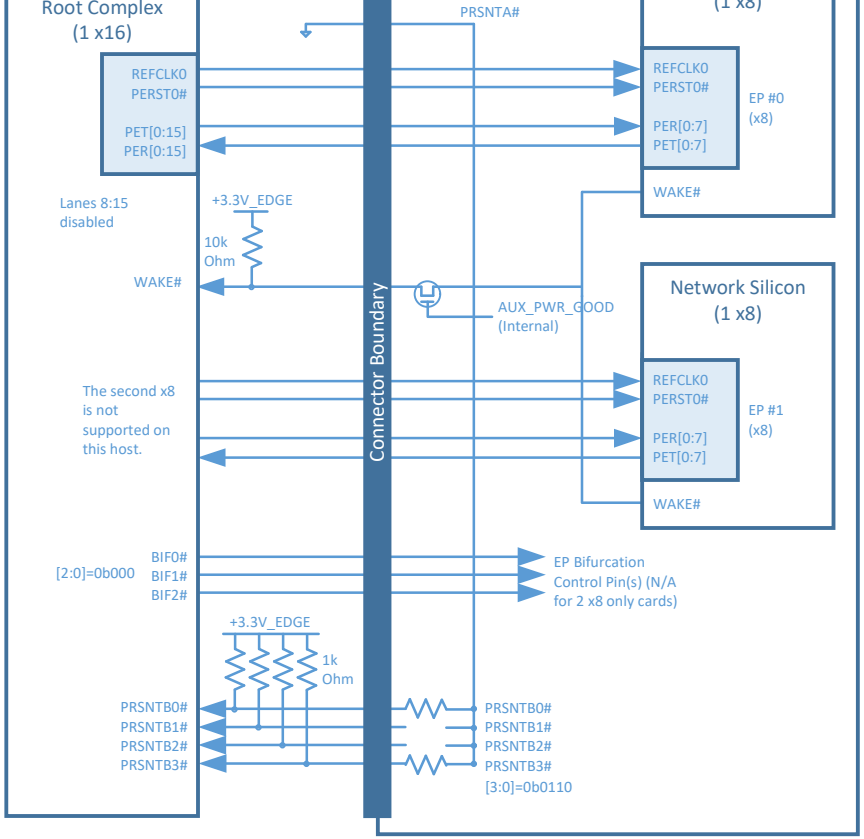
Four Hosts (4 x4) and Type 4 Add-in Card (Single Controller, 4 x4)

Updated 20180409a-TN – Diagram copied into the 0v73 specification
- added WAKE# gating via the AUX_PWR_EN signal to prevent WAKE# assertion prior to D3 state

Updated 20180508b-TN – Diagrams copied into the 0v73 20180508b spec
- Changed WAKE# to being gated by an internal (on-card) AUX_PWR_GOOD signal instead of AUX_PWR_EN



Four Hosts (4 x4) and Type 3 Add-in Card (Four Controllers, 4 x4)



Single Host with no Bifurcation (1 x16) and Dual Controllers, 2 x8 – results in 1x

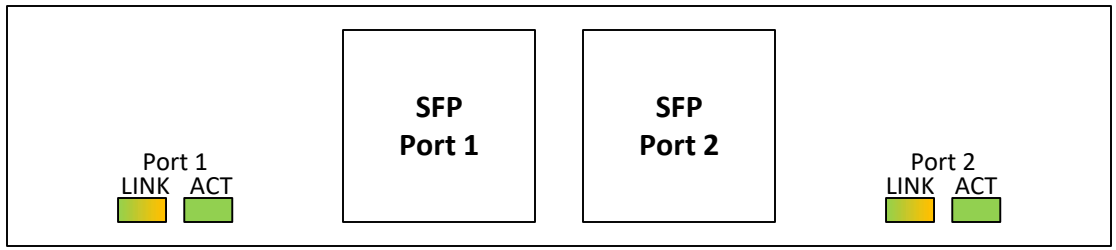
Updated 20180508b-TN – Diagrams copied into the 0v73 20180508b spec
- Changed WAKE# to being gated by an internal (on-card) AUX_PWR_GOOD signal instead of AUX_PWR_EN

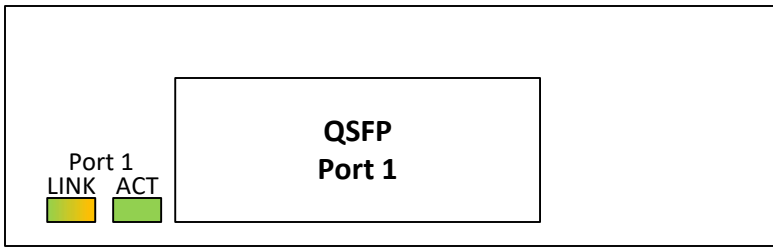
Updated 20180604d-TN – Diagrams copied into the 0v74 20180604d spec
- Fixed BIF values for all 5 examples.

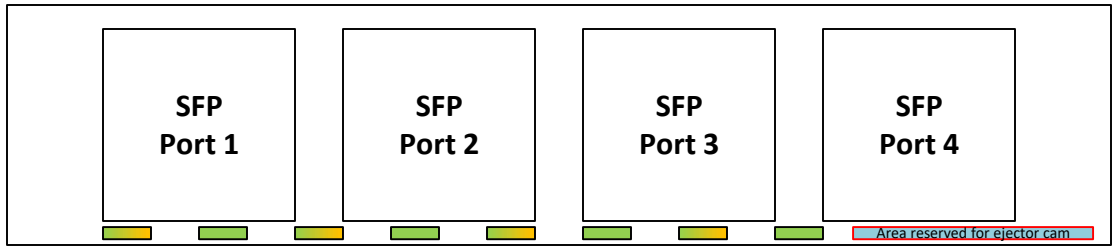
Updated 20180712a – 4 x4 BIF pin values updated and copied into the 0v82 20180712c spec

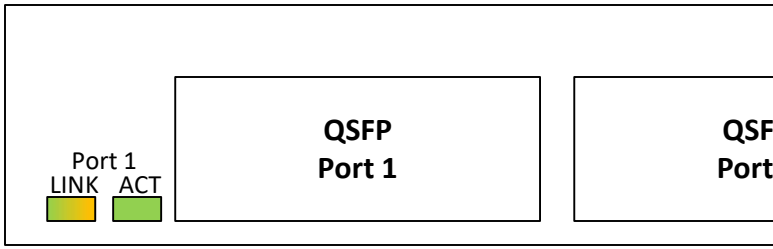
ults in 1x8

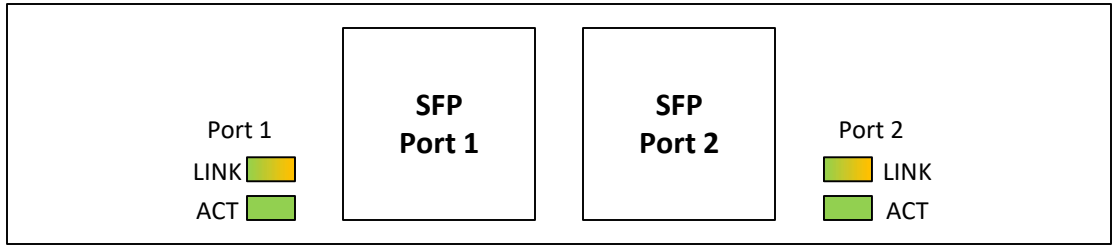
Updated 20180802a-TN – Diagram copied into the 0v82 specification

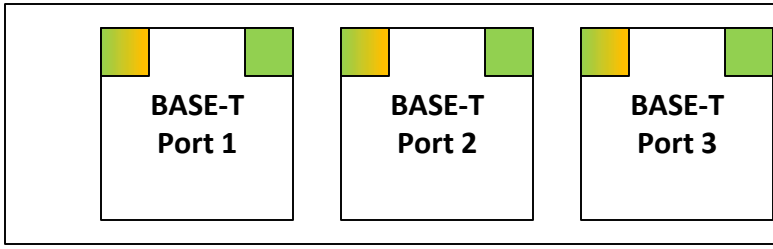


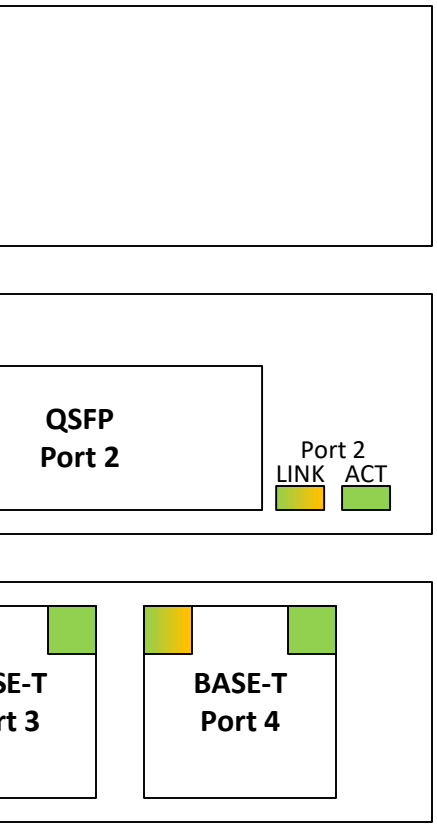












Change history:

20180425 – Add LEDs to the underside of the 4xSFP and 2xQSFP implementations. Right angle SMT LEDs on the leading edge of the board.

20180801 – Change dual QSFP to topside LEDs per ME request.
20180802 – Remove the circular stack LEDs for the top side as that would impede airflow.
20180803 – Add back the stacked LEDs.. Lower power cards should be able to still do this.

1/19/2018 Proposal (to incorporate in the 0.8 spec) Green = 513-537 nm wavelength Yellow = 580-589 nm wavelength **OCP NIC 3.0 Cards:** Link (Bi-color – green, yellow) - Green – solid illumination when linked up at the highest speed - Yellow – solid illumination when linked up at the not highest speed - The Link LED can be blinked for port identification Activity (Single Color, green only) - Green, solid – no activity present - Green, blinking – activity present	**OCP NIC 3.0 Baseboards (Scan Chain implementation):** Link (Single color – green) - Green – solid illumination when linked up. - The Link LED can be blinked for port identification Activity (Single Color, green only) - Green, solid – no activity present - Green, blinking – activity present

2/6/2018 Proposal (to incorporate in the 0.8 spec) – **note that the scan chain and on-card LED implementations are now identica**l.

Green = 513-537 nm wavelength
Amber = 580-589 nm wavelength

OCP NIC 3.0 Cards / OCP NIC 3.0 Baseboards (Scan Chain implementation):

Link (Bi-color – green, amber)
- Green – solid illumination when linked up at the highest speed
- Yellow – solid illumination when linked up at the not highest speed
- The Link LED can be blinked for port identification

Activity (Single Color, green only)
- Green, solid – link up, no activity present
- Green, blinking – link up, activity present
- Off – no link, no activity.

MAC Address Label Example 1 – Single Host, Quad Port, Single Managed Controller

P1: AA:BB:CC:DD:EE:F0
P2: AA:BB:CC:DD:EE:F1
P3: AA:BB:CC:DD:EE:F2
P4: AA:BB:CC:DD:EE:F3
ME1: AA:BB:CC:DD:EE:F4

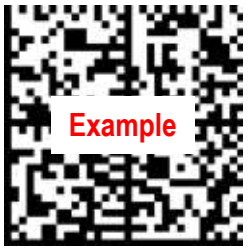
MAC Address Label Example 2 - Single Host, Octal Port, Dual Managed Controller

P1: AA:BB:CC:DD:EE:F0
P2: AA:BB:CC:DD:EE:F1
P3: AA:BB:CC:DD:EE:F2
P4: AA:BB:CC:DD:EE:F3
P5: AA:BB:CC:DD:EE:F4
P6: AA:BB:CC:DD:EE:F5
P7: AA:BB:CC:DD:EE:F6
P8: AA:BB:CC:DD:EE:F7
ME1: AA:BB:CC:DD:EE:F8
ME2: AA:BB:CC:DD:EE:F9

MAC Address Label Example 3 - Dual Host, Quad Port, Dual Managed Controller

H1 P1: AA:BB:CC:DD:EE:F0
H1 P2: AA:BB:CC:DD:EE:F1
H2 P3: AA:BB:CC:DD:EE:F2
H2 P4: AA:BB:CC:DD:EE:F3
ME1: AA:BB:CC:DD:EE:F4
ME2: AA:BB:CC:DD:EE:F5

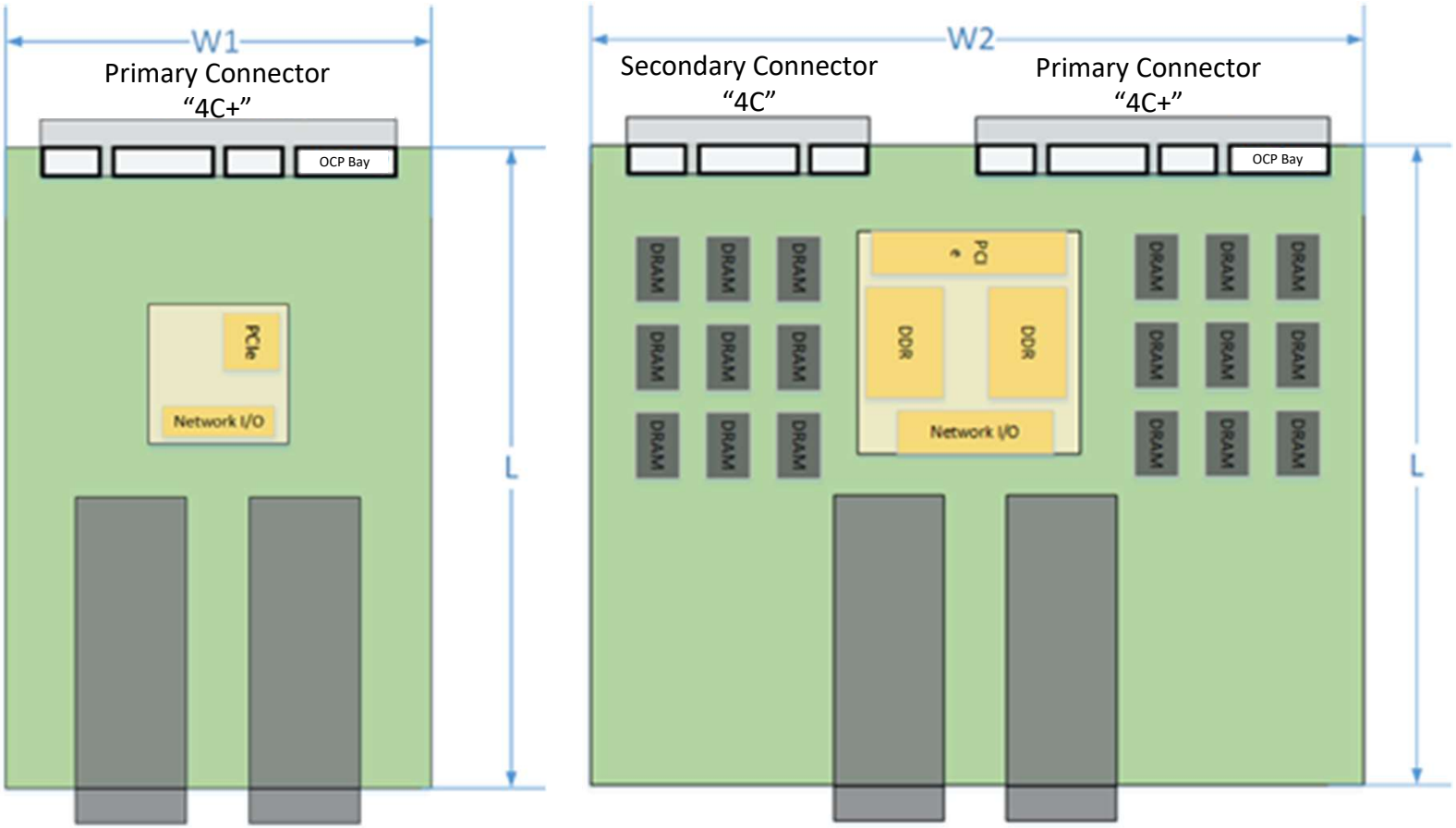
MAC Address Label Example 4 – Quad Host, Single Port, Single Managed Controller



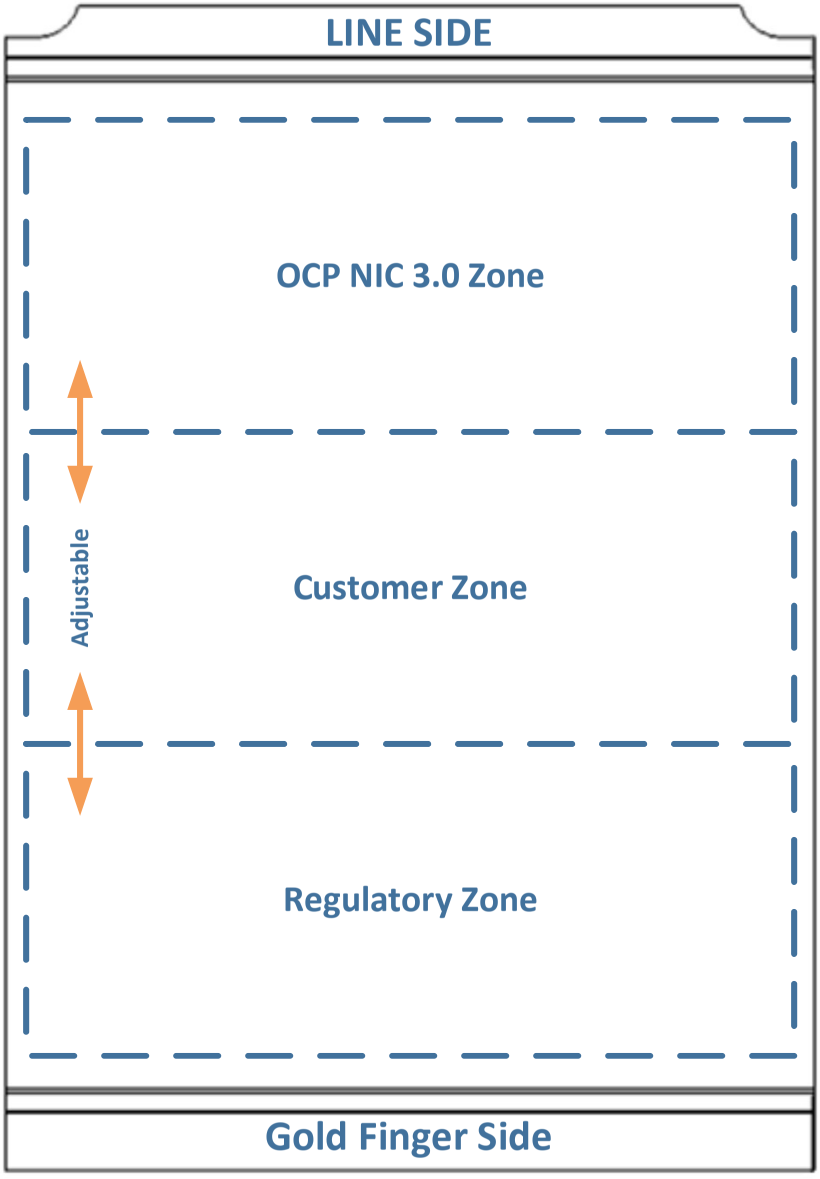
H1 P1: AA:BB:CC:DD:EE:F0
H2 P1: AA:BB:CC:DD:EE:F2
H3 P1: AA:BB:CC:DD:EE:F4
H4 P1: AA:BB:CC:DD:EE:F6

Change history:

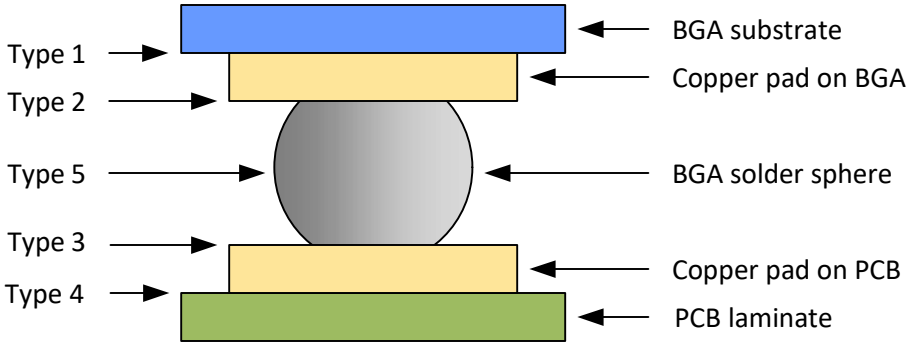
0v84 20180910 – Changed MAC address element separator from periods “.” to colons “:”



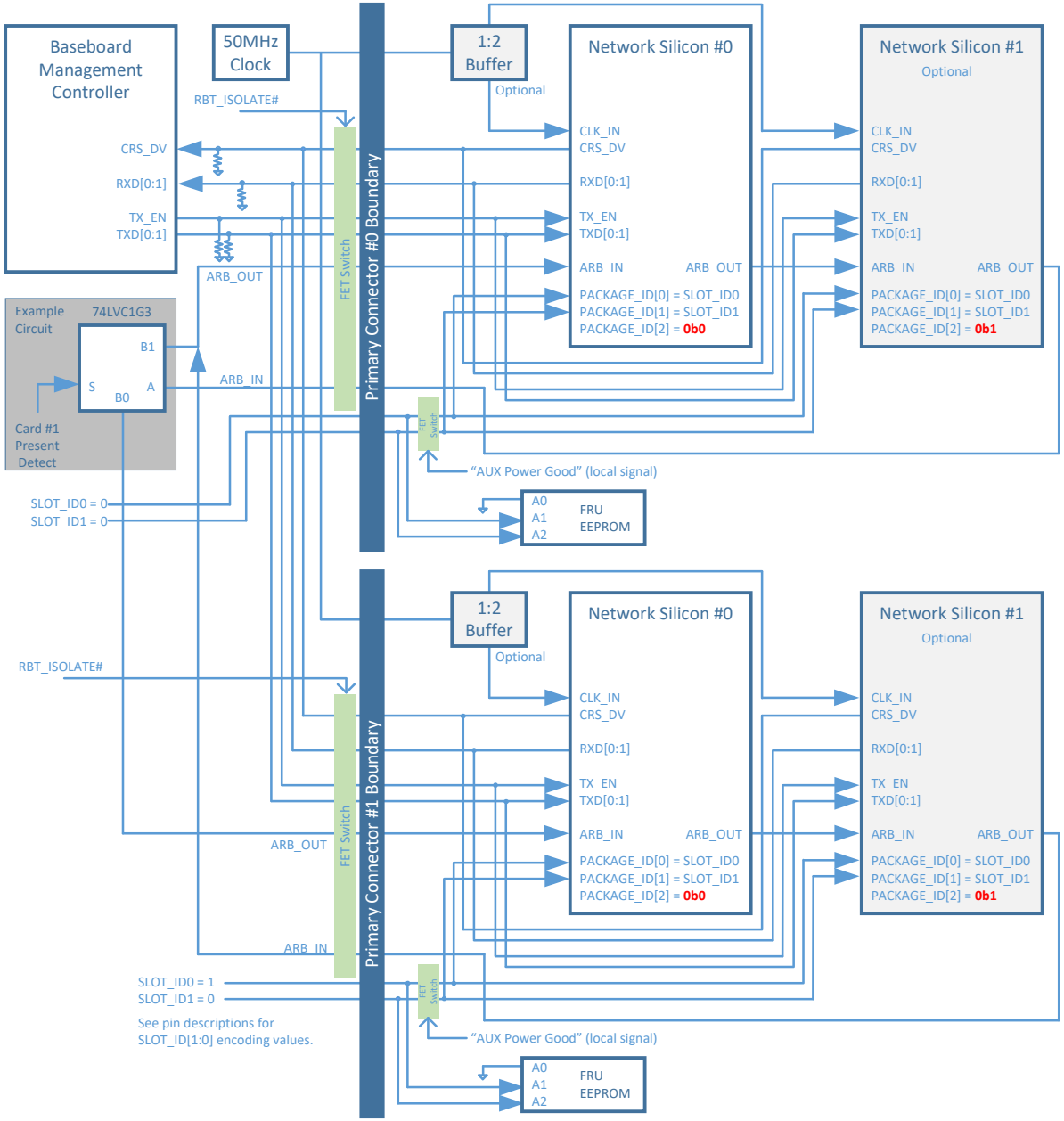
Dye and Pull diagram


LINE SIDE
OCP NIC 3.0 Zone
Adjustable
Customer Zone
Regulatory Zone
Gold Finger Side

Dye and Pull diagram

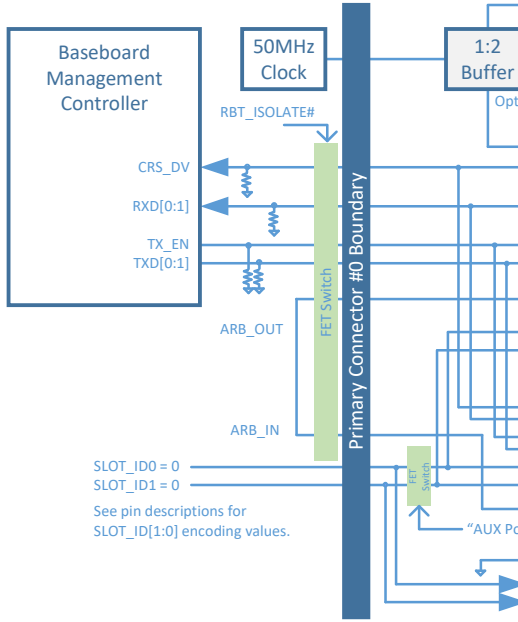


Baseboard with Dual Primary Connectors



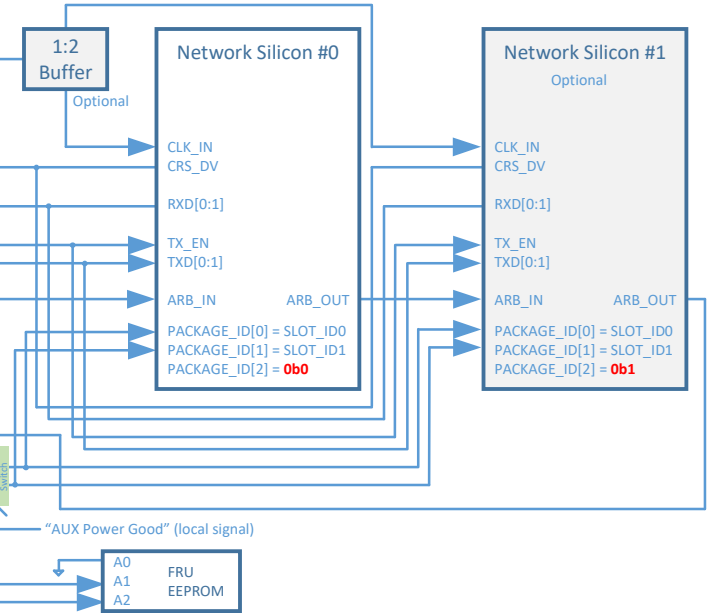
For baseboard designs with a single primary connector, connect ARB_IN to ARB_OUT to complete the NC-SI hardware arbitration ring. For Designs with multiple Primary Connectors, connect ARB_IN and ARB_OUT to an analog mux to complete the NC-SI arbitration ring based on the number of cards installed in the system.

Baseboard with a S



- The package ID is part of the Channel ID. The Package
(Channel_ID [7..5]). The most significant bit is set to 0
NC-SI spec, but a device can have it configurable.
- The Package Id [2] bit (Channel_ID[7]) is set on the car
there are up to two discrete network controllers on th
NIC 3.0 card.
- The Package Id [1] bit (Channel_ID[6]) is equal to the S
- The Package Id [0] bit (Channel_ID[5]) is equal to the S

n a Single Primary Connector



Updated 20180330-TN – Diagram copied into the 0v73 specification
Updated 20180409-TN – Diagram copied into the 0v73 specification
- Add quick switch that is tied to AUX_PWR_EN to prevent NC-SI leakage.

Updated 20180508b-TN – Diagrams copied into the 0v73 20180508b spec.
- Update SLOT_ID[1:0] implementation.

Updated 20180515a-TN – Diagrams copied into the 0v73 20180508b spec.
- Moved RBT isolation to baseboard side per OCP NIC 3.0 Working Session #18.
- RBT isolators controlled by a signal called RBT_ISOLATE# on the baseboard. Implementation determined by baseboard vendor. Must connect bus only after NIC_PWR_GOOD=0b1 indication from AUX Power Mode onwards.

Updated 20180525a-TN – Diagrams copied into the 0v74 20180525b spec.
- Update RBT Package ID[2:0] mapping as PackageID[2] – controller instance; PackageID[1:0] == SLOT_ID[1:0]

Updated 20180619a-TN – Diagrams copied into the 0v81 20180619a spec.
- SLOT_ID[1:0] buffering now on NIC side; add FRU EEPROM to diagram for clarity.

774 The Channel ID field comprises two subfields, Package ID and Internal Channel ID, as described in
775 Table 2.

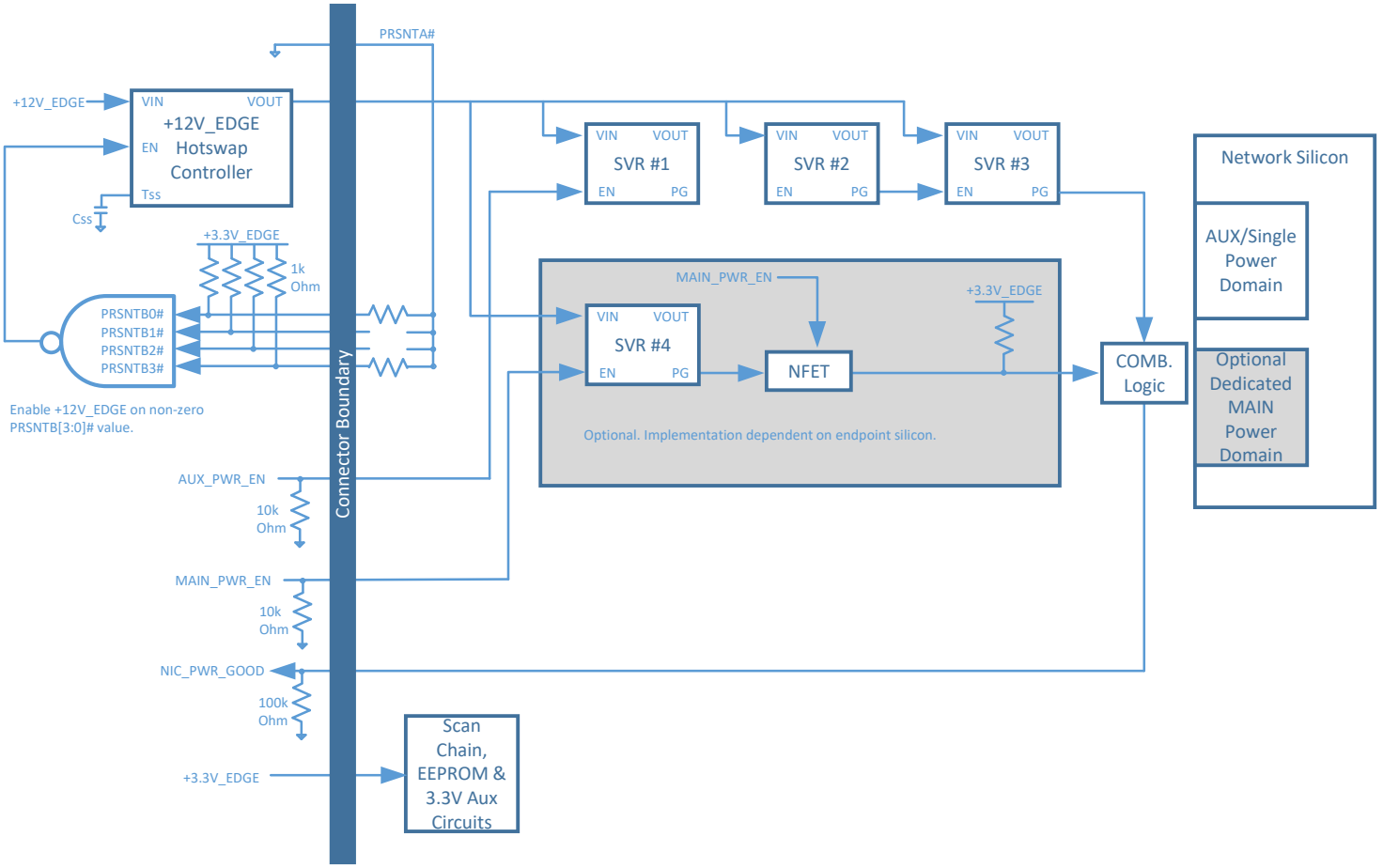
776 **Table 2 – Channel ID Format**

Bits	Field Name	Description
[7..5]	Package ID	The Package ID is required to be common across all channels within a single Network Controller that share a common NC-SI physical interconnect. The system integrator will typically configure the Package IDs starting from 0 and increasing sequentially for each physical Network Controller. The Network Controller shall allow the least significant two bits of this field to be configurable by the system integrator, with the most significant bit of this field = 0b. An implementation is allowed to have all 3 bits configurable.
[4..0]	Internal Channel ID	The Network Controller shall support Internal Channel IDs that are numbered starting from 0 and increasing sequentially for each Pass-through channel supported by the Network Controller that is accessible by the Management Controller through the NC-SI using NC-SI commands. An implementation is allowed to support additional configuration options for the Internal Channel ID as long as the required numbering can be configured. An Internal Channel ID value of 0x1F applies to the entire Package.

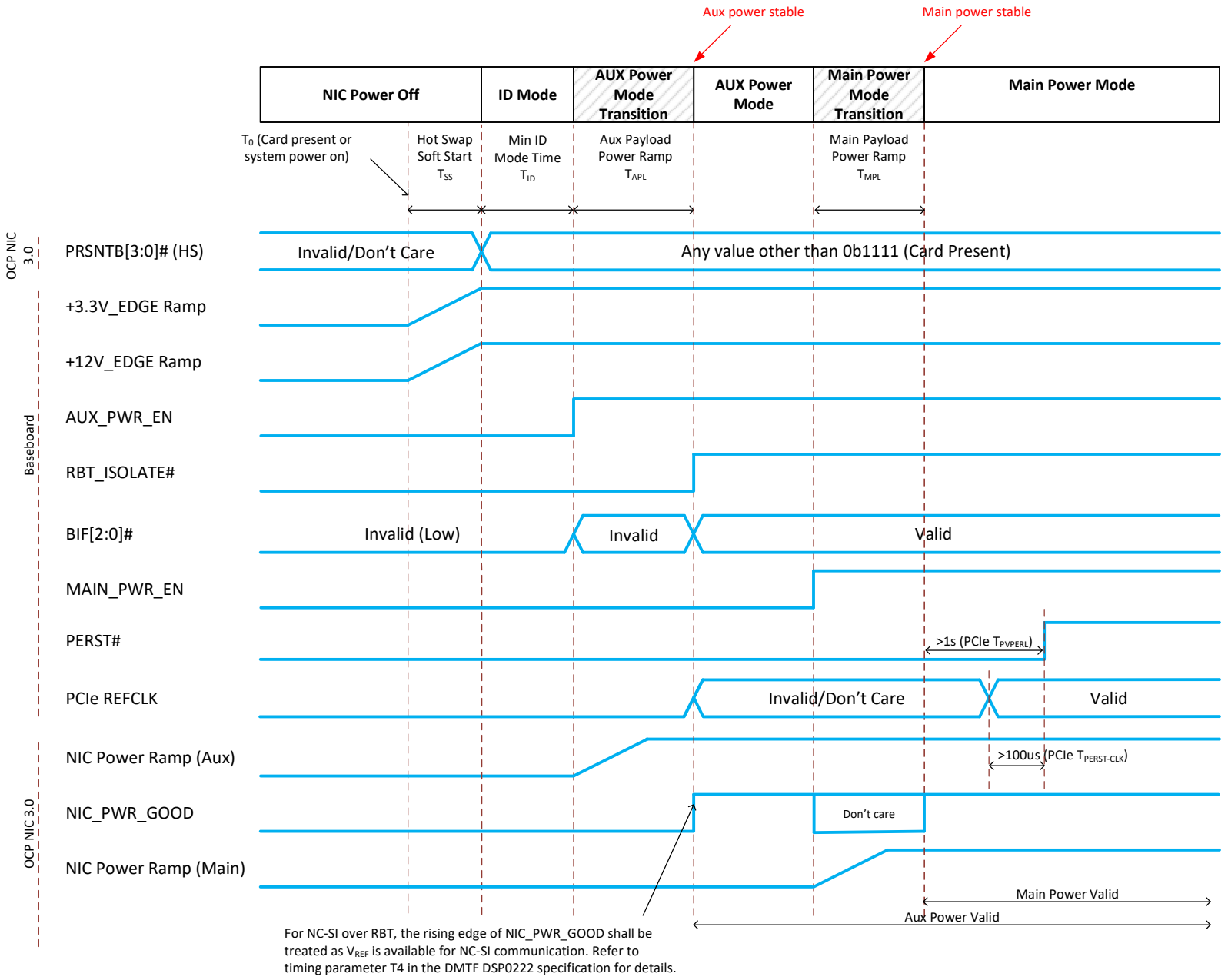
he Package ID is 3 bits
t is set to 0 per the DMTF
rable.
t on the card in the event
ollers on the same OCP

ual to the SLOT_ID1
ual to the SLOT_ID0

Baseboard Hot Plug Support Example



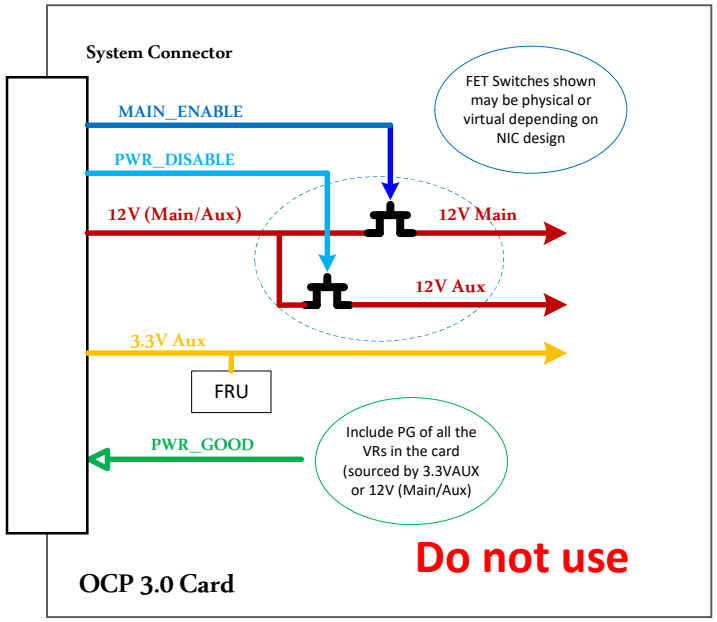
Updated 20180919-TN – Diagram copied into the 0v84 specification

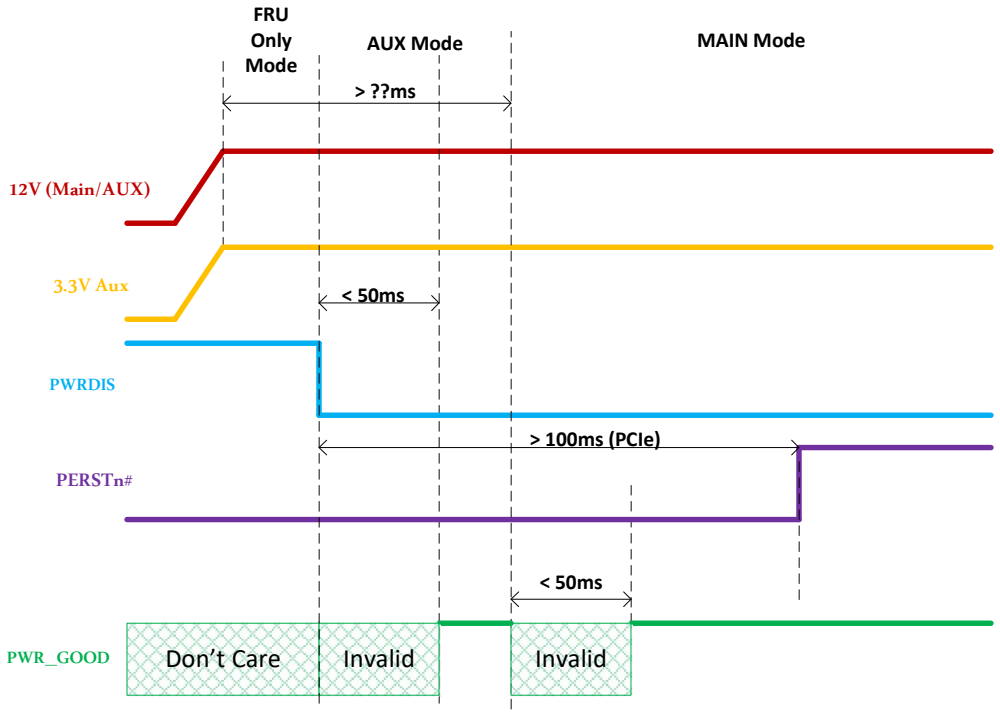


Change history:

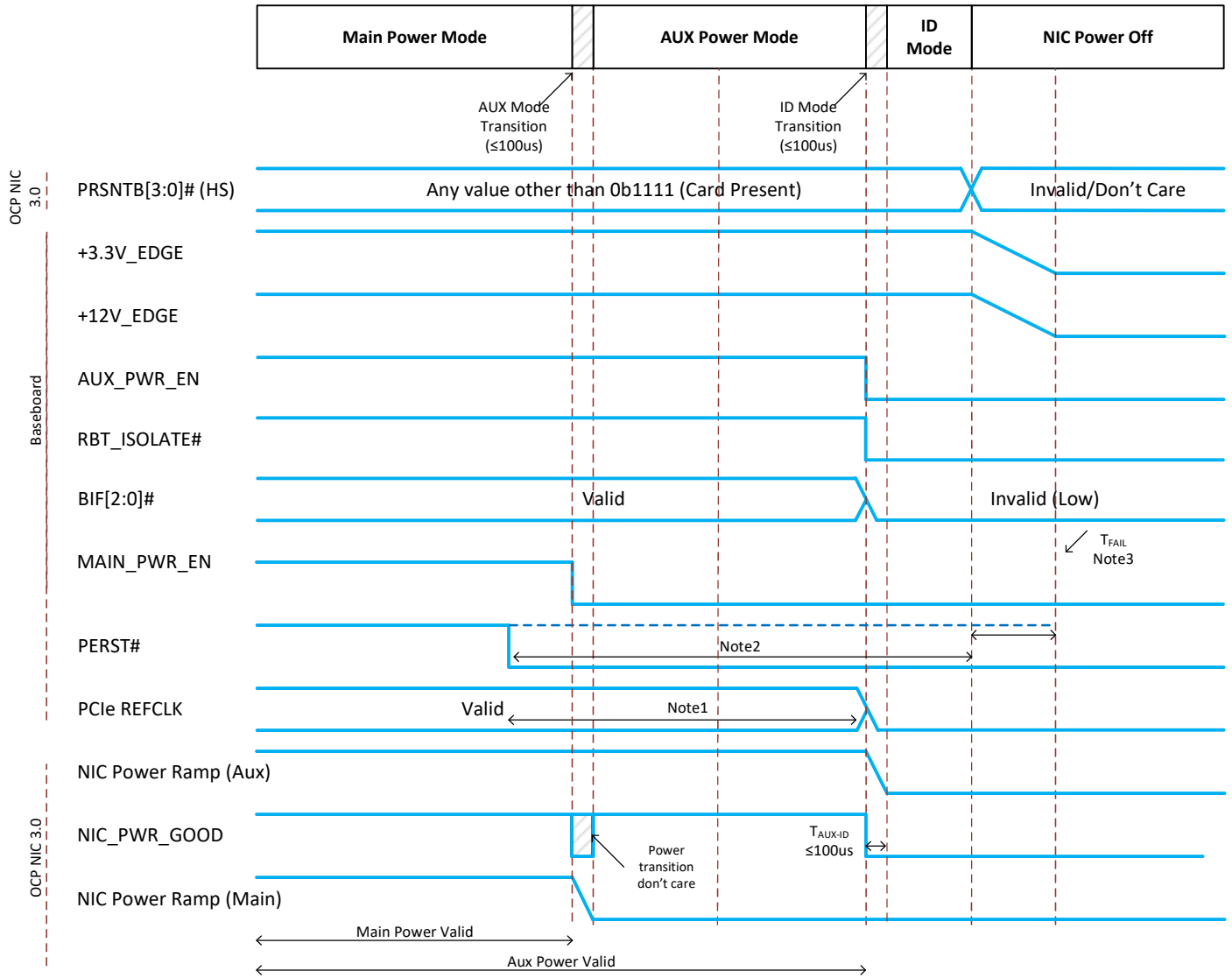
0v84 20180919 – Add RBT_ISOLATE# signal
0v84 20180926 – Changed BIF[2:0]# LOW prior to AUX_PWR_EN; add transition state prior to fully entering aux power mode.

Diagrams below from Jon Lewis. See updated diagrams in this Visio file





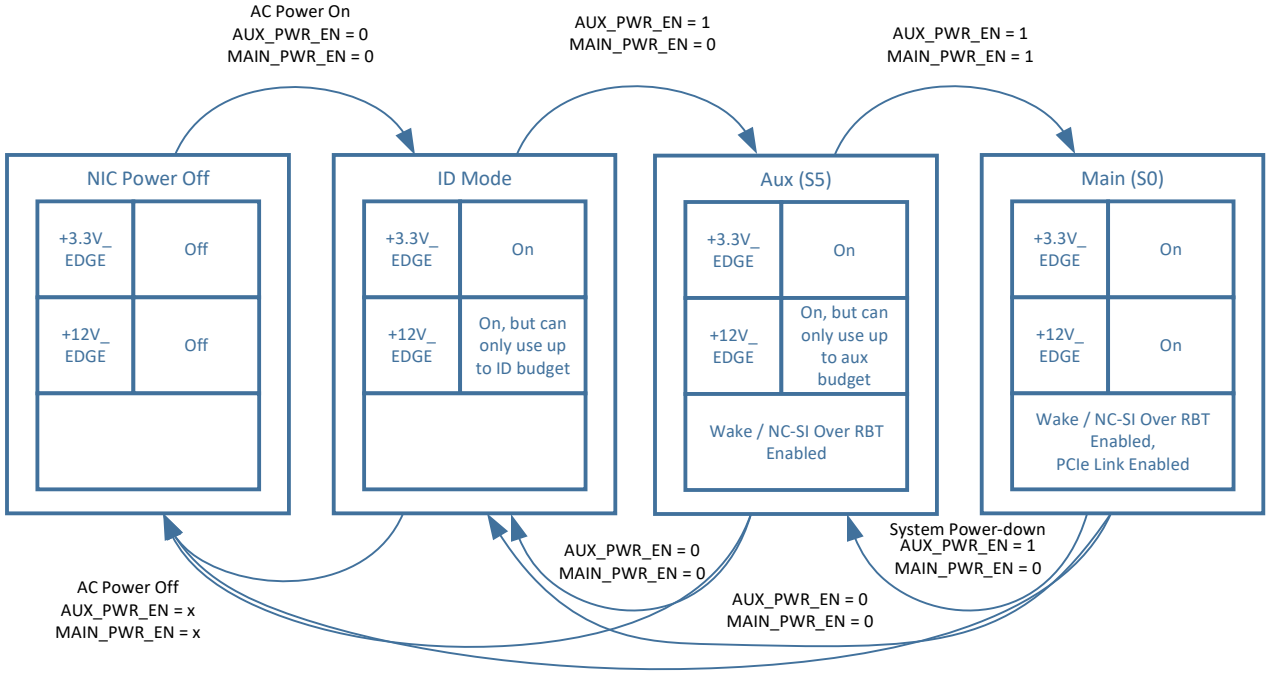
Updated 20180919-TN – Diagram copied into the 0v84 specification

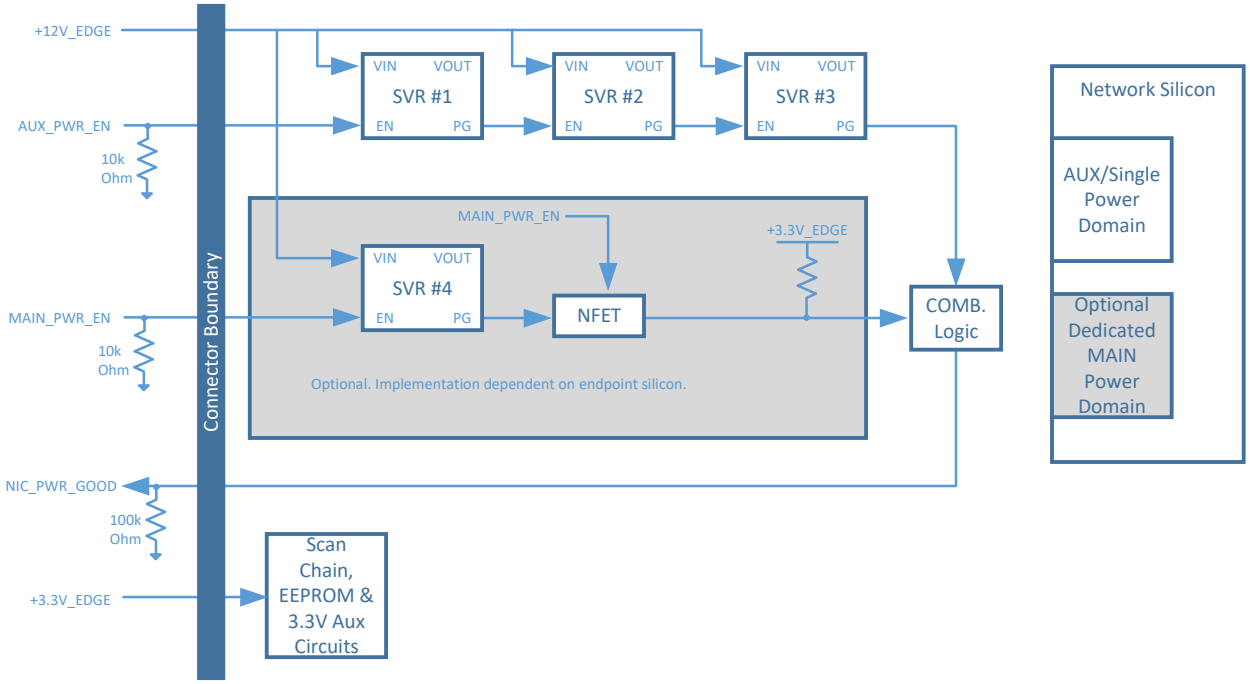


Note1: REFCLK go inactive after PERST# goes active. (PCIe CEM Section 2.2.3)
Note2: PERST# goes active before the power on the connector is removed. (PCIe CEM Section 2.2.3)
Note3: In the case of a surprise power down, PERST# goes active T_{FAIL} after power is no longer stable.

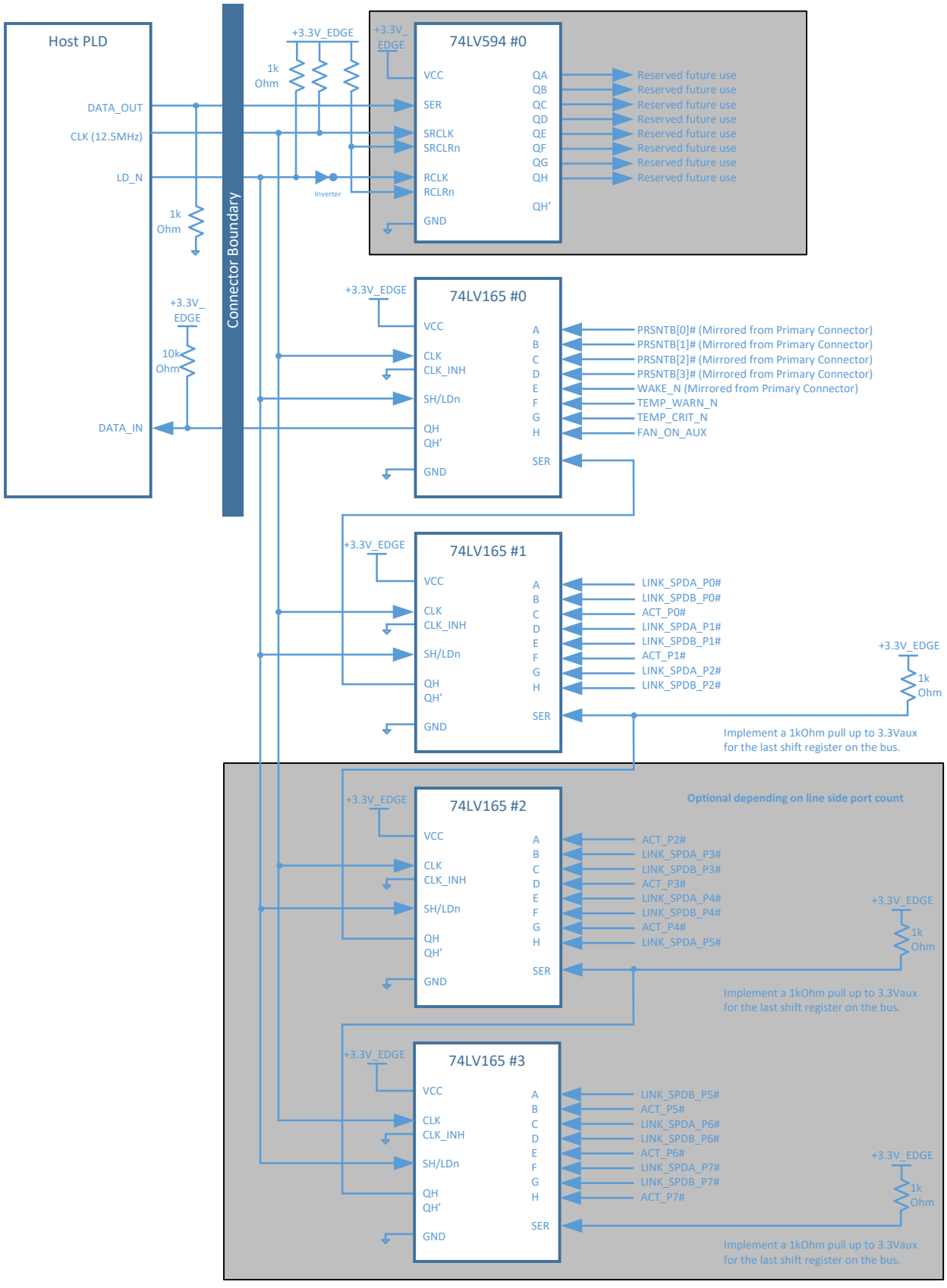
Change history:

0v84 20180919 – Add RBT_ISOLATE# signal
0v84 20180926 – Changed BIF[2:0]# to invalid (low) after AUX_PWR_EN deassertion.


AC Power On
AUX_PWR_EN = 0
MAIN_PWR_EN = 0
AUX_PWR_EN = 1
MAIN_PWR_EN = 0
AUX_PWR_EN = 1
MAIN_PWR_EN = 1
NIC Power Off
+3.3V_ EDGE
Off
+12V_ EDGE
Off
ID Mode
+3.3V_ EDGE
On
+12V_ EDGE
On, but can only use up to ID budget
Aux (S5)
+3.3V_ EDGE
On
+12V_ EDGE
On, but can only use up to aux budget
Wake / NC-SI Over RBT Enabled
Main (S0)
+3.3V_ EDGE
On
+12V_ EDGE
On
Wake / NC-SI Over RBT Enabled,
PCIe Link Enabled
AC Power Off
AUX_PWR_EN = x
MAIN_PWR_EN = x
AUX_PWR_EN = 0
MAIN_PWR_EN = 0
AUX_PWR_EN = 0
MAIN_PWR_EN = 0
System Power-down
AUX_PWR_EN = 1
MAIN_PWR_EN = 0


+12V_EDGE
AUX_PWR_EN
10k Ohm
MAIN_PWR_EN
10k Ohm
NIC_PWR_GOOD
100k Ohm
+3.3V_EDGE
Connector Boundary
VIN VOUT
SVR #1
EN PG
VIN VOUT
SVR #2
EN PG
VIN VOUT
SVR #3
EN PG
MAIN_PWR_EN
+3.3V_EDGE
VIN VOUT
SVR #4
EN PG
NFET
Optional. Implementation dependent on endpoint silicon.
COMB. Logic
Scan Chain, EEPROM & 3.3V Aux Circuits
Network Silicon
AUX/Single Power Domain
Optional Dedicated MAIN Power Domain

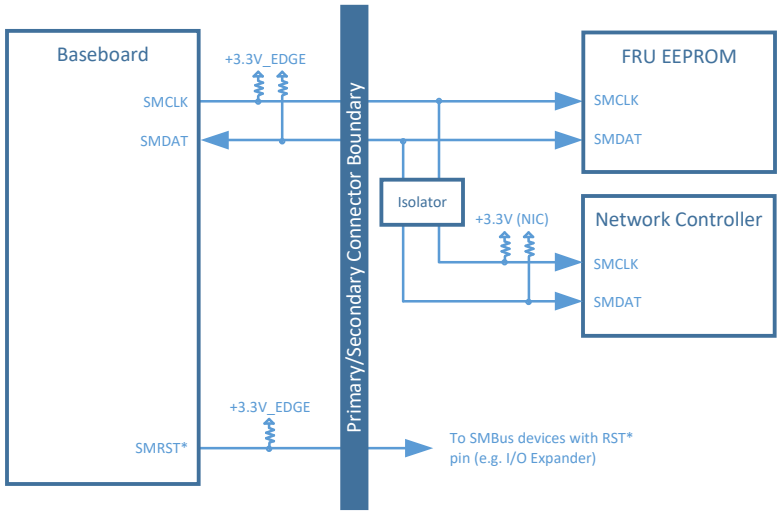
Updated 20180604b-TN – Diagram copied into the 0v74 specification

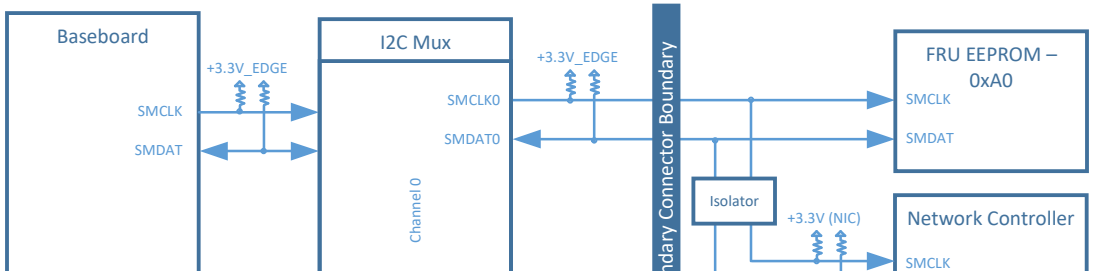


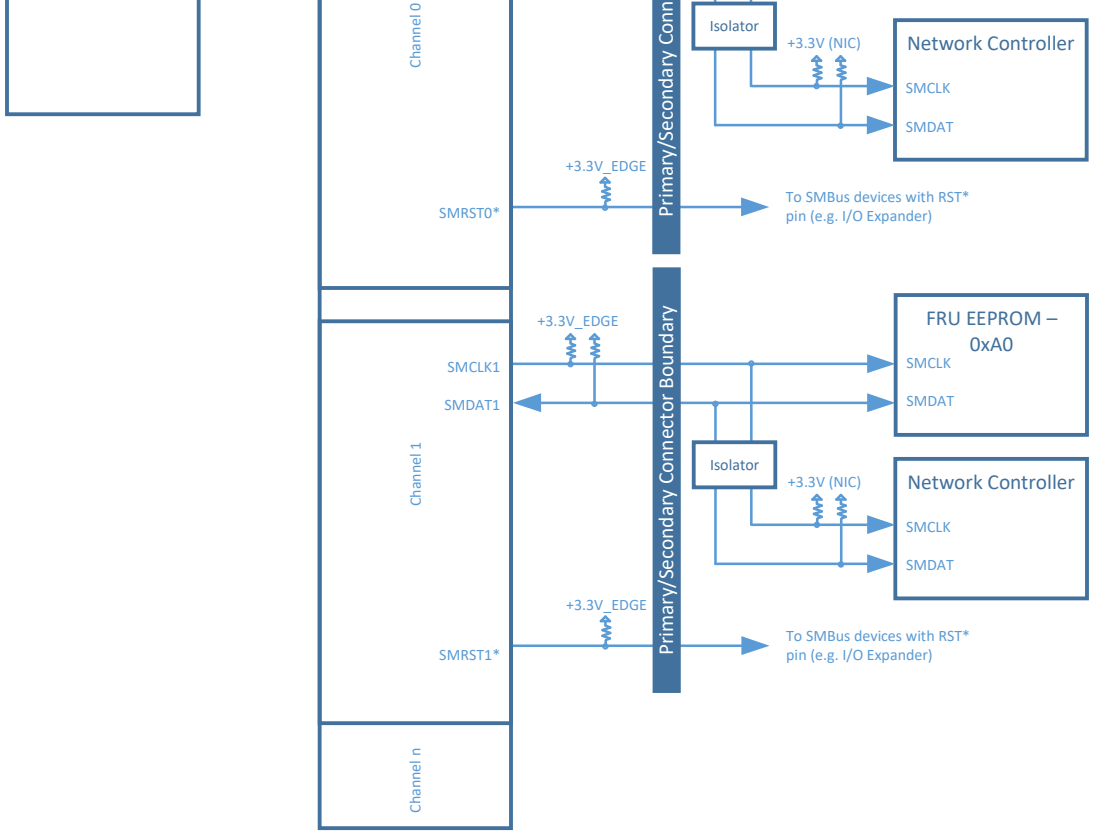
Shift registers 0 & 1 are mandatory for up to dual port applications.
Shift registers 2 & 3 are mandatory for up to quad port applications.
If both shift registers 2 & 3 are not used, add a 1kOhm pull up resistor to 3.3Vaux on the SER input of shift register 1.
If shift register 3 is not used, add a 1kOhm pull up resistor to 3.3Vaux on the SER input of shift register 2.
If all shift registers are used, add a 1kOhm pull up resistor to 3.3Vaux on the SER input of shift register 3.

Updated 20180507a-TN – Add DATA_OUT bit 0 definition for SLOT_ID1
Updated 20180508a-TN – Update LED bit ordering to optimize dual port applications
Updated 20180525b-TN – Remove SLOT_ID1 from DATA_OUT (pin redefined on OCP_A6)
Updated 20180604b-TN – LED ACT/LINK pins are active low. Updated names with "#"

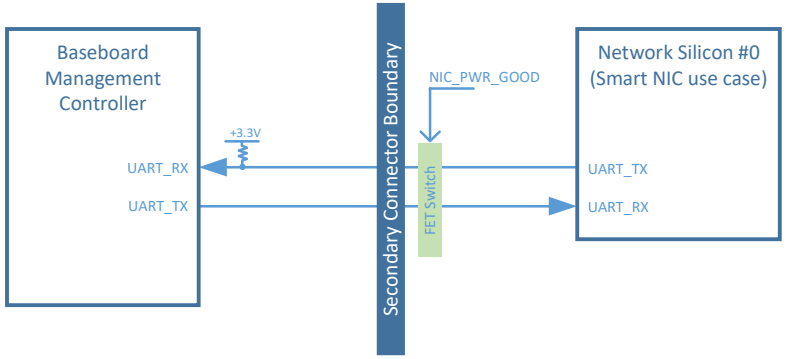
SMBus Connection Example






Channel 0
Primary/Secondary Connector Boundary
Isolator
+3.3V (NIC)
Network Controller
SMCLK
SMDAT
+3.3V_EDGE
SMRST0*
To SMBus devices with RST* pin (e.g. I/O Expander)
Channel 1
SMCLK1
SMDAT1
FRU EEPROM – 0xA0
SMRST1*
Channel n

UART Block diagram



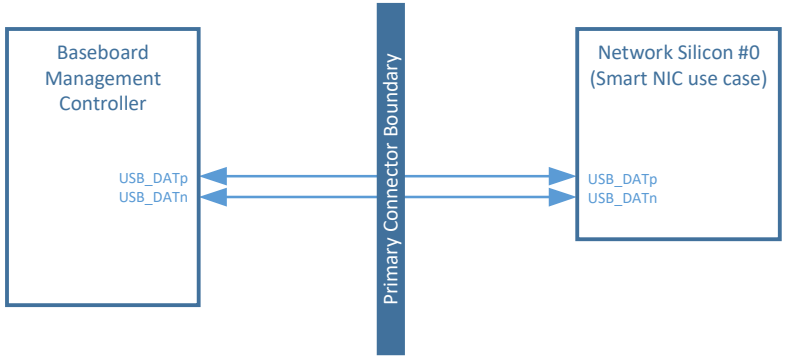
Updated 20180515b-TN – Diagrams copie
- Add UART

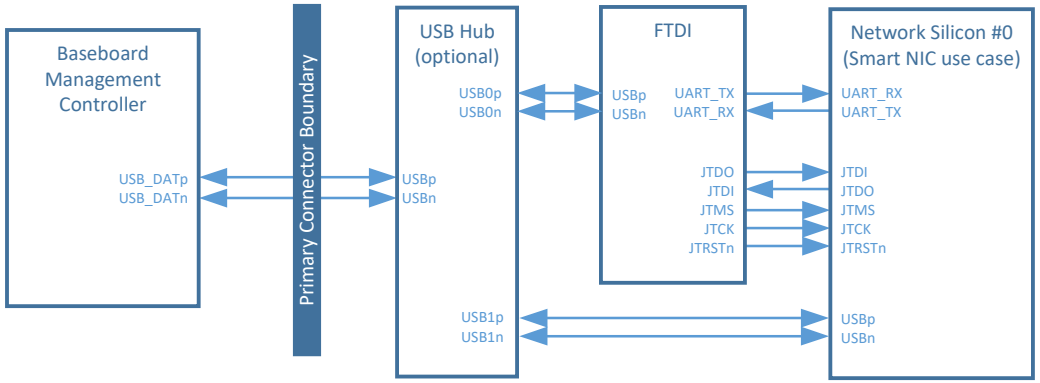
Updated 20180525b-TN – Diagrams copie
- Move UART buffer to the NIC side for c

ns copied into the 0v73 20180514a spec.

ns copied into the 0v74 20180525b spec.
de for cost burden.

USB 2.0 Block diagram





Updated 20180525b-TN – Diagrams copie
- Add USB 2.0 with buffer to the NIC side

Updated 20180705a-TN – Diagrams copie
- Add both diagrams to 0v81 since the US

USB hub optional. Used if multiple USB virtual interfaces are defined.

Connector Edge to USB may be direct of bus has a single target.
Use a USB hub if a target is an FTDI and USB.
No hub required for an FTDI implementation only (e.g. serial/JTAG)

ns copied into the 0v74 20180525b spec.
NIC side for cost burden.

ns copied into the 0v81 20180705b spec.
e the USB/serial addition has been approved by the WG.