

OCP NIC 3.0 Design Specification

Version 0.70

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1 Overview

1.1 License

As of January 23rd, 2018, the following persons or entities have made this Specification available under the Open Compute Project Hardware License (Permissive) Version 1.0 (OCPHL-P)

OCP NIC Subgroup

An electronic copy of the OCPHL-P is available at:

http://www.opencompute.org/assets/download/01-Contribution-Licenses/OCPHL-Permissive-v1.0.pdf

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1.2 Acknowledgements

The OCP NIC 3.0 specification was created under a collaboration from many OCP member companies, and facilitated by the OCP NIC Subgroup under the OCP Server Workgroup.

The OCP NIC Subgroup would like to acknowledge the following member companies for their contributions to the OCP NIC 3.0 specification:

Table 1: Acknowledgements – By Company

Amphenol Corporation

Broadcom Limited

Dell EMC

Facebook, Inc.

Hewlett Packard Enterprise

Lenovo Group Ltd

Mellanox Technologies, Ltd

Netronome Systems, Inc.

Quanta Computer Inc.

TE Connectivity Corporation

Intel Corporation

1.3 Background

The OCP NIC 3.0 specification is a follow-on to the OCP Mezz 2.0 rev 1.00 design specification. The OCP NIC 3.0 specification supports two basic card sizes: Small Card, and Large Card. The Small Card allows for up to 16 PCIe lanes on the card edge while the Large Card supports up to 32 PCIe lanes. Compared to the OCP Mezz Card 2.0 Design Specification, the updated OCP NIC 3.0 specification provides a broader solution space for the NIC and system vendors to support the following use case scenarios:

- NICs with a higher Thermal Design Power (TDP)
- Power delivery supports up to 80W to a single connector (Small) card, and up to 150W to a dual connector (Large) card
 - Note: Baseboard vendors need to evaluate if there is sufficient airflow to thermally cool the OCP NIC 3.0 card. Refer to Section 6 for additional details.
- Supports up to PCIe Gen5 on the baseboard and OCP NIC 3.0 card
- Support for up to 32 lanes of PCIe per OCP NIC 3.0 card
- Support for single host, multi-root complex, and multi-host environments
- Supports a greater board area for more complex OCP NIC 3.0 card designs
- Support for Smart NIC implementations with on-board DRAM and accelerators
- Simplification of FRU installation and removal while reducing overall down time

A representative Small Card OCP NIC 3.0 card is shown in Figure 1 and a representative Large Card is shown in Figure 2.

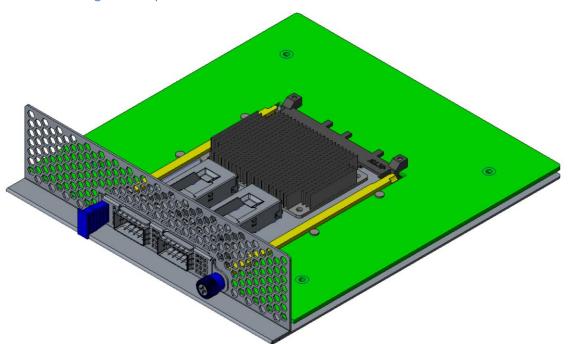


Figure 1: Representative Small OCP NIC 3.0 Card with Dual QSFP Ports

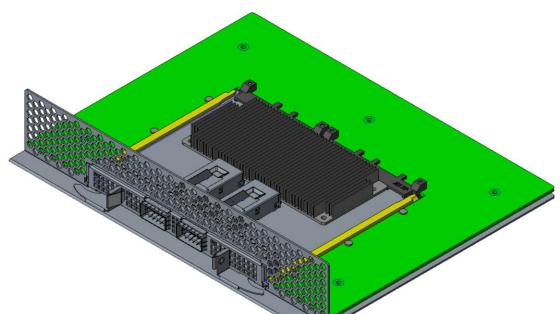


Figure 2: Representative Large OCP NIC 3.0 Card with Dual QSFP Ports and on-board DRAM

In order to achieve the features outlined in this specification, OCP NIC 3.0 compliant cards are not backwards compatible with OCP Mezz 2.0 cards.

This specification is created under OCP Server workgroup – OCP NIC subgroup. An electronic copy of this specification can be found on the Open Compute Project and the OCP Marketplace websites:

http://www.opencompute.org/wiki/Server/Mezz#Specifications_and_Designs

http://opencompute.org/products/specsanddesign?keyword=SPEC%2C+NIC

1.4 Overview

1.4.1 Mechanical Form factor overview

The OCP NIC 3.0 specification defines a third generation mechanical form factor that allows for interoperability between compliant baseboards and OCP NIC 3.0 cards.

OCP NIC 3.0 cards have two form factors – Small and Large. These cards are shown in Figure 3 below. The components shown in the figures are for illustrative purposes. The Small form factor card has one connector (Primary Connector) on the baseboard. The Large form factor card has one or two connectors (Primary Connector only and both the Primary and Secondary Connectors) on the baseboard.

Both the Primary and Secondary Connectors and card edge gold fingers are defined in and compliant to SFF-TA-1002. The Primary Connector is the "4C+" variant, the Secondary Connector is the "4C" version. On the OCP NIC 3.0 card side, the card edge is implemented with gold fingers. The Small Card gold finger area only occupies the Primary Connector area for up to 16 PCIe lanes. The Large Card gold finger area may occupy both the Primary and Secondary Connectors for up to 32 PCIe lanes, or optionally just the Primary Connector for up to 16 PCIe lane implementations.

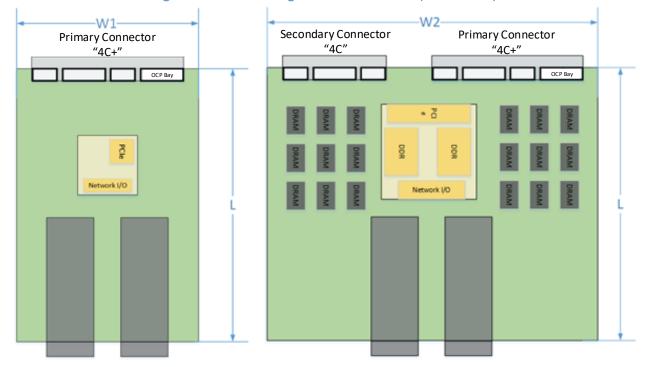


Figure 3: Small and Large Card Form-Factors (not to scale)

The two form factor dimensions are shown in Table 2.

Form Width Secondary Depth **Primary Typical Use Case** Factor Connector Connector "4C+" Small W1 = 76L = 115 N/A Low profile and NIC with a similar profile as an OCP NIC mm mm 168 pins 2.0 card; up to 16 PCle lanes. "4C+" "4C" W2 = 139Larger PCB width to support L = 115 Large mm mm 168 pins 140 pins additional NICs; up to 32 PCIe lanes.

Table 2: OCP 3.0 Form Factor Dimensions

The OCP NIC 3.0 design allows downward compatibility between the two card sizes. Table 3 shows the compatibility between the baseboard and NIC combinations. A Small size baseboard slot may only accept a small sized NIC. A Large size baseboard slot may accept a small or large sized NIC.

Baseboard	NIC Size / Supp	orted PCIe Width
Slot Size	Small	Large
Small	Up to 16 PCIe lanes	Not Supported
Large	Up to 16 PCIe lanes	Up to 32 PCIe lanes

Table 3: Baseboard to OCP NIC Form factor Compatibility Chart

There are two baseboard connector mounting options available for system designers: straddle mount and right angle (RA). The straddle mount connector option allows the OCP NIC and baseboard to exist in a co-planer position. To achieve this, a cutout exists on the baseboard and is defined in this specification. Alternatively, the right angle option allows the OCP NIC to be installed on top of the baseboard. A baseboard cutout is not required for the right angle connector. The right angle option allows the baseboard to use this area for additional routing or backside component placement. The straddle mount and right angle connectors are shown in Section 3.2.

For both the baseboard and OCP NIC 3.0 card, this specification defines the component and routing keep out areas. Refer to Section 2.5 for details.

Both the straddle mount and right angle implementations shall accept the same OCP NIC 3.0 card and shall be supported in the baseboard chassis regardless of the baseboard connector selection (right angle or straddle mount) so long as the baseboard slot and OCP NIC 3.0 card sizes are a supported combination as shown in Table 3.

This specification defines the form factor at the OCP NIC 3.0 card level, including the front panel, latching mechanism and card guide features.

More details about the card form-factor is shown in Section 2.

1.4.2 Electrical overview

This specification defines the electrical interface between baseboard and the OCP NIC 3.0 card. The electrical interface is implemented with a right angle or straddle mount connector on baseboard and gold finger on the OCP NIC 3.0 card. As previously noted in the mechanical overview, each card may implement a Primary Connector or Primary + Secondary Connector. Cards using only the Primary Connector are suitable for both the Small and Large form-factors and may support up to 16 lanes of PCIe. The Secondary Connector, when used in conjunction with the Primary Connector, allows Large form-factor implementations and may support up to 32 lanes of PCIe.

1.4.2.1 Primary Connector

The Primary Connector provides all OCP specific management functions as well as up to 16 lanes of PCIe between the OCP NIC and the system motherboard.

Management Function Overview (OCP Bay):

- DMTF DSP0222 1.1 compliant Network Controller Sideband Interface (NC-SI) RMII Based Transport (RBT) Physical Interface
- Power management and status reporting
 - o Power break for emergency power reduction
 - State change control
- Control / status serial bus
 - NIC-to-Host status
 - Port LED Link/Activity
 - Environmental Indicators
 - Host-to-NIC configuration Information
- Multi-host PCIe support signals (2x PCIe resets, 2x reference clocks)
 - The OCP bay provides PERST2#, PERST3#, REFCLK2 and REFCLK3. This enables support for up to four hosts when used in conjunction with PERST0#, PERST1#, REFCLK0 and REFCLK1 in the Primary 4C region.
- PCIe Wake signal

See Section 3.5 for a complete list of pin and function descriptions for the OCP Bay portion of the Primary Connector.

PCIe Interface Overview (4C Connector):

- 16x differential transmit/receive pairs
 - o Up to PCle Gen 5 support
- 2x 100 MHz differential reference clocks
- Control signals
 - o 2x PCIe Resets
 - Link Bifurcation Control
 - Card power disable/enable
- SMBus 2.0
- Power
 - o +12V EDGE

- +3.3V_EDGE
- o Power distribution between the aux and main power domains is up to the baseboard vendor

See Section 3.4 for a complete list of pin and function descriptions for the 4C+ connector.

1.4.2.2 Secondary Connector

The Secondary Connector provides an additional 16 lanes of PCIe and their respective control signals.

PCIe Interface Overview (4C Connector):

- 16x differential transmit/receive pairs
 - Up to PCle Gen 5 support
- 2x 100 MHz differential reference clocks
- Control signals
 - o 2x PCIe Resets
 - Link Bifurcation Control
 - o Card power disable/enable
- SMBus 2.0
- Power
 - o +12V_EDGE
 - o +3.3V EDGE
 - o Power distribution between the aux and main power domains is up to the baseboard vendor

See Section 3.4 for a complete list of pin and function descriptions for the 4C connector.

1.5 References

- DMTF Standard. *DSP0222, Network Controller Sideband Interface (NC-SI) Specification.* Distributed Management Task Force (DMTF), Rev 1.1.0, September 23rd, 2015.
- DMTF Standard. *DSP0222, Network Controller Sideband Interface (NC-SI) Specification.* Distributed Management Task Force (DMTF), Rev 1.2.0, Work-In-Progress.
- DMTF Standard. DSP0236, Management Component Transport Protocol (MCTP) Base Specification. Distributed Management Task Force (DMTF), Rev 1.3.0, November 24th, 2016.
- DMTF Standard. DSP0237, Management Component Transport Protocol (MCTP) SMBus/I2C
 Transport Binding Specification. Distributed Management Task Force (DMTF), Rev 1.1.0, May 21st, 2017.
- DMTF Standard. DSP0238, Management Component Transport Protocol (MCTP) PCIe VDM
 Transport Binding Specification. Distributed Management Task Force (DMTF), Rev 1.0.2, December 7th, 2014.
- DMTF Standard. DSP0239, MCTP IDs and Codes Specification. Distributed Management Task Force (DMTF), Rev 1.5.0, December 17th, 2017.
- DMTF Standard. DSP0240, Platform Level Data Model (PLDM) Base Specification. Distributed Management Task Force (DMTF), Rev 1.0.0, April 23rd, 2009.
- DMTF Standard. DSP0240, Platform Level Data Model (PLDM) over MCTP Binding Specification. Distributed Management Task Force (DMTF), Rev 1.0.0, April 23rd, 2009.
- DMTF Standard. DSP0245, Platform Level Data Model (PLDM) IDs and Codes Specification.
 Distributed Management Task Force (DMTF), Rev 1.2.0, November 24th, 2016.
- DMTF Standard. DSP0248, Platform Level Data Model (PLDM) for Platform Monitoring and Control Specification. Distributed Management Task Force (DMTF), Rev 1.1.1, January 10th, 2017.
- DMTF Standard. DSP0248, Platform Level Data Model (PLDM) State Sets Specification. Distributed Management Task Force (DMTF), Rev 1.0.0, March 16th, 2009.
- DMTF Standard. DSP0261, NC-SI over MCTP Binding Specification. Distributed Management Task Force (DMTF), Rev 1.2.0, August 26th, 2017.
- EDSFF. Enterprise and Datacenter SSD Form Factor Connector Specification. Enterprise and Datacenter SSD Form Factor Working Group, Rev 0.9 (draft), August 2nd 2017.
- IPMI Platform Management FRU Information Storage Definition, v1.2, February 28th, 2013.
- National Institute of Standards and Technology (NIST). *Special Publication 800-193, Platform Firmware Resiliency Guidelines*, draft, May 2017.
- NXP Semiconductors. I²C-bus specification and user manual. NXP Semiconductors, Rev 6, April 4th, 2014.
- Open Compute Project. OCP NIC Subgroup. Online. http://www.opencompute.org/wiki/Server/Mezz
- PCIe Base Specification. PCI Express Base Specification, Revision 4.0 Version 1.0, October 5th, 2017.
- PCIe CEM Specification. PCI Express Card Electromechanical Specification, Revision 4.0 (draft).
- SMBus Management Interface Forum. *System Management Bus (SMBus) Specification*. System Management Interface Forum, Inc, Version 2.0, August 3rd, 2000.
- SNIA. SFF-TA-1002, Specification for Protocol Agnostic Multi-Lane High Speed Connector. SNIA SFF TWG Technology Affiliate, Rev 1.1 draft, January 18th, 2018.

1.5.1 Trademarks

Names and brands may be claimed as trademarks by their respective companies.

2 Card Form Factor

2.1 Form Factor Options

OCP NIC 3.0 provides two fundamental form factor options: a Small Card (76mm x 115mm) and a Large Card (139mm x 115mm).

These form factors support a Primary Connector and optionally, a Secondary Connector. The Primary Connector is defined to be a SFF-TA-1002 compliant 4C+ connector. The 4C+ connector is a 4C complaint implementation plus a 28-pin bay for OCP NIC 3.0 specific pins. The Secondary Connector is the 4C connector as defined in SFF-TA-1002. The 4C specification supports up to 32 differential pairs for a x16 PCIe connection per connector. For host platforms, the 28-pin OCP bay is required for the Primary Connector. This is also mandatory for OCP NIC 3.0 cards.

The Small Card uses the Primary 4C+ connector to provide up to a x16 PCIe interface to the host. The additional 28-pin OCP bay carries sideband management interfaces as well as OCP NIC 3.0 specific control signals for multi-host PCIe support. The small size card provides sufficient faceplate area to accommodate up to 2x QSFP modules, 4x SFP modules, or 4x RJ-45 for BASE-T operation. The Small Card form factor supports up to 80W of delivered power to the card edge. An example Small Card form factor is shown in Figure 1.

The Large Card uses the Primary 4C+ connector to provide the same functionality as the Small Card along with an additional Secondary 4C connector to provide up to a x32 PCIe interface. The Large Card may utilize both the Primary and Secondary Connectors, or just the Primary Connector for lower PCIe lane count applications. Table 4 summarizes the Large Card permutations. The Large Card supports higher power envelopes and provides additional board area for more complex designs. The Large Card form factor supports up to 150W of delivered power to the card edge across the two connectors. An example Large Card form factor is shown in Figure 2.

For Large Cards, implementations may use both the Primary and Secondary Connector (as shown in Figure 4), or may use the Primary Connector only (as shown in Figure 5) for the card edge gold fingers.

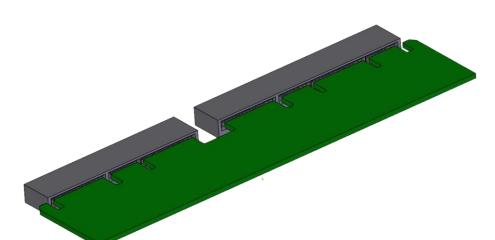


Figure 4: Primary Connector (4C+) and Secondary Connector (4C) (Large) OCP NIC 3.0 Cards

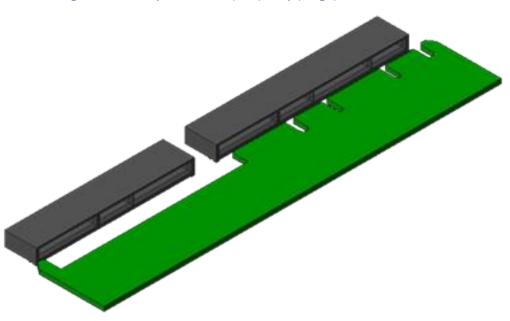


Figure 5: Primary Connector (4C+) Only (Large) OCP NIC 3.0 Cards

For both form-factors, an OCP NIC 3.0 card may optionally implement a subset of pins to support up to a x8 PCIe connection. This is implemented using a 2C card edge per SFF-TA-1002. The Primary Connector may support a 2C sized OCP NIC 3.0 card along with the 28 pin OCP bay shown in the 4C+ drawings. The following diagram from the SFF-TA-1002 specification illustrates the supported host Primary and Secondary Connectors and OCP NIC 3.0 card configurations.

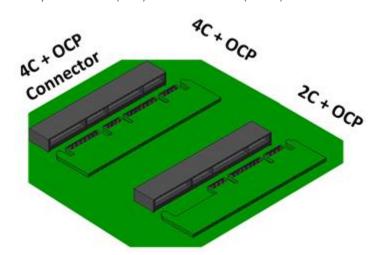


Figure 6: Primary Connector (4C+) with 4C and 2C (Small) OCP NIC 3.0 Cards

Table 4 summarizes the supported card form factors. Small form factors cards support the Primary Connector and up to 16 PCIe lanes. Large form factor cards support implementations with both the Primary and Secondary Connectors and up to 32 PCIe lanes, or a Primary Connector only implementation with up to 16 PCIe lanes.

Table 4: OCP NIC 3.0 Card Definitions

Add in Card Size and	Secondary Connector		Prir	mary Connector	
max PCIe Lane Count	4C Connect	or, x16 PCle	4C+ Connect	tor, x16 PCle	OCP Bay
Small (x8)				2C+	OCP Bay
Small (x16)			40	C+	OCP Bay
Large (x8)				2C+	OCP Bay
Large (x16)			40	C+	OCP Bay
Large (x24)		2C	40	C+	OCP Bay
Large (x32)	4	·C	40	C+	OCP Bay

2.2 I/O bracket

The following section defines the standard I/O bracket and standard chassis opening required for both the Small and Large form-factor cards.

2.2.1 Small Form Factor OCP NIC 3.0 Card I/O Bracket

Figure 7 and Figure 8 shows the standard Small Card form factor I/O bracket with a thumbscrew and pull tab assembly.



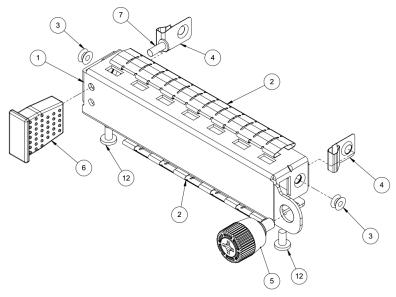


Figure 8: Small Card Standard I/O Bracket with Thumbscrew and Pulltab (2D View)

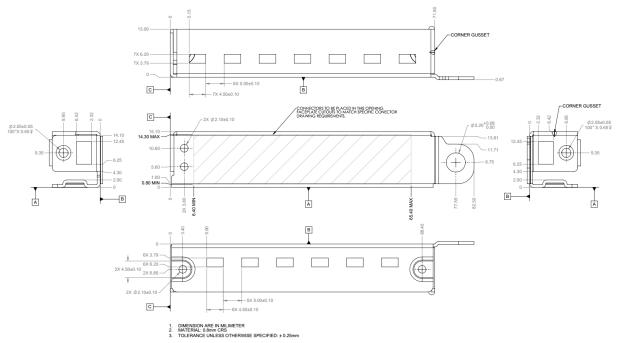


Figure 9 and Figure 10 shows the standard Small Card form factor I/O bracket with a latching lever assembly

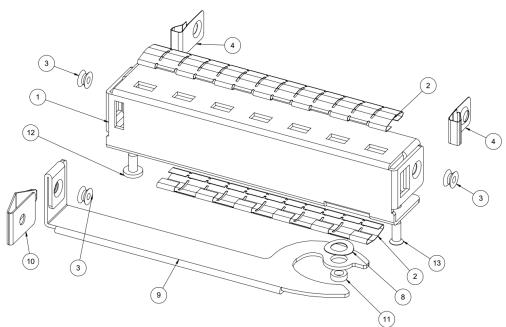


Figure 9: Small Card Generic I/O Bracket with a Latching Lever (3D View)

Figure 10: Small Card Generic I/O Bracket with a Latching Lever (2D View)

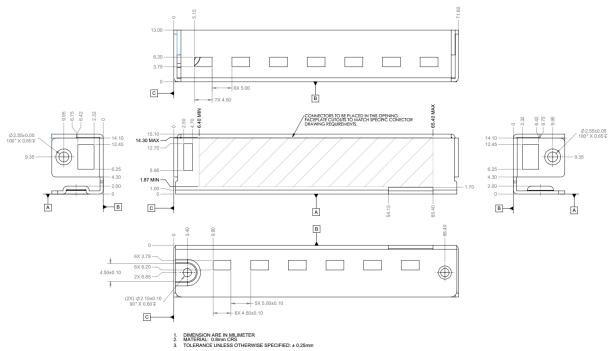


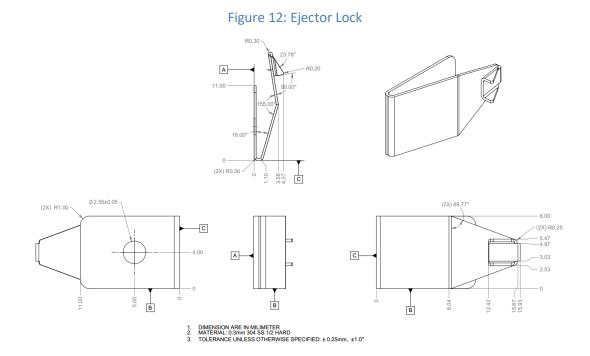
Figure 11 shows the Small Card form factor ejector lever.

R150

R150
R

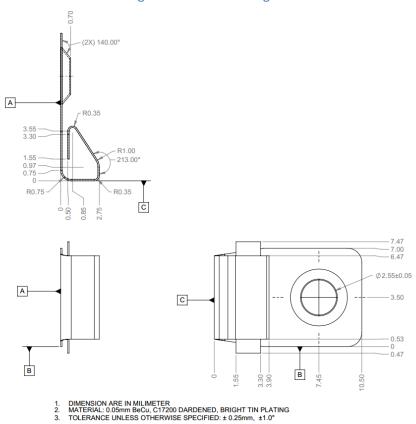
Figure 11: Small Card Ejector Lever (2D View)

The Small Card ejector uses a locking mechanism at the end of the handle to retain the lever position. This is shown in Figure 12.



The side EMI finger is defined in Figure 13. The top and bottom EMI fingers are commercial off the shelf components and are listed in the mechanical BOM in Table 5.

Figure 13: Side EMI Finger



3. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.25mm, ±1.0°

In addition to the sheet metal, Table 5 lists the additional hardware components used for the Small Card assembly.

Table 5: Mechanical BOM for the Small Card Assembly

Item#	Item description	Supplier Part Number
1 Bracket S		See Figure 8 and Figure 10.
		NIC_OCPv3_SFF_Bracket_1tab_20180124.pdf
		NIC_OCPv3_SFF_Bracket_latch_20180124.pdf
2	Top and bottom EMI fingers	TF187VE32F11
3	Rivet	1-AC-2421-03_2.4x2.1
4	Side EMI Finger	See Figure 13 and drawing
		NIC_OCPv3_sideEMI_20180124.pdf
5	Thumbscrew	J-4C-99-343-KEEE_rev04
6	Pull Tab	TBD TBD
7	Screw for securing pull tab (M2 x 5mm)	ICTB0D200509B-ZD01
8	Ejector Compression Washer	TBD
9	Ejector Handle	See Figure 11 and drawing
		NIC_OCPv3_EjectorHandle_20180124.pdf
10	Ejector lock	See Figure 12 and drawing
		NIC_OCPv3_EjectorLock_20180124.pdf
11	Ejector Bushing	TBD

12	Screw (used for attaching backet to NIC)	FCMMQ200503N
13	Screw (used for attaching bracket and	ICMMAJ200403N3
	ejector to NIC)	
14	SMT Nut (on NIC)	82-950-22-010-01-RL

Note: The "Pull Tab" shown in the 3D drawings and in Table 5 are tentative. Alternate designs are under evaluation and therefore the BOM may change in the next revision of the specification.

Figure 14 shows the thumbscrew + pull tab assembly and Figure 15 shows the card assembly with the ejector.

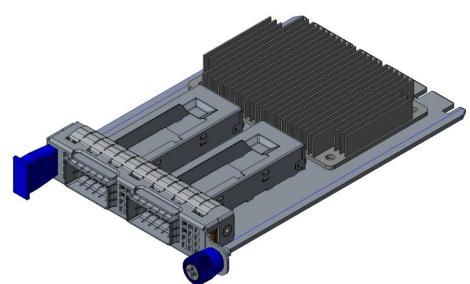
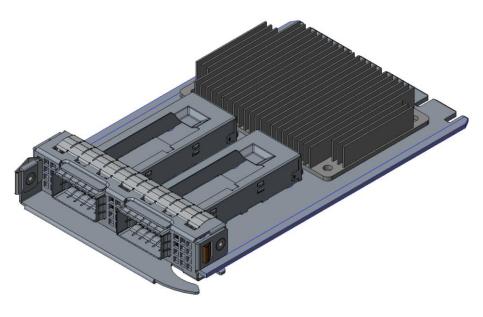


Figure 14: Small Card Assembly (Thumbscrew + Pull Tab Version)





Note: The OCP NIC 3.0 card supplier shall add port identification on the bracket that meet their manufacturing and customer requirements.

2.2.2 Small Form Factor OCP NIC 3.0 Card with Thumbscrew Critical-to-Function (CTF) Dimensions

The following dimensions are considered critical-to-function (CTF) for each small form factor OCP NIC 3.0 card with thumbscrew. The CTF default tolerances are shown in Table 6.

Table 6: CTF Default Tolerances

CTF DEFAULT TOLERANCES		
DIMENSION RANGE	TOLERANCE	
	TWO PLACE DECIMALS: X.XX	
LINEAR:	± 0.30	
ANGULAR:	± 1.00 DEGREES	
HOLE DIAMETER:	± 0.13	

Figure 16: Small Form Factor OCP NIC 3.0 Card with Thumbscrew CTF Dimensions (Top View)

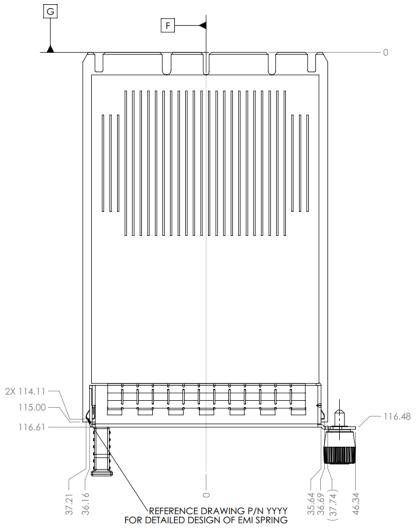


Figure 17: Small Form Factor OCP NIC 3.0 Card with Thumbscrew CTF Dimensions (Front View)

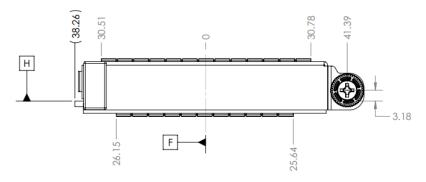
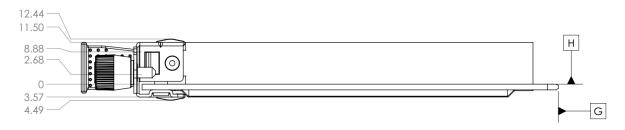


Figure 18: Small Form Factor OCP NIC 3.0 Card with Thumbscrew CTF Dimensions (Side View)



2.2.3 Small Form Factor OCP NIC 3.0 Card with Ejector Latch Critical-to-Function (CTF) Dimensions

The following dimensions are considered critical-to-function (CTF) for each small form factor OCP NIC 3.0 card with ejector latch. The CTF default tolerances are shown in Table 7.

Table 7: CTF Default Tolerances

CTF DEFAULT TOLERANCES		
DIMENSION RANGE	TOLERANCE	
	TWO PLACE DECIMALS: X.XX	
LINEAR:	± 0.30	
ANGULAR:	± 1.00 DEGREES	
HOLE DIAMETER:	± 0.13	

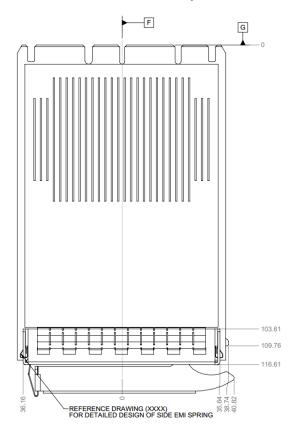


Figure 19: Small Form Factor OCP NIC 3.0 Card with Ejector CTF Dimensions (Top View)

Figure 20: Small Form Factor OCP NIC 3.0 Card with Ejector CTF Dimensions (Front View)

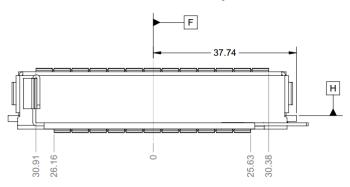
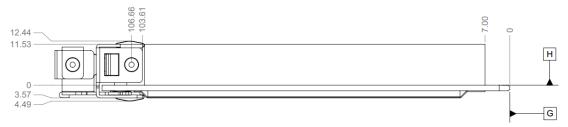


Figure 21: Small Form Factor OCP NIC 3.0 Card with Ejector CTF Dimensions (Side View)



2.2.4 Small Form Factor OCP NIC 3.0 Baseboard Critical-to-Function (CTF) Dimensions

The following dimensions are considered critical-to-function (CTF) for each small form factor baseboard chassis.

Figure 22: Small Form Factor Baseboard Chassis CTF Dimensions (Rear View)

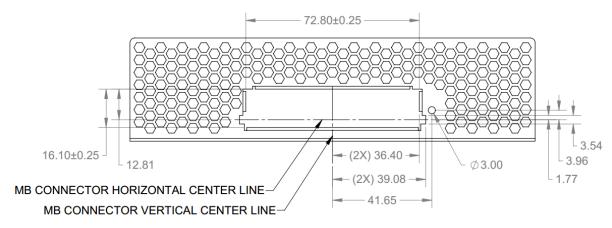


Figure 23: Small Form Factor Baseboard Chassis to Card Thumb Screw CTF Dimensions (Side View)

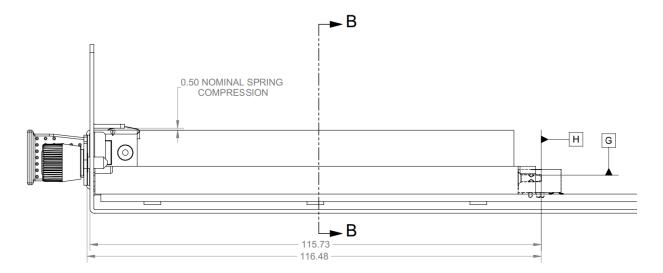


Figure 24: Small Form Factor Baseboard Chassis to Ejector lever Card CTF Dimensions (Side View)

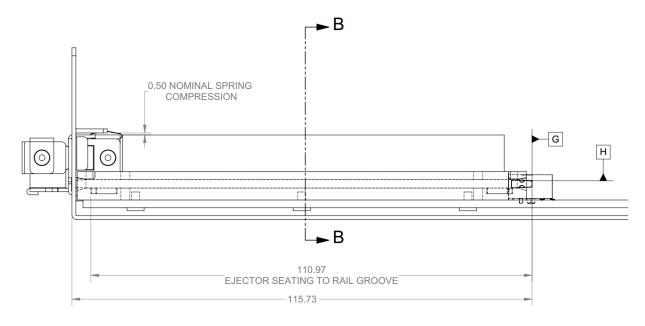


Figure 25: Small Form Factor Baseboard Chassis CTF Dimensions (Rear Rail Guide View)

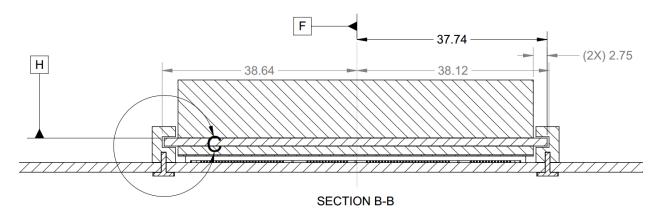
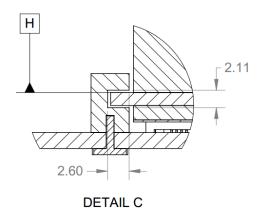


Figure 26: Small Form Factor Baseboard Chassis CTF Dimensions (Rail Guide Detail) - Detail C



Card guides are identical between the Small and Large form factor cards. The card guide 3D CAD packages may be downloaded from the OCP NIC 3.0 Wiki site: http://www.opencompute.org/wiki/Server/Mezz.

2.2.5 Large Form Factor OCP NIC 3.0 Card I/O Bracket

Figure 27 and Figure 28 shows the standard Large Card form factor I/O bracket with ejector levers.

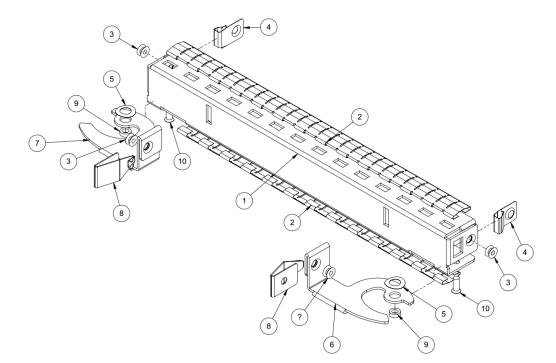


Figure 27: Large Card I/O Bracket with Ejector (3D View)

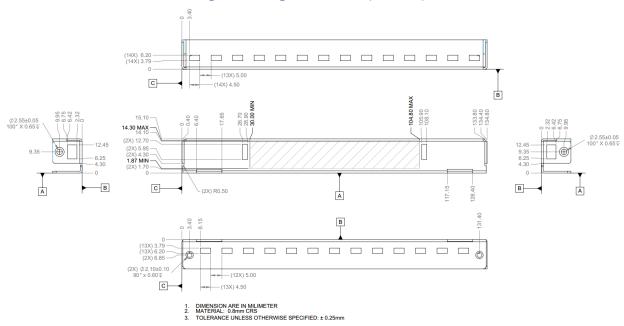


Figure 28: Large I/O Bracket (2D View)

The left and right ejector handles for the Large Card standard I/O bracket are shown in Figure 29 and Figure 30.

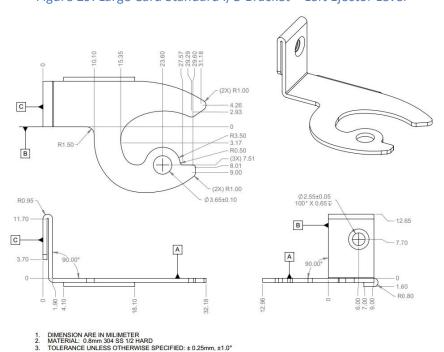


Figure 29: Large Card Standard I/O Bracket – Left Ejector Lever

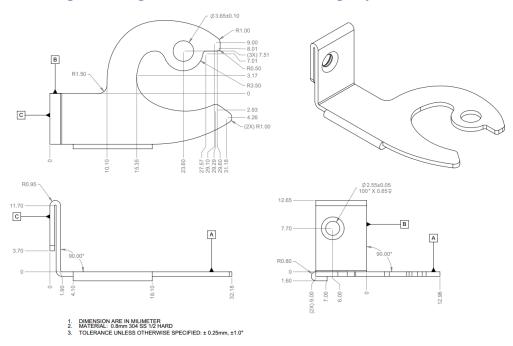


Figure 30: Large Card Standard I/O Bracket – Right Ejector Lever

In addition to the sheet metal, Table 8 lists the additional hardware components used for the Small Card bracket assembly.

Item#	Item description	Supplier Part Number
1	Bracket	See Figure 28 & Drawing:
		NIC_OCPv3_LFF_Bracket_latch_20180124.pdf
2	Top and bottom EMI fingers	TF187VE32F11
3	Rivet	1-AC-2421-03_2.4x2.1
4	Side EMI Finger	See Figure 13 from Small Card & Drawing
		NIC_OCPv3_sideEMI_20180124.pdf
5	Ejector Compression Washer	TBD TBD
6	Ejector Lever – Left	See Figure 29 & Drawing
		NIC_OCPv3_EjectorLever_Left_20180124.pdf
7	Ejector Lever – Right	See Figure 30 & Drawing
		NIC_OCPv3_EjectorLever_Right_20180124.pdf
8	Ejector Lock	See Figure 12 from Small Card & Drawing
		NIC_OCPv3_EjectorLock_20180124.pdf
9	Ejector Bushing	TBD
10	Screw (for attaching bracket & ejector to	ICMMAJ200403N3
	NIC)	
11	SMT Nut (on NIC)	82-950-22-010-01-RL

Table 8: Mechanical BOM for the Large Card Assembly

Figure 31 shows a dual QSFP assembly and Figure 32 shows a quad SFP assembly on the OCP NIC 3.0 card.

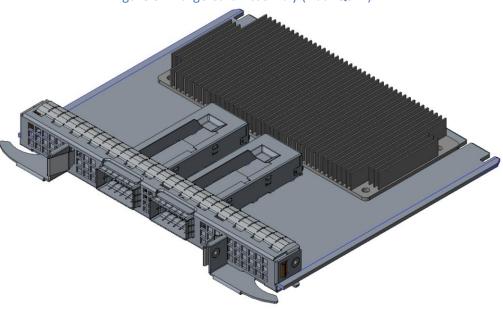
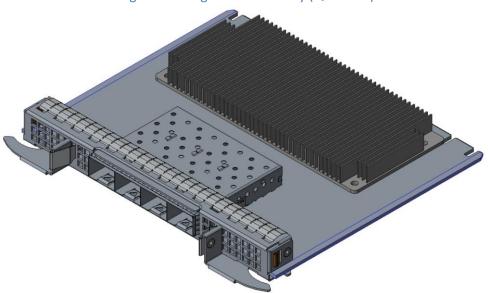


Figure 31: Large Card Assembly (Dual QSFP)





Note: The OCP NIC 3.0 card supplier shall add port identification on the bracket that meet their manufacturing and customer requirements.

2.2.6 Large Form Factor OCP NIC 3.0 Card Critical-to-Function (CTF) Dimensions

The following dimensions are considered critical-to-function (CTF) for each large form factor OCP NIC 3.0 card.

Table 9: CTF Default Tolerances

CTF DEFAULT TOLERANCES		
DIMENSION RANGE	TOLERANCE	
	TWO PLACE DECIMALS: X.XX	
LINEAR:	± 0.30	
ANGULAR:	± 1.00 DEGREES	
HOLE DIAMETER:	± 0.13	

Figure 33: Large Form Factor OCP NIC 3.0 Card with Ejector CTF Dimensions (Top View)

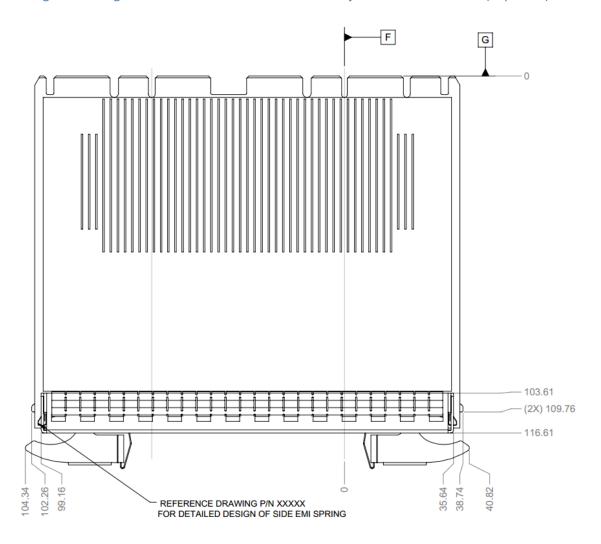


Figure 34: Large Form Factor OCP NIC 3.0 Card with Ejector CTF Dimensions (Front View)

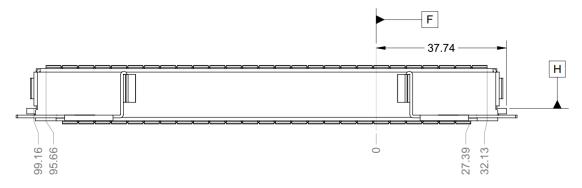
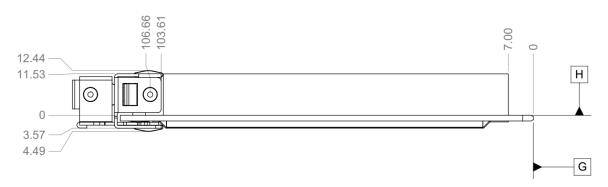


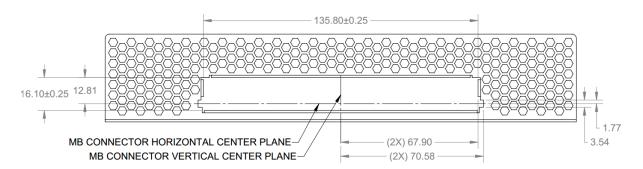
Figure 35: Large Form Factor OCP NIC 3.0 Card with Ejector CTF Dimensions (Side View)



2.2.7 Large Form Factor OCP NIC 3.0 Baseboard Critical-to-Function (CTF) Dimensions

The following dimensions are considered critical-to-function (CTF) for each large form factor baseboard chassis.

Figure 36: Large Form Factor Baseboard Chassis CTF Dimensions (Rear View)



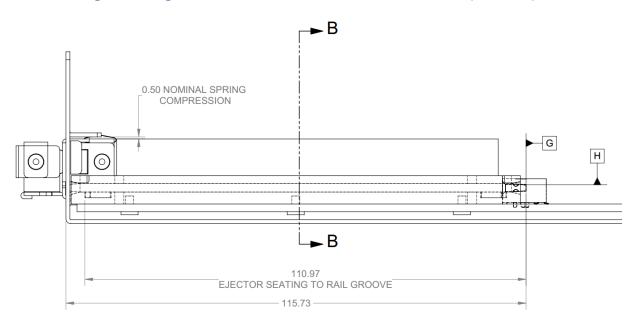


Figure 37: Large Form Factor Baseboard Chassis CTF Dimensions (Side View)

Figure 38: Large Form Factor Baseboard Chassis CTF Dimensions (Rail Guide View)

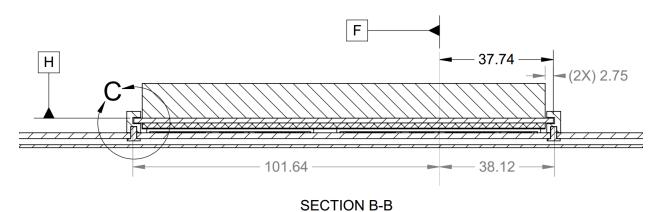
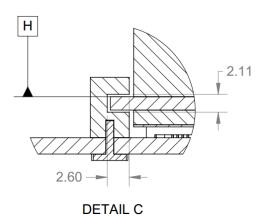


Figure 39: Large Form Factor Baseboard Chassis CTF Dimensions (Rail Guide – Detail C)



Card guides are identical between the Small and Large form factor cards. The card guide 3D CAD packages may be downloaded from the OCP NIC 3.0 Wiki site: http://www.opencompute.org/wiki/Server/Mezz.

2.3 Line Side I/O Implementations

At the time of this writing, the Small and Large form-factor implementations have been optimized to support the following standard line side I/O implementations:

Form Factor	Max Topology Connector Count		
Small	2x QSFP+/QSFP28/QSFP56		
Small	4x SFP28+/SFP28/SFP56		
Small	4x RJ-45		
Large	2x QSFP+/QSFP28/QSFP56		
Large	4x SFP+/SFP28/SFP56		
Large	4x RJ-45		

Table 10: OCP NIC 3.0 Line Side I/O Implementations

Note: For brevity, references to QSFP+, QSFP28 and QSFP56 shall be referred to as QSFP for the remainder of this document. Similarly, references to SFP+, SFP28 and SFP56 shall be referred to as SFP.

Additional combinations and connector types are permissible as I/O form-factor technologies and thermal capabilities evolve.

2.4 Port Numbering and LED Implementations

The OCP NIC 3.0 I/O bracket shall provide port labeling for user identification.

Additionally, LEDs shall be implemented on the OCP NIC 3.0 I/O bracket when there is sufficient space for local indication. LEDs may also be implemented on the card Scan Chain (as defined in Section 3.5.3) for remote link/activity indication on the baseboard. These two cases are described in the sections below. In both cases, the actual link rate may be directly queried through the management interface.

2.4.1 OCP NIC 3.0 Port Naming and Port Numbering

The naming of all OCP NIC 3.0 external ports shall start from Port 0. When viewing the OCP NIC 3.0 card from the I/O side and with the primary side components facing up, Port 0 shall be located on the left hand side. The port numbers shall sequentially increase to the right. Refer to Figure 40 as an example implementation.

2.4.2 OCP NIC 3.0 Card LED Configuration

For low I/O count small form-factor cards without built in light pipes (such as 1x QSFP, 2x SFP, or 2x RJ-45), or a large form-factor cards, where additional I/O bracket area is available, the card shall implement on-board link/activity indications in place of the Scan Chain LED stream. The recommended local (on-card) LED implementation uses two physical LEDs (a discrete Link/Activity LED and a bi-colored Speed A/Speed B LED). Table 11 describes the OCP NIC 3.0 card LED implementations.

Table 11: OCP NIC 3.0 Card LED Configuration with Two Physical LEDs per Port

LED Pin	LED Color	Description
Link /	Green	Active low. Multifunction LED.
Activity		This LED shall be used to indicate link and link activity.
		When the link is up and no link activity is present, then this LED shall be lit and solid. This indicates that the link is established, there are no local or remote faults, and the link is ready for data packet transmission/reception.
		When the link is up and there is link activity, then this LED should blink at the interval of 50-500ms during link activity.
		The Link/Activity LED shall be located on the left hand side or located on the top for each port when the OCP NIC 3.0 card is viewed in the horizontal plane.
Speed	Green	Active low. Bicolor multifunction LED.
	Amber Off	The LED is Green when the port is linked at its maximum speed. The LED is Amber when the port is linked at it second highest speed. The LED is off when the device is linked at a speed lower than the second highest capable speed, or no link is present.
		The Amber Speed LED indicator may be used for port identification through vendor specific link diagnostic software.
		The bicolor speed LED shall be located on the right hand side or located on the bottom for each port when the OCP NIC 3.0 card is viewed in the horizontal plane.

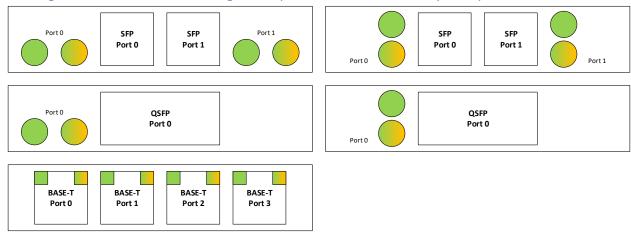
2.4.3 OCP NIC 3.0 Card LED Ordering

For all OCP NIC 3.0 card use cases, each port shall implement the green Link/Activity LED and a bicolor green/amber speed A/B LED.

When the OCP NIC 3.0 card is viewed from the horizontal position, and with the primary component side facing up, the Link/Activity LED shall be located on the left side for each port and the speed LED shall be located on the right side for each port. The port ordering shall increase from left to right.

The placement of the Link/Activity and Speed LEDs on the faceplate may be left up to the discretion of the OCP NIC 3.0 card designer. The LED port association shall be clearly labeled on the OCP NIC 3.0 card.

Figure 40: Port and LED Ordering - Example Small Card Link/Activity and Speed LED Placement



Note: The example port and LED ordering diagrams shown in Figure 40 are viewed with the card in the horizontal position and the primary side is facing up.

2.4.4 Baseboard LEDs Configuration over the Scan Chain

A small form-factor OCP NIC 3.0 with a fully populated I/O bracket (2x QSFP, 4x SFP or 4x RJ-45) does not have sufficient space for discrete on-board (faceplate) LED indicators. In this case, the line side link and activity LED indicators are implemented on the baseboard system via the Scan Chain. The Scan Chain bit stream is defined in Section 3.5.3.

The baseboard LED implementation uses two discrete LEDs – Link/Activity and Speed indication. The physical baseboard LED implementation is left up to the baseboard vendor and is not defined in this specification. The LED implementation is optional for baseboards.

At the time of this writing, the Scan Chain definition allows for up to one link/activity and one speed LED per port. A total of up to 8 ports are supported in the Scan Chain. The bit stream defines the LEDs to be active low (on). The Scan Chain LED implementation allows the NIC LED indicators to be remotely located on the OCP NIC 3.0 compliant chassis (e.g. front LED indicators with rear I/O cards).

2.5 Mechanical Keep Out Zones

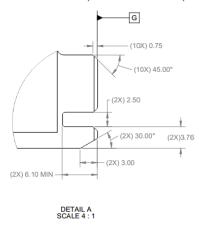
2.5.1 Small Card Form Factor Keep Out Zones

CONNECTOR KEEP IN ZONE REPRESENT MAXIMUM CONNECTOR BODY SIZE, NOTINCLUDING GROUDING FINGERS. CONNECTOR PROTRUSION -COMPONENT AND TRACE FREE AREA, TOP & BOTTOM LAYERS, TRACE PERMITTED ON INTERNAL LAYERS UP TO 1.0MM MAX FROM PCB EDGE FROM PCB EDGE 115.00 G CONNECTOR KEEP IN. SMT COMPONENT PERMITTED 1MM EDGE KEEPOUT (2x)109.76 - 104.00 MAX -7.00 MIN -⊕ 2.75 MIN REFERENCE SFF-TA-1002 CONNECTOR SPEC 29.51 MAX 76.00 65.00 32.24 lacktriangledown(2X) Ø5.50 — PLATED PAD FOR GROUNDING (2X) \emptyset $3.20^{+0.08}_{0.00}$ PTH -COMPONENT KEEP IN COMPONENT AND TRACE FREE AREA, TOP & BOTTOM LAYERS. TRACE PERMITTED ON INTERNAL LAYERS UP TO 1.0MM MAX FROM PCB EDGE

Figure 41: Small Form Factor Keep Out Zone - Top View



TOLERANCE UNLESS OTHERWISE SPECIFIED: ±0.13, ±1.0°



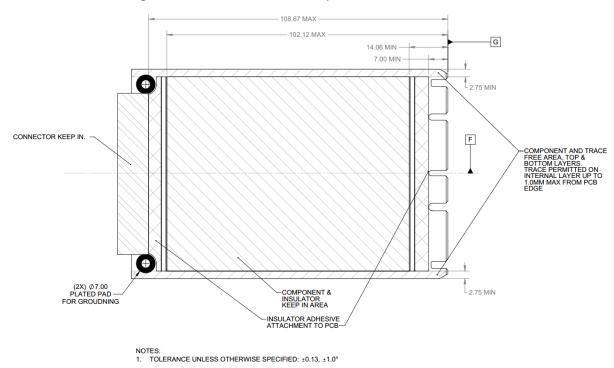
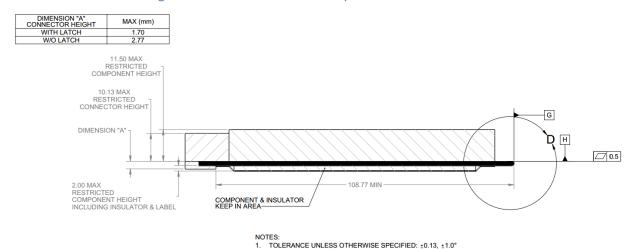


Figure 43: Small Form Factor Keep Out Zone – Bottom View

Figure 44: Small Form Factor Keep Out Zone – Side View



G Н ┌ 1.57 (2X) 0.62 -(2X)30.00° -INSULATOR DETAIL D SCALE 4:1

Figure 45: Small Form Factor Keep Out Zone - Side View - Detail D

2.5.2 Large Card Form Factor Keep Out Zones

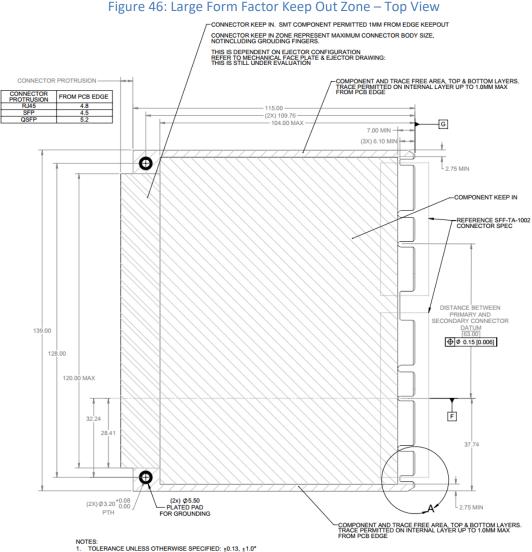


Figure 46: Large Form Factor Keep Out Zone – Top View



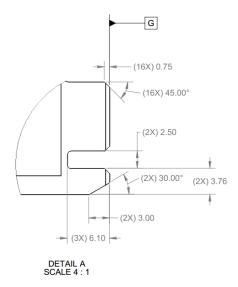
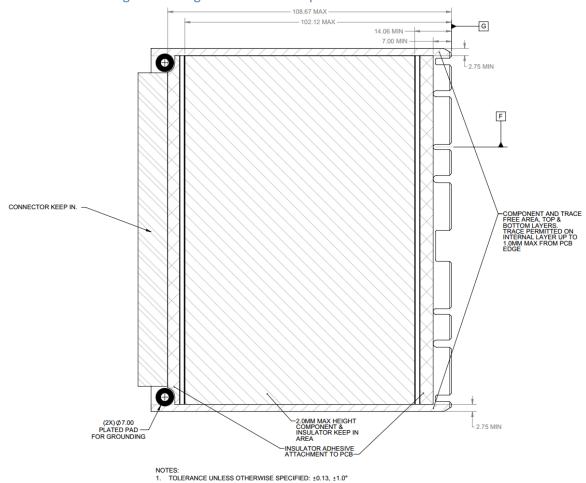


Figure 48: Large Form Factor Keep Out Zone – Bottom View



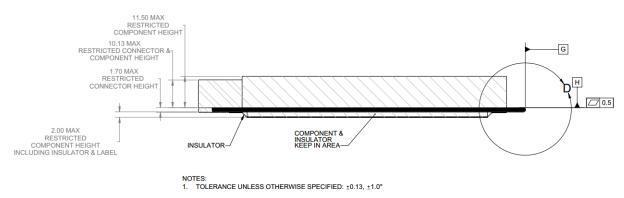
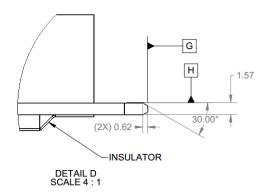


Figure 49: Large Form Factor Keep Out Zone – Side View

Figure 50: Large Form Factor Keep Out Zone - Side View - Detail D



2.5.3 Baseboard Keep Out Zones

Refer to the 3D CAD files for the baseboard keep out zones for both the Small and Large Card form factor designs. The 3D CAD files are available for download on the OCP NIC 3.0 Wiki: http://www.opencompute.org/wiki/Server/Mezz

2.6 Insulation Requirements

All OCP NIC 3.0 cards shall implement an insulator to prevent the bottom side card components from shorting out to the baseboard chassis. The recommended insulator thickness is 0.25mm and shall reside within the following mechanical envelope for the Small and Large size cards.

Small Card Insulator

Figure 51: Small Card Bottom Side Insulator (3D View)

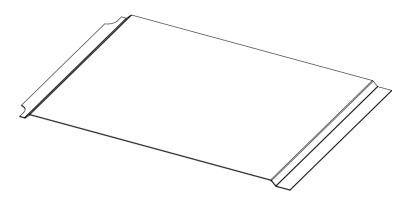


Figure 52: Small Card Bottom Side Insulator (Top and Side View)

- DIMENSION ARE IN MILIMETER
 MATERIAL: FORMEX GK-10BK 0.25mm THICKNESS
- ADHESIVE 3M 467MP 0.05mm THICKNESS TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.30mm, ±1.0°
- С 101.67 (2X) R3.70 (2X) 98.93 88.06 (2X) 6.40 70.50 В (2X) 5.00 (2X) 2.06-2.00 MAX -ADHESIVE SURFACE BOTTOM SIDE C

2.6.2 Large Card Insulator

Figure 53: Large Card Bottom Side Insulator (3D View)

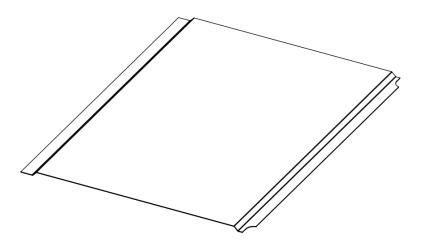
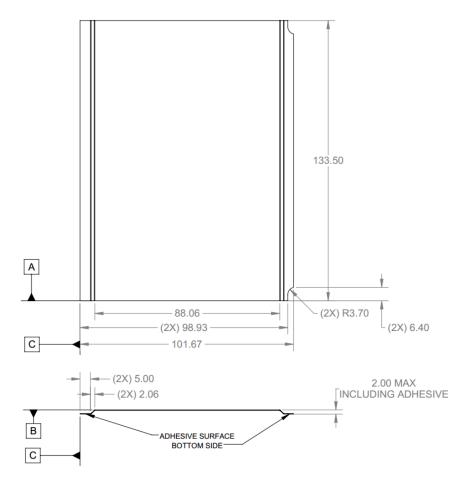


Figure 54: Large Card Bottom Side Insulator (Top and Side View)

- DIMENSION ARE IN MILIMETER
 MATERIAL: FORMEX GK-10BK 0.25mm THICKNESS
- ADHESIVE 3M 467MP 0.05mm THICKNESS
- TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.30mm, ±1.0°



2.7 Labeling Requirements

OCP NIC 3.0 cards shall implement all (or a subset of) label items listed below as deemed necessary by each customer. All labels shall be placed on the secondary side of the insulator and within their designated areas or zones.

There are four label areas for the OCP NIC 3.0 cards:

- Serial Number Labels
- Part Number Labels
- MAC Labels
- Regulatory Labels

Note: regulatory marks may printed on the insulator instead of affixed via a label.

Additional labels can be placed on the primary side or on the PCB itself. This is up to the NIC vendor(s) to find the appropriate location(s) within each label zone.

2.7.1 General Guidelines

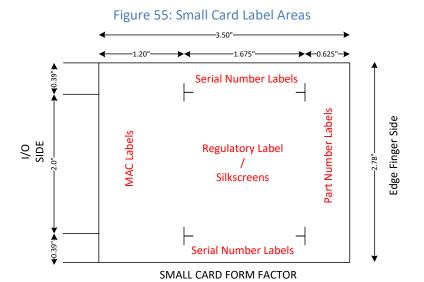
Each board shall have a unique label for identification. The label information shall be both in human readable and machine readable formats (linear or 2D data matrix). The label may include:

- Serial number
- Date Code
- Manufacturing Site Code

The label size and typeface may vary based on each customer's label content and requirements. The following sections show representative label examples for each label area.

2.7.2 Small Card Label Areas

Small form factor OCP NIC 3.0 card labels shall be placed in the indicated areas below.



http://opencompute.org

2.7.3 Large Card Label Areas

Large form factor OCP NIC 3.0 card labels shall be placed in the indicated areas below.

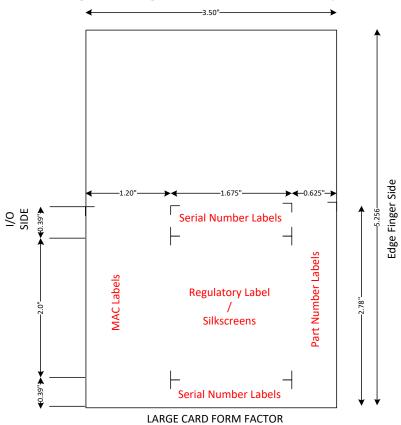


Figure 56: Large Card Label Placement Example

2.7.4 NIC Vendor Factory Label Example

An example NIC vendor factory label is shown in Figure 57.

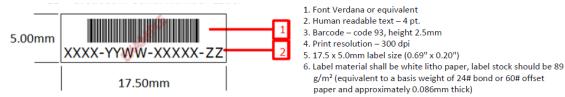
1. Verdana 4 pt. font or equivalent
2. Barcode – code 128
3. 300 DPI printer minimum. Must meet the contrast and print growth requirements per ISO/IES 16022 and have a print quality level of "C" or higher per ISO/IEC 15415
4. 1.000" x 0.400" label size, corner radius 0.025" – 0.100" (0.635mm – 2.54mm)
5. Material: Polyester with acrylic adhesive
6. Color: White
7. Thickness: 0.05mm

Figure 57: NIC Vendor Factory Label Example

2.7.5 NIC Vendor Serial Number Label Example

An example NIC vendor serial number label is shown in Figure 58.

Figure 58: NIC Vendor Serial Number Label Example



2.7.6 Baseboard MAC and Serial Number Label Example

An example baseboard MAC and serial number label is shown in Figure 59.

Figure 59: Baseboard MAC and Serial Number Label Example



2.7.7 Regulatory Label Example

An example regulatory label is shown in Figure 60. The regulatory markings information may be directly printed on to the insulator.

Figure 60: OCP NIC 3.0 Card Regulatory Label Example



- 1. Verdana 4.5 pt. font or equivalent
- 2. All logo heights are 5mm
- 300 DPI printer minimum. Must meet the contrast and print growth requirements per ISO/IES 16022 and have a print quality level of "C" or higher per ISO/IEC 15415
- 4. 1.500" x 0.750" (35mm 19mm) label size, corner radius 0.025" 0.100" (0.635mm 2.54mm)
- 5. Material: Polyester with acrylic adhesive
- 6. Color: White
- 7. Thickness: 0.05mm

2.7.8 System Vendor Part Number Label Example

An example system vendor part number label is shown in Figure 61.

Figure 61: System Vendor Part Number Label Example



- 1. Font Verdana or equivalent
- 2. Human readable text 6 pt.
- 3. Barcode code 93, height 6.0 mm
- 4. Print resolution 300 dpi
- 5. 18.0mm x 10.0mm label size (0.7" x 0.375")
- 6. Label material shall be white litho paper, label stock should be 89 $\,$ g/m 2 (equivalent to a basis weight of 24# bond or 60# offset paper and approximately 0.086mm thick)
- 7. The area occupied by the human readable text and barcode should be visually aligned to the center of the label. This alignment is for reference only, but must facilitate 100% scanning capability. See example below.

2.7.9 NIC Vendor Part Number Label Example

An example NIC vendor part number label is shown in Figure 62.

Figure 62: OCP NIC 3.0 Card Vendor Part Number Label



- 1. Font Verdana or equivalent
- 2. Human readable text 6 pt.
- 3. Barcode code 93, height 6.0 mm
- 4. Print resolution 300 dpi
- 5. 18 mm x 10 mm label size (0.7" x 0.375")
- 6. Label material shall be white litho paper, label stock should be 89 g/m² (equivalent to a basis weight of 24# bond or 60# offset paper and approximately 0.086mm thick)
- 7. The area occupied by the human readable text and barcode should be visually aligned to the center of the label. This alignment is for reference only, but must facilitate 100% scanning capability. See example below.

2.8 NIC Implementation Examples

Typical OCP NIC 3.0 implementation examples are included in the 3D CAD package. The purpose of these examples is to demonstrate the implementation feasibility. Additional use cases beyond the implementation examples are possible as long they adhere to the OCP NIC 3.0 specification.

Note: For brevity, references to QSFP+, QSFP28 and QSFP56 shall be referred to as QSFP in this document. Similarly, references to SFP+, SFP28 and SFP56 shall be referred to as SFP.

The 3D CAD files may be obtained from the OCP NIC 3.0 Wiki: http://www.opencompute.org/wiki/Server/Mezz

Implementation Example 3D CAD File name Small form factor Single/Dual QSFP ports 01 nic v3 sff2q 1tab asm.stp 01 nic v3 sff2q latch asm.stp Small form factor Single/Dual SFP ports N/A Small form factor Quad SFP ports 01 nic v3 sff4s 1tab asm.stp 01 nic v3 sff4s latch asm.stp Small form factor Quad 10GBASE-T ports 01 nic v3 sff4r 1tab asm.stp 01_nic_v3_sff4r_latch_asm.stp 01 nic v3 lff2q asm.stp Large form factor Single/Dual QSFP ports Large form factor Single/Dual SFP ports N/A Large form factor Quad SFP ports 01_nic_v3_lff4s_asm.stp Large form factor Quad 10GBASE-T ports 01 nic v3 lff4r asm.stp

Table 12: NIC Implementation Examples and 3D CAD

2.9 Non-NIC Use Cases

The OCP NIC 3.0 specification is mainly targeted for Network Interface Card applications. It is possible to use the same OCP NIC 3.0 card form-factor, baseboard interface and mechanical design to enable non-NIC use cases. These non-NIC use cases use the same baseboard/OCP NIC 3.0 card interface as defined in Section 3. The non-NIC use cases are not covered in the current revision of the OCP NIC 3.0 specification. Example non-NIC use cases implement various external I/O interfaces and are shown in Table 13.

Example Use Case	Card External I/O Interface(s)
PCIe Retimer Card	PCIe
Accelerator Card	N/A
NVMe Card	N/A
Storage HBA / RAID Card	N/A <mark>/ TBD</mark>

Table 13: Example Non-NIC Use Cases

3 Card Edge and Baseboard Connector Interface

3.1 Gold Finger Requirements

The OCP NIC 3.0 cards are compliant to the SFF-TA-1002 specification with respect to the gold fingers and connectors.

Small Size cards fit in the Primary Connector. Primary Connector compliant cards are 76mm x 115mm and may implement the full 168-pins. The Primary Connector cards may optionally implement a subset of gold finger pins if there is a reduced PCle width requirement (such as 1 x8 and below). In this case, the card edge gold finger may implement a 2C design. The overall board thickness is 1.57mm. The gold finger dimensions for the Primary Connector compliant cards are shown below.

Large Size Cards support up to a x32 PCIe implementation and may use both the Primary and Secondary (4C) Connectors. Large Size Cards may implement a reduced PCIe lane count and optionally implement only the Primary Connector 4C+, or 2C OCP bay.

Note: The "B" pins on the connector are associated with the top side of the OCP NIC 3.0 card. The "A" pins on the connector are associated with the bottom side of the OCP NIC 3.0 card.

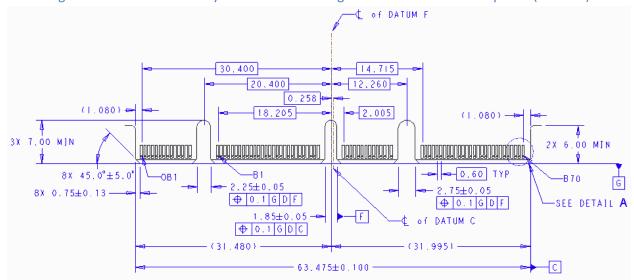


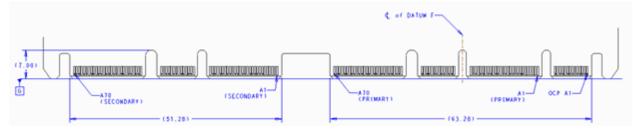
Figure 63: Small Size Primary Connector Gold Finger Dimensions – x16 – Top Side ("B" Pins)



Figure 64: Large Size Card Gold Finger Dimensions – x32 – Top Side ("B" Pins)

Ğ (SECONDARY) 61 (SECONDARY) (63,28)

Figure 65: Large Size Card Gold Finger Dimensions – x32 – Bottom Side ("A" Pins)



3.1.1 **Gold Finger Mating Sequence**

Per the SFF-TA-1002 specification, the Primary and Secondary Connectors are protocol agnostic and are optimized for high speed differential pairs. For use in the OCP NIC 3.0 application, some pin locations are used for single ended control nets or power and would benefit from a shorter pin length for staggering. As such, the recommended OCP NIC 3.0 card gold finger staging is shown in Table 14 for a two stage, first-mate, last-break functionality. The host connectors have a single stage mating and do not implement different pin lengths.

The AIC Plug (Free) side refers to the OCP NIC 3.0 card gold fingers; the receptacle (Fixed) side refers to the physical connector on the host platform. This table is based on the SFF-TA-1002 Table A-1 with modifications for OCP NIC 3.0. Refer to the mechanical drawings for pin the first-mate and second-mate lengths.

Note: Pin names in Table 14 are used for first mate/second mate reference only. Full pin definitions are described in Sections 3.3 and 3.4.

	Side B				Sic	le A	
	Gold Finger Side (Free)		Gold Finger Side (Free) Receptacle		Gold Finger Side (Free)		Receptacle
	2 nd Mate	1 st Mate	(Fixed)		2 nd Mate	1 st Mate	(Fixed)
OCP B1	NIC_PWR_GOOD			OCP A1	PERST2#		
OCP B2	MAIN_PWR_EN			OCP A2	PERST3#		
OCP B3	LD#			OCP A3	WAKE#		
OCP B4	DATA_IN			OCP A4	RBT_ARB_IN		
OCP B5	DATA_OUT			OCP A5	RBT_ARB_OUT		
OCP B6	CLK			OCP A6	GND		
OCP B7	SLOT_ID			OCP A7	RBT_TX_EN		
OCP B8	RBT_RXD1			OCP A8	RBT_TXD1		
OCP B9	RBT_RXD0			OCP A9	RBT_TXD0		
OCP B10	GND			OCP A10	GND		
OCP B11	REFCLKn2			OCP A11	REFCLKn3		

Table 14: Contact Mating Positions for the Primary and Secondary Connectors

OCP B12	REFCLKp2	ОСР	A12 REFCLKp3	
OCP B13	GND	ОСР		
OCP B14	RBT_CRS_DV	OCP	A14 RBT_CLK_IN	
		Mechanical Ke	/	
B1	+12V_EDGE	A1	GND	
B2	+12V_EDGE	A2	GND	
B3	+12V_EDGE	A3	GND	
B4	+12V_EDGE	A4	GND	
B5	+12V_EDGE	A5	GND	
B6	+12V_EDGE	A6	GND	
B7	BIFO#	A7	SMCLK	
B8	BIF1#	A8	SMDAT	
B9	BIF2#	A9	SMRST#	
B10	PERSTO#	A10	PRSNTA#	
B11	+3.3V_EDGE	A11	PERST1#	
B12	AUX_PWR_EN	A12	PRSNTB2#	
B13	GND	A13	GND	
B14	REFCLKn0	A14	REFCLKn1	
B15	REFCLKp0	A15	REFCLKp1	
B16	GND	A16	GND	
B17	PETn0	A17	PERn0	
B18	PETp0	A18	PERp0	
B19	GND	A19	GND	
B20	PETn1	A20	PERn1	
B21	PETp1	A21	PERp1	
B22	GND	A22	GND	
B23	PETn2	A23	PERn2	
B24	PETp2	A24	PERp2	
B25	GND	A25	GND	
B26	PETn3	A26	PERn3	
B27	PETp3	A27	PERp3	
B28	GND	A28	GND	
		Mechanical Ke		
B29	GND	A29	GND	
B30	PETn4	A30	PERn4	
B31	PETp4	A31	PERp4	
B32	GND	A32	GND	
B33	PETn5	A33	PERn5	
B34	PETp5	A34	PERp5	
B35	GND	A35	GND	
B36	PETn6	A36	PERn6	
B37	PETp6	A37	PERp6	
B38	GND	A38	GND	
B39	PETn7	A39	PERn7	
B40	PETp7	A40	PERp7	
B41	GND	A41	GND	
B41 B42	PRSNTBO#	A41 A42	PRSNTB1#	
DTZ	1 HOIVIDON	Mechanical Ke		
B43	GND	A43		
B43	PETn8	A43 A44	PERn8	
B44 B45	PETP8	A44 A45	PERp8	
B45	GND	A45 A46	GND	
B40 B47	PETn9	A46 A47	PERn9	
B47	PETP9	A47 A48	PERp9	
B49	GND	A48 A49	GND	
B50	PETn10	A50	PERn10	
B50 B51	PETp10	A50 A51	PERp10	
B51 B52	GND	A51 A52	GND GND	
	PETn11			
B53		A53	PERn11	
B54	PETp11	A54	PERp11	
B55	GND DETro12	A55	GND PERn12	
B56	PETn12	A56		
B57	PETp12	A57	PERp12	
B58	GND	A58	GND	
B59	PETn13	A59	PERn13	
B60	PETp13	A60	PERp13	
B61	GND	A61	GND	
B62	PETn14	A62	PERn14	
B63	PETp14	A63	PERp14	
B64	GND	A64	GND	
B65	PETn15	A65	PERn15	

B66	PETp15		A66	PERp15	
B67	GND		A67	GND	
B68	PWRBRK#		A68	RFU 2, N/C	
B69	RFU 1, N/C		A69	RFU 3, N/C	
B70	PRSNTB3#		A70	RFU 4, N/C	

3.2 Baseboard Connector Requirements

The OCP NIC 3.0 connectors are compliant to the "4C+" and "4C" connectors as defined in the SFF-TA-1002 specification for a right angle or straddle mount form-factor. The Primary Connector is a 4C+ implementation with 168-pins. The Secondary Connector is a 4C implementation with 140-pins. Both the Primary and Secondary Connectors includes support for up to 32 differential pairs to support a x16 PCle connection. Each connector also provides 6 pins of +12V_EDGE, and 1 pin of +3.3V_EDGE for power. This implementation is common between both the Primary and Secondary Connectors. In addition, the 4C+ implementation of the Primary Connector has a 28-pin OCP Bay used for management and support for up to a 4 x2 and 4 x4 multi-host configuration on the Primary Connector. The Primary and Secondary Connector drawings are shown below.

All diagram units are in mm unless otherwise noted.

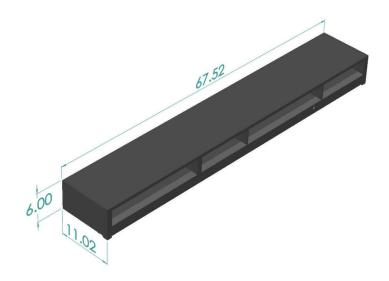
3.2.1 Right Angle Connector

The following offset and height options are available for the right angle Primary and Secondary Connectors.

Table 15: Right Angle Connector Options

Name	Pins	Style and Baseboard Thickness	Offset (mm)
Primary Connector – 4C+	168 pins	Right Angle	4mm
Secondary Connector – 4C	140 pins	Right Angle	4mm

Figure 66: 168-pin Base Board Primary Connector – Right Angle



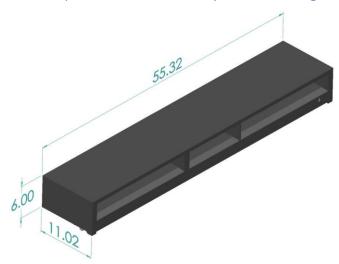


Figure 67: 140-pin Base Board Secondary Connector – Right Angle

3.2.2 Right Angle Offset

The OCP NIC 3.0 right angle connectors have a 4.0mm offset from the baseboard (pending SI simulation results). This is shown in Figure 68.

Figure 68: OCP NIC 3.0 Card and Host Offset for Right Angle Connectors



3.2.3 Straddle Mount Connector

The following offset and height options are available for the straddle mount Primary and Secondary Connectors.

Table 16: Straddle Mount Connector Options

Name	Pins	Style and Baseboard Thickness	Offset (mm)
Primary Connector – 4C+	168 pins	Straddle Mount for 0.062"	Coplanar (0mm)
Primary Connector – 4C+	168 pins	Straddle Mount for 0.076"	-0.3mm
Primary Connector – 4C+	168 pins	Straddle Mount for 0.093"	Coplanar (0mm)
Secondary Connector – 4C	140 pins	Straddle Mount for 0.062"	Coplanar (0mm)
Secondary Connector – 4C	140 pins	Straddle Mount for 0.076"	-0.3mm
Secondary Connector – 4C	140 pins	Straddle Mount for 0.093"	Coplanar (0mm)

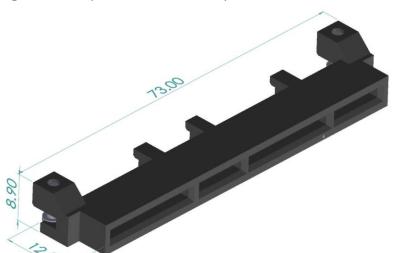
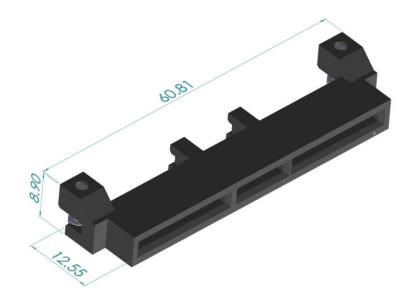


Figure 69: 168-pin Base Board Primary Connector – Straddle Mount

Figure 70: 140-pin Base Board Secondary Connector – Straddle Mount



3.2.4 Straddle Mount Offset and PCB Thickness Options

The OCP NIC 3.0 straddle mount connectors have four baseboard PCB thicknesses they can accept. The available options are shown in Figure 71. The thicknesses are 0.062'', 0.076'', 0.093'', and 0.105''. These PCBs must be controlled to a thickness of $\pm 10\%$. These are available for both the Primary and Secondary Connector locations. At the time of this writing, the most commonly used part is expected to be the 0.076'' baseboard thickness.

Connector Mating PCB Host PCB **Mating PCB** Connector **Host PCB Thickness Thickness** .062" (1.57mm) Α .076" (1.93mm) В .062" (1.57mm) .093" (2.36mm) C .105" (2.67mm) D

Figure 71: OCP NIC 3.0 Card and Baseboard PCB Thickness Options for Straddle Mount Connectors

The connectors are capable of being used coplanar as shown in Figure 72. Additionally, the connectors are also capable of having a 0.3mm offset from the centerline of the host board as shown in Figure 73.

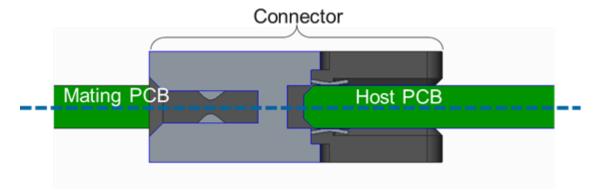
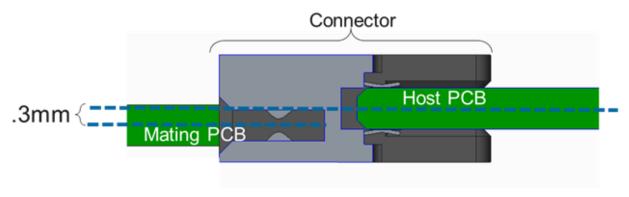


Figure 72: 0mm Offset (Coplanar) for 0.062" Thick Baseboards

Figure 73: 0.3mm Offset for 0.076" Thick Baseboards



3.2.5 Large Card Connector Locations

In order to the support the large form factor, systems must locate the Primary and Secondary Connectors per the mechanical drawing shown in Figure 74 and Figure 75.

Figure 74: Primary and Secondary Connector Locations for Large Card Support with Right Angle

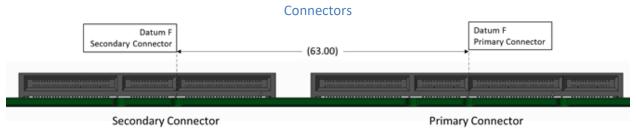
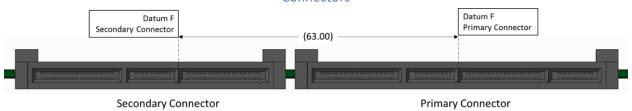


Figure 75: Primary and Secondary Connector Locations for Large Card Support with Straddle Mount Connectors



3.3 Pin definition

The pin definitions of an OCP NIC 3.0 card with up to a x32 PCIe interface are shown in Table 17 and Table 18. All signal directions are shown from the perspective of the baseboard.

A baseboard system may provide a combination of Primary Connectors only, or Primary and Secondary Connectors to support multiple sizes of OCP NIC 3.0 cards. Both connectors share common functionality with power, SMBus 2.0, x16 PCle and bifurcation control. The Primary Connector 4C+ definition has an additional OCP Bay (pins OCP_A[1:14], OCP_B[1:14]) with additional REFCLKs for supporting up to four PCle hosts, NC-SI over RBT connectivity and a Scan Chain for information exchange between the host and card. The NIC is required to implement the Scan Chain, while the baseboard may choose to

optionally implement it. Depending on the baseboard form-factor, multiple OCP NIC 3.0 compliant cards may be designed into the system.

The pins common to the Primary and Secondary Connectors are shown in Section 3.4. The OCP Bay pins on the Primary Connector only are shown in Section 3.5.

Cards or systems that do not require the use of a PCIe x16 connection may optionally implement a subset electrical connections as applicable to the design. For example, a x8 (or smaller) card using the first 8 PCIe lanes that is compliant with the Primary Connector pinout. Refer to Sections 3.1 and 3.2 for mechanical details. For these cases, the Primary Connector matches the 2C dimensions as defined in SFF-TA-1002.

In all cases, the physical baseboard connectors shall support x16 PCIe widths and must be implemented with the Primary (4C+) and Secondary (4C) connectors.

Side B Side A PERST2# OCP_B1 NIC_PWR_GOOD OCP A1 Primary Connector (2C+, x8, 112-pin OCP NIC 3.0 card with OCP bay) Primary Connector (4C+, x16, 168-pin OCP NIC 3.0 card with OCP Bay) OCP B2 MAIN_PWR_EN PERST3# OCP A2 OCP B3 LD# WAKE# OCP A3 OCP B4 DATA IN RBT_ARB_IN OCP A4 OCP B5 DATA OUT RBT_ARB_OUT OCP A5 OCP_B6 CLK **GND** OCP A6 OCP_B7 SLOT ID RBT_TX_EN OCP A7 OCP B8 RBT RXD1 RBT TXD1 OCP A8 OCP B9 **RBT RXD0** RBT TXD0 OCP A9 OCP_B10 OCP A10 GND **GND** OCP_B11 REFCLKn2 REFCLKn3 OCP A11 OCP_B12 REFCLKp2 REFCLKp3 OCP A12 GND OCP_A13 OCP_B13 GND OCP B14 RBT CRS DV RBT CLK IN OCP A14 **Mechanical Key** GND В1 Α1 +12V_EDGE В2 **GND** A2 В3 **EDGE** GND А3 В4 +12V EDGE GND Α4 В5 +12V EDGE **GND** A5 В6 +12V EDGE GND Α6 В7 BIFO# **SMCLK** Α7 В8 BIF1# **SMDAT** Α8 BIF2# SMRST# Α9 В9 B10 PRSNTA# A10 PERSTO# B11 +3.3V EDGE PERST1# A11 B12 AUX PWR EN PRSNTB2# A12 A13 **B13 GND GND** B14 REFCLKn0 REFCLKn1 A14 **B15** REFCLKp0 REFCLKp1 A15 B16 GND GND A16 **B17** PETn0 PERn0 A17 B18 PETp0 PERp0 A18 B19 **GND** GND A19 B20 PETn1 PERn1 A20 B21 A21 PETp1 PERp1

Table 17: Primary Connector Pin Definition (x16) (4C+)

B22	GND	GND	A22	
B23	PETn2	PERn2	A23	
B24	PETp2	PERp2	A24	
B25	GND	GND	A25	
B26	PETn3	PERn3	A26	
B27	PETp3	PERp3	A27	
B28	GND	GND	A28	
	Mechan	ical Key		
B29	GND	GND	A29	
B30	PETn4	PERn4	A30	
B31	PETp4	PERp4	A31	
B32	GND	GND	A32	
B33	PETn5	PERn5	A33	
B34	PETp5	PERp5	A34	
B35	GND	GND	A35	
B36	PETn6	PERn6	A36	
B37	РЕТр6	PERp6	A37	
B38	GND	GND	A38	
B39	PETn7	PERn7	A39	
B40	PETp7	PERp7	A40	
B41	GND	GND	A41	
B42	PRSNTB0#	PRSNTB1#	A42	
	Mechan	ical Key		
B43	GND	GND	A43	
B44	PETn8	PERn8	A44	
B45	PETp8	PERp8	A45	
B46	GND	GND	A46	
B47	PETn9	PERn9	A47	
B48	PETp9	PERp9	A48	
B49	GND	GND	A49	
B50	PETn10	PERn10	A50	
B51	PETp10	PERp10	A51	
B52	GND	GND	A52	
B53	PETn11	PERn11	A53	
B54	PETp11	PERp11	A54	
B55	GND	GND	A55	
B56	PETn12	PERn12	A56	
B57	PETp12	PERp12	A57	
B58	GND	GND	A58	
B59	PETn13	PERn13	A59	
B60	PETp13	PERp13	A60	
B61	GND	GND	A61	
B62	PETn14	PERn14	A62	
B63	PETp14	PERp14	A63	
B64	GND	GND	A64	
B65	PETn15	PERn15	A65	
B66	PETp15	PERp15	A66	
B67	GND	GND	A67	
B68	PWRBRK#	RFU2, N/C	A68	
B69	RFU1, N/C	RFU3, N/C	A69	
B70	PRSNTB3#	RFU4, N/C	A70	
		, ,		

Table 18: Secondary Connector Pin Definition (x16) (4C)

	Side B	Side A	(- /	
B1	+12V_EDGE	GND	A1	10
B2	+12V_EDGE	GND	A2	èc
B3	+12V_EDGE	GND	A3	onc
B4	+12V_EDGE	GND	A4	lan
B5	+12V_EDGE	GND	A5	00/
B6	+12V_EDGE	GND	A6	n l
B7	BIFO#	SMCLK	A7	ect
B8	BIF1#	SMDAT	A8	ğ
B9	BIF2#	SMRST#	A9	(4 _C
B10	PERSTO#	PRSNTA#	A10	χ.
B11	+3.3V_EDGE	PERST1#	A11	.6,
B12	AUX_PWR_EN	PRSNTB2#	A12	140
B13	GND	GND	A13	- pi
B14	REFCLKn0	REFCLKn1	A14	n O
B15	REFCLKp0	REFCLKp1	A15	Ğ
B16	GND	GND	A16	Z
B17	PETn0	PERn0	A10	Secondary Connector (4C, x16, 140-pin OCP NIC 3.0 card)
B17	PETp0	PERPO	A17	О с
B19	GND	GND	A19	ard
B20	PETn1	PERn1	A20	J
B21	PETp1	PERp1	A20	
B22	GND	GND	A21	
B23	PETn2	PERn2	A23	
B23	PETp2	PERp2	A24	
B25	GND	GND	A24 A25	
B26	PETn3	PERn3	A26	
B27	PETp3	PERp3	A20 A27	
B28	GND	GND	A27	
D28		nical Key	A20	
B29	GND	GND	A29	
B30	PETn4	PERn4	A30	
B31	PETp4	PERp4	A31	
B32	GND	GND	A32	
B33	PETn5	PERn5	A33	
B34	PETp5	PERp5	A34	
B35	GND	GND	A35	
B36	PETn6	PERn6	A36	
B37	PETp6	PERp6	A37	
B38	GND	GND	A38	
B39	PETn7	PERn7	A39	
B40	PETp7	PERp7	A40	
B41	GND	GND	A40 A41	
B41 B42	PRSNTBO#	PRSNTB1#	A41 A42	
D4Z		nical Key	A4Z	
B43	GND	GND	A43	
B44	PETn8	PERn8	A44	
B45	PETp8	PERp8	A44 A45	
B45	GND	GND	A45	
B47	PETn9	PERn9	A40 A47	
B47 B48	PETIP9	PERIP9	A47 A48	
B49	GND	GND	A46 A49	
B50	PETn10	PERn10	A50	
B51	PETp10	PERp10	A50	
דרם	LLIDIO	FLVh10	MJI	

B52	GND	GND	A52	
B53	PETn11	PERn11	A53	
B54	PETp11	PERp11	A54	
B55	GND	GND	A55	
B56	PETn12	PERn12	A56	
B57	PETp12	PERp12	A57	
B58	GND	GND	A58	
B59	PETn13	PERn13	A59	
B60	PETp13	PERp13	A60	
B61	GND	GND	A61	
B62	PETn14	PERn14	A62	
B63	PETp14	PERp14	A63	
B64	GND	GND	A64	
B65	PETn15	PERn15	A65	
B66	PETp15	PERp15	A66	
B67	GND	GND	A67	
B68	PWRBRK#	RFU2, N/C	A68	
B69	RFU1, N/C	RFU3, N/C	A69	
B70	PRSNTB3#	RFU4, N/C	A70	

3.4 Signal Descriptions – Common

The pins shown in this section are common to both the Primary and Secondary Connectors. All pin directions are from the perspective of the baseboard.

The OCP NIC 3.0 card shall implement protection methods to prevent leakage paths between the V_{AUX} and V_{MAIN} power domains in the event that a NIC is powered down in a powered up baseboard.

Note: Pins that are only used on Primary Connector 28-pin OCP bay are defined in Section 3.5.

3.4.1 PCIe Interface Pins

This section provides the pin assignments for the PCIe interface signals. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0. Example connection diagrams for are shown in Figure 89.

Table 19: Pin Descriptions – PCle 1

Signal Name	Pin #	Baseboard Direction	Signal Description
REFCLKn0	B14	Output	PCIe compliant differential reference clock #0, and
REFCLKp0	B15		#1. 100MHz reference clocks are used for the OCP
REFCLKn1	A14	Output	NIC 3.0 card PCIe core logic.
REFCLKp1	A15		
			For baseboards, the REFCLKO and REFCLK1 signals shall be available at the connector. Baseboards should disable REFCLK1 if it is not used by the OCP NIC 3.0 card.
			For OCP NIC 3.0 cards, the required REFCLKs shall be connected per the endpoint datasheet. Unused REFCLKs on the OCP NIC 3.0 card shall be left as a no connect.

			Note: For cards that only support 1 x16, REFCLKO is used. For cards that support 2 x8, REFCLKO is used for the first eight PCIe lanes, and REFCLK1 is used for the second eight PCIe lanes. REFCLKO is always available to all OCP NIC 3.0 cards. The card should not assume REFCLK1 is available until the bifurcation negotiation process is completed.
			Refer to Section 2.1 in the PCIe CEM Specification, Rev 4.0 for electrical details.
PETn0	B17	Output	Transmitter differential pairs [0:15]. These pins are
PETp0	B18		connected from the baseboard transmitter
PETn1	B20	Output	differential pairs to the receiver differential pairs on
PETp1	B21		the OCP NIC 3.0 card.
PETn2	B23	Output	TI 801 1 11 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
PETp2	B24		The PCIe transmit pins shall be AC coupled on the
PETn3	B26	Output	baseboard with capacitors. The AC coupling capacitor
PETp3	B27		value shall use the C _{TX} parameter value specified in
PETn4	B30	Output	the PCIe Base Specification.
PETp4	B31		For headheande the DET[0:45] signals are many in the
PETn5	B33	Output	For baseboards, the PET[0:15] signals are required at
PETp5	B34		the connector.
PETn6	B36	Output	For OCD NIC 2 0 cards, the required DET[0:15] signals
PETp6	B37	1.	For OCP NIC 3.0 cards, the required PET[0:15] signals shall be connected to the endpoint silicon. For silicon
PETn7	B39	Output	that uses less than a x16 connection, the appropriate
PETp7	B40	10	PET[0:15] signals shall be connected per the endpoint
PETn8	B44	Output	datasheet.
PETp8	B45		
PETn9	B47	Output	Refer to Section 6.1 in the PCIe CEM Specification,
PETp9	B48	0.1.	Rev 4.0 for details.
PETn10	B50	Output	
PETp10	B51	0.1.	\dashv
PETn11	B53	Output	
PETp11	B54	0.1.	\dashv
PETn12	B56	Output	
PETp12	B57	0	\dashv
PETn13	B59	Output	
PETp13	B60	0	\dashv
PETn14	B62	Output	
PETp14	B63	Outout	\dashv
PETn15	B65	Output	
PETp15	B66	Innut	Pacaivar differential pairs [0:15] These pins are
PERnO	A17 A18	Input	Receiver differential pairs [0:15]. These pins are connected from the OCP NIC 3.0 card transmitter
PERp0		Innu+	connected from the OCP NIC 3.0 card transmitter
PERn1	A20	Input	

DED:: 1	4.24	1	differential action to the annual condition of the control of
PERp1	A21	1	differential pairs to the receiver differential pairs on
PERn2	A23	Input	the baseboard.
PERp2	A24		
PERn3	A26	Input	The PCIe receive pins shall be AC coupled on the OCP
PERp3	A27		NIC 3.0 card with capacitors. The AC coupling
PERn4	A30	Input	capacitor value shall use the C _{TX} parameter value
PERp4	A31		specified in the PCIe Base Specification.
PERn5	A33	Input	
PERp5	A34		For baseboards, the PER[0:15] signals are required at
PERn6	A36	Input	the connector.
PERp6	A37	'	
PERn7	A39	Input	For OCP NIC 3.0 cards, the required PER[0:15] signals
PERp7	A40	mpac	shall be connected to the endpoint silicon. For silicon
PERn8	A44	Input	that uses less than a x16 connection, the appropriate
	A44 A45	iliput	PER[0:15] signals shall be connected per the endpoint
PERp8		la a t	datasheet.
PERn9	A47	Input	
PERp9	A48		Refer to Section 6.1 in the PCIe CEM Specification,
PERn10	A50	Input	Rev 4.0 for details.
PERp10	A51		Nev 4.0 for details.
PERn11	A53	Input	
PERp11	A54		
PERn12	A56	Input	
PERp12	A57		
PERn13	A59	Input	
PERp13	A60		
PERn14	A62	Input	1
PERp14	A63	'	
PERn15	A65	Input	
PERp15	A66	pac	
PERSTO#	B10	Output	PCIe Reset #0, #1. Active low.
PERST1#	A11	Output	Tele Reset #0, #1. Active low.
I LIISTI#	711		When PERSTn# is deasserted, the signal shall indicate
			the applied power is within tolerance and stable for
			the OCP NIC 3.0 card.
			the OCP NIC 3.0 card.
			PERST# shall be deasserted at least 100ms after the
			power rails are within the operating limits per the
			PCIe CEM Specification. The PCIe REFCLKs shall also
			become stable within this period of time.
			PERST shall be pulled high to +3.3V_EDGE on the
			baseboard.
			For OCP NIC 3.0, PERST deassertion shall also indicate
			the full card power envelope is available to the OCP
			NIC 3.0 card.

For baseboards, the PERST[0:1]# signals are required at the connector.
For OCP NIC 3.0 cards, the required PERST[0:1]# signals shall be connected to the endpoint silicon. Unused PERST[0:1]# signals shall be left as a no connect.
Note: For cards that only support 1 x16, PERSTO# is used. For cards that support 2 x8, PERSTO# is used for the first eight PCIe lanes, and PERST1# is used for the second eight PCIe lanes.
PERSTO# is always available to all OCP NIC 3.0 cards. The card should not assume PERST1# is available until the bifurcation negotiation process is completed.
Refer to Section 2.2 in the PCIe CEM Specification, Rev 4.0 for details.

3.4.2 PCIe Present and Bifurcation Control Pins

This section provides the pin assignments for the PCIe present and bifurcation control signals. The AC/DC specifications are defined in Section 3.12. An example connection diagram is shown in Figure 76.

The PRSNTA#/PRSNTB[0:3]# state shall be used to determine if a card has been physically plugged in. The BIF[0:2]# pins shall be latched before PWR_EN assertion to ensure the correct values are detected by the system. Changing the pin states after this timing window is not allowed. Refer to the AC timing diagram in Section 3.12 for details.

Table 20: Pin Descriptions – PCle Present and Bifurcation Control Pins

Signal Name	Pin #	Baseboard Direction	Signal Description
PRSNTA#	A10	Output	Present A is used for OCP NIC 3.0 card presence and PCIe capabilities detection.
			For baseboards, this pin shall be directly connected to GND.
			For OCP NIC 3.0 cards, this pin shall be directly connected to the PRSNTB[3:0]# pins.
PRSNTB0#	B42	Input	Present B [0:3]# are used for OCP NIC 3.0 card
PRSNTB1#	A42		presence and PCIe capabilities detection.
PRSNTB2#	A12		
PRSNTB3#	B70		For baseboards, these pins shall be connected to the I/O hub and pulled up to +3.3V_EDGE using 1kOhm resistors.

			For OCP NIC 3.0 cards, these pins shall be strapped to PRSNTA# per the encoding definitions described in Section 3.6. Note: PRSNTB3# is located at the bottom of the 4C connector and is only applicable for OCP NIC 3.0 cards with a PCle width of x16 (or greater). OCP NIC 3.0 cards that implement a 2C card edge do not use the PRSNTB3# pin for capabilities or present detection.
BIFO# BIF1# BIF2#	B7 B8 B9	Output	Bifurcation [0:2]# pins allow the baseboard to force configure the OCP NIC 3.0 card bifurcation. For baseboards, these pins shall be outputs driven from the baseboard I/O hub and allow the system to force configure the OCP NIC 3.0 card bifurcation. The baseboard may optionally tie the BIF[0:2]# signals to +3.3V_EDGE or to ground per the definitions are described in Section 3.6 if no dynamic bifurcation configuration is required.
			For OCP NIC 3.0 cards, these signals shall connect to the endpoint bifurcation pins if it is supported. Note: the required combinatorial logic output for endpoint bifurcation is dependent on the specific silicon and is not defined in this specification.

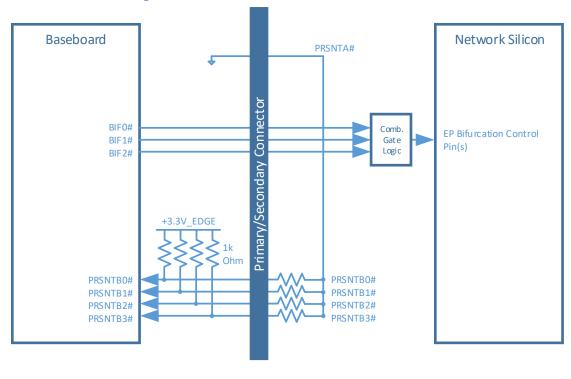


Figure 76: PCIe Present and Bifurcation Control Pins

3.4.3 SMBus Interface Pins

This section provides the pin assignments for the SMBus interface signals. The AC/DC specifications are defined in the SMBus 2.0 and I²C bus specifications. An example connection diagram is shown in Figure 77.

Signal Name	Pin #	Baseboard	Signal Description
Signal Name	FIII#	Direction	Signal Description
SMCLK	A7	Output, OD	SMBus clock. Open drain, pulled up to +3.3V_EDGE on the baseboard.
			For baseboards, the SMCLK from the platform SMBus master shall be connected to the connector.
			For OCP NIC 3.0 cards, the SMCLK from the endpoint silicon shall be connected to the card edge gold fingers.
SMDAT	A8	Input / Output, OD	SMBus Data. Open drain, pulled up to +3.3V_EDGE on the baseboard.
			For baseboards, the SMDAT from the platform SMBus master shall be connected to the connector.

Table 21: Pin Descriptions – SMBus

			For OCP NIC 3.0 cards, the SMDAT from the endpoint silicon shall be connected to the card edge gold fingers.
SMRST#	A9	Output, OD	For baseboards, this pin shall be pulled up to +3.3V_EDGE. The SMRST pin may be used to reset optional downstream SMBus devices (such as temperature sensors). The SMRST# implementation shall be mandatory for baseboard implementations. For OCP NIC 3.0 cards, SMRST# is optional and is dependent on the OCP NIC 3.0 card implementation. The SMRST# signal shall be left as a no connect if it is not used on the OCP NIC 3.0 card.

Baseboard +3.3V_EDGE FRU EEPROM Primary/Secondary Connector Boundary SMCLK SMCLK SMDAT SMDAT I2C Isolator Network Controller +3.3V (NIC) SMCLK SMDAT +3.3V_EDGE To SMB us devices with RST* pin (e.g. I/O Expander) SMRST*

Figure 77: Example SMBus Connections

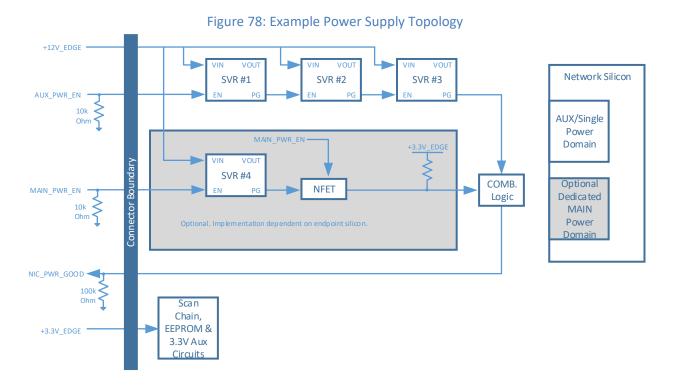
3.4.4 Power Supply Pins

This section provides the pin assignments for the power supply interface signals. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0 and amended in Section 3.10. An example connection diagram is shown in Figure 78.

Table 22: Pin Descriptions – Power

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
GND	Various	GND	Ground return; a total of 46 ground pins are on
			the main 140-pin connector area. Refer to
			Section 3.3 for details.
+12V_EDGE	B1, B2,	Power	+12V main or +12V aux power; total of 6 pins per
	B3, B4,		connector. The +12V_EDGE pins shall be rated to
	B5, B6		1.1A per pin with a maximum derated power
			delivery of 80W.
			The +12V_EDGE power pins shall be within the
			rail tolerances as defined in Section 3.10 when
			the PWR_EN pin is driven high by the baseboard.
+3.3V_EDGE	B11	Power	+3.3V main or +3.3V aux power; total of 1 pin per
			connector. The +3.3V_EDGE pin shall be rated to
			1.1A for a maximum derated power delivery of
			3.63W.
			The +3.3V_EDGE power pin shall be within the
			rail tolerances as defined in Section 3.10 when
			the PWR_EN pin is driven high by the baseboard.
AUX_PWR_EN	B12	Output	Aux Power enable. Active high.
			This pin indicates that the +12_EDGE and
			+3.3V_EDGE power is from the baseboard aux
			power rails.
			This signal shall be pulled down to GND through
			a 10kOhm resistor on the baseboard. This
			ensures the OCP NIC 3.0 card power is disabled
			until instructed to turn on by the baseboard.
			When low, the OCP NIC 3.0 card supplies running
			on aux power shall be disabled.
			When high, the OCP NIC 3.0 card supplies
			running on aux power shall be enabled.
			For OCP NIC 3.0 cards that do not use a separate
			"main power" domain circuitry, the

	1		
			AUX_PWR_EN signal serves as the primary
			method to enable all the card power supplies.
PWRBRK#	B68	Output, OD	Power break. Active low, open drain.
			This signal shall be pulled up to +3.3V_EDGE on the OCP NIC 3.0 card with a minimum of 95kOhm. The pull up on the baseboard shall be a
			stiffer resistance in-order to meet the timing specs as shown in the PCIe CEM Specification.
			When this signal is driven low by the baseboard, the Emergency Power Reduction State is requested. The OCP NIC 3.0 card shall move to a lower power consumption state.
			For baseboards, the PWRBRK# pin shall be implemented and available on the Primary Connector.
			For OCP NIC 3.0 cards, the PWRBRK# pin usage is optional. If used, the PWRBRK# should be connected to the network silicon to enable reduced power state. If not used, the PWRBRK# signal shall be left as a no connect.



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3.4.5 Miscellaneous Pins

This section provides the pin assignments for the miscellaneous interface signals.

Table 23: Pin Descriptions – Miscellaneous 1

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
RFU1, N/C	B69	Input /	Reserved future use pins. These pins shall be left as
RFU2, N/C	A68	Output	no connect.
RFU3, N/C	A69		
RFU4, N/C	A70		

3.5 Signal Descriptions – OCP Bay (Primary Connector)

The following section describes the functions in the Primary Connector 28-pin OCP bay. This 28-pin bay is shown in Section 3.3 and have pin numbers designated as OCP_B[1:14], and OCP_A[1:14]. All pin directions on this OCP bay are from the perspective of the baseboard.

The OCP NIC 3.0 card shall implement protection methods to prevent leakage paths between the V_{aux} and V_{main} power domains in the event that a NIC is powered down in a powered up baseboard.

Note: The pins that are common to both the Primary and Secondary Connectors are defined in Section 3.4.

3.5.1 PCIe Interface Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the PCIe interface signals on the Primary Connector OCP bay. The AC/DC specifications are defined in the PCIe CEM Specification. An example connection diagram that shows REFCLK2, REFCLK3, PERST2# and PERST3# is shown in Section 3.7.

Table 24: Pin Descriptions – PCle 2

			Descriptions – PCIe 2	
Signal Name	Pin #	Baseboard	Signal Description	
		Direction		
REFCLKn2	OCP_B11	Output	PCIe compliant differential reference clock #2, and	
REFCLKp2	OCP_B12		#3. 100MHz reference clocks are used for the OCP	
REFCLKn3	OCP_A11	Output	NIC 3.0 card PCIe core logic.	
REFCLKp3	OCP_A12			
			For baseboards, the REFCLK2 and REFCLK3 signals	
			are required at the Primary Connector. Baseboards	
			may disable REFCLK2 and REFCLK3 if they are not	
			used by the OCP NIC 3.0 card.	
			For OCP NIC 3.0 cards, the required REFCLKs shall be	
			connected per the endpoint datasheet. Unused	
			REFCLKs on the OCP NIC 3.0 card shall be left as a no	
			connect.	
			Note: REFCLK2 and REFCLK3 are only used for cards	
			that only support a four link PCIe bifurcation mode.	
			The card should not assume REFCLK2 and REFCLK3	
			are available until the bifurcation negotiation	
			process is completed.	
			Refer to Section 2.1 in the PCIe CEM Specification,	
			Rev 4.0 for details.	
PERST2#	OCP_A1	Output	PCIe Reset #2, #3. Active low.	
PERST3#	OCP_A2			
			When PERSTn# is deasserted, the signal shall	
			indicate the applied power is within tolerance and	
			stable for the OCP NIC 3.0 card.	

	1		
			PERST# shall be deasserted at least 100ms after the power rails are within the operating limits per the PCIe CEM Specification. The PCIe REFCLKs shall also become stable within this period of time.
			PERST shall be pulled high to +3.3V_EDGE on the baseboard.
			For OCP NIC 3.0, PERST deassertion shall also indicate the full card power envelope is available to the OCP NIC 3.0 card.
			For baseboards, the PERST[2:3]# signals are required at the connector.
			For OCP NIC 3.0 cards, the required PERST[2:3]# signals shall be connected to the endpoint silicon. Unused PERST[2:3]# signals shall be left as a no connect.
			Note: PERST2# and PERST3# are only used for cards that support a four link PCIe bifurcation mode.
			The card should not assume PERST2# and PERST3# are available until the bifurcation negotiation process is completed.
			Refer to Section 2.2 in the PCIe CEM Specification, Rev 4.0 for details.
WAKE#	OCP_A3	Input, OD	WAKE#. Open drain. Active low.
			This signal shall be driven by the OCP NIC 3.0 card to notify the baseboard to restore PCIe link. For OCP NIC 3.0 cards that support multiple WAKE# signals, their respective WAKE# pins may be tied together as the signal is open-drain to form a wired-OR.
			For baseboards, this signal shall be pulled up to +3.3V_EDGE on the baseboard with a 10kOhm resistor. This signals shall be connected to the system WAKE# signal.
			For OCP NIC 3.0 cards, this signal shall be directly connected to the endpoint silicon WAKE# pin(s). This pin shall be left as a no connect if WAKE# is not supported by the silicon.
	<u> </u>		

Refer to Section 2.3 in the PCIe CEM Specification,
Rev 4.0 for details.

3.5.2 NC-SI Over RBT Interface Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the NC-SI over RBT interface signals on the Primary Connector OCP bay. The AC/DC specifications for NC-SI over RBT are defined in the DMTF DSP0222 NC-SI specification. An example connection diagram is shown in Figure 79.

Table 25: Pin Descriptions – NC-SI Over RBT

Signal Name	Pin #	Baseboard Direction	Signal Description
RBT_REF_CLK	OCP_A14	Output	Reference clock input. Synchronous clock reference for receive, transmit and control interface. The clock shall have a typical frequency of 50MHz.
			For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the Primary Connector OCP bay. This signal requires a 100kOhm pull down resistor on the baseboard. If the baseboard does not support NC-SI over RBT, then this signal shall be terminated to ground through a 100kOhm pull down resistor.
			For OCP NIC 3.0 cards, this pin shall be connected between the gold finger to the endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.
RBT_CRS_DV	OCP_B14	Input	Carrier sense/receive data valid. This signal is used to indicate to the baseboard that the carrier sense/receive data is valid.
			For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull down resistor on the baseboard. If the baseboard does not support NC-SI over RBT, then this signal shall be terminated to ground through a 100kOhm pull down resistor.
			For OCP NIC 3.0 cards, this pin shall be connected between the gold finger to the endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.
RBT_RXD0 RBT_RXD1	OCP_B9 OCP_B8	Input	Receive data. Data signals from the network controller to the BMC.

			For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull-up resistor to +3.3V_EDGE on the baseboard. If the baseboard does not support NC-SI over RBT, then this signal shall be terminated to +3.3V_EDGE through a 100kOhm pull-up. For OCP NIC 3.0 cards, this pin shall be connected between the gold finger and the RBT_RXD[0:1] pins on endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.
RBT_TX_EN	OCP_A7	Output	Transmit enable.
			For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull down resistor to ground on the baseboard. If the baseboard does not support NC-SI over RBT, then this signal shall be terminated to ground through a 100kOhm pull down.
			For OCP NIC 3.0 cards, this pin shall be connected between the gold finger to the endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.
RBT_TXD0 RBT_TXD1	OCP_A9 OCP_A8	Output	Transmit data. Data signals from the BMC to the network controller.
			For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull-up resistor to +3.3V_EDGE on the baseboard. If the baseboard does not support NC-SI over RBT, then this signal shall be terminated to +3.3V_EDGE through a 100kOhm pull-up.
			For OCP NIC 3.0 cards, this pin shall be connected between the gold finger to the RBT_TXD[0:1] pins on the endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.
RBT_ARB_OUT	OCP_A5	Output	NC-SI hardware arbitration output. This pin shall only be used if the endpoint silicon supports hardware arbitration. This pin shall be connected to the RBT_ARB_IN signal of an adjacent device in the hardware arbitration ring.

			The baseboard shall implement a multiplexing implementation that directs the RBT_ARB_OUT to the RBT_ARB_IN pin of the next NC-SI over RBT capable device in the ring, or back to the RBT_ARB_IN pin of the source device if there is a single device on the ring. For baseboards, this pin shall be connected between the baseboard OCP connector(s) to complete the hardware arbitration ring. If the baseboard does not support NC-SI over RBT, this signal shall be directly connected to the RBT_ARB_IN pin to allow a complete hardware arbitration ring on the OCP NIC 3.0 card. For OCP NIC 3.0 cards, this pin shall be connected
			from the gold finger to the RBT_ARB_IN pin on the endpoint silicon. This pin shall be directly connected to the card edge RBT_ARB_IN pin if NC-SI is not supported. This allows the hardware arbitration signals to pass through in a multi-Primary Connector baseboard.
RBT_ARB_IN	OCP_A4	Input	NC-SI hardware arbitration input. This pin shall only be used if the endpoint silicon supports hardware arbitration. This pin shall be connected to the RBT_ARB_OUT signal of an adjacent device in the hardware arbitration ring.
			The baseboard shall implement a multiplexing implementation that directs the RBT_ARB_IN to the RBT_ARB_OUT pin of the next NC-SI over RBT capable device in the ring, or back to the RBT_ARB_OUT pin of the source device if there is a single device on the ring.
			For baseboards, this pin shall be connected between the baseboard OCP connector(s) to complete the hardware arbitration ring. If the baseboard does not support NC-SI over RBT, this signal shall be directly connected to the RBT_ARB_OUT pin to allow a complete hardware arbitration ring on the OCP NIC 3.0 card.
			For OCP NIC 3.0 cards, this pin shall be connected between the gold finger to the RBT_ARB_OUT pin on the endpoint silicon. This pin shall be directly connected to the card edge RBT_ARB_OUT pin if NC-SI is not supported. This allows the hardware

			arbitration signals to pass through in a multi-Primary Connector baseboard.
SLOT_ID	OCP_B7	Output	NC-SI Address pin. This pin shall only be used if the end point silicon supports package identification.
			For baseboards, this pin shall be used to set the slot ID value. This pin shall be directly to GND for SlotID = 0. This pin shall be pulled up to +3.3V_EDGE for SlotID = 1.
			For OCP NIC 3.0 cards, this pin shall be connected to the endpoint device GPIO associated with the Package ID[1] field. Refer to Section 4.8.1 and the device datasheet for details.
			For OCP NIC 3.0 cards with multiple endpoint devices, the SLOT_ID pin may be used to configure a different Package ID value so long as the resulting combination does not cause addressing interferences.
			For endpoint devices without NC-SI over RBT support, this pin shall be left as a no connect on the OCP NIC 3.0 card.

50MHz 1:2 Network Silicon #0 Baseboard Network Silicon #1 Clock Buffer Management Optional Optional Controller CLK_IN CRS_DV CLK_IN CRS_DV RXD[0:1] RXD[0:1] RXD[0:1] TX_EN TXD[0:1] TX_EN TX EN Primary Connector TXD[0:1] TXD[0:1] ARB_OUT ARB_IN ARB_OUT ARB_IN ARB OUT PACKAGE_ID[0] = **0b0**PACKAGE_ID[1] = SLOT_ID
PACKAGE_ID[2] = 0b0 PACKAGE_ID[0] = **0b1**PACKAGE_ID[1] = SLOT_ID
PACKAGE_ID[2] = 0b0 SLOT_ID ARB_IN

Figure 79: NC-SI Over RBT Connection Example – Single Primary Connector

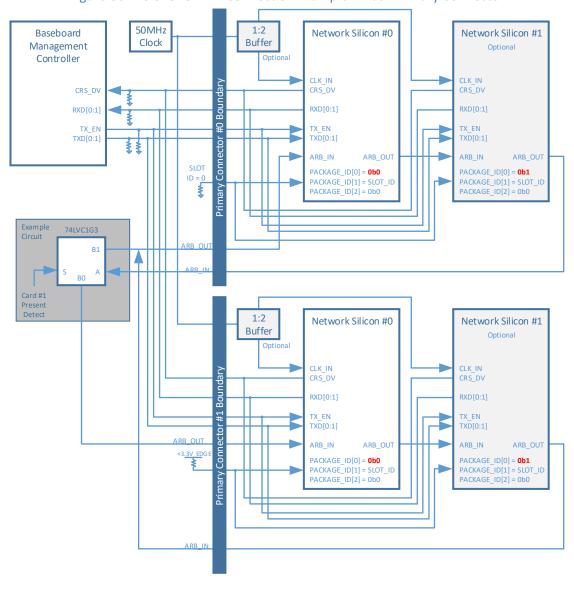


Figure 80: NC-SI Over RBT Connection Example – Dual Primary Connector

Note 1: For baseboard designs with a single Primary Connector, connect ARB_IN to ARB_OUT to complete the NC-SI hardware arbitration ring. For designs with multiple Primary Connectors, connect ARB_IN and ARB_OUT to an analog mux to complete the NC-SI arbitration ring based on the number of cards installed in the system. An example dual Primary Connector implementation is shown in Figure 80.

Note 2: For OCP NIC 3.0 cards with two discrete endpoint silicon, the Package ID[0] bit shall be statically set based on its silicon instance. For example, the figure above shows Network Silicon #0 and Network Silicon #1. Network Silicon #0 has Package ID[0] = 0b0, Network Silicon #1 has Package ID[0] = 0b1.

3.5.3 Scan Chain Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the Scan Bus interface signals on the Primary Connector OCP Bay. An example timing diagram is shown in Figure 81. An example connection diagram is shown in Figure 82.

Table 26: Pin Descriptions – Scan Chain

Signal Name	Pin #	Baseboard Direction	Signal Description
CLK	OCP_B6	Output	Scan clock. The CLK is an output pin from the baseboard to the OCP NIC 3.0 card. The CLK may run up to 12.5MHz.
			For baseboard implementations, the CLK pin shall be connected to the Primary Connector. The CLK pin shall be tied directly to GND if the scan chain is not used.
			For NIC implementations, the CLK pin shall be connected to Shift Registers 0 & 1, and optionally connected to Shift Registers 2 & 3 (if implemented) as defined in the text and Figure 82, below. The CLK pin shall be pulled up to +3.3V_EDGE through a 1kOhm resistor.
DATA_OUT	OCP_B5	Output	Scan clock data output from the baseboard to the OCP NIC 3.0 card. This bit stream is used to shift in NIC configuration data.
			For baseboard implementations, the DATA_OUT pin shall be connected to the Primary Connector. The DATA_OUT pin shall be tied directly to GND if the scan chain is not used.
			For NIC implementations, the DATA_OUT pin may be left floating if it is not used for OCP NIC 3.0 card configuration. The DATA_OUT pin shall be pulled up to +3.3V_EDGE through a 1kOhm resistor.
DATA_IN	OCP_B4	Input	Scan clock data input to the baseboard. This bit stream is used to shift out NIC status bits.
			For baseboard implementations, the DATA_IN pin shall be pulled up to +3.3V_EDGE through a 10kOhm resistor to prevent the input signal from floating if a card is not installed. This pin may be left as a no connect if the scan chain is not used.

			For NIC implementations, the DATA_IN scan chain is required. The DATA_IN pin shall be connected to Shift Registers 0 & 1, as defined in the text and Figure 82.
LD#	OCP_B3	Output	Scan clock shift register load. Used to latch configuration data on the OCP NIC 3.0 card.
			For baseboard implementations, the LD# pin shall be pulled up to +3.3V_EDGE through a 1kOhm resistor if the scan chain is not used to prevent the OCP NIC 3.0 card from erroneous data latching.
			For NIC implementations, the LD# pin implementation is required. The LD# pin shall be connected to Shift Registers 0 & 1 as defined in the text and Figure 82. The LD# pin shall be pulled up to +3.3V_EDGE through a 1kOhm resistor.

Figure 81: Example Scan Chain Timing Diagram

🆴 /scan_chain_example/CLK 🏷 /scan_chain_example/LD_N [byte0[7:0] | byte1[7:0] | byte2[7:0] | byte3[7:0] [byte0[7:0] [byte1[7:0] [byte2[7:0] [byte0[7:0] [byte1[7:0] (byte3[7:0] (byte2[7:0] (byte1[7:0] (byte0[7:0] [byte3[7:0] [byte2[7:0] [byte1[7:0] [byte3[7:0] [byte2[7:0] byte0[7:0]

The scan chain provides side band status indication between the OCP NIC 3.0 card and the baseboard. The scan chain bit definition is defined in the two tables below. The scan chain data stream is 32-bits in length for both the DATA OUT and the DATA IN streams. The scan chain implementation is optional on the host, but is mandatory on all OCP NIC 3.0 cards. The scan chain components operates on the +3.3V EDGE power domain.

The DATA OUT bus is an output from the host. The DATA OUT bus provides initial configuration options to the OCP NIC 3.0 card. At the time of this writing, the default implementation does not use the DATA_OUT stream and is not implemented on the NIC. However, all baseboard systems that implement the Scan Chain shall connect DATA_OUT between the platform and the Primary Connector for futureproofing NIC implementations and subsequent revisions of this specification.

Byte.bit	DATA_OUT Field	Default	Description
	Name	Value	
0.[07]	RSVD	0b000000	Reserved. Byte 0 value is 0h00.
1.[07]	RSVD	0h00	Reserved. Byte 1 value is 0h00.
2.[07]	RSVD	0h00	Reserved. Byte 2 value is 0h00.
3.[07]	RSVD	0h00	Reserved. Byte 3 value is 0h00.

Table 27: Pin Descriptions – Scan Chain DATA_OUT Bit Definition

The DATA_IN bus is an input to the host and provides NIC status indication. The default implementation is completed with two 8-bit 74LV165 parallel in to serial out shift registers in a cascaded implementation. Up to four shift registers may be implemented to provide additional NIC status indication to the host platform.

DATA_IN shift registers 0 & 1 shall be mandatory for scan chain implementations. DATA_IN shift registers 2 & 3 are optional depending on the card type and fields being reported to the host. DATA_IN shift register 2 may be used to indicate future definitions of the scan chain bit stream. DATA_IN shift registers 3 (in conjunction with shift register 2) are required for reporting link/activity indication on card implementations with 5-8 ports.

The host should read the DATA_IN bus multiple times to qualify the incoming data stream. The number of data qualification reads is dependent on the baseboard implementation.

A 1kOhm pull up resistor shall be implemented on the NIC to the SER input of the last shift register on the DATA_IN scan chain to maintain a default bit value of 0b1 for unused bits for implementations using less than four shift registers.

Table 28: Pin Descriptions – Scan Bus DATA_IN Bit Definition

Byte.bit	DATA_OUT Field	Default	Description
	Name	Value	
0.0	PRSNTB[0]#	0bX	PRSNTB[3:0]# bits shall reflect the same state as
0.1	PRSNTB[1]#	0bX	the signals on the Primary Connector.
0.2	PRSNTB[2]#	0bX	
0.3	PRSNTB[3]#	0bX	
0.4	WAKE_N	0bX	PCIe WAKE_N signal shall reflect the same state as the signal on the Primary Connector.
0.5	TEMP_WARN_N	0b1	Temperature monitoring pin from the on-card thermal solution. This pin shall be asserted low when temperature sensor exceeds the temperature warning threshold.
0.6	TEMP_CRIT_N	0b1	Temperature monitoring pin from the on-card thermal solution. This pin shall be asserted low when temperature sensor exceeds the temperature critical threshold.
0.7	FAN_ON_AUX	0b0	When high, FAN_ON_AUX shall request the system fan to be enabled for extra cooling in the S5 state.
1.0	LINK_ACT_P0	0b1	Port 03 link/activity indication. Active low.
1.1	LINK_ACT_P1	0b1	
1.2	LINK_ACT_P2	0b1	0b0 – Link LED is illuminated on the host platform.
1.3	LINK_ACT_P3	0b1	0b1 – Link LED is not illuminated on the host platform.
			Steady = link is detected on the port. Blinking = activity is detected on the port. The blink rate should blink low for 50-500ms during activity periods.

			Off = the physical link is down or disabled
1.4	SPEED_A_P0	0b1	Port 03 speed A (max rate) indication. Active low.
1.5	SPEED_A_P1	0b1	
1.6	SPEED A P2	0b1	0b0 – Port is linked at maximum speed.
1.7	SPEED_A_P3	0b1	0b1 – Port is not linked at the maximum speed or no link is present.
2.0	ScanChainVer[0]	0b1	ScanChainVer[1:0] shall be used to indicate the
2.1	ScanChainVer[1]	0b1	scan chain bit definition version. The encoding shall be as follows:
			Ob11 – Scan chain bit definition version 1 corresponding to OCP NIC 3.0 version 1.0.
2.2	DC//D	Ol- 4	All other encoding values shall be reserved.
2.2	RSVD	0b1	Byte 2 bits [2:7] are reserved. These bits shall
2.3	RSVD	0b1	default to the value of 0b1. These bits may be used
2.4	RSVD	0b1	in future versions of the scan chain.
2.5	RSVD	0b1	
2.6	RSVD	0b1	
2.7	RSVD	0b1	
3.0	LINK_ACT_P4	0b1	Port 47 link/activity indication. Active low.
3.1	LINK_ACT_P5	0b1	
3.2	LINK_ACT_P6	0b1	0b0 – Link LED is illuminated on the host platform.
3.3	LINK_ACT_P7	0b1	0b1 – Link LED is not illuminated on the host platform.
			Steady = link is detected on the port. Blinking = activity is detected on the port. The blink rate should blink low for 50-500ms during activity periods. Off = the physical link is down or disabled
3.4	SPEED_A_P4	0b1	Port 47 speed A (max rate) indication. Active low.
3.5	SPEED_A_P5	0b1	
3.6	SPEED_A_P6	0b1	0b0 – Port is linked at maximum speed.
3.7	SPEED_A_P7	0b1	Ob1 – Port is not linked at the maximum speed or no link is present.

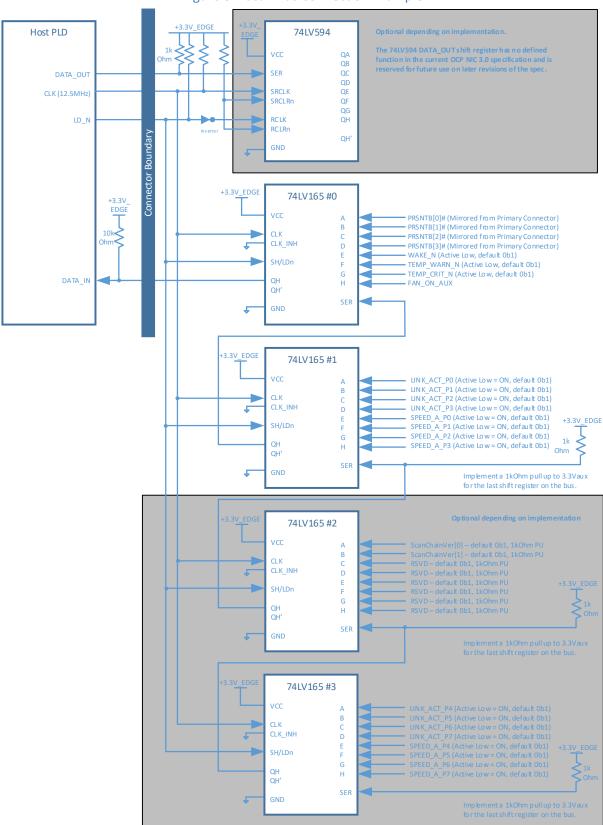


Figure 82: Scan Bus Connection Example

3.5.4 Primary Connector Miscellaneous Pins – OCP Bay (Primary Connector)

This section provides the miscellaneous pin assignments for the pins on the Primary Connector OCP Bay. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0 and Section 3.12. An example NIC_PWR_GOOD connection diagram is shown in Figure 78.

Table 29: Pin Descriptions – Miscellaneous 2

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
MAIN_PWR_EN	OCP_B2	Output	Main Power Enable. Active high.
			This pin indicates that the +12_EDGE and +3.3V_EDGE power is from the baseboard main power rails. Additionally, this signal notifies the OCP NIC 3.0 card to enable any power supplies that run only in the Main Power Mode.
			The MAIN_PWR_EN pin is driven by the baseboard. This pin must be implemented on baseboard systems, but may optionally be used by the OCP NIC 3.0 card depending on the end point silicon implementation. Depending on the silicon vendor, end point devices may be able to operate in a single power domain, or may require separate power domains to function.
			For baseboard implementations, this signal shall be pulled down to GND through a 10kOhm resistor on the baseboard. This ensures the OCP NIC 3.0 card power is disabled until instructed to turn on by the baseboard.
			When low, the OCP NIC 3.0 card supplies running on main power shall be disabled.
			When high, the OCP NIC 3.0 card supplies running on main power shall be enabled.
			This pin may be left as a no connect for OCP NIC 3.0 cards that do not use a separate "main power" domain SVR circuitry.
NIC_PWR_GOOD	OCP_B1	Input	NIC Power Good. Active high. This signal is driven by the OCP NIC 3.0 card.
			When high, this signal shall indicate that all of the OCP NIC 3.0 card power rails are operating within nominal tolerances. Where appropriate, designs that have a separate Main Power domain indication

			should also connect to the NIC_PWR_GOOD signal via a FET to isolate the domains. Refer to Figure 78 in Section 3.4.4 for an example implementation.
			When low, this signal shall indicate that, AUX_PWR_EN is deasserted, the OCP NIC 3.0 card power supplies are not yet within nominal tolerances or are in a fault condition.
			Further, for cards that implement a MAIN_PWR_EN signal, the NIC_PWR_GOOD signal also indicates if main power is good. This indication may only be qualified in the main power mode when MAIN_PWR_EN is asserted. Refer to Figure 78 in Section 3.4.4 for an example implementation
			For baseboards, this pin may be connected to the platform I/O hub as a NIC power health status indication. This signal shall be pulled down to ground with a 100kOhm resistor on the baseboard to prevent a false power good indication if no OCP NIC 3.0 card is present.
			For OCP NIC 3.0 cards this signal shall indicate the OCP NIC 3.0 card power is "good." This signal may be implemented by combinatorial logic, a cascaded power good tree or a discrete power good monitor output.
			When high, this signal should be treated as V_{REF} is available for NC-SI communications. Refer to timing parameter T4 in the DMTF DSP0222 specification for details.
			It is expected that a baseboard will not drive signals other than SMBus and the Scan Chain to the OCP NIC 3.0 card when this signal is low.
GND	OCP_A6 OCP_A10 OCP_A13 OCP B10 OCP_B13	GND	Ground return; a total of 5 ground pins are on the OCP bay area.

3.6 PCle Bifurcation Mechanism

OCP NIC 3.0 baseboards and OCP NIC 3.0 cards support multiple bifurcation combinations. Single socket baseboards with a single or multiple root ports, as well as a multi-socket baseboards with a single or

multiple root ports are supported. The bifurcation mechanism also supports OCP NIC 3.0 cards with a single or multiple end points. These features are accomplished via I/O pins on the Primary and Secondary Connector:

- PRSNTA#, PRSNTB[3:0]#. The PRSNTA# pin shall connect to the PRSNTB# pins as a hard coded value on the OCP NIC 3.0 card. The encoding of the PRSNTB[3:0]# pins allows the baseboard to determine the PCIe Links available on the OCP NIC 3.0 card.
- BIF[3:0]#. The BIF# pin states shall be controlled by the baseboard to allow the baseboard to
 override the default end point bifurcation for silicon that support bifurcation. Additional
 combinatorial logic is required and is specific to the card silicon. The combinatorial logic is not
 covered in this specification. The BIF[3:0]# pins may optionally be hardcoded for baseboards
 that do not require a dynamic bifurcation override.

A high level bifurcation connection diagram is shown in Figure 76.

3.6.1 PCIe OCP NIC 3.0 Card to Baseboard Bifurcation Configuration (PRSNTA#, PRSNTB[3:0]#)

The OCP NIC 3.0 card to baseboard configuration mechanism consists of four dual use pins (PRSNTB[3:0]#) on the OCP NIC 3.0 card and a grounded PRSNTA# pin on the baseboard. These pins provide card presence detection as well as mechanism to notify the baseboard of the pre-defined PCIe lane width capabilities. The PRSNTB[3:0]# pins are pulled up to +3.3V_EDGE on the baseboard and are active low signals. A state of 0b1111 indicates that no card is present in the system. Depending on the capabilities of the OCP NIC 3.0 card, a selection of PRSNTB[3:0]# signals may be strapped to the PRSNTA# signal and is pulled low by the baseboard. The encoding of the PRSTNB[3:0]# bits is shown in Table 30 for x16 and x8 PCIe cards.

3.6.2 PCIe Baseboard to OCP NIC 3.0 Card Bifurcation Configuration (BIF[2:0]#)

Three signals (BIF[2:0]#) are driven by the baseboard to notify requested bifurcation on the OCP NIC 3.0 card silicon. This allows the baseboard to set the lane configuration on the OCP NIC 3.0 card that supports multiple bifurcation options.

For example, a baseboard that has four separate hosts that support a 4 x4 connection, should appropriately drive the BIF[2:0]# pins per Table 30 and indicate to the OCP NIC 3.0 card silicon to setup a 4 x4 configuration.

As previously noted, the BIF[2:0]# signals require additional combinatorial logic to decode the BIF[2:0]# value and appropriately apply it to the end-point silicon. The combinatorial logic is not covered in the specification as its implementation is specific to the vendor silicon used.

3.6.3 PCIe Bifurcation Decoder

The combination of the PRSNTB[3:0]# and BIF[2:0]# pins deterministically sets the PCIe lane width for a given combination of baseboard and OCP NIC 3.0 cards. Table 30 shows the resulting number of PCIe links and its width for known combinations of baseboards and OCP NIC 3.0 cards.

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*Note: The baseboard must disable PCIe lanes during the initialization phase if the number of detected PCIe links are greater than what is supported on the baseboard to prevent a nondeterministic solution. For example, if the baseboard only supports a 1 x16 connection, and the OCP NIC 3.0 card only supports a 2 x8 connection, the baseboard must disable PCIe lanes 8-15 to prevent any potential LTSSM issues during the discovery phase.

Table 30: PCle Bifurcation Decoder for x16 and x8 Card Widths

					Single Host	Host			RSVD	Dual Host	Quad Host	Quad Host	
		Host	1Host	1 Host	1 Host	1 Host	1 Host	1 Host	RSVD	2 Hosts	4 Hosts	4 Hosts	
		Host CPU Sockets	1 Upstream Socket	1 Upstream Socket	1Upstream Socket	2 Upstream Sockets	1 Upstream Socket 1 Upstream Socket 2 Upstream Sockets 4 Upstream Sockets	4 Sockets (1 Socket per Host) First 8 PCle lanes	RSVD	2 Upstream Sockets (1 Socket per Host)	4 Upstream Sockets (1 Socket per Host)	4 Sockets (1 Socket per Host) First 8 PCle lanes	_
	Network Card – Supported PCIe Configurations	Total PCIe Links	1 Link (No Bifurcation)	1 or 2 Links	1, 2, or 4 Links	2 Links	4 Links	4 x2 links	RSVD	2 Links	4 Links	4 x2 links	
		System Support	1x16, 1x8, 1x4, 1x2, 1x1	1x16, 1x8, 1x4, 1x2, 1x1	1x16,1x8,1x4,1x2,1x1	1x8,1x4,1x2,1x1			RSVD	2.00 Suc			
Minimum				200,204,205,201	4×4 4×7 4×1	2 no, 2 nt, 2 n2, 2n1	4×4 4×2 4×1	4×2 4×1		200,204,205,201	4×4 4×2 4×1	4×2 4×1	L
Required		System Encoding BIF[2:0]#	00000	00000	00000	00001	01000	06011	09100	0b101	0P110	0b111	
	Card Short Supported Bifurcation	Add-in-Card Encoding		ı		1					ı	ı	
П	1000	Object 11	DSM - Pard not prepare in the sustem	the custom									L
		061110	1.8	1×8	9×F	9%	4%.	1,42		1.88	1×4	1×2	
1	1x8 Option A					(Socket 0 only)	(Socket 0 only)	(Socket 0 only)		(Host 0 only)	(Host 0 only)	(Host Donly)	
	1×4, 1×2, 1×1 1×4	0b1 110	184	1×4	1×4	1x4 (Socket 0 only)	1x4 (Socket 0 only)	1x2 (Socket 0 only)		1x4 (Host 0 only)	1x4 (Host 0 only)	1x2 (Host 0 only)	
	142,181	0b1 110	1 _K 2	142	142	1 _{HZ} (Socket 0 only)	1 _H 2 (Socket 0 only)	1 _H 2 (Socket 0 only)		1 _N 2 (Host 0 only)	1 _K 2 (Host 0 only)	1x2 (Host 0 only)	
	181	0b1 110	181	TRI.	181	1x1 (Socket 0 only)	1x1 (Socket 0 only)	1x1 (Socket 0 only)		1x1 (Host 0 only)	1x1 (Host 0 only)	1k1 (Host 0 only)	
	1x8, 1x4, 1x2, 1x1 1x8 Option B 2x4, 2x2, 2x1	0b1 101	188	8×F	8×	1x8 (Sooket 0 only)	2×4	2 x2 (Sooket 0 & 2 only)		1x8 (Host 0 only)	2×4	2 x2 (Host 0 & 2 only)	
	2x8,2x4,2x2,2x1 2x8 Dption B 4x4,4x2,4x1	0b1 101	1x8°	2x8	2×8	2×8	4×4	2x2 (Sooket 0 & 2 only)		2×8	4×4	2 x 2 (Host 0 & 2 only)	
	1x8,1x4 2x4, 1x8 Option D 4x2 (First 8 lanes), 4x1	0b11 00	1x8	188	1×8	1x8 (Socket 0 only)	2×4	4 %2		1x8 (Host 0 only)	2 ×4	4 %2	
	1x16.1x8,1x4 2x8,2x4, 1x16.0ption D 4x4,4x2 (First 8lanes),4x1	0b1 100	1×16	1×15	1×16	2×8	4%4	4 % 2	1	2×8	4 84	4×2	
	RSVD RSVD	0b1 011	RSVD - The encoding of 0	b1011 is reserved due to in	sufficient spacing between	n PRSNTA and PRSNTB2	RSVD - The encoding of 0b1011 is reserved due to insufficient spacing between PRSNIA and PRSNIB2 pin to provide positive card identification.	d identification.					
	Ž.	051 010	184	184	2 ×4	1x4 (Socket 0 only)	2×4	2 x2 (Socket 0 & 2 only)		1x4 (Host 0 only)	2×4	2 x2 (Host 0 & 1 only)	
	4 k.2 (First 8 lanes), 4 k.1 2 k.2, 2 k.1 4 k.2 1 k.2, 1 k.1	0b1 001	142	142	2 + 2	1x2 (Socket 0 only)	2 42	4 14.2		1x2 (Host 0 only)	2 11.2	4 112	
		1 0b1000											
	1x16.1x8,1x4,1x2,1x1 1x16 Option A	050111	31×1	1×16	1×16	1x8 (Socket 0 only)	1x4 (Sooket 0 only)	1x2 (Socket 0 only)	ı	1x8 (Host 0 only)	1x4 (Host 0 only)	1x2 (Host 0 only)	_
	2x8,2x4,2x2,2x1 2x8 Option A	060110	188	2 x8	2 x8	2×8	2 x4 (Socket 0 & 2 only)	2 x2 (Socket 0 & 2 only)		2×8	2x4 (Host 0 & 2 only)	1x2 (Host 0 & Tonly)	
	1x16,1x8,1x4,1x2,1x1 1x16 Option B 2x8,2x4,2x2,2x1	060 101	1x16	1x16	1×16	2 и8	2 x4 (Socket 0 & 2 only)	1x2 (Socket 0 only)		2м8	2x4 (Host 0 & 2 only)	2x2 (Host 0& Tonly)	
	1x16, 1x8, 1x4 2x8, 2x4, 2x2, 2x1 1x16 Option C, 4x4, 4x2, 4x1	060100	1816	1×16	1×16	2 ×8	4×4	2 x2 (Socket 0 & 2 only)		2 x8	4×4	2 x2 (Host 0 & 1 only)	
	4×4, 4×2, 4×1	060 011	1×4°	2×4*	4 84	2x4 (EP 0 and 2 only)	4×4	4 x2 (Socket 0 & 2 only)		2x4 (EP 0 and 2 only)	4 x4	4 x2 (Host 0 & Tonly)	
		060 010											
		000001	-										
		0P0 000		-	-	-	-	-		-	-	-	

3.6.4 Bifurcation Detection Flow

The following detection flow shall be used to determine the resulting link count and lane width based on the baseboard and OCP NIC 3.0 card configurations.

- 1. The baseboard shall read the state of the PRSNTB[3:0]# pins. An OCP NIC 3.0 card is present in the system if the resulting value is not 0b1111.
- 2. Firmware determines the OCP NIC 3.0 card PCIe lane width capabilities per Table 30 by reading the PRSNTB[3:0]# pins.
- 3. The baseboard reconfigures the PCIe bifurcation on its ports to match the highest common lane width and lowest common link count on the card.
- 4. For cases where the baseboard request a link count override (such as requesting a 4-host baseboard requesting 4 x4 operation on a supported card that would otherwise default to a 2 x8 case), the BIF[0:2]# pins shall be asserted as appropriate. Asserting the BIF[0:2]# pins assumes the OCP NIC 3.0 card supports the requested link override.
- 5. The BIF[0:2]# pins must be in their valid states upon the assertion of PWR_EN.
- 6. PWR EN is asserted.
- 7. A OCP NIC 3.0 card is allowed 25ms between PWR_EN assertion and NIC_PWR_GOOD assertion.
- 8. PERST# shall be deasserted >1s after NIC_PWR_GOOD assertion as defined in Figure 91. Refer to Section 3.12 for timing details.

3.6.5 PCIe Bifurcation Examples

For illustrative purposes, the following figures show several common bifurcation permutations.

3.6.5.1 Single Host (1 x16) Baseboard with a 1 x16 OCP NIC 3.0 Card (Single Controller)

Figure 83 illustrates a single host baseboard that supports x16 with a single controller OCP NIC 3.0 card that also supports x16. The PRSTNB[3:0]# state is 0b0111. The BIF[2:0]# state is 0b000 as there is no need to instruct the end-point network controller to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16. The single host baseboard determines that it is also capable of supporting 1 x16. The resulting link width is 1 x16.

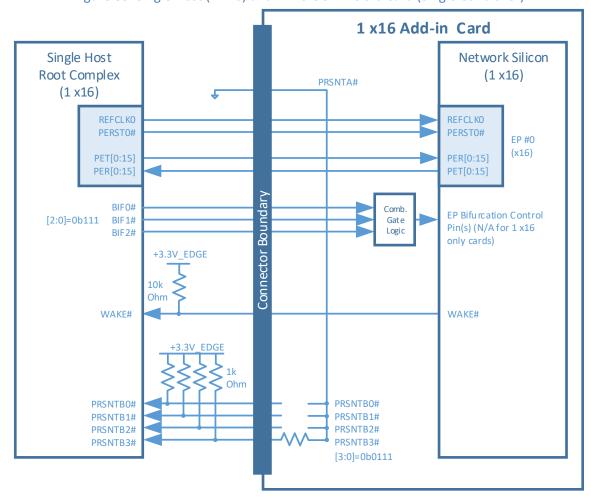


Figure 83: Single Host (1 x16) and 1 x16 OCP NIC 3.0 Card (Single Controller)

3.6.5.2 Single Host (2 x8) Baseboard with a 2 x8 OCP NIC 3.0 Card (Dual Controllers)

Figure 84 illustrates a single host baseboard that supports 2 x8 with a single controller OCP NIC 3.0 card that also supports 2 x8 with dual controllers. The PRSTNB[3:0]# state is 0b0110. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 2 x8. The single host baseboard determines that it is also capable of supporting 2 x8. The resulting link width is 2 x8.

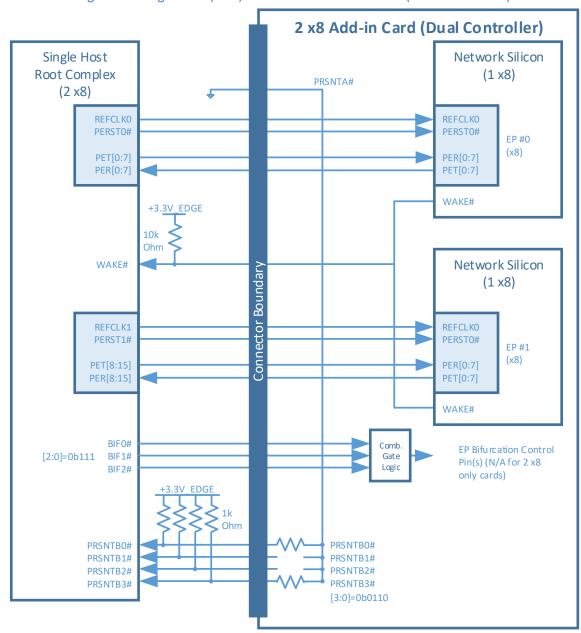


Figure 84: Single Host (2 x8) and 2 x8 OCP NIC 3.0 Card (Dual Controllers)

3.6.5.3 Quad Host (4 x4) Baseboard with a 4 x4 OCP NIC 3.0 Card (Single Controller)

Figure 85 illustrates a quad host baseboard that supports 4 x4 with a single controller OCP NIC 3.0 card that supports 1 x16, 2 x8 and 4 x4. The PRSTNB[3:0]# state is 0b0011. The BIF[2:0]# state is 0b101 as the end point network controller is forced to bifurcate to 4 x4. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16, 2 x8 and 4 x4. The quad host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

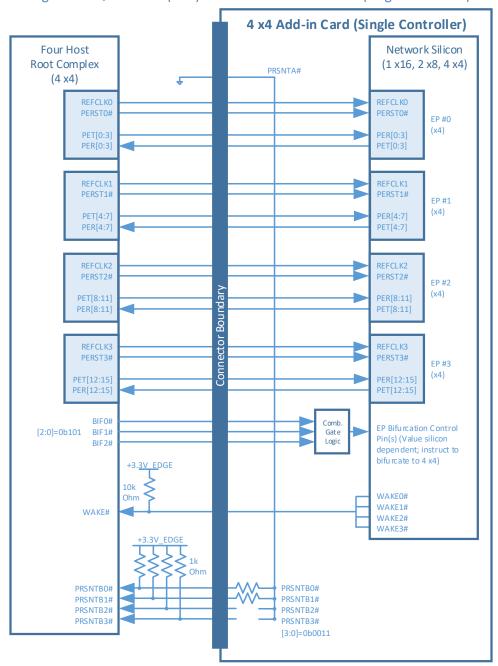


Figure 85: Quad Hosts (4 x4) and 4 x4 OCP NIC 3.0 Card (Single Controller)

3.6.5.4 Quad Host (4 x4) Baseboard with a 4 x4 OCP NIC 3.0 Card (Quad Controllers)

Figure 86 illustrates a quad host baseboard that supports 4 x4 with a quad controller OCP NIC 3.0 card that supports 4 x4. The PRSTNB[3:0]# state is 0b0011. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 4 x4. The quad host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

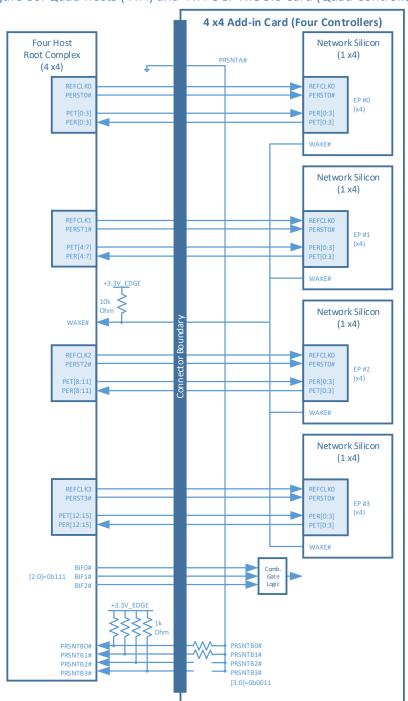


Figure 86: Quad Hosts (4 x4) and 4 x4 OCP NIC 3.0 Card (Quad Controllers)

3.6.5.5 Single Host (1 x16, no Bifurcation) Baseboard with a 2 x8 OCP NIC 3.0 Card (Dual Controller)

Figure 87 illustrates a single host baseboard that supports 1 x16 with a dual controller OCP NIC 3.0 card that supports 2 x8. The PRSTNB[3:0]# state is 0b0110. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 2 x8. The quad host baseboard determines that it is capable of 1x 16, but down shifts to 1 x8. The resulting link width is 1 x8 and only on endpoint 0.

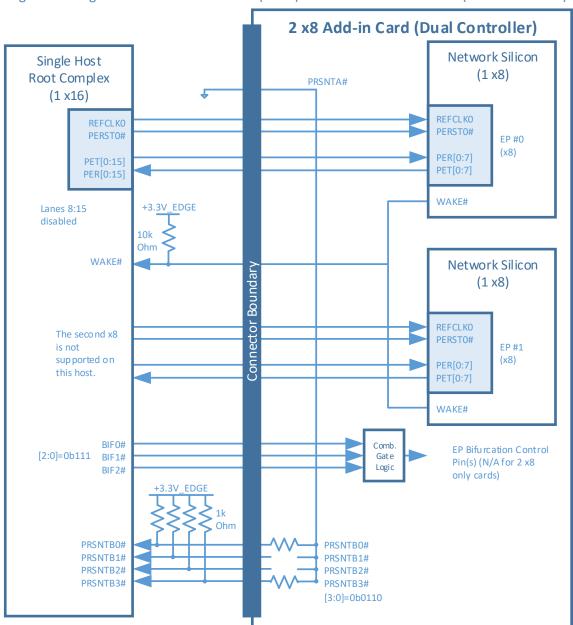


Figure 87: Single Host with no Bifurcation (1 x16) and 2 x8 OCP NIC 3.0 Card (Dual Controllers)

3.7 PCIe Clocking Topology

The OCP NIC 3.0 specification allows for up to four PCIe REFCLKs on the Primary Connector and up to two PCIe REFCLKs on the Secondary Connector. In general, the association of each REFCLK is based on the PCIe Link number on a per connector basis and is shown in Table 31. Cards that implement both the Primary and Secondary Connectors have a total of up to 6 REFCLKs.

REFCLK #	Description	Availability (Connector)
REFCLK0	REFCLK associated with Link 0.	Primary and Secondary Connectors.
REFCLK1	REFCLK associated with Link 1.	Primary and Secondary Connectors.
REFCLK2	REFCLK associated with Link 2.	Primary Connector only.
REFCLK3	REFCLK associated with Link 3.	Primary Connector only.

Table 31: PCIe Clock Associations

For each OCP NIC 3.0 card, the following REFCLK connection rules must be followed:

- For a 1 x16 capable OCP NIC 3.0 card, REFCLKO shall be used for lanes [0:15].
- For a 2 x8 capable OCP NIC 3.0 card, REFCLKO shall be used for lanes [0:7] and REFCLK1 shall be used for lanes [8:15].
 - For a 4 x4 capable OCP NIC 3.0 card, REFCLK0 shall be used for lanes [0:3], REFCLK1 shall be used for lanes [4:7], REFCLK2 shall be used for lanes [8:11] and REFCLK3 shall be used for lanes [12:15]. Pins for REFCLK2 and REFCLK3 are described in Section 3.5.1 and are located on the 28-pin OCP bay.

Root Complex Network Silicon **Root Complex** Network Silicon (1 x16) (1 x16) (2 x8) (2 x8) REECLKO REFCLKO REECLKO REFCLKO Connector Boundary PERSTO# PERSTO# PERSTO: PERSTO# FP #0 FP #0 PER[0:15] PER[0:7] PET[0:15] PET[0:7 PER[0:15] PET[0:15] PER[0: PET[0:7] REFCLK1 REFCLK1 +3.3<u>V</u> EDGE PERST1# PERST1# 10k PER[8:15] PER[8:15] PET[8:15] WAKE# +3.3V_EDGE 10k WAKEO# WAKE1#

Figure 88: PCIe Interface Connections for 1 x16 and 2 x8 OCP NIC 3.0 Cards

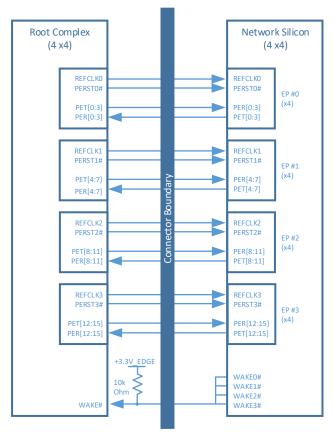


Figure 89: PCIe Interface Connections for a 4 x4 OCP NIC 3.0 Card

3.8 PCle Bifurcation Results and REFCLK Mapping

For the cases where the baseboard and OCP NIC 3.0 card bifurcation are permissible, this section enumerates all of the supported PCIe link, lane and REFCLK mappings for each supported configuration. The bifurcation decoder is shown in Section 3.6.3.

Table 32: Bifurcation for Single Host, Single Socket and Single Upstream Link (BIF[2:0]#=0b000)

	Lane 15		0.			-,	Host	Host 0		Link 0, Lane 15				- 6	Link 0,	Host (Link 0, Lane 15	Link 0, Lane 15	Host		
		-					t Ho	t Ho							_		_	_	t Ho		
	3 Lane 14	-					Host ed Disable	Host ed Disable) Link 0, 3 Lane 14					, Link 0, 3 Lane 14	Host ed Disable) Link 0, 3 Lane 14	, Link 0, 3 Lane 14	Host Pd Disable		
	Lane 13	-					Host d Disable	Host d Disable		Link 0, Lane 13					Link 0, Lane 13	Host d Disable	Link 0, Lane 13		Host d Disable		
	Lane 12	-					Host Host Host Host Host Host Host Host	Host Host Host Host Host Host Host Host		Link 0, Lane 12					Link 0, Lane 12	Host Host Host Host Host Host Host Host	Link 0, Lane 12		Host Host Host Host Host Host Disabled		
	Lane 11						Host Disabled	Host Disabled		Link 0, Lane 11					Link 0, Lane 11	Host Disabled	Link 0, Lane 11		Host		
	Lane 10						Host Disabled	Host Disabled		Link 0, Lane 10					Link 0, Lane 10	Host Disabled	Link 0, Lane 10	Link 0, Lane 10	Host		
	6 aue 7						Host Disabled	Host Disabled		Link 0, Lane 9					Link 0, Lane 9	Host Disabled	Link 0, Lane 9	Link 0, Lane 9	Host Disabled		
	Lane 8						Host Disabled	Host Disabled		Link 0, Lane 8					Link 0, Lane 8	Host Disabled	Link 0, Lane 8	Link 0, Lane 8	Host Host Host Host Host Host Host Host		
ĺ	Lane 7		Link 0, Lane 7				Link 0, Lane 7	Link 0, Lane 7	Link 0, Lane 7	Link 0, Lane 7					Link 0, Lane 7	Link 0, Lane 7	Link 0, Lane 7	Link 0, Lane 7	Host		
İ	Lane 6		Link 0, Lane 6				Link 0, Lane 6	Link 0, Lane 6	Link 0, Lane 6	Link 0, Lane 6					Link 0, Lane 6	Link 0, Lane 6	Link 0, Lane 6	Link 0, Lane 6	Host		
l	Lane 5		Link 0, Lane 5				Link 0, Lane 5	Link 0, Lane 5	Link 0, Lane 5	Link 0, Lane 5					Link 0, Lane 5	Link 0, Lane 5	Link 0, Lane 5	Link 0, Lane 5	Host isabled		l
Ì	Lane 4		Link 0, Lane 4				Link 0, Lane 4	Link 0, Lane 4	Link 0, Lane 4	Link 0, Lane 4					Link 0, Lane 4	Link 0, Lane 4	Link 0, Lane 4	Link 0, Lane 4	Host isabled D		ı
l	Lane 3		Link 0, Lane 3	Link 0, Lane 3			Link 0, Lane 3	Link 0, Lane 3	Link 0, Lane 3	Link 0, Lane 3		Link 0, Lane 3			Link 0, Lane 3	Link 0, Lane 3	Link 0, Lane 3	Link 0, Lane 3	Link 0, Lane 3 D		
	Lane 2		Link 0, Lane 2	Link 0, Lane 2			Link 0, Lane 2	Link 0, Lane 2	Link 0, Lane 2	Link 0, Lane 2		Link 0, Lane 2			Link 0, Lane 2	Link 0, Lane 2	Link 0, Lane 2	Link 0, Lane 2	Link 0, Lane 2		l
	Lane 1		Link 0, Lane 1				Link 0, Lane 1	Link 0, Lane 1		Link 0, Lane 1		Link 0, Lane 1	Link 0, Lane 1		Link 0, Lane 1	Link 0, Lane 1	Link 0, Lane 1		Link 0, Lane 1		
ŀ	Lane 0		Link 0, Lane 0	-		Link 0, Lane 0	Link 0, Lane 0	Link 0, Lane 0	Link 0, Lane 0	Link 0, Lane 0		Link 0, Lane 0			Link 0, Lane 0	Link 0, Lane 0	Link 0, Lane 0		Link 0, Lane 0		
	Resulting Link		1 x8	1×4	1x2	1x1	1x8	1×8*	1 x8	1×16		1 ×4	1 x2		1×16	1×8*	1×16	1×16	1 x4*		
	BIF[2:0]#	00000	00090	00090	00090	00090	00090	00090	00000	00000	00000	00090	00000	00000	00090	00090	00090	000000	00090	00000	
	Upstream Links	1 Link	1 Link	1 Link	1 Link	1 Link	1 Link	1 Link	1 Link	1 Link	1 Link	1 Link	1 Link	1 Link	1 Link	1 Link	1 Link	1 Link	1 Link	1 Link	
	Upstream Devices	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	
	Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	
	Add-in-Card Encoding PRSNTB[3:0]#	0b1111	0b1110	0b1110	001110	051110	061101	0b1101	0b1100	0b1100	0b1011	001010	0b1001	0b1000	060111	00110	000101	000100	050011	000010	
il	Supported Bifurcation Modes	Card Not Present	1 x8, 1 x4, 1 x2, 1 x1	1 x4, 1 x2, 1 x1	1x2,1x1	1x1	1 x8, 1 x4, 1 x2, 1 x1 1 x8 Option B 2 x4, 2 x2, 2 x1	2 x8, 2 x4, 2 x2, 2 x1 2 x8 Option B 4 x4, 4 x2, 4 x1	nes) 4x1	4 x1		x2, 2 x1 x2, 1 x1	ines), 4 x1	RSVD for future x8 encoding	1 x16, 1 x8, 1 x4, 1 x2, 1 x1	2 x8, 2 x4, 2 x2, 2 x1	1 x16, 1 x8, 1 x4, 1 x2, 1 x1 2 x8, 2 x4, 2 x2, 2 x1			RSVD	
1034, 211514 - 41	Min Card Card Short Width Name	Not Present	1 x8 Option A	1 x4	1x2	1×1	1 x8 Option B	2 x8 Option B	1 x8 Option D	1 x16 Option D	RSVD	2 x4	4 x2	RSVD	1 x16 Option A	2 x8 Option A	1 x16 Option B	1 x16 Option C	4 ×4	RSVD	
П	n Can /idth	n/a	JC 3C	l z	20	20	30	40	20	- P	RSVD	30	30	RSVD	9	40	Q 40	40	4C	RSVD	-

Table 33: Bifurcation for Single Host, Single Socket and Single/Dual Upstream Links (BIF[2:0]#=0b000)

Host Upstream Socket 10-21lins 00000 Lane Lane Lane Lane Disabled Di	1 Host 1 Upstream Socket 1 or 2 Links 00000 1 one 0 1	1 Host 1 Upstream Socket 1 or 2 Links 00000 1 or 2 Links 1 Upstream Socket 1 or 2 Links 00000 1 or 2 Links 1 Upstream Socket 1 or 2 Links 00000 1 or 2 Links 1 Upstream Socket 1 or 2 Links 00000 1 or 2 Links 1 Upstream Socket 1 or 2 Links 1 Upstream Socket 1 or 2 Links 0 00000 1 or 2 Links 1 Upstream Socket 1 or 2 Links 0 00000 1 or 2 Links 1 Upstream Socket 1 Upstream Socket 1 or 2 Links 1 Upstream Socket 1 or 2 Links 1 Upstream Socket 1 or 2 Links 1 Upstream Socket 1 Upstream Socket 1 or 2 Links 1 Upstream Socket 1 Upstream Socket 1 or 2 Links 1 Upstream Socket 1 Upstream Socket 1 Upstream Socket 1 Or 2 Links 1 Upstream Socket 1 Upstre
1 Host 1 Upstream Socket 1 or 2 Links 0b000 1 Host 1 Upstream Socket 1 or 2 Links 0b000	1 Host 1 Upstream Socket 1 or 2 Links 0b000 1 Host 1 Upstream Socket 1 or 2 Links 0b000	1 Host 1 Upstream Socket 1 or 2 Links 0b000 1 Host 1 Upstream Socket 1 or 2 Links 0b000
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1 Host 1 Upstream Socket 1 or 2 Links 0b000	1 Host 1 Upstream Socket 1 or 2 Links 0b000	1 Host 1 Upstream Socket 1 or 2 Links 05000
1 Host 1 Upstream Socket 1 or 2 Links 05000	1 Host 1 Upstream Socket 1 or 2 Links 06000	1 Host 1 Upstream Socket 1 or 2 Links 0b000
The state of the s	ALTONO AL	
1 Host 1 Upstream Socket 1 or 2 Links 0b000	1 Host 1 Upstream Socket 1 or 2 Links 05000	1 Host 1 Upstream Socket 1 or 2 Links 06000
1 Host 1 Upstream Socket 1 or 2 Links 0b000	1 Host 1 Upstream Socket 1 or 2 Links 0b000	1 Host 1 Upstream Socket 1 or 2 Links 0b000
1 Host 1 Upstream Socket 1 or 2 Links 06000	1 Host 1 Upstream Socket 1 or 2 Links 05000	1 Host 1 Upstream Socket 1 or 2 Links 06000
1 Host 1 Upstream Socket 1 or 2 Links 0b000 1 Host 1 Upstream Socket 1 or 2 Links 0b000	1 Host 1 Upstream Socket 1 or 2 Links 0b000 1 Host 1 Upstream Socket 1 or 2 Links 0b000	1 Host 1 Upstream Socket 1 or 2 Links 0b000 1 Host 1 Upstream Socket 1 or 2 Links 0b000
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1 1 1 1 1 1 1 1 1 1	1 Host 1 Upstream Societ 1 or 2 Links 00000 1 or 2 Links 00000 1 or 3 Links 0	1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1	1.05 1.05	1.05 1.05
1 Host 1 Upstream Societ 1 or 2 Links 00000 2 vit Link 0 Link	1 Host 1 Upstream Societ 1 or 2 Links 00000 2 vit 1 Links 1 Li	1 Host 1 Upstream Societ 1 or 2 Links 1 Un
Host Upstream Socket 10r2 Links 00000 2 M Link 0,	Host Upstream Socket 10 72 Links 00000 2 MT Link 0, Link 0	Host Upstream Socket 1072 Links 00000 2 km² Link 0, Link 2, Link 2
1 Host 1 Upstream Socket 1 or 2 Links 00000 2 M ^{4*} Link L	1 Host 1 Upstream Socket 1 or 2 Links 00000 2 M ^{4*} Link 0, Link 0	1 Host 1 Upstream Socket 1 or 2 Links 00000 2 M ^{4*} Link 0, Link 2, Link 2
1 Host Upstream Socket 1 or 2 Links 00000 1 Host 1 Host 1 Upstream Socket 1 or 2 Links 00000 1 Host 1 Host 1 Upstream Socket 1 or 2 Links 00000 1 Host 1 Upstream Socket 1 or 2 Links 00000 1 Host 1 Upstream Socket 1 or 2 Links 00000 1 Host 1 Upstream Socket 1 Links 1 Upstream Socket	1 Host 1 Upstream Socket 1 or 2 Links 00000 2 M ⁴	1 Host Upstream Socker 1 or 2 Links Deboto Link
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Marcia M	Marcol M	Marcol M
March Marc	March Marc	March Marc
Decision 14-655 14-655 14-655 14-65	Decision 14-655	Decision 14-65 10-057 10-05
1 House 1 Ho	1 House 1 Ho	1 House 1 Ho
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Marcol M	Second Host	Second Host
Marcia M	Marcia M	March Marc
March 1962 1962 1962 1962 1962 1963 1964 1962	March 1962 1962 1962 1962 1962 1963 1963 1964 1962	March 1965
March Marc	March Marc	March Marc
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Dillo 1 Host 1 Upstream Socket 1 or 2 Links 00000 1 Host 1 Links 1 Lin	Dillo 1 Host 1 Upstream Socket 1 or 2 Links 2000 1 kg Link 0	Dillo
001100 1 Host 1 Upstream Socket 1 or 2 Links 00000 1 Host Link	001100 1140st 101pstream Socket 1 or 2 Links 00000 1 sk Link 0 Link	001100 1140st 101pstream Societ 1072 Links 00000 2.88 Link 0
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1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1
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Decision 14 Decision 14 Decision 10 of 21 Decision 14 Decisi	Deligio 110st 110streem Socket 1or 2 Links 0000 156 Link 0, Link	1
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00100 110cs 1 10cs 10cs 1 10cs 10cs 1 10cs	00100 1 Host 1 Upstream Socket 1 or 2 Links 00000 2 x8 Link 0	00100 1 1 1 1 1 1 1 1
DOLIGIO 114051 1045stream Socket 1or 2 Links 06000 1x8 Link 0	001001 114051 1045stream Socket 1 or 2 Links 00000 1 k8 Link 0 Link	001001 110031 1
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1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1
The column The	The column The	The column The
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01110	01110	01110
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14-011 1	14010 14051 140517eem Socket 1 or 2 Links 06000 141 11n0 1nn 0	14-011 1
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001110	01110	01110
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1 1 1 1 1 1 1 1 1 1	Hoss Upstream Socket 10r2 Links Coope 142 Link 0 Lin	1 1 1 1 1 1 1 1 1 1
Debilio Host Host Lipstream Socket 1 or 2 Links Debolo 1x2 Links Lin	Debilio Host Host Lipsteem Socket 1 or 2 Links Debolo 1x2 Link	Debilio Host Host Lipsteem Socket 1 or 2 Links Debolo 1x2 Linko Link
1101 11051 1015steem Socket 107 Links 1000 1x4 11nk	1101 11051 110557000000000000000000000000000000000	01110

Table 34: Bifurcation for Single Host, Single Socket and Single/Dual/Quad Upstream Links (BIF[2:0]#=0b000)

ingleh	lost, Single Ups	Single Host, Single Upstream Socket, One, Two or Four Upstream Links	Upstream Links		1 x16, 1 x8, 1 x4, 1 x2, 1 2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1																		
		Supported Bifurcation Modes	Add.in.Card							l	r	-	F	F		L	L	L	L	L		L	L
Min Card	Min Card Card Short		Encoding				BIF[2:0]#											_					
Width	Name		PRSNTB[3:0]#	Host	Upstream Devices	Upstream Links		Resulting Link	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6 La	Lane 7	Lane 8 Lar	Lane 9 Lan	Lane 10 Lane 11	11 Lane 12	12 Lane 13	13 Lane 14	4 Lane 15
n/a	Not Present	Card Not Present	0b1111	1 Host	1 Upstream Socket	1, 2, or 4 Links	00000																
2C	1 x8 Option A	1 x8, 1 x4, 1 x2, 1 x1	061110	1 Host	1 Upstream Socket	1, 2, or 4 Links	00000	1x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, I	Link 0, I	Link 0, L	Link 0, Lin Lane 6 La	Link 0, Lane 7							
2C	1 x4	1 x4, 1 x2, 1 x1	061110	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	1 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3											
3C	1x2	1 x2, 1 x1	001110	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	1x2	Link 0, Lane 0	Link 0, Lane 1													
3C	1x1	1 x 1	0b1110	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	1x1	Link 0, Lane 0														
20	1 x8 Option B	1 x8, 1 x4, 1 x2, 1 x1 1 x8 Option B 2 x4, 2 x2, 2 x1	0b1101	1 Host	1 Upstream Socket	1, 2, or 4 Links	00000	1 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, I	Link 0, I	Link 0, L	Link 0, Lin	Link 0, Hi	Host Ho	Host Ho	Host Host Disabled Disabled	st Host	t Host	Host Host Disabled Disabled	Host Pd Disabled
40	2 x8 Option B	2 x8, 2 x4, 2 x2, 2 x1 2 x8 Option B 4 x4, 4 x2, 4 x1	0b1101	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	2 x8	Link 0, Lane 0	Link 0, Lane 1			-	_			Link 1, Lin Lane 0 Lar	Link 1, Lin Lane 1 Lar	Link 1, Link 1, Lane 2 Lane 3	1, Link 1,	1, Link 1, 4 Lane 5	1, Link 1, 5 Lane 6	
		1 x8, 1 x4	0b1100	1 Host	1 Upstream Socket	1, 2, or 4 Links		1x8	Link 0,	Link 0,	Н		Н	Н	Н			H	Н	Н	Н	Н	H
2C	1 x8 Option D	2 x4, 1 x8 Option D 4 x2 (First 8 lanes), 4 x1					00000		Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5 Li		Lane 7				_			
Q4 C	1 x16 Option D	1x16,1x8,1x4 2x8,2x4, 1x16 Option D 4x4,4x2 (First 8 lanes),4x1	001100	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	1×16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, I Lane 3 I	Link 0, I Lane 4 I	Link 0, L Lane 5 Li	Link 0, Lin Lane 6 La	Link 0, Lir Lane 7 Lar	Link 0, Lin Lane 8 Lar	Link 0, Lin Lane 9 Lan	Link 0, Link 0, Lane 10 Lane 11	0, Link 0, 11 Lane 12	0, Link 0, 12 Lane 13), Link 0, 13 Lane 14), Link 0,
RSVD	RSVD	RSVD	0b1011	1 Host	1 Upstream Socket	1.2. or 4 Links	00000																L
۷	2 x4	2x4, 2x2, 2x1 1x4, 1x2, 1x1	001010	1 Host		1, 2, or 4 Links	00090	2 x4	Link 0,	Link 0,	Link 0,	Link 0,	Link 1,	Link 1, L	Link 1, Lin	Link 1,							
۽ ا	2	4 x2 (First 8 lanes), 4 x1 2 x2, 2 x1	061001	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	2 x 2	Link 0, Lane 0	Link 0, Lane 1													
RSVD	RSVD	RSVD for future x8 encoding	001000	1 Host	1 Upstream Socket	1, 2, or 4 Links	00000																
40	1 x16 Option A	1x16, 1x8, 1x4, 1x2, 1x1	060111	1 Host		1, 2, or 4 Links	00090	1×16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, I	Link 0, I	Link 0, L	Link 0, Lin Lane 6 La	Link 0, Lir Lane 7 Lar	Link 0, Lin Lane 8 Lar	Link 0, Lin Lane 9 Lan	Link 0, Link 0, ane 10 Lane 11	0, Link 0, 11 Lane 12	0, Link 0, 12 Lane 13), Link 0, 13 Lane 14), Link 0, 4 Lane 15
4C	2 x8 Option A	2 x8, 2 x4, 2 x2, 2 x1	000110	1 Host	1 Upstream Socket	1, 2, or 4 Links	00000	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, I	Link 0, I	Link 0, L	Link 0, Lin Lane 6 La	Link 0, Lir Lane 7 Lar	Link 1, Lin Lane 0 Lar	Link 1, Lin Lane 1 Lar	Link 1, Link 1, Lane 2 Lane 3	1, Link 1,	1, Link 1, 4 Lane 5	1, Link 1, 5 Lane 6	, Link 1, 6 Lane 7
4C	1 x16 Option E	1 x16, 1 x8, 1 x4, 1 x2, 1 x1 1 x16 Option B 2 x8, 2 x4, 2 x2, 2 x1	000101	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	1×16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, I	Link 0, I	Link 0, L	Link 0, Lin Lane 6 La	Link 0, Lir Lane 7 Lar	Link 0, Lin Lane 8 Lar	Link 0, Lin Lane 9 Lan	Link 0, Link 0, Lane 10 Lane 11	0, Link 0, 11 Lane 12	0, Link 0, 12 Lane 13), Link 0, 13 Lane 14), Link 0,
4C	1 x16 Option C	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 2 x2, 2 x1 1 x16 Option C 4 x4, 4 x2, 4 x1	000100	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	1×16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, I	Link 0, L	Link 0, Lin Lane 6 La	Link 0, Lir Lane 7 Lar	Link 0, Lin Lane 8 Lar	Link 0, Lin Lane 9 Lan	Link 0, Link 0, Lane 10 Lane 11	0, Link 0, 11 Lane 12	0, Link 0, 12 Lane 13), Link 0, 13 Lane 14), Link 0,
4C	4 x4	4 x4, 4 x2, 4 x1	000011	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	4 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, I Lane 3	Link 1, l	Link 1, L Lane 1 L	Link 1, Lin Lane 2 La	Link 1, Lir Lane 3 Lar	Link 2, Lin Lane 0 Lar	Link 2, Lin Lane 1 Lar	Link 2, Link 2, Lane 2 Lane 3	2, Link 3,	3, Link 3, 0 Lane 1	3, Link 3, 1 Lane 2	, Link 3, 2 Lane 3
RSVD	RSVD	RSVD	000010	1 Host	1 Upstream Socket	1, 2, or 4 Links	00000																
RSVD	RSVD	RSVD	000001	1 Host	_	1, 2, or 4 Links	00000																
RSVD	RSVD	RSVD	000000	1 Host	1 Upstream Socket	1, 2, or 4 Links	00000																

Table 35: Bifurcation for Single Host, Dual Sockets and Dual Upstream Links (BIF[2:0]#=0b001)

Single	Host, Two Upstr	Single Host, Two Upstream Sockets, Two Upstream Links	S)		1x8, 1x4, 1x2, 1x1 2x8, 2x4, 2x2, 2x1																		
		Supported Bifurcation Modes	Add-in-Card																				
Min Ca Width	Min Card Card Short Width Name		Encoding PRSNTBI3:01#	Host	Upstream Devices	Upstream Links	BIF[2:0]#	Resulting Link	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4 Lar	Lane 5 Lane 6	6 Lane 7	7 Lane 8	Lane 9	Lane 10	Lane 11	Lane 12	Lane 13 Lar	Lane 14 Lan	Lane 15
e/u	Not Present	Card Not Present	0b1111	1 Host		2 Links	00001					Н			Н						-		
ş		1 x8, 1 x4, 1 x2, 1 x1	051110	1 Host	2 Upstream Sockets	2 Links	00001	1×8	Link 0,		Link 0, Li	Link 0, Lir	Link 0, Lin	Link 0, Link 0,	0, Link 0,								
3	1 xs Option	1 1 2 1 1 2 1 2 1	0h1110	1 Host	2 Unstream Sorkets	2 Links		(Socket Uoniy)	-	Lanel	+	+	+	+	+								
3C	1 x4	1 67, 1 62, 1 61			C operation and a second	C C C C C C C C C C C C C C C C C C C	00001	(Socket 0 only)	_	-	-	Lane 3											
20	1×2	1 x2, 1 x1	051110	1 Host	2 Upstream Sockets	2 Links	00001	1 x2 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1													
30	1x1	1x1	051110	1 Host	2 Upstream Sockets	2 Links	00001	1x1 (Socket 0 only)	Link 0, Lane 0														
		1x8,1x4,1x2,1x1	001101	1 Host	2 Upstream Sockets	2 Links	00001	1×8	_								Host	Host	Host	Host	Host H	Host Host	st
20	1 x8 Option	1 x8 Option B 2 x4, 2 x2, 2 x1						(Socket 0 only)	Lane 0	+	+	+	+	+	+	П	d Disable	Disabled	Disabled	Disabled D	-	3	palo
40	2 x8 Option E	2 x8 Option B 4 x4, 4 x2, 4 x1	051101	1 Host	2 Upstream Sockets	2 Links	00001	2 x8	Link 0, Lane 0	Link 0, 1	Link 0, Li Lane 2 La	Link 0, Lir Lane 3 Lar	Link 0, Lin Lane 4 Lar	Link 0, Link 0, Lane 5 Lane 6	0, Link 0,), Link 1, 7 Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lir Lane 5 La	Link 1, Lin Lane 6 Lar	Link 1, Lane 7
		1 x8, 1 x4	0b1100	1 Host	2 Upstream Sockets	2 Links		1 x8	Link 0,	Link 0, 1	Link 0, Li	Link 0, Lir	Link 0, Lin	Link 0, Link 0,	0, Link 0,),							
ر	1 vg Ontion	2 x4,					00001	(Socket 0 only)	Lane 0	Lane 1	Lane 2 La	Lane 3 Lar	Lane 4 Lar	Lane 5 Lane 6	e Lane 7	7							
		1x16.1x8.1x4	001100	1 Host	2 Upstream Sockets	2 Links		2 x8	Link 0.	Link 0.	Link 0. Li	Link 0. Lir	Link 0. Lin	Link 0. Link 0.	0. Link 0.	Link 1.	Link 1.	Link 1.	Link 1.	Link 1.	Link 1. Lir	Link 1. Lin	Link 1.
		2 x8, 2 x4,					00001		Lane 0							_	_	Lane 2	Lane 3	Lane 4			Lane 7
4C	1 x16 Option	1x16 Option D 4 x4, 4 x2 (First 8 lanes), 4x1													_								
RSVD	RSVD	RSVD	0b1011	1 Host	2 Upstream Sockets	2 Links	00001																
		2 x4, 2 x2, 2 x1	001010	1 Host	2 Upstream Sockets	2 Links	0000	1 x4	Link 0,		_	Link 0,											
20	2 x4	1 x4, 1 x2, 1 x1					10000	(Socket 0 only)	Lane 0	-	Lane 2 La	Lane 3											
		4 x2 (First 8 lanes), 4 x1	0b1001	1 Host	2 Upstream Sockets	2 Links		1 x2	Link 0,	Link 0,					_	_							
3C	4 x2	2 x2, 2 x1 1 x2, 1 x1					00001	(Socket 0 only)	Lane 0	Lane 1													
RSVD	RSVD	RSVD for future x8 encoding	0b1000	1 Host	2 Upstream Sockets	2 Links	00001																
40	1 x16 Option A	1 x16, 1 x8, 1 x4, 1 x2, 1 x1	050111	1 Host	2 Upstream Sockets	2 Links	00001	1 x8 (Socket 0 only)	Link 0, Lane 0	Link 0, 1 Lane 1 L	Link 0, Li Lane 2 La	Link 0, Lir Lane 3 Lar	Link 0, Lin Lane 4 Lar	Link 0, Link 0, Lane 5 Lane 6	0, Link 0,	7							
4C	2 x8 Option A	2 x8, 2 x4, 2 x2, 2 x1 A	000110	1 Host	2 Upstream Sockets	2 Links	00001	2 x8	Link 0, Lane 0	Link 0, 1	Link 0, Li	Link 0, Lin Lane 3 Lar	Link 0, Lin Lane 4 Lar	Link 0, Link 0, Lane 5 Lane 6	0, Link 0,), Link 1,	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lin Lane 5 La	Link 1, Link 1, Lane 6 Lane 7	k 1, e 7
ç	0 000	1 x16, 1 x8, 1 x4, 1 x2, 1 x1	000101	1 Host	2 Upstream Sockets	2 Links	00001	2 x8	Link 0,	Link 0, 1	Link 0, Li	Link 0, Lin	Link 0, Lin		0, Link 0,), Link 1,	Link 1,	Link 1,	Link 1,	Link 1,	Link 1, Lir	Link 1, Link 1,	Link 1,
ř	in indicator	1 x16, 1 x8, 1 x4	000100	1 Host	2 Upstream Sockets	2 Links		2 x8	Link 0,		+	+	+	+	+		-	Link 1,	Link 1,	+	+	+	Link 1,
J.	1 v16 Ontion	2 x8, 2 x4, 2 x2, 2 x1 1 x15 Ontion C 4 x4 4 x7 4 x1					00001		Lane 0	Lane 1	Lane 2 La	Lane 3 Lar	Lane 4 Lar	Lane 5 Lane 6	e lane 7	7 Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5 La	Lane 6 Lar	Lane 7
L		4 x4 4 x2 4 x1	000011	1 Host	2 Unstream Sockets	2 Links		2 x4	Link 0.	Link 0	Link 0.	Link 0.				Link 2.	Link 2.	Link 2	Link 2				
4C	4 x4						00001	(EP 0 and 2 only)	Lane 0			Lane 3				Lane 0		Lane 2	Lane 3				
RSVD			000010	1 Host	2 Upstream Sockets	2 Links	00001																
RSVD	- 1	RSVD	000001	1 Host	2 Upstream Sockets	2 Links	00001																
RSVD	RSVD		000000	1 Host	2 Upstream Sockets	2 Links	00001																

Table 36: Bifurcation for Single Host, Quad Sockets and Quad Upstream Links (BIF[2:0]#=0b010)

Lane 10 Lane 11 Lane 12 Host Host Host Host Link 2 Link 3. Link 2 Link 3. Lane 2 Lane 3 Lane 0.
Link 2, Link 2, Link 3, Link 3, Lane 1 Lane 2 Lane 3 Lane 0 Lane 1
Link 2, Link 3, Lane 2 Lane 3 Lane 0
Link 2, Link 2, Link 3, Lane 2 Lane 3 Lane 0
Link 2. Link 3.
Lane 2
Link 2,
rane z
LIIIK 2,
13-10-0
רפווב ז רפווב ז
Link 2, Link 3,
Lane 2 Lane 3 Lane 0
Link 2, Link 2, Link 3,
Isabled Disabled Disabled Disabled Di
Host Host Host
rane 10 Lane 11 Lane 12
Jane 10 Jane 11

Table 37: Bifurcation for Single Host, Quad Sockets and Quad Upstream Links – First 8 PCIe Lanes (BIF[2:0]#=0b011)

Upstream Society 4 Upstream Links 00011		Resulting Link lane 0 lane 1 lane 2 lane 3 lane 4 lane 5 lane 6 lane 8 lane 9		24011	only) Lane 0	1x2 Link 0, Link 0, Goodest Only Inno 1 Inno 1	Link 0,	(Aluo	1x1 Link 0, Socket 0 only Lane 0	2 x 2 Link 0, Link 1, Link 1, Socket 0 & 2 only) Lane 0 Lane 1 Lane 0 Lane 1	2x2 Link 0, Link 1, Link 1, Link 1, Socket 0 & 2 only) Lane 0 Lane 1 Lane 0 Lane 1	Link 2,	Lane 0 Lane 1 Lane 0 Lane 1 Lane 0 Lane 1 Lane 0 Lane 1	Link 0, Link 1, Link 2, Link 2, Link 3,	Lane 0 Lane 1 Lane 0 Lane 1 Lane 0 Lane 1 Lane 1		2x2 Link 0, Link 0, Link 1, Link 1, Link 1, Sorter 0 8 2 only lane 0 lane 1 lane 1	Link 0,	Lane 0 Lane 1 Lane 0 Lane 1 Lane 0 Lane 1 Lane 0 Lane 1		1x2 Link 0, Link 0, Socket 0 only) Lane 0 Lane 1	2x2 Linko, Linko, Linko, Linki, Linki, Linki, Cockerto 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	Link 0, Link 0,	(Socketuoniy) Lane Lane 1	2 only) Lane 0 Lane 1 Lane 0	4x2 Link 0, Link 1, Link 1, Link 1, Link 1, Socket 0 & 2 only Lane 0 Lane 1 Lane 1		
Upstream Dovices Upstream tikks 4 Upstream Societis 4 Linis 4 Upstream Societis 5 Linis 4 Upstream Societis 5 Linis 4 Upstream Societis 6 Linis 6 Linis 6 Linis 6 Linis 6 Linis 7	HF[2:0]#				_		+	+					06011		00011	0b011			06011	0b011				(200				0h011
4 12, 441 Upstream Devices 4 Upstream Societs 5 Upstream Societs 6 Upstream Societs 6 Upstream Societs 7 Upstream Societs 6 Upstream Societs			4 links	Alinks	2	4 Links	4 Links		4 Links	4 Links	4 Links	4 Links		4 Links		4 Links	4 Links	4 Links		4 Links	4 Links	4 Links	4 Links	Alinke		4 Links	4 Links	41inks
Host	4 x2, 4x1		т	A Hostraam Sorkats	a characteristics	4 Upstream Sockets	4 Upstream Sockets		4 Upstream Sockets	4 Upstream Sockets	4 Upstream Sockets	4 Upstream Sockets		4 Upstream Sockets		4 Upstream Sockets	4 Upstream Sockets	4 Upstream Sockets		4 Upstream Sockets	4 Upstream Sockets	4 Upstream Sockets	4 Upstream Sockets	A Hostraam Corkets		4 Upstream Sockets	4 Upstream Sockets	4 Unstream Sockets
Singe Hoot, Four Upstream Societies, Four Upstream Intos - Fines Binnes Min Card Card Short		Host	1 Host	1 Hoer	i i	1 Host	1 Host		1 Host	1 Host	1 Host	1 Host		1 Host		1 Host	1 Host	1 Host		1 Host	1 Host	1 Host	1 Host	1 Hoet	7	1 Host	1 Host	1 Host

Table 38: Bifurcation for Dual Host, Dual Sockets and Dual Upstream Links (BIF[2:0]#=0b101)

Child	Additional Extending 1.585_246_2.824 Machine Mac	Auchinocompany Control Company Control Com	Models	Model-cord Fine Color Fin	Machicural Encoding Host Upstream Boxies 2.16,2 x4,3 x2,2 x4,	Processing	Machine Carroll Machine Ca	Additional Encoding Execution Execut	Continue
Marchanger Mar	Auchier Card State 2 March	Auchiecoung Procession Sectors Links L	Machical Card Lance Lanc	Head standy	Paster P	Procedure	Modelst-Card Properties P	Additional Executions 1.86 2.84, 2.0.234 Additional Executions Additi	Market
Prescription Pres	Auchier Card Extraction Law	Auchie-Card Control	Find the control of	Machine Continue	Machicural Encoding 186, 244, 242, 244 Machicural Encoding 186, 246, 244, 242, 244 Machicural Encoding 186, 246, 244, 242, 244 Machicural Encoding 2 dots 2	Processing Pro	Packer P	Add bin-Card Extractions	Courtier
Executing that Exec	Auchier Card Extraction Control of the Contro	Auchinology Processing Society China Links L	Machine Card Lance Card L	Model-Load Host Upstream Bookes Links	Machicard Fine	Packel-Card	Auchier-Land Executed Execu	Additional Encoding	Consider
Child	Auchier Card Exclusion Links L	Auchinocompany Control of Con	Models	Model-correction	Machicard	Processing	Auchier Card Sept. 20, 214	Additional Encoding Execution Execut	Continue
Procession Pro	Auchierany 2.184_2.24.4 Auchierany 2.184_2.24.4 Auchierany 2.184_2.24.4 Auchierany 2.184_2.24.4 Auchierany Auchierany 2.184_2.24.4 Auchierany Auchie	Auchiecous Excelling State Long State	Machical	Find the color	Paster P	Procedure	Mode in-Land Participation	Additional Executions 1.88 2.84, 2.02, 244 2.02,	Mode beams Control C
Executing bigs Executing lists Executing l	Auchier Card Exception Links L	Auchinocompany Control of Con	Medita Card Encoding Fig. 2014 Deciding Encoding Encod	Model-Conference	Machicard	Processing	Auchier Card Sept. 202, 2xd Sept. 2xd, 2xd, 2xd, 2xd, 2xd, 2xd, 2xd, 2xd,	Additional Encoding Execution Execut	
Child	Authority Continue	Auchino Continue 2 + 16, 2 + 1, 2 + 1, 2 + 1 Auchino Continue 2 + 16, 2 + 1, 2 + 1, 2 + 1, 2 + 1, 3 + 3 + 3 + 3 + 3 + 3 + 3 + 3 + 3 + 3	Problem Card Property Problem Card Problem	Model-Conference	Machicard	Processing	Auchier Card Experiment Society 2.04,2.02,241 Expensive Society 2.1045 Expensive Society Expensive Society 2.1045	Additional Executions Control Cont	Excelling 1
Proceding	Auchier Card Excelling 1985 244, 24, 244 Excelling Link Excelling Link Lin	Auchiecoung Proceedings Procession Scotters Links Li	Mode-Card Page Lance L	Host Upstream Society 2 Links Chind	Passiving	Procession Pro	Modelstand Presentation Presen	Additional Encoding 1.88 2.84 2.0.234 Additional Encoding	Accession
Encoding	Additional Extending 2.88, 2.84, 2.44 Machine Line	Auchin-County County Cou	Machine Card Host Upstream Society Links Upstream Society Upstream Society Links Upstream Society Links Upstream Society Upstream Society Links Upstream Society Upstream Society Links Upstream Society Links Upstream Society Upstream Society Links Up	Model-Load Host Upstream Bookes Upstream Sockes Links	Machicard	Principal	Auchier Card State	Additional Encoding Execution Execut	Accessing Conference Conf
Proceding Proc	Auchier Card Extraction Law	Accidence 2.08, 2.44, 24, 24, 244 Accidence 2.08, 2.44, 24, 24, 24, 24, 24, 24, 24, 24, 24,	Proceedings Procession Pr	Machinorary Finoding Finodi	Machicural Encoding 186, 244, 247, 244 Machicural Encoding 186, 246, 247, 247, 244 Machicural Encoding 2 Host 2 Lighteen Societes 2 Links 00-101 186, 246, 246, 246, 246, 246, 246, 246, 24	Processing Pro	Add the Card According	Additional Extensional Presentations 1.8.8 2.84, 2.6.2.34 Additional Extensional Ex	Proceedings
Proceding	Auchier Card Extraction Auchier Card Extraction	Auchiectura Control	Procession	Machinorary Finosity Prost Upstream Bookes 2 Links Dobot Dobot Prost Dobot	Particular Protection Particular Par	Procedure	Add the Card Add	Additional Extensional Exten	Accepted Conference Confe
Procession	Additional Colored Additio	Auchie-County County Cou	Machical	Head stand Head H	Packed Control Pack	Packer P	Mode in-Land Particulary	Additional Encoding 1.88 2.84 2.8.2.24 2.8.2.24 2.8.2.24 2.8.2.24	
Executive Heat Lord	Additional Electroding 2.58,2.94,2.24 Electroding	Auchie-Card Continue Contin	Proceedings Procession	Machine Continue	Machicural Encoding 1.06 2 Mark 2.0, 2.14 Machicural Encoding 1.06 2 Machicural Encoding 1.06	Processing Pro	Proceding	Auchiecture Conference Co	Control Cont
Procession Pro	Auchier Card Exclusion Line L	Auchiectual	Machine	Host Upstream Society 2 Links Choice C	Passiving	Procedure	Principal	Additional Executions 1.88 2.84, 2.0.234 Additional Executions	
Experience Continue Continu	Additional Extensional Exten	Auchin-Counting 2 + 65 + 2 + 5 + 2 + 2 + 3 + 3 + 3 + 3 + 3 + 3 + 3 + 3	Machine Card Excellent Card Excell	Model-Load Host Upstream Devices Upstream Society 2 Upstream S	Machicard Fine Upstream Society 2 Links China Chin	Add the Carrela	Add included protections 2.64,2.20,2.24 2.04,3.20,2.44 BEFD019 (Most beauting link protection) Lanc 0 Lanc 1 Lanc 2 Lanc 3 Lanc 4 Lanc 3 Lanc 4 Lanc 5 Lanc 5 Lanc 3 Lanc 4 Lanc 5 Lanc 5 Lanc 3 Lanc 4 Lanc 5	Additional Encoding Execution Execut	Conference Con
Proceding Proc	Auchiecand Control C	Auchie-Card Continue Contin	Proceedings	Machicard Hort Upstream Devices Links British Breathing Link Lane	Marketana	Processing Pro	Proofing Proof P	Add bin-Card Exclosing Fiscoling F	Proceedings
Protocology	Auchier Card Extraction Law	Auchiecoung Control	Machine Mach	Host Upstream Society 2 Links Upstrea	Passiving	Procedure	Note the control of	Additional Executions 1.8.8.2.84.2.0.2.34 Additional Executions Addit	Accepted Continued Conti
Executing that Exec	Additional Encoding 1.585.246.241 Encoding Enco	Auchin-Counting 2 × 8, 2 × 4, 2 × 2, 2 × 4 Auchin-Counting Line	Models	Model-Card Host Upstream Devices Upstream Society 2 Upstream S	Machicard	Add the Card Execution E	Add included Principles Add included Expending Link Executing Link Lane 0 Lane 1 Lane 2 Lane 3 Lane 4 Lane 5 Lane 6 Lane 7 Lane 7 Lane 7 Lane 6 Lane 7 <td> Auchin-Card Excellent Ex</td> <td> Excelling Line Lane La</td>	Auchin-Card Excellent Ex	Excelling Line Lane La
Proceding Part Long Lo	Auchier Card Execution Line Lane L	Auchie-Card Continue Contin	Encoding	Machinorary Finoding Hort Upstream Devices Links Upstream Society Links	Machicural Encoding 186, 244, 247, 244 Machicural Encoding	Proceedings Procedings Proceedings Proceedings Procedings Pr	Principal Foot 1962-1962	Add bin-Card Excepting Links Excepting Link Lane	Problem
Protecting Continue	Auchier Card Extraction Law 2 Law 3 Law 6	Auchiectura Conferent Scotes	According Acco	House Choice House Choice House Choice House Choice Choic	Machicura	2 kg. 2 kg	Add in-Land Extraction Fraction Fraction Extraction Extrac	Additional Executions Addi	Accepted Conference Confe
PASSATT PASS	Auchinicated Lane	2 kg 2 k	Encoding	Machinorary Facoring Hort Upstream Devices Luiks Upstream Society Luiks	Machicural Encoding 1.06 2 Mg/Land	2.62, 2.64, 2.62, 2.64 Host Upstream Devices Upstream Devices Upstream Devices Upstream Devices Upstream Devices Upstream Devices Upstream Scote Upstream Sc	According	2.66_2.94_2.02_2.84 2.02_2.94_2.02_4 2.04_2.04_4 2	Control Cont
PASSECTION PROPERTY PROPERT	Additional Experiments Additional Experime	Auchie-Card Confession Co	Proceeding	Hotelean	Packed Contained 1968 2 No. 2 A.J. Packed Contained Packed Con	Procedure Proc	Presentable	Add bin-Card Excepting Link Lin	
	Additional Add	Auchiecoung Proceedings Procedings P	Additional Conference	Model-Corting	Machicura	Packel Encoding 2.62,216,120,214 Packel Encoding Packel E	Auchier-Land State Lane	Additional Encoding 1.88 2.84, 2.0.2.34 Additional Encoding	Accepted Continue
PASSATT PASS	Additional Extensional Presentations 1.88 1.8	Auchie-Card Control	2 Mail Land 1985	Model-Card Host Upstream Devices Lane	Machicard	Add the Card Extraction E	Additional Encoding Additional Encoding Resulting Link Lane 0 Lane 1 Lane 2 Lane 3 Lane 3 Lane 3 Lane 5 Lane 6 Lane 7 Lane 7 Lane 3 Lane 3 Lane 3 Lane 3 Lane 5 Lane 6 Lane 7 Lane 7 Lane 5 Lane 6 Lane 7 Lane 7 Lane 7 Lane 7 Lane 3 Lane 3 Lane 6 Lane 7 <	2.66_2.84_2.20_2.84 2.02_2.84_2.20_2.84 ENTERONING ENTERONIN	2.65.2 M, 2.02.241 2.65.2 M,
PASSATE PASS	Additional File Conference Lance	Accepted	Proceeding	Machinorary Finosofies Fi	Machicural Encoding 10,8,2 kd, 2	Processing Pro	Packer P	2.68,2 M, 2.02,2 M 2.06,2 M, 2.02,2 M, 2.	1
Consideration Most Upstream Devices Upstream Links Upstream Devices Upstream Sockets Upstream Sockets Units	Additional Experiment Addi	Auchiecoung 2.06, 2.44, 24, 244	According Acco	Machinocard	Machicural Encoding 186, 244, 242, 244 Matthematical Encoding Machicural Encodin	2.62.2 M. J. 2.2.2 L. 1 SH [J. 2.2 L. 1 SH [Auchier-Land Execution Franciscope Execution	Additional Encoding 2.88,2.84,2.0.234 Additional Encoding	Accepted Conference Confe
Additional Experimental Continuation	Additional Encoding 1.08,2.94,2.42,2.41 Additional Encoding 1.08,2.94,2.42,2.41 Additional Encoding 1.08,2.94,2.42,2.41 Additional Encoding 1.08,2.41 Addition	Auchin-Count County Coun	Authorized Checking Authorized Checking Check	Model-card Host Upstream Devices Upstream Devices Upstream Society Upstream Soc	Model-Condition 1.06.2 Mg, 2.0.2 Mg Mg/Rolf Resulting Link Lane 0 Lane 1 Lane 2 Lane 3 Lane 4 Lane 5 Lane 5 Lane 6 Lane 7	Add th. Card Add	Add include Additional Expending Link And include And incl	Auchin-Card Excellent Exellent Exell	Continue
Additional Host Upgreen Devices Upgreen House Upgreen Ho	Additional Encoding 1.88, 2.84, 2.42, 2.44 Encoding Enco	Accidence Construction Constru	Problem	Machinorary Face of the part Lane La	Machicural Encoding 186, 244, 247, 244 Machicural Encoding	Proceedings Process	Packed Control Pack	Auchie-Gard Constitution Const	
Conception Host Upstream Devices Upstream Links DeliZOJP Resulting Link Link O	Additional Encoding 2.58,2.94,2.42,241 Electroding	Auchie Card Lane		Machinocard	Machicura	2.62.2 M. J. 2.2.2 Z. 1 Part Configuration Pa	Add in-Land Extraction Fraction Frac	Additional Encoding 1.88 2.84, 2.6.2.34 Additional Encoding Percoding	Auchinomy Conference Conf
Additional Experimental Continuity Additional Cont	Additional Line L	Auchin-Count Conference C	Additional Control C		Mode-Condition 1.06, 2.44, 2.42, 2.44 Most	Add th. Card Add	Add include Add include Executing Link Lane of Lane	Auchin-Card Excellent Control of Contr	
Additional Host Uppercent Devices Uppercent Lines Host Uppercent Devices Upper	Additional Encoding 1.08,2.94,2.2.2.34	Additional Content Content	Proceeding	Machine Control Machine Machine Control Machine	Machicural Encoding 1.06 2 Machicural Enc	Packed Continue 18,8, 18,12,241 Packed Continue Packed Con	Auchinicated Encoding February Encoding Encod	Auchie-Gard Excellent Continue Conti	
Additional Host Upstream Devices Upstream links BHF20jp Resulting Link Lane	Additional Line L	Proceding Proceeding Proceding Pro		Model-Corting	Machicular 1,00,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,	Procedure	Proofing	Add sin Card Exception	
Additional Expositions Additional Expositional Expositions Additional Expositions Additi	Additional Exceptions 2.58,2.94,2.42,2.41 Additional Exceptions Additional Exceptions Additional Exceptions Additional Exceptions Additional Exceptions Additional Exceptions Additional Exception Additional Exceptional Exception Additional Exception Additional Exception Additional Exception Additional Exceptional Exceptional Exceptional Exceptional Exception Additional Exceptional Exception Exceptional Exception E	Auchinocompany Conference	Additional Content	Model-Conference 1.06.2 kg. 2.0.2 kg. 4 Model-Conference Model	Model-Coard	Add the Cart	Add include Add include Add include BIF DOTE BIF DOTE <td> Additional Encoding Execution Execut</td> <td> Accepted Conference Confe</td>	Additional Encoding Execution Execut	Accepted Conference Confe
Additional Host Uppercent Devices Uppercent Lines Uppercent	Additional Encoding 1.08,1.24,1.24,1.24	Additional Content Content	2 AS 2 A	Model-Card Host Upstream Devices Lane	Makehocard	Add in-Card Executing Line Lane La	Auchinicated Encoding Francisco Fr	Auchie-Gard Check	Automotive Check
Experimental Procession Procession Control Proc	Additional Encoding Lance	2 Light State	2 - 62 2 - 62	Additional Encoding Host Upstream Society Links Berpolity Links Li	Additional Encoding 186, 244, 247, 241 186, 244, 247, 244 186, 244, 247, 244 186, 244, 247, 244 186, 244, 247, 244 186, 244, 247, 244 186, 244, 247, 244 186, 244, 247, 244 186, 244, 247, 244 186, 244, 247, 244 186, 244, 247, 244 186, 244, 247, 244 186, 244, 247, 244 186, 244, 247, 244 186, 244, 247, 244, 247, 244 186, 244, 247, 247	2.62, 2.42, 2.22, 2.43 Birk Ball Bir	2.62 2.64, 2.02, 2.04 Post	Considerate	2.62 2.64, 2.02, 2.41 Encoding Fine Collision Fine Collis
Expectation Procession Pr	Auchier Card Auch	Auchie Card Config	2 Log 3 Log 2 Log 3 Lo	Additional Flooring	Auchicutum 2.08.2 xt, 2.02.2xt Hoot Upstream Links HFR-0 # Resulting Link Link 0, Link 0	2.62.24,2.2.24	Add in-Land	Additional Encoding 1.88 2.84, 2.0.2.34 Mode	2 \(\text{Add-in-card} \)
Exclusion Fig. 2 Log team Devices Upstream Devices Upstream Devices Upstream Devices Upstream Devices Upstream Sockets 2 Links L	Auchiecture 2.08,2.94,242,541 Auchiecture 2.08,2.94,2.94,241 Auchiecture 2.08,2.94,2.94,241 Auchiecture 2.08,2.94,2.94,241 Auchiecture 2.08,2.94,2.94,241 Auchiecture 2.08,2.94,2.94,241 Auchiecture 2.08,2.94,2.94,241 Auchiecture 2.08,2.94,2.94,2.94,241 Auchiecture 2.09,2.94,2.94,241 Auchiecture 2.09,2.94,2.94,2.94,2.94,2.94,2.94,2.94,2.9	Auchie-Card Conference Co	2 Mg Local	Abbit Action Abbi	Model-Cond Care C	Add the Card Add	Auchier Card Experimental Card Experimen	Auchin-Card Excellent Config Free Config	Conference Con
Model Mode	Additional Encoding Lance	2 Light State	2 AS 2 A	Additional Encoding Host Upstream Society Links Berping Host Upstream Society Links Link	Additional Encoding 1.06 2 Mg 2-7, 2.41 Mg 2 Mg 1 Mg 1 Mg 2 Mg 2 Mg 2 Mg 2 Mg 2	2.62, 2.42, 2.22, 2.43 Berging Link Beschring Link Beschring Link Berging Link Beschring Link	Additionary Constraints	Auchin-Card Constitution Const	2.65.2 kg, 2.62,
Experimental Foot Light Example Market Long	Authorised Aut	2 Lig. 3 Lig. 2 Lig. 2 Lig. 3 Lig. 2 Lig. 2 Lig. 2 Lig. 3 Lig. 3 Lig. 2 Lig. 3 Lig.	2.06.2 hot 2.0 2.06.2 hot 2.0 2.06.2 hot 3.0 2.06	2.06.2.2.0.2.2.0.1 Abditional Encoding Face of the Control o	Abbit Care 2.08.2 kJ, 2.0.2 24 Mode Leave 2.08.2 kJ, 2.08.2 kJ, 2.0.2 24 Mode Leave 2.08.2 kJ, 2	2.62.2 M. 2.22.21 Septemble Septemb	Add the Card Add	Excepting First 2 x4, 2 x2, 2x4 Most Uppressm Societies Properties Propert Properties Properties Properties Properties Propertie	2 Log 2 Lo
Footing Footing Constitution	Auchier Card Auch	Auchie Count Conference C	2 Log 3 Log 2 Log 3 Lo	Additional Encoding 2.46,2 x2,2 x4 Mostream Devices Berticol Bertic	Additional Encoding 1.06.2 M; 2.0.2 241 Most Upstream Devices Upstream Devices Upstream Scotes 2 Links Obj. 1.0	2.66,2 to 2.02,2 to 2.02 2.66,2 to 2.02 2.64	Add in-Card	Additional Encoring Excellent Section Ex	Additional Encoding
Modifice Conference	Auchiencing Lancing	Audito-Card Conference Co	Additional Encoding	Abbit Action Abbi	Properties Pro	Additional Encoding Properties Line	Auchience Continue	Additional Engage Color	Conclusion Con
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Experiment Fine Light Experiment Light Expe	Additional Add	2 kg 2 k	2 kg 2 k	Additional Encoding Proceeding Line Li	Abbit Control 1962	2.62.2 M. 2.22.21 Sept. 2.22.22 Sept. 2.22 S	Add the Card Add	Character Char	2 to 2, 2 to
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Table 39: Bifurcation for Quad Host, Quad Sockets and Quad Upstream Links (BIF[2:0]#=0b110)

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		Lane 14									Host	-11	Link 3,	7 ALIPT			1040	S L	Lane 2											Link 3,	Lane 2	Link 3,	Lane 2		
		Lane 13									Host	Disabled	Link 3,	Talle			link a	, L	Lane 1											Link 3,	Lane 1	Link 3,	Lane 1		
		Lane 12									Host	Disabled	Link 3,	rallen			Links	5	Lane 0	Ī										Link 3,	Lane 0	Link 3,	Lane 0		
		Lane 11									Host	Disabled	Link 2,	called			Link 2	, ,	Lane 3								Link 2,	Lane 3	Link 2,	Link 2,	Lane 3	Link 2,	Lane 3		
		Lane 10									Host	Disabled Disabled Disabled Disabled Disabled	Link 2,	7 AUPT			Link	, and a	Lane 2								Link 2,	Lane 2	Link 2,	Link 2,	Lane 2	Link 2,	Lane 2		
		Lane 9									Host	Disabled	Link 2,	TalleT	_		Link 2	, Luc 2,	Lane 1								Link 2,	Lane 1	Link 2,	Link 2,	Lane 1	Link 2,	Lane 1		
		Lane 8									Host	Disabled	Link 2,	רפנובים			1 into	, L	Lane 0								Link 2,	Lane 0	Link 2,	Link 2,	Lane 0	Link 2,	Lane 0		
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		Lane 4	Ī								Link 1,	Lane 0	Link 1,	ratie	Link 1,	Lane 0	Link 1	,	Lane 0		Link 1,	Lane 0	Link 1,	Lane 0						Link 1,	Lane 0	Link 1,	Lane 0		
		Lane 3		Link 0,	Lane 3	Link 0,	Lane 3				Link 0,	Lane 3	Link 0,	ralle o	Link 0,	Lane 3	Odeil	3	Lane 3		Link 0,	Lane 3				Link 0,	Link 0,	Lane 3	Link 0,	Link 0,	Lane 3	Link 0,	Lane 3		Ī
		Lane 2		Link 0,	Lane 2	Link 0,	Lane 2				Link 0,	Lane 2	Link 0,	7 aue 7	Link 0,	Lane 2	Over	3	Lane 2		Link 0,	Lane 2				Link 0,	Link 0,	Lane 2	Link 0,	Link 0,	Lane 2	Link 0,	Lane 2		
		Lane 1		Link 0,	Lane 1	Link 0,	Lane 1	Link 0,			Link 0,	Lane 1	Link 0,	Talle	Link 0,	Lane 1	linko	3	Lane 1		Link 0,	Lane 1	Link 0,	Lane 1		Link 0,	Link 0,	Lane 1	Link 0,	Link 0,	Lane 1	Link 0,	Lane 1		
		Lane 0		Link 0,	Lane 0	Link 0,	Lane 0	Link 0,	Link 0,	Lane 0	Link 0,	Lane 0	Link 0,	naue :	Link 0,	Lane 0	Odeil	, c	Lane 0		Link 0,	Lane 0	Link 0,	Lane 0		Link 0,	Link 0,	Lane 0	Link 0,	Link 0,	Lane 0	Link 0,	Lane 0		
		Resulting Link		1 x4	(Host 0 only)	1 x4	(Host 0 only)	1 x2	1x1	(Host 0 only)	2 x4		4 ×4		2 x4		A v.A				2 x4		2 x 2			1 x4 (Host 0 only)	2 x4	(Host 0 & 2 only)	2 x4 (Host 0 & 2 only)	4 x4		4 x4			
	BIF[2:0]#		0b110	010-10	001100	01110	0.1100	0b110		00110	0b110		0b110	İ	_	00110	İ	01-440	06110	0h110	000	OTTON		0b110	00110	00110	0h110	0.1100	00110	İ	06110	011440	OTTON	00110	0h110
		Upstream Links	4 Links	4 Links		4 Links		4 Links	4 Links		4 Links		4 Links		4 Links		Alinke	2		4 Links	4 Links		4 Links		4 Links	4 Links	4 Links		4 Links	4 Links		4 Links		4 Links	4 links
4 x4, 4 x2, 4 x1		Upstream Devices	4 Upstream Sockets	4 Upstream Sockets		4 Upstream Sockets		4 Upstream Sockets	4 Upstream Sockets		4 Upstream Sockets		4 Upstream Sockets		4 Upstream Sockets		A Hostraam Cockate	+ observant socurers		4 Unstream Sockets	4 Upstream Sockets		4 Upstream Sockets		4 Upstream Sockets	4 Upstream Sockets	4 Upstream Sockets		4 Upstream Sockets	4 Upstream Sockets		4 Upstream Sockets		4 Upstream Sockets	4 Unstream Sockets
		Host	4 Host	4 Host		4 Host		4 Host	4 Host		4 Host		4 Host		4 Host		A Host	i i		4 Host	4 Host		4 Host		4 Host	4 Host	4 Host		4 Host	4 Host		4 Host		4 Host	4 Host
	Add-in-Card Encoding	PRSNTB[3:0]#	0b1111	0b1110		0b1110		0b1110	0b1110		0b1101		0b1101		001100		061100	201100		Ob1011	0b1010		0b1001		0b1000	060111	000110		000101	000100		060011		000010	Ob0001
Quad Host, Four Upstream Sockets, Four Upstream Links	Supported Bifurcation Modes		Card Not Present	1 x8, 1 x4, 1 x2, 1 x1		1 x4, 1 x2, 1 x1		1x2, 1x1	1x1		1x1	1 x8 Option B 2 x4, 2 x2, 2 x1	2 x8, 2 x4, 2 x2, 2 x1		1 x4	2 x4,	4 X2 (FIRST 8 IBNES), 4 X1	2 -0 2 -0	1 x16 Option D 4 x4, 4 x2 (First 8 lanes): 4 x1		x2, 2 x1	1 x4, 1 x2, 1 x1	t 8 lanes), 4 x1	2 x2, 2 x1 1 x2, 1 x1	future x8 encoding	1 x16, 1 x8, 1 x4, 1 x2, 1 x1	2 x8, 2 x4, 2 x2, 2 x1		1 x16 Ontion B 2 x8 2 x4 2 x2 2 x1	1 x16, 1 x8, 1 x4	2 x8, 2 x4, 2 x2, 2 x1 1 x16 Option C 4 x4, 4 x2, 4 x1	4 x4, 4 x2, 4 x1			RSVD
ost, Four Upstre	Min Card Card Short	Name	Not Present		1 x8 Option A		1 x4	5	-	1x1		1 x8 Option B	9	z xo option b		9	1 xs option D		1 x16 Option D	BSVD		2 x4		4 x2	RSVD	1 x16 Ontion A		2 x8 Option A	1 v16 Ontlon B		1 x16 Option C		4 x 4	RSVD	RSVD
H De	fin Can	Width	n/a		3C		2C	۲	,	2C		2C	ş	١		,	7		Ų	RSVD		20		3C	RSVD	Š.		4C	4C		4C		46	RSVD	RSVD

Table 40: Bifurcation for Quad Host, Quad Sockets and Quad Upstream Links – First 8 lanes (BIF[2:0]#=0b111)

ad Host, F.	our Upstrea.	Quad Host, Four Upstream Sockets, Four Upstream links, First 8 PCIe Ianes	ks, First 8 PCIe lan	ş	4 x2, 4 x1																	
Min Card Card Short		Supported Bifurcation Modes	Add-in-Card Encoding				BIF[2:0]#															
Width Name			PRSNTB[3:0]#	Host	Upstream Devices	Upstream Links		Resulting Link	Lane 0	Lane 1	Lane 2	Lane 3 La	Lane 4 Lar	Lane 5 Lan	Lane 6 Lane 7	7 Lane 8	8 Lane 9	Lane 10	Lane 11	Lane 12 Lane 13	_	Lane 14 Lane 15
n/a Not	Not Present	Card Not Present	0b1111	4 Host	4 Upstream Sockets	4 x2 Links	0b111													Ī		
1 x6	1 x8 Option A	1 x8, 1 x4, 1 x2, 1 x1	051110	4 Host	4 Upstream Sockets	4 x2 Links	001111	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1												
	1 x4	1 x4, 1 x2, 1 x1	061110	4 Host	4 Upstream Sockets	4 x2 Links	0b111	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1												
	1×2	1x2, 1x1	061110	4 Host	4 Upstream Sockets	4 x2 Links	0b111	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1												
	1x1	1×1	061110	4 Host	4 Upstream Sockets	4 x2 Links	0b111	1x1 (Host 0 only)	Link 0, Lane 0													
1×6	8 Option B	1 x8 Option B 2 x4, 2 x2, 2 x1	001101	4 Host	4 Upstream Sockets	4 x2 Links	0b111	2 x2 (Host 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1 Di	Host Host Disabled Disabled		Link 2, Lin Lane 0 Lan	Link 2, Host Lane 1 Disable	Host Host Host Host Host Host Host Host	t Host led Disable	: Host ed Disable	Host ed Disabled	Host Disabled	Host Disabled	Host I	Host Host isable
2 x6	8 Option B	2 x8, 2 x4, 2 x2, 2 x1 2 x8 Option B 4 x4, 4 x2, 4 x1	0b1101	4 Host	4 Upstream Sockets	4 x2 Links	0b111	2 x2 (Host 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1 Di	Host I	Host Lir Disabled Lar	Link 2, Lin Lane 0 Lan	Link 2, Host Lane 1 Disabled	st Host bled Disable	t Host led Disabled	: Host ed Disable	Host Host Host Host Host Host Host Host	Host Disabled	Host Disabled	Host Fisabled Dis	Host Host isable
		1x8, 1x4 2x4	0b1100	4 Host	4 Upstream Sockets	4 x2 Links	0b111	4 x2	Link 0,	Link 0,	Link 1, Li	Link 1, Lir	Link 2, Lin	Link 2, Link 3,		3,						
1 x2	8 Option D	1 x8 Option D 4 x2 (First 8 lanes), 4 x1								-	_		_	_		•						
		1x16, 1x8, 1x4 2x8, 2x4,	0b1100	4 Host	4 Upstream Sockets	4 x2 Links	0b111	4 x2	Link 0, Lane 0	Link 0, Lane 1	Link 1, U	Link 1, Lir Lane 1 Lar	Link 2, Lin Lane 0 Lan	Link 2, Link 3, Lane 1 Lane 0	k3, Link3, e0 Lane1	3,3						
4C 1x16	16 Option D	1 x16 Option D 4 x4, 4 x2 (First 8 lanes), 4 x1	051011	t House	A Hortroam Cockets	A v3 Links	0H111														+	
ш.		2 × 2 × 2 × 3	001010	4 Host	4 Upstream Sockets	4 v2 Links	11100	2.8.2	Linko	Linko	link1	Link 1								İ		
	2 x4	1 x4, 1 x2, 1 x1			Constant of the constant of th	1 A.C. CIII II.3	0b111	(Host 0 & 1 only)	Lane 0		\rightarrow	Lane 1										
		4 x2 (First 8 lanes), 4 x1	0b1001	4 Host	4 Upstream Sockets	4 x2 Links	05111	4 x2	Link 0,	Link 0,	Link 1, Li	Link 1, Lir	Link 2, Lin	Link 2, Link 3,	k3, Link3,	6) -					_	
	4 x2	1 x2, 1 x1					11100		Called		_					•						
RSVD RSVD		RSVD for future x8 encoding	001000	4 Host	4 Upstream Sockets	4 x2 Links	0b111													Ī		
1 x1	1 x16 Option A	1x16, 1x8, 1x4, 1x2, 1x1	060111	4 Host	4 Upstream Sockets	4 x2 Links	0b111	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1												
		2 x8, 2 x4, 2 x2, 2 x1	000110	4 Host	4 Upstream Sockets	4 x2 Links	0b111	1x2	Link 0,	Link 0,												
7 ×	z xe Uption A	1x16 1x8 1x4 1x7 1x1	010101	4 Host	4 Unstream Sorkets	4 x2 Links		(HOST U ONIY)	Lane	Lane 1										Ī		
1 x 1	16 Option B	1 x16 Option B 2 x8, 2 x4, 2 x2, 2 x1					0b111	(Host 0 only)	Lane 0	Lane 1												
		1 x16, 1 x8, 1 x4 2 x8, 2 x4, 2 x2, 2 x1	000100	4 Host	4 Upstream Sockets	4 x2 Links	0b111	2 x2 (Host 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1		Lir	Link 2, Lin Lane 0 Lan	Link 2, Lane 1								
1xi	16 Option C	1 x16 Option C 4 x4, 4 x2, 4 x1											-									
	4 x4	4 x4, 4 x2, 4 x1	000011	4 Host	4 Upstream Sockets	4 x2 Links	0b111	2 x2 (Host 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1		رة ت	Link 2, Lin Lane 0 Lan	Link 2, Lane 1								
		RSVD	000010	4 Host	4 Upstream Sockets	4 x2 Links	0b111															
RSVD RSVD		RSVD	000001	4 Host	4 Upstream Sockets	4 x2 Links	0b111															
UNS ON		DOLLO	00000																			

3.9 Power Capacity and Power Delivery

There are four permissible power states: NIC Power Off, ID Mode, Aux Power Mode (S5), and Main Power Mode (S0). The transition of these states is shown in Figure 90. The max available power envelopes for each of these states are defined in Table 41.

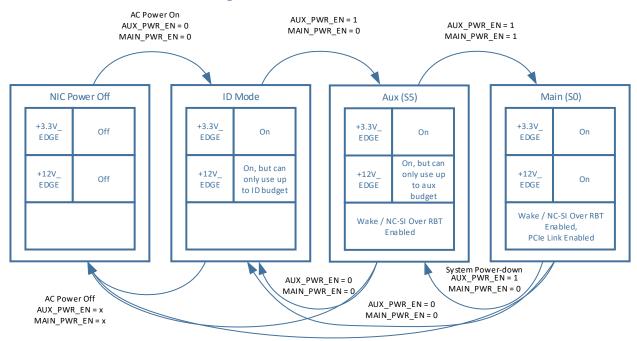


Figure 90: Baseboard Power States

Table 41: Power States

Power State	PWR_EN	PERSTn	FRU	Scan	WAKEn	RBT	PCle	+3.3V	+12V
				Chain		Link	Link	_EDGE	_EDGE
NIC Power Off	Invalid /	Invalid /							
	Don't Care	Don't Care							
ID Mode	Low	Low	Χ	Х				Χ	Χ
Aux Power	High	Low	Х	Х	Х	Χ		Х	Х
Mode (S5)									
Main Power	High	High	Х	Х	Х	Χ	Х	Х	Х
Mode (S0)									

3.9.1 NIC Power Off

In NIC power off mode, all power delivery has been turned off or disconnected from the baseboard. Transition to this state can be from any other state.

3.9.2 ID Mode

In the ID Mode, only +3.3V_EDGE is available for powering up management only functions. FRU and scan chain accesses are only allowed in this mode. The +12V_EDGE rail is not intended to be used in ID Mode, however leakage current may be present. The max leakage is defined in Section 3.10. An OCP NIC 3.0 card shall transition to this mode when AUX PWR EN=0 and MAIN PWR EN=0.

3.9.3 Aux Power Mode (S5)

In Aux Power Mode provides both +3.3V_EDGE as well as +12V_EDGE is available. +12V_EDGE in Aux mode may be used to deliver power to the OCP NIC 3.0 card, but only up to the Aux mode budget as defined in Table 42. An OCP NIC 3.0 card shall transition to this mode when AUX_PWR_EN=1 and MAIN_PWR_EN=0.

3.9.4 Main Power Mode (S0)

In Main Power Mode provides both +3.3V_EDGE and +12V_EDGE across the OCP connector. The OCP NIC 3.0 card operates in full capacity. Up to 80W may be delivered on +12V_EDGE for a Small Card and up to 150W for a Large Card. Additionally, up to 3.63W is delivered on each +3.3V_EDGE pin. An OCP NIC 3.0 card shall transition to this mode when AUX_PWR_EN=1 and MAIN_PWR_EN=1.

3.10 Power Supply Rail Requirements and Slot Power Envelopes

The baseboard provides +3.3V_EDGE and +12V_EDGE to both the Primary and Secondary Connectors. The rail requirements are leveraged from the PCle CEM 4.0 specification. For OCP NIC 3.0 cards, the requirements are as follows:

Power Rail	15W Slot	25W Slot	35W Slot	80W Slot	150W
	Small Card	Small Card	Small Card	Small Card	Large Card
	Hot Aisle	Hot Aisle	Hot Aisle	Cold Aisle	Cold Aisle
+3.3V_EDGE					
Voltage Tolerance	±9% (max)	±9% (max)	±9% (max)	±9% (max)	±9% (max)
Supply Current					
ID Mode	375mA (max)	375mA (max)	375mA (max)	375mA (max)	375mA (max)
Aux Mode	1.1A (max)	1.1A (max)	1.1A (max)	1.1A (max)	2.2A (max)
Main Mode	1.1A (max)	1.1A (max)	1.1A (max)	1.1A (max)	2.2A (max)
Capacitive Load	150μF (max)	150μF (max)	150μF (max)	150μF (max)	300μF (max)
+12V_EDGE					
Voltage Tolerance	±8% (max)	±8% (max)	±8% (max)	±8% (max)	±8% (max)
Supply Current					
ID Mode	100mA (max)	100mA (max)	100mA (max)	100mA (max)	100mA (max)
Aux Mode	0.7A (max)	1.1A (max)	1.5A (max)	3.3A (max)	6.3A (max)
Main Mode	1.25A (max)	2.1A (max)	2.9A (max)	6.6A (max)	12.5A (max)
Capacitive Load	500μF (max)	500μF (max)	1000μF (max)	1000μF (max)	2000μF (max)

Table 42: Baseboard Power Supply Rail Requirements – Slot Power Envelopes

Note: While cards may draw up to the published power ratings, the baseboard vendor shall evaluate its cooling capacity for each slot power envelope.

The OCP NIC 3.0 FRU definition provides a record for the max power consumption of the card. This value shall be used to aid in determining if the card may be enabled in a given OCP slot. Refer to Section 4.10.2 for the available FRU records.

Additionally, the baseboard shall advertise its slot power limits to aid in the overall board power budget allocation to prevent a high power card from being enabled in a lower power class slot. This is implemented via the Slot Power Limit Control mechanism as defined in the PCIe Base Specification. The end point silicon will power up in a low power state until power is negotiated.

3.11 Hot Swap Considerations for +12V EDGE and +3.3V EDGE Rails

For baseboards that support system hot (powered on) OCP NIC 3.0 card insertions and extractions, the system implementer shall consider the use of hotswap controllers on both the +12V_EDGE and

+3.3V_EDGE pins to prevent damage to the baseboard or the OCP NIC 3.0 card. Hotswap controllers help with in-rush current limiting while also providing overcurrent protection, undervoltage and overvoltage protection capabilities.

The hotswap controller may gate the +12V_EDGE and +3.3V_EDGE based on the PRSNTB[3:0]# value. Per Section 3.6.3, a card is present in the system when the encoded value is not 0b1111. The PRSNTB[3:0]# may be AND'ed together and connected to the hotswap controller to accomplish this result. Per the OCP NIC 3.0 mechanical definition (Section 3.1.1), the present pins are short pins and engage only when the card is positively seated.

Baseboards that do not support hot insertion, or hot extractions may opt to not implement these features.

3.12 Power Sequence Timing Requirements

The following figure shows the power sequence of PRSNTB[3:0]#, +3.3V_EDGE, +12V_EDGE relative to AUX_PWR_EN, BIF[2:0]#, MAIN_PWR_EN, PERSTn*, and PCIe REFCLK stable on the baseboard. Additionally the OCP NIC 3.0 card power ramp, and NIC_PWR_GOOD are shown. Please refer to Section 3.5.4 for the NIC_PWR_GOOD definition. Refer to DMTF DSP0222 for details on the NC-SI clock startup requirements.

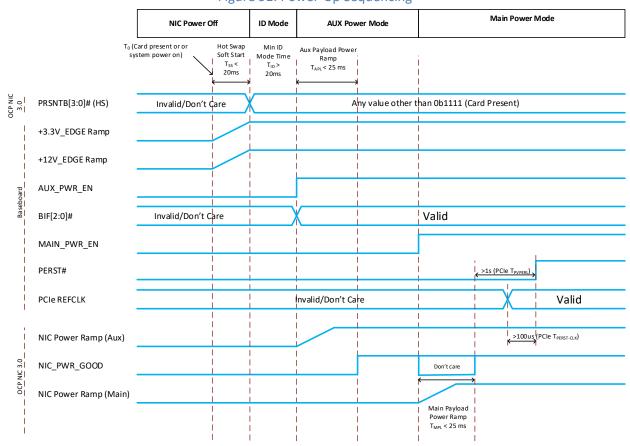


Figure 91: Power-Up Sequencing

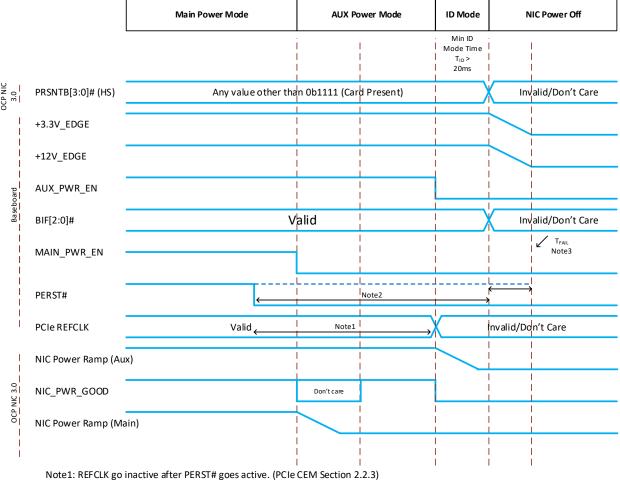


Figure 92: Power-Down Sequencing

 $Note 2: PERST\#\ goes\ active\ before\ the\ power\ on\ the\ connector\ is\ removed.\ (PCIe\ CEM\ Section\ 2.2.3)$

Note 3: In the case of a surprise power down, PERST# goes active T_{FAL} after power is no longer stable.

Table 43: Power Sequencing Parameters

Parameter	Value	Units	Description
T _{ss}	20	ms	Maximum time between system +3.3V_EDGE and +12V_EDGE ramp
			to power stable.
T _{ID}	>20	ms	Minimum guaranteed time per spec to spend in ID mode.
T _{APL}	<25	ms	Maximum time between AUX_PWR_EN assertion to
			NIC_PWR_GOOD assertion.
T _{MPL}	<25	ms	Maximum time between MAIN_PWR_EN assertion to
			NIC_PWR_GOOD assertion.
T _{PVPERL}	>1	S	Minimum time between NIC_PWR_GOOD assertion in Main Power
			Mode and PERST# deassertion. For OCP NIC 3.0 applications, this
			value is >1 second. This is longer than the minimum value specified
			in the PCIe CEM Specification, Rev 4.0.
T _{PERST-CLK}	>100	μs	Min Time REFCLK is stable before PERST# inactive

T _{FAIL}	<500	ns	In the case of a surprise power down, PERST# goes active T _{FAIL} after
			power is no longer stable.

Management and Pre-OS Requirements

OCP NIC 3.0 card management is an important aspect to overall system management. This section specifies a common set of management requirements for OCP NIC 3.0 implementations. There are three types of implementations (RBT+MCTP Type, RBT Type, and MCTP Type) depending on the physical sideband management interfaces, transports, and traffic supported over different transports. An OCP NIC 3.0 implementation shall support at least one type of implementation for card management. For a given type of implementation, an OCP NIC 3.0 card shall support type specific requirements described in Sections 4.1 through 4.7.

Table 44: OCP NIC 3.0 Management Implementation Definitions

Management Type	Definition
RBT Type	The RBT Type management interface is exclusive to the Reduced Media
	Independent Interface (RMII) Based Transport (RBT). The NIC card is required
	to support the DSP0222 Network Controller Sideband Interface (NC-SI)
	Specification for this management
RBT+MCTP Type	The RBT+MCTP management interface supports both the RBT and MCTP
	standards, specifically DSP0222 Network Controller Sideband Interface (NC-SI)
	Specification, DSP0236 Management Component Transport Protocol (MCTP)
	Base Specification, and the associated binding specifications. This is the
	preferred management implementation for baseboard NIC cards. See MCTP
	Type below for more details
MCTP Type	The MCTP management interface supports MCTP standards specifically
	DSP0236 Management Component Transport Protocol (MCTP) Base
	Specification and the associated binding specifications. The PMCI Platform
	Layer Data Model (PLDM) will be the primary payload (or "MCTP Message")
	to convey information from the OCP 3.0 NIC to the management controller.
	The NC-SI over MCTP Message Type may also be used monitoring and pass-
	through communication.

4.1 Sideband Management Interface and Transport

OCP NIC 3.0 sideband management interfaces are used by a Management Controller (MC) or Baseboard Management Controller (BMC) to communicate with the NIC. Table 45 summarizes the sideband management interface and transport requirements.

Requirement **RBT+MCTP RBT Type** Type

Table 45: Sideband	Management Interf	ace and Trans	port Requirements

Management Component Transport Protocol (MCTP) Base	Required	N/A	Required
1.3 (DSP0236 1.3 compliant) over MCTP/SMBus Binding			
(DSP0237 1.1 compliant)			
PCIe VDM compliant physical interface	Optional	Optional	Optional
Management Component Transport Protocol (MCTP) Base	Optional	Optional	Optional
1.3 (DSP0236 1.3 compliant) over MCTP/PCIe VDM Binding			
(DSP0238 1.0 compliant)			

4.2 NC-SI Traffic

DMTF DSP0222 defines two types of NC-SI traffic: Pass-Through and Control. Table 46 summarizes the NC-SI traffic requirements.

Requirement **RBT+MCTP RBT Type MCTP** Type Type NC-SI Control over RBT (DMTF DSP0222 1.1 or later Required Required N/A compliant) NC-SI Control over MCTP (DMTF DSP0261 1.2 compliant) Required N/A Required NC-SI Pass-Through over RBT (DMTF DSP0222 1.1 compliant) Required Required N/A NC-SI Pass-Through over MCTP (DMTF DSP0261 1.2 Optional N/A Optional compliant)

Table 46: NC-SI Traffic Requirements

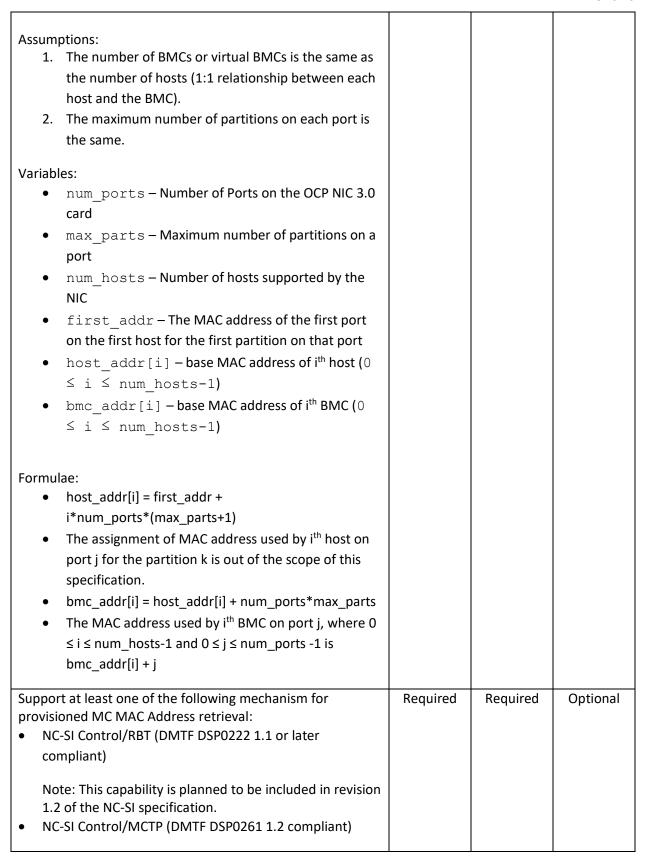
Note: A Management Controller (MC) is allowed to use NC-SI Control traffic only without enabling NC-SI pass-through.

4.3 Management Controller (MC) MAC Address Provisioning

An OCP NIC 3.0 compliant card that supports NC-SI pass-through shall provision one or more MAC addresses for Out-Of-Band (OOB) management traffic. The number of MC MAC addresses provisioned is implementation dependent. These MAC addresses are not exposed to the host(s) as available MAC addresses. The MC is not required to use these provisioned MAC addresses. Table 47 summarizes the MC MAC address provisioning requirements.

Requirement	RBT+MCTP	RBT Type	MCTP
	Type		Type
One or more MAC Addresses shall be provisioned for the MC.	Required	Required	Optional
The OCP NIC 3.0 platform may use the NIC vendor allocated MAC addresses for the BMC. Each management channel requires a dedicated MAC address. Some platforms may employ multiple BMCs (or virtual BMCs) each with a dedicated MAC address. The NIC may also support multiple partitions on a physical port.			
The recommended MAC address allocation scheme is stated below.			

Table 47: MC MAC Address Provisioning Requirements



4.4 Temperature Reporting

An OCP NIC 3.0 implementation can have several silicon components including one or more ASICs implementing NIC functions and one or more transceiver modules providing physical network media connectivity. For the system management, it is important that temperatures of these components can be retrieved over sideband interfaces.

The temperature reporting interface shall be accessible in Aux Power Mode (S5), and Main Power Mode (S0). Table 48 summarizes temperature reporting requirements. These requirements improve the system thermal management and allow the baseboard management device to access key component temperatures on an OCP NIC 3.0 card. When the temperature reporting function is implemented, it is recommended that the temperature reporting accuracy is within ±3°C.

Table 48: Temperature Reporting Requirements

Requirement	RBT+MCTP	RBT Type	MCTP Type
	Type		
Component Temperature Reporting for a component with TDP ≥8W	Required	Required	Required
Component Temperature Reporting for a component with TDP <8W	Recommended	Recommended	Recommended
When the temperature sensor reporting function is implemented, the OCP NIC 3.0 card shall support PLDM for Platform Monitoring and Control (DSP0248 1.1 compliant) for temperature reporting.	Required	Required	Required
When the temperature sensor reporting function is implemented, the OCP NIC 3.0 card shall report upper-warning, upper-critical, and upper-fatal thresholds for PLDM numeric sensors. Note: For definitions of the warning, critical, and fatal thresholds, refer to DSP0248 1.1.	Required	Required	Required
When the temperature reporting function is implemented using PLDM numeric sensors, the temperature tolerance shall be reported.	Required	Required	Required
Support for NIC self-shutdown. The purpose of this feature is to "self-protect" the NIC from permanent damage due to high operating temperature experienced by the NIC. The NIC shall monitor its temperature and shutdown itself as soon as the threshold value is	Required	Required	Required
reached. The value of the self-shutdown threshold is implementation specific. It is recommended that the self-shutdown threshold value is higher than the maximum			

junction temperature of the ASIC implementing the NIC function and this value is between the	
critical and fatal temperature thresholds.	
Note: It is assumed that a system management	
function will prevent a component from	
reaching its fatal threshold temperature.	
The OCP NIC 3.0 card does not need to know	
the reason for the self-shutdown threshold	
crossing (e.g. fan failure). After entering the	
self-shutdown state, the OCP NIC 3.0 card is not	
required to be operational. This might cause	
the system with the OCP NIC 3.0 card to	
become unreachable via the NIC. An AC power	
cycle of the system may be required to bring	
the NIC back to an operational state. In order to	
recover the NIC from the self-shutdown state,	
the OCP NIC 3.0 card should go through the NIC	
power off state as described in Section 3.9.1.	

4.5 Power Consumption Reporting

An OCP NIC 3.0 implementation may be able to report the power consumed by one or more component implementing NIC functions. It is important for the system management that the information about the power consumption can be retrieved over sideband interfaces. Table 49 summarizes power consumption reporting requirements.

Requirement	RBT+MCTP	RBT Type	МСТР
	Туре		Туре
Component Estimated Power Consumption Reporting	Required	Required	Required
Component Runtime Power Consumption Reporting	Optional	Optional	Optional
PLDM for Platform Monitoring and Control (DSP0248 1.1	Required	Required	Required
compliant) for component power consumption reporting			

Table 49: Power Consumption Reporting Requirements

4.6 Pluggable Transceiver Module Status and Temperature Reporting

A pluggable transceiver module is a compact, hot-pluggable transceiver used to connect the OCP 3.0 NIC to an external physical medium. It is important for proper system operation to know the presence and temperature of pluggable transceiver modules. Table 50 summarizes pluggable module status reporting requirements.

Table 50: Pluggable Module Status Reporting Requirements

RBT+MCTP RBT

Requirement	RBT+MCTP	RBT Type	MCTP
	Type		Type
Pluggable Transceiver modules Presence Status and	Required	Required	Required
Temperature Reporting			

PLDM for Platform Monitoring and Control (DSP0248 1.1	Required	Required	Required
compliant) for reporting the pluggable transceiver module			
presence status and pluggable transceiver module			
temperature			

4.7 Management and Pre-OS Firmware Inventory and Update

An OCP NIC 3.0 implementation can have different types of firmware components for data path, control path, and management path operations. It is desirable that OCP NIC 3.0 implementations support an OS-independent mechanism for the management firmware update. It is desirable that the management firmware update does not require a system reboot for the new firmware image to become active. Table 51 summarizes the firmware inventory and update requirements.

6	, ,	· ·	
Requirement	RBT+MCTP	RBT Type	MCTP
	Type		Type
Network boot in UEFI driver (supporting both IPv4 and	Required	Required	Required
IPv6 addressing for network boot)			
UEFI secure boot for UEFI drivers	Required	Required	Required
UEFI secure firmware update	Required	Required	Required
PLDM for Firmware Update (DSP0267 1.0 compliant)	Required	Recommended	Required

Table 51: Management and Pre-OS Firmware Inventory and Update Requirements

4.7.1 Secure Firmware

It is highly recommended that an OCP NIC 3.0 card supports a secure firmware feature. In the future versions of the OCP NIC 3.0 specification, the secure firmware feature is intended to be required. When the secure firmware feature is enabled and where export compliance permits, the OCP NIC 3.0 card shall verify firmware components prior to the execution, execute only signed and verified firmware components, and only allow authenticated firmware updates. Where applicable, an OCP NIC 3.0 implementation shall use the guidelines provided in NIST SP 800-193 (draft) Platform Resiliency Guidelines for the following secure firmware functions:

- Signed Firmware Updates
- Ensure only valid/authenticated firmware updates can be applied. Refer to: NIST 800-193
 Section 3.5 Firmware Update Mechanisms, and 4.1.2 Root of Trust for Update (RTU) and Chain of Trust for Update (CTU)
- Ensure authentication mechanisms cannot be bypassed. Refer to NIST 800-193 Section 4.2 Protection.
- Secure Boot
- Only boot trusted/authenticated firmware: NIST 800-193 4.1.3 Root of Trust for Detection (RTD) and Chain of Trust for Detection (CTD), and Section 4.3 Detection
- Recovery mechanism in case of boot failure: NIST 800-193 Section 4.4 Recovery

4.7.2 Firmware Inventory

The OCP NIC 3.0 card shall allow queries to obtain the firmware component versions, device model, and device ID via in-band and out-of-band interfaces without impacting NIC function and performance of said paths.

4.7.3 Firmware Inventory and Update in Multi-Host Environments

A multi-host capable OCP NIC 3.0 card shall gracefully handle concurrent in-band queries from multiple hosts and out-of-band access from the BMC for firmware component versions, device model, and device ID information.

A multi-host capable OCP NIC 3.0 card shall only permit one entity to perform write accesses to NIC firmware at a time, without creating contention.

A multi-host capable OCP NIC 3.0 card shall gracefully handle exceptions when more than one entity attempts to perform concurrent NIC firmware writes.

4.8 NC-SI Package Addressing and Hardware Arbitration Requirements

NC-SI over RBT is implemented via RMII pins between the MC and the OCP NIC 3.0 card. Protocol and implementation details of NC-SI over RBT can be found in the DMTF DSP0222 standard.

4.8.1 NC-SI over RBT Package Addressing

NC-SI over RBT capable OCP NIC 3.0 cards shall use a unique Package ID per ASIC when multiple ASICs share the single NC-SI physical interconnect to ensure there are no addressing conflicts.

Baseboards use the Slot_ID pin on the Primary Connector for this identification. The Slot_ID value may be directly connected to GND (Slot ID = 0), or pulled up to +3.3V_EDGE (Slot ID = 1).

Package ID[2:0] is a 3-bit field and is encoded in the NC-SI Channel ID as bits [7:5]. Package ID[2] defaults to 0b0 in the NC-SI specification, but is optionally configurable if the target silicon supports configuring this bit. Package ID[1] is directly connected to the SLOT_ID pin. Package ID[0] is set to 0b0 for Network Controller ASIC #0. For an OCP NIC 3.0 card with two discrete silicon instances, Package ID[0] shall be set to 0b1 for Network Controller ASIC #1. Refer to the specific endpoint device datasheet for details on the Package ID configuration options.

Up to four silicon devices are supported on the bus if only Package ID[1:0] is configurable (e.g. Package ID[2] is statically set to 0b0). Up to eight silicon devices are supported on the NC-SI bus if Package ID[2:0] are all configurable.

Refer to the DMTF DSP0222 standard for more information on package addressing, Slot ID and Package ID.

4.8.2 Arbitration Ring Connections

For baseboards that implement two or more Primary Connectors, the NC-SI over RBT arbitration ring may be connected to each other. The arbitration ring shall support operation with a one card, or both cards installed. Figure 80 shows an example connection with dual Primary Connectors.

4.9 SMBus 2.0 Addressing Requirements

The SMBus provides a low speed management bus for the OCP NIC 3.0 card. The FRU EEPROM and onboard temperature sensors are connected on this bus. Additionally, network controllers may utilize the SMBus 2.0 interface for MCTP communications. OCP NIC 3.0 does not support MCTP over I²C due to the use of specific SMBus 2.0 addressing. Proper power domain isolation shall be implemented on the NIC.

4.9.1 SMBus Address Map

OCP NIC 3.0 cards shall support SMBus ARP (be ARP-capable) to allow the cards to be dynamically assigned addresses for MCTP communications to avoid address conflicts and eliminate the need for manual configuration of addresses. The address type of dynamic addresses can be either dynamic and persistent address device or dynamic and volatile address device. Refer to SMBus 2.0 specification and Section 6.11 of DSP0237 1.1 for details on SMBus address assignment.

A system implementation may choose to only use fixed addresses for an OCP NIC 3.0 card on the system. The assignment of these fixed addresses is system dependent and outside the scope of this specification. When fixed addresses are assigned to OCP NIC 3.0 card, then the OCP NIC 3.0 card shall be a fixed and discoverable SMBus device. Refer to SMBus 2.0 specification for more details.

All predefined SMBus addresses for OCP NIC 3.0 are shown in Table 52. Baseboard and OCP NIC 3.0 card designers must ensure additional devices do not conflict. The addresses shown are in 8-bit format and represent the read/write address pair.

Address (8-bit)	Device	Notes
0xA0 / 0xA1 - SLOT0	EEPROM	On-board FRU EEPROM.
0xA2 / 0xA3 - SLOT1		
		Mandatory. Powered from Aux power domain.
		The EEPROM ADDRO pin shall be connected to the SLOT_ID
		pin on the OCP NIC 3.0 card gold finger to allow up to two
		OCP NIC 3.0 cards to exist on the same I ² C bus.

Table 52: SMBus Address Map

4.10 FRU EEPROM

4.10.1 FRU EEPROM Address, Size and Availability

The FRU EEPROM provided for the baseboard to determine the card type and is directly connected to the SMBus on the card edge. Only one EEPROM is required for a single physical OCP NIC 3.0 card regardless of the PCIe width or number of physical card edge connectors it occupies. The FRU EEPROM shall be connected to the Primary Connector SMBus.

The EEPROM is addressable at the addresses indicated in Table 52. The write/read pair is presented in 8-bit format. The size of EEPROM shall be at least 4Kbits for the base EEPROM map. OCP NIC 3.0 card suppliers may use a larger size EEPROM if needed to store vendor specific information.

The FRU EEPROM is readable in all three power states (ID mode, AUX(S5) mode, and MAIN(S0) mode.

4.10.2 FRU EEPROM Content Requirements

The FRU EEPROM shall follow the data format specified in the IPMI Platform Management FRU Information Storage Definition v1.2. Both the Product Info and Board Info records shall be populated in the FRU EEPROM. Where applicable, fields common to the Product Info and Board Info records shall be populated with the same values so they are consistent.

The OEM record 0xC0 is used to store specific records for the OCP NIC 3.0. For an OCP NIC 3.0 card, the FRU EEPROM OEM record content based on the format defined in Table 53 shall be populated.

Table 53: FRU EEPROM Record – OEM Record 0xC0, Offset 0x00

Offset	Length	Description
0	3	Manufacturer ID.
		For OCP NIC 3.0 compliant cards, the value of this field shall be set to the OCP IANA assigned number. This value is 0x7FA600, LS byte first. (42623 in decimal)
3	1	OCP NIC 3.0 FRU OEM Record Version.
		For OCP NIC 3.0 cards compliant to this specification, the value of this field shall be set to 0x01.
4	1	Card Max power (in Watts) in MAIN(S0) mode.
		0x00 – 0xFE – Card power rounded up to the nearest Watt for fractional values. 0xFF – Unknown
5	1	Card Max power (in Watts) in AUX(S5) mode.
		0x00 – 0xFE – Card power rounded up to the nearest Watt for fractional values. 0xFF – Unknown
6	1	Hot Aisle Card Cooling Tier.
		The encoded value reports the OCP NIC 3.0 Card Hot Card Cooling Tier as defined in Section 6.6.1.
		0x00 – RSVD
		0x01 – Hot Aisle Cooling Tier 1
		0x02 – Hot Aisle Cooling Tier 2
		0x03 – Hot Aisle Cooling Tier 3
		0x04 – Hot Aisle Cooling Tier 4 0x05 – Hot Aisle Cooling Tier 5
		0x06 – Hot Aisle Cooling Tier 6
		0x07 – Hot Aisle Cooling Tier 7
		0x08 – Hot Aisle Cooling Tier 8
		0x09 – Hot Aisle Cooling Tier 9
		0x0A – Hot Aisle Cooling Tier 10
		0x0B – Hot Aisle Cooling Tier 11
		0x0C – Hot Aisle Cooling Tier 12
		0x0D – 0xFE – Reserved
		0xFF – Unknown
7	1	Cold Aisle Card Cooling Tier.
		The encoded value reports the OCP NIC 3.0 Card Cold Aisle Cooling Tier as defined in Section 6.6.2.
		0x00 – RSVD
		0x01 – Cold Aisle Cooling Tier 1
		0x02 – Cold Aisle Cooling Tier 2
		0x03 – Cold Aisle Cooling Tier 3
		0x04 – Cold Aisle Cooling Tier 4
		0x05 – Cold Aisle Cooling Tier 5
		0x06 – Cold Aisle Cooling Tier 6
		0x07 – Cold Aisle Cooling Tier 7
		0x08 – Cold Aisle Cooling Tier 8 0x09 – Cold Aisle Cooling Tier 9
		0x0A – Cold Aisle Cooling Tier 10
		0x0B – Cold Aisle Cooling Tier 11

	1	
		0x0C – Cold Aisle Cooling Tier 12
		0x0D – 0xFE – Reserved
		0xFF – Unknown
8	1	Card active/passive cooling.
		This bit defines if the card has passive cooling (there is no fan on the card) or active cooling (a fan is located on the card).
		0x00 – Passive Cooling
		0x01 – Active Cooling
		0x02 – 0xFE – Reserved
		0xFF – Unknown
9	2	Hot aisle standby airflow requirement.
		The encoded value represents the amount of airflow, in LFM, required to cool the card in AUX (S5) mode while operating in a hot aisle environment.
		Byte 9 is the LS byte, byte 10 is the MS byte.
		0x0000-0xFFFE – LFM required for cooling card in Hot Aisle Operation.
		0xFFFF – Unknown.
11	2	Cold aisle standby airflow requirement.
		The encoded value represents the amount of airflow, in LFM, required to cool the
		card in AUX (S5) mode while operating in a cold aisle environment.
		Byte 11 is the LS byte, byte 12 is the MS byte.
		0x0000-0xFFFE – LFM required for cooling card in Cold Aisle Operation. 0xFFFF – Unknown.
13	1	Temperature Target Max – ASIC 0.
		$0x00 - 0xFE - The T_{max}$ value of ASIC 0. The temperature value is in degrees Celsius. $0xFF - Unknown$
14	1	Temperature Target Max – ASIC 1.
		$0x00 - 0xFE - The T_{max}$ value of ASIC 0. The temperature value is in degrees Celsius. $0xFF - Unknown$
15:30	16	Reserved for future use.
		Set each byte to 0xFF for this version of the specification.
31	1	Number of physical controllers (N).
		This byte denotes the number of physical controllers on the OCP NIC 3.0 card. If N=0, no controllers exist on this OCP NIC 3.0 card and this is the last byte in the FRU OEM Record.
		If $N\geq 1$, then the controller UDID records below shall be included for each controller N .
32+16*(N-	16	Controller N UDID.
1):16*N+31		MS Byte First (to align the FRU order to the reported UDID order on the SMBus). This field is populated for values of N≥1 for each controller N.
<u> </u>	1	

5 Routing Guidelines and Signal Integrity Considerations

5.1 NC-SI Over RBT

For the purposes of this specification, the min and max electrical trace length of the NC-SI signals shall be between 2 inches and 4 inches. The traces shall be implemented as 50 Ohm impedance controlled nets. This requirement applies to both the small and large form factor OCP NIC 3.0 cards.

5.2 SMBus 2.0

This section is a placeholder for SMBus 2.0 related routing guidelines and SI considerations. The OCP NIC 3.0 subgroup intends to define the bus operational speed range, capacitive loading, range of pull up resistance values. Doing so allows the baseboard suppliers to design a SMBus interface that is compatible with OCP NIC 3.0 products.

5.3 PCle

This section is a placeholder for the PCIe routing guidelines and SI considerations.

OCP NIC 3.0 card suppliers shall follow the PCIe routing specifications. At this time, the OCP NIC 3.0 subgroup is working to identify and agree to the channel budget for an OCP NIC 3.0 card and leave sufficient margin for the baseboard. Refer to the PCIe CEM and PCIe Base specifications for end-to-end channel signal integrity considerations.

6 Thermal and Environmental

6.1 Airflow Direction

The OCP NIC 3.0 is designed to operate in either of two different airflow directions which are referred to as Hot Aisle and Cold Aisle. In both Hot Aisle and Cold Aisle configurations all airflow is directed over the topside of the card. Component placement must assume that no airflow will exist on the bottom side of the card. The local approach air temperature and speed to the card is dependent on the capability of the system adopting OCP NIC 3.0 card. These parameters may be impacted by the operational altitude and relative humidity in Hot Aisle or Cold Aisle configurations. Design boundary conditions for Hot Aisle and Cold Aisle cooling are included below in Sections 6.1.1 and 6.1.2 respectively.

The two airflow directions should not result in multiple thermal solutions to separately satisfy the varying thermal boundary conditions. Ideally, any specific OCP NIC 3.0 card design should function in systems with either Hot Aisle or Cold Aisle cooling. Thermal analysis in support of this specification have shown the Hot Aisle configuration to be more challenging than Cold Aisle but card vendors should make that determination for each card that is developed.

6.1.1 Hot Aisle Cooling

The airflow in typical server systems will approach from the card edge or heatsink side of the card. This airflow direction is referred to as Hot Aisle cooling and is illustrated below in Figure 93. The term Hot Aisle refers to the card being located at the rear of the system where the local inlet airflow is preheated by the upstream system components (e.g. HDD, CPU, DIMM, etc.).

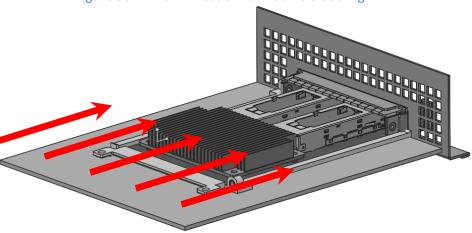


Figure 93: Airflow Direction for Hot Aisle Cooling

The boundary conditions for Hot Aisle cooling are shown below in Table 54 and Table 55. The low temperature is listed at 5°C and assumes fresh air could be ducted to the back of the system from the front. More typically the inlet temperature to the OCP NIC 3.0 card will be in the same range as PCle cards located at the back of the system – 55°C. Depending on the system design, power density, and airflow the inlet temperature to the OCP NIC 3.0 card may be as high as 60°C or 65°C. The airflow velocities listed in Table 55 represent the airflow velocities typical in mainstream servers. Higher airflow velocities are available within the Hot Aisle cooling tiers listed in Table 59 but card designers must be sure to understand the system level implications of such high card LFM requirements.

Table 54: Hot Aisle Air Temperature Boundary Conditions

	Low	Typical	High	Max
Local Inlet air	5°C	55°C	60°C	65°C
temperature	(system inlet)	33 C	00 C	03 C

Table 55: Hot Aisle Airflow Boundary Conditions

	Low	Typical	High	Max
Local inlet air	50 LFM	100-200 LFM	300 LFM	System
velocity	50 LFIVI	100-200 LFIVI	300 LFIVI	Dependent

6.1.2 Cold Aisle Cooling

When installed in the front of a server the airflow will approach from the I/O connector (e.g. SFP, QSFP or RJ-45) side of the card. This airflow direction is referred to as Cold Aisle cooling and is illustrated below in Figure 94. The term Cold Aisle refers to the card being located at the front of the system where the local inlet airflow is assumed to be the same temperature as the system inlet airflow.

Figure 94: Airflow Direction for Cold Aisle Cooling

The boundary conditions for Cold Aisle cooling are shown below in Table 56 and Table 57. The temperature values listed in Table 56 assume the inlet temperature to the OCP NIC 3.0 card to be the same as the system inlet. The low, typical, high, and max temperatures listed align with the ASHRAE A1, A2, A3, and A4 environmental classes. Depending on the system, the supported ASHRAE class may be limit the maximum temperature to the OCP 3.0 NIC card. However, for more broad industry support, cards should be designed to the upper end of the ASHRAE classes (i.e. A4).

Table 56: Cold Aisle Air Temperature Boundary Conditions

	Low	Typical	High	Max	
Local Inlet Air	5°C	25-35°C	40°C	45°C	
Temperature	5 C	ASHRAE A1/A2	ASHRAE A3	ASHRAE A4	

Table 57: Cold Aisle Airflow Boundary Conditions

	Low	Typical	High	Max
Local Inlet Air	50 LFM	100 LFM	200 LFM	System
Velocity	JU LFIVI	TOO FLIAI	ZOO LFIVI	Dependent

6.2 Design Guidelines

The information in this section is intended to serve as a quick reference guide for OCP NIC 3.0 designers early in the design process. The information should be used as a reference for upfront thermal design and feasibility and should not replace detailed card thermal design analysis. The actual cooling capability of the card shall be defined based on the testing with the OCP NIC 3.0 thermal test fixture documentation in Section 6.4.

6.2.1 ASIC Cooling – Hot Aisle

The ASIC or controller chip is typically the highest power consumer on the card. Thus, as OCP NIC 3.0 cards are developed it is important to understand the ASIC cooling capability. Figure 95 below provides an estimate of the maximum ASIC power that can be supported as a function of the local inlet velocity for the small card form factor. Each curve in Figure 95 represents a different local inlet air temperature from 45°C to 65°C.

The curves shown in Figure 95 were obtained using CFD analysis of a reference OCP NIC 3.0 small form factor card. The reference card has a 20mm x 20mm ASIC with two QSFP connectors. Figure 96 shows a comparison of the 3D CAD and CFD model geometry for the reference OCP NIC 3.0 card. Additional card geometry parameters and boundary conditions used in the reference CFD analysis are summarized in Table 58. The OCP NIC 3.0 simulation was conducted within a virtual version of the test fixture defined in Section 6.4.

An increase in the supported ASIC power or a decrease in the required airflow velocity may be achieved through heatsink size and material changes. For example, a larger heatsink or a heatsink made out of copper could improve ASIC cooling and effectively shift up the supportable power curves shown in Figure 95.

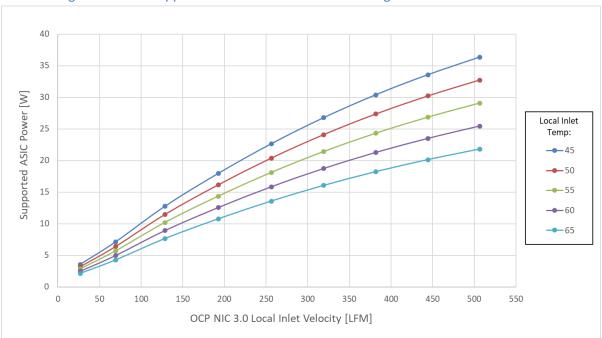


Figure 95: ASIC Supportable Power for Hot Aisle Cooling – Small Card Form Factor

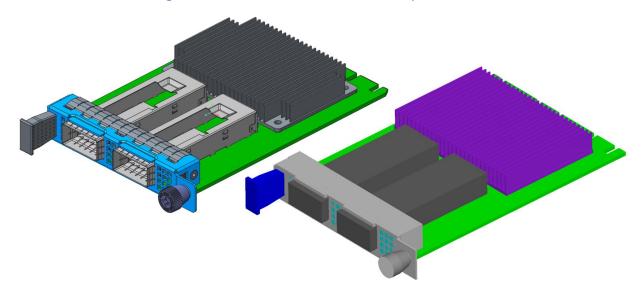


Figure 96: OCP NIC 3.0 Reference Geometry CAD & CFD

Table 58: Reference OCP NIC 3.0 Small Card Geometry

OCP NIC 3.0 Form Factor	Small Card
Heatsink Width	65mm
Heatsink Length	54mm
Heatsink Height	9.24mm
Heatsink Base Thickness	1.5mm
Fin Count/Thickness	28/0.5mm
Heatsink Material	Extruded Aluminum
ASIC Width	20
ASIC Length	20
ASIC Height	2.26
ASIC Theta-JC	0.17 C/W
ASIC Theta-JB	10 C/W
OCP PCB In-Plane Conductivity	34 W/mK
OCP PCB Normal Conductivity	0.33 W/mK
ASIC Max T-case	95°C
OCP NIC 3.0 I/O Connectors	Two QSFP @ 3.5W each

It is important to point out that the curves shown in Figure 95 represent only the maximum ASIC power that can be supported vs. the supplied inlet velocity. Other heat loads on the card may require airflow velocities above and beyond that required to cool the ASIC. SFP or QSFP optical transceivers located downstream of the AISC will in many cases pose a greater cooling challenge than the ASIC cooling. Cooling the optical transceivers becomes even more difficult as the ASIC power is increased due to additional preheating of the air as it moves through the ASIC heatsink. OCP NIC 3.0 designers must consider all heat sources early in the design process to ensure the card thermal solution is sufficient for the feature set.

Card designers must also consider the airflow capability of the server systems that the cards are targeted for use within. Figure 97 below shows the ASIC supportable power curves with an overlay of three server airflow capability ranges. Designers must ensure that their thermal solutions and resulting card airflow requirements fall within the range of supportable system airflow velocity. Cards that are under-designed (e.g. require airflow greater than the system capability) will have thermal issues when deployed into the server system. Card designers are advised to work closely with system vendors to ensure they target the appropriate airflow and temperature boundary conditions.

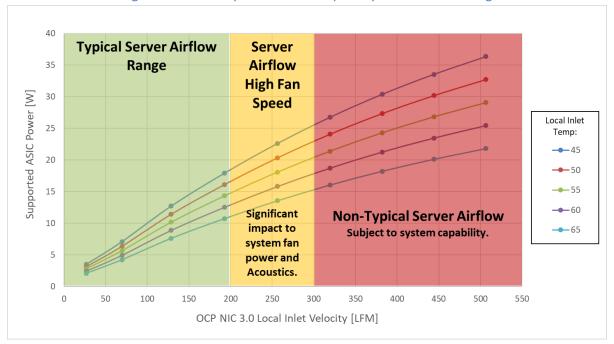


Figure 97: Server System Airflow Capability – Hot Aisle Cooling

6.2.2 ASIC Cooling – Cold Aisle

Compared to the Hot Aisle cooling there are several key differences for Cold Aisle ASIC cooling. With Cold Aisle cooling the airflow is pulled from the I/O connector side of the card. The I/O connectors and faceplate venting may affect the airflow through the ASIC heatsink. The I/O connectors may also preheat the airflow by some amount. In a Cold Aisle cooling configuration, other parallel airflow paths may result in less airflow passing over and through the OCP NIC 3.0 card compared to the Hot Aisle. The ASIC cooling analysis for Cold Aisle was conducted utilizing the same geometry and boundary conditions described in Figure 96 and Table 58 with airflow moving from I/O connector to ASIC (opposite to the Hot Aisle analysis). Figure 98 below shows the results of this analysis for the Cold Aisle cooling configuration. Each curve in Figure 98 represents a different system inlet air temperature from 25°C to 45°C.

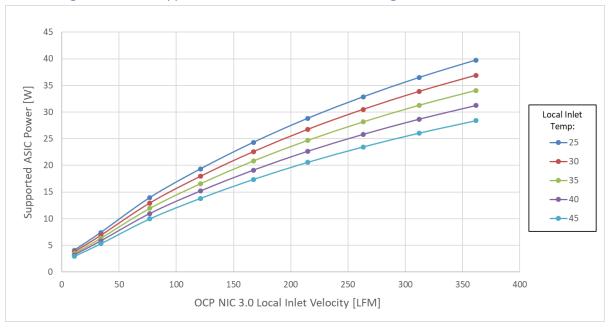


Figure 98: ASIC Supportable Power for Cold Aisle Cooling – Small Card Form Factor

Similar to Figure 97 for Hot Aisle cooling, Figure 99 below shows the ASIC supportable power curves with an overlay of three Cold Aisle server airflow capability ranges. Designers must ensure that their thermal solutions and resulting card airflow requirements fall within the range of supportable Cold Aisle system airflow velocity. Cards that are under-designed (e.g. require airflow greater than the system capability) will have thermal issues when deployed into the server system. Card designers are advised to work closely with system vendors to ensure they target the appropriate airflow and temperature boundary conditions for both Hot and Cold Aisle cooling.

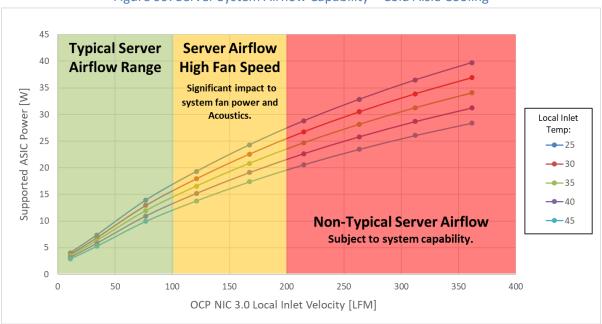


Figure 99: Server System Airflow Capability - Cold Aisle Cooling

A comparison of Hot Aisle (55°C) and Cold Aisle (35°C) ASIC cooling capability curves is shown below in Figure 100. The comparison shows the Hot Aisle ASIC cooling capability at 12W at 150LFM while the cold Aisle cooling capability shows support for 19W at 150LFM. In general, based on the reference geometry, the Cold Aisle cooling configuration allows for higher supported ASIC power at lower velocities due primarily to the lower inlet temperatures local to the OCP NIC 3.0 card when in the Cold Aisle cooling configuration.

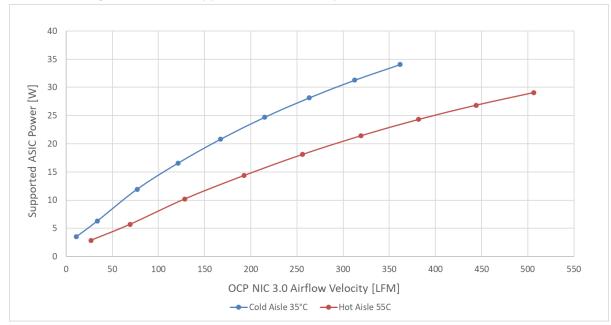


Figure 100: ASIC Supportable Power Comparison – Small Card Form Factor

6.3 Thermal Simulation (CFD) Modeling

Thermal simulation of OCP NIC 3.0 cards using CFD is recommended. The information that follows includes details of the geometry that should be used for CFD modeling of the OCP NIC 3.0 Small form factor. The geometry described below was developed to ensure consistency across card vendors when analyzing the card cooling and thermal solution. The geometry to be used for CFD analysis is based on the OCP NIC 3.0 thermal test fixture detailed in Section 6.4.

6.3.1 CFD Geometry - Small Card

The geometry to be used for CFD analysis is defined by the following parameters:

- Sheet metal enclosure
- Internal width: 128mm
- Internal height: 40.6mm
- Internal length: 256.7mm
- Fixture Faceplate Open Area Ratio: 25% (as shown in Figure 101)
- Internal height between top side of board and fixture cover: 34.94mm
- OCP Card is centered on the width of the host PCB.
- Inlet temperature boundary condition: desired approach temperature, e.g. 55°C
- Airflow boundary condition: Desired volume flow in the range of 1 to 20 CFM

- OCP NIC 3.0 local velocity monitor:
- Hot Aisle Cooling monitor plane 25mm upstream from ASIC heatsink
- Cold Aisle Cooling monitor planes upstream and downstream of ASIC heatsink depending on I/O connector proximity to ASIC heatsink.

CAD step files for the Hot Aisle CFD and Cold Aisle CFD geometry are available for download on the OCP NIC 3.0 Wiki: http://www.opencompute.org/wiki/Server/Mezz.

6.3.2 Transceiver Simulation Modeling

The OCP NIC 3.0 subgroup plans to provide transceiver (both optical and active copper) thermal models to aid in simulating card operational conditions in the Hot Aisle and Cold Aisle.

This section is a placeholder and will be updated in a future revision of this specification.

6.4 Thermal Test Fixture – Small Card

Full definition of the thermal test fixture will be included in a future specification release. Images of preliminary design are shown in Figure 101 and Figure 102.

CAD Files for the current revision of the test fixture are available for download on the OCP NIC 3.0 Wiki: http://www.opencompute.org/wiki/Server/Mezz.

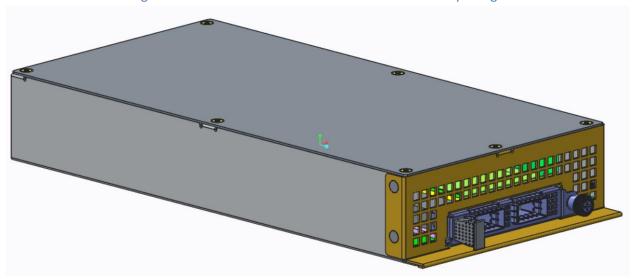
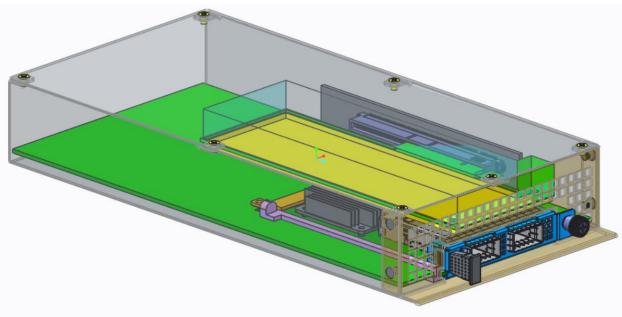


Figure 101: Small Card Thermal Test Fixture Preliminary Design





6.5 Sensor Requirements

See Sections 4.4 to 4.6 for information relating to temperature sensor and reporting requirements.

6.6 Card Cooling Tiers

Section 4.10.2 defines a number of registers that may be read by the associated baseboard system. Two of these registers provide the Hot Aisle and Cold Aisle Card Cooling Tiers that may be used for fan speed control. The Card Cooling Tiers relate the card local inlet temperature to the required local inlet velocity which allows the system to set fan speeds according to the cooling requirements of the card.

The Card Cooling Tier registers are particularly useful for systems that do not implement temperature sensor monitoring. The register may also be used as a backup for cards that do implement temperature sensor monitoring.

6.6.1 Hot Aisle Cooling Tiers

Card Cooling Tiers for Hot Aisle Cooling are defined in Table 59. The values in the table are listed with units shown in LFM. Future releases of this specification will provide more detail to the Card Cooling Tier curve definition.

								, ,				
	Target Operating Region Server Airflow High Fan Speed					Non-Typical Server Airflow - Subject to System Capability						
OCP NIC 3.0 Local Inlet Temperature [°C]	Tier 1	Tier 2	Tier 3	Tier 4	Tier 5	Tier 6	Tier 7	Tier 8	Tier 9	Tier 10	Tier 11	Tier 12
5												
10												
15						k-in		-1416	JCS			
20						11 3. . 0		0816	339			
25				1		K_lili	<u>Lil.a.</u>					
30				<u> </u>	נישען	99						
35												
40												
45												
50												
55	50	100	150	200	250	300	350	400	450	500	750	1000
60												
65												

Table 59: Hot Aisle Card Cooling Tier Definitions (LFM)

6.6.2 Cold Aisle Cooling Tiers

Card Cooling Tiers for Cold Aisle Cooling are defined in Table 60. The values in the table are listed with units shown in LFM. Future releases of this specification will provide more detail to the Card Cooling Tier curve definition.

	Tar	get Opera	ating Reg	ion		Server Airflow High Fan Speed Non-Typical Server Airflow - Subject to System				o System C	apability	
OCP NIC 3.0 Local												
Inlet	Tier 1	Tier 2	Tier 3	Tier 4	Tier 5	Tier 6	Tier 7	Tier 8	Tier 9	Tier 10	Tier 11	Tier 12
Temperat												
ure [°C]												
10						<u>ķ in</u>		NOTE P	<u> </u>			
15				•		l , i n	-P F4	- رکار				
20				—— <i>\</i>	MOA	12-11-	3					
25				-								
30												
35	50	100	150	200	250	300	350	400	450	500	750	1000
40												
45												
50												
55												
60												
65												

Table 60: Cold Aisle Card Cooling Tier Definitions (LFM)

6.7 Shock & Vibration

This specification does not cover the shock and vibration testing requirements for an OCP NIC 3.0 add in card or its associated baseboard systems. OCP NIC 3.0 components are deployed in various environments. It is up to each OCP NIC 3.0 card and baseboard vendor to decide how the shock and vibration tests shall be done.

6.8 Gold Finger Plating Requirements

This section defines the minimum plating/quality requirements for the OCP NIC 3.0 gold fingers.

6.8.1 Host Side Gold Finger Plating Requirements

Per Section 6.4 (Environmental Requirements) of the PCIe CEM specification, the minimum host side gold finger plating is 30 microinches of gold over 50 microinches of nickel. OCP NIC 3.0 card vendors shall individually evaluate the minimum plating required.

The recommendation for OCP NIC 3.0 is to 30 microinches of gold over 150 microinches of nickel.

6.8.2 Line Side Gold Finger Plating Requirements

This section is a placeholder and will be updated in a future revision of the specification.

For the line side golder finger plating, the recommendation from transceiver module vendors is to plate 50 microinches of gold over 50 microinches of nickel

7 Regulatory

7.1 Required Compliance

An OCP NIC 3.0 card shall meet the following Environmental, EMC and safety requirements.

7.1.1 Required Environmental Compliance

- China RoHS Directive
- **EU RoHS 2 Directive (2011/65/EU)** aims to reduce the environmental impact of electronic and electrical equipment (EEE) by restricting the use of certain hazardous materials. The substances banned under RoHS are lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls, polybrominated diphenyl ether, and four phthalates.
- **EU REACH Regulation (EC) No 1907/2006** addresses the production and use of chemical substances and their potential impact on human health and the environment.
- **EU Waste Electrical and Electronic Equipment ("WEEE")** Directive (2012/19/EU) mandates the treatment, recovery and recycling of EEE.
- The Persistent Organic Pollutants Regulation (EC) No. 850/2004 bans production, placing on the market and use of certain persistent organic pollutants.
- The California Safe Drinking Water and Toxic Enforcement Act of 1986 ("Prop 65") sets forth a list of regulated chemicals that require warnings in the State of California.
- The Packaging and Packaging Waste Directive 94/62/EC limits certain hazardous substances in the packaging materials
- Batteries Directive 2006/66/EC regulates the manufacture and disposal of all batteries and accumulators, including those included in appliances.

7.1.2 Required EMC Compliance

Radiated and Conducted Emissions requirements are based on deployed geographical locations.
 Refer to Table 61 for details.

Table 61: FCC Class A Radiated and Conducted Emissions Requirements Based on Geographical Location

Targeted Geography	Applicable Specifications	
USA	FCC, 47 CFR Part 15, Class A digital device (USA)	
Canada	ICES-003, class A (CAN)	
EU	EN 55032: 2015+AC:2016 Class A Radiated and Conducted Emissions requirements for European Union	
	EN 55024: 2010+A1:2015 Immunity requirements for European Union (EU)	
Australia/New Zealand	AS/NZS CISPR 32:2015 Class A	
	CISPR 32:2015 for Radiated and Conducted Emissions requirements	
Japan	VCCI 32-1 Class A Radiated and Conducted Emissions requirements	
Korea	KN32 – Radiated and Conducted Emissions	
	KN35- Immunity	
Taiwan	BSMI CNS13438: 2006 (complete) Class A Radiated and Conducted Emissions requirements	

- **CE** Equipment must pass the CE specification
- All technical requirements covered under EMC Directive (2014/30/EU)

7.1.3 Required Product Safety Compliance

• Safety - requirements are listed in Table 62.

Table 62: Safety Requirements

Targeted Geography	Applicable Specifications
Safety	UL 60950-1/CSA C22.2 No. 60950-1-07, 2nd Edition + Amendment 1 + Amendment 2, dated 2011/12/19.
	The Bi-National Standard for Safety of Information Technology Equipment, EN60950-1: 2006+A11:2009+A1:2010+A12:2010+A2:2013
	IEC 60950-1 (Ed 2) + A1 + A2.
	62368-1 may also be co-reported depending on region

7.2 Recommended Compliance

An OCP NIC 3.0 card is recommended to meet below compliance requirements.

7.2.1 Recommended Environmental Compliance

- **Halogen Free:** IEC 61249-2-21 Definition of halogen free: 900ppm for Bromine or Chlorine, or 1500ppm combined total halogens.
- Arsenic: 1000 ppm (or 0.1% by weight)
- Emerging: US Conflict Minerals law: section 1502 of the Dodd-Frank Act requires companies using tin, tantalum, tungsten, and gold ("3TG") in their products to verify and disclose the mineral source. While this does not apply to products that are used to provide services, such as Infrastructure hardware products, the OCP NIC Subgroup is considering voluntarily reporting of this information.

7.2.2 Recommended EMC Compliance

• 10dB margin to FCC sub-part 15 b class A emission requirements as specified in Section 7.1.2.

8 Revision History

Author	Description	Revision	Date
OCP NIC 3.0 Subgroup	Initial public review.	0.70	01/23/2018