Open Compute Project

OCP NIC 3.0 Design Specification

Version 0.62

Author: OCP Server Workgroup, OCP NIC subgroup

Commented [NT1]: Mechanical drawings will be updated 1/19/2018

All connector/SFF-TA-1002 related items will be updated 1/19/2018 as well. This coincides with the SFF-TA-1002 draft 1.1 release.

Commented [NT2]: General: All PWRDIS has been changed to PWR_EN.

Style Definition: TOC 3: Tab stops: 0.92", Left

Commented [NT3]: The Primary "4C + OCP" connector is now referenced as "4C+" in the SFF-TA-1002 spec. Editor needs to do a global update and reference the connector as "4C+".

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1 Overview

1.1 License

As of July 26, 2016, the following persons or entities have made this Specification available under the Open Compute Project Hardware License (Permissive) Version 1.0 (OCPHL-P)

- OCP NIC Subgroup

An electronic copy of the OCPHL-P is available at:

http://www.opencompute.org/assets/download/01-Contribution-Licenses/OCPHL-Permissive-v1.0.pdf

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Or use Facebook (representing OCP NIC subgroup)

will confirm FB legal before modifying

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1.2 Acknowledgements

The OCP NIC 3.0 specification was created under a collaboration from many OCP member companies, and facilitated by the OCP NIC Subgroup under the OCP Server Workgroup.

The OCP NIC Subgroup would like to acknowledge the following member companies for their contributions to the OCP NIC 3.0 specification:

Table 1: Acknowledgements – By Company

Amphenol ~~ICC / TCS~~
Broadcom
Dell EMC
Facebook
Hewlett Packard Enterprise
Intel Corporation
Lenovo
Mellanox
Netronome
Quanta Cloud Technology
TE

1.3 Background

The OCP NIC 3.0 specification is a follow-on to the OCP Mezz 2.0 rev 1.00 design specification. The OCP NIC 3.0 specification supports two basic card sizes: Small Card, and Large Card. The Small Card allows for up to 16 PCIe lanes on the card edge while a Large Card supports up to 32 PCIe lanes. Compared to the OCP Mezz Card 2.0 Design Specification, the updated OCP NIC 3.0 specification provides a broader solution space for NIC and system vendors to support the following use case scenarios:

- NICs with a higher TDP
- Power delivery ~~Support~~ support up to 80W ~~of power delivery~~ to a single connector (Small) card; and up to 150W to a dual connector (Large) card
    - Note: Baseboard vendors need to evaluate if there is sufficient airflow to thermally cool the OCP NIC 3.0 card. Refer to Section 6 ~~7.1.1~~ for additional details.
- Support up to PCIe Gen5 on the ~~system~~ baseboard and OCP NIC 3.0 card
- Support for up to 32 lanes of PCIe per OCP NIC 3.0 card
- Support for single host, multi-root complex and multi-host environments
- Support a greater board area for more complex OCP NIC 3.0 card designs
- Support for Smart NIC implementations with on-board DRAM and accelerators
- Simplification of FRU installation and removal while reducing overall down time

A representative Small Card OCP NIC 3.0 card is shown in Figure 1 and a representative Large Card is shown in Figure 2.

Figure 1: Representative Small OCP NIC 3.0 Card with Quad SFP Ports

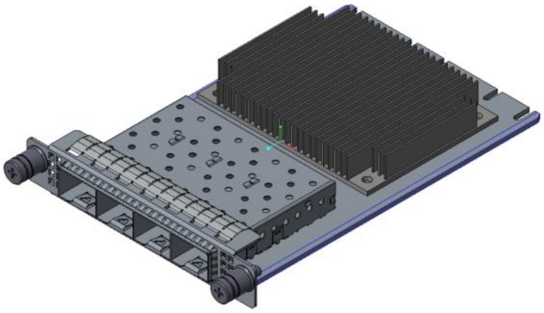
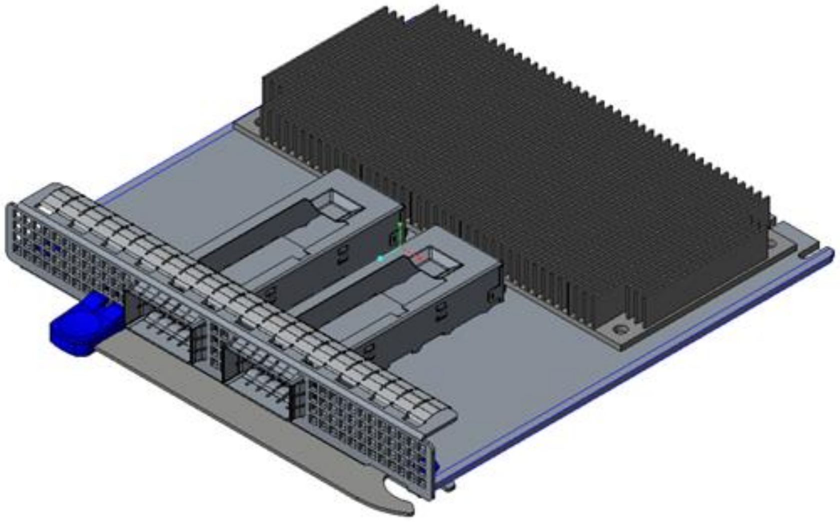


Figure 2: Representative Large OCP NIC 3.0 Card with Dual QSFP Ports and on-board DRAM



In order to achieve the features outlined in this specification, OCP NIC 3.0 compliant cards are not backwards compatible to OCP Mezz 2.0 cards.

This specification is created under OCP Server workgroup – OCP NIC subgroup. An electronic copy of this specification can be found on the Open Compute Project and the OCP Marketplace websites:

http://www.opencompute.org/wiki/Server/Mezz#Specifications_and_Designs

http://opencompute.org/products/specsanddesign?keyword=SPEC%2C+NIC

1.4 Overview

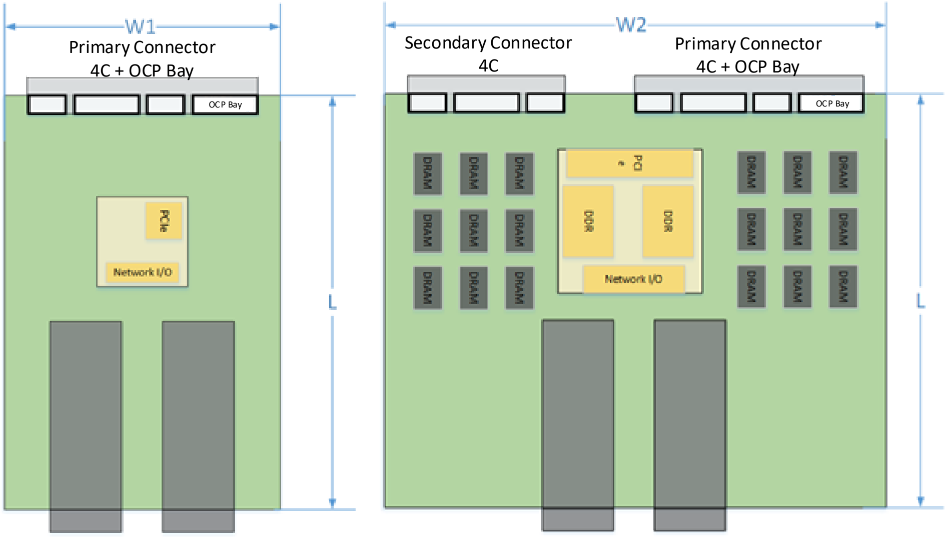
1.4.1 Mechanical Form factor overview

The OCP NIC 3.0 specification defines a third generation mechanical form factor that allows for interoperability between compliant baseboards and OCP NIC 3.0 cards.

OCP NIC 3.0 cards have two form factors – Small and Large. These cards are shown in Figure 3 below. The components shown in the figures are for illustrative purposes. The Small form factor card has one connector (Primary Connector) on baseboard. The Large form factor card has one or two connectors (Primary Connector only and both the Primary and Secondary Connectors) on the baseboard.

Both the Primary and Secondary Connectors are defined in and compliant to SFF-TA-1002. On the OCP NIC 3.0 card side, the card edge is implemented with gold fingers. The Small Card gold finger area only occupies the Primary Connector area for up to 16 PCIe lanes. The Large Card gold finger area may occupy both the Primary and Secondary Connectors for up to 32 PCIe lanes, or optionally just the Primary Connector for up to 16 PCIe lane implementations. The gold finger design follows SFF-TA-1002 as well.

Figure 3: Small and Large Card Form-Factors (not to scale)



The two form factor dimensions are shown in Table 2.

Table 2: OCP 3.0 Form Factor Dimensions

Form Factor	Width	Depth	Primary Connector	Secondary Connector	Typical Use Case
Small	W1 = 76 mm	L = 115 mm	4C + OCP sideband 168 pins	N/A	Low profile and NIC with a similar profile as an OCP NIC 2.0 card; up to 16 PCIe lanes.
Large	W2 = 139 mm	L = 115 mm	4C + OCP sideband 168 pins	4C 140 pins	Larger PCB width to support additional NICs; up to 32 PCIe lanes.

The OCP NIC 3.0 design allows downward compatibility between the two card sizes. Table 3 shows the compatibility between the baseboard and NIC combinations. A Small size baseboard slot may only accept a small sized NIC. A Large size baseboard slot may accept a small or large sized NIC.

Table 3: Baseboard to OCP NIC Form factor Compatibility Chart

Baseboard Slot Size	NIC Size / Supported PCIe Width	
	Small	Large
Small	Up to 16 PCIe lanes	Not Supported
Large	Up to 16 PCIe lanes	Up to 32 PCIe lanes

There are two baseboard connector options available for system designers: straddle mount and right angle (RA). The straddle mount connector option allows the OCP NIC and baseboard to exist in a co-planer position. To achieve this, a cutout exists on the baseboard and is defined in this specification. Alternatively, the right angle option allows the OCP NIC to be installed on top of the baseboard. A baseboard cutout is not required for the right angle connector. The right angle option allows the baseboard to use this area for additional routing or backside component placement. The straddle mount and right angle connectors are shown in Section 3.2.

For both the baseboard and OCP NIC 3.0 card, this specification defines the component and routing keep out areas. Refer to Section 2.5 for details.

Both the straddle mount and right angle implementations shall accept the same OCP NIC 3.0 card and shall be supported in the baseboard chassis regardless of the baseboard connector selection (right angle or straddle mount) so long as the baseboard slot and OCP NIC 3.0 card sizes are a supported combination as shown in Table 3.

This specification defines the form factor at the OCP NIC 3.0 card level, including the front panel, latching mechanism and card guide features.

More details about the card form-factor is shown in Section 2.

1.4.2 Electrical overview

This specification defines the electrical interface between baseboard and the OCP NIC 3.0 card. The electrical interface is implemented with a right angle or straddle mount connector on baseboard and gold finger on the OCP NIC 3.0 card. As previously noted in the mechanical overview, each card may implement a Primary Connector or Primary + Secondary Connector. Cards using only the Primary Connector are suitable for both the Small and Large form-factors and may support up to 16 lanes of PCIe. The Secondary Connector, when used in conjunction with the Primary Connector, allows Large form-factor implementations and may support up to 32 lanes of PCIe.

1.4.2.1 Primary Connector

The Primary Connector provides all OCP specific management functions as well as up to 16 lanes of PCIe between the OCP NIC and the system motherboard.

Management Function Overview (OCP Bay):

- DMTF DSP0222 1.1 compliant Network Controller Sideband Interface (NC-SI) RMII Based Transport (RBT) Physical Interface
- Power management and status reporting
    - Power ~~disable~~break for emergency power reduction
    - State change control
- Control / status serial bus
    - NIC-to-Host status
        - Port LED Link/Activity
        - Environmental Indicators
    - Host-to-NIC configuration Information
- Multi-host PCIe support signals (2x PCIe resets, 2x reference clocks)
    - The OCP bay provides PERST2#, PERST3#, REFCLK2 and REFCLK3. This enables support for up to four hosts when used in conjunction with PERST0#, PERST1#, REFCLK0 and REFCLK1 in the Primary 4C region.
- PCIe Wake signal

See Section 3.5 for a complete list of pin and function descriptions for the OCP Bay portion of the Primary Connector.

PCIe Interface Overview (4C Connector):

- 16x differential transmit/receive pairs
    - Up to PCIe Gen 5 support
- 2x 100 MHz differential reference clocks
- Control signals
    - 2x PCIe Resets
    - Link Bifurcation Control
    - Card power disable/enable
- SMBus 2.0
- Power
    - +12V_EDGE

  - +3.3V_EDGE
  - Power distribution between the aux and main power domains is up to the baseboard vendor

See Section 3.4 for a complete list of pin and function descriptions for the 4C connector.

1.4.2.2 Secondary Connector

The Secondary Connector provides an additional 16 lanes of PCIe and their respective control signals.

PCIe Interface Overview (4C Connector):

- 16x differential transmit/receive pairs
  - Up to PCIe Gen 5 support
- 2x 100 MHz differential reference clocks
- Control signals
  - 2x PCIe Resets
  - Link Bifurcation Control
  - Card power disable/enable
- SMBus 2.0
- Power
  - +12V_EDGE
  - +3.3V_EDGE
  - Power distribution between the aux and main power domains is up to the baseboard vendor

See Section 3.4 for a complete list of pin and function descriptions for the 4C connector.

1.5 References

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- PCIe CEM Specification. *PCI Express Card Electromechanical Specification*, Revision 4.0 (draft).
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- SNIA. SFF-TA-1002, Specification for Protocol Agnostic Multi-Lane High Speed Connector. SNIA SFF TWG Technology Affiliate, Rev 1.~~0~~1 draft, ~~December 12th, 2017~~January 18th, 2018.

1.5.1 Trademarks

* Names and brands may be claimed as trademarks by their respective companies.

2 Card Form Factor

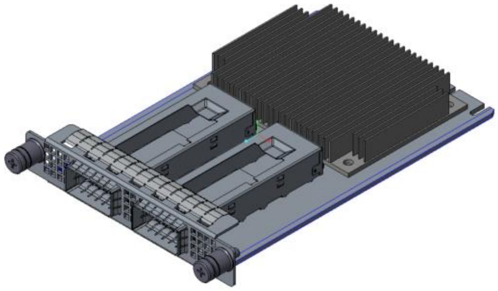
2.1 Form Factor Options

OCP NIC 3.0 provides two fundamental form factor options: a Small Card (76mm x 115mm) and a Large Card (139mm x 115mm).

These form factors support a Primary Connector and optionally, a Secondary Connector. The Primary Connector is defined to be a SFF-TA-1002 compliant 4C connector plus a 28-pin bay for OCP NIC 3.0 specific pins. The Secondary Connector is the 4C connector as defined in SFF-TA-1002. The 4C specification supports up to 32 differential pairs for a x16 PCIe connection per connector. For host platforms, the 28-pin OCP bay is required for the Primary Connector. This is also mandatory for OCP NIC 3.0 cards.

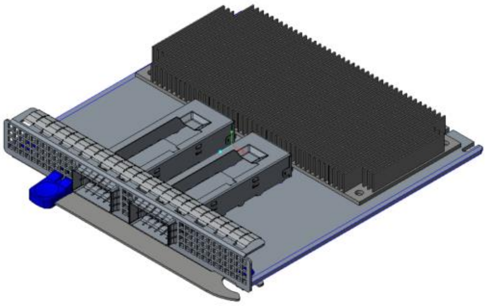
The Small Card uses the Primary 4C connector to provide up to a x16 PCIe interface to the host. The additional 28-pin OCP bay carries sideband management interfaces as well as OCP NIC 3.0 specific control signals for multi-host PCIe support. The small size card provides sufficient faceplate area to accommodate up to 2x QSFP modules, 4x SFP modules, or 4x RJ-45 for BASE-T operation. The Small Card form factor supports up to 80W of delivered power to the card edge.

Figure 4: Example Small Card Form Factor



The Large Card uses the Primary 4C + OCP bay connector to provide the same functionality as the Small Card along with an additional Secondary 4C connector to provide up to a x32 PCIe interface. The Large Card may utilize both the Primary and Secondary Connectors, or just the Primary Connector for lower PCIe lane count applications. Table 4 summarizes the Large Card permutations. The Large Card supports higher power envelopes and provides additional board area for more complex designs. The Large Card form factor supports up to 150W of delivered power to the card edge across the two connectors.

Figure 5: Example Large Card Form Factor



For Large Cards, implementations may use both the Primary and Secondary Connector (as shown in Figure 6), or may use the Primary Connector only (as shown in Figure 7) for the card edge gold fingers.

Figure 6: Primary Connector (4C + OCP Bay) and Secondary Connector (4C) (Large) OCP NIC 3.0 Cards

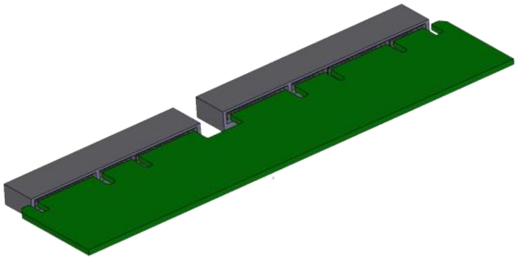
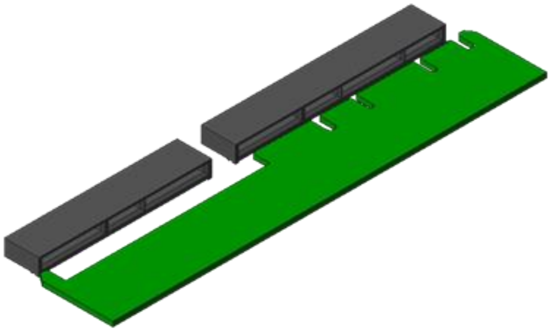


Figure 7: Primary Connector (4C + OCP Bay) Only (Large) OCP NIC 3.0 Cards



For both form-factors, an OCP NIC 3.0 card may optionally implement a subset of pins to support up to a x8 PCIe connection. This is implemented using a 2C card edge per SFF-TA-1002. The Primary Connector may support a 2C sized OCP NIC 3.0 card along with the 28 pin OCP bay. The following diagram from the

SFF-TA-1002 specification illustrates the supported host Primary and Secondary Connectors and OCP NIC 3.0 card configurations.

Figure 8: Primary Connector (4C + OCP Bay) with 4C and 2C (Small) OCP NIC 3.0 Cards

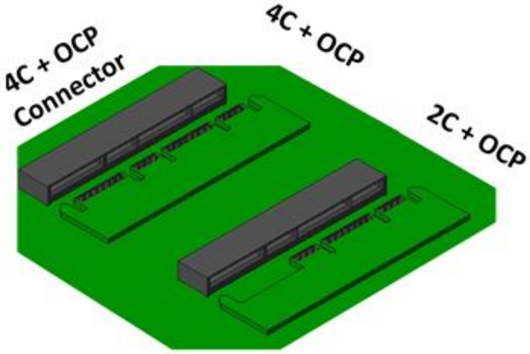


Table 4

~~Table 4~~ summarizes the supported card form factors. Small form factors cards support the Primary Connector and up to 16 PCIe lanes. Large form factor cards support implementations with both the Primary and Secondary Connectors and up to 32 PCIe lanes, or a Primary Connector only implementation with up to 16 PCIe lanes.

Table 4: OCP NIC 3.0 Card Definitions

Add in Card Size and max PCIe Lane Count	**Secondary Connector**		**Primary Connector**		
	4C Connector, x16 PCIe		4C Connector, x16 PCIe		OCP Bay
Small (x8)				2C	OCP Bay
Small (x16)			4C		OCP Bay
Large (x8)				2C	OCP Bay
Large (x16)			4C		OCP Bay
Large (x24)		2C	4C		OCP Bay
Large (x32)	4C		4C		OCP Bay

2.2 I/O bracket

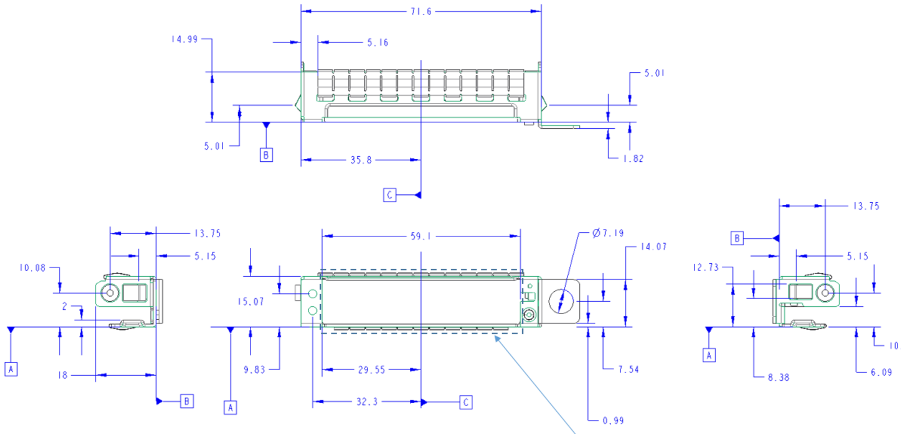
Commented [NT5]: Mechanical drawings to be updated.

The following section defines the standard I/O bracket and standard chassis opening required for both the Small and Large form-factor cards.

2.2.1 Small Form Factor OCP NIC 3.0 Card I/O Bracket

Figure 9 defines the standard Small Card form factor I/O bracket.

Figure 9: Small Card Standard I/O Bracket



*Connectors to be located in this opening. Faceplate cutouts to match specific connector drawing requirements

Note: The OCP NIC 3.0 card supplier shall add port identification on bracket that meet their manufacturing and customer requirements.

For RJ-45 implementations, a customized bracket must be created. Figure 10 shows an implementation example.

Figure 10: Small Card Customized bracket for RJ-45 Connector

Drawing to be inserted

Figure 11 shows the standalone bracket assembly and Figure 12 shows the bracket assembly on the OCP NIC 3.0 card.

Figure 11: Small Card 3D Bracket Assembly (Standalone)

TBD

Figure 12: Small Card 3D Bracket Assembly (Installed on in the OCP NIC 3.0 Card)

TBD

In addition to the sheet metal, Table 5 lists the additional hardware components used for the Small Card bracket assembly.

Table 5: Mechanical BOM for the Small Card Bracket

Item description	Supplier Part Number
Top and bottom EMI fingers	TF187VE32F11
Screw / Rivet (part of bracket assy)?	TBD
Side EMI Finger	TBD
Thumb screw	TBD
Pull Tab	TBD
Latch	TBD
Screw (attaching Bracket & NIC)	TBD
SMT Nut (on NIC)	TBD

Note: The “Pull Tab” shown in the 3D drawings and in Table 5 are tentative. Alternate designs are under evaluation and therefore the BOM may change in the next revision of the specification.

2.2.2 Small Form Factor OCP NIC 3.0 Card Critical-to-Function (CTF) Dimensions

The following dimensions are considered critical-to-function (CTF) for each small form factor OCP NIC 3.0 card.

Figure 13: Small Form Factor OCP NIC 3.0 Card Critical-to-Function (CTF) Dimensions (Top View)

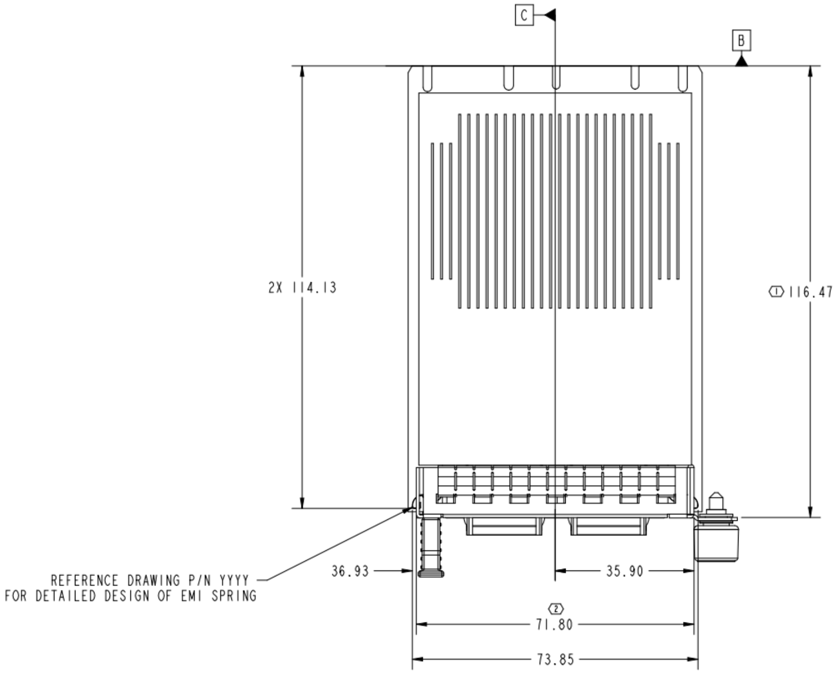


Figure 14: Small Form Factor OCP NIC 3.0 Card Critical-to-Function (CTF) Dimensions (Front View)

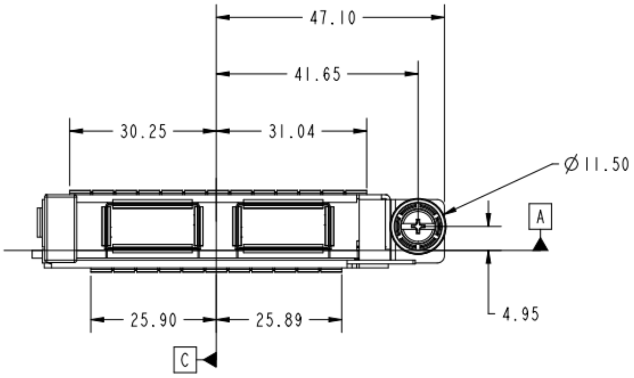


Figure 15: Small Form Factor OCP NIC 3.0 Card Critical-to-Function (CTF) Dimensions (Side View – Left)

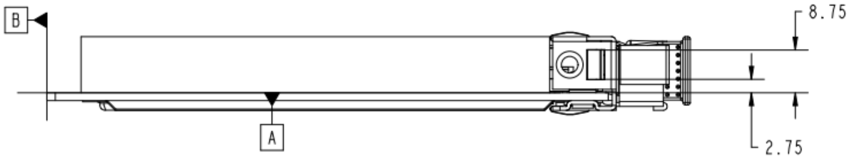
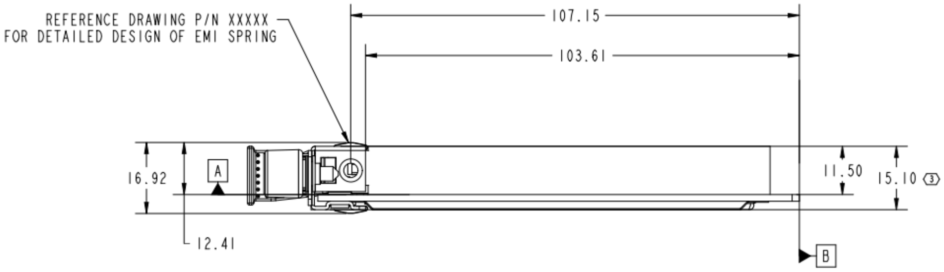


Figure 16: Small Form Factor OCP NIC 3.0 Card Critical-to-Function (CTF) Dimensions (Side View – Right)



2.2.3 Small Form Factor OCP NIC 3.0 Baseboard Critical-to-Function (CTF) Dimensions

The following dimensions are considered critical-to-function (CTF) for each small form factor baseboard chassis.

Figure 17: Small Form Factor Baseboard Chassis Critical-to-Function (CTF) Dimensions (Rear View)

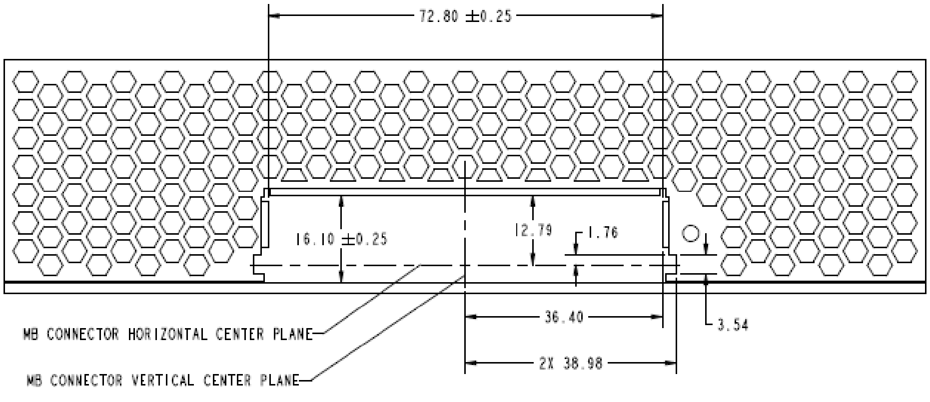


Figure 18: Small Form Factor Baseboard Chassis Critical-to-Function (CTF) Dimensions (Side View)

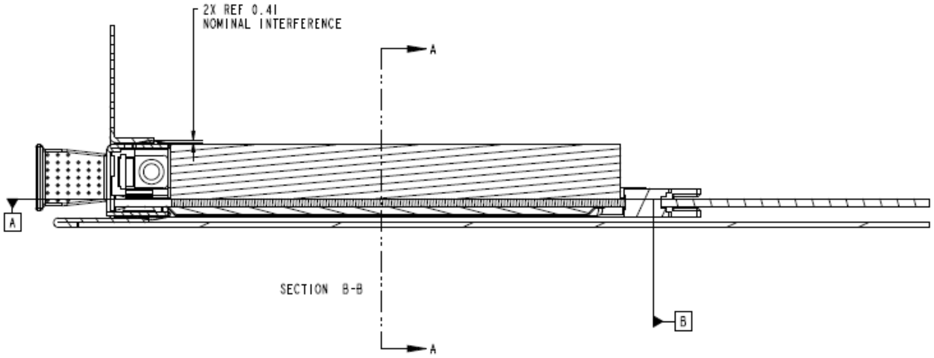


Figure 19: Small Form Factor Baseboard Chassis Critical-to-Function (CTF) Dimensions (Rear Rail Guide View)

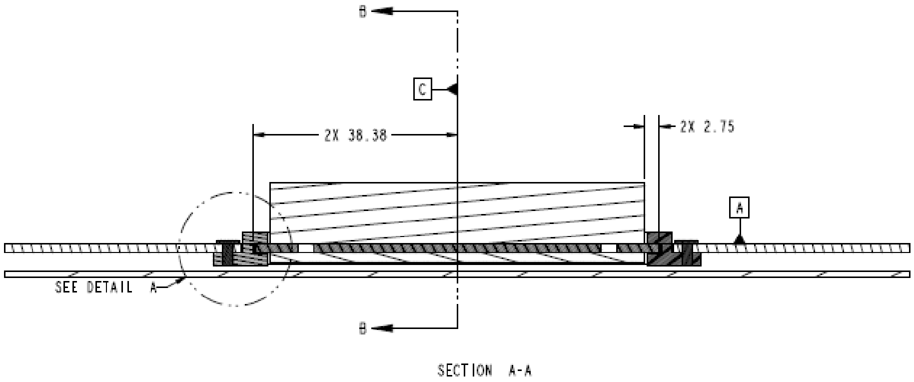
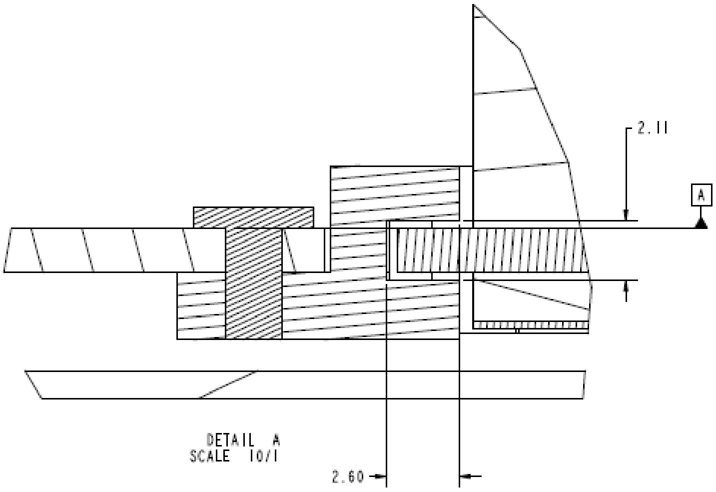


Figure 20: Small Form Factor Baseboard Chassis Critical-to-Function (CTF) Dimensions (Rail Guide Detail)



On the baseboard side, the following mechanical dimensions shall be met to support a small form factor OCP NIC 3.0 card:

Figure 21: Baseboard and Rail Assembly Drawing for Small Cards

TBD; need 3D baseboard and rail assembly drawing.

2.2.4 Large Form Factor OCP NIC 3.0 Card I/O Bracket

TBD. Definition is in progress. All drawings from the Small Form-Factor implementation need to be replicated for the Large form-factor.

Figure 22 defines the standard Large Card form factor I/O bracket.

Figure 22: Large Card Standard I/O Bracket

TBD

Note: The OCP NIC 3.0 card supplier shall add port identification on bracket that meet their manufacturing and customer requirements.

For RJ-45 implementations, a customized bracket must be created. Figure 23 shows an implementation example.

Figure 23: Large Card Customized bracket for RJ-45 Connector

Drawing to be inserted

Figure 24 shows the standalone bracket assembly and Figure 25 shows the bracket assembly on the OCP NIC 3.0 card.

Figure 24: Large Card 3D Bracket Assembly (Standalone)

TBD

Figure 25: Large Card 3D Bracket Assembly (Installed on the OCP NIC 3.0 Card)

TBD

In addition to the sheet metal, Table 6 lists the additional hardware components used for the Small Card bracket assembly.

Table 6: Mechanical BOM for the Large Card Bracket

Item description	**Supplier Part Number**
Top and bottom EMI fingers	TBD
Screw / Rivet (part of bracket assy)?	TBD
Side EMI Finger	TBD
Thumb screw	TBD
Pull Tab	TBD
Latch	TBD
Screw (attaching Bracket & NIC)	TBD
SMT Nut (on NIC)	TBD

Note: The “Pull Tab” shown in the 3D drawings and in Table 6 are tentative. Alternate designs are under evaluation and therefore the BOM may change in the next revision of the specification.

2.2.5 Large Form Factor OCP NIC 3.0 Card Critical-to-Function (CTF) Dimensions

The following dimensions are considered critical-to-function (CTF) for each large form factor OCP NIC 3.0 card.

Figure 26: Large Form Factor OCP NIC 3.0 Card Critical-to-Function (CTF) Dimensions (Top View)

TBD

Figure 27: Large Form Factor OCP NIC 3.0 Card Critical-to-Function (CTF) Dimensions (Front View)

TBD

Figure 28: Large Form Factor OCP NIC 3.0 Card Critical-to-Function (CTF) Dimensions (Side View – Left)

TBD

Figure 29: Large Form Factor OCP NIC 3.0 Card Critical-to-Function (CTF) Dimensions (Side View – Right)

TBD

2.2.6 Large Form Factor OCP NIC 3.0 Baseboard Critical-to-Function (CTF) Dimensions

The following dimensions are considered critical-to-function (CTF) for each large form factor baseboard chassis.

Figure 30: Large Form Factor Baseboard Chassis Critical-to-Function (CTF) Dimensions (Rear View)

TBD

Figure 31: Large Form Factor Baseboard Chassis Critical-to-Function (CTF) Dimensions (Side View)

TBD

Figure 32: Large Form Factor Baseboard Chassis Critical-to-Function (CTF) Dimensions (Rear Rail Guide View)

TBD

Figure 33: Large Form Factor Baseboard Chassis Critical-to-Function (CTF) Dimensions (Rail Guide Detail)

TBD

On the baseboard side, the following mechanical dimensions shall be met to support a large form factor OCP NIC 3.0 card:

Figure 34: Baseboard and Rail Assembly Drawing for Large Card

TBD; need 3D baseboard and rail assembly drawing for Large Card.

2.3 Line Side I/O Implementations

At the time of this writing, the Small and Large form-factor implementations have been optimized to support the following standard line side I/O implementations:

Table 7: OCP NIC 3.0 Line Side I/O Implementations

Form Factor	Max Topology Connector Count
Small	2x QSFP+/QSFP28/QSFP56
Small	4x SFP28+/SFP28/SFP56
Small	4x RJ-45
Large	2x QSFP+/QSFP28/QSFP56
Large	4x SFP+/SFP28/SFP56
Large	4x RJ-45

Note: For brevity, references to QSFP+, QSFP28 and QSFP56 shall be referred to as QSFP in this document. Similarly, references to SFP+, SFP28 and SFP56 shall be referred to as SFP.

Additional combinations and connector types are permissible as I/O form-factor technologies and thermal capabilities evolve.

2.4 Port Numbering and LED Implementations

The OCP NIC 3.0 I/O bracket shall provide port labeling for user identification.

Additionally, LEDs shall be implemented on the OCP NIC 3.0 I/O bracket when there is sufficient space for local indication. LEDs may also be implemented on the card Scan Chain (as defined in Section 3.5.3) for remote link/activity indication on the baseboard. These two cases are described in the sections below. In both cases, the actual link rate may be directly queried through the management interface.

2.4.1 OCP NIC 3.0 Port Naming and Port Numbering

The naming of all OCP NIC 3.0 external ports shall start from Port 0. When viewing the OCP NIC 3.0 card from the I/O side and with the primary side components facing up, Port 0 shall be located on the left hand side. The port numbers shall sequentially increase to the right. Refer to Figure 35 as an example implementation.

2.4.2 OCP NIC 3.0 Card LED Configuration

For low I/O count small form-factor cards without built in light pipes (such as 1x QSFP~~28~~, 2x SFP~~28~~, or 2x RJ-45), or a large form-factor cards, where additional I/O bracket area is available, the card shall implement on-board link/activity indications in place of the Scan Chain LED stream. The recommended local (on-card) LED implementation uses two physical LEDs (a discrete Link/Activity LED and a bi-colored Speed A/Speed B LED). Table 8 describes the OCP NIC 3.0 card LED implementations.

Table 8: OCP NIC 3.0 Card LED Configuration with Two Physical LEDs per Port

LED Pin	LED Color	Description
	Green	Active low. Multifunction LED.

Link / Activity		This LED shall be used to indicate link and link activity. When the link is up and no link activity is present, then this LED shall be lit and solid. This indicates that the link is established, there are no local or remote faults, and the link is ready for data packet transmission/reception. When the link is up and there is link activity, then this LED should blink at the interval of 50-500ms during link activity. The Link/Activity LED shall be located on the left hand side or located on the top for each port when the OCP NIC 3.0 card is viewed in the horizontal plane.
Speed	Green Amber Off	Active low. Bicolor multifunction LED. The LED is Green when the port is linked at its maximum speed. The LED is Amber when the port is linked at it second highest speed. The LED is off when the device is linked at a speed lower than the second highest capable speed, or no link is present. The Amber Speed LED indicator may be used for port identification through vendor specific link diagnostic software. The bicolor speed LED shall be located on the right hand side or located on the bottom for each port when the OCP NIC 3.0 card is viewed in the horizontal plane.

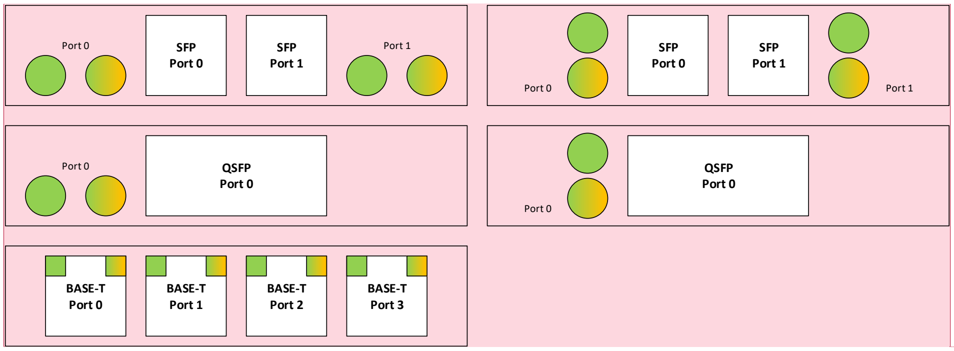
2.4.3 OCP NIC 3.0 Card LED Ordering

For all OCP NIC 3.0 card use cases, each port shall implement the green Link/Activity LED and a bicolor green/amber speed A/B LED.

When the OCP NIC 3.0 card is viewed from the horizontal position, and with the primary component side facing up, ~~For horizontal LED positions,~~ the Link/Activity LED shall be located on the left side for each port and the speed LED shall be located on the right side for each port. The port ordering shall increase from left to right.

The placement of the Link/Activity and Speed LEDs on the faceplate may be left up to the discretion of the OCP NIC 3.0 card designer. The LED port association shall be clearly labeled on the OCP NIC 3.0 card.

Figure 35: Port and LED Ordering – Example Small Card Link/Activity and Speed LED Placement



Commented [JN6]: Suggest to add illustration of PCB in order to show this is "up side up"

2.4.4 Baseboard LEDs Configuration Over the Scan Chain

A small form-factor OCP NIC 3.0 with a fully populated I/O bracket (2x QSFP~~28~~, 4x SFP~~28~~ or 4x RJ-45) does not have sufficient space for discrete on-board (faceplate) LED indicators. In this case, the line side link and activity LED indicators are implemented on the baseboard system via the Scan Chain. The Scan Chain bit stream is defined in Section 3.5.3.

The baseboard LED implementation uses two discrete LEDs (Link/Activity and Speed indication). The physical baseboard LED implementation is left up to the baseboard vendor and is not defined in this specification. The LED implementation is optional for baseboards.

At the time of this writing, the Scan Chain definition allows for up to one link/activity and one speed LED per port. A total of up to 8 ports are supported in the Scan Chain. The bit stream defines the LEDs to be active low (on). The Scan Chain LED implementation allows the NIC LED indicators to be remotely located on the OCP NIC 3.0 compliant chassis (e.g. front LED indicators with rear I/O cards).

2.5 Mechanical Keepout Zones

Commented [NT7]: Mechanical drawings to be updated.

2.5.1 Baseboard Keep Out Zones – Small Card Form Factor

TBD – Need keepout drawings and envelopes for small / large size baseboard including primary/secondary/rail keepouts/cutout for straddle mount/keepout for right angle.

2.5.2 Baseboard Keep Out Zones – Large Card Form Factor

TBD. – need input from mechanical engineering

2.5.3 Small Card Form Factor Keep Out Zones

Figure 36: Small Form Factor Keep Out Zone – Top View

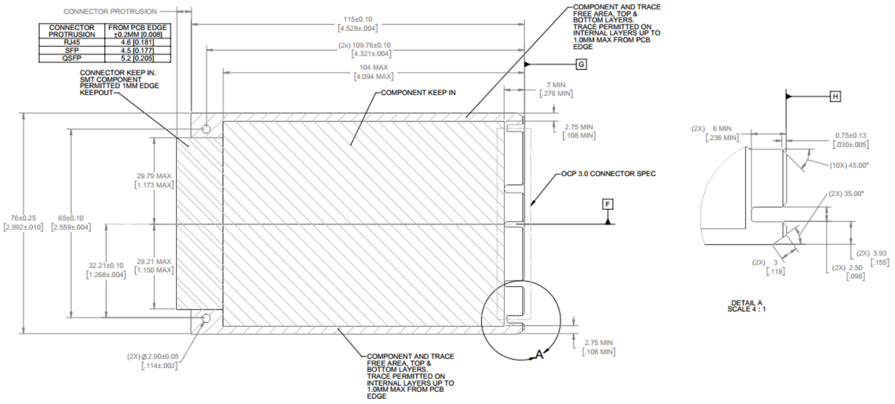


Figure 37: Small Form Factor Keep Out Zone – Bottom View

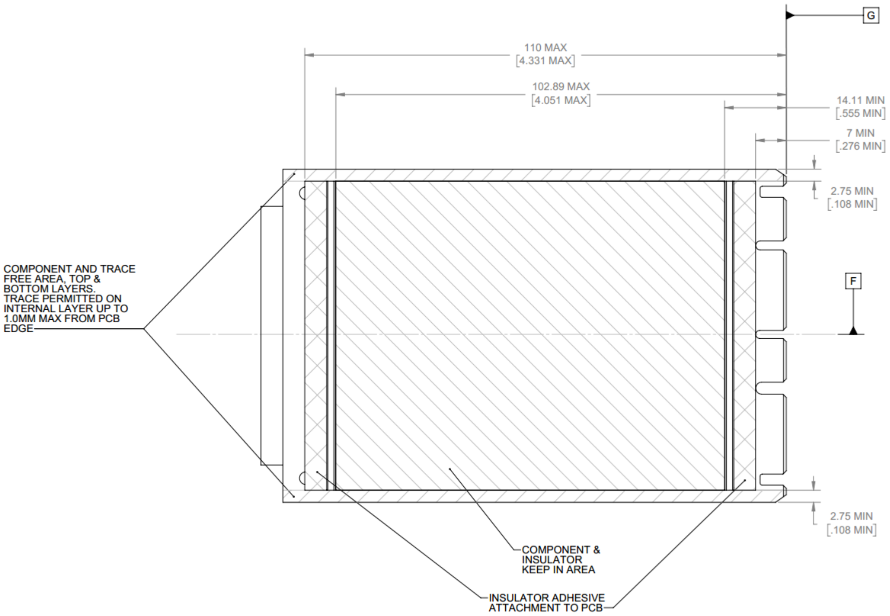
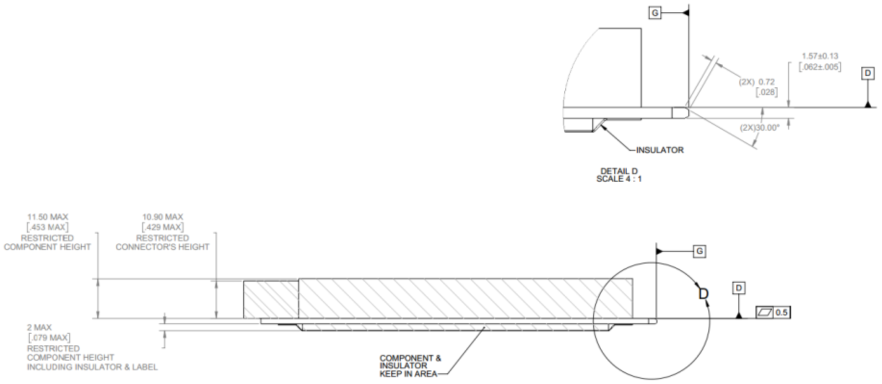


Figure 38: Small Form Factor Keep Out Zone – Side View



2.5.4 Large Card Form Factor Keep Out Zones

Figure 39: Large Form Factor Keep Out Zone – Top View

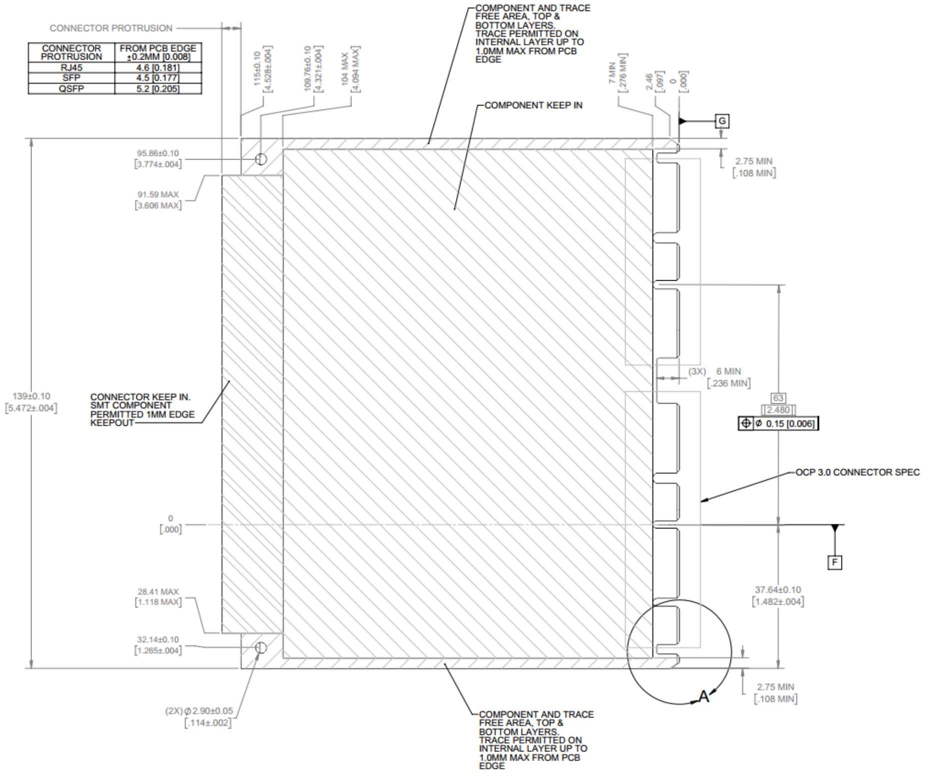


Figure 40: Large Form Factor Keep Out Zone – Bottom View

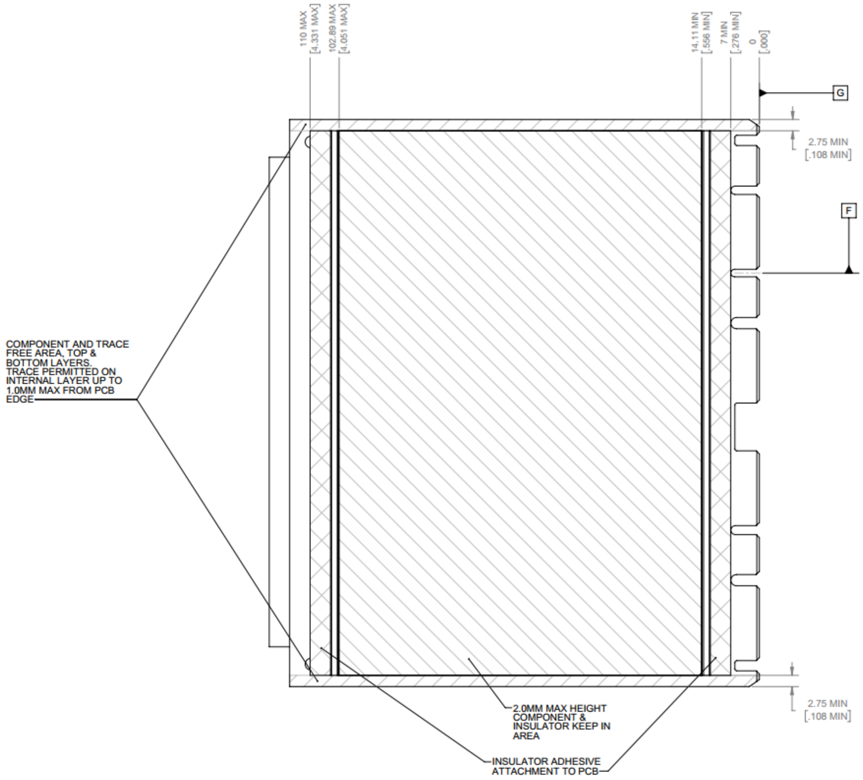
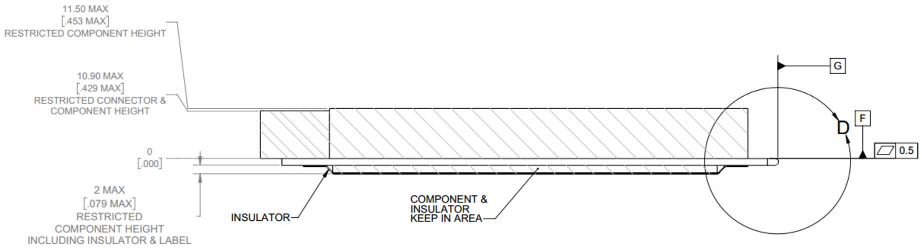


Figure 41: Large Form Factor Keep Out Zone – Side View



2.6 Insulation Requirements

Commented [NT8]: Mechanical drawings to be updated.

All OCP NIC 3.0 cards shall implement an insulator to prevent the bottom side card components from shorting out to the baseboard chassis. The recommended insulator thickness is 0.25mm and shall reside within the following mechanical envelope for the Small and Large size cards.

2.6.1 Small Card Insulator

Figure 42: Small Card Bottom Side Insulator (Top and 3/4 View)

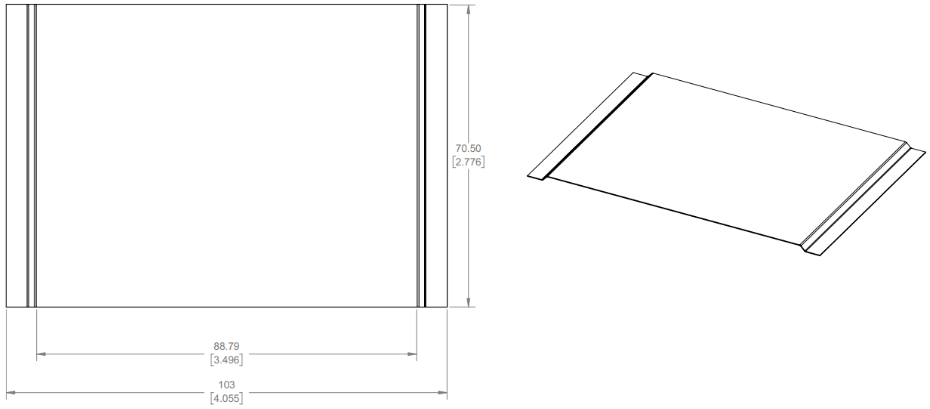
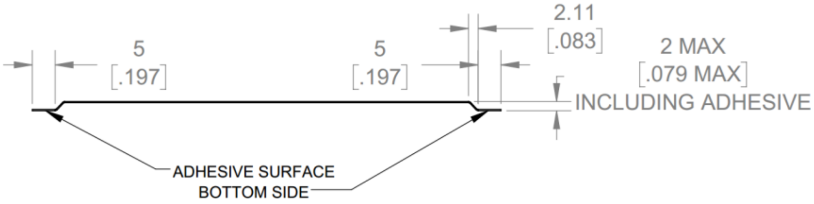


Figure 43: Small Card Bottom Side Insulator (Side View)



2.6.2 Large Card Insulator

Figure 44: Large Card Bottom Side Insulator (Top and 3/4 View)

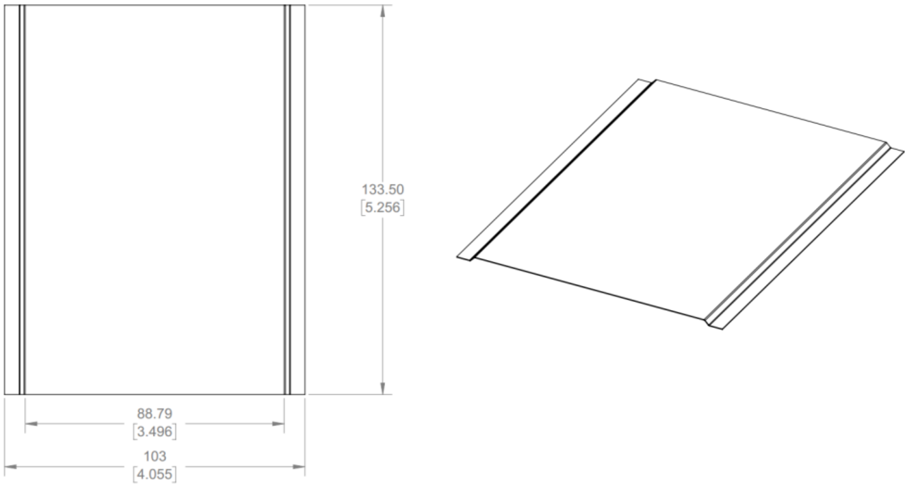
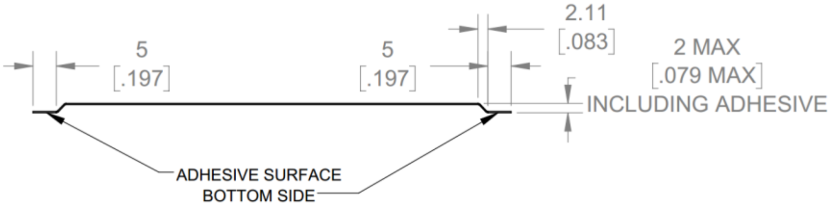


Figure 45: Large Card Bottom Side Insulator (Side View)



2.7 Labeling Requirements

Commented [NT9]: The labeling requirements is a work in progress.

OCP NIC 3.0 cards shall implement all (or a subset of) label items listed below as deemed necessary by each end customer.

2.7.1 NIC Vendor Factory Label

The label is human readable using a Verdana (or equivalent san serif typeface) at 4pt size. The label contains the following information:

- Item 1: Part number with revision
- Item 2: Part number with revision (no spaces, underscores or dashes in the barcode). The barcode encoding format is Code 128. The barcode is variable in length.
- Item 3: CM Part Number
- Item 4: CM Work Order Number
- Item 5: CM Manufacturing Data Code (MM-DD-YY)
- Item 6: Deviation Number – if no deviation is used, print DEV00000

Figure 46: NIC Vendor Factory Label

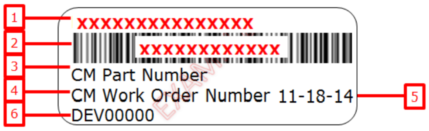


Image of label is for reference only;
actual label will have different data.

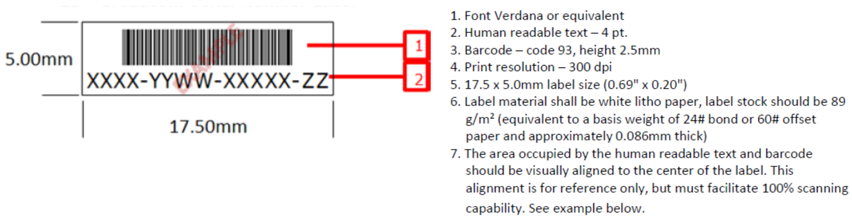
1. Verdana 4 pt. font or equivalent
2. Barcode – code 128
3. 300 DPI printer minimum. Must meet the contrast and print growth requirements per ISO/IES 16022 and have a print quality level of “C” or higher per ISO/IEC 15415
4. 1.000" x 0.400" label size, corner radius 0.025" – 0.100" (0.635mm – 2.54mm)
5. Material: Polyester with acrylic adhesive
6. Color: White
7. Thickness: 0.05mm

2.7.2 NIC Vendor Serial Number Label

The NIC serial number label shall contain the following information:

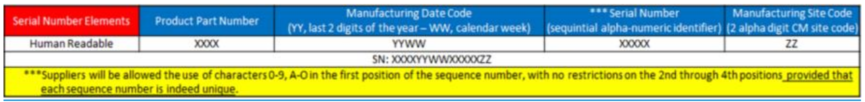
- Item 1: 1D barcode. Encoded as Code 93. No dashes should be encoded in the barcode element.
- Item 2: Human readable serial number uses a Verdana (or equivalent san serif typeface) at 4pt size.

Figure 47: NIC Vendor Serial Number Label



1. Font Verdana or equivalent
2. Human readable text – 4 pt.
3. Barcode – code 93, height 2.5mm
4. Print resolution – 300 dpi
5. 17.5 x 5.0mm label size (0.69" x 0.20")
6. Label material shall be white litho paper, label stock should be 89 g/m² (equivalent to a basis weight of 24# bond or 60# offset paper and approximately 0.086mm thick)
7. The area occupied by the human readable text and barcode should be visually aligned to the center of the label. This alignment is for reference only, but must facilitate 100% scanning capability. See example below.

Figure 48: NIC Vendor Serial Number Label Field Format

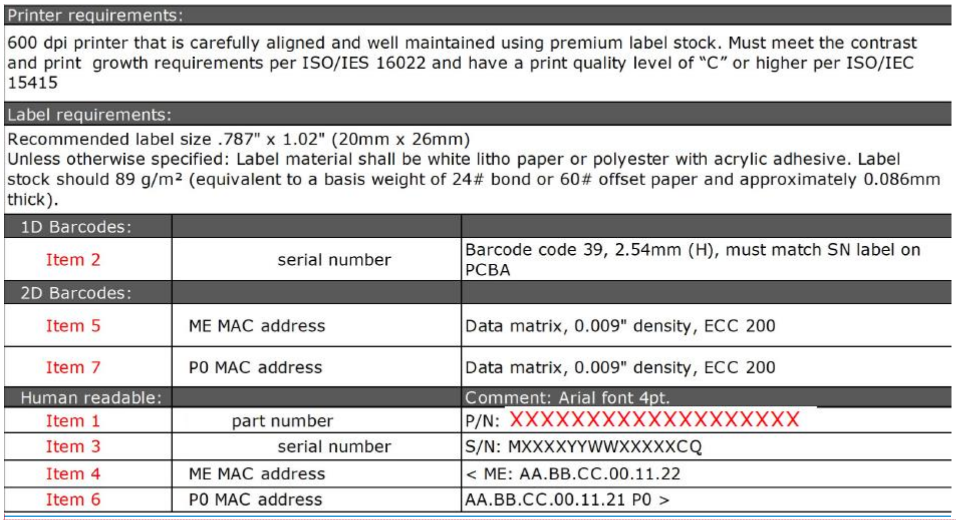


Serial Number Elements	Product Part Number	Manufacturing Date Code (YY, last 2 digits of the year – WW, calendar week)	*** Serial Number (sequintial alpha-numeric identifier)	Manufacturing Site Code (2 alpha digit CM site code)
Human Readable	XXXX	YYWW	XXXXX	ZZ
SN: XXXXYYWWXXXXXZZ				
***Suppliers will be allowed the use of characters 0-9, A-O in the first position of the sequence number, with no restrictions on the 2nd through 4th positions provided that each sequence number is indeed unique.				

2.7.3 Baseboard MAC and Serial Number Label

Figure 49: Baseboard MAC and Serial Number Label

*Image of label is for reference only – actual label will have different data. Refer to PSD for details.



Printer requirements:		
600 dpi printer that is carefully aligned and well maintained using premium label stock. Must meet the contrast and print growth requirements per ISO/IES 16022 and have a print quality level of "C" or higher per ISO/IEC 15415		
Label requirements:		
Recommended label size .787" x 1.02" (20mm x 26mm) Unless otherwise specified: Label material shall be white litho paper or polyester with acrylic adhesive. Label stock should 89 g/m² (equivalent to a basis weight of 24# bond or 60# offset paper and approximately 0.086mm thick).		
1D Barcodes:		
Item 2	serial number	Barcode code 39, 2.54mm (H), must match SN label on PCBA
2D Barcodes:		
Item 5	ME MAC address	Data matrix, 0.009" density, ECC 200
Item 7	P0 MAC address	Data matrix, 0.009" density, ECC 200
Human readable:		Comment: Arial font 4pt.
Item 1	part number	P/N: XXXXXXXXXXXXXXXXXXX
Item 3	serial number	S/N: MXXXXYYWWXXXXXCQ
Item 4	ME MAC address	< ME: AA.BB.CC.00.11.22
Item 6	P0 MAC address	AA.BB.CC.00.11.21 P0 >

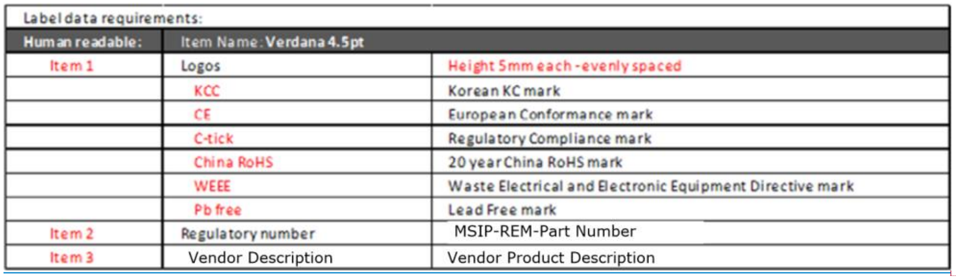
Commented [TN10]: I suggest converting this table over to text. OR make the other label requirements the same format.

2.7.4 Regulatory Label

Figure 50: OCP NIC 3.0 Card Regulatory Label

Image of label is for reference only; actual label will have different data.

1. Verdana 4.5 pt. font or equivalent
2. All logo heights are 5mm
3. 300 DPI printer minimum. Must meet the contrast and print growth requirements per ISO/IES 16022 and have a print quality level of "C" or higher per ISO/IEC 15415
4. 1.500" x 0.750" (35mm – 19mm) label size, corner radius 0.025" – 0.100" (0.635mm – 2.54mm)
5. Material: Polyester with acrylic adhesive
6. Color: White
7. Thickness: 0.05mm



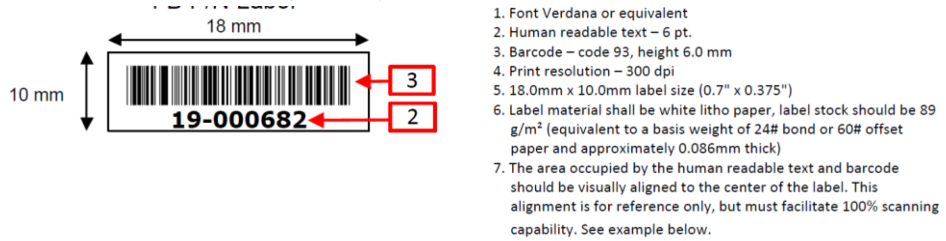
Label data requirements:		
Human readable:	Item Name: Verdana 4.5pt	
Item 1	Logos	Height 5mm each - evenly spaced
	KCC	Korean KC mark
	CE	European Conformance mark
	C-tick	Regulatory Compliance mark
	China RoHS	20 year China RoHS mark
	WEEE	Waste Electrical and Electronic Equipment Directive mark
	Pb free	Lead Free mark
Item 2	Regulatory number	MSIP-REM-Part Number
Item 3	Vendor Description	Vendor Product Description

Commented [TN11]: I suggest converting this table over to text. OR make the other label requirements the same format.

2.7.5 System Vendor Part Number Label

Commented [TN12]: Do we need a baseboard label? I propose we remove this. Just like the baseboard MAC and serial number label.

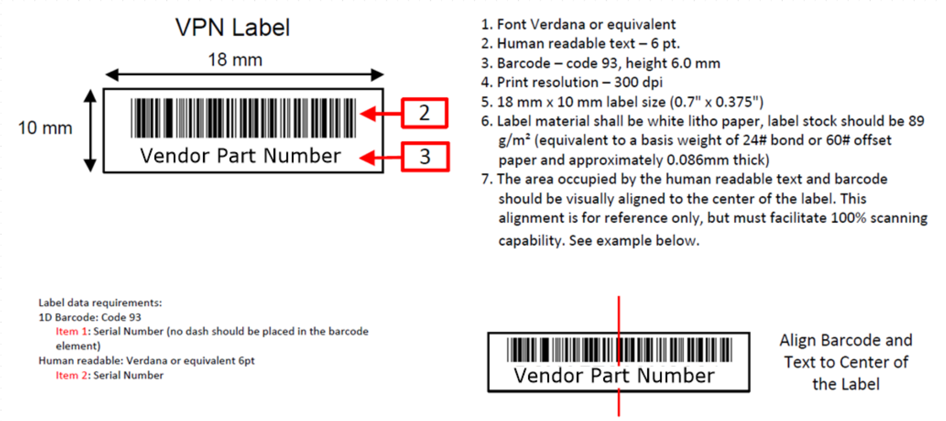
Figure 51: System Vendor Part Number Label



1. Font Verdana or equivalent
2. Human readable text – 6 pt.
3. Barcode – code 93, height 6.0 mm
4. Print resolution – 300 dpi
5. 18.0mm x 10.0mm label size (0.7" x 0.375")
6. Label material shall be white litho paper, label stock should be 89 g/m² (equivalent to a basis weight of 24# bond or 60# offset paper and approximately 0.086mm thick)
7. The area occupied by the human readable text and barcode should be visually aligned to the center of the label. This alignment is for reference only, but must facilitate 100% scanning capability. See example below.

2.7.6 NIC Vendor Part Number Label

Figure 52: OCP NIC 3.0 Card Vendor Part Number Label



1. Font Verdana or equivalent
2. Human readable text – 6 pt.
3. Barcode – code 93, height 6.0 mm
4. Print resolution – 300 dpi
5. 18 mm x 10 mm label size (0.7" x 0.375")
6. Label material shall be white litho paper, label stock should be 89 g/m² (equivalent to a basis weight of 24# bond or 60# offset paper and approximately 0.086mm thick)
7. The area occupied by the human readable text and barcode should be visually aligned to the center of the label. This alignment is for reference only, but must facilitate 100% scanning capability. See example below.

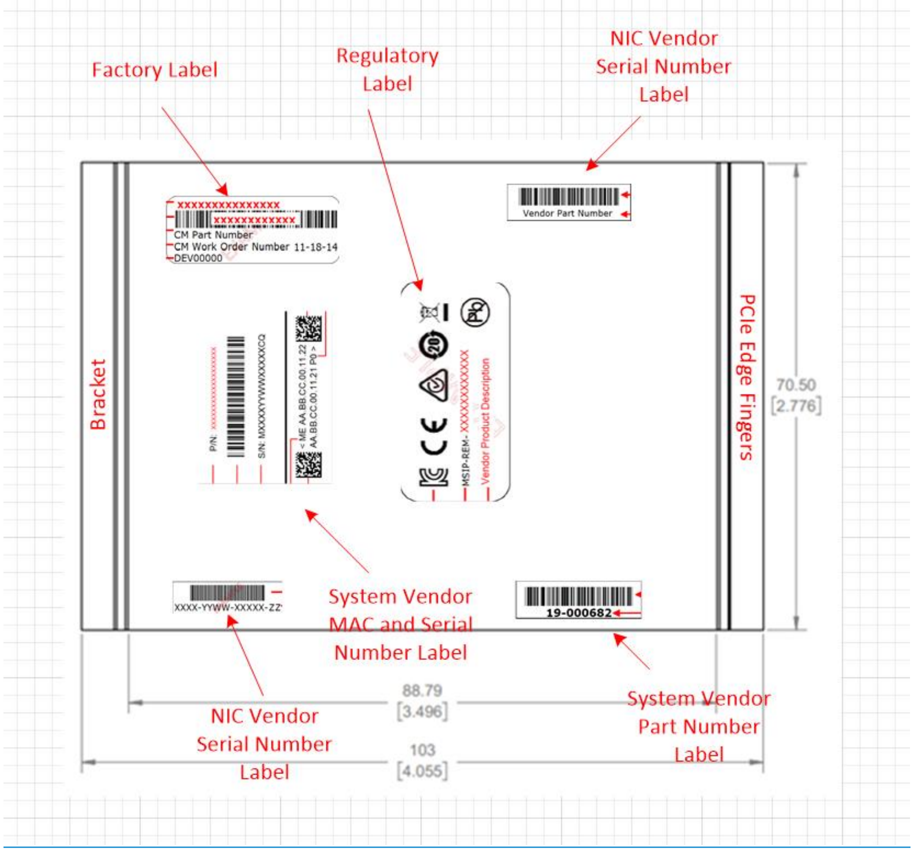
Label data requirements:
1D Barcode: Code 93
  Item 1: Serial Number (no dash should be placed in the barcode element)
Human readable: Verdana or equivalent 6pt
  Item 2: Serial Number

Align Barcode and Text to Center of the Label

2.7.7 Small Card Label Placement

The image below is an example of the label locations for the ~~small card~~Small Card form factor.

Figure 53: Small Card Label Placement Example

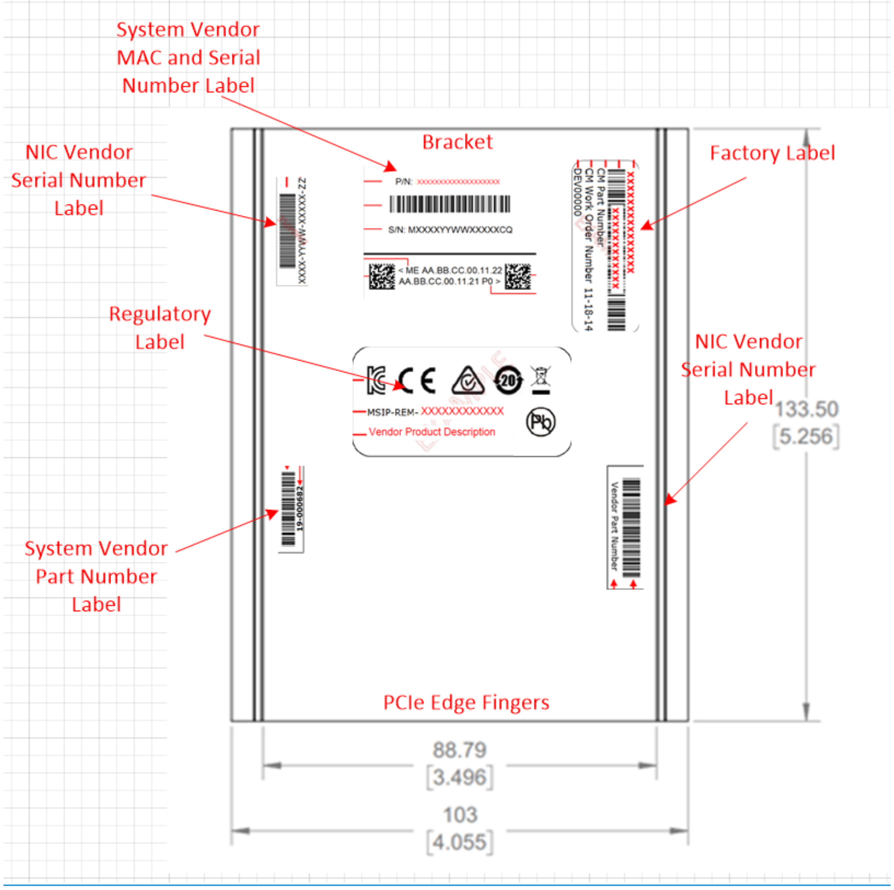


Note: Labels are not to scale in this drawing.

2.7.8 Large Card Label Placement

The image below is an example of the label locations for the ~~large card~~Large Card form factor.

Figure 54: Large Card Label Placement Example



Note: Labels are not to scale in this drawing.

2.8 NIC Implementation Examples

Typical OCP NIC 3.0 implementation examples are included in the 3D CAD package. The purpose of these examples is to demonstrate the implementation feasibility. Additional use cases beyond the implementation examples are possible as long they adhere to the OCP NIC 3.0 specification.

Note: For brevity, references to QSFP+, QSFP28 and QSFP56 shall be referred to as QSFP in this document. Similarly, references to SFP+, SFP28 and SFP56 shall be referred to as SFP.

The 3D CAD files may be obtained from: {TBD}

Table 9: NIC Implementation Examples and 3D CAD

Implementation Example	**3D CAD File name**
Small form factor Single/Dual QSFP ports	
Small form factor Single/Dual SFP ports	
Small form factor Quad SFP ports	
Small form factor Quad 10GBASE-T ports	
Large form factor Single/Dual QSFP ports	
Large form factor Single/Dual SFP ports	
Large form factor Quad SFP ports	
Large form factor Quad 10GBASE-T ports	

2.9 Non-NIC Use Cases

The OCP NIC 3.0 specification is mainly targeted for Network Interface Card applications. It is possible to use the same OCP NIC 3.0 card form-factor, baseboard interface and mechanical design to enable non-NIC use cases. These non-NIC use cases use the same baseboard/OCP NIC 3.0 card interface as defined in Section 3. The non-NIC use cases are not covered in the current revision of the OCP NIC 3.0 specification. Example non-NIC use cases implement various external I/O interfaces and are shown in Table 10.

Table 10: Example Non-NIC Use Cases

Example Use Case	**Card External I/O Interface(s)**
PCIe Retimer Card	PCIe
Accelerator Card	N/A
NVMe Card	N/A
Storage HBA / RAID Card	N/A / TBD

3 Card Edge and Baseboard Connector Interface

3.1 Gold Finger Requirements

Commented [NT13]: All gold finger dimensions will be updated from the SFF-TA-1002 v1.1 draft specification.

The OCP NIC 3.0 cards are compliant to the SFF-TA-1002 specification with respect to the gold fingers and connectors.

Small Size cards fit in the Primary Connector. Primary Connector compliant cards are 76mm x 115mm and may implement the full 168-pins. The Primary Connector cards may optionally implement a subset of gold finger pins if there is a reduced PCIe width requirement (such as 1 x8 and below). In this case, the card edge gold finger may implement a 2C design. The overall board thickness is 1.57mm. The gold finger dimensions for the Primary Connector compliant cards are shown below.

Large Size Cards support up to a x32 PCIe implementation and may use both the Primary and Secondary (4C) Connectors. Large Size Cards may implement a reduced PCIe lane count and optionally implement only the Primary Connector 4C, or 2C plus OCP bay.

Note: The “B” pins on the connector are associated with the top side of the OCP NIC 3.0 card. The “A” pins on the connector are associated with the bottom side of the OCP NIC 3.0 card.

Figure 55: Small Size Primary Connector Gold Finger Dimensions – x16 – Top Side (“B” Pins)

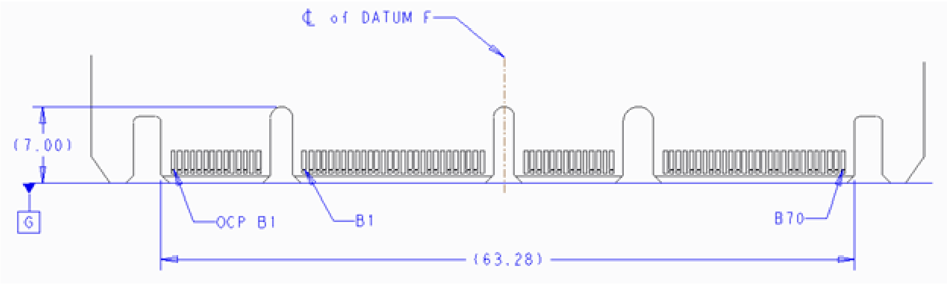


Figure 56: Small Size Primary Connector Gold Finger Dimensions – x16 – Bottom Side (“A” Pins)

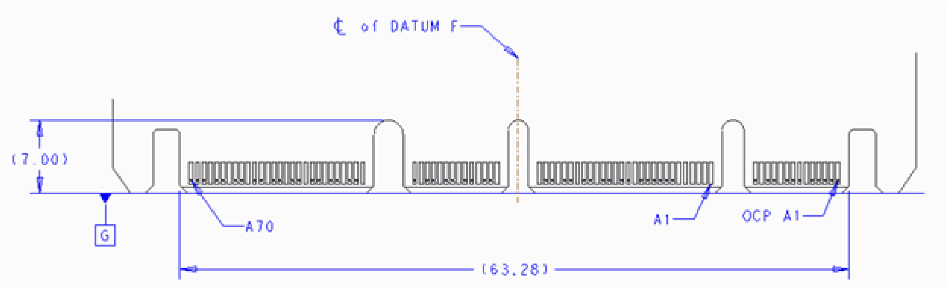


Figure 57: Large Size Card Gold Finger Dimensions – x32 – Top Side (“B” Pins)

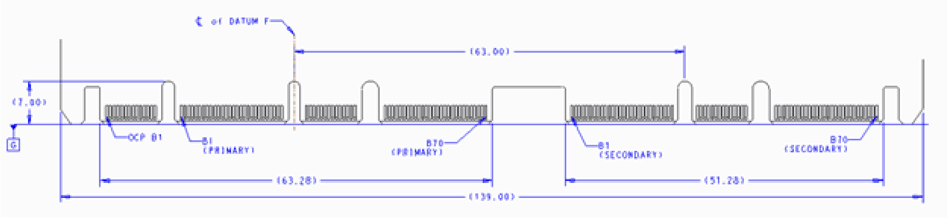
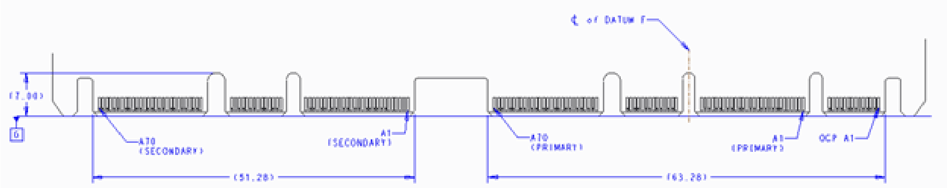


Figure 58: Large Size Card Gold Finger Dimensions – x32 – Bottom Side (“A” Pins)



3.1.1 Gold Finger Mating Sequence

Per the SFF-TA-1002 specification, the Primary and Secondary Connectors are protocol agnostic and are optimized for high speed differential pairs. For use in the OCP NIC 3.0 application, some pin locations are used for single ended control nets or power and would benefit from a shorter pin length for staggering. As such, the recommended OCP NIC 3.0 card gold finger staging is shown in Table 11 for a two stage, first-mate, last-break functionality. The host connectors have a single stage mating and do not implement different pin lengths.

The AIC Plug (Free) side refers to the OCP NIC 3.0 card gold fingers; the receptacle (Fixed) side refers to the physical connector on the host platform. This table is based on the SFF-TA-1002 Table A-1 with modifications for OCP NIC 3.0. Refer to the mechanical drawings for pin the first-mate and second-mate lengths.

Note: Pin names in Table 11 are used for first mate/second mate reference only. Full pin definitions are described in Sections 3.3 and 3.4.

Table 11: Contact Mating Positions for the Primary and Secondary Connectors

Side B					Side A			
	AIC Plug (Free)		Receptacle (Fixed)			AIC Plug (Free)		Receptacle (Fixed)
	2nd Mate	1st Mate				2nd Mate	1st Mate	
OCP B1	NIC_PWR_GOOD				OCP A1	PERST2#		
OCP B2	PWRBRK#				OCP A2	PERST3#		
OCP B3	LD#				OCP A3	WAKE#		
OCP B4	DATA_IN				OCP A4	RBT_ARB_IN		
OCP B5	DATA_OUT				OCP A5	RBT_ARB_OUT		
OCP B6	CLK				OCP A6	GND	🟩	
OCP B7	SLOT_ID				OCP A7	RBT_TX_EN		
OCP B8	RBT_RXD1				OCP A8	RBT_TXD1		
OCP B9	RBT_RXD0				OCP A9	RBT_TXD0		
OCP B10	GND	🟩			OCP A10	GND	🟩	
OCP B11	REFCLKn2				OCP A11	REFCLKn3		

Commented [CP14]: Not sure why only the GND pins do the 1st mate while all other pins do 2nd? Do not see PRSNT pins act as the last mate pins. Is this still work-in-progress?

Commented [NT15R14]: Waiting on HPe recommendation for electrical or mechanical protection methods to prevent damage to the card.

The OCP Subgroup decided to keep the same 1st and 2nd mate gold finger lengths per the SFF-TA-1002 recommendations.

OCP B12	REFCLKp2		OCP A12	REFCLKp3	
OCP B13	GND		OCP A13	GND	
OCP B14	RBT_CRS_DV		OCP A14	RBT_CLK_IN	
Mechanical Key					
B1	+12V_EDGE		A1	GND	
B2	+12V_EDGE		A2	GND	
B3	+12V_EDGE		A3	GND	
B4	+12V_EDGE		A4	GND	
B5	+12V_EDGE		A5	GND	
B6	+12V_EDGE		A6	GND	
B7	BIF0#		A7	SMCLK	
B8	BIF1#		A8	SMDAT	
B9	BIF2#		A9	SMRST#	
B10	PERST0#		A10	PRSNTA#	
B11	+3.3V_EDGE		A11	PERST1#	
B12	~~PWRDIS~~PWR_EN		A12	PRSNTB2#	
B13	GND		A13	GND	
B14	REFCLKn0		A14	REFCLKn1	
B15	REFCLKp0		A15	REFCLKp1	
B16	GND		A16	GND	
B17	PETn0		A17	PERn0	
B18	PETp0		A18	PERp0	
B19	GND		A19	GND	
B20	PETn1		A20	PERn1	
B21	PETp1		A21	PERp1	
B22	GND		A22	GND	
B23	PETn2		A23	PERn2	
B24	PETp2		A24	PERp2	
B25	GND		A25	GND	
B26	PETn3		A26	PERn3	
B27	PETp3		A27	PERp3	
B28	GND		A28	GND	
Mechanical Key					
B29	GND		A29	GND	
B30	PETn4		A30	PERn4	
B31	PETp4		A31	PERp4	
B32	GND		A32	GND	
B33	PETn5		A33	PERn5	
B34	PETp5		A34	PERp5	
B35	GND		A35	GND	
B36	PETn6		A36	PERn6	
B37	PETp6		A37	PERp6	
B38	GND		A38	GND	
B39	PETn7		A39	PERn7	
B40	PETp7		A40	PERp7	
B41	GND		A41	GND	
B42	PRSNTB0#		A42	PRSNTB1#	
Mechanical Key					
B43	GND		A43	GND	
B44	PETn8		A44	PERn8	
B45	PETp8		A45	PERp8	
B46	GND		A46	GND	
B47	PETn9		A47	PERn9	
B48	PETp9		A48	PERp9	
B49	GND		A49	GND	
B50	PETn10		A50	PERn10	
B51	PETp10		A51	PERp10	
B52	GND		A52	GND	
B53	PETn11		A53	PERn11	
B54	PETp11		A54	PERp11	
B55	GND		A55	GND	
B56	PETn12		A56	PERn12	
B57	PETp12		A57	PERp12	
B58	GND		A58	GND	
B59	PETn13		A59	PERn13	
B60	PETp13		A60	PERp13	
B61	GND		A61	GND	
B62	PETn14		A62	PERn14	
B63	PETp14		A63	PERp14	
B64	GND		A64	GND	
B65	PETn15		A65	PERn15	

B66	PETp15		A66	PERp15	
B67	GND		A67	GND	
B68	RFU, N/C		A68	RFU, N/C	
B69	RFU, N/C		A69	RFU, N/C	
B70	PRSNTB3#		A70	RFU, N/C	

3.2 Baseboard Connector Requirements

The OCP NIC 3.0 connectors are compliant to the “4C connector” as defined in the SFF-TA-1002 specification for a right angle or straddle mount form-factor. The 4C connector is 140-pins in width and includes support for up to 32 differential pairs to support a x16 PCIe connection. The connector also provides 6 pins of +12V_EDGE, and 1 pin of +3.3V_EDGE for power. This implementation is common between both the Primary and Secondary Connectors. In addition, the Primary Connector has a 28-pin OCP Bay to the right of pin 1. These pins are used for management and support for up to a 4 x2 and 4 x4 multi-host configuration on the Primary Connector. The Primary and Secondary Connector drawings are shown below.

All diagram units are in mm unless otherwise noted.

3.2.1 Right Angle Connector

Commented [NT16]: All connector drawings + dimensions need to be updated .

The following offset and height options are available for the right angle Primary and Secondary Connectors.

Table 12: Right Angle Connector Options

Name	Pins	Style and Baseboard Thickness	Offset (mm)
Primary Connector – 4C + OCP	168 pins	Right Angle	4mm
Secondary Connector – 4C	140 pins	Right Angle	4mm

Figure 59: 168-pin Base Board Primary Connector – Right Angle

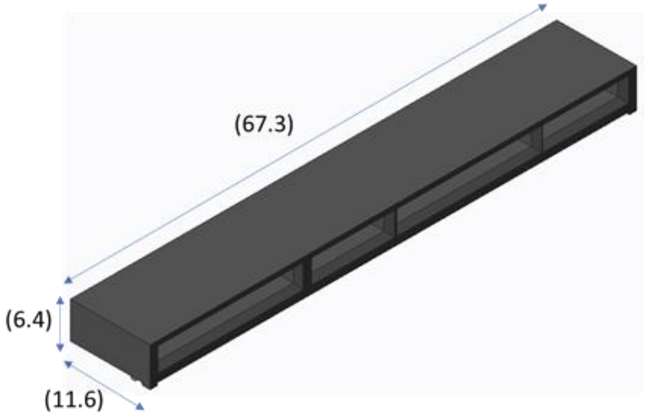
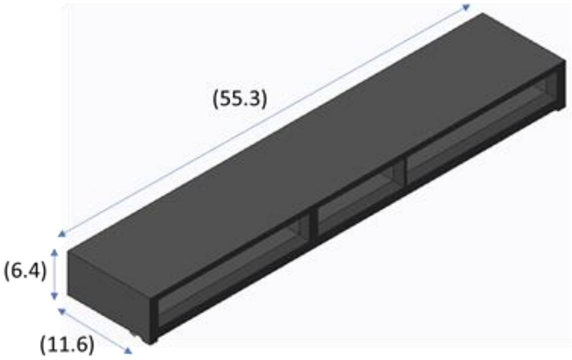


Figure 60: 140-pin Base Board Secondary Connector – Right Angle



3.2.2 Right Angle Offset

The OCP NIC 3.0 right angle connectors have a 4.0mm offset from the baseboard (pending SI simulation results). This is shown in Figure 61.

Figure 61: OCP NIC 3.0 Card and Host Offset for Right Angle Connectors

TBD

3.2.3 Straddle Mount Connector

The following offset and height options are available for the straddle mount Primary and Secondary Connectors.

Table 13: Straddle Mount Connector Options

Name	**Pins**	**Style and Baseboard Thickness**	**Offset (mm)**
Primary Connector – 4C + OCP	168 pins	Straddle Mount for 0.062”	Coplanar (0mm)
Primary Connector – 4C + OCP	168 pins	Straddle Mount for 0.076”	-0.3mm
Primary Connector – 4C + OCP	168 pins	Straddle Mount for 0.093”	Coplanar (0mm)
Secondary Connector – 4C	140 pins	Straddle Mount for 0.062”	Coplanar (0mm)
Secondary Connector – 4C	140 pins	Straddle Mount for 0.076”	-0.3mm
Secondary Connector – 4C	140 pins	Straddle Mount for 0.093”	Coplanar (0mm)

Figure 62: 168-pin Base Board Primary Connector – Straddle Mount

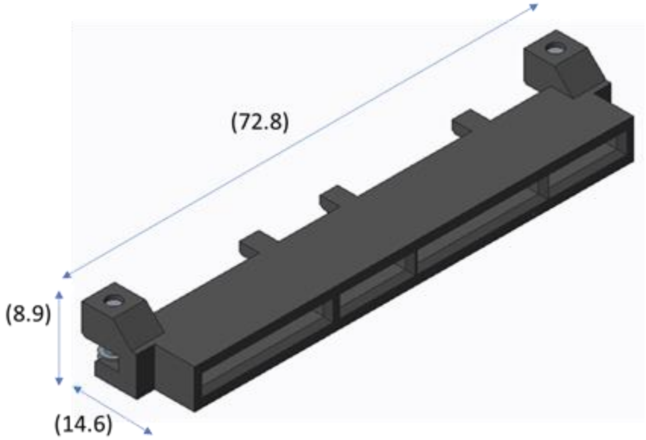
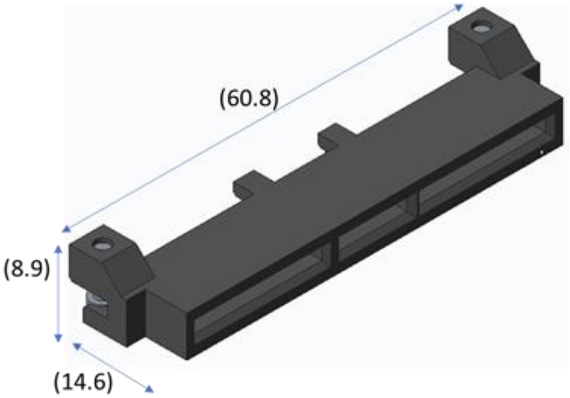


Figure 63: 140-pin Base Board Secondary Connector – Straddle Mount



3.2.4 Straddle Mount Offset and PCB Thickness Options

The OCP NIC 3.0 straddle mount connectors have four baseboard PCB thicknesses they can accept. The available options are shown in Figure 64. The thicknesses are 0.062'', 0.076'', 0.093'', and 0.105''. These PCBs must be controlled to a thickness of ±10%. These are available for both the Primary and Secondary Connector locations. At the time of this writing, the most commonly used part is expected to be the 0.076'' baseboard thickness.

Commented [CP17]: +/-8% for all thickness would have cost impact. Need feedbacks from PCB and connector vendors. May be 8% for thicker (>=0.093) boards and 10% for others?

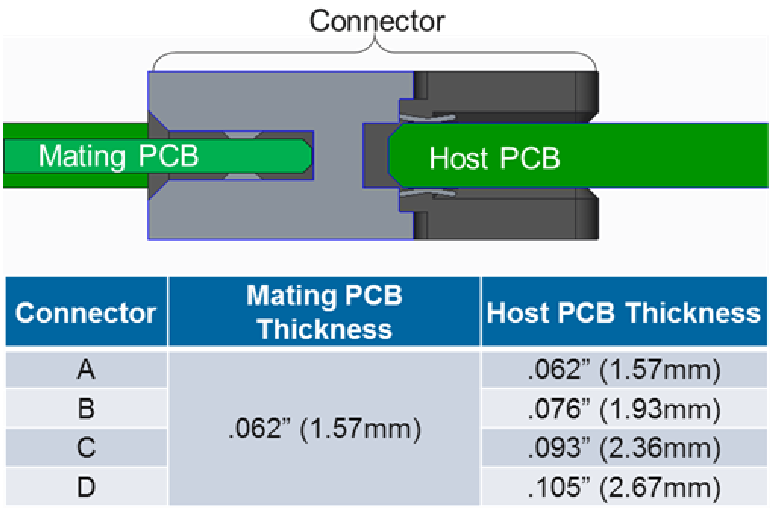
Commented [TN18R17]: Per Josh @ Facebook:

Hi All,

I just happened to have a meeting with TE/David this morning and asked about this. The connector supports +/-8% on the NIC side and +/-10% on the MB side. Looks like we just need to update 3.2.4 accordingly. Did this concern only apply to the MB side? BTW – on the NIC side this tolerance matches PCIE which is obviously do-able.

Thanks
Joshua Held
Mechanical Engineer

Figure 64: OCP NIC 3.0 Card and Baseboard PCB Thickness Options for Straddle Mount Connectors



Connector	Mating PCB Thickness	Host PCB Thickness
A	.062” (1.57mm)	.062” (1.57mm)
B		.076” (1.93mm)
C		.093” (2.36mm)
D		.105” (2.67mm)

The connectors are capable of being used coplanar as shown in Figure 65. Additionally, the connectors are also capable of having a 0.3mm offset from the centerline of the host board as shown in Figure 66.

Figure 65: 0mm Offset (Coplanar) for 0.062” Thick Baseboards

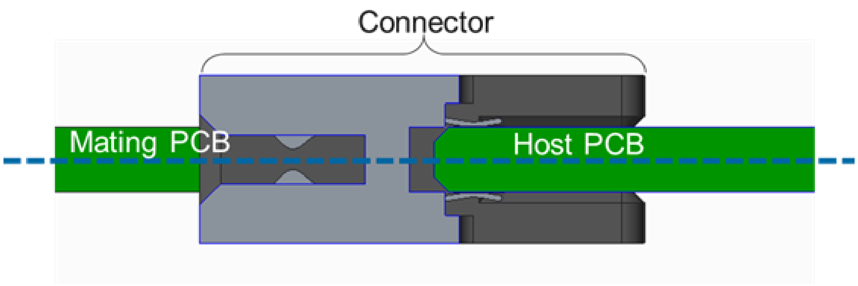
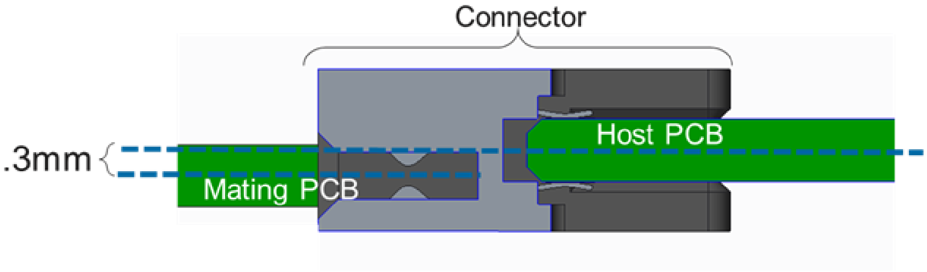


Figure 66: 0.3mm Offset for 0.076” Thick Baseboards



3.2.5 Large Card Connector Locations

In order to the support the large form factor, systems must locate the Primary and Secondary Connectors per the mechanical drawing shown in Figure 67 and Figure 68.

Figure 67: Primary and Secondary Connector Locations for Large Card Support with Right Angle Connectors

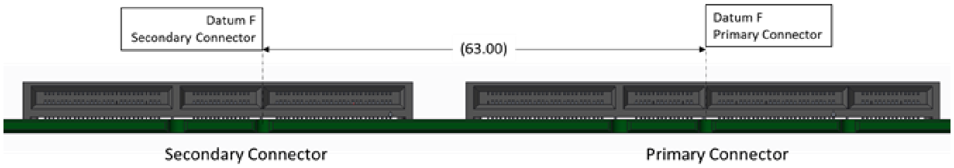
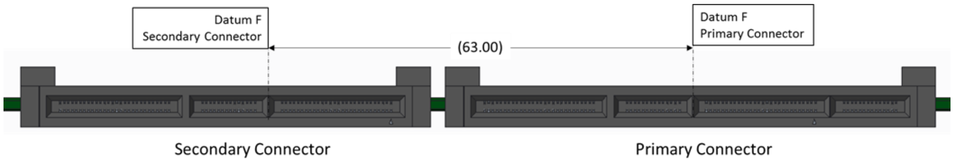


Figure 68: Primary and Secondary Connector Locations for Large Card Support with Straddle Mount Connectors



3.3 Pin definition

The pin definitions of an OCP NIC 3.0 card with up to a x32 PCIe interface are shown in Table 14 and Table 15. All signal directions are shown from the perspective of the baseboard.

A baseboard system may provide a combination of Primary Connectors only, or Primary and Secondary Connectors to support multiple sizes of OCP NIC 3.0 cards. Both connectors share common functionality with power, SMBus 2.0, x16 PCIe and bifurcation control. The Primary Connector has an additional OCP Bay (pins OCP_A[1:14], OCP_B[1:14]) with additional REFCLKs for supporting up to four PCIe hosts, NC-SI over RBT connectivity and a Scan Chain for information exchange between the host and card. The NIC is required to implement the Scan Chain, while the baseboard may choose to optionally implement it.

Depending on the baseboard form-factor, multiple OCP NIC 3.0 compliant cards may be designed into the system.

The pins common to the Primary and Secondary Connectors are shown in Section 3.4. The OCP Bay pins on the Primary Connector only are shown in Section 3.5.

Cards or systems that do not require the use of a PCIe x16 connection may optionally implement a subset electrical connections as applicable to the design. For example, a x8 (or smaller) card using the first 8 PCIe lanes that is compliant with the Primary Connector pinout. Refer to Sections 3.1 and 3.2 for mechanical details. For these cases, the Primary Connector matches the 2C dimensions as defined in SFF-TA-1002.

In all cases, the physical baseboard connectors shall support x16 PCIe widths and must be implemented with the Primary (4C + OCP Bay) and Secondary (4C) connectors.

Table 14: Primary Connector Pin Definition (x16) (4C + OCP Bay)

Side B		Side A			
OCP_B1	NIC_PWR_GOOD	PERST2#	OCP_A1	**Primary Connector (x16, 168-pin OCP NIC 3.0 card with OCP Bay)**	**Primary Connector (x8, 112-pin OCP NIC 3.0 card with OCP bay)**
OCP_B2	PWRBRK#	PERST3#	OCP_A2		
OCP_B3	LD#	WAKE#	OCP_A3		
OCP_B4	DATA_IN	RBT_ARB_IN	OCP_A4		
OCP_B5	DATA_OUT	RBT_ARB_OUT	OCP_A5		
OCP_B6	CLK	GND	OCP_A6		
OCP_B7	SLOT_ID	RBT_TX_EN	OCP_A7		
OCP_B8	RBT_RXD1	RBT_TXD1	OCP_A8		
OCP_B9	RBT_RXD0	RBT_TXD0	OCP_A9		
OCP_B10	GND	GND	OCP_A10		
OCP_B11	REFCLKn2	REFCLKn3	OCP_A11		
OCP_B12	REFCLKp2	REFCLKp3	OCP_A12		
OCP_B13	GND	GND	OCP_A13		
OCP_B14	RBT_CRS_DV	RBT_CLK_IN	OCP_A14		
Mechanical Key					
B1	+12V_EDGE	GND	A1		
B2	+12V_EDGE	GND	A2		
B3	+12V_EDGE	GND	A3		
B4	+12V_EDGE	GND	A4		
B5	+12V_EDGE	GND	A5		
B6	+12V_EDGE	GND	A6		
B7	BIF0#	SMCLK	A7		
B8	BIF1#	SMDAT	A8		
B9	BIF2#	SMRST#	A9		
B10	PERST0#	PRSNTA#	A10		
B11	+3.3V_EDGE	PERST1#	A11		
B12	~~PWRDIS~~PWR_EN	PRSNTB2#	A12		
B13	GND	GND	A13		
B14	REFCLKn0	REFCLKn1	A14		
B15	REFCLKp0	REFCLKp1	A15		
B16	GND	GND	A16		
B17	PETn0	PERn0	A17		
B18	PETp0	PERp0	A18		
B19	GND	GND	A19		
B20	PETn1	PERn1	A20		
B21	PETp1	PERp1	A21		

B22	GND	GND	A22
B23	PETn2	PERn2	A23
B24	PETp2	PERp2	A24
B25	GND	GND	A25
B26	PETn3	PERn3	A26
B27	PETp3	PERp3	A27
B28	GND	GND	A28
Mechanical Key			
B29	GND	GND	A29
B30	PETn4	PERn4	A30
B31	PETp4	PERp4	A31
B32	GND	GND	A32
B33	PETn5	PERn5	A33
B34	PETp5	PERp5	A34
B35	GND	GND	A35
B36	PETn6	PERn6	A36
B37	PETp6	PERp6	A37
B38	GND	GND	A38
B39	PETn7	PERn7	A39
B40	PETp7	PERp7	A40
B41	GND	GND	A41
B42	PRSNTB0#	PRSNTB1#	A42
Mechanical Key			
B43	GND	GND	A43
B44	PETn8	PERn8	A44
B45	PETp8	PERp8	A45
B46	GND	GND	A46
B47	PETn9	PERn9	A47
B48	PETp9	PERp9	A48
B49	GND	GND	A49
B50	PETn10	PERn10	A50
B51	PETp10	PERp10	A51
B52	GND	GND	A52
B53	PETn11	PERn11	A53
B54	PETp11	PERp11	A54
B55	GND	GND	A55
B56	PETn12	PERn12	A56
B57	PETp12	PERp12	A57
B58	GND	GND	A58
B59	PETn13	PERn13	A59
B60	PETp13	PERp13	A60
B61	GND	GND	A61
B62	PETn14	PERn14	A62
B63	PETp14	PERp14	A63
B64	GND	GND	A64
B65	PETn15	PERn15	A65
B66	PETp15	PERp15	A66
B67	GND	GND	A67
B68	RFU, N/C	RFU, N/C	A68
B69	RFU, N/C	RFU, N/C	A69
B70	PRSNTB3#	RFU, N/C	A70

Table 15: Secondary Connector Pin Definition (x16) (4C)

Side B		**Side A**		
B1	+12V_EDGE	GND	A1	**Secondary Connector (x16, 140-pin OCP NIC 3.0 card)**
B2	+12V_EDGE	GND	A2	
B3	+12V_EDGE	GND	A3	
B4	+12V_EDGE	GND	A4	
B5	+12V_EDGE	GND	A5	
B6	+12V_EDGE	GND	A6	
B7	BIF0#	SMCLK	A7	
B8	BIF1#	SMDAT	A8	
B9	BIF2#	SMRST#	A9	
B10	PERST0#	PRSNTA#	A10	
B11	+3.3V_EDGE	PERST1#	A11	
B12	~~PWRDIS~~PWR_EN	PRSNTB2#	A12	
B13	GND	GND	A13	
B14	REFCLKn0	REFCLKn1	A14	
B15	REFCLKp0	REFCLKp1	A15	
B16	GND	GND	A16	
B17	PETn0	PERn0	A17	
B18	PETp0	PERp0	A18	
B19	GND	GND	A19	
B20	PETn1	PERn1	A20	
B21	PETp1	PERp1	A21	
B22	GND	GND	A22	
B23	PETn2	PERn2	A23	
B24	PETp2	PERp2	A24	
B25	GND	GND	A25	
B26	PETn3	PERn3	A26	
B27	PETp3	PERp3	A27	
B28	GND	GND	A28	
Mechanical Key				
B29	GND	GND	A29	
B30	PETn4	PERn4	A30	
B31	PETp4	PERp4	A31	
B32	GND	GND	A32	
B33	PETn5	PERn5	A33	
B34	PETp5	PERp5	A34	
B35	GND	GND	A35	
B36	PETn6	PERn6	A36	
B37	PETp6	PERp6	A37	
B38	GND	GND	A38	
B39	PETn7	PERn7	A39	
B40	PETp7	PERp7	A40	
B41	GND	GND	A41	
B42	PRSNTB0#	PRSNTB1#	A42	
Mechanical Key				
B43	GND	GND	A43	
B44	PETn8	PERn8	A44	
B45	PETp8	PERp8	A45	
B46	GND	GND	A46	
B47	PETn9	PERn9	A47	
B48	PETp9	PERp9	A48	
B49	GND	GND	A49	
B50	PETn10	PERn10	A50	
B51	PETp10	PERp10	A51	

B52	GND	GND	A52	
B53	PETn11	PERn11	A53	
B54	PETp11	PERp11	A54	
B55	GND	GND	A55	
B56	PETn12	PERn12	A56	
B57	PETp12	PERp12	A57	
B58	GND	GND	A58	
B59	PETn13	PERn13	A59	
B60	PETp13	PERp13	A60	
B61	GND	GND	A61	
B62	PETn14	PERn14	A62	
B63	PETp14	PERp14	A63	
B64	GND	GND	A64	
B65	PETn15	PERn15	A65	
B66	PETp15	PERp15	A66	
B67	GND	GND	A67	
B68	RFU, N/C	RFU, N/C	A68	
B69	RFU, N/C	RFU, N/C	A69	
B70	PRSNTB3#	RFU, N/C	A70	

3.4 Signal Descriptions – Common

The pins shown in this section are common to both the Primary and Secondary Connectors. All pin directions are from the perspective of the baseboard.

The OCP NIC 3.0 card shall implement protection methods to prevent leakage paths between the Vaux and Vmain power domains in the event that a NIC is powered down in a powered up baseboard.

Note: Pins that are only used on Primary Connector 28-pin OCP bay are defined in Section 3.5.

3.4.1 PCIe Interface Pins

This section provides the pin assignments for the PCIe interface signals. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0. Example connection diagrams for are shown in Figure 82.

Table 16: Pin Descriptions – PCIe 1

Signal Name	Pin #	Baseboard Direction	Signal Description
REFCLKn0 REFCLKp0	B14 B15	Output	PCIe compliant differential reference clock #0, and #1. 100MHz reference clocks are used for the OCP NIC 3.0 card PCIe core logic. For baseboards, the REFCLK0 and REFCLK1 signals shall be available at the connector. Baseboards should disable REFCLK1 if it is not used by the OCP NIC 3.0 card. For OCP NIC 3.0 cards, the required REFCLKs shall be connected per the endpoint datasheet. Unused REFCLKs on the OCP NIC 3.0 card shall be left as a no connect.
REFCLKn1 REFCLKp1	A14 A15	Output	

			Note: For cards that only support 1 x16, REFCLK0 is used. For cards that support 2 x8, REFCLK0 is used for the first eight PCIe lanes, and REFCLK1 is used for the second eight PCIe lanes. REFCLK0 is always available to all OCP NIC 3.0 cards. The card should not assume REFCLK1 is available until the bifurcation negotiation process is completed. Refer to Section 2.1 in the PCIe CEM Specification, Rev 4.0 for electrical details.
PETn0 PETp0	B17 B18	Output	Transmitter differential pairs [0:15]. These pins are connected from the baseboard transmitter differential pairs to the receiver differential pairs on the OCP NIC 3.0 card. The PCIe transmit pins shall be AC coupled on the baseboard with capacitors. The AC coupling capacitor value shall use the C_{TX} parameter value specified in the PCIe Base Specification. For baseboards, the PET[0:15] signals are required at the connector. For OCP NIC 3.0 cards, the required PET[0:15] signals shall be connected to the endpoint silicon. For silicon that uses less than a x16 connection, the appropriate PET[0:15] signals shall be connected per the endpoint datasheet. Refer to Section 6.1 in the PCIe CEM Specification, Rev 4.0 for details.
PETn1 PETp1	B20 B21	Output	
PETn2 PETp2	B23 B24	Output	
PETn3 PETp3	B26 B27	Output	
PETn4 PETp4	B30 B31	Output	
PETn5 PETp5	B33 B34	Output	
PETn6 PETp6	B36 B37	Output	
PETn7 PETp7	B39 B40	Output	
PETn8 PETp8	B44 B45	Output	
PETn9 PETp9	B47 B48	Output	
PETn10 PETp10	B50 B51	Output	
PETn11 PETp11	B53 B54	Output	
PETn12 PETp12	B56 B57	Output	
PETn13 PETp13	B59 B60	Output	
PETn14 PETp14	B62 B63	Output	
PETn15 PETp15	B65 B66	Output	
PERn0 PERp0	A17 A18	Input	Receiver differential pairs [0:15]. These pins are connected from the OCP NIC 3.0 card transmitter
PERn1	A20	Input	

Commented [CP19]: REFCLK0 is available all the time while add-in card should not assume REFCLK1 is avail until bifurcation negotiation is completed. Minimize clock distribution for single host application.

PERp1	A21		differential pairs to the receiver differential pairs on the baseboard. The PCIe receive pins shall be AC coupled on the OCP NIC 3.0 card with capacitors. The AC coupling capacitor value shall use the C_{TX} parameter value specified in the PCIe Base Specification . For baseboards, the PER[0:15] signals are required at the connector. For OCP NIC 3.0 cards, the required PER[0:15] signals shall be connected to the endpoint silicon. For silicon that uses less than a x16 connection, the appropriate PER[0:15] signals shall be connected per the endpoint datasheet. Refer to Section 6.1 in the PCIe CEM Specification, Rev 4.0 for details.
PERn2 PERp2	A23 A24	Input	
PERn3 PERp3	A26 A27	Input	
PERn4 PERp4	A30 A31	Input	
PERn5 PERp5	A33 A34	Input	
PERn6 PERp6	A36 A37	Input	
PERn7 PERp7	A39 A40	Input	
PERn8 PERp8	A44 A45	Input	
PERn9 PERp9	A47 A48	Input	
PERn10 PERp10	A50 A51	Input	
PERn11 PERp11	A53 A54	Input	
PERn12 PERp12	A56 A57	Input	
PERn13 PERp13	A59 A60	Input	
PERn14 PERp14	A62 A63	Input	
PERn15 PERp15	A65 A66	Input	
PERST0# PERST1#	B10 A11	Output	PCIe Reset #0, #1. Active low. When PERSTn# is deasserted, the signal shall indicate the applied power is within tolerance and stable for the OCP NIC 3.0 card. PERST# shall be deasserted at least 100ms after the power rails are within the operating limits per the PCIe CEM Specification. The PCIe REFCLKs shall also become stable within this period of time. PERST shall be pulled high to +3.3V_EDGE on the baseboard. For OCP NIC 3.0, PERST deassertion shall also indicate the full card power envelope is available to the OCP NIC 3.0 card.

			For baseboards, the PERST[0:1]# signals are required at the connector. For OCP NIC 3.0 cards, the required PERST[0:1]# signals shall be connected to the endpoint silicon. Unused PERST[0:1]# signals shall be left as a no connect. **Note:** For cards that only support 1 x16, PERST0# is used. For cards that support 2 x8, PERST0# is used for the first eight PCIe lanes, and PERST1# is used for the second eight PCIe lanes. PERST0# is always available to all OCP NIC 3.0 cards. The card should not assume PERST1# is available until the bifurcation negotiation process is completed. Refer to Section 2.2 in the PCIe CEM Specification, Rev 4.0 for details.

Commented [CP20]: PERST0# is always avail while add-in card should not assume PERST1# is avail until bifurcation negotiation is completed

3.4.2 PCIe Present and Bifurcation Control Pins

This section provides the pin assignments for the PCIe present and bifurcation control signals. The AC/DC specifications are defined in Section 3.12. An example connection diagram is shown in Figure 69.

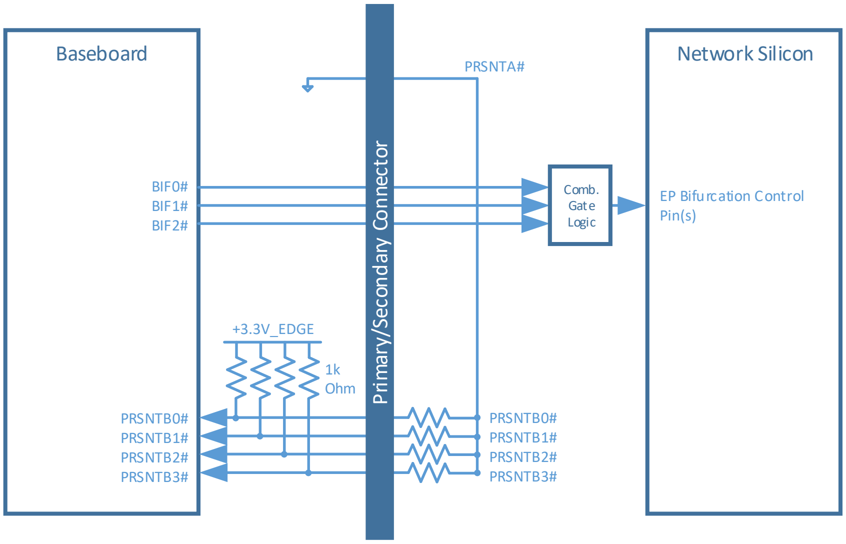
The PRSNTA#/PRSNTB[0:3]# state shall be used to determine if a card has been physically plugged in. The BIF[0:2]# pins shall be latched before ~~PWRDIS~~ PWR_EN ~~de~~assertion to ensure the correct values are detected by the system. Changing the pin states after this timing window is not allowed. Refer to the AC timing diagram in Section 3.12 for details.

Table 17: Pin Descriptions – PCIe Present and Bifurcation Control Pins

Signal Name	Pin #	Baseboard Direction	Signal Description
PRSNTA#	A10	Output	Present A is used for OCP NIC 3.0 card presence and PCIe capabilities detection. For baseboards, this pin shall be directly connected to GND. For OCP NIC 3.0 cards, this pin shall be directly connected to the PRSNTB[3:0]# pins.
PRSNTB0# PRSNTB1# PRSNTB2# PRSNTB3#	B42 A42 A12 B70	Input	Present B [0:3]# are used for OCP NIC 3.0 card presence and PCIe capabilities detection.

			For baseboards, these pins shall be connected to the I/O hub and pulled up to +3.3V_EDGE using 1kOhm resistors. For OCP NIC 3.0 cards, these pins shall be strapped to PRSNTA# per the encoding definitions described in Section 3.6. Note: PRSNTB3# is located at the bottom of the 4C connector and is only applicable for OCP NIC 3.0 cards with a PCIe width of x16 (or greater). OCP NIC 3.0 cards that implement a 2C card edge do not use the PRSNTB3# pin for capabilities or present detection.
BIF0# BIF1# BIF2#	B7 B8 B9	Output	Bifurcation [0:2]# pins allow the baseboard to force configure the OCP NIC 3.0 card bifurcation. For baseboards, these pins shall be outputs driven from the baseboard I/O hub and allow the system to force configure the OCP NIC 3.0 card bifurcation. The baseboard may optionally tie the BIF[0:2]# signals to +3.3V_EDGE or to ground per the definitions are described in Section 3.6 if no dynamic bifurcation configuration is required. For OCP NIC 3.0 cards, these signals shall connect to the endpoint bifurcation pins if it is supported. Note: the required combinatorial logic output for endpoint bifurcation is dependent on the specific silicon and is not defined in this specification.

Figure 69: PCIe Present and Bifurcation Control Pins


Baseboard
Primary/Secondary Connector
Network Silicon
PRSNTA#
BIF0#
BIF1#
BIF2#
Comb. Gate Logic
EP Bifurcation Control Pin(s)
+3.3V_EDGE
1k Ohm
PRSNTB0#
PRSNTB1#
PRSNTB2#
PRSNTB3#
PRSNTB0#
PRSNTB1#
PRSNTB2#
PRSNTB3#

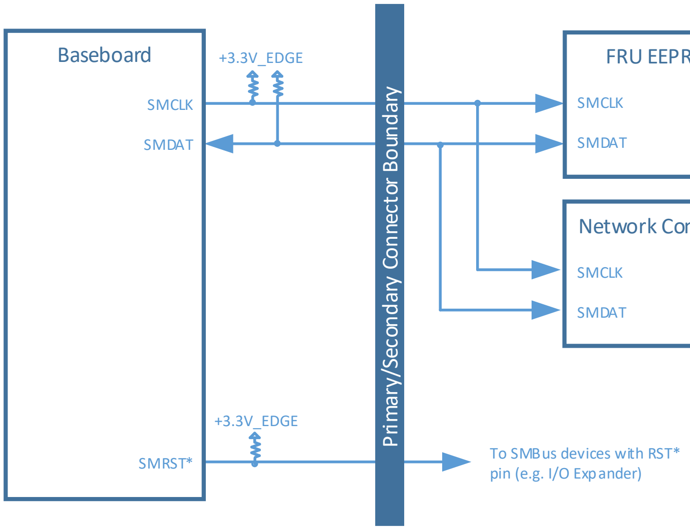
3.4.3 SMBus Interface Pins

This section provides the pin assignments for the SMBus interface signals. The AC/DC specifications are defined in the SMBus 2.0 and I^{2}C bus specifications. An example connection diagram is shown in Figure 70.

Table 18: Pin Descriptions – SMBus

Signal Name	**Pin #**	**Baseboard Direction**	**Signal Description**
SMCLK	A7	Output, OD	SMBus clock. Open drain, pulled up to +3.3V_EDGE on the baseboard. For baseboards, the SMCLK from the platform SMBus master shall be connected to the connector. For OCP NIC 3.0 cards, the SMCLK from the endpoint silicon shall be connected to the card edge gold fingers.
SMDAT	A8	Input / Output, OD	SMBus Data. Open drain, pulled up to +3.3V_EDGE on the baseboard. For baseboards, the SMDAT from the platform SMBus master shall be connected to the connector. For OCP NIC 3.0 cards, the SMDAT from the endpoint silicon shall be connected to the card edge gold fingers.
SMRST#	A9	Output, OD	SMBus reset. Open drain. For baseboards, this pin shall be pulled up to +3.3V_EDGE. The SMRST pin may be used to reset optional downstream SMBus devices (such as temperature sensors). The SMRST# implementation shall be mandatory for baseboard implementations. For OCP NIC 3.0 cards, SMRST# is optional and is dependent on the OCP NIC 3.0 card implementation. The SMRST# signal shall be left as a no connect if it is not used on the OCP NIC 3.0 card.

Figure 70: Example SMBus Connections



3.4.4 Power Supply Pins

This section provides the pin assignments for the power supply interface signals. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0 and amended in Section 3.10. An example connection diagram is shown in Figure 71.

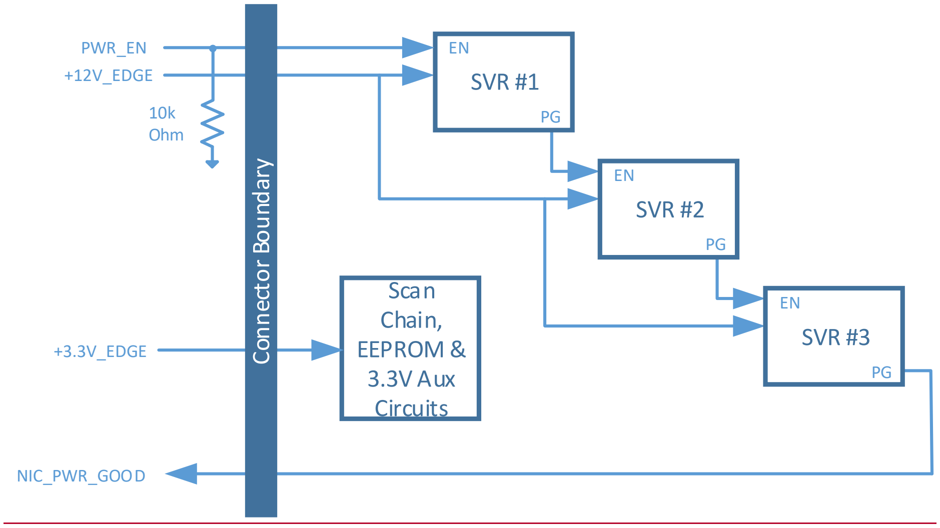
Table 19: Pin Descriptions – Power

Signal Name	**Pin #**	**Baseboard Direction**	**Signal Description**
GND	Various	GND	Ground return; a total of 46 ground pins are on the main 140-pin connector area. Refer to Section 3.3 for details.
+12V_EDGE	B1, B2, B3, B4, B5, B6	Power	+12V main or +12V aux power; total of 6 pins per connector. The +12V_EDGE pins shall be rated to 1.1A per pin with a maximum derated power delivery of 80W. The +12V_EDGE power pins shall be within the rail tolerances as defined in Section 3.10 when the ~~PWRDIS~~ PWR_EN pin is driven ~~low~~ high by the baseboard.
+3.3V_EDGE	B11	Power	+3.3V main or +3.3V aux power; total of 1 pin per connector. The +3.3V_EDGE pin shall be rated to 1.1A for a maximum derated power delivery of 3.63W.

			The +3.3V_EDGE power pin shall be within the rail tolerances as defined in Section 3.10 when the ~~PWRDIS~~ PWR_EN pin is driven ~~low~~ high by the baseboard.
~~PWRDIS~~PWR_EN	B12	Output~~, O/D~~	Power ~~disable~~enable. Active high.~~ Open-drain.~~ This signal shall be pulled ~~up~~ down to ~~+3.3V_EDGE~~ GND through a 10kOhm resistor on the baseboard. This ensures the OCP NIC 3.0 card power is disabled until instructed to turn on by the baseboard. When ~~high~~low, ~~all~~ the OCP NIC 3.0 card supplies shall be disabled. When ~~low~~high, the OCP NIC 3.0 card supplies shall be enabled.

Commented [TN21]: Change PWRDIS to PWR_EN global replace.
Remove inverter.
Edit text regarding polarity to match.

Figure 71: Example Power Supply Topology



3.4.5 Miscellaneous Pins

This section provides the pin assignments for the miscellaneous interface signals.

Table 20: Pin Descriptions – Miscellaneous 1

Signal Name	Pin #	Baseboard Direction	Signal Description
RFU, N/C	B68, B69, A68, A69, A70	Input / Output	Reserved future use pins. These pins shall be left as no connect.

3.5 Signal Descriptions – OCP Bay (Primary Connector)

The following section describes the functions in the Primary Connector 28-pin OCP bay. This 28-pin bay is shown in Section 3.3 and have pin numbers designated as OCP_B[1:14], and OCP_A[1:14]. All pin directions on this OCP bay are from the perspective of the baseboard.

The OCP NIC 3.0 card shall implement protection methods to prevent leakage paths between the V_{aux} and V_{main} power domains in the event that a NIC is powered down in a powered up baseboard.

Note: The pins that are common to both the Primary and Secondary Connectors are defined in Section 3.4.

3.5.1 PCIe Interface Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the PCIe interface signals on the Primary Connector OCP bay. The AC/DC specifications are defined in the PCIe CEM Specification. An example connection diagram that shows REFCLK2, REFCLK3, PERST2# and PERST3# is shown in Section 3.7.

Table 21: Pin Descriptions – PCIe 2

Signal Name	Pin #	Baseboard Direction	Signal Description
REFCLKn2 REFCLKp2	OCP_B11 OCP_B12	Output	PCIe compliant differential reference clock #2, and #3. 100MHz reference clocks are used for the OCP NIC 3.0 card PCIe core logic. For baseboards, the REFCLK2 and REFCLK3 signals are required at the Primary Connector. Baseboards may disable REFCLK2 and REFCLK3 if they are not used by the OCP NIC 3.0 card. For OCP NIC 3.0 cards, the required REFCLKs shall be connected per the endpoint datasheet. Unused REFCLKs on the OCP NIC 3.0 card shall be left as a no connect.
REFCLKn3 REFCLKp3	OCP_A11 OCP_A12	Output	

			Note: REFCLK2 and REFCLK3 are not used for cards that only support a 1 x16, 1 x8 or 2 x8 connection. The card should not assume REFCLK2 and REFCLK3 are available until the bifurcation negotiation process is completed. Refer to Section 2.1 in the PCIe CEM Specification, Rev 4.0 for details.
PERST2# PERST3#	OCP_A1 OCP_A2	Output	PCIe Reset #2, #3. Active low. When PERSTn# is deasserted, the signal shall indicate the applied power is within tolerance and stable for the OCP NIC 3.0 card. PERST# shall be deasserted at least 100ms after the power rails are within the operating limits per the PCIe CEM Specification. The PCIe REFCLKs shall also become stable within this period of time. PERST shall be pulled high to +3.3V_EDGE on the baseboard. For OCP NIC 3.0, PERST deassertion shall also indicate the full card power envelope is available to the OCP NIC 3.0 card. For baseboards, the PERST[2:3]# signals are required at the connector. For OCP NIC 3.0 cards, the required PERST[2:3]# signals shall be connected to the endpoint silicon. Unused PERST[2:3]# signals shall be left as a no connect. **Note:** PERST2# and PERST3# are not used for cards that only support a 1 x16 or 2 x8 connection. The card should not assume PERST2# and PERST3# are available until the bifurcation negotiation process is completed. Refer to Section 2.2 in the PCIe CEM Specification, Rev 4.0 for details.
WAKE#	OCP_A3	Input, OD	WAKE#. Open drain. Active low.

Commented [CP22]: Can we make this statement more accurate to cover all of the multi-host cases with >2 hosts?

Commented [CP23]: Can we make this statement more accurate to cover all of the multi-host cases with >2 hosts? And this note should be aligned with REFCLK2/REFCLK3

			This signal shall be driven by the OCP NIC 3.0 card to notify the baseboard to restore PCIe link. For OCP NIC 3.0 cards that support multiple WAKE# signals, their respective WAKE# pins may be tied together as the signal is open-drain to form a wired-OR. For baseboards, this signal shall be pulled up to +3.3V_EDGE on the baseboard with a 10kOhm resistor. This signals shall be connected to the system WAKE# signal. For OCP NIC 3.0 cards, this signal shall be directly connected to the endpoint silicon WAKE# pin(s). This pin shall be left as a no connect if WAKE# is not supported by the silicon. Refer to Section 2.3 in the PCIe CEM Specification, Rev 4.0 for details.

3.5.2 NC-SI Over RBT Interface Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the NC-SI over RBT interface signals on the Primary Connector OCP bay. The AC/DC specifications for NC-SI over RBT are defined in the DMTF DSP0222 NC-SI specification. An example connection diagram is shown in Figure 72.

Table 22: Pin Descriptions – NC-SI Over RBT

Signal Name	**Pin #**	**Baseboard Direction**	**Signal Description**
RBT_REF_CLK	OCP_A14	Output	Reference clock input. Synchronous clock reference for receive, transmit and control interface. The clock shall have a typical frequency of 50MHz. For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the Primary Connector OCP bay. This signal requires a 100kOhm pull down resistor on the baseboard. If the baseboard does not support NC-SI over RBT, then this signal shall be terminated to ground through a 100kOhm pull down resistor. For OCP NIC 3.0 cards, this pin shall be connected between the gold finger to the endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.
RBT_CRS_DV	OCP_B14	Input	Carrier sense/receive data valid. This signal is used to indicate to the baseboard that the carrier sense/receive data is valid. For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull down resistor on the baseboard. If the baseboard does not support NC-SI over RBT, then this signal shall be terminated to ground through a 100kOhm pull down resistor. For OCP NIC 3.0 cards, this pin shall be connected between the gold finger to the endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.
RBT_RXD0 RBT_RXD1	OCP_B9 OCP_B8	Input	Receive data. Data signals from the network controller to the BMC. For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull-up resistor to +3.3V_EDGE on the baseboard. If the

			baseboard does not support NC-SI over RBT, then this signal shall be terminated to +3.3V_EDGE through a 100kOhm pull-up. For OCP NIC 3.0 cards, this pin shall be connected between the gold finger and the RBT_RXD[0:1] pins on endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.
RBT_TX_EN	OCP_A7	Output	Transmit enable. For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull down resistor to ground on the baseboard. If the baseboard does not support NC-SI over RBT, then this signal shall be terminated to ground through a 100kOhm pull down. For OCP NIC 3.0 cards, this pin shall be connected between the gold finger to the endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.
RBT_TXD0 RBT_TXD1	OCP_A9 OCP_A8	Output	Transmit data. Data signals from the BMC to the network controller. For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull-up resistor to +3.3V_EDGE on the baseboard. If the baseboard does not support NC-SI over RBT, then this signal shall be terminated to +3.3V_EDGE through a 100kOhm pull-up. For OCP NIC 3.0 cards, this pin shall be connected between the gold finger to the RBT_TXD[0:1] pins on the endpoint silicon. This pin shall be left as a no connect if NC-SI over RBT is not supported.
RBT_ARB_OUT	OCP_A5	Output	NC-SI hardware arbitration output. This pin shall only be used if the endpoint silicon supports hardware arbitration. This pin shall be connected to the RBT_ARB_IN signal of an adjacent device in the hardware arbitration ring. The baseboard shall implement a multiplexing implementation that directs the RBT_ARB_OUT to the RBT_ARB_IN pin of the next NC-SI over RBT capable device in the ring, or back to the

			RBT_ARB_IN pin of the source device if there is a single device on the ring. For baseboards, this pin shall be connected between the baseboard OCP connector(s) to complete the hardware arbitration ring. If the baseboard does not support NC-SI over RBT, this signal shall be directly connected to the RBT_ARB_IN pin to allow a complete hardware arbitration ring on the OCP NIC 3.0 card. For OCP NIC 3.0 cards, this pin shall be connected from the gold finger to the RBT_ARB_IN pin on the endpoint silicon. This pin shall be directly connected to the card edge RBT_ARB_IN pin if NC-SI is not supported. This allows the hardware arbitration signals to pass through in a multi-Primary Connector baseboard.
RBT_ARB_IN	OCP_A4	Input	NC-SI hardware arbitration input. This pin shall only be used if the endpoint silicon supports hardware arbitration. This pin shall be connected to the RBT_ARB_OUT signal of an adjacent device in the hardware arbitration ring. The baseboard shall implement a multiplexing implementation that directs the RBT_ARB_IN to the RBT_ARB_OUT pin of the next NC-SI over RBT capable device in the ring, or back to the RBT_ARB_OUT pin of the source device if there is a single device on the ring. For baseboards, this pin shall be connected between the baseboard OCP connector(s) to complete the hardware arbitration ring. If the baseboard does not support NC-SI over RBT, this signal shall be directly connected to the RBT_ARB_OUT pin to allow a complete hardware arbitration ring on the OCP NIC 3.0 card. For OCP NIC 3.0 cards, this pin shall be connected between the gold finger to the RBT_ARB_OUT pin on the endpoint silicon. This pin shall be directly connected to the card edge RBT_ARB_OUT pin if NC-SI is not supported. This allows the hardware arbitration signals to pass through in a multi-Primary Connector baseboard.
SLOT_ID	OCP_B7	Output	NC-SI Address pin. This pin shall only be used if the end point silicon supports package identification.

			For baseboards, this pin shall be used to set the slot ID value. This pin shall be directly to GND for SlotID = 0. This pin shall be pulled up to +3.3V_EDGE for SlotID = 1. For OCP NIC 3.0 cards, this pin shall be connected to the endpoint device GPIO associated with the Package ID[1] field. Refer to Section 4.8.1 and the device datasheet for details. For OCP NIC 3.0 cards with multiple endpoint devices, the SLOT_ID pin may be used to configure a different Package ID value so long as the resulting combination does not cause addressing interferences. For endpoint devices without NC-SI over RBT support, this pin shall be left as a no connect on the OCP NIC 3.0 card.

Figure 72: NC-SI Over RBT Connection Example – Single Primary Connector

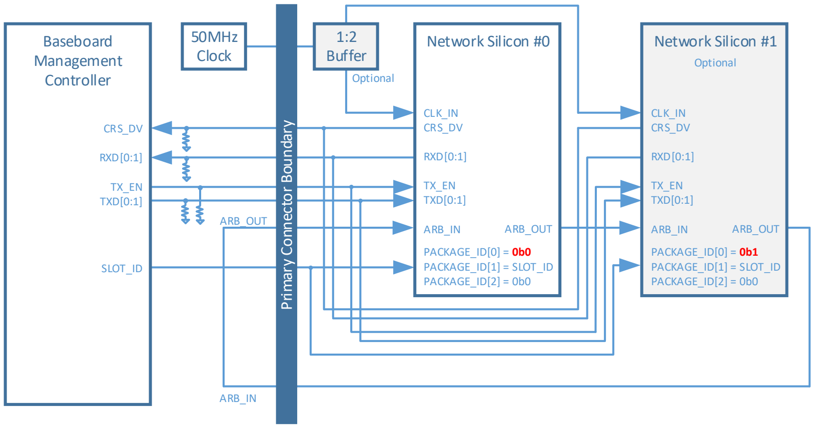
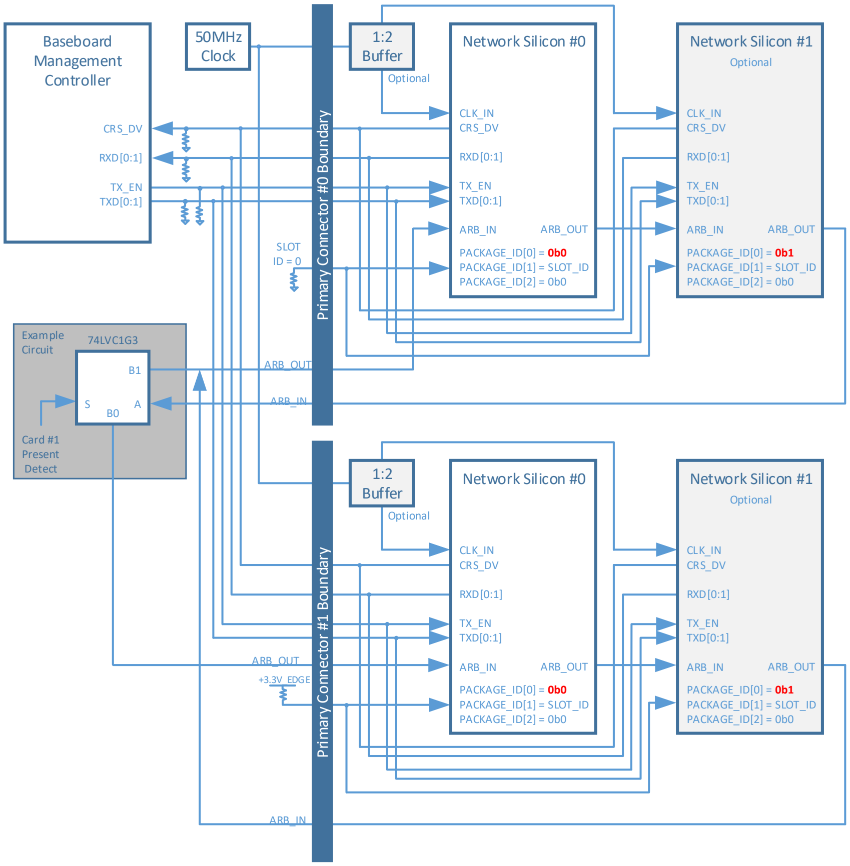


Figure 73: NC-SI Over RBT Connection Example – Dual Primary Connector



Note 1: For baseboard designs with a single Primary Connector, connect ARB_IN to ARB_OUT to complete the NC-SI hardware arbitration ring. For designs with multiple Primary Connectors, connect ARB_IN and ARB_OUT to an analog mux to complete the NC-SI arbitration ring based on the number of cards installed in the system. An example dual Primary Connector implementation is shown in Figure 73.

Note 2: For OCP NIC 3.0 cards with two discrete endpoint silicon, the Package ID[0] bit shall be statically set based on its silicon instance. For example, the figure above shows Network Silicon #0 and Network Silicon #1. Network Silicon #0 has Package ID[0] = 0b0, Network Silicon #1 has Package ID[0] = 0b1.

3.5.3 Scan Chain Pins – OCP Bay (Primary Connector)

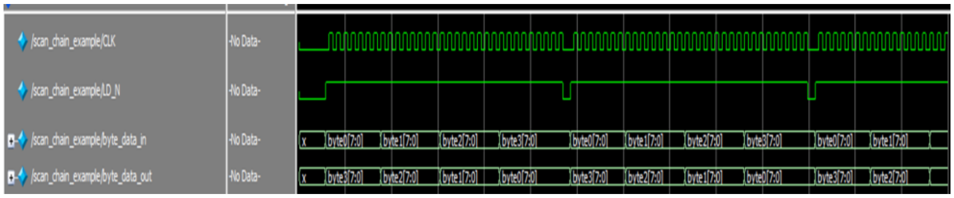
This section provides the pin assignments for the Scan Bus interface signals on the Primary Connector OCP Bay. An example timing diagram is shown in Figure 74. An example connection diagram is shown in Figure 75.

Table 23: Pin Descriptions – Scan Chain

Signal Name	Pin #	Baseboard Direction	Signal Description
CLK	OCP_B6	Output	Scan clock. The CLK is an output pin from the baseboard to the OCP NIC 3.0 card. The CLK may run up to 12.5MHz. For baseboard implementations, the CLK pin shall be connected to the Primary Connector. The CLK pin shall be tied directly to GND if the scan chain is not used. For NIC implementations, the CLK pin shall be connected to Shift Registers 0 & 1, and optionally connected to Shift Registers 2 & 3 (if implemented) as defined in the text and Figure 75, below. The CLK pin shall be pulled up to +3.3V_EDGE through a 1kOhm resistor.
DATA_OUT	OCP_B5	Output	Scan clock data output from the baseboard to the OCP NIC 3.0 card. This bit stream is used to shift in NIC configuration data. For baseboard implementations, the DATA_OUT pin shall be connected to the Primary Connector. The DATA_OUT pin shall be tied directly to GND if the scan chain is not used. For NIC implementations, the DATA_OUT pin may be left floating if it is not used for OCP NIC 3.0 card configuration. The DATA_OUT pin shall be pulled up to +3.3V_EDGE through a 1kOhm resistor.
DATA_IN	OCP_B4	Input	Scan clock data input to the baseboard. This bit stream is used to shift out NIC status bits. For baseboard implementations, the DATA_IN pin shall be pulled up to +3.3V_EDGE through a 10kOhm resistor to prevent the input signal from floating if a card is not installed. This pin may be left as a no connect if the scan chain is not used.

			For NIC implementations, the DATA_IN scan chain is required. The DATA_IN pin shall be connected to Shift Registers 0 & 1, as defined in the text and Figure 75.
LD#	OCP_B3	Output	Scan clock shift register load. Used to latch configuration data on the OCP NIC 3.0 card. For baseboard implementations, the LD# pin shall be pulled up to +3.3V_EDGE through a 1kOhm resistor if the scan chain is not used to prevent the OCP NIC 3.0 card from erroneous data latching. For NIC implementations, the LD# pin implementation is required. The LD# pin shall be connected to Shift Registers 0 & 1 as defined in the text and Figure 75. The LD# pin shall be pulled up to +3.3V_EDGE through a 1kOhm resistor.

Figure 74: Example Scan Chain Timing Diagram



The scan chain provides side band status indication between the OCP NIC 3.0 card and the baseboard. The scan chain bit definition is defined in the two tables below. The scan chain data stream is 32-bits in length for both the DATA_OUT and the DATA_IN streams. The scan chain implementation is optional on the host, but is mandatory on all OCP NIC 3.0 cards. The scan chain components operates on the +3.3V_EDGE power domain.

The DATA_OUT bus is an output from the host. The DATA_OUT bus provides initial configuration options to the OCP NIC 3.0 card. At the time of this writing, the default implementation does not use the DATA_OUT stream and is not implemented on the NIC. However, all baseboard systems that implement the Scan Chain shall connect DATA_OUT between the platform and the Primary Connector for future-proofing NIC implementations and subsequent revisions of this specification.

Table 24: Pin Descriptions – Scan Chain DATA_OUT Bit Definition

Byte.bit	**DATA_OUT Field Name**	**Default Value**	**Description**
0.[0..7]	RSVD	0b000000	Reserved. Byte 0 value is 0h00.
1.[0..7]	RSVD	0h00	Reserved. Byte 1 value is 0h00.
2.[0..7]	RSVD	0h00	Reserved. Byte 2 value is 0h00.
3.[0..7]	RSVD	0h00	Reserved. Byte 3 value is 0h00.

The DATA_IN bus is an input to the host and provides NIC status indication. The default implementation is completed with two 8-bit 74LV165 parallel in to serial out shift registers in a cascaded implementation. Up to four shift registers may be implemented to provide additional NIC status indication to the host platform.

DATA_IN shift registers 0 & 1 shall be mandatory for scan chain implementations. DATA_IN shift registers 2 & 3 are optional depending on the card type and fields being reported to the host. DATA_IN shift register 2 may be used to indicate future definitions of the scan chain bit stream. DATA_IN shift registers 3 (in conjunction with shift register 2) are required for reporting link/activity indication on card implementations with 5-8 ports.

The host should read the DATA_IN bus multiple times to qualify the incoming data stream. The number of data qualification reads is dependent on the baseboard implementation.

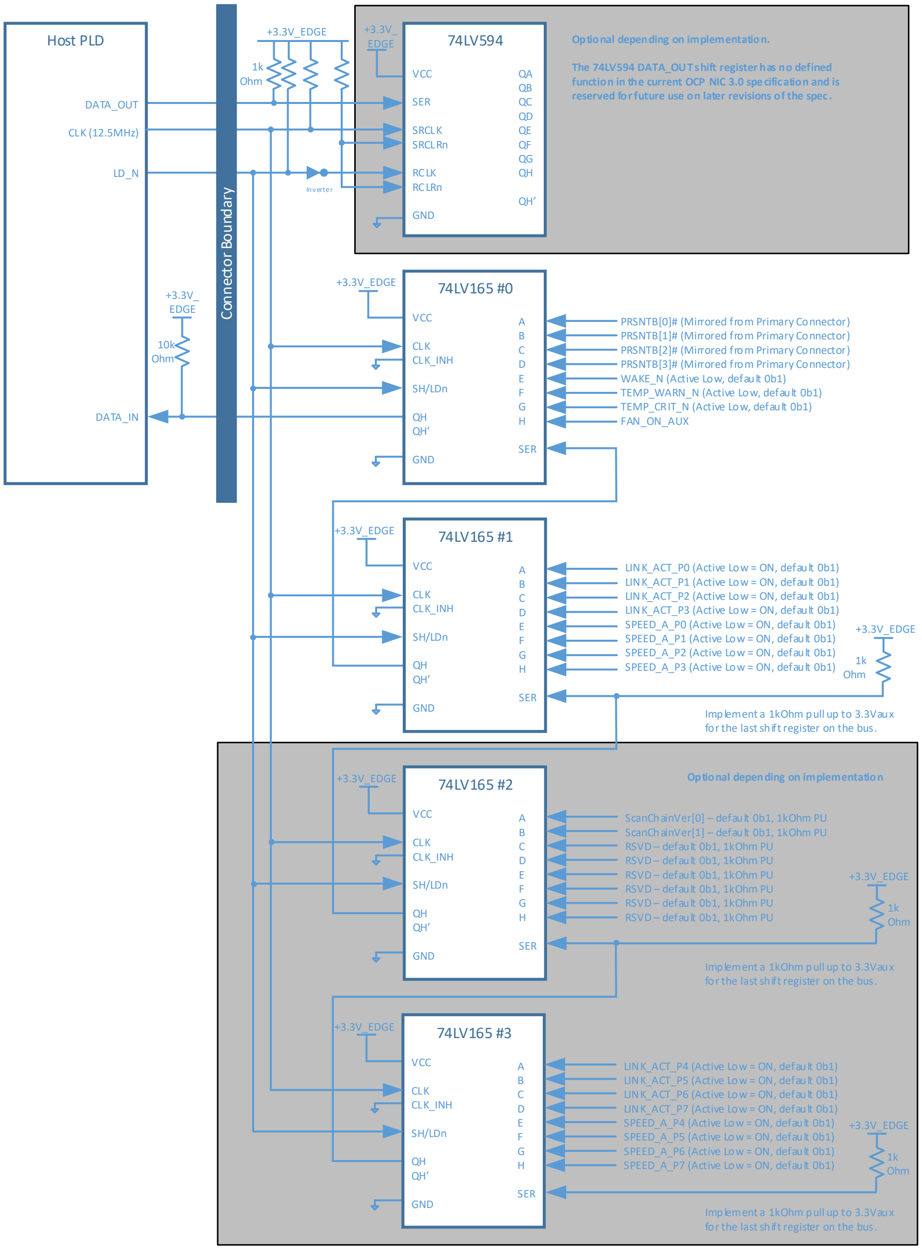
A 1kOhm pull up resistor shall be implemented on the NIC to the SER input of the last shift register on the DATA_IN scan chain to maintain a default bit value of 0b1 for unused bits for implementations using less than four shift registers.

Table 25: Pin Descriptions – Scan Bus DATA_IN Bit Definition

Byte.bit	DATA_OUT Field Name	Default Value	Description
0.0	PRSNTB[0]#	0bX	PRSNTB[3:0]# bits shall reflect the same state as the signals on the Primary Connector.
0.1	PRSNTB[1]#	0bX	
0.2	PRSNTB[2]#	0bX	
0.3	PRSNTB[3]#	0bX	
0.4	WAKE_N	0bX	PCIe WAKE_N signal shall reflect the same state as the signal on the Primary Connector.
0.5	TEMP_WARN_N	0b1	Temperature monitoring pin from the on-card thermal solution. This pin shall be asserted low when temperature sensor exceeds the temperature warning threshold.
0.6	TEMP_CRIT_N	0b1	Temperature monitoring pin from the on-card thermal solution. This pin shall be asserted low when temperature sensor exceeds the temperature critical threshold.
0.7	FAN_ON_AUX	0b0	When high, FAN_ON_AUX shall request the system fan to be enabled for extra cooling in the S5 state.
1.0	LINK_ACT_P0	0b1	Port 0..3 link/activity indication. Active low. 0b0 – Link LED is illuminated on the host platform. 0b1 – Link LED is not illuminated on the host platform. **Steady** = link is detected on the port. **Blinking** = activity is detected on the port. The blink rate should blink low for 50-500ms during activity periods.
1.1	LINK_ACT_P1	0b1	
1.2	LINK_ACT_P2	0b1	
1.3	LINK_ACT_P3	0b1	

			Off = the physical link is down or disabled
1.4	SPEED_A_P0	0b1	Port 0..3 speed A (max rate) indication. Active low. 0b0 – Port is linked at maximum speed. 0b1 – Port is not linked at the maximum speed or no link is present.
1.5	SPEED_A_P1	0b1	
1.6	SPEED_A_P2	0b1	
1.7	SPEED_A_P3	0b1	
2.0	ScanChainVer[0]	0b1	ScanChainVer[1:0] shall be used to indicate the scan chain bit definition version. The encoding shall be as follows: 0b11 – Scan chain bit definition version 1 corresponding to OCP NIC 3.0 version 1.0. All other encoding values shall be reserved.
2.1	ScanChainVer[1]	0b1	
2.2	RSVD	0b1	Byte 2 bits [2:7] are reserved. These bits shall default to the value of 0b1. These bits may be used in future versions of the scan chain.
2.3	RSVD	0b1	
2.4	RSVD	0b1	
2.5	RSVD	0b1	
2.6	RSVD	0b1	
2.7	RSVD	0b1	
3.0	LINK_ACT_P4	0b1	Port 4..7 link/activity indication. Active low. 0b0 – Link LED is illuminated on the host platform. 0b1 – Link LED is not illuminated on the host platform. **Steady** = link is detected on the port. **Blinking** = activity is detected on the port. The blink rate should blink low for 50-500ms during activity periods. **Off** = the physical link is down or disabled
3.1	LINK_ACT_P5	0b1	
3.2	LINK_ACT_P6	0b1	
3.3	LINK_ACT_P7	0b1	
3.4	SPEED_A_P4	0b1	Port 4..7 speed A (max rate) indication. Active low. 0b0 – Port is linked at maximum speed. 0b1 – Port is not linked at the maximum speed or no link is present.
3.5	SPEED_A_P5	0b1	
3.6	SPEED_A_P6	0b1	
3.7	SPEED_A_P7	0b1	

Figure 75: Scan Bus Connection Example



Optional depending on implementation.

The 74LV594 DATA_OUT shift register has no defined function in the current OCP NIC 3.0 specification and is reserved for future use on later revisions of the spec.

Implement a 1kOhm pull up to 3.3Vaux for the last shift register on the bus.

Optional depending on implementation

Implement a 1kOhm pull up to 3.3Vaux for the last shift register on the bus.

Implement a 1kOhm pull up to 3.3Vaux for the last shift register on the bus.

3.5.4 Primary Connector Miscellaneous Pins – OCP Bay (Primary Connector)

This section provides the miscellaneous pin assignments for the pins on the Primary Connector OCP Bay. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0 and Section 3.12. An example PWRBRK# connection is shown in the PCIe CEM Specification. An example NIC_PWR_GOOD connection diagram is shown in Figure 71.

Table 26: Pin Descriptions – Miscellaneous 2

Signal Name	**Pin #**	**Baseboard Direction**	**Signal Description**
PWRBRK#	OCP_B2	Output, OD	Power break. Active low, open drain. This signal shall be pulled up to +3.3V_EDGE on the OCP NIC 3.0 card with a minimum of 95kOhm. The pull up on the baseboard shall be a stiffer resistance in-order to meet the timing specs as shown in the PCIe CEM Specification. When this signal is driven low by the baseboard, the Emergency Power Reduction State is requested. The OCP NIC 3.0 card shall move to a lower power consumption state.
NIC_PWR_GOOD	OCP_B1	Input	NIC Power Good. Active high. This signal is driven by the OCP NIC 3.0 card. When high, this signal shall indicate that all of the OCP NIC 3.0 card power rails are operating within nominal tolerances. When low, this signal shall indicate that the OCP NIC 3.0 card power supplies are not yet within nominal tolerances or are in a fault condition. For baseboards, this pin may be connected to the platform I/O hub as a NIC power health status indication. This signal shall be pulled down to ground with a 100kOhm resistor on the baseboard to prevent a false power good indication if no OCP NIC 3.0 card is present. For OCP NIC 3.0 cards this signal shall indicate the OCP NIC 3.0 card power is “good.”~~.~~ This signal may be implemented by a cascaded power good or a discrete power good monitor output. When high, this signal should be treated as V_{REF} is available for NC-SI communications.

			It is expected that a ~~system~~ baseboard will not drive signals other than SMBus and the Scan Chain when to the OCP NIC 3.0 card this signal is low.
GND	OCP_A6 OCP_A10 OCP_A13 OCP B10 OCP_B13	GND	Ground return; a total of 5 ground pins are on the OCP bay area.

3.6 PCIe Bifurcation Mechanism

OCP NIC 3.0 baseboards and OCP NIC 3.0 cards support multiple bifurcation combinations. Single socket baseboards with a single or multiple root ports, as well as a multi-socket baseboards with a single or multiple root ports are supported. The bifurcation mechanism also supports OCP NIC 3.0 cards with a single or multiple end points. These features are accomplished via I/O pins on the Primary and Secondary Connector:

- PRSNTA#, PRSNTB[3:0]#. The PRSNTA# pin shall connect to the PRSNTB# pins as a hard coded value on the OCP NIC 3.0 card. The encoding of the PRSNTB[3:0]# pins allows the baseboard to determine the PCIe Links available on the OCP NIC 3.0 card.
- BIF[3:0]#. The BIF# pin states shall be controlled by the baseboard to allow the baseboard to override the default end point bifurcation for silicon that support bifurcation. Additional combinatorial logic is required and is specific to the card silicon. The combinatorial logic is not covered in this specification. The BIF[3:0]# pins may optionally be hardcoded for baseboards that do not require a dynamic bifurcation override.

A high level bifurcation connection diagram is shown in Figure 69.

3.6.1 PCIe OCP NIC 3.0 Card to Baseboard Bifurcation Configuration (PRSNTA#, PRSNTB[3:0]#)

The OCP NIC 3.0 card to baseboard configuration mechanism consists of four dual use pins (PRSNTB[3:0]#) on the OCP NIC 3.0 card and a grounded PRSNTA# pin on the baseboard. These pins provide card presence detection as well as mechanism to notify the baseboard of the pre-defined PCIe lane width capabilities. The PRSNTB[3:0]# pins are pulled up to +3.3V_EDGE on the baseboard and are active low signals. A state of 0b1111 indicates that no card is present in the system. Depending on the capabilities of the OCP NIC 3.0 card, a selection of PRSNTB[3:0]# signals may be strapped to the PRSNTA# signal and is pulled low by the baseboard. The encoding of the PRSTNB[3:0]# bits is shown in Table 27 for x16 and x8 PCIe cards.

3.6.2 PCIe Baseboard to OCP NIC 3.0 Card Bifurcation Configuration (BIF[2:0]#)

Three signals (BIF[2:0]#) are driven by the baseboard to notify requested bifurcation on the OCP NIC 3.0 card silicon. This allows the baseboard to set the lane configuration on the OCP NIC 3.0 card that supports multiple bifurcation options.

For example, a baseboard that has four separate hosts that support a 4 x4 connection, should appropriately drive the BIF[2:0]# pins per Table 27 and indicate to the OCP NIC 3.0 card silicon to setup a 4 x4 configuration.

As previously noted, the BIF[2:0]# signals require additional combinatorial logic to decode the BIF[2:0]# value and appropriately apply it to the end-point silicon. The combinatorial logic is not covered in the specification as its implementation is specific to the vendor silicon used.

3.6.3 PCIe Bifurcation Decoder

The combination of the PRSNTB[3:0]# and BIF[2:0]# pins deterministically sets the PCIe lane width for a given combination of baseboard and OCP NIC 3.0 cards. Table 27 shows the resulting number of PCIe links and its width for known combinations of baseboards and OCP NIC 3.0 cards.

***Note:** The baseboard must disable PCIe lanes during the initialization phase if the number of detected PCIe links are greater than what is supported on the baseboard to prevent a nondeterministic solution. For example, if the baseboard only supports a 1 x16 connection, and the OCP NIC 3.0 card only supports a 2 x8 connection, the baseboard must disable PCIe lanes 8-15 to prevent any potential LTSSM issues during the discovery phase.

Table 27: PCIe Bifurcation Decoder for x16 and x8 Card Widths

				Single Host						RSVD	Dual Host	Quad Host	Quad Host
	Network Card – Supported PCIe Configurations		Host	**1 Host**	**1 Host**	**1 Host**	**1 Host**	**1 Host**	**1 Host**	**RSVD**	**2 Hosts**	**4 Hosts**	**4 Hosts**
			Host CPU Sockets	**1 Upstream Socket**	**1 Upstream Socket**	**1 Upstream Socket**	**2 Upstream Sockets**	**4 Upstream Sockets**	**4 Sockets (1 Socket per Host) First 8 PCIe lanes**	RSVD	**2 Upstream Sockets (1 Socket per Host)**	**4 Upstream Sockets (1 Socket per Host)**	**4 Sockets (1 Socket per Host) First 8 PCIe lanes**
			Total PCIe Links	**1 Link (No Bifurcation)**	**1 or 2 Links**	**1, 2, or 4 Links**	**2 Links**	**4 Links**	**4 x2 links**	RSVD	**2 Links**	**4 Links**	**4 x2 links**
			System Support	1x16, 1x8, 1x4, 1x2, 1x1	1x16, 1x8, 1x4, 1x2, 1x1 2x8, 2x4, 2x2, 2x1	1x16, 1x8, 1x4, 1x2, 1x1 2x8, 2x4, 2x2, 2x1 4x4, 4x2, 4x1	1x8, 1x4, 1x2, 1x1 2x8, 2x4, 2x2, 2x1	4x4, 4x2, 4x1	4x2, 4x1	RSVD	2x8, 2x4, 2x2, 2x1	4x4, 4x2, 4x1	4x2, 4x1
Minimum Required Card Edge			System Encoding BIF[2:0]#	0b000	0b000	0b000	0b001	0b010	0b011	0b100	0b101	0b110	0b111
	Card Short Name	**Supported Bifurcation Modes**	**Add-in-Card Encoding** PRSNTB[3:0]#	-	-	-	-	-	-	-	-	-	-
n/a	Not Present	Card Not Present	0b1**111**	RSVD – Card not present in the system									
2C	1x8 Option A	1x8, 1x4, 1x2, 1x1	0b1**110**	1x8	1x8	1x8	1x8 (Socket 0 only)	1x4 (Socket 0 only)	1x2 (Socket 0 only)	-	1x8 (Host 0 only)	1x4 (Host 0 only)	1x2 (Host 0 only)
2C	1x4	1x4, 1x2, 1x1	0b1**110**	1x4	1x4	1x4	1x4 (Socket 0 only)	1x4 (Socket 0 only)	1x2 (Socket 0 only)	-	1x4 (Host 0 only)	1x4 (Host 0 only)	1x2 (Host 0 only)
2C	1x2	1x2, 1x1	0b1**110**	1x2	1x2	1x2	1x2 (Socket 0 only)	1x2 (Socket 0 only)	1x2 (Socket 0 only)	-	1x2 (Host 0 only)	1x2 (Host 0 only)	1x2 (Host 0 only)
2C	1x1	1x1	0b1**110**	1x1	1x1	1x1	1x1 (Socket 0 only)	1x1 (Socket 0 only)	1x1 (Socket 0 only)	-	1x1 (Host 0 only)	1x1 (Host 0 only)	1x1 (Host 0 only)
2C	1x8 Option B	1x8, 1x4, 1x2, 1x1 2x4, 2x2, 2x1	0b1**101**	1x8	1x8	1x8	1x8 (Socket 0 only)	2x4	2x2 (Socket 0 & 2 only)	-	1x8 (Host 0 only)	2x4	2x2 (Host 0 & 2 only)
4C	2x8 Option B	2x8, 2x4, 2x2, 2x1 4x4, 4x2, 4x1	0b1**101**	1x8*	2x8	2x8	2x8	4x4	2x2 (Socket 0 & 2 only)	-	2x8	4x4	2x2 (Host 0 & 2 only)
2C	1x8 Option D	1x8, 1x4 2x4, 4x2 (First 8 lanes), 4x1	0b1**100**	1x8	1x8	1x8	1x8 (Socket 0 only)	2x4	4x2	-	1x8 (Host 0 only)	2x4	4x2
4C	1x16 Option D	1x16, 1x8, 1x4 2x8, 2x4, 4x4, 4x2 (First 8 lanes), 4x1	0b1**100**	1x16	1x16	1x16	2x8	4x4	4x2	-	2x8	4x4	4x2
RSVD	RSVD	RSVD	0b1**011**	RSVD – The encoding of 0b1011 is reserved due to insufficient spacing between PRSNTA and PRSNTB2 pin to provide positive card identification.									
2C	2x4	2x4, 2x2, 2x1 1x4, 1x2, 1x1	0b1**010**	1x4	1x4	2x4	1x4 (Socket 0 only)	2x4	2x2 (Socket 0 & 2 only)	-	1x4 (Host 0 only)	2x4	2x2 (Host 0 & 1 only)
2C	4x2	4x2 (First 8 lanes), 4x1 2x2, 2x1 1x2, 1x1	0b1**001**	1x2	1x2	2x2	1x2 (Socket 0 only)	2x2	4x2	-	1x2 (Host 0 only)	2x2	4x2
RSVD	RSVD	RSVD for future x8 encoding	0b1**000**	-	-	-	-	-	-	-	-	-	-
4C	1x16 Option A	1x16, 1x8, 1x4, 1x2, 1x1	0b0**111**	1x16	1x16	1x16	1x8 (Socket 0 only)	1x4 (Socket 0 only)	1x2 (Socket 0 only)	-	1x8 (Host 0 only)	1x4 (Host 0 only)	1x2 (Host 0 only)
4C	2x8 Option A	2x8, 2x4, 2x2, 2x1	0b0**110**	1x8*	2x8	2x8	2x8	2x4 (Socket 0 & 2 only)	2x2 (Socket 0 & 2 only)	-	2x8	2x4 (Host 0 & 2 only)	1x2 (Host 0 & 1 only)
4C	1x16 Option B	1x16, 1x8, 1x4, 1x2, 1x1 2x8, 2x4, 2x2, 2x1	0b0**101**	1x16	1x16	1x16	2x8	2x4 (Socket 0 & 2 only)	1x2 (Socket 0 only)	-	2x8	2x4 (Host 0 & 2 only)	2x2 (Host 0 & 1 only)
4C	1x16 Option C	1x16, 1x8, 1x4 2x8, 2x4, 2x2, 2x1 4x4, 4x2, 4x1	0b0**100**	1x16	1x16	1x16	2x8	4x4	2x2 (Socket 0 & 2 only)	-	2x8	4x4	2x2 (Host 0 & 1 only)
4C	4x4	4x4, 4x2, 4x1	0b0**011**	1x4*	2x4*	4x4	2x4 (EP 0 and 2 only)	4x4	4x2 (Socket 0 & 2 only)	-	2x4 (EP 0 and 2 only)	4x4	4x2 (Host 0 & 1 only)
RSVD	RSVD	RSVD	0b0**010**	-	-	-	-	-	-	-	-	-	-
RSVD	RSVD	RSVD	0b0**001**	-	-	-	-	-	-	-	-	-	-
RSVD	RSVD	RSVD	0b0**000**	-	-	-	-	-	-	-	-	-	-

Commented [CP24]: Can we make this table more readable? The current format is really hard to read

Commented [NT25R24]: Hi Paul –

Would you please suggest a suitable format?

Commented [NT26R24]: Document editor will investigate other methods to get higher DPI output for this table. (e.g. embedding the spreadsheet in this view)

3.6.4 Bifurcation Detection Flow

The following detection flow shall be used to determine the resulting link count and lane width based on the baseboard and OCP NIC 3.0 card configurations.

1. The baseboard shall read the state of the PRSNTB[3:0]# pins. An OCP NIC 3.0 card is present in the system if the resulting value is not 0b1111.
2. Firmware determines the OCP NIC 3.0 card PCIe lane width capabilities per Table 27 by reading the PRSNTB[3:0]# pins.
3. The baseboard reconfigures the PCIe bifurcation on its ports to match the highest common lane width and lowest common link count on the card.
4. For cases where the baseboard request a link count override (such as requesting a 4-host baseboard requesting 4 x4 operation on a supported card that would otherwise default to a 2 x8 case), the BIF[0:2]# pins shall be asserted as appropriate. Asserting the BIF[0:2]# pins assumes the OCP NIC 3.0 card supports the requested link override.
5. The BIF[0:2]# pins must be in their valid states upon the ~~de~~assertion of ~~PWRDIS~~PWR_EN.
6. ~~PWRDIS~~ PWR_EN is ~~de~~asserted.
7. A OCP NIC 3.0 card is allowed 25ms between ~~PWRDIS~~ PWR_EN ~~de~~assertion and NIC_PWR_GOOD assertion.
8. PERST# shall be deasserted >1s after NIC_PWR_GOOD assertion as defined in Figure 84. Refer to Section 3.12 for timing details.

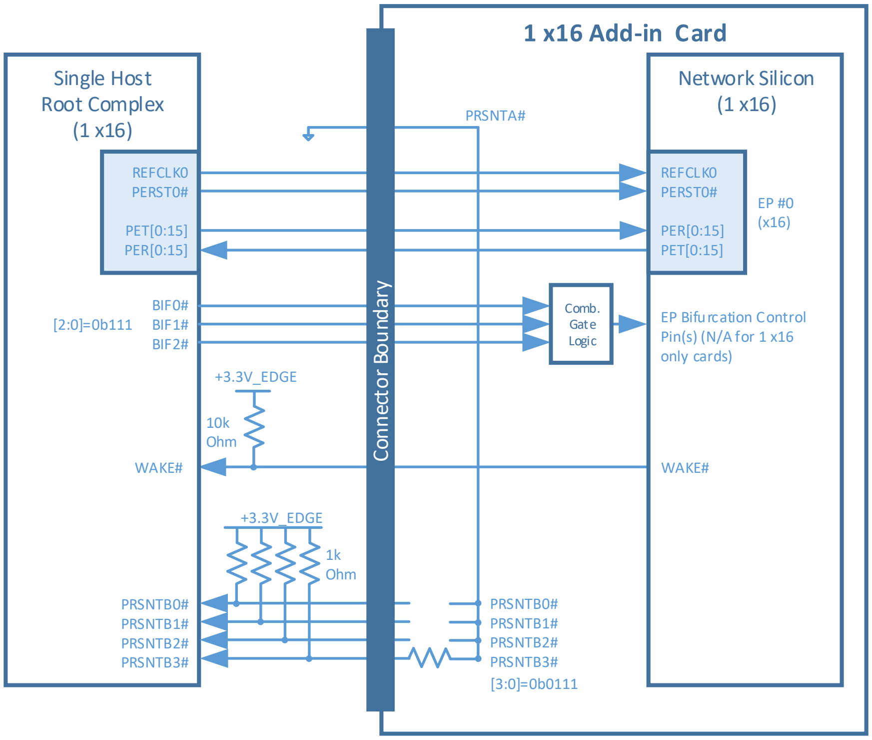
3.6.5 PCIe Bifurcation Examples

For illustrative purposes, the following figures show several common bifurcation permutations.

3.6.5.1 Single Host (1 x16) Baseboard with a 1 x16 OCP NIC 3.0 Card (Single Controller)

Figure 76 illustrates a single host baseboard that supports x16 with a single controller OCP NIC 3.0 card that also supports x16. The PRSTNB[3:0]# state is 0b0111. The BIF[2:0]# state is 0b000 as there is no need to instruct the end-point network controller to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16. The single host baseboard determines that it is also capable of supporting 1 x16. The resulting link width is 1 x16.

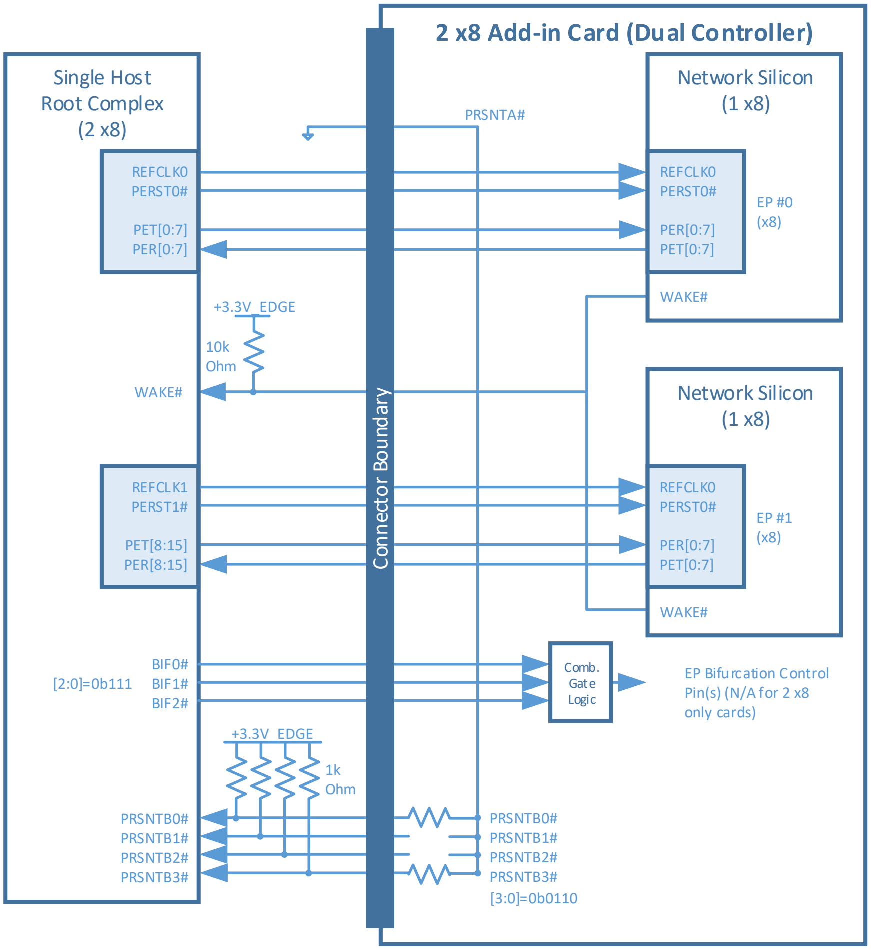
Figure 76: Single Host (1 x16) and 1 x16 OCP NIC 3.0 Card (Single Controller)



3.6.5.2 Single Host (2 x8) Baseboard with a 2 x8 OCP NIC 3.0 Card (Dual Controllers)

Figure 77 illustrates a single host baseboard that supports 2 x8 with a single controller OCP NIC 3.0 card that also supports 2 x8 with dual controllers. The PRSNTB[3:0]# state is 0b0110. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 2 x8. The single host baseboard determines that it is also capable of supporting 2 x8. The resulting link width is 2 x8.

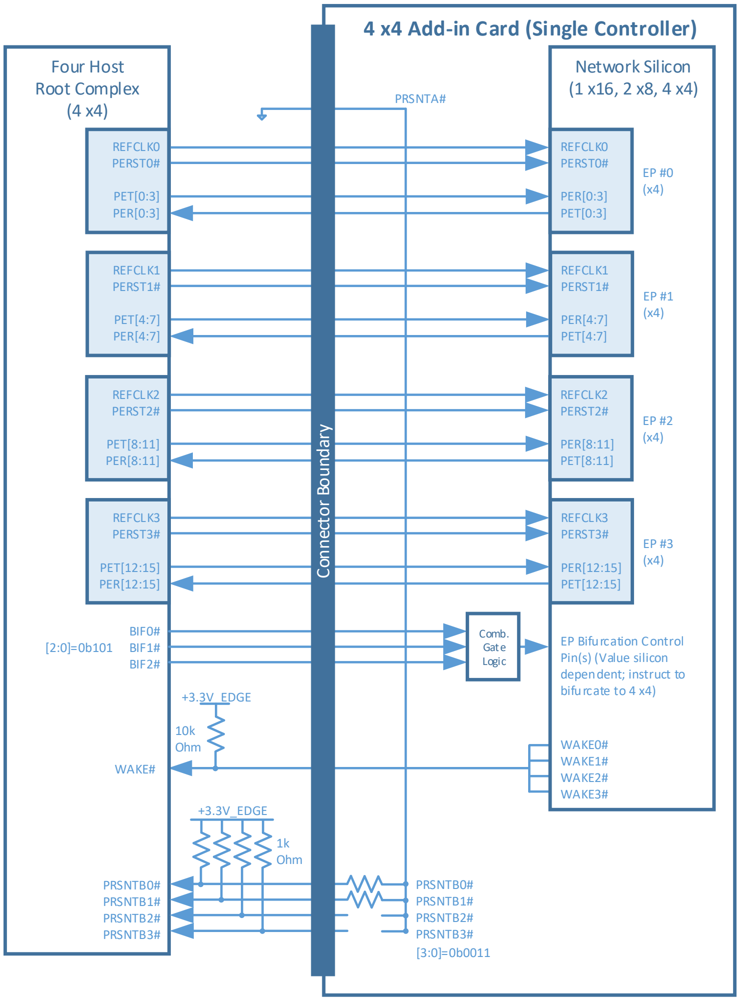
Figure 77: Single Host (2 x8) and 2 x8 OCP NIC 3.0 Card (Dual Controllers)



3.6.5.3 Quad Host (4 x4) Baseboard with a 4 x4 OCP NIC 3.0 Card (Single Controller)

Figure 78 illustrates a ~~four~~ quad host baseboard that supports 4 x4 with a single controller OCP NIC 3.0 card that supports 1 x16, 2 x8 and 4 x4. The PRSTNB[3:0]# state is 0b0011. The BIF[2:0]# state is 0b101 as the end point network controller is forced to bifurcate to 4 x4. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16, 2 x8 and 4 x4. The ~~four~~ quad host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

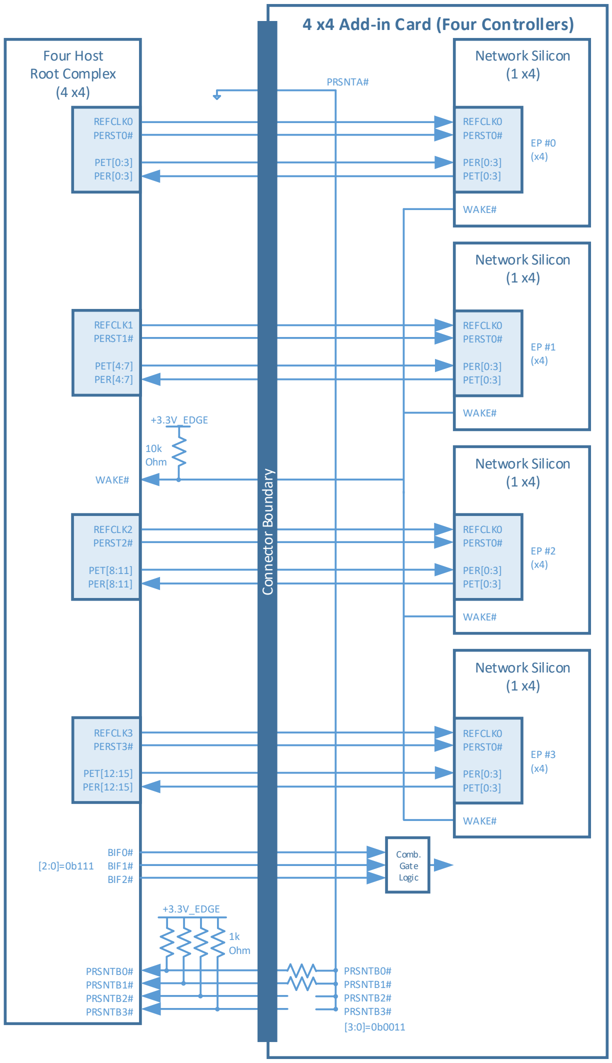
Figure 78: ~~Four~~ Quad Hosts (4 x4) and 4 x4 OCP NIC 3.0 Card (Single Controller)



3.6.5.4 Quad Host (4 x4) Baseboard with a 4 x4 OCP NIC 3.0 Card (Quad Controllers)

Figure 79 illustrates a ~~four~~ quad host baseboard that supports 4 x4 with a ~~four~~ quad controller OCP NIC 3.0 card that supports 4 x4. The PRSTNB[3:0]# state is 0b0011. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 4 x4. The ~~four~~ quad host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

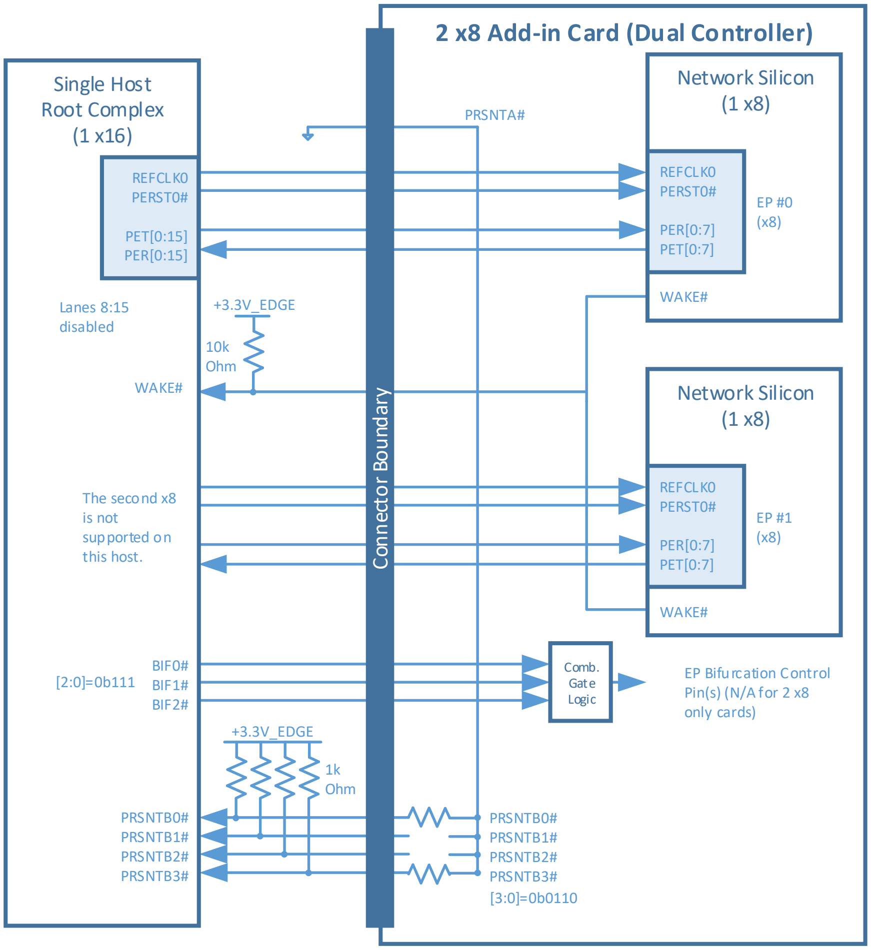
Figure 79: ~~Four~~ Quad Hosts (4 x4) and 4 x4 OCP NIC 3.0 Card (~~Four~~ Quad Controllers)



3.6.5.5 Single Host (1 x16, no Bifurcation) Baseboard with a 2 x8 OCP NIC 3.0 Card (Dual Controller)

Figure 80 illustrates a single host baseboard that supports 1 x16 with a dual controller OCP NIC 3.0 card that supports 2 x8. The PRSTNB[3:0]# state is 0b0110. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 2 x8. The ~~four~~ quad host baseboard determines that it is capable of 1x 16, but down shifts to 1 x8. The resulting link width is 1 x8 and only on endpoint 0.

Figure 80: Single Host with no Bifurcation (1 x16) and 2 x8 OCP NIC 3.0 Card (~~Two~~ Dual Controllers)



3.7 PCIe Clocking Topology

The OCP NIC 3.0 specification allows for up to four PCIe REFCLKs on the Primary Connector and up to two PCIe REFCLKs on the Secondary Connector. In general, the association of each REFCLK is based on the PCIe Link number on a per connector basis and is shown in Table 28. Cards that implement both the Primary and Secondary Connectors have a total of up to 6 REFCLKs.

Table 28: PCIe Clock Associations

REFCLK #	Description	Availability (Connector)
REFCLK0	REFCLK associated with Link 0.	Primary and Secondary Connectors.
REFCLK1	REFCLK associated with Link 1.	Primary and Secondary Connectors.
REFCLK2	REFCLK associated with Link 2.	Primary Connector only.
REFCLK3	REFCLK associated with Link 3.	Primary Connector only.

For each OCP NIC 3.0 card, the following REFCLK connection rules must be followed:

- For a 1 x16 capable OCP NIC 3.0 card, REFCLK0 shall be used for lanes [0:15].
- For a 2 x8 capable OCP NIC 3.0 card, REFCLK0 shall be used for lanes [0:7] and REFCLK1 shall be used for lanes [8:15].
- For a 4 x4 capable OCP NIC 3.0 card, REFCLK0 shall be used for lanes [0:3], REFCLK1 shall be used for lanes [4:7], REFCLK2 shall be used for lanes [8:11] and REFCLK3 shall be used for lanes [12:15]. Pins for REFCLK2 and REFCLK3 are described in Section 3.5.1 and are located on the 28-pin OCP bay.

Figure 81: PCIe Interface Connections for 1 x16 and 2 x8 OCP NIC 3.0 Cards

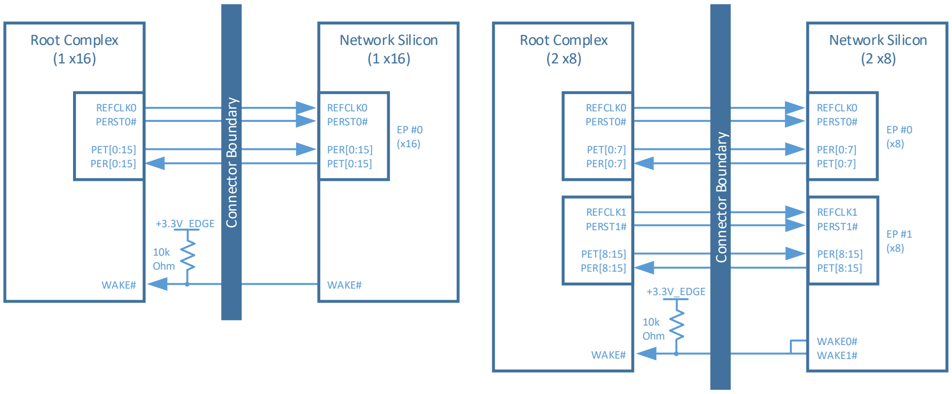
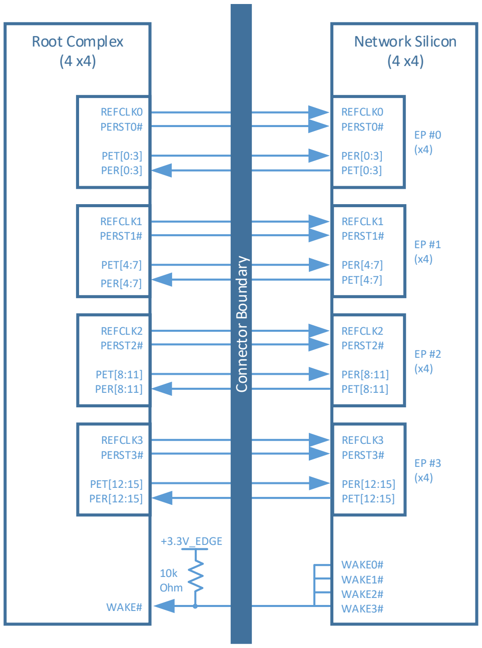


Figure 82: PCIe Interface Connections for a 4 x4 OCP NIC 3.0 Card



3.8 PCIe Bifurcation Results and REFCLK Mapping

For the cases where the baseboard and OCP NIC 3.0 card bifurcation are permissible, this section enumerates all of the supported PCIe link, lane and REFCLK mappings for each supported configuration. The bifurcation decoder is shown in Section 3.6.3.

Table 29: Bifurcation for Single Host, Single Socket and Single Upstream Link (BIF[2:0]#=0b000)

Commented [CP27]: Can we turn this table into a more readable format? Same as the following bifurcation tables

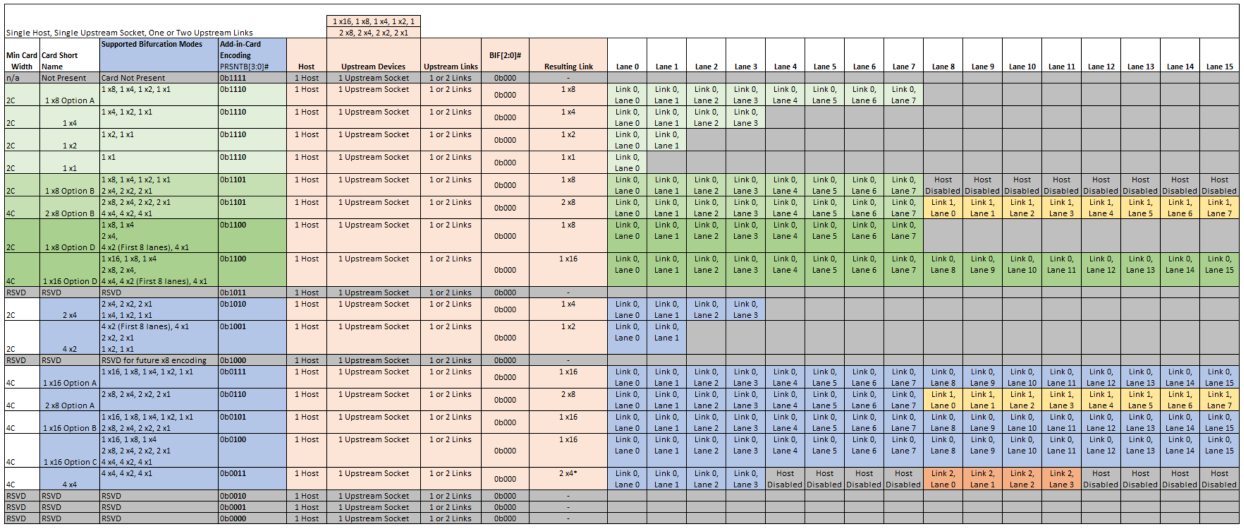
Commented [NT28R27]: Can you please provide a suggestion on how to format these tables differently?

Single Host, Single Upstream Socket, One Upstream Link, no bifurcation

1 x16, 1 x8, 1 x4, 1 x2, 1

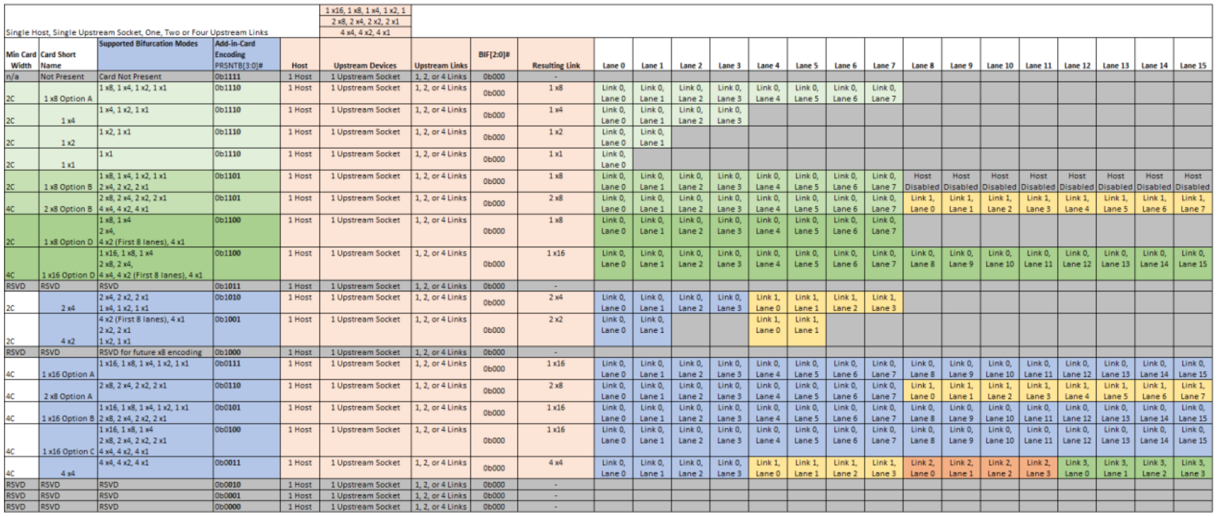
Min Card Width	Card Short Name	Supported Bifurcation Modes	Add-in-Card Encoding PRSNTB[3:0]#	Host	Upstream Devices	Upstream Links	BIF[2:0]#	Resulting Link	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7	Lane 8	Lane 9	Lane 10	Lane 11	Lane 12	Lane 13	Lane 14	Lane 15
n/a	Not Present	Card Not Present	0b1111	1 Host	1 Upstream Socket	1 Link	0b000	-																
2C	1 x8 Option A	1 x8, 1 x4, 1 x2, 1 x1	0b1110	1 Host	1 Upstream Socket	1 Link	0b000	1 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7								
2C	1 x4	1 x4, 1 x2, 1 x1	0b1110	1 Host	1 Upstream Socket	1 Link	0b000	1 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3												
2C	1 x2	1 x2, 1 x1	0b1110	1 Host	1 Upstream Socket	1 Link	0b000	1 x2	Link 0, Lane 0	Link 0, Lane 1														
2C	1 x1	1 x1	0b1110	1 Host	1 Upstream Socket	1 Link	0b000	1 x1	Link 0, Lane 0															
2C	1 x8 Option B	1 x8, 1 x4, 1 x2, 1 x1 2 x4, 2 x2, 2 x1	0b1101	1 Host	1 Upstream Socket	1 Link	0b000	1 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled
4C	2 x8 Option B	2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b1101	1 Host	1 Upstream Socket	1 Link	0b000	1 x8*	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled
2C	1 x8 Option D	1 x8, 1 x4 2 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	1 Host	1 Upstream Socket	1 Link	0b000	1 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7								
4C	1 x16 Option D	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 4 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	1 Host	1 Upstream Socket	1 Link	0b000	1 x16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 0, Lane 8	Link 0, Lane 9	Link 0, Lane 10	Link 0, Lane 11	Link 0, Lane 12	Link 0, Lane 13	Link 0, Lane 14	Link 0, Lane 15
RSVD	RSVD	RSVD	0b1011	1 Host	1 Upstream Socket	1 Link	0b000	-																
2C	2 x4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1010	1 Host	1 Upstream Socket	1 Link	0b000	1 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3												
2C	4 x2	4 x2 (First 8 lanes), 4 x1 2 x2, 2 x1 1 x2, 1 x1	0b1001	1 Host	1 Upstream Socket	1 Link	0b000	1 x2	Link 0, Lane 0	Link 0, Lane 1														
RSVD	RSVD	RSVD for future x8 encoding	0b1000	1 Host	1 Upstream Socket	1 Link	0b000	-																
4C	1 x16 Option A	1 x16, 1 x8, 1 x4, 1 x2, 1 x1	0b0111	1 Host	1 Upstream Socket	1 Link	0b000	1 x16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 0, Lane 8	Link 0, Lane 9	Link 0, Lane 10	Link 0, Lane 11	Link 0, Lane 12	Link 0, Lane 13	Link 0, Lane 14	Link 0, Lane 15
4C	2 x8 Option A	2 x8, 2 x4, 2 x2, 2 x1	0b0110	1 Host	1 Upstream Socket	1 Link	0b000	1 x8*	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled
4C	1 x16 Option B	1 x16, 1 x8, 1 x4, 1 x2, 1 x1 2 x8, 2 x4, 2 x2, 2 x1	0b0101	1 Host	1 Upstream Socket	1 Link	0b000	1 x16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 0, Lane 8	Link 0, Lane 9	Link 0, Lane 10	Link 0, Lane 11	Link 0, Lane 12	Link 0, Lane 13	Link 0, Lane 14	Link 0, Lane 15
4C	1 x16 Option C	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b0100	1 Host	1 Upstream Socket	1 Link	0b000	1 x16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 0, Lane 8	Link 0, Lane 9	Link 0, Lane 10	Link 0, Lane 11	Link 0, Lane 12	Link 0, Lane 13	Link 0, Lane 14	Link 0, Lane 15
4C	4 x4	4 x4, 4 x2, 4 x1	0b0011	1 Host	1 Upstream Socket	1 Link	0b000	1 x4*	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled
RSVD	RSVD	RSVD	0b0010	1 Host	1 Upstream Socket	1 Link	0b000	-																
RSVD	RSVD	RSVD	0b0001	1 Host	1 Upstream Socket	1 Link	0b000	-																
RSVD	RSVD	RSVD	0b0000	1 Host	1 Upstream Socket	1 Link	0b000	-																

Table 30: Bifurcation for Single Host, Single Socket and Single/Dual Upstream Links (BIF[2:0]#=0b000)



Single Host, Single Upstream Socket, One or Two Upstream Links					1 x16, 1 x8, 1 x4, 1 x2, 1 2 x8, 2 x4, 2 x2, 2 x1																	
Min Card Width	**Card Short Name**	**Supported Bifurcation Modes**	**Add-in-Card Encoding** PRSNTB[3:0]#	**Host**	**Upstream Devices**	**Upstream Links**	**BIF[2:0]#**	**Resulting Link**	**Lane 0**	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 4**	**Lane 5**	**Lane 6**	**Lane 7**	**Lane 8**	**Lane 9**	**Lane 10**	**Lane 11**	**Lane 12**	**Lane 13**	**Lane 14**	**Lane 15**
n/a	Not Present	Card Not Present	0b1111	1 Host	1 Upstream Socket	1 or 2 Links	0b000	-																
2C	1 x8 Option A	1 x8, 1 x4, 1 x2, 1 x1	0b1110	1 Host	1 Upstream Socket	1 or 2 Links	0b000	1 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7								
2C	1 x4	1 x4, 1 x2, 1 x1	0b1110	1 Host	1 Upstream Socket	1 or 2 Links	0b000	1 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3												
2C	1 x2	1 x2, 1 x1	0b1110	1 Host	1 Upstream Socket	1 or 2 Links	0b000	1 x2	Link 0, Lane 0	Link 0, Lane 1														
2C	1 x1	1 x1	0b1110	1 Host	1 Upstream Socket	1 or 2 Links	0b000	1 x1	Link 0, Lane 0															
2C	1 x8 Option B	1 x8, 1 x4, 1 x2, 1 x1 2 x4, 2 x2, 2 x1	0b1101	1 Host	1 Upstream Socket	1 or 2 Links	0b000	1 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled
4C	2 x8 Option B	2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b1101	1 Host	1 Upstream Socket	1 or 2 Links	0b000	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
2C	1 x8 Option D	1 x8, 1 x4 2 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	1 Host	1 Upstream Socket	1 or 2 Links	0b000	1 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7								
4C	1 x16 Option D	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 4 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	1 Host	1 Upstream Socket	1 or 2 Links	0b000	1 x16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 0, Lane 8	Link 0, Lane 9	Link 0, Lane 10	Link 0, Lane 11	Link 0, Lane 12	Link 0, Lane 13	Link 0, Lane 14	Link 0, Lane 15
RSVD	RSVD	RSVD	0b1011	1 Host	1 Upstream Socket	1 or 2 Links	0b000	-																
2C	2 x4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1010	1 Host	1 Upstream Socket	1 or 2 Links	0b000	1 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3												
2C	4 x2	4 x2 (First 8 lanes), 4 x1 2 x2, 2 x1 1 x2, 1 x1	0b1001	1 Host	1 Upstream Socket	1 or 2 Links	0b000	1 x2	Link 0, Lane 0	Link 0, Lane 1														
RSVD	RSVD	RSVD for future x8 encoding	0b1000	1 Host	1 Upstream Socket	1 or 2 Links	0b000	-																
4C	1 x16 Option A	1 x16, 1 x8, 1 x4, 1 x2, 1 x1	0b0111	1 Host	1 Upstream Socket	1 or 2 Links	0b000	1 x16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 0, Lane 8	Link 0, Lane 9	Link 0, Lane 10	Link 0, Lane 11	Link 0, Lane 12	Link 0, Lane 13	Link 0, Lane 14	Link 0, Lane 15
4C	2 x8 Option A	2 x8, 2 x4, 2 x2, 2 x1	0b0110	1 Host	1 Upstream Socket	1 or 2 Links	0b000	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
4C	1 x16 Option B	1 x16, 1 x8, 1 x4, 1 x2, 1 x1 2 x8, 2 x4, 2 x2, 2 x1	0b0101	1 Host	1 Upstream Socket	1 or 2 Links	0b000	1 x16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 0, Lane 8	Link 0, Lane 9	Link 0, Lane 10	Link 0, Lane 11	Link 0, Lane 12	Link 0, Lane 13	Link 0, Lane 14	Link 0, Lane 15
4C	1 x16 Option C	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b0100	1 Host	1 Upstream Socket	1 or 2 Links	0b000	1 x16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 0, Lane 8	Link 0, Lane 9	Link 0, Lane 10	Link 0, Lane 11	Link 0, Lane 12	Link 0, Lane 13	Link 0, Lane 14	Link 0, Lane 15
4C	4 x4	4 x4, 4 x2, 4 x1	0b0011	1 Host	1 Upstream Socket	1 or 2 Links	0b000	2 x4*	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3	Host Disabled	Host Disabled	Host Disabled	Host Disabled
RSVD	RSVD	RSVD	0b0010	1 Host	1 Upstream Socket	1 or 2 Links	0b000	-																
RSVD	RSVD	RSVD	0b0001	1 Host	1 Upstream Socket	1 or 2 Links	0b000	-																
RSVD	RSVD	RSVD	0b0000	1 Host	1 Upstream Socket	1 or 2 Links	0b000	-																

Table 31: Bifurcation for Single Host, Single Socket and Single/Dual/Quad Upstream Links (BIF[2:0]#=0b000)



Single Host, Single Upstream Socket, One, Two or Four Upstream Links

1 x16, 1 x8, 1 x4, 1 x2, 1
2 x8, 2 x4, 2 x2, 2 x1
4 x4, 4 x2, 4 x1

Min Card Width	Card Short Name	Supported Bifurcation Modes	Add-in-Card Encoding PRSNTB[3:0]#	Host	Upstream Devices	Upstream Links	BIF[2:0]#	Resulting Link	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7	Lane 8	Lane 9	Lane 10	Lane 11	Lane 12	Lane 13	Lane 14	Lane 15
n/a	Not Present	Card Not Present	0b1111	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	-																
2C	1 x8 Option A	1 x8, 1 x4, 1 x2, 1 x1	0b1110	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	1 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7								
2C	1 x4	1 x4, 1 x2, 1 x1	0b1110	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	1 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3												
2C	1 x2	1 x2, 1 x1	0b1110	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	1 x2	Link 0, Lane 0	Link 0, Lane 1														
2C	1 x1	1 x1	0b1110	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	1 x1	Link 0, Lane 0															
2C	1 x8 Option B	1 x8, 1 x4, 1 x2, 1 x1 2 x4, 2 x2, 2 x1	0b1101	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	1 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled
4C	2 x8 Option B	2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b1101	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
2C	1 x8 Option D	1 x8, 1 x4 2 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	1 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7								
4C	1 x16 Option D	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 4 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	1 x16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 0, Lane 8	Link 0, Lane 9	Link 0, Lane 10	Link 0, Lane 11	Link 0, Lane 12	Link 0, Lane 13	Link 0, Lane 14	Link 0, Lane 15
RSVD	RSVD	RSVD	0b1011	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	-																
2C	2 x4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1010	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	2 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3								
2C	4 x2	4 x2 (First 8 lanes), 4 x1 2 x2, 2 x1 1 x2, 1 x1	0b1001	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	2 x2	Link 0, Lane 0	Link 0, Lane 1			Link 1, Lane 0	Link 1, Lane 1										
RSVD	RSVD	RSVD for future x8 encoding	0b1000	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	-																
4C	1 x16 Option A	1 x16, 1 x8, 1 x4, 1 x2, 1 x1	0b0111	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	1 x16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 0, Lane 8	Link 0, Lane 9	Link 0, Lane 10	Link 0, Lane 11	Link 0, Lane 12	Link 0, Lane 13	Link 0, Lane 14	Link 0, Lane 15
4C	2 x8 Option A	2 x8, 2 x4, 2 x2, 2 x1	0b0110	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
4C	1 x16 Option B	1 x16, 1 x8, 1 x4, 1 x2, 1 x1 2 x8, 2 x4, 2 x2, 2 x1	0b0101	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	1 x16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 0, Lane 8	Link 0, Lane 9	Link 0, Lane 10	Link 0, Lane 11	Link 0, Lane 12	Link 0, Lane 13	Link 0, Lane 14	Link 0, Lane 15
4C	1 x16 Option C	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b0100	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	1 x16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 0, Lane 8	Link 0, Lane 9	Link 0, Lane 10	Link 0, Lane 11	Link 0, Lane 12	Link 0, Lane 13	Link 0, Lane 14	Link 0, Lane 15
4C	4 x4	4 x4, 4 x2, 4 x1	0b0011	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	4 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3	Link 3, Lane 0	Link 3, Lane 1	Link 3, Lane 2	Link 3, Lane 3
RSVD	RSVD	RSVD	0b0010	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	-																
RSVD	RSVD	RSVD	0b0001	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	-																
RSVD	RSVD	RSVD	0b0000	1 Host	1 Upstream Socket	1, 2, or 4 Links	0b000	-																

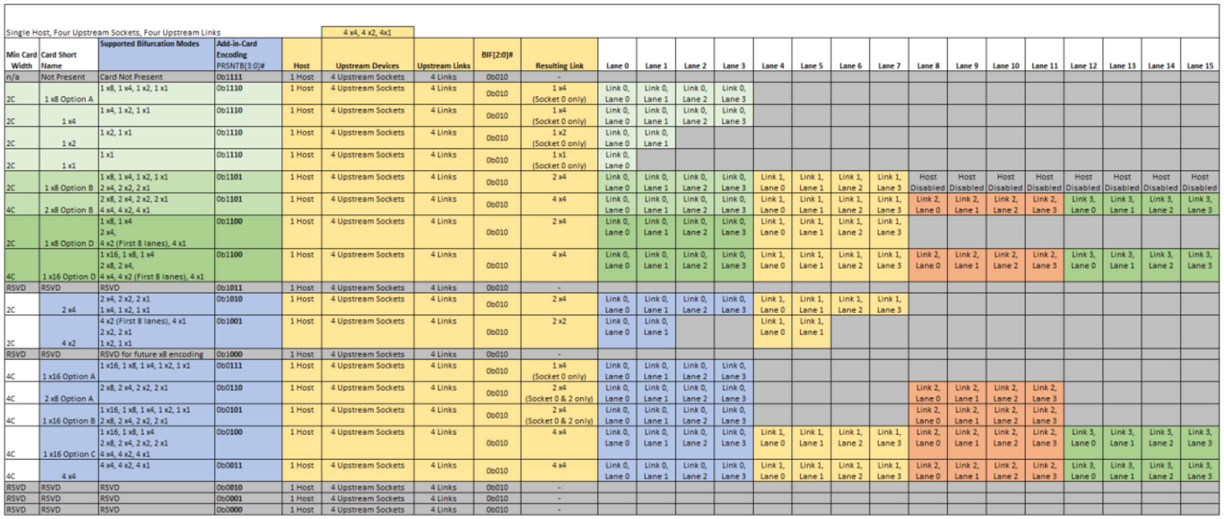
Table 32: Bifurcation for Single Host, Dual Sockets and Dual Upstream Links (BIF[2:0]#=0b001)

Single Host, Two Upstream Sockets, Two Upstream Links

1 x8, 1 x4, 1 x2, 1 x1
2 x8, 2 x4, 2 x2, 2x1

Min Card Width	Card Short Name	Supported Bifurcation Modes	Add-in-Card Encoding PRSNTB[3:0]#	Host	Upstream Devices	Upstream Links	BIF[2:0]#	Resulting Link	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7	Lane 8	Lane 9	Lane 10	Lane 11	Lane 12	Lane 13	Lane 14	Lane 15
n/a	Not Present	Card Not Present	0b1111	1 Host	2 Upstream Sockets	2 Links	0b001	-																
2C	1 x8 Option A	1 x8, 1 x4, 1 x2, 1 x1	0b1110	1 Host	2 Upstream Sockets	2 Links	0b001	1 x8 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7								
2C	1 x4	1 x4, 1 x2, 1 x1	0b1110	1 Host	2 Upstream Sockets	2 Links	0b001	1 x4 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3												
2C	1 x2	1 x2, 1 x1	0b1110	1 Host	2 Upstream Sockets	2 Links	0b001	1 x2 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1														
2C	1 x1	1 x1	0b1110	1 Host	2 Upstream Sockets	2 Links	0b001	1 x1 (Socket 0 only)	Link 0, Lane 0															
2C	1 x8 Option B	1 x8, 1 x4, 1 x2, 1 x1 2 x4, 2 x2, 2 x1	0b1101	1 Host	2 Upstream Sockets	2 Links	0b001	1 x8 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled
4C	2 x8 Option B	2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b1101	1 Host	2 Upstream Sockets	2 Links	0b001	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
2C	1 x8 Option D	1 x8, 1 x4 2 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	1 Host	2 Upstream Sockets	2 Links	0b001	1 x8 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7								
4C	1 x16 Option D	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 4 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	1 Host	2 Upstream Sockets	2 Links	0b001	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
RSVD	RSVD	RSVD	0b1011	1 Host	2 Upstream Sockets	2 Links	0b001	-																
2C	2 x4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1010	1 Host	2 Upstream Sockets	2 Links	0b001	1 x4 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3												
2C	4 x2	4 x2 (First 8 lanes), 4 x1 2 x2, 2 x1 1 x2, 1 x1	0b1001	1 Host	2 Upstream Sockets	2 Links	0b001	1 x2 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1														
RSVD	RSVD	RSVD for future x8 encoding	0b1000	1 Host	2 Upstream Sockets	2 Links	0b001	-																
4C	1 x16 Option A	1 x16, 1 x8, 1 x4, 1 x2, 1 x1	0b0111	1 Host	2 Upstream Sockets	2 Links	0b001	1 x8 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7								
4C	2 x8 Option A	2 x8, 2 x4, 2 x2, 2 x1	0b0110	1 Host	2 Upstream Sockets	2 Links	0b001	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
4C	1 x16 Option B	1 x16, 1 x8, 1 x4, 1 x2, 1 x1 2 x8, 2 x4, 2 x2, 2 x1	0b0101	1 Host	2 Upstream Sockets	2 Links	0b001	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
4C	1 x16 Option C	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b0100	1 Host	2 Upstream Sockets	2 Links	0b001	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
4C	4 x4	4 x4, 4 x2, 4 x1	0b0011	1 Host	2 Upstream Sockets	2 Links	0b001	2 x4 (EP 0 and 2 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3					Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3				
RSVD	RSVD	RSVD	0b0010	1 Host	2 Upstream Sockets	2 Links	0b001	-																
RSVD	RSVD	RSVD	0b0001	1 Host	2 Upstream Sockets	2 Links	0b001	-																
RSVD	RSVD	RSVD	0b0000	1 Host	2 Upstream Sockets	2 Links	0b001	-																

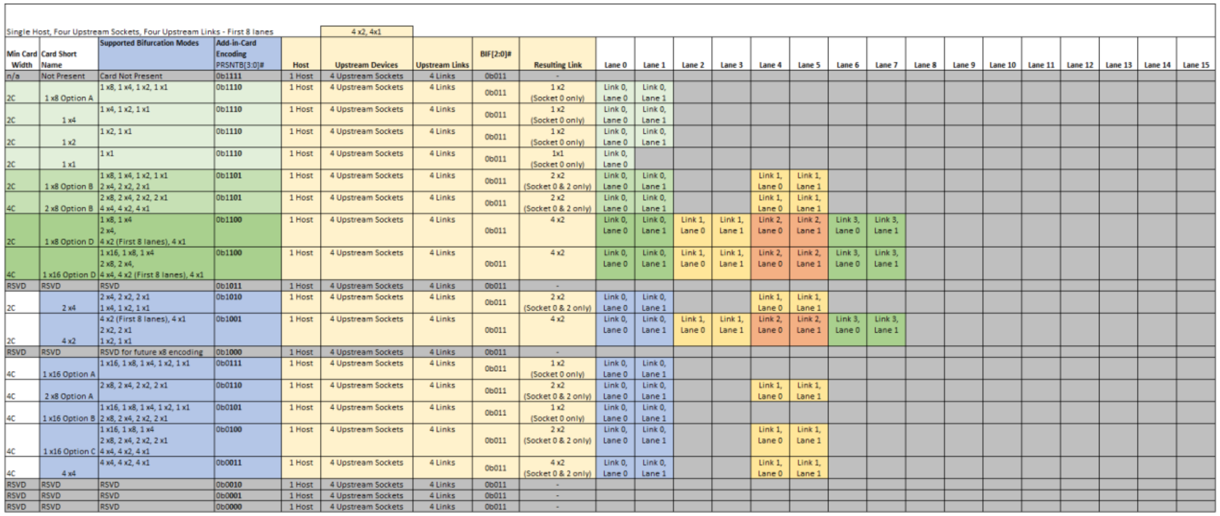
Table 33: Bifurcation for Single Host, Quad Sockets and Quad Upstream Links (BIF[2:0]#=0b010)



Single Host, Four Upstream Sockets, Four Upstream Links

					4 x4, 4 x2, 4x1																			
Min Card Width	**Card Short Name**	**Supported Bifurcation Modes**	**Add-in-Card Encoding** PRSNTB[3:0]#	**Host**	**Upstream Devices**	**Upstream Links**	**BIF[2:0]#**	**Resulting Link**	**Lane 0**	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 4**	**Lane 5**	**Lane 6**	**Lane 7**	**Lane 8**	**Lane 9**	**Lane 10**	**Lane 11**	**Lane 12**	**Lane 13**	**Lane 14**	**Lane 15**
n/a	Not Present	Card Not Present	0b1111	1 Host	4 Upstream Sockets	4 Links	0b010	-																
2C	1 x8 Option A	1 x8, 1 x4, 1 x2, 1 x1	0b1110	1 Host	4 Upstream Sockets	4 Links	0b010	1 x4 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3												
2C	1 x4	1 x4, 1 x2, 1 x1	0b1110	1 Host	4 Upstream Sockets	4 Links	0b010	1 x4 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3												
2C	1 x2	1 x2, 1 x1	0b1110	1 Host	4 Upstream Sockets	4 Links	0b010	1 x2 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1														
2C	1 x1	1 x1	0b1110	1 Host	4 Upstream Sockets	4 Links	0b010	1 x1 (Socket 0 only)	Link 0, Lane 0															
2C	1 x8 Option B	1 x8, 1 x4, 1 x2, 1 x1 2 x4, 2 x2, 2 x1	0b1101	1 Host	4 Upstream Sockets	4 Links	0b010	2 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled
4C	2 x8 Option B	2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b1101	1 Host	4 Upstream Sockets	4 Links	0b010	4 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3	Link 3, Lane 0	Link 3, Lane 1	Link 3, Lane 2	Link 3, Lane 3
2C	1 x8 Option D	1 x8, 1 x4 2 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	1 Host	4 Upstream Sockets	4 Links	0b010	2 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3								
4C	1 x16 Option D	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 4 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	1 Host	4 Upstream Sockets	4 Links	0b010	4 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3	Link 3, Lane 0	Link 3, Lane 1	Link 3, Lane 2	Link 3, Lane 3
RSVD	RSVD	RSVD	0b1011	1 Host	4 Upstream Sockets	4 Links	0b010	-																
2C	2 x4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1010	1 Host	4 Upstream Sockets	4 Links	0b010	2 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3								
2C	4 x2	4 x2 (First 8 lanes), 4 x1 2 x2, 2 x1 1 x2, 1 x1	0b1001	1 Host	4 Upstream Sockets	4 Links	0b010	2 x2	Link 0, Lane 0	Link 0, Lane 1			Link 1, Lane 0	Link 1, Lane 1										
RSVD	RSVD	RSVD for future x8 encoding	0b1000	1 Host	4 Upstream Sockets	4 Links	0b010	-																
4C	1 x16 Option A	1 x16, 1 x8, 1 x4, 1 x2, 1 x1	0b0111	1 Host	4 Upstream Sockets	4 Links	0b010	1 x4 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3												
4C	2 x8 Option A	2 x8, 2 x4, 2 x2, 2 x1	0b0110	1 Host	4 Upstream Sockets	4 Links	0b010	2 x4 (Socket 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3					Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3				
4C	1 x16 Option B	1 x16, 1 x8, 1 x4, 1 x2, 1 x1 2 x8, 2 x4, 2 x2, 2 x1	0b0101	1 Host	4 Upstream Sockets	4 Links	0b010	2 x4 (Socket 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3					Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3				
4C	1 x16 Option C	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b0100	1 Host	4 Upstream Sockets	4 Links	0b010	4 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3	Link 3, Lane 0	Link 3, Lane 1	Link 3, Lane 2	Link 3, Lane 3
4C	4 x4	4 x4, 4 x2, 4 x1	0b0011	1 Host	4 Upstream Sockets	4 Links	0b010	4 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3	Link 3, Lane 0	Link 3, Lane 1	Link 3, Lane 2	Link 3, Lane 3
RSVD	RSVD	RSVD	0b0010	1 Host	4 Upstream Sockets	4 Links	0b010	-																
RSVD	RSVD	RSVD	0b0001	1 Host	4 Upstream Sockets	4 Links	0b010	-																
RSVD	RSVD	RSVD	0b0000	1 Host	4 Upstream Sockets	4 Links	0b010	-																

Table 34: Bifurcation for Single Host, Quad Sockets and Quad Upstream Links – First 8 PCIe Lanes (BIF[2:0]#=0b011)



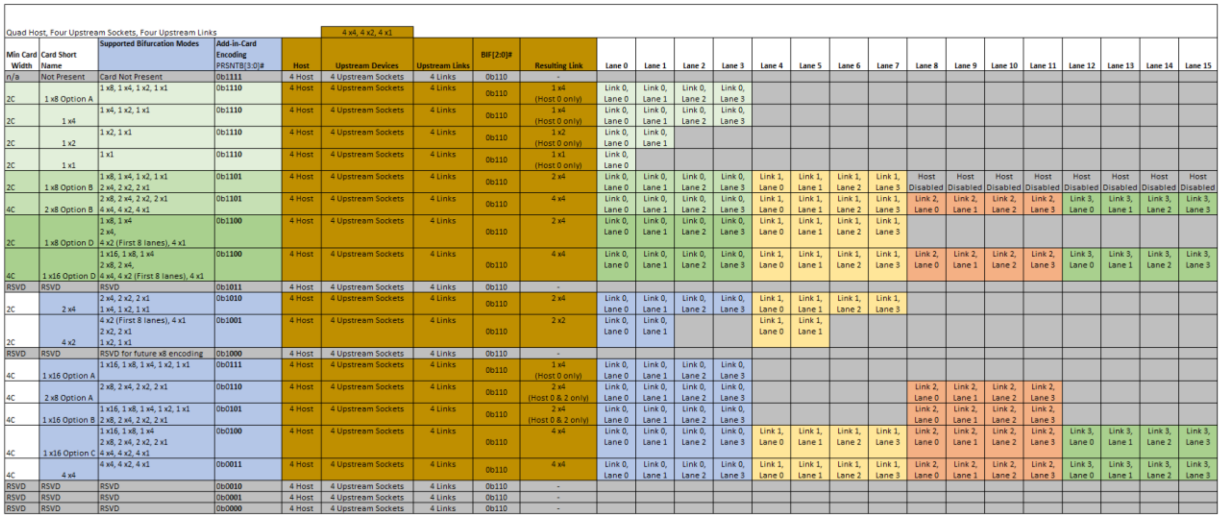
Single Host, Four Upstream Sockets, Four Upstream Links - First 8 lanes

					4 x2, 4x1																			
Min Card Width	**Card Short Name**	**Supported Bifurcation Modes**	**Add-in-Card Encoding PRSNTB[3:0]#**	**Host**	**Upstream Devices**	**Upstream Links**	**BIF[2:0]#**	**Resulting Link**	**Lane 0**	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 4**	**Lane 5**	**Lane 6**	**Lane 7**	**Lane 8**	**Lane 9**	**Lane 10**	**Lane 11**	**Lane 12**	**Lane 13**	**Lane 14**	**Lane 15**
n/a	Not Present	Card Not Present	0b1111	1 Host	4 Upstream Sockets	4 Links	0b011	-																
2C	1 x8 Option A	1 x8, 1 x4, 1 x2, 1 x1	0b1110	1 Host	4 Upstream Sockets	4 Links	0b011	1 x2 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1														
2C	1 x4	1 x4, 1 x2, 1 x1	0b1110	1 Host	4 Upstream Sockets	4 Links	0b011	1 x2 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1														
2C	1 x2	1 x2, 1 x1	0b1110	1 Host	4 Upstream Sockets	4 Links	0b011	1 x2 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1														
2C	1 x1	1 x1	0b1110	1 Host	4 Upstream Sockets	4 Links	0b011	1x1 (Socket 0 only)	Link 0, Lane 0															
2C	1 x8 Option B	1 x8, 1 x4, 1 x2, 1 x1 2 x4, 2 x2, 2 x1	0b1101	1 Host	4 Upstream Sockets	4 Links	0b011	2 x2 (Socket 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1			Link 1, Lane 0	Link 1, Lane 1										
4C	2 x8 Option B	2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b1101	1 Host	4 Upstream Sockets	4 Links	0b011	2 x2 (Socket 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1			Link 1, Lane 0	Link 1, Lane 1										
2C	1 x8 Option D	1 x8, 1 x4 2 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	1 Host	4 Upstream Sockets	4 Links	0b011	4 x2	Link 0, Lane 0	Link 0, Lane 1	Link 1, Lane 0	Link 1, Lane 1	Link 2, Lane 0	Link 2, Lane 1	Link 3, Lane 0	Link 3, Lane 1								
4C	1 x16 Option D	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 4 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	1 Host	4 Upstream Sockets	4 Links	0b011	4 x2	Link 0, Lane 0	Link 0, Lane 1	Link 1, Lane 0	Link 1, Lane 1	Link 2, Lane 0	Link 2, Lane 1	Link 3, Lane 0	Link 3, Lane 1								
RSVD	RSVD	RSVD	0b1011	1 Host	4 Upstream Sockets	4 Links	0b011	-																
2C	2 x4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1010	1 Host	4 Upstream Sockets	4 Links	0b011	2 x2 (Socket 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1			Link 1, Lane 0	Link 1, Lane 1										
2C	4 x2	4 x2 (First 8 lanes), 4 x1 2 x2, 2 x1 1 x2, 1 x1	0b1001	1 Host	4 Upstream Sockets	4 Links	0b011	4 x2	Link 0, Lane 0	Link 0, Lane 1	Link 1, Lane 0	Link 1, Lane 1	Link 2, Lane 0	Link 2, Lane 1	Link 3, Lane 0	Link 3, Lane 1								
RSVD	RSVD	RSVD for future x8 encoding	0b1000	1 Host	4 Upstream Sockets	4 Links	0b011	-																
4C	1 x16 Option A	1 x16, 1 x8, 1 x4, 1 x2, 1 x1	0b0111	1 Host	4 Upstream Sockets	4 Links	0b011	1 x2 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1														
4C	2 x8 Option A	2 x8, 2 x4, 2 x2, 2 x1	0b0110	1 Host	4 Upstream Sockets	4 Links	0b011	2 x2 (Socket 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1			Link 1, Lane 0	Link 1, Lane 1										
4C	1 x16 Option B	1 x16, 1 x8, 1 x4, 1 x2, 1 x1 2 x8, 2 x4, 2 x2, 2 x1	0b0101	1 Host	4 Upstream Sockets	4 Links	0b011	1 x2 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1														
4C	1 x16 Option C	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b0100	1 Host	4 Upstream Sockets	4 Links	0b011	2 x2 (Socket 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1			Link 1, Lane 0	Link 1, Lane 1										
4C	4 x4	4 x4, 4 x2, 4 x1	0b0011	1 Host	4 Upstream Sockets	4 Links	0b011	4 x2 (Socket 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1			Link 1, Lane 0	Link 1, Lane 1										
RSVD	RSVD	RSVD	0b0010	1 Host	4 Upstream Sockets	4 Links	0b011	-																
RSVD	RSVD	RSVD	0b0001	1 Host	4 Upstream Sockets	4 Links	0b011	-																
RSVD	RSVD	RSVD	0b0000	1 Host	4 Upstream Sockets	4 Links	0b011	-																

Table 35: Bifurcation for Dual Host, Dual Sockets and Dual Upstream Links (BIF[2:0]#=0b101)

Dual Host, Two Upstream Sockets, Two Upstream Links					2 x8, 2 x4, 2 x2, 2 x1																			
Min Card Width	Card Short Name	Supported Bifurcation Modes	Add-in-Card Encoding PRSNTB[3:0]#	Host	Upstream Devices	Upstream Links	BIF[2:0]#	Resulting Link	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7	Lane 8	Lane 9	Lane 10	Lane 11	Lane 12	Lane 13	Lane 14	Lane 15
n/a	Not Present	Card Not Present	0b1111	2 Host	2 Upstream Sockets	2 Links	0b101	-																
2C	1 x8 Option A	1 x8, 1 x4, 1 x2, 1 x1	0b1110	2 Host	2 Upstream Sockets	2 Links	0b101	1 x8 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7								
2C	1 x4	1 x4, 1 x2, 1 x1	0b1110	2 Host	2 Upstream Sockets	2 Links	0b101	1 x4 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3												
2C	1 x2	1 x2, 1 x1	0b1110	2 Host	2 Upstream Sockets	2 Links	0b101	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1														
2C	1 x1	1 x1	0b1110	2 Host	2 Upstream Sockets	2 Links	0b101	1 x1 (Host 0 only)	Link 0, Lane 0															
2C	1 x8 Option B	1 x8, 1 x4, 1 x2, 1 x1 2 x4, 2 x2, 2 x1	0b1101	2 Host	2 Upstream Sockets	2 Links	0b101	1 x8 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled
4C	2 x8 Option B	2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b1101	2 Host	2 Upstream Sockets	2 Links	0b101	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
2C	1 x8 Option D	1 x8, 1 x4 2 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	2 Host	2 Upstream Sockets	2 Links	0b101	1 x8 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7								
4C	1 x16 Option D	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 4 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	2 Host	2 Upstream Sockets	2 Links	0b101	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
RSVD	RSVD	RSVD	0b1011	2 Host	2 Upstream Sockets	2 Links	0b101	-																
2C	2 x4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1010	2 Host	2 Upstream Sockets	2 Links	0b101	1 x4 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3												
2C	4 x2	4 x2 (First 8 lanes), 4 x1 2 x2, 2 x1 1 x2, 1 x1	0b1001	2 Host	2 Upstream Sockets	2 Links	0b101	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1														
RSVD	RSVD	RSVD for future x8 encoding	0b1000	2 Host	2 Upstream Sockets	2 Links	0b101	-																
4C	1 x16 Option A	1 x16, 1 x8, 1 x4, 1 x2, 1 x1	0b0111	2 Host	2 Upstream Sockets	2 Links	0b101	1 x8 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7								
4C	2 x8 Option A	2 x8, 2 x4, 2 x2, 2 x1	0b0110	2 Host	2 Upstream Sockets	2 Links	0b101	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
4C	1 x16 Option B	1 x16, 1 x8, 1 x4, 1 x2, 1 x1 2 x8, 2 x4, 2 x2, 2 x1	0b0101	2 Host	2 Upstream Sockets	2 Links	0b101	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
4C	1 x16 Option C	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b0100	2 Host	2 Upstream Sockets	2 Links	0b101	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
4C	4 x4	4 x4, 4 x2, 4 x1	0b0011	2 Host	2 Upstream Sockets	2 Links	0b101	2 x4 (EP 0 and 2 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3					Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3				
RSVD	RSVD	RSVD	0b0010	2 Host	2 Upstream Sockets	2 Links	0b101	-																
RSVD	RSVD	RSVD	0b0001	2 Host	2 Upstream Sockets	2 Links	0b101	-																
RSVD	RSVD	RSVD	0b0000	2 Host	2 Upstream Sockets	2 Links	0b101	-																

Table 36: Bifurcation for Quad Host, Quad Sockets and Quad Upstream Links (BIF[2:0]#=0b110)



Quad Host, Four Upstream Sockets, Four Upstream Links

					4 x4, 4 x2, 4 x1																			
Min Card Width	Card Short Name	Supported Bifurcation Modes	Add-in-Card Encoding PRSNTB[3:0]#	Host	Upstream Devices	Upstream Links	BIF[2:0]#	Resulting Link	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7	Lane 8	Lane 9	Lane 10	Lane 11	Lane 12	Lane 13	Lane 14	Lane 15
n/a	Not Present	Card Not Present	0b1111	4 Host	4 Upstream Sockets	4 Links	0b110	-																
2C	1 x8 Option A	1 x8, 1 x4, 1 x2, 1 x1	0b1110	4 Host	4 Upstream Sockets	4 Links	0b110	1 x4 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3												
2C	1 x4	1 x4, 1 x2, 1 x1	0b1110	4 Host	4 Upstream Sockets	4 Links	0b110	1 x4 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3												
2C	1 x2	1 x2, 1 x1	0b1110	4 Host	4 Upstream Sockets	4 Links	0b110	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1														
2C	1 x1	1 x1	0b1110	4 Host	4 Upstream Sockets	4 Links	0b110	1 x1 (Host 0 only)	Link 0, Lane 0															
2C	1 x8 Option B	1 x8, 1 x4, 1 x2, 1 x1 2 x4, 2 x2, 2 x1	0b1101	4 Host	4 Upstream Sockets	4 Links	0b110	2 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled
4C	2 x8 Option B	2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b1101	4 Host	4 Upstream Sockets	4 Links	0b110	4 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3	Link 3, Lane 0	Link 3, Lane 1	Link 3, Lane 2	Link 3, Lane 3
2C	1 x8 Option D	1 x8, 1 x4 2 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	4 Host	4 Upstream Sockets	4 Links	0b110	2 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3								
4C	1 x16 Option D	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 4 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	4 Host	4 Upstream Sockets	4 Links	0b110	4 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3	Link 3, Lane 0	Link 3, Lane 1	Link 3, Lane 2	Link 3, Lane 3
RSVD	RSVD	RSVD	0b1011	4 Host	4 Upstream Sockets	4 Links	0b110	-																
2C	2 x4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1010	4 Host	4 Upstream Sockets	4 Links	0b110	2 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3								
2C	4 x2	4 x2 (First 8 lanes), 4 x1 2 x2, 2 x1 1 x2, 1 x1	0b1001	4 Host	4 Upstream Sockets	4 Links	0b110	2 x2	Link 0, Lane 0	Link 0, Lane 1			Link 1, Lane 0	Link 1, Lane 1										
RSVD	RSVD	RSVD for future x8 encoding	0b1000	4 Host	4 Upstream Sockets	4 Links	0b110	-																
4C	1 x16 Option A	1 x16, 1 x8, 1 x4, 1 x2, 1 x1	0b0111	4 Host	4 Upstream Sockets	4 Links	0b110	1 x4 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3												
4C	2 x8 Option A	2 x8, 2 x4, 2 x2, 2 x1	0b0110	4 Host	4 Upstream Sockets	4 Links	0b110	2 x4 (Host 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3					Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3				
4C	1 x16 Option B	1 x16, 1 x8, 1 x4, 1 x2, 1 x1 2 x8, 2 x4, 2 x2, 2 x1	0b0101	4 Host	4 Upstream Sockets	4 Links	0b110	2 x4 (Host 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3					Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3				
4C	1 x16 Option C	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b0100	4 Host	4 Upstream Sockets	4 Links	0b110	4 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3	Link 3, Lane 0	Link 3, Lane 1	Link 3, Lane 2	Link 3, Lane 3
4C	4 x4	4 x4, 4 x2, 4 x1	0b0011	4 Host	4 Upstream Sockets	4 Links	0b110	4 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3	Link 3, Lane 0	Link 3, Lane 1	Link 3, Lane 2	Link 3, Lane 3
RSVD	RSVD	RSVD	0b0010	4 Host	4 Upstream Sockets	4 Links	0b110	-																
RSVD	RSVD	RSVD	0b0001	4 Host	4 Upstream Sockets	4 Links	0b110	-																
RSVD	RSVD	RSVD	0b0000	4 Host	4 Upstream Sockets	4 Links	0b110	-																

Table 37: Bifurcation for Quad Host, Quad Sockets and Quad Upstream Links – First 8 lanes (BIF[2:0]#=0b111)

Quad Host, Four Upstream Sockets, Four Upstream links, First 8 PCIe lanes

					4 x2, 4 x1																			
Min Card Width	**Card Short Name**	**Supported Bifurcation Modes**	**Add-in-Card Encoding** PRSNTB[3:0]#	**Host**	**Upstream Devices**	**Upstream Links**	**BIF[2:0]#**	**Resulting Link**	**Lane 0**	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 4**	**Lane 5**	**Lane 6**	**Lane 7**	**Lane 8**	**Lane 9**	**Lane 10**	**Lane 11**	**Lane 12**	**Lane 13**	**Lane 14**	**Lane 15**
n/a	Not Present	Card Not Present	0b1111	4 Host	4 Upstream Sockets	4 x2 Links	0b111	-																
2C	1 x8 Option A	1 x8, 1 x4, 1 x2, 1 x1	0b1110	4 Host	4 Upstream Sockets	4 x2 Links	0b111	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1														
2C	1 x4	1 x4, 1 x2, 1 x1	0b1110	4 Host	4 Upstream Sockets	4 x2 Links	0b111	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1														
2C	1 x2	1 x2, 1 x1	0b1110	4 Host	4 Upstream Sockets	4 x2 Links	0b111	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1														
2C	1 x1	1 x1	0b1110	4 Host	4 Upstream Sockets	4 x2 Links	0b111	1x1 (Host 0 only)	Link 0, Lane 0															
2C	1 x8 Option B	1 x8, 1 x4, 1 x2, 1 x1 2 x4, 2 x2, 2 x1	0b1101	4 Host	4 Upstream Sockets	4 x2 Links	0b111	2 x2 (Host 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1	Host Disabled	Host Disabled	Link 2, Lane 0	Link 2, Lane 1	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled
4C	2 x8 Option B	2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b1101	4 Host	4 Upstream Sockets	4 x2 Links	0b111	2 x2 (Host 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1	Host Disabled	Host Disabled	Link 2, Lane 0	Link 2, Lane 1	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled	Host Disabled
2C	1 x8 Option D	1 x8, 1 x4 2 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	4 Host	4 Upstream Sockets	4 x2 Links	0b111	4 x2	Link 0, Lane 0	Link 0, Lane 1	Link 1, Lane 0	Link 1, Lane 1	Link 2, Lane 0	Link 2, Lane 1	Link 3, Lane 0	Link 3, Lane 1								
4C	1 x16 Option D	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 4 x4, 4 x2 (First 8 lanes), 4 x1	0b1100	4 Host	4 Upstream Sockets	4 x2 Links	0b111	4 x2	Link 0, Lane 0	Link 0, Lane 1	Link 1, Lane 0	Link 1, Lane 1	Link 2, Lane 0	Link 2, Lane 1	Link 3, Lane 0	Link 3, Lane 1								
RSVD	RSVD	RSVD	0b1011	4 Host	4 Upstream Sockets	4 x2 Links	0b111	-																
2C	2 x4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1010	4 Host	4 Upstream Sockets	4 x2 Links	0b111	2 x2 (Host 0 & 1 only)	Link 0, Lane 0	Link 0, Lane 1	Link 1, Lane 0	Link 1, Lane 1												
2C	4 x2	4 x2 (First 8 lanes), 4 x1 2 x2, 2 x1 1 x2, 1 x1	0b1001	4 Host	4 Upstream Sockets	4 x2 Links	0b111	4 x2	Link 0, Lane 0	Link 0, Lane 1	Link 1, Lane 0	Link 1, Lane 1	Link 2, Lane 0	Link 2, Lane 1	Link 3, Lane 0	Link 3, Lane 1								
RSVD	RSVD	RSVD for future x8 encoding	0b1000	4 Host	4 Upstream Sockets	4 x2 Links	0b111	-																
4C	1 x16 Option A	1 x16, 1 x8, 1 x4, 1 x2, 1 x1	0b0111	4 Host	4 Upstream Sockets	4 x2 Links	0b111	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1														
4C	2 x8 Option A	2 x8, 2 x4, 2 x2, 2 x1	0b0110	4 Host	4 Upstream Sockets	4 x2 Links	0b111	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1														
4C	1 x16 Option B	1 x16, 1 x8, 1 x4, 1 x2, 1 x1 2 x8, 2 x4, 2 x2, 2 x1	0b0101	4 Host	4 Upstream Sockets	4 x2 Links	0b111	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1														
4C	1 x16 Option C	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b0100	4 Host	4 Upstream Sockets	4 x2 Links	0b111	2 x2 (Host 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1			Link 2, Lane 0	Link 2, Lane 1										
4C	4 x4	4 x4, 4 x2, 4 x1	0b0011	4 Host	4 Upstream Sockets	4 x2 Links	0b111	2 x2 (Host 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1			Link 2, Lane 0	Link 2, Lane 1										
RSVD	RSVD	RSVD	0b0010	4 Host	4 Upstream Sockets	4 x2 Links	0b111	-																
RSVD	RSVD	RSVD	0b0001	4 Host	4 Upstream Sockets	4 x2 Links	0b111	-																
RSVD	RSVD	RSVD	0b0000	4 Host	4 Upstream Sockets	4 x2 Links	0b111	-																

3.9 Power Capacity and Power Delivery

There are four permissible power states: NIC Power Off, ID Mode, Aux Power Mode (S5), and Main Power Mode (S0). The transition of these states is shown in Figure 83. The max available power envelopes for each of these states are defined in Table 38.

Figure 83: Baseboard Power States

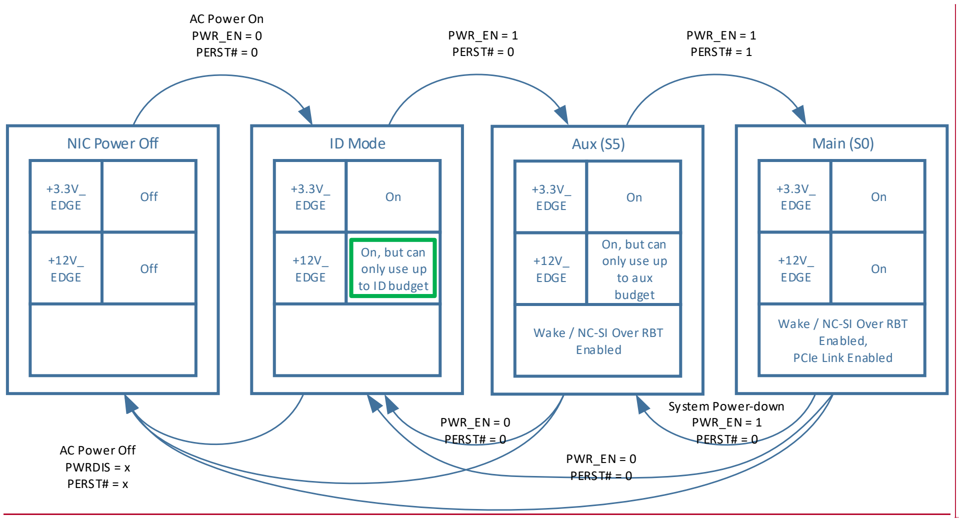


Table 38: Power States

Power State	~~PWRDIS~~PWR_EN	PERSTn	FRU	Scan Chain	WAKEn	RBT Link	PCIe Link	+3.3V_EDGE	+12V_EDGE
NIC Power Off	Invalid / Don't Care	Invalid / Don't Care							
ID Mode	~~High~~Low	Low	X	X				X	X
Aux Power Mode (S5)	~~Low~~High	Low	X	X	X	X		X	X
Main Power Mode (S0)	~~Low~~High	High	X	X	X	X	X	X	X

3.9.1 NIC Power Off

In NIC power off mode, all power delivery has been turned off or disconnected from the baseboard. Transition to this state can be from any other state.

3.9.2 ID Mode

In the ID Mode, only +3.3V_EDGE is available for powering up management only functions. FRU and scan chain accesses are only allowed in this mode. The +12V_EDGE rail is not intended to be used in ID Mode, however leakage current may be present. The max leakage is defined in Section 3.10. An OCP NIC 3.0 card shall transition to this mode when ~~PWRDIS~~PWR_EN=~~1~~ 0 and PERST#=0.

Commented [CP29]: Why do we turn on the 12V rail in ID mode(when PWRDIS is high)? We can live with having only 3.3AUX rail powering the FRU and scan chain. And the 12V should be blocked to the AIC by PWRDIS signal, like what's been described in section 3.9.2

Commented [NT30R29]: +12V is available up to the budget value due to leakage. It's not actually used in this state. The working group was OK with this value.

3.9.3 Aux Power Mode (S5)

In Aux Power Mode provides both +3.3V_EDGE as well as +12V_EDGE is available. +12V_EDGE in Aux mode may be used to deliver power to the OCP NIC 3.0 card, but only up to the Aux mode budget as defined in Table 39. An OCP NIC 3.0 card shall transition to this mode when ~~PWRDIS~~PWR_EN=~~0~~ 1 and PERST#=0.

3.9.4 Main Power Mode (S0)

In Main Power Mode provides both +3.3V_EDGE and +12V_EDGE across the OCP connector. The OCP NIC 3.0 card operates in full capacity. Up to 80W may be delivered on +12V_EDGE for a Small Card and up to 150W for a Large Card~~,~~. Additionally, up to~~and~~ 3.63W is delivered on each ~~the~~ +3.3V_EDGE pins. An OCP NIC 3.0 card shall transition to this mode when ~~PWRDIS~~PWR_EN=~~0~~ 1 and PERST#=1.

3.10 Power Supply Rail Requirements and Slot Power Envelopes

The baseboard provides +3.3V_EDGE and +12V_EDGE to both the Primary and Secondary Connectors. The rail requirements are leveraged from the PCIe CEM 4.0 specification. For OCP NIC 3.0 cards, the requirements are as follows:

Table 39: Baseboard Power Supply Rail Requirements – Slot Power Envelopes

Power Rail	**15W Slot Small Card Hot Aisle**	**25W Slot Small Card Hot Aisle**	**35W Slot Small Card Hot Aisle**	**80W Slot Small Card Cold Aisle**	**150W Large Card Cold Aisle**
+3.3V_EDGE					
Voltage Tolerance	±9% (max)	±9% (max)	±9% (max)	±9% (max)	±9% (max)
Supply Current					
ID Mode	375mA (max)	375mA (max)	375mA (max)	375mA (max)	375mA (max)
Aux Mode	1.1A (max)	1.1A (max)	1.1A (max)	1.1A (max)	2.2A (max)
Main Mode	1.1A (max)	1.1A (max)	1.1A (max)	1.1A (max)	2.2A (max)
Capacitive Load	150µF (max)	150µF (max)	150µF (max)	150µF (max)	300µF (max)
+12V_EDGE					
Voltage Tolerance	±8% (max)	±8% (max)	±8% (max)	±8% (max)	±8% (max)
Supply Current					
ID Mode	100mA (max)	100mA (max)	100mA (max)	100mA (max)	100mA (max)
Aux Mode	0.7A (max)	1.1A (max)	1.5A (max)	3.3A (max)	6.3A (max)
Main Mode	1.25A (max)	2.1A (max)	2.9A (max)	6.6A (max)	12.5A (max)
Capacitive Load	500µF (max)	500µF (max)	1000µF (max)	1000µF (max)	2000µF (max)

Note: While cards may draw up to the published power ratings, the baseboard vendor shall evaluate its cooling capacity for each slot power envelope. Additionally, the baseboard shall advertise its slot power limits to aid in the overall board power budget allocation to prevent a high power card from being enabled in a lower power class slot.

3.11 Hot Swap Considerations for +12V_EDGE and +3.3V_EDGE Rails

For baseboards that support system hot (powered on) OCP NIC 3.0 card insertions and extractions, the system implementer shall consider the use of hotswap controllers on both the +12V_EDGE and +3.3V_EDGE pins to prevent damage to the baseboard or the OCP NIC 3.0 card. Hotswap controllers help with in-rush current limiting while also providing overcurrent protection, undervoltage and overvoltage protection capabilities.

The hotswap controller may gate the +12V_EDGE and +3.3V_EDGE based on the PRSNTB[3:0]# value. Per Section 3.6.3, a card is present in the system when the encoded value is not 0b1111. The PRSNTB[3:0]# may be AND'ed together and connected to the hotswap controller to accomplish this

Commented [CP31]: Do we want to specify the PCIE "Slot Power Limit Control" mechanism to avoid an overdrawing device? Looks like now a Small Card slot has to support up to 80W. How do we prevent users from installing a 80W card into a 30W slot if we do not have the power negotiation mechanism? considering to avoid extra cost on platform side Fuse and crowbar circuit.

Commented [NT32R31]: The baseboard will have knowledge of it's slot power limit. Per the last two tables in the FRU EEPROM section, there are provisions for max power in Aux and in main modes. Is this sufficient?

I can add text "the baseboard shall advertise it's slot power limits to aid in overall board budget allocation" (or similar text)

Commented [NT33]: 500uF/500uF/1000uF/1000uF/2000uF. Tentative. Waiting for recommended values from system vendors.

Commented [CP34]: Do we still plan to put in some basic protection mechanism (either ME or TVS) to prevent system damage from undesired user hot-swap?

Commented [TN35R34]: Snippet from e-mail conversation:

Section 3.11 –
<PC> This will be provided this week from our power experts.
Josh, The need of ME protection mechanism to avoid unwanted hot-swaps on unsupported servers should also be discussed. Had this topic been brought up in the ME sessions yet?
JH 1/16 – We haven't discussed in that meeting; I have discussed with Jia in detail though. We have two versions of faceplates for W1, one that's tool-less and one that has a thumbscrew. The thumbscrew version does have some added 'inconvenience' to dissuade users from doing this. HPE ME's appear solely focused on the thumbscrew version. We have no space to add additional mechanism to do this more actively. In my experience this will occur no matter the amount of barriers you put in place, the HW must be able to do this without sustaining damage. In my past systems such an event would require system power cycle for recovery.

result. Per the OCP NIC 3.0 mechanical definition (Section 3.1.1), the present pins are short pins and engage only when the card is positively seated.

Baseboards that do not support hot insertion, or hot extractions may opt to not implement these features.

3.12 Power Sequence Timing Requirements

The following figure shows the power sequence of PRSNTB[3:0]#, +3.3V_EDGE, +12V_EDGE relative to ~~PWRDIS~~PWR_EN, BIF[2:0]#, PERSTn*, the OCP NIC 3.0 card power ramp and NIC_PWR_GOOD. Please refer to Section 3.5.4 for the NIC_PWR_GOOD definition.

Figure 84: Power-Up Sequencing

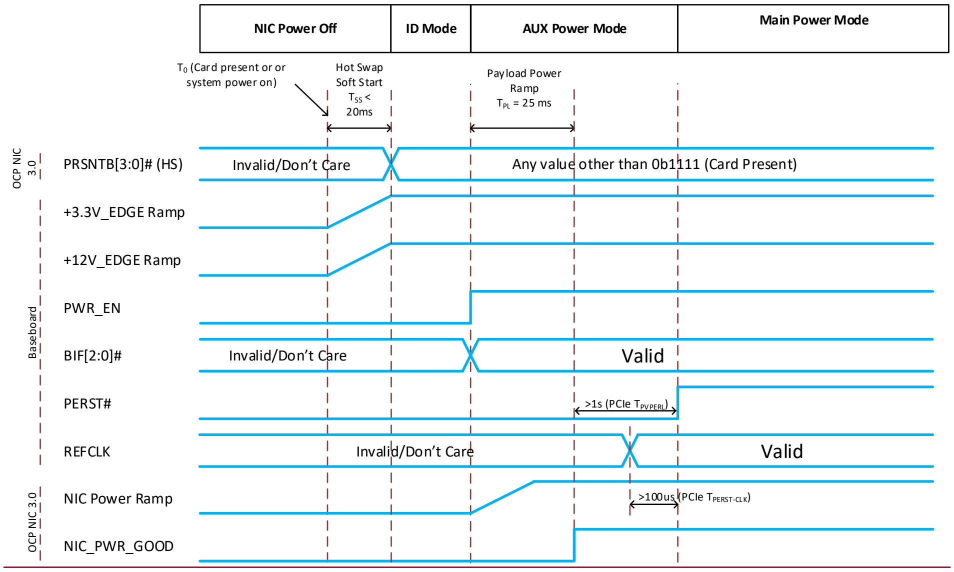
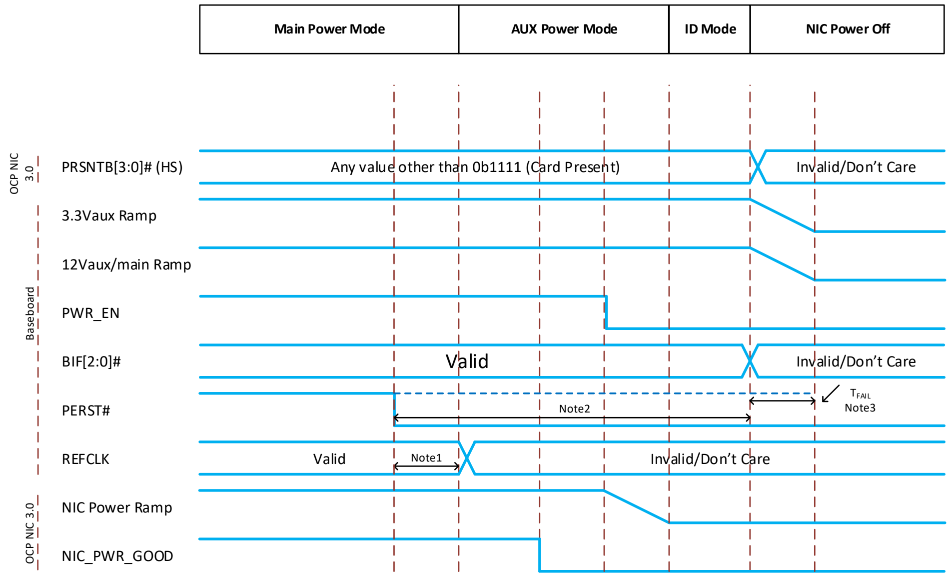


Figure 85: Power-Down Sequencing



Note1: REFCLK go inactive after PERST# goes active.
Note2: PEREST# goes active before the power on the connector is removed.
Note3: In the case of a surprise power down, PERST# goes active TFAIL after power is no longer stable.

Table 40: Power Sequencing Parameters

Parameter	Value	Units	Description
T_{SS}	20	ms	Max time between system +3.3V_EDGE and +12V_EDGE ramp to power stable.
T_{PL}	<25	ms	Max time between the ~~NIC payload power ramp~~ PWR_EN assertion to NIC_PWR_GOOD assertion.
T_{PVPERL}	>1	s	~~Max~~ Minimum time between ~~PWRDIS~~ NIC_PWR_GOOD ~~de~~assertion and PERST# deassertion. For OCP NIC 3.0 applications, this value is >1 second. This is longer than the minimum value specified ~~from~~ in the PCIe CEM Specification, Rev 4.0.
$T_{PERST\text{-}CLK}$	>100	µs	~~Max~~ Min Time REFCLK is stable before PERST# inactive
T_{FAIL}	<500	ns	In the case of a surprise power down, PERST# goes active T_{FAIL} after power is no longer stable.

Commented [TN36]: Yuval recommends 1second for this value to allow secure boot

Need to update this in the power up sequencing diagram.

4 Management and Pre-OS Requirements

OCP NIC 3.0 card management is an important aspect to overall system management. This section specifies a common set of management requirements for OCP NIC 3.0 implementations. There are three types of implementations (RBT+MCTP Type, RBT Type, and MCTP Type) depending on the physical sideband management interfaces, transports, and traffic supported over different transports. An OCP NIC 3.0 implementation shall support at least one type of implementation for card management. For a given type of implementation, an OCP NIC 3.0 card shall support type specific requirements described in Sections 4.1 through 4.7.

Commented [HS37]: Pat will send Hemal definition of each term here. Change MCTP to MCTP/SMBus Type.

4.1 Sideband Management Interface and Transport

OCP NIC 3.0 sideband management interfaces are used by a Management Controller (MC) or Baseboard Management Controller (BMC) to communicate with the NIC. Table 41 summarizes the sideband management interface and transport requirements.

Table 41: Sideband Management Interface and Transport Requirements

Requirement	**RBT+MCTP Type**	**RBT Type**	**MCTP Type**
NC-SI 1.1 compliant RMII Based Transport (RBT) including physical interface defined in Section 10 of DMTF DSP0222	Required	Required	N/A
I^{2}C compliant physical interface for FRU EEPROM	Required	Required	Required
SMBus 2.0 compliant physical interface	Required	N/A	Required
Management Component Transport Protocol (MCTP) Base 1.3 (DSP0236 1.3 compliant) over MCTP/SMBus Binding (DSP0237 1.1 compliant)	Required	N/A	Required
PCIe VDM compliant physical interface	Optional	Optional	Optional
Management Component Transport Protocol (MCTP) Base 1.3 (DSP0236 1.3 compliant) over MCTP/PCIe VDM Binding (DSP0238 1.0 compliant)	Optional	Optional	Optional

4.2 NC-SI Traffic

DMTF DSP0222 defines two types of NC-SI traffic: Pass-Through and Control. Table 42 summarizes the NC-SI traffic requirements.

Table 42: NC-SI Traffic Requirements

Requirement	**RBT+MCTP Type**	**RBT Type**	**MCTP Type**
NC-SI Control over RBT (DMTF DSP0222 1.1 or later compliant)	Required	Required	N/A
NC-SI Control over MCTP (DMTF DSP0261 1.2 compliant)	Required	N/A	Required
NC-SI Pass-Through over RBT (DMTF DSP0222 1.1 compliant)	Required	Required	N/A
NC-SI Pass-Through over MCTP (DMTF DSP0261 1.2 compliant)	Optional	N/A	Optional

Note: A Management Controller (MC) is allowed to use NC-SI Control traffic only without enabling NC-SI pass-through.

4.3 Management Controller (MC) MAC Address Provisioning

An OCP NIC 3.0 compliant card that supports NC-SI pass-through shall provision one or more MAC addresses for Out-Of-Band (OOB) management traffic. The number of MC MAC addresses provisioned is implementation dependent. These MAC addresses are not exposed to the host(s) as available MAC addresses. The MC is not required to use these provisioned MAC addresses. Table 43 summarizes the MC MAC address provisioning requirements.

Table 43: MC MAC Address Provisioning Requirements

Requirement	**RBT+MCTP Type**	**RBT Type**	**MCTP Type**
One or more MAC Addresses shall be provisioned for the MC. The OCP NIC 3.0 platform may use the NIC vendor allocated MAC addresses for the BMC. Each management channel requires a dedicated MAC address. Some platforms may employ multiple BMCs (or virtual BMCs) each with a dedicated MAC address. The NIC may also support multiple partitions on a physical port. The recommended MAC address allocation scheme is stated below. Assumptions: 1. The number of BMCs or virtual BMCs is the same as the number of hosts (1:1 relationship between each host and the BMC). 2. The maximum number of partitions on each port is the same. Variables: • `num_ports` – Number of Ports on the OCP NIC 3.0 card • `max_parts` – Maximum number of partitions on a port • `num_hosts` – Number of hosts supported by the NIC • `first_addr` – The MAC address of the first port on the first host for the first partition on that port • `host_addr[i]` – base MAC address of ith host (`0 ≤ i ≤ num_hosts-1`) • `bmc_addr[i]` – base MAC address of ith BMC (`0 ≤ i ≤ num_hosts-1`)	Required	Required	Optional

Formulae: • host_addr[i] = first_addr + i*num_ports*(max_parts+1) • The assignment of MAC address used by i^{th} host on port j for the partition k is out of the scope of this specification. • bmc_addr[i] = host_addr[i] + num_ports*max_parts • The MAC address used by i^{th} BMC on port j, where 0 ≤ i ≤ num_hosts-1 and 0 ≤ j ≤ num_ports -1 is bmc_addr[i] + j			
Support at least one of the following mechanism for provisioned MC MAC Address retrieval: • NC-SI Control/RBT (DMTF DSP0222 1.1 or later compliant) Note: This capability is planned to be included in revision 1.2 of the NC-SI specification. • NC-SI Control/MCTP (DMTF DSP0261 1.2 compliant)	Required	Required	Optional

4.4 Temperature Reporting

An OCP NIC 3.0 implementation can have several silicon components including one or more ASICs implementing NIC functions and one or more transceiver modules providing physical network media connectivity. For the system management, it is important that temperatures of these components can be retrieved over sideband interfaces.

The temperature reporting interface shall be accessible in Aux Power Mode (S5), and Main Power Mode (S0). Table 44 summarizes temperature reporting requirements. These requirements improve the system thermal management and allow the baseboard management device to access key component temperatures on an OCP NIC 3.0 card. When the temperature reporting function is implemented, it is recommended that the temperature reporting accuracy is within ±3°C.

Table 44: Temperature Reporting Requirements

Requirement	RBT+MCTP Type	RBT Type	MCTP Type
Component Temperature Reporting for a component with TDP ≥8W	Required	Required	Required
Component Temperature Reporting for a component with TDP <8W	Recommended	Recommended	Recommended
When the temperature sensor reporting function is implemented, the OCP NIC 3.0 card shall PLDM for Platform Monitoring and Control (DSP0248 1.1 compliant) for temperature reporting.	Required	Required	Required
~~When the temperature sensor reporting function is implemented, the temperature reporting accuracy on the card shall be within ±3°C.~~	~~Required~~	~~Required~~	~~Required~~

Commented [JN38]: Other than Temperature, is there other information in transceiver may be extracted? Such as serial number / Serdes settings?

Commented [NT39R38]: Per Jia – deferring this comment as it will not be addressed in the v0.70 release.

Commented [CR40]: Section 4 (or anywhere else) does not define a place for the card to report the sensor maximum or target for closed loop fan control - this needs to be defined for the

Commented [CR41]: Section 4.4 does not define where/how the card should report a maximum for sensors that report temperature. This is required in order for systems to implement closed loop control.

When the temperature sensor reporting function is implemented, r~~R~~eporting of upper-warning, upper-critical, and upper-fatal thresholds for PLDM numeric sensors~~ for temperature reporting~~. Note: For definitions of the upper-warning, upper-critical, and upper-fatal thresholds, refer to DSP0248 1.1.	Required	Required	Required
When the temperature ~~sensor~~ reporting function is implemented using PLDM numeric sensors, the temperature ~~reporting accuracy~~ tolerance ~~on the card shall be within ±3°C~~shall be reported.	Required	Required	Required
Support for NIC self-shutdown. The purpose of this feature is to “self-protect” the NIC from permanent damage due to high operating temperature experienced by the NIC. The NIC shall monitor its temperature and shut-down itself as soon as the threshold value is reached. The value of the self-shutdown threshold is implementation specific. It is recommended that the self-shutdown threshold value is higher than the maximum junction temperature of the ASIC implementing the NIC function and this value is ~~. The self-shutdown threshold value shall be~~ between the critical and fatal temperature thresholds. Note: It is assumed that a system management function will prevent a component from reaching its fatal threshold temperature. The OCP NIC 3.0 card does not need to know the reason for the self-shutdown threshold crossing (e.g. fan failure). After entering the self-shutdown state, the OCP NIC 3.0 card is not required to be operational. This might cause the system with the OCP NIC 3.0 card to become unreachable via the NIC. An AC power cycle of the system may be required to bring the NIC back to an operational state. In order to recover the NIC from the self-shutdown state, the OCP NIC 3.0 card should go through the NIC power off state as described in Section 3.9.1.	Required	Required	Required
~~Report self-shutdown temperature threshold using PLDM for platform monitoring and control (DSP0248 1.1 compliant)~~	~~Required~~	~~Required~~	~~Required~~

4.5 Power Consumption Reporting

An OCP NIC 3.0 implementation may be able to report the power consumed by one or more component implementing NIC functions. It is important for the system management that the information about the power consumption can be retrieved over sideband interfaces. Table 45 summarizes power consumption reporting requirements.

Table 45: Power Consumption Reporting Requirements

Requirement	**RBT+MCTP Type**	**RBT Type**	**MCTP Type**
Component Estimated Power Consumption Reporting	Required	Required	Required
Component Runtime Power Consumption Reporting	Optional	Optional	Optional
PLDM for Platform Monitoring and Control (DSP0248 1.1 compliant) for component power consumption reporting	Required	Required	Required

4.6 Pluggable Transceiver Module Status and Temperature Reporting

Pluggable modules like an optical module or a direct attached copper cable is used to connect an OCP NIC to a physical medium. It is important to know the presence of pluggable modules and information about insertion/deletion of pluggable modules. Table 46 summarizes pluggable module status reporting requirements.

Commented [HS42]: Hemal to work with Jon Lewis to refine this definition.

Table 46: Pluggable Module Status Reporting Requirements

Requirement	**RBT+MCTP Type**	**RBT Type**	**MCTP Type**
Pluggable Transceiver modules Presence Status and Temperature Reporting	Required	Required	Required
PLDM for Platform Monitoring and Control (DSP0248 1.1 compliant) for reporting the pluggable transceiver module presence status and pluggable transceiver module temperature	Required	Required	Required

4.7 Management and Pre-OS Firmware Inventory and Update

An OCP NIC 3.0 implementation can have different types of firmware components for data path, control path, and management path operations. It is desirable that OCP NIC 3.0 implementations support an OS-independent ~~Out-Of-Band~~ mechanism for the management firmware update. It is desirable that the management firmware update does not require a system reboot for the new firmware image to become active. Table 47 summarizes the firmware inventory and update requirements.

Table 47: Management and Pre-OS Firmware Inventory and Update Requirements

Requirement	**RBT+MCTP Type**	**RBT Type**	**MCTP Type**
Network boot in UEFI driver (supporting both IPv4 and IPv6 addressing for network boot)	Required	Required	Required
UEFI secure boot for UEFI drivers	Required	Required	Required
UEFI secure firmware update	Required	Required	Required
PLDM for Firmware Update (DSP0267 1.0 compliant)	Required	Recommended	Required

4.7.1 Secure Firmware

It is highly recommended that an OCP NIC 3.0 card supports a secure firmware feature. In the future versions of the OCP NIC 3.0 specification, the secure firmware feature is intended to be required. When the secure firmware feature is enabled and where export compliance permits, the OCP NIC 3.0 card shall verify firmware components prior to the execution, execute only signed and verified firmware components, and only allow authenticated firmware updates. Where applicable, an OCP NIC 3.0 implementation shall use the guidelines provided in NIST SP 800-193 (draft) Platform Resiliency Guidelines for the following secure firmware functions:

- Signed Firmware Updates
    - Ensure only valid/authenticated firmware updates can be applied. Refer to: NIST 800-193 Section 3.5 Firmware Update Mechanisms, and 4.1.2 Root of Trust for Update (RTU) and Chain of Trust for Update (CTU)
    - Ensure authentication mechanisms cannot be bypassed. Refer to NIST 800-193 Section 4.2 Protection.
- Secure Boot
    - Only boot trusted/authenticated firmware: NIST 800-193 4.1.3 Root of Trust for Detection (RTD) and Chain of Trust for Detection (CTD), and Section 4.3 Detection
    - Recovery mechanism in case of boot failure: NIST 800-193 Section 4.4 Recovery

4.7.2 Firmware Inventory

The OCP NIC 3.0 card shall allow queries to obtain the firmware component versions, device model, and device ID via in-band and out-of-band interfaces without impacting NIC function and performance of said paths.

4.7.3 Firmware Inventory and Update in Multi-Host Environments

A multi-host capable OCP NIC 3.0 card shall gracefully handle concurrent in-band queries from multiple hosts and out-of-band access from the BMC for firmware component versions, device model, and device ID information.

A multi-host capable OCP NIC 3.0 card shall only permit one entity to perform write accesses to NIC firmware at a time, without creating contention.

A multi-host capable OCP NIC 3.0 card shall gracefully handle exceptions when more than one entity attempts to perform concurrent NIC firmware writes.

4.8 NC-SI Package Addressing and Hardware Arbitration Requirements

NC-SI over RBT is implemented via RMII pins between the MC and the OCP NIC 3.0 card. Protocol and implementation details of NC-SI over RBT can be found in the DMTF DSP0222 standard.

4.8.1 NC-SI over RBT Package Addressing

NC-SI over RBT capable OCP NIC 3.0 cards shall use a unique Package ID per ASIC when multiple ASICs share the single NC-SI physical interconnect to ensure there are no addressing conflicts.

Baseboards use the Slot_ID pin on the Primary Connector for this identification. The Slot_ID value may be directly connected to GND (Slot ID = 0), or pulled up to +3.3V_EDGE (Slot ID = 1).

Package ID[2:0] is a 3-bit field and is encoded in the NC-SI Channel ID as bits [7:5]. Package ID[2] defaults to 0b0 in the NC-SI specification, but is optionally configurable if the target silicon supports configuring this bit. Package ID[1] is directly connected to the SLOT_ID pin. Package ID[0] is set to 0b0 for Network Controller ASIC #0. For an OCP NIC 3.0 card with two discrete silicon instances, Package ID[0] shall be set to 0b1 for Network Controller ASIC #1. Refer to the specific endpoint device datasheet for details on the Package ID configuration options.

Up to four silicon devices are supported on the bus if only Package ID[1:0] is configurable (e.g. Package ID[2] is statically set to 0b0). Up to eight silicon devices are supported on the NC-SI bus if Package ID[2:0] are all configurable.

Refer to the DMTF DSP0222 standard for more information on package addressing, Slot ID and Package ID.

4.8.2 Arbitration Ring Connections

For baseboards that implement two or more Primary Connectors, the NC-SI over RBT arbitration ring may be connected to each other. The arbitration ring shall support operation with a one card, or both cards installed. Figure 73 shows an example connection with dual Primary Connectors.

4.9 SMBus 2.0 Addressing Requirements

The SMBus provides a low speed management bus for the OCP NIC 3.0 card. The FRU EEPROM and on-board temperature sensors are connected on this bus. Additionally, network controllers may utilize the SMBus interface for MCTP communications. Proper power domain isolation shall be implemented on the NIC.

4.9.1 SMBus Address Map

OCP NIC 3.0 cards shall support SMBus ARP (be ARP-capable) to allow the cards to be dynamically assigned addresses for MCTP communications to avoid address conflicts and eliminate the need for manual configuration of addresses. The address type of dynamic addresses can be either dynamic and persistent address device or dynamic and volatile address device. Refer to SMBus 2.0 specification and Section 6.11 of DSP0237 1.1 for details on SMBus address assignment.

Commented [HS43]: Pat will send Hemal text to differentiate dynamic persistent and dynamic non-persistent. Add a reference to the SMBus address table from DSP0237 1.1.

A system implementation may choose to only use fixed addresses for an OCP NIC 3.0 card on the system. The assignment of these fixed addresses is system dependent and outside the scope of this specification. When fixed addresses are assigned to OCP NIC 3.0 card, then the OCP NIC 3.0 card shall be a fixed and discoverable SMBus device. Refer to SMBus 2.0 specification for more details.

All predefined SMBus addresses for OCP NIC 3.0 are shown in Table 48. Baseboard and OCP NIC 3.0 card designers must ensure additional devices do not conflict. The addresses shown are in 8-bit format and represent the read/write address pair.

Table 48: SMBus Address Map

Address (8-bit)	Device	Notes
0xA0 / 0xA1 – SLOT0 0xA2 / 0xA3 – SLOT1	EEPROM	On-board FRU EEPROM. Mandatory. Powered from Aux power domain. The EEPROM ADDR0 pin shall be connected to the SLOT_ID pin on the OCP NIC 3.0 card gold finger to allow up to two OCP NIC 3.0 cards to exist on the same I^2C bus.

4.10 FRU EEPROM

Commented [HS44]: Should PLDM for FRU data transfer be specified? Hemal to take a look at PLDM for FRU spec mandatory requirements and optional requirements as they apply to OCP NIC 3.0.

4.10.1 FRU EEPROM Address, Size and Availability

The FRU EEPROM provided for the baseboard to determine the card type and is directly connected to the SMBus on the card edge. Only one EEPROM is required for a single physical OCP NIC 3.0 card regardless of the PCIe width or number of physical card edge connectors it occupies. The FRU EEPROM shall be connected to the Primary Connector SMBus.

The EEPROM is addressable at the addresses indicated in Table 48. The write/read pair is presented in 8-bit format. The size of EEPROM shall be at least 4Kbits for the base EEPROM map. OCP NIC 3.0 card suppliers may use a larger size EEPROM if needed to store vendor specific information.

The FRU EEPROM is readable in all three power states (ID mode, AUX(S5) mode, and MAIN(S0) mode.

4.10.2 FRU EEPROM Content Requirements

The FRU EEPROM shall follow the data format specified in the IPMI Platform Management FRU Information Storage Definition v1.2. Both the Product Info and Board Info records shall be populated in the FRU EEPROM. The OEM record 0xC0 is used to store specific records for the OCP NIC 3.0. For an OCP NIC 3.0 card, the FRU EEPROM OEM record content based on the format defined in Table 49~~Table 49~~ shall be populated.

Commented [HS45]: Need feedback.

Table 49: FRU EEPROM Record – OEM Record 0xC0, Offset 0x00

Offset	Length	Description
0	3	Manufacturer ID, LS Byte first (3 bytes total). For OCP NIC 3.0 compliant cards, the value of this field shall be set to the OCP IANA assigned number. This value is 0x7FA600, LS byte first. (42623 in decimal)
3	1	OCP NIC 3.0 FRU OEM Record Version. For OCP NIC 3.0 cards compliant to this specification, the value of this field shall be set to 1.
4	1	Card Max power (in Watts) in MAIN(S0) mode. Rounded up to the nearest Watt for fractional values.
5	1	Card Max power (in Watts) in AUX(S5) mode. Rounded up to the nearest Watt for fractional values.
6	1	Thermal Reporting Tier 0xFF – Unknown Note: This field will be defined in a companion Thermal Specification for OCP NIC 3.0.
7	1	Airflow Impedance Tier 0xFF – Unknown Note: This field will be defined in a companion Thermal Specification for OCP NIC 3.0.
8:9	2	Reserved for future use. Set to 0xFF for this version of the specification.
10	1	Number of controllers (N).
11:26	16	Controller 1 UDID. MS Byte First (to align the FRU order to the reported UDID order on the SMBus)
…	…	…

11+16*(N-1):16*N+10	16	Controller N UDID. MS Byte First (to align the FRU order to the reported UDID order on the SMBus).

5 Routing Guidelines and Signal Integrity Considerations

5.1 NC-SI Over RBT

For the purposes of this specification, the min and max electrical trace length of the NC-SI signals shall be between 2 inches and 4 inches. The traces shall be implemented as 50 Ohm impedance controlled nets.

5.2 PCIe

This section is a placeholder for the PCIe routing guidelines and SI considerations.

OCP NIC 3.0 card suppliers shall follow the PCIe routing specifications. At this time, the OCP NIC 3.0 subgroup is working to identify and agree to the channel budget for an OCP NIC 3.0 card and leave sufficient margin for the baseboard. Refer to the PCIe CEM and PCIe Base specifications for end-to-end channel signal integrity considerations.

Commented [CP46]: We are expecting more information such as IL/RL/Jitter/Xtalk requirements in this section

Commented [JN47]:
1.Discussion point of 1st draft (define or not define in 1.00?)
2. Anything other than loss and impedance shall be defined to be complete

Commented [TN48]: Point to the PCIe spec for the electrical specs (See PCIe CEM Section 6.3.x. 4.7.x, 4.8) and SFF-TA-1002.

6 Thermal and Environmental

Commented [CP49]: Do we plan to add in the connector envirnmental environmental requirements such as connector gold plating thickness? Similar to what's been defined in the PCIe CEM 3.0 CH 6.4.

6.1 Airflow Direction

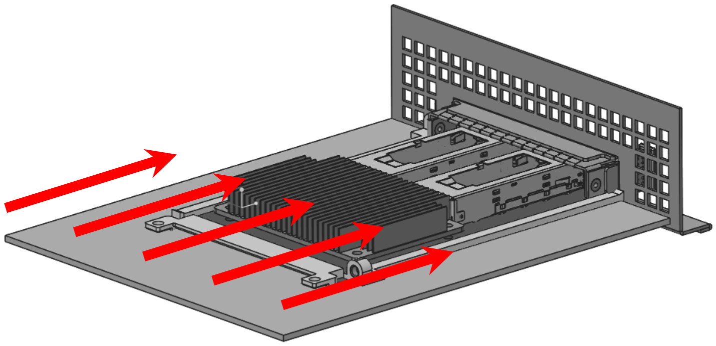
The OCP NIC 3.0 is designed to operate in either of two different airflow directions which are referred to as Hot Aisle and Cold Aisle. In both Hot Aisle and Cold Aisle configurations all airflow is directed over the topside of the card. Component placement must assume that no airflow will exist on the bottom side of the card. The local approach air temperature and speed to the card is dependent on the capability of the system adopting OCP NIC 3.0 card. These parameters may be impacted by the operational altitude and relative humidity in both Hot Aisle or Cold Aisle configuration. Design boundary conditions for Hot Aisle and Cold Aisle cooling are included below in Sections 6.1.1 and 6.1.2 respectively.

The two airflow directions should not result in multiple thermal solutions to separately satisfy the varying thermal boundary conditions. Ideally, any specific OCP NIC 3.0 card design should function in systems with either Hot Aisle or Cold Aisle cooling. Thermal analysis in support of this specification have shown the Hot Aisle configuration to be more challenging than Cold Aisle but card vendors should make that determination for each card that is developed.

6.1.1 Hot Aisle Cooling

The airflow in typical server systems will approach from the card edge or heatsink side of the card. This airflow direction is referred to as Hot Aisle cooling and is illustrated below in Figure 86. The term Hot Aisle refers to the card being located at the rear of the system where the local inlet airflow is preheated by the upstream system components (e.g. HDD, CPU, DIMM, etc.).

Figure 86: Airflow Direction for Hot Aisle Cooling



The boundary conditions for Hot Aisle cooling are shown below in

Table 50 and Table 51. The low temperature is listed at 5°C and assumes fresh air could be ducted to the back of the system from the front. More typically the inlet temperature to the OCP NIC 3.0 card will be in the same range as PCIe cards located at the back of the system – 55°C. Depending on the system design, power density, and airflow the inlet temperature to the OCP NIC 3.0 card may be as high as 60°C or 65°C. The airflow velocities listed in Table 51 represent the airflow velocities typical in mainstream servers. Higher airflow velocities are available within the Hot Aisle cooling tiers listed in Table 55 but card designers must be sure to understand the system level implications of such high card LFM requirements.

Table 50: Hot Aisle Air Temperature Boundary Conditions

	Low	Typical	High	Max
Local Inlet air temperature	5°C (system inlet)	55°C	60°C	65°C

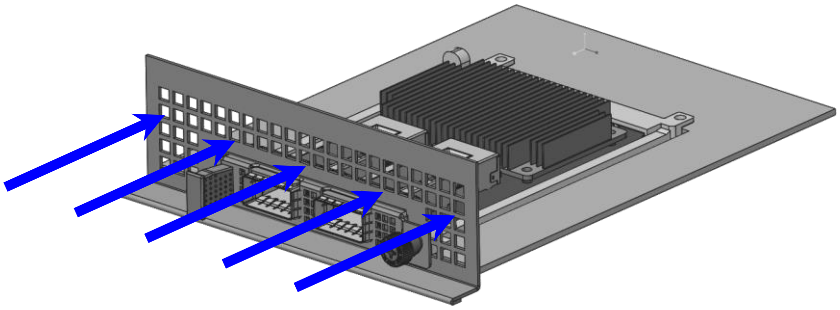
Table 51: Hot Aisle Airflow Boundary Conditions

	Low	Typical	High	Max
Local inlet air velocity	50 LFM	100-200 LFM	300 LFM	System Dependent

6.1.2 Cold Aisle Cooling

When installed in the front of a server the airflow will approach from the I/O connector (e.g. SFP, QSFP or RJ-45) side of the card. This airflow direction is referred to as Cold Aisle cooling and is illustrated below in Figure 87. The term Cold Aisle refers to the card being located at the front of the system where the local inlet airflow is assumed to be the same temperature as the system inlet airflow.

Figure 87: Airflow Direction for Cold Aisle Cooling



The boundary conditions for Cold Aisle cooling are shown below in Table 52 and

Table 53. The temperature values listed in Table 52 assume the inlet temperature to the OCP NIC 3.0 card to be the same as the system inlet. The low, typical, high, and max temperatures listed align with the ASHRAE A1, A2, A3, and A4 environmental classes. Depending on the system, the supported ASHRAE class may be limit the maximum temperature to the OCP 3.0 NIC card. However, for more broad industry support, cards should be designed to the upper end of the ASHRAE classes (i.e. A4).

Table 52: Cold Aisle Air Temperature Boundary Conditions

	Low	Typical	High	Max
Local Inlet Air Temperature	5°C	25-35°C ASHRAE A1/A2	40°C ASHRAE A3	45°C ASHRAE A4

Table 53: Cold Aisle Airflow Boundary Conditions

	Low	Typical	High	Max
Local Inlet Air Velocity	50 LFM	100 LFM	200 LFM	System Dependent

6.2 Design Guidelines

The information in this section is intended to serve as a quick reference guide for OCP NIC 3.0 designers early in the design process. The information should be used as a reference for upfront thermal design and feasibility and should not replace detailed card thermal design analysis. The actual cooling capability of the card shall be defined based on the testing with the OCP NIC 3.0 thermal test fixture documentation in Section 6.4.

6.2.1 ASIC Cooling – Hot Aisle

The ASIC or controller chip is typically the highest power consumer on the card. Thus, as OCP NIC 3.0 cards are developed it is important to understand the ASIC cooling capability.

Figure 88 below provides an estimate of the maximum ASIC power that can be supported as a function of the local inlet velocity for the small card form factor. Each curve in

Figure 88 represents a different local inlet air temperature from 45°C to 65°C.

The curves shown in

Figure 88 were obtained using CFD analysis of a reference OCP NIC 3.0 small form factor card. The reference card has a 20mm x 20mm ASIC with two QSFP connectors. Figure 89 shows a comparison of the 3D CAD and CFD model geometry for the reference OCP NIC 3.0 card. Additional card geometry parameters and boundary conditions used in the reference CFD analysis are summarized in

Table 54. The OCP NIC 3.0 simulation was conducted within a virtual version of the test fixture defined in Section 6.4

An increase in the supported ASIC power or a decrease in the required airflow velocity may be achieved through heatsink size and material changes. For example, a larger heatsink or a heatsink made out of copper could improve ASIC cooling and effectively shift up the supportable power curves shown in

Figure 88.

Figure 88: ASIC Supportable Power for Hot Aisle Cooling – Small Card Form Factor

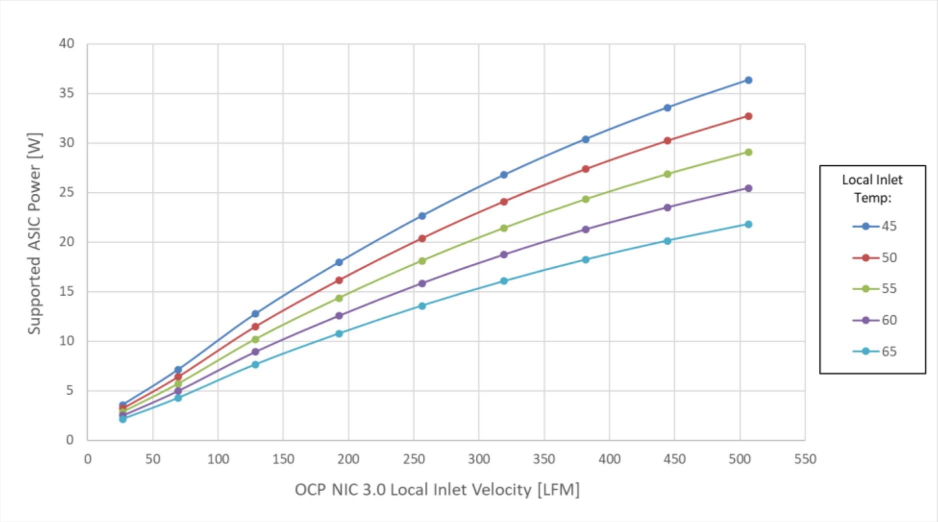


Figure 89: OCP NIC 3.0 Reference Geometry CAD & CFD

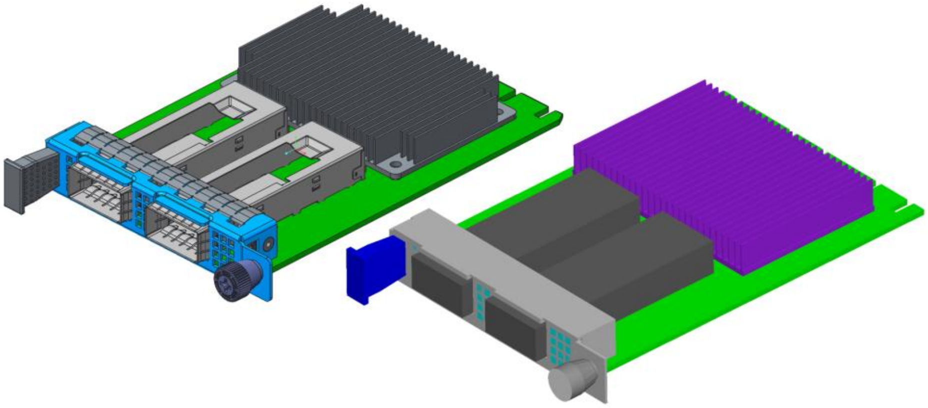


Table 54: Reference OCP NIC 3.0 Small Card Geometry

OCP NIC 3.0 Form Factor	Small Card
Heatsink Width	65mm
Heatsink Length	54mm
Heatsink Height	9.24mm
Heatsink Base Thickness	1.5mm
Fin Count/Thickness	28/0.5mm
Heatsink Material	Extruded Aluminum
ASIC Width	20
ASIC Length	20
ASIC Height	2.26
ASIC Theta-JC	0.17 C/W
ASIC Theta-JB	10 C/W
OCP PCB In-Plane Conductivity	34 W/mK
OCP PCB Normal Conductivity	0.33 W/mK
ASIC Max T-case	95°C
OCP NIC 3.0 I/O Connectors	Two QSFP @ 3.5W each

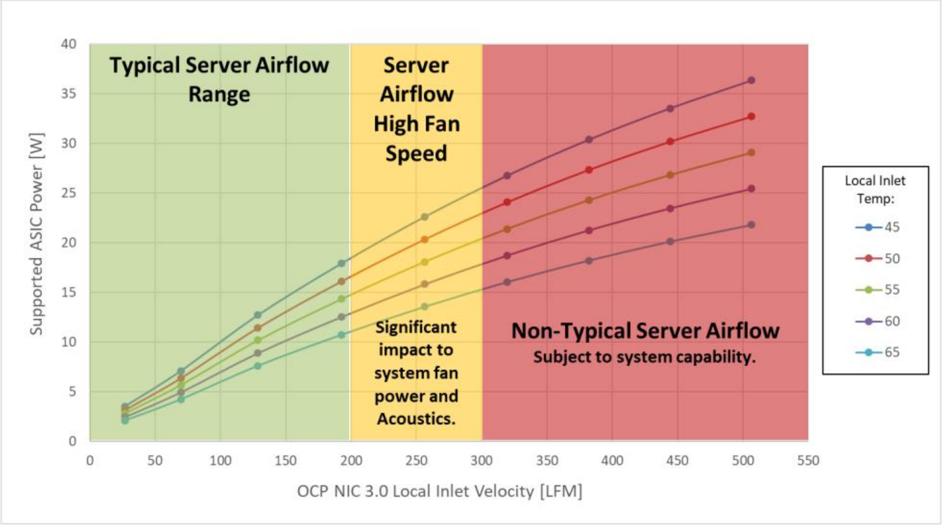
It is important to point out that the curves shown in

Figure 88 represent only the maximum ASIC power that can be supported vs. the supplied inlet velocity. Other heat loads on the card may require airflow velocities above and beyond that required to cool the ASIC. SFP or QSFP optical transceivers located downstream of the AISC will in many cases pose a greater cooling challenge than the ASIC cooling. Cooling the optical transceivers becomes even more difficult as the ASIC power is increased due to additional preheating of the air as it moves through the ASIC heatsink. OCP NIC 3.0 designers must consider all heat sources early in the design process to ensure the card thermal solution is sufficient for the feature set.

Card designers must also consider the airflow capability of the server systems that the cards are targeted for use within.

Figure 90 below shows the ASIC supportable power curves with an overlay of three server airflow capability ranges. Designers must ensure that their thermal solutions and resulting card airflow requirements fall within the range of supportable system airflow velocity. Cards that are under-designed (e.g. require airflow greater than the system capability) will have thermal issues when deployed into the server system. Card designers are advised to work closely with system vendors to ensure they target the appropriate airflow and temperature boundary conditions.

Figure 90: Server System Airflow Capability – Hot Aisle Cooling



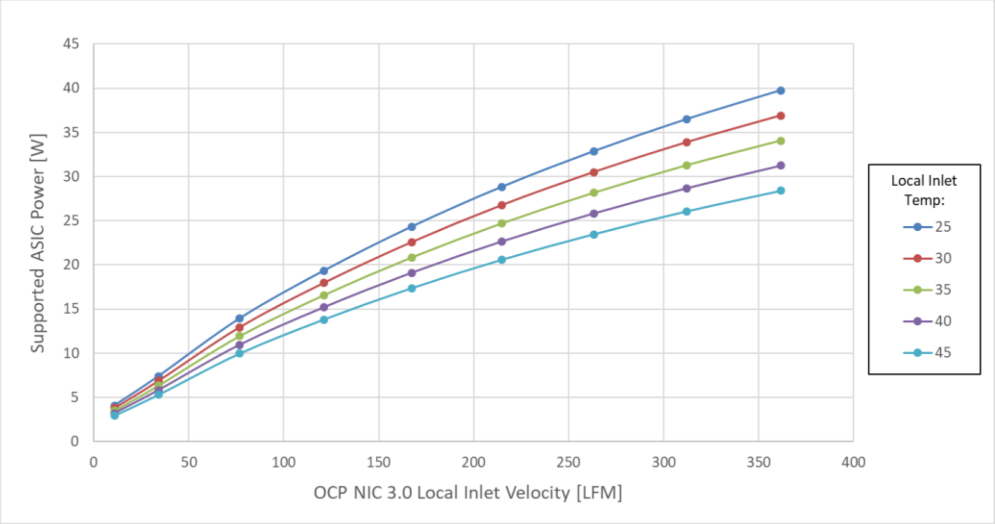
6.2.2 ASIC Cooling – Cold Aisle

Compared to the Hot Aisle cooling there are several key differences for Cold Aisle ASIC cooling. With Cold Aisle cooling the airflow is pulled from the I/O connector side of the card. The I/O connectors and faceplate venting may affect the airflow through the ASIC heatsink. The I/O connectors may also preheat the airflow by some amount. In a Cold Aisle cooling configuration, other parallel airflow paths may result in less airflow passing over and through the OCP NIC 3.0 card compared to the Hot Aisle. The ASIC cooling analysis for Cold Aisle was conducted utilizing the same geometry and boundary conditions described in Figure 89 and

Table 54 with airflow moving from I/O connector to ASIC (opposite to the Hot Aisle analysis).

Figure 91 below shows the results of this analysis for the Cold Aisle cooling configuration. Each curve in Figure 91 represents a different system inlet air temperature from 25°C to 45°C.

Figure 91: ASIC Supportable Power for Cold Aisle Cooling – Small Card Form Factor

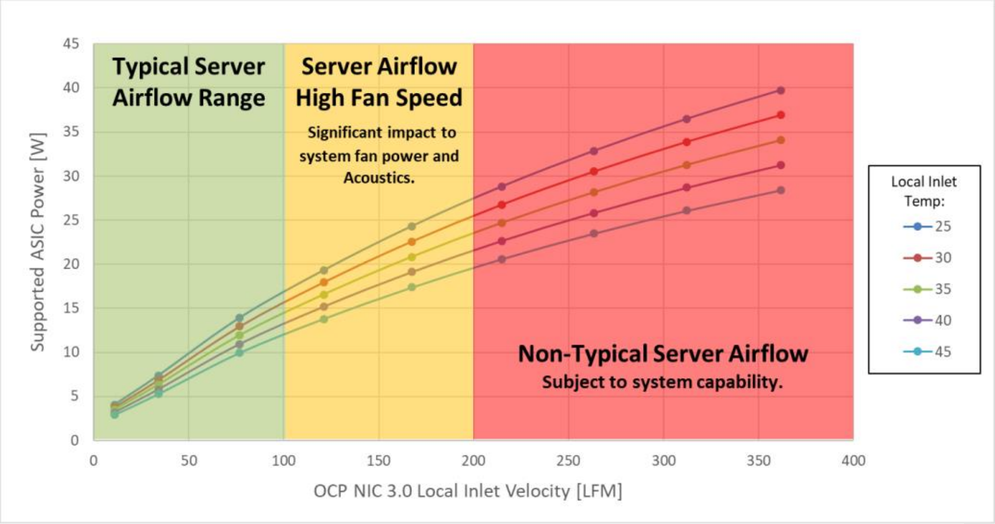


Similar to

Figure 90 for Hot Aisle cooling,

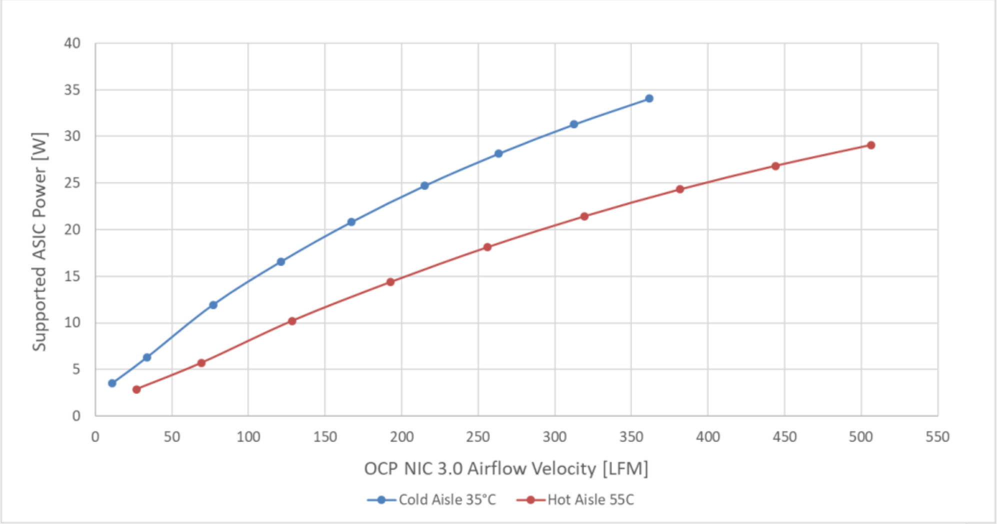
Figure 92 below shows the ASIC supportable power curves with an overlay of three Cold Aisle server airflow capability ranges. Designers must ensure that their thermal solutions and resulting card airflow requirements fall within the range of supportable Cold Aisle system airflow velocity. Cards that are under-designed (e.g. require airflow greater than the system capability) will have thermal issues when deployed into the server system. Card designers are advised to work closely with system vendors to ensure they target the appropriate airflow and temperature boundary conditions for both Hot and Cold Aisle cooling.

Figure 92: Server System Airflow Capability – Cold Aisle Cooling



A comparison of Hot Aisle (55°C) and Cold Aisle (35°C) ASIC cooling capability curves is shown below in Figure 93. The comparison shows the Hot Aisle ASIC cooling capability at 12W at 150LFM while the cold Aisle cooling capability shows support for 19W at 150LFM. In general, based on the reference geometry, the Cold Aisle cooling configuration allows for higher supported ASIC power at lower velocities due primarily to the lower inlet temperatures local to the OCP NIC 3.0 card when in the Cold Aisle cooling configuration.

Figure 93: ASIC Supportable Power Comparison – Small Card Form Factor



6.3 Thermal Simulation (CFD) Modeling

Thermal simulation of OCP NIC 3.0 cards using CFD is recommended. The information that follows includes details of the geometry that should be used for CFD modeling of the OCP NIC 3.0 Small form factor. The geometry described below was developed to ensure consistency across card vendors when analyzing the card cooling and thermal solution. The geometry to be used for CFD analysis is based on the OCP NIC 3.0 thermal test fixture detailed in Section 6.4.

6.3.1 CFD Geometry – Small Card

The geometry to be used for CFD analysis is defined by the following parameters:

- Sheet metal enclosure
- Internal width: 128mm
- Internal height: 40.6mm
- Internal length: 256.7mm

Fixture Faceplate Open Area Ratio: 25% (as shown in

- Figure 94)
- Internal height between top side of board and fixture cover: 34.94mm
- OCP Card is centered on the width of the host PCB.
- Inlet temperature boundary condition: desired approach temperature, e.g. 55°C
- Airflow boundary condition: Desired volume flow in the range of 1 to 20 CFM
- OCP NIC 3.0 local velocity monitor:
- Hot Aisle Cooling – monitor plane 25mm upstream from ASIC heatsink

- Cold Aisle Cooling – monitor planes upstream and downstream of ASIC heatsink depending on I/O connector proximity to ASIC heatsink.

CAD step files for the Hot Aisle CFD geometry are available for download here: NEED A LINK
CAD step files for the Cold Aisle CFD geometry are available for download here: NEED A LINK

6.3.2 Optics Simulation Modeling

This section TBD.

6.4 Thermal Test Fixture – Small Card

Full definition of the thermal test fixture will be included in a future specification release. Images of preliminary design shown below in Figure 94 and Figure 95.

CAD Files for the current revision of the test fixture are available for download here: NEED A LINK

Figure 94: Small Card Thermal Test Fixture Preliminary Design

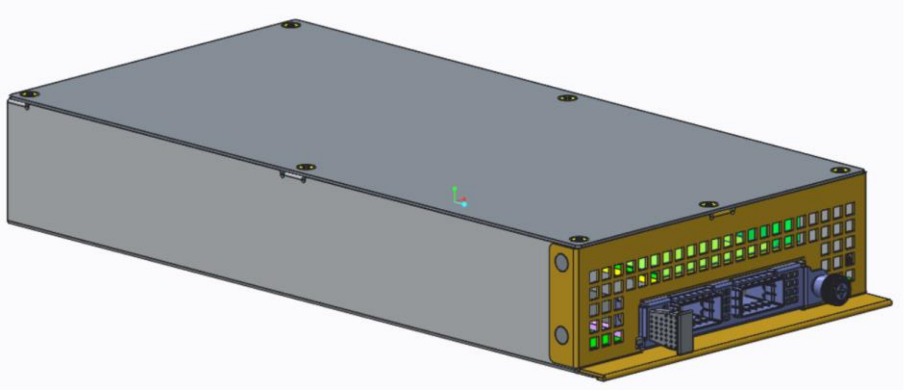
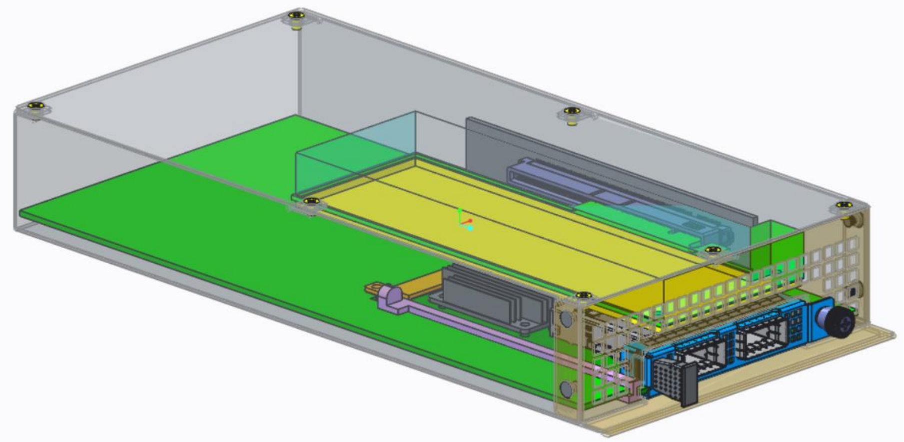


Figure 95: Small Card Thermal Test Fixture Preliminary Design – Transparent View



6.5 Sensor Requirements

See Sections 4.4 to 4.6 for information relating to temperature sensor and reporting requirements.

6.6 Card Cooling Tiers

Section 4.10.2 defines a number of registers that may be read by the associated baseboard system. Two of these registers provide the Hot Aisle and Cold Aisle Card Cooling Tiers that may be used for fan speed control. The Card Cooling Tiers relate the card local inlet temperature to the required local inlet velocity which allows the system to set fan speeds according to the cooling requirements of the card.

The Card Cooling Tier registers are particularly useful for systems that do not implement temperature sensor monitoring. The register may also be used as a backup for cards that do implement temperature sensor monitoring.

6.6.1 Hot Aisle Cooling Tiers

Card Cooling Tiers for Hot Aisle Cooling are defined in Table 55. Future releases of this specification will provide more detail to the Card Cooling Tier curve definition.

Table 55: Hot Aisle Card Cooling Tier Definitions

	Target Operating Region				**Server Airflow High Fan Speed**		**Non-Typical Server Airflow - Subject to System Capability**					
OCP NIC 3.0 Local Inlet Temperature [°C]	Tier 1	Tier 2	Tier 3	Tier 4	Tier 5	Tier 6	Tier 7	Tier 8	Tier 9	Tier 10	Tier 11	Tier 12
5												
10												
15												
20												
25												
30												
35												
40												
45												
50												
55	50	100	150	200	250	300	350	400	450	500	750	1000
60												
65												

6.6.2 Cold Aisle Cooling Tiers

Card Cooling Tiers for Cold Aisle Cooling are defined in Table 56. Future releases of this specification will provide more detail to the Card Cooling Tier curve definition.

Table 56: Cold Aisle Card Cooling Tier Definitions

	Target Operating Region				**Server Airflow High Fan Speed**		**Non-Typical Server Airflow - Subject to System Capability**					
OCP NIC 3.0 Local Inlet Temperature [°C]	Tier 1	Tier 2	Tier 3	Tier 4	Tier 5	Tier 6	Tier 7	Tier 8	Tier 9	Tier 10	Tier 11	Tier 12
5												
10												
15												
20												
25												
30												
35	50	100	150	200	250	300	350	400	450	500	750	1000
40												
45												
50												
55												
60												
65												

~~6.1~~6.7 Shock & Vibration

This specification does not cover the shock and vibration testing requirements for an OCP NIC 3.0 add in card or its associated baseboard systems. OCP NIC 3.0 components are deployed in various environments. It is up to each OCP NIC 3.0 card and baseboard vendor to decide how the shock and vibration tests shall be done.

7 Regulatory

7.1 Required Compliance

An OCP NIC 3.0 card shall meet the following Environmental, EMC and safety requirements.

7.1.1 Required Environmental Compliance

- **China RoHS Directive**
- **EU RoHS 2 Directive (2011/65/EU)** aims to reduce the environmental impact of electronic and electrical equipment (EEE) by restricting the use of certain hazardous materials. The substances banned under RoHS are lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls, polybrominated diphenyl ether, and four phthalates.
- **EU REACH Regulation (EC) No 1907/2006** addresses the production and use of chemical substances and their potential impact on human health and the environment.
- **EU Waste Electrical and Electronic Equipment (“WEEE”)** Directive (2012/19/EU) - mandates the treatment, recovery and recycling of EEE.
- **The Persistent Organic Pollutants Regulation (EC) No. 850/2004** bans production, placing on the market and use of certain persistent organic pollutants.
- **The California Safe Drinking Water and Toxic Enforcement Act of 1986 (“Prop 65”)** sets forth a list of regulated chemicals that require warnings in the State of California.
- **The Packaging and Packaging Waste Directive 94/62/EC** limits certain hazardous substances in the packaging materials
- **Batteries Directive 2006/66/EC** regulates the manufacture and disposal of all batteries and accumulators, including those included in appliances.

7.1.2 Required EMC Compliance

- Radiated and Conducted Emissions requirements are based on deployed geographical locations. Refer to Table 57~~Table 51~~ for details.

Table 57~~51~~: FCC Class A Radiated and Conducted Emissions Requirements Based on Geographical Location

Targeted Geography	**Applicable Specifications**
USA	FCC, 47 CFR Part 15, Class A digital device (USA)
Canada	ICES-003, class A (CAN)
EU	EN 55032: 2015 Class A Radiated and Conducted Emissions requirements for European Union EN 55024: 2010 Immunity requirements for European Union (EU)
Australia/New Zealand	AS/NZS CISPR 22:2009 + A1:2010 Class A and CISPR 32:2015 for Radiated and Conducted Emissions requirements
Japan	VCCI:2015-04 Class A Radiated and Conducted Emissions requirements
Korea	KN32 – Radiated and Conducted Emissions KN35- Immunity

Taiwan	BSMI CNS13438: 2006 (complete) Class A Radiated and Conducted Emissions requirements

- **CE** – Equipment must pass the CE specification
- All technical requirements covered under **EMC Directive (2014/30/EU)**

7.1.3 Required Product Safety Compliance

- Safety - requirements are listed in Table 58~~Table 52~~.

Table 58~~52~~: Safety Requirements

Targeted Geography	Applicable Specifications
Safety	UL/CSA 60950-1-07, 2nd Edition + amendment 1, dated 2011/12/19. The Bi-National Standard for Safety of Information Technology Equipment, EN60950-1: 2006+A11:2009+A1:2010+A12:2010+A2:2013 62368-1 may also be co-reported depending on region

7.2 Recommended Compliance

An OCP NIC 3.0 card is recommended to meet below compliance requirements.

7.2.1 Recommended Environmental Compliance

- **Halogen Free:** IEC 61249-2-21 Definition of halogen free: 900ppm for Br or CI, or 1500ppm combined.
- **Arsenic:** 1000 ppm (or 0.1% by weight)
- **Emerging: US Conflict Minerals law: section 1502 of the Dodd-Frank Act** requires companies using tin, tantalum, tungsten, and gold (“3TG”) in their products to verify and disclose the mineral source. While this does not apply to products that are used to provide services, such as Infrastructure hardware products, the OCP NIC Subgroup is considering voluntarily reporting of this information.

7.2.2 Recommended EMC Compliance

- 10dB margin to FCC sub-part 15 b class A emission requirements as specified in Section 7.1.2~~6.3.1.2~~.

8 Revision History

Author	Description	Revision	Date
Thomas Ng Intel Corporation	Initial draft with contributions and collaboration from the OCP NIC 3.0 subgroup.	0.01-0.62	01/17/2018
OCP NIC 3.0 Subgroup	Initial public review.	0.70	01/25/2018