



OCP NIC 3.0 Design Specification

Version 0.530.50

|

Author: OCP Server Workgroup, OCP NIC subgroup



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1 Overview

1.1 License

As of July 26, 2016, the following persons or entities have made this Specification available under the Open Compute Project Hardware License (Permissive) Version 1.0 (OCPHL-P)

OCP NIC Subgroup

An electronic copy of the OCPHL-P is available at:

http://www.opencompute.org/assets/download/01-Contribution-Licenses/OCPHL-Permissive-v1.0.pdf

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1.2 Background

The OCP NIC 3.0 specification is a follow-on to the OCP 2.0 form-factor for PCIe add-in cards. The OCP NIC 3.0 specification supports two basic card sizes: Small Card, and Large Card. The Small Card allows for up to 16 PCIe lanes on the card edge while a Large Card supports up to 32 PCIe lanes. Compared to the OCP Mezz Card 2.0 Design Specification, the updated specification provides a broader solution space for NIC and system vendors to support the following use case scenarios:

- NICs with a higher TDP
- Support up to 80W of power delivery to a single connector (Small) card; and 150W to a dual connector (Large) card
- Support up to PCIe Gen5 on the system and add-in card
- Support for up to 32 lanes of PCIe per add-in card
- Support for single host, multi-root complex and multi-host environments
- Support a greater board area for more complex add-in card designs
- Support for Smart NIC implementations with on-board DRAM and accelerators
- Simplification of FRU installation and removal while reducing overall down time

A representative Small Card OCP 3.0 NIC mezzanine card is shown in Figure 1 and a representative Large Card is shown in Figure 2.

Figure 1: Representative Small OCP NIC 3.0 Card with Quad SFP Ports

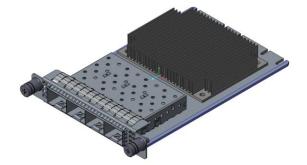
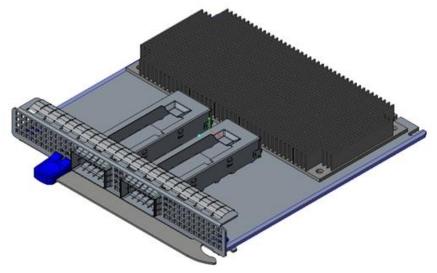




Figure 2: Representative Large OCP NIC 3.0 Card with Dual QSFP Ports and on-board DRAM



In order to achieve the features outlined in this specification, OCP 3.0 compliant cards are not backwards compatible to OCP Mezz 2.0 cards.

This specification is created under OCP Server workgroup – OCP NIC subgroup. An electronic copy of this specification can be found on the Open Compute Project website:

http://www.opencompute.org/wiki/Server/Mezz#Specifications and Designs

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1.3 Acknowledgements

The OCP NIC Subgroup would like to acknowledge the following member companies for their contributions to the OCP NIC 3.0 specification:

Table 1: Acknowledgements – By Company

Amphenol TCS Broadcom Dell Facebook Hewlett Packard Enterprise

Intel Corporation Lenovo Mellanox Netronome TE **Commented [NT1]:** What is the preferred way to do Acknowledgements?

By company? Individual? Sorted alphabetically? By contribution amount?

Am I missing any contributing companies?



1.4 Overview

1.4.1 Mechanical Form factor overview

The OCP NIC 3.0 specification defines a third generation mechanical form factor that allows for interoperability between compliant baseboards and add-in cards.

OCP NIC 3.0 cards have two form factors – Small and Large. These cards are shown in Figure 3 below. The components shown in the figures are for illustrative purposes. The Small form factor card has one connector (Primary connector) on baseboard. The Large form factor card has one or two connectors (Primary Connector only and both the Primary and Secondary Connectors) on the baseboard.

Both the Primary and Secondary connectors are defined in and compliant to SFF-TA-1002. On the add-in card side, the card edge is implemented with gold fingers. The small card gold finger area only occupies the Primary Connector area for up to 16 PCIe lanes. The large card gold finger area may occupy both the Primary and Secondary connectors for up to 32 PCIe lanes, or optionally just the Primary connector for up to 16 PCIe lanes. The gold finger design follows SFF-TA-1002 as well.

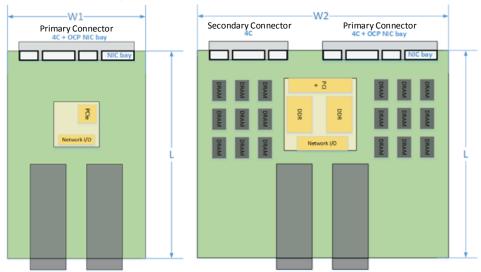


Figure 3: Small and Large Card Form-Factors (not to scale)

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The two form factor dimensions are shown in Table 2.

	Table 2: OCP 3.0 Form Factor Dimensions						
Form Factor	Width	Depth	Primary Connector	Secondary Connector	Typical Use Case		
Small	W1 = 76 mm	L = 115 mm	4C + OCP sideband 168 pins	N/A	Low profile and NIC with a similar profile as an OCP NIC 2.0 add-in card; up to 16 PCIe lanes.		
Large	W2 = 139 mm	L = 115 mm	4C + OCP sideband 168 pins	4C 140 pins	Larger PCB width to support additional NICs; up to 32 PCIe lanes.		

The OCP NIC 3.0 design allows downward compatibility between the two card sizes. Table 3 shows the compatibility between the baseboard and NIC combinations. A small size baseboard slot may only accept a small sized NIC. A Large size baseboard slot may accept a small or large sized NIC.

Table 3: Baseboard to OCP NIC Form factor Compatibility Chart

Baseboard	NIC Size / Supported PCIe Width			
Slot Size	Small	Large		
Small	Up to 16 PCIe lanes	Not Supported		
Large	Up to 16 PCIe lanes	Up to 32 PCIe lanes		

There are two baseboard connector options available for system designers: straddle mount and right angle (RA). The straddle mount connector option allows the OCP NIC and baseboard to exist in a coplaner position. To achieve this, a cutout exists on the baseboard and is defined in this specification. Alternatively, the right angle option allows the OCP NIC to be installed on top of the baseboard. A baseboard cutout is not required for the right angle connector. The right angle option allows the baseboard to use this area for additional routing or backside component placement. The straddle mount and right angle connectors are shown in Section 3.2.

For both the baseboard and OCP card, this specification defines the component and routing keep out areas. Refer to Section <u>2.52.6</u> for details.

Both the straddle mount and right angle implementations shall accept the same OCP add-in card and shall be supported in the baseboard chassis regardless of the baseboard connector selection (right angle or straddle mount) so long as the baseboard slot side and add-in card sizes are a supported combination as shown in Table 3.

This specification defines the form factor at the add-in card level, including the front panel, latching mechanism and card guide features.

More details about the card form-factor is shown in Section 2.



1.4.2 Electrical overview

This specification defines the electrical interface between baseboard and the add-in card. The electrical interface is implemented with a right angle or straddle mount connector on baseboard and gold finger on the add-in card. As previously noted in the mechanical overview, each card may implement a Primary Connector or Primary + Secondary Connector. Cards using only the Primary connector are suitable for both the Small and Large form-factors and may support up to 16 lanes of PCIe. The Secondary connector, when used in conjunction with the Primary connector, allows Large form-factor implementations and may support up to 32 lanes of PCIe.

1.4.2.1 Primary Connector

The Primary connector provides all OCP specific management functions as well as up to 16 lanes of PCIe between the OCP NIC and the system motherboard.

Management Function Overview (OCP Bay):

- DSP0222 1.1 compliant Network Controller Sideband Interface (NC-SI) RMII Based Transport (RBT) Physical Interface
- Power management and status reporting
 - Power disable
 - State change control
- SMBus 2.0
- Control / status serial bus
 - NIC-to-Host status
 - Port LED Link/Activity
 - Environmental Indicators
 - Host-to-NIC configuration Information
- Multi-host PCIe support signals (2x PCIe resets, 2x reference clocks)
 - The OCP bay provides PERST2#, PERST3#, REFCLK2 and REFCLK3. This enables support for up to four hosts when used in conjunction with PERST0#, PERST1#, REFCLK0 and REFCLK1 in the Primary 4C region.
- PCIe Wake signal

See Section 3.5 for a complete list of pin and function descriptions for the OCP Bay portion of the primary connector.

PCIe Interface Overview (4C Connector):

- 16x differential transmit/receive pairs
 - Up to PCle Gen 5 support
- 2x 100 MHz differential reference clocks
- Control signals
 - o 2x PCIe Resets
 - Link Bifurcation Control
 - o Card power disable/enable
- Power

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- \circ 12V /12V AUX
- 3.3V AUX

See Section 3.4 for a complete list of pin and function descriptions for the 4C connector.

1.4.2.2 Secondary Connector

The secondary connector provides an additional 16 lanes of PCIe and their respective control signals.

PCIe Interface Overview (4C Connector):

- 16x differential transmit/receive pairs
 - Up to PCle Gen 5 support
- 2x 100 MHz differential reference clocks
- Control signals
 - 2x PCIe Resets
 - Link Bifurcation Control
 - Card power disable/enable
- Power
 - 12V /12V AUX
- 3.3V AUX

See Section 3.4 for a complete list of pin and function descriptions for the 4C connector.



1.5 References

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2 Card Form Factor

2.1 Overview

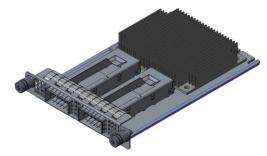
2.22.1 Form Factor Options

OCP3.0 provides two fundamental form factor options: a small card (76mm x 115mm) and a large card (139mm x 115mm).

These form factors support a Primary Connector and optionally, a Secondary Connector. The Primary Connector is defined to be a SFF-TA-1002 compliant 4C connector plus a 28-pin bay for OCP 3.0 specific pins. The Secondary Connector is the 4C connector as defined in SFF-TA-1002. The 4C specification supports up to 32 differential pairs for a x16 PCle connection per connector. For host platforms, the 28-pin OCP bay is required for the Primary connector. This is also mandatory for add-in cards.

The small card uses the Primary 4C connector to provide up to a x16 PCIe interface to the host. The additional 28-pin OCP bay carries sideband management interfaces as well as OCP NIC 3.0 specific control signals for multi-host PCIe support. The small size card provides sufficient faceplate area to accommodate up to 2x QSFP modules, 4x SFP modules, or 4x RJ-45 for BASE-T operation. The small card form factor supports up to 80W of delivered power to the card edge.

Figure 4: Example Small Card Form Factor



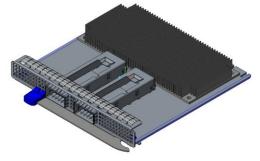
The large card uses the Primary 4C + OCP bay connector to provide the same functionality as the small card along with an additional Secondary 4C connector to provide up to a x32 PCIe interface. The large card may utilize both the Primary and Secondary connectors, or just the Primary connector for lower PCIe lane count applications. Table 4 summarizes the large card permutations. The large size card supports higher power envelopes and provides additional board area for more complex designs. The large card form factor supports up to 150W of delivered power to the card edge across the two connectors.

Commented [HS2]: For some use cases, secondary connector is not required to be used for large card size. We need to discuss and clarify it.

Commented [TN3R2]: I made a place holder for a Large Card that only uses the Primary Connector. See the end of this section.

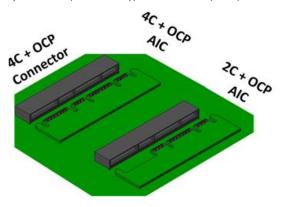


Figure 5: Example Large Card Form Factor



For both form factors, an add in card may optionally implement a subset of pins to support up to a x8 PCIe connection. This is implemented using a 2C card edge per SFF-TA-1002. The Primary Connector may support a 2C sized add-in card along with the 28 pin OCP bay. The following diagram from the SFF-TA-1002 specification illustrates the supported host Primary and Secondary Connectors and add-in card configurations.

Figure 6: Primary Connector (4C + OCP Bay) with 4C and 2C (Small) Add in Cards



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For both form-factors, an add-in card may optionally implement a subset of pins to support up to a x8 PCIe connection. This is implemented using a 2C card edge per SFF-TA-1002. The Primary Connector may support a 2C sized add-in card along with the 28 pin OCP bay. The following diagram from the SFF-TA-1002 specification illustrates the supported host Primary and Secondary Connectors and add-in card configurations.

Figure 86: Primary Connector (4C + OCP Bay) with 4C and 2C (Small) Add-in Cards



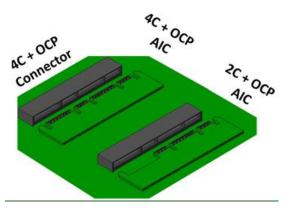


Table 4

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Connector and up to 16 PCIe lanes. Large form factor cards support implementations with both the Primary and Secondary Connectors and up to 32 PCIe lanes, or a Primary Connector only implementation with up to 16 PCIe lanes.

Table 4 summarizes the supported card form factors. Small form factors cards support the Primary Connector and up to 16 PCIe lanes. Large form factor cards support implementations with both the Primary and Secondary Connectors and up to 32 PCIe lanes, or a Primary Connector only implementation with up to 16 PCIe lanes.

Table 4: OCP NIC 3.0 Card Definitions

Add in Card Size and	Secondary Connector		Primary Connector		
max PCIe Lane Count	4C Connector, x16 PCIe		4C Connector, x16 PCIe		OCP Bay
Small (x8)				2C	OCP Bay
Small (x16)			4	С	OCP Bay
Large (x8)				2C	OCP Bay
Large (x16)			4	С	OCP Bay
Large (x24)		2C	4	С	OCP Bay
Large (x32)	4C		4	С	OCP Bay

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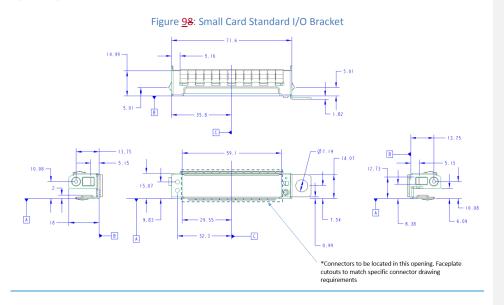


2.32.2 I/O bracket

The following section defines the standard I/O bracket and standard chassis opening required for both the Small and Large form-factor cards.

2.3.12.2.1 Small Form Factor Add-in Card I/O Bracket

Figure 9-Figure 8 defines the standard Small Card form factor I/O bracket.



Note: The add-in card supplier shall add port identification on bracket that meet their manufacturing and customer requirements.

For RJ-45 implementations, a customized bracket must be created. Figure 10Figure 9 shows an example.

Figure <u>109</u>: Small Card Customized bracket for RJ-45 Connector Drawing to be inserted

Figure 11 Figure 10 shows the standalone bracket assembly and Figure 12 Figure 11 shows the bracket in card.

Figure <u>11</u>10: Small Card 3D Bracket Assembly (Standalone)

TBD

Figure <u>12</u>11: Small Card 3D Bracket Assembly (Installed on Add-in Card) TBD

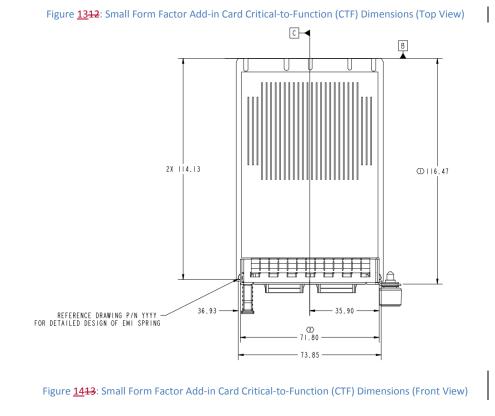
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In addition to the sheet metal, Table 5 lists the additional hardware components used for the Small Card bracket assembly.

Item description	Supplier Part Number		
Top and bottom EMI fingers	TF187VE32F11		
Screw / Rivet (part of bracket assy)?	TBD		
Side EMI Finger	TBD		
Thumb screw	TBD		
Pull Tab	TBD		
Latch	TBD		
Screw (attaching Bracket & NIC)	TBD		
SMT Nut (on NIC)	TBD		

2.3.22.2.2 Small Form Factor Add-in Card Critical-to-Function (CTF) Dimensions

The following dimensions are considered critical-to-function (CTF) for each small form factor add-in card.





1

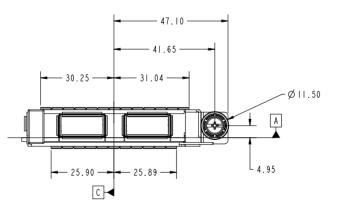
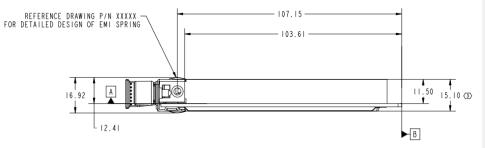


Figure <u>15</u>14: Small Form Factor Add-in Card Critical-to-Function (CTF) Dimensions (Side View – Left)

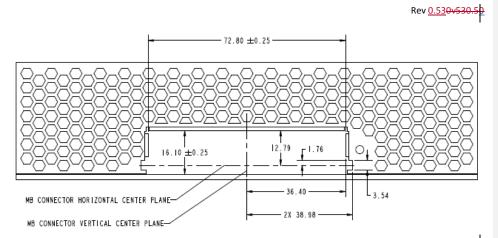


Figure <u>1615</u>: Small Form Factor Add-in Card Critical-to-Function (CTF) Dimensions (Side View – Right)

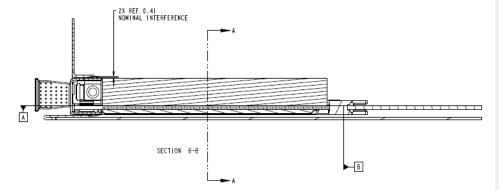


2.3.32.2.3 Small Form Factor Baseboard Critical-to-Function (CTF) Dimensions The following dimensions are considered critical-to-function (CTF) for each small form factor baseboard chassis.

Figure <u>1716</u>: Small Form Factor Baseboard Chassis Critical-to-Function (CTF) Dimensions (Rear View)









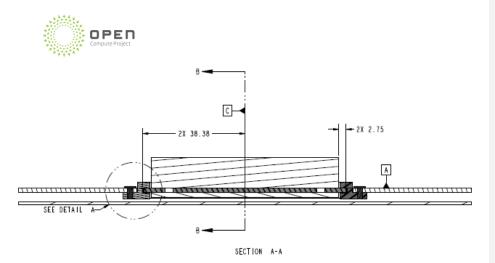
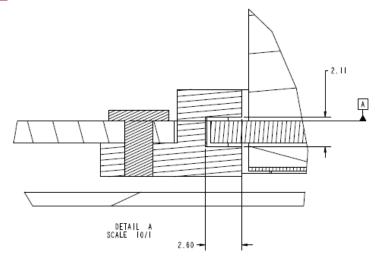


Figure 2019: Small Form Factor Baseboard Chassis Critical-to-Function (CTF) Dimensions (Rail Guide



On the baseboard side, the following mechanical dimensions shall be met to support a small form factor add-in card:

Figure 2120: Baseboard and Rail Assembly Drawing for Small Cards TBD; need 3D baseboard and rail assembly drawing.

2.3.42.2.4 Large Form Factor Add-in Card I/O Bracket TBD. <u>Definition is in progress.</u> <need input from OCP mechanical groups>. All drawings from the Small Form-Factor implementation need to be replicated for the Large form-factor. Figure 22 defines the standard Large Card form factor I/O bracket.

Open Compute Project • NIC • 3.0 Rev 0.530-630-64 Figure 22: Large Card Standard I/O Bracket TBD Note: The add-in card supplier shall add port identification on bracket that meet their manufacturing and customer requirements. For RI-45 implementations, a customized bracket must be created. Figure 23 shows an implementation example. Figure 23: Large Card Customized bracket for RI-45 Connector Drawing to be inserted Figure 24: Large Card 3D Bracket Assembly (Standalone) TBD Figure 25: Large Card 3D Bracket Assembly (Installed on Add-in Card) TBD Figure 25: Large Card 3D Bracket Assembly (Installed on Add-in Card) TBD Figure 25: Large Card 3D Bracket Assembly (Installed on Add-in Card) TBD Figure 25: Large Card 3D Bracket Assembly (Installed on Add-in Card) TBD Second bracket assembly Table 6: Mechanical BOM for the Large Card Bracket Immode bracket assembly Table 6: Mechanical BOM for the Large Card Bracket Immode bracket assembly Secrew Nivet (part of bracket assembly			
Figure 22: Large Card Standard I/O Bracket IBD Note: The add-in card supplier shall add port identification on bracket that meet their manufacturing and customer requirements. Gr RI-45 implementations, a customized bracket must be created. Figure 23 shows an implementation bracket for RI-45 Connector Drawing to be inserted Sigure 23: Large Card Customized bracket for RI-45 Connector Drawing to be inserted Sigure 24: Large Card 3D Bracket Assembly (Standalone) IBD Figure 25: Large Card 3D Bracket Assembly (Installed on Add-in Card) IBD Figure 25: Large Card 3D Bracket Assembly (Installed on Add-in Card) IBD Figure 25: Large Card 3D Bracket Assembly (Installed on Add-in Card) IBD Figure 25: Large Card 3D Bracket Assembly (Installed on Add-in Card) IBD Addition to the sheet metal, Table 6 Table 5 lists the additional hardware components used for the small Card bracket assembly. Table 6: Mechanical BOM for the Large Card Bracket Item description Supplier Part Number Top and bottom FMI fingers 100 100 100 Sup		Open Compute Project • NIC • 3.0	
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2.2.5 Large Form Factor Add-in Card Critical-to-Function (CTF) Dimensions The following dimensions are considered critical-to-function (CTF) for each large form factor add-in card. Figure 26: Large Form Factor Add-in Card Critical-to-Function (CTF) Dimensions (Top View) TBD Figure 27: Large Form Factor Add-in Card Critical-to-Function (CTF) Dimensions (Front View)			
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Figure 28: Large Form Factor Add-in Card Critical-to-Function (CTF) Dimensions (Side View - Left) TBD Figure 29: Large Form Factor Add-in Card Critical-to-Function (CTF) Dimensions (Side View - Right) TBD 2.2.6 Large Form Factor Baseboard Critical-to-Function (CTF) Dimensions The following dimensions are considered critical-to-function (CTF) for each large form factor baseboard chassis. Figure 30: Large Form Factor Baseboard Chassis Critical-to-Function (CTF) Dimensions (Rear View) TBD Figure 31: Large Form Factor Baseboard Chassis Critical-to-Function (CTF) Dimensions (Side View) TBD Figure 32: Large Form Factor Baseboard Chassis Critical-to-Function (CTF) Dimensions (Rear Rail Guide View) TBD Figure 33: Large Form Factor Baseboard Chassis Critical-to-Function (CTF) Dimensions (Rail Guide Detail) TBD On the baseboard side, the following mechanical dimensions shall be met to support a large form factor add-in card: Figure 34: Baseboard and Rail Assembly Drawing for Large Card

TBD; need 3D baseboard and rail assembly drawing for large card.

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2.42.3 Line Side I/O Implementations

At the time of this writing, the Small and Large form-factor implementations have been optimized to support the following standard line side I/O implementations:

Table 764: OCP 3.0 Line Side I/O Implementations			
Form Factor	Max Topology Connector Count		
Small	2x QSFP28		
Small	4x SFP28		
Small	4x RJ-45		
Large	2x QSFP28		
Large	4x SFP28		
Large	4x RJ-45		

Additional combinations are permissible as I/O form-factor technologies and thermal capabilities evolve.

2.52.4 LED Implementations

LEDs may be implemented on the card Scan Chain (as defined in Section <u>3.5.3</u>) for remote link/activity indication on the baseboard. <u>LEDs shall be</u>-or optionally be implemented on the OCP NIC 3.0 I/O bracket if when there is sufficient space for local indication. These two cases are described below. In both cases, the actual link rate may be directly queried through the management interface.

2.5.12.4.1 Baseboard LEDs Configuration Over the Scan Chain

A small form-factor OCP NIC 3.0 with a fully populated I/O bracket (2x QSFP28, 4x SFP28 or 4x RJ-45) has insufficient space for discrete on-board (faceplate) LED indicators. In this case, the line side link and activity LED indicators are implemented on the baseboard system via the Scan Chain. The Scan Chain bit stream is defined in Section 3.5.3.

The baseboard LED implementation uses two discrete LEDs (Link/Activity and Speed indication). <u>Table</u> <u>8</u><u>Table 7</u> describes the baseboard LED configuration for baseboard implementations.

This-The LED implementation is required for all add-in cards. <u>The LED implementation is optional for</u> <u>baseboards</u>.

Commented [JN4]: When space allows, I think the card LED implementation is not optional, but a requirement. This shall be 90%+ of the use cases (single / dual SFP, QSFP)

Commented [JD5]: Maybe use a different name for the serial bus? Seeing the Scan Chain usually refers to JTAG? (Pretty minor comment though)

Commented [JN6]: Double check if dual QSFP has room for LED?

2x QSFP shall be smaller than 4x SFP+ and the extra space could be used for LED implementation



Table <u>875</u> : Baseboard LED Configurations with Two Physical LEDs per Port				
LED Pin	LED Color	Description		
Link /	Green	Active low. Multifunction LED.		

Green	Active low. Multifunction LED.
	This LED shall be used to indicate link and link activity.
	When the link is up and no link activity is present, then this LED shall
	be lit and solid. This indicates that the link is established, there are no
	local or remote faults, and the link is ready for data packet
	transmission/reception.
	When the link is up and there is link activity, then this LED should blink
	at the interval of 50-500ms during link activity.
	The baseboard Link/Activity LED location is not mandated in this
	specification and will be defined by the system vendor.
Green	Active low. Multifunction LED.
Off	
	The LED is Green when the port is linked at its maximum speed.
	The LED is off when the device is linked at a speed lower than the
	highest capable speed, or no link is present.
	The baseboard bicolor speed LED location is not mandated in this
	specification and will be defined by the system vendor.
	Green

At the time of this writing, the Scan Chain definition allows for up to one link/activity and one speed LED per port. A total of up to 8 ports are supported in the Scan Chain. The bit stream defines the LEDs to be active low (on). The Scan Chain LED implementation allows the NIC LED indicators to be remotely located on the OCP 3.0 compliant chassis (e.g. front LED indicators with rear I/O cards).

2.5.22.4.2 Add-in Card LED Configuration

For low I/O count small form-factor cards without built in light pipes (such as 1x QSFP28, 2x SFP28, or 2x RJ-45), or a large form-factor OCP 3.0 NIC, where additional I/O bracket area is available, the card may shall optionally implement on-board link/activity indications in place of the Scan Chain LED stream. The recommended local (on-card) LED implementation uses two physical LEDs (a discrete Link/Activity LED and a bi-colored Speed A/Speed B LED). Table 9Table 8 describes the add-in card LED implementations.

Commented [JN7]: 1.For current define, it is not bi-color 2.However, it makes sense to use bi-color to have same amount of feature as on-NIC-LED.

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	Table <u>98</u> : Add-in Card LED Configuration with Two Physical LEDs per Port				
LED Pin	LED Color	Description			
Link / Activity	Green	Active low. Multifunction LED.			
,		This LED shall be used to indicate link and link activity.			
		When the link is up and no link activity is present, then this LED shall be lit and solid. This indicates that the link is established, there are no local or remote faults, and the link is ready for data packet transmission/reception.			
		When the link is up and there is link activity, then this LED should blink at the interval of 50-500ms during link activity.			
		The Link/Activity LED shall be located on the left hand side or located on the top for each port when the add-in card is viewed in the horizontal plane.			
Speed	Green	Active low. Bicolor multifunction LED.			
	Amber Off	The LED is Green when the port is linked at its maximum speed. The LED is Amber when the port is linked at it second highest speed. The LED is off when the device is linked at a speed lower than the second highest capable speed, or no link is present.			
		The Amber Speed LED indicator may be used for port identification through vendor specific link diagnostic software.			
		The bicolor speed LED shall be located on the right hand side or located on the bottom for each port when the add-in card is viewed in the horizontal plane.			

2.5.32.4.3 Add-in Card LED Ordering

For all add-in card use cases, each port shall implement the green Link/Activity LED and a bicolor green/amber speed A/B LED. For all baseboards, each port shall implement the green Link/Activity LED and a green speed A LED.

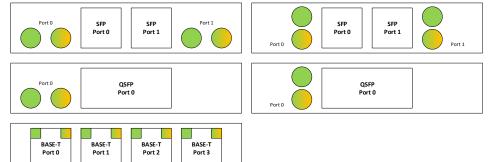
For horizontal LED positions, the Link/Activity LED shall be located on the left side for each port and the speed LED shall be located on the right side for each port.

For vertical LED positions, the Link/Activity LED shall be located on top and the speed LED shall be located on the bottom.

The placement of the LEDs on the faceplate may be left up to the discretion of the add-in card and baseboard designers. The LED port association shall be clearly labeled on the add-in card and on the baseboard.



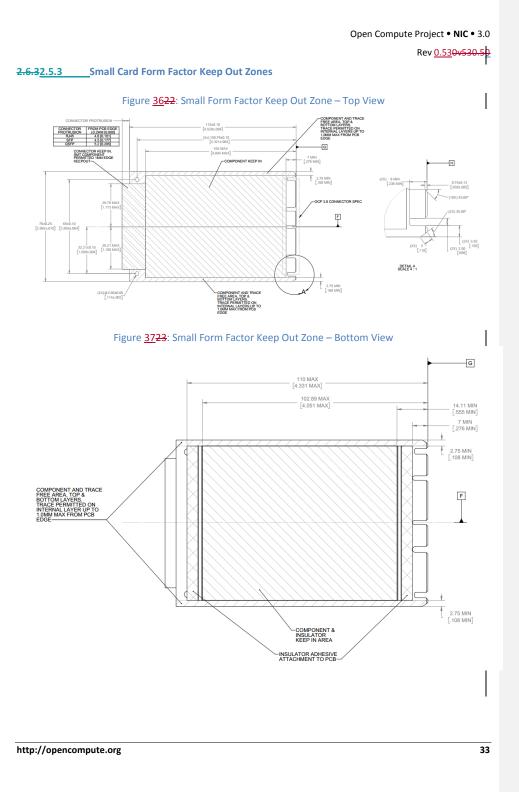
Figure 3521: LED Ordering – Example Small Card Link/Activity and Speed LED Placement



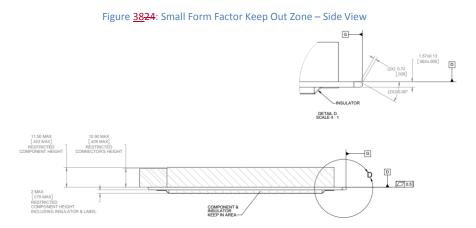
2.62.5 Mechanical Keepout Zones

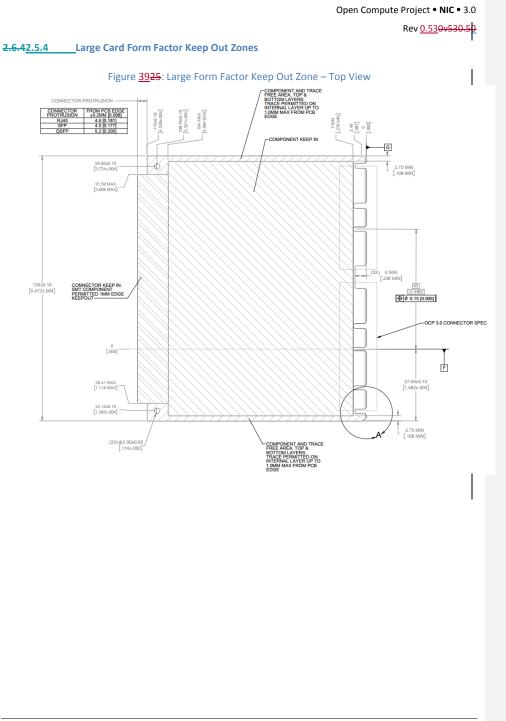
2.6.12.5.1 Baseboard Keep Out Zones – Small Card Form Factor TBD – Need keepout drawings and envelopes for small / large size baseboard including primary/secondary/rail keepouts/cutout for straddle mount/keepout for right angle.

2.6.22.5.2 Baseboard Keep Out Zones – Large Card Form Factor TBD. – need input from mechanical engineering











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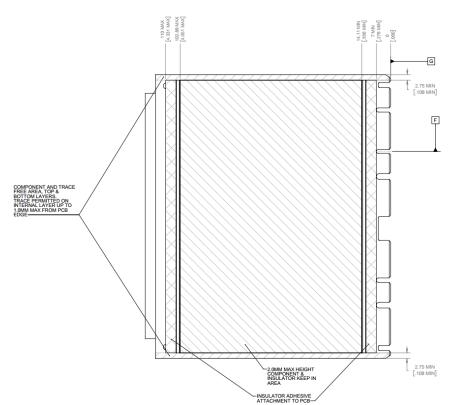
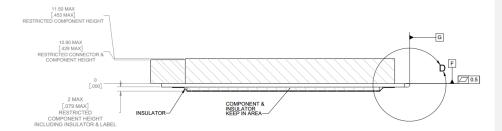


Figure <u>40</u>26: Large Form Factor Keep Out Zone – Bottom View

Figure <u>41</u>27: Large Form Factor Keep Out Zone – Side View



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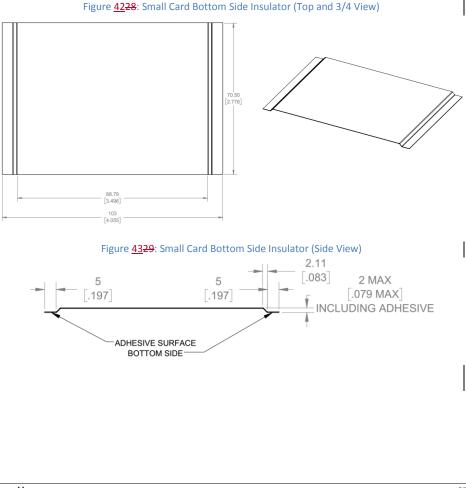
2.82.6 Labeling Requirements

Editor's note [TN 20171214]: Consider the following label attributes:

- Label attributes are human (e.g. ASCII) and machine readable (e.g. barcode)
- Add-in card MAC address shall be visible (used MAC address range, or base value)
- Board serial number

2.92.7 Insulation Requirements

All cards shall implement an insulator to prevent the bottom side card components from shorting out to the baseboard chassis. The recommended insulator thickness is 0.25mm and shall reside within the following mechanical envelope for the Small and Large size cards.





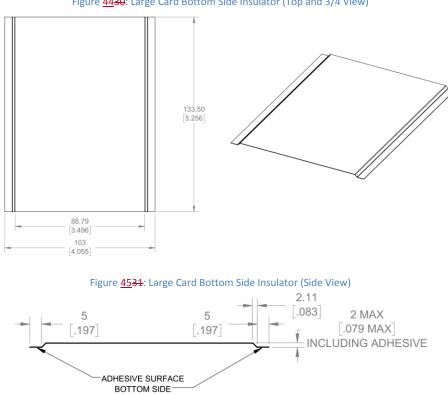


Figure <u>4430</u>: Large Card Bottom Side Insulator (Top and 3/4 View)

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<mark>2.10</mark> 2.8 TBD	NIC Implementation Examples
<u>2.11</u> 2.9	Non-NIC Use Cases
"PCIe interface	with extra management sideband"
2.11.1 2.9.1 TBD	PCIe Retimer card
2.11.2 2.9.2 TBD	Accelerator card
2 <u>.11.3</u> 2.9.3 TBD	Storage HBA / RAID card



3 Card Edge and Baseboard Connector Interface

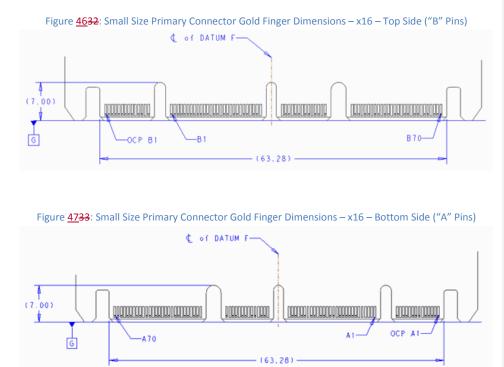
3.1 Gold Finger Requirements

The OCP NIC 3.0 add-in cards are compliant to the SFF-TA-1002 specification with respect to the gold fingers and connectors.

Small Size cards fit in the Primary Connector. Primary Connector compliant cards are 76mm x 115mm and may implement the full 168-pins. The Primary Connector cards may optionally implement a subset of gold finger pins if there is a reduced PCIe width requirement (such as 1 x8 and below). In this case, the card edge gold finger may implement a 2C design. The overall board thickness is 1.57mm. The gold finger dimensions for the Primary Connector compliant cards are shown below.

Large Size Cards support up to a x32 PCIe implementation and may use both the Primary and Secondary connectors. Large Size Cards may implement a reduced PCIe lane count and optionally implement only the Primary Connector 4C, or 2C plus OCP bay.

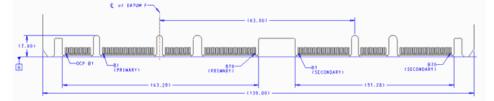
Note: The "B" pins on the connector are associated with the top side of the add-in card. The "A" pins on the connector are associated with the bottom side of the add-in card.

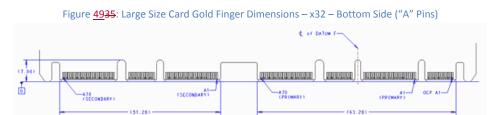


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Figure <u>48</u>34: Large Size Card Gold Finger Dimensions – x32 – Top Side ("B" Pins)





3.1.1 Gold Finger Mating Sequence

Per the SFF-TA-1002 specification, the Primary and Secondary connectors are protocol agnostic and are optimized for high speed differential pairs. For use in the OCP NIC 3.0 application, some pin locations are used for single ended control nets or power and would benefit from a shorter pin length for staggering. As such, the recommended add-in card gold finger staging is shown in <u>Table 10</u>Table 9 for a two stage, mate, last-break functionality. The host connectors have a single stage mating and do not implement different pin lengths.

The AIC Plug (Free) side refers to the add-in card gold fingers; the receptacle (Fixed) side refers to the physical connector on the host platform. This table is based on the SFF-TA-1002 Table A-1 with modifications for OCP NIC 3.0. Refer to the mechanical drawings for pin the first-mate and second-mate lengths.

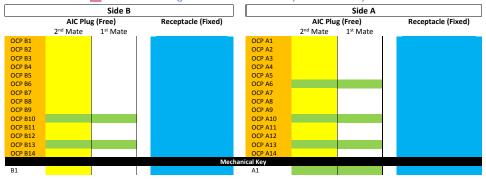
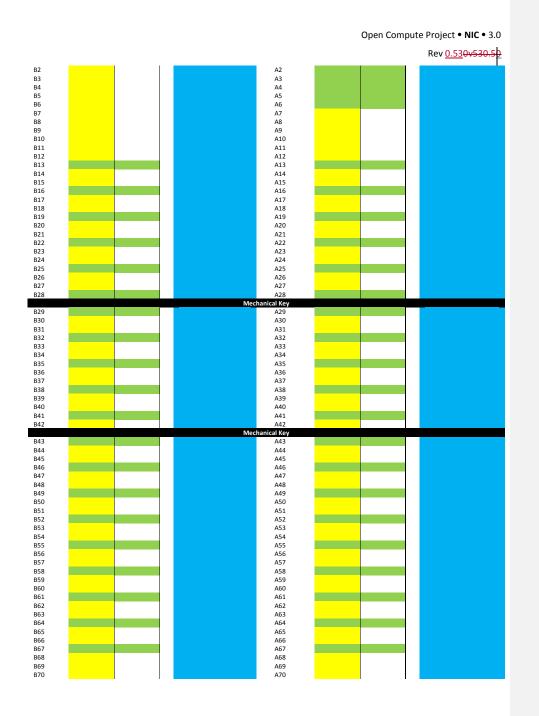


Table 109: Contact Mating Positions for the Primary and Secondary Connectors



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3.2 Baseboard Connector Requirements

The OCP NIC 3.0 connectors are compliant to the "4C connector" as defined in the SFF-TA-1002 specification for a right angle or straddle mount form-factor. The 4C connector is 140-pins in width and includes support for up to 32 differential pairs to support a x16 PCIe connection. The connector also provides 6 pins of 12V for payload power. This implementation is common between both the Primary and Secondary Connectors. In addition, the Primary Connector has a 28-pin OCP Bay to the right of pin 1. These pins are used for management and support for up to a 4 x2 and 4 x4 multi-host configuration on the Primary Connector. The Primary and Secondary Connector drawings are shown in Figure 50-Figure 51-Figure 37, Figure 53-Figure 38 and Figure 54-Figure 39 below.

All diagram units are in mm unless otherwise noted.

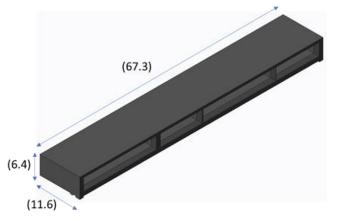
3.2.1 Right Angle Connector

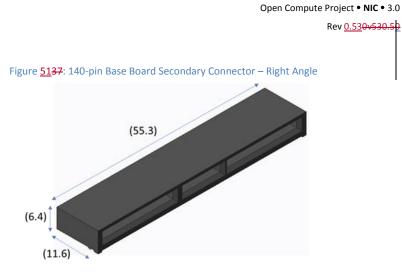
The following offset and height options are available for the right angle Primary and Secondary Connectors.

Table <u>11</u>10: Right Angle Connector Options

Name	Pins	Style and Baseboard Thickness	Offset (mm)
Primary Connector – 4C + OCP	168 pins	Right Angle	4mm
Secondary Connector – 4C	140 pins	Right Angle <mark>"</mark>	4mm

Figure 5036: 168-pin Base Board Primary Connector – Right Angle





3.2.2 Right Angle Offset

The OCP NIC 3.0 right angle connectors have a 4.0mm offset from the baseboard (pending SI simulation results). This is shown in Figure 45.

Figure 5245: Add-in Card and Host Offset for Right Angle Connectors

TBD

3.2.3 Straddle Mount Connector

The following offset and height options are available for the straddle mount Primary and Secondary Connectors.

4244 0

Table <u>1211</u> : Straddle Mount Connector Options					
Name	Pins	Style and Baseboard Thickness	Offset (mm)		
Primary Connector – 4C + OCP	168 pins	Straddle Mount for 0.062"	Coplanar (0mm)		
Primary Connector – 4C + OCP	168 pins	Straddle Mount for 0.076"	-0.3mm		
Primary Connector – 4C + OCP	168 pins	Straddle Mount for 0.093"	Coplanar (0mm)		
Secondary Connector – 4C	140 pins	Straddle Mount for 0.062"	Coplanar (0mm)		
Secondary Connector – 4C	140 pins	Straddle Mount for 0.076"	-0.3mm		
Secondary Connector – 4C	140 pins	Straddle Mount for 0.093"	Coplanar (0mm)		

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Figure 538: 168-pin Base Board Primary Connector – Straddle Mount

Field Code Changed

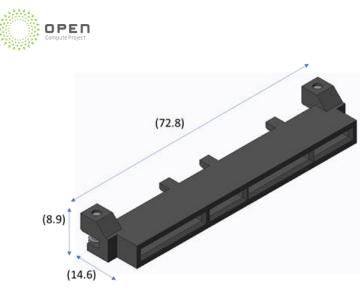
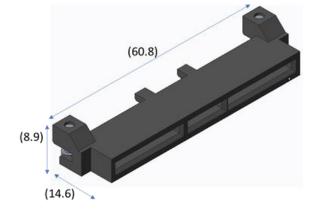


Figure <u>54</u>39: 140-pin Base Board Secondary Connector – Straddle Mount

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In order to the support the large form factor, systems must locate the Primary and Secondary Connectors per the mechanical drawing shown in Figure 40 and Figure 41.

Figure 40: Primary and Secondary Connector Locations for Large Card Support For Right Angle Connectors

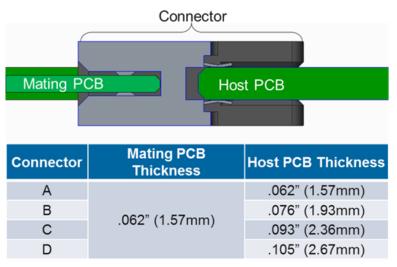
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Datum F	Datum F
Figure 41: Primary and Secondary Connector Locatic	ons for Large Card Support For Straddle Mount
Connecto	ərs



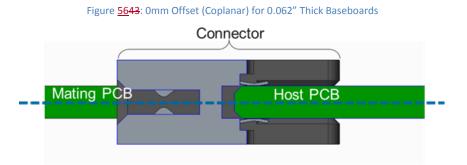
3.2.23.2.4 Straddle Mount Offset and PCB Thickness Options

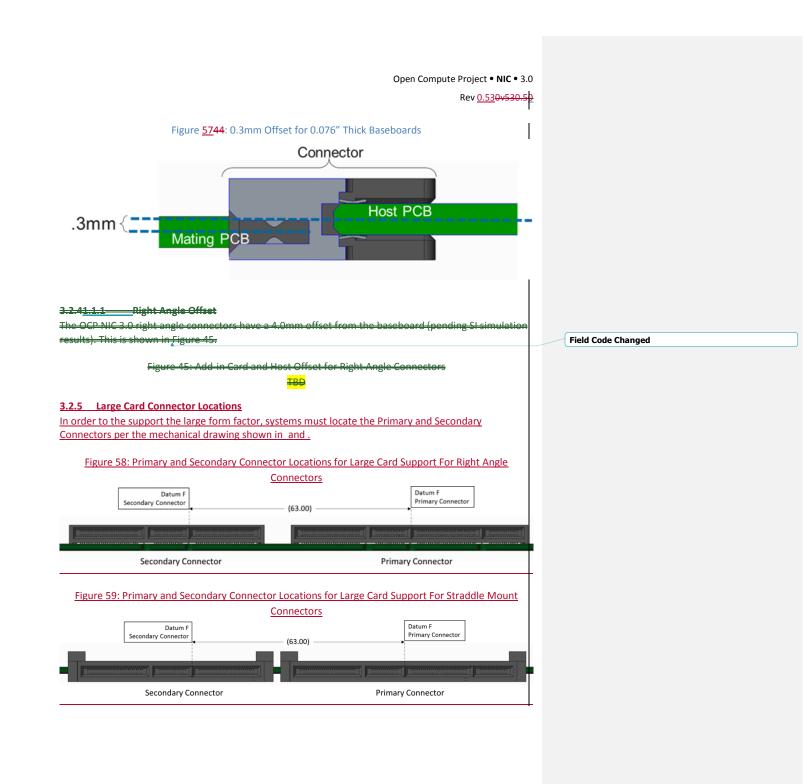
The OCP NIC 3.0 straddle mount connectors have four PCB thicknesses they can accept. The available options are shown in Figure 55Figure 42. The thicknesses are 0.062", 0.076", 0.093", and 0.105". These must be controlled to a thickness of $\pm 8\%$. These are available for both the Primary and Secondary connector locations. At the time of this writing, the most commonly used part is expected to be the 0.076" host board thickness.





The connectors are capable of being used coplanar as shown in Figure 56Figure 43. Additionally, the are also capable of having a 0.3mm offset from the centerline of the host board as shown in Figure







3.3 Pin definition

The pin definitions of an OCP NIC 3.0 card with up to a x32 PCIe interface are shown in Table 13Table 12 Table 14Table 13. All signal directions are shown from the perspective of the baseboard.

A baseboard system may provide a combination of Primary Connectors only, or Primary and Secondary Connectors to support multiple sizes of add-in cards. Both connectors share common functionality with power, SMBus 2.0, x16 PCIe and bifurcation control. The Primary Connector has an additional OCP Bay (pins OCP_A[1:14], OCP_B[1:14]) with additional REFCLKs for supporting up to four PCIe hosts, NC-SI connectivity and a Scan Chain for information exchange between the host and card. The NIC is required to implement the Scan Chain, while the baseboard may choose to optionally implement it. Depending on the baseboard form-factor, multiple OCP NIC 3.0 compliant cards may be designed into the system.

The pins common to the Primary and Secondary Connectors are shown in Section 3.4. The OCP Bay pins on the Primary Connector only are shown in Section 3.5.

Cards or systems that do not require the use of a PCIe x16 connection may optionally implement a subset electrical connections as applicable to the design. For example, a x8 (or smaller) card using the first 8 PCIe lanes that is compliant with the Primary Connector pinout. Refer to Sections 3.1 and 3.2 for mechanical details. For these cases, the Primary Connector matches the 2C dimensions as defined in SFF-TA-1002.

In all cases, the physical baseboard connectors shall support x16 PCIe widths and must be implemented with the Primary (4C + OCP Bay) and Secondary (4C) connectors.

Table 1312: Primary Connector Pin Definition (x16) (4C + OCP Bay)

Side B Side A NIC_PWR_GOOD OCP_B1 OCP_A1 Primary Connector (x16, 168-pin add-in card with OCP Bay) Primary PERST3# OCP_B2 PWRBRK# OCP_A2 OCP_B3 OCP A3 ID# WAKE-RBT_ARB_IN OCP_B4 DATA_IN OCP_A4 Connector (x8, 112-pin DATA_OUT OCP_B5 RBT_ARB_OUT OCP_A5 OCP A6 OCP B6 CLK GND OCP_B7 SLOT_ID RBT_TX_EN OCP_A7 OCP B8 RBT_RXD1 OCP_A8 RBT_TXD1 OCP_B9 OCP_A9 RBT RXD0 RBT TXD0 OCP A10 OCP B10 GND GND OCP_B11 REFCLKn2 REFCLKn3 OCP_A11 add-in card with OCP_B12 OCP_A12 **REFCLKp**2 **REFCLKp3** OCP B13 GND GND OCP A13 OCP B14 RBT_CRS_DV RBT_CLK_IN OCP_A14 Mechanical Key GND B1 A1 B2 GND A2 ÔÇ B3 GND A3 bay) Β4 GND Α4 B5 GND Α5 AUX B6 A6 GND Β7 BIFO# Α7 SMCLK B8 BIF1# SMDAT A8 В9 BIF2# SMRST# A9

Commented [HS8]: We should not require scan chain support for all NICs.

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				Rev <u>0.5</u>	
B10	PERSTO#	PRSNTA#	A10		
B11	+3.3V/+3.3V_AUX	PERST1#	A11		
B12	PWRDIS	PRSNTB2#	A12		
B13	GND	GND	A13		
B14	REFCLKn0	REFCLKn1	A14		
B15	REFCLKp0	REFCLKp1	A15		
B16	GND	GND	A16		
B17	PETn0	PERn0	A17		
B18	PETp0	PERp0	A18		
B19	GND	GND	A19		
B20	PETn1	PERn1	A20		
B21	PETp1	PERp1	A21		
B22	GND	GND	A22		
B23	PETn2	PERn2	A23		
B24	PETp2	PERp2	A24		
B25	GND	GND	A25		
B26	PETn3	PERn3	A26		
B27	PETp3	PERp3	A27		
B28	GND	GND	A28		
	Mechan	ical Key			
B29	GND	GND	A29		
B30	PETn4	PERn4	A30		
B31	PETp4	PERp4	A31		
B32	GND	GND	A32		
B33	PETn5	PERn5	A33		
B34	PETp5	PERp5	A34		
B35	GND	GND	A35		
B36	PETn6	PERn6	A36		
B37	PETp6	PERp6	A37		
B38	GND	GND	A38		
B39	PETn7	PERn7	A39		
B40	PETp7	PERp7	A40		
B41	GND	GND	A41		
B42	PRSNTB0#	PRSNTB1#	A42		
	Mechan	ical Key			
B43	GND	GND	A43		
B44	PETn8	PERn8	A44		
B45	PETp8	PERp8	A45		
B46	GND	GND	A46		
B47	PETn9	PERn9	A47		
B48	PETp9	PERp9	A48		
B49	GND	GND	A49		
B50	PETn10	PERn10	A50		
B51	PETp10	PERp10	A51		
B52	GND	GND	A52		
B53	PETn11	PERn11	A53		
B54	PETp11	PERp11	A54		
B55	GND	GND	A55		
B56	PETn12	PERn12	A56		
B57	PETp12	PERp12	A57		
B58	GND	GND	A58		
B59	PETn13	PERn13	A59		
B60	PETp13	PERp13	A60		
B61	GND	GND	A61		
B62	PETn14	PERn14	A62		
B63	PETp14	PERp14	A63		
	1		•		



B64	GND	GND	A64	
B65	PETn15	PERn15	A65	
B66	PETp15	PERp15	A66	
B67	GND	GND	A67	
B68	RFU, N/C	RFU, N/C	A68	
B69	RFU, N/C	RFU, N/C	A69	
B70	PRSNTB3#	RFU, N/C	A70	

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				Rev <u>0.5</u>	01330.35
		ary Connector Pin Definition (x1	6) (4C)		
	Side B	Side A			
B1	+12V/+12V_AUX	GND	A1	Se	Se
B2	+12V/+12V_AUX	GND	A2	ŝ	ŝ
B3	+12V/+12V_AUX	GND	A3	nda	Secondary Connector (x8, 84-pin add-in card)
B4	+12V/+12V_AUX	GND	A4	7	7
B5	+12V/+12V_AUX	GND	A5	G	6 G
B6	+12V/+12V_AUX	GND	A6	ine	ine
B7	BIFO#	SMCLK	A7	6	6
B8	BIF1#	SMDAT	A8	r (x	r (x
B9	BIF2#	SMRST#	A9	16,	,00 00
B10	PERSTO#	PRSNTA#	A10	14	4
B11	+3.3V/+3.3V_AUX	PERST1#	A11	문	ă.
B12	PWRDIS	PRSNTB2#	A12		ado
B13	GND	GND	A13	bbi	÷
B14	REFCLKn0	REFCLKn1	A14	<u> </u>	ន
B15	REFCLKp0	REFCLKp1	A15	Secondary Connector (x16, 140-pin add-in card)	rd)
B16	GND	GND	A16	਼ੁ	
B17	PETn0	PERn0	A17	_	
B18	PETp0	PERp0	A18		
B19	GND	GND	A19		
B20	PETn1	PERn1	A20	-	
B21 B22	PETp1	PERp1	A21		
	GND	GND	A22		
B23	PETn2	PERn2	A23		
B24 B25	PETp2	PERp2 GND	A24 A25	-	
B25 B26	GND		A25 A26		
B20 B27	PETn3	PERn3	A26 A27		
B27 B28	PETp3 GND	PERp3 GND	A27 A28		
DZO		nical Key	AZO		
B29	GND	GND	A29		
B20	PETn4	PERn4	A30		
B30 B31	PETp4	PERp4	A31		
B32	GND	GND	A32		
B33	PETn5	PERn5	A33		
B33	PETp5	PERp5	A34	-	
B35	GND	GND	A35		
B36	PETn6	PERn6	A36		
B37	РЕТрб	PERp6	A37		
B38	GND	GND	A38		
B39	PETn7	PERn7	A39		
B35 B40	PETp7	PERp7	A40		
B40 B41	GND	GND	A41		
B41 B42	PRSNTB0#	PRSNTB1#	A42		
		nical Key			
B43	GND	GND	A43		
B44	PETn8	PERn8	A44		
B45	PETp8	PERp8	A45		
B46	GND	GND	A46		
B47	PETn9	PERn9	A47		
B48	PETp9	PERp9	A48		
B49	GND	GND	A49		
B50	PETn10	PERn10	A50		
B51	PETp10	PERp10	A51		
			-		•

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B52	GND	GND	A52	
B53	PETn11	PERn11	A53	
B54	PETp11	PERp11	A54	
B55	GND	GND	A55	
B56	PETn12	PERn12	A56	
B57	PETp12	PERp12	A57	
B58	GND	GND	A58	
B59	PETn13	PERn13	A59	
B60	PETp13	PERp13	A60	
B61	GND	GND	A61	
B62	PETn14	PERn14	A62	
B63	PETp14	PERp14	A63	
B64	GND	GND	A64	
B65	PETn15	PERn15	A65	
B66	PETp15	PERp15	A66	
B67	GND	GND	A67	
B68	RFU, N/C	RFU, N/C	A68	
B69	RFU, N/C	RFU, N/C	A69	
B70	PRSNTB3#	RFU, N/C	A70	

3.4 Signal Descriptions – Common

The pins shown in this section are common to both the Primary and Secondary Connectors. All pin directions are from the perspective of the baseboard.

The add-in card shall implement protection methods to prevent leakage paths between the Vaux and Vmain power domains in the event that a NIC is powered down in a powered up baseboard.

Note: Pins that are only used on Primary Connector 28-pin OCP bay are defined in Section 3.5.

3.4.1 PCIe Interface Pins

This section provides the pin assignments for the PCIe interface signals. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0. Example connection diagrams for are shown in Figure <u>72Figure 58</u>.

Signal Name	Pin #	Baseboard Direction	Signal Description
REFCLKn0	B14	Output	PCIe compliant differential reference clock #0, and
REFCLKp0	B15		#1. 100MHz reference clocks are used for the add-in
REFCLKn1	A14	Output	card PCIe core logic.
REFCLKp1	A15		
			For baseboards, the REFCLK0 and REFCLK1 signals
			shall be available at the connector. Baseboards shall
			disable REFCLK1 if it is not used by the add-in card.
			For add-in cards, the required REFCLKs shall be
			connected per the endpoint datasheet. Unused

Table 1514: Pin Descriptions – PCIe 1

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			REFCLKs on the add-in card shall be left as a no
			connect.
			Note: For cards that only support 1 x16, REFCLK0 is used. For cards that support 2 x8, REFCLK0 is used for the first eight PCIe lanes, and REFCLK1 is used for the second eight PCIe lanes.
			Refer to Section 2.1 in the PCIe CEM Specification, Rev 4.0 for electrical details.
PETn0	B17	Output	Transmitter differential pairs [0:15]. These pins are
PETp0	B18		connected from the baseboard transmitter
PETn1	B20	Output	differential pairs to the receiver differential pairs on
PETp1	B21		the add-in card.
PETn2	B23	Output	
PETp2	B24		The PCIe transmit pins shall be AC coupled on the
PETn3	B26	Output	baseboard with capacitors. The capacitors shall be
РЕТр3	B27		placed next to the baseboard transmitters. The AC
PETn4	B30	Output	coupling capacitor value shall be between 176nF
PETp4	B31		(min) and 265nF (max).
PETn5	B33	Output	
РЕТр5	B34		For baseboards, the PET[0:15] signals are required at
PETn6	B36	Output	the connector.
РЕТр6	B37		
PETn7	B39	Output	For add-in cards, the required PET[0:15] signals shall
РЕТр7	B40		be connected to the endpoint silicon. For silicon that
PETn8	B44	Output	uses less than a x16 connection, the appropriate
РЕТр8	B45		PET[0:15] signals shall be connected per the endpoint
PETn9	B47	Output	datasheet.
РЕТр9	B48		Defer to Section 6.1 in the DCIs CEM Specification
PETn10	B50	Output	Refer to Section 6.1 in the PCIe CEM Specification,
PETp10	B51		Rev 4.0 for details.
PETn11	B53	Output	
PETp11	B54		
PETn12	B56	Output	
PETp12	B57		
PETn13	B59	Output	
PETp13	B60		
PETn14	B62	Output	
PETp14	B63		
PETn15	B65	Output	
PETp15	B66		
PERn0	A17	Input	Receiver differential pairs [0:15]. These pins are
PERp0	A18		connected from the add-in card transmitter
PERn1	A20	Input	differential pairs to the receiver differential pairs on
PERp1	A21		the baseboard.
PERn2	A23	Input	
L	1		I.



PERp2	A24		The PCIe receive pins shall be AC coupled on the add-
PERn3	A26	Input	in card with capacitors. The capacitors shall be placed
PERp3	A27		next to the add-in card transmitters. The AC coupling
PERn4	A30	Input	capacitor value shall be between 176nF (min) and
PERp4	A31		265nF (max).
PERn5	A33	Input	
PERp5	A34		For baseboards, the PER[0:15] signals are required at
PERn6	A36	Input	the connector.
PERp6	A37		
PERn7	A39	Input	For add-in cards, the required PER[0:15] signals shall
PERp7	A40		be connected to the endpoint silicon. For silicon that
PERn8	A44	Input	uses less than a x16 connection, the appropriate
PERp8	A45		PER[0:15] signals shall be connected per the endpoint
PERn9	A47	Input	datasheet.
PERp9	A48		
PERn10	A50	Input	Refer to Section 6.1 in the PCIe CEM Specification,
PERp10	A51		Rev 4.0 for details.
PERn11	A53	Input	
PERp11	A54		
PERn12	A56	Input	
PERp12	A57		
PERn13	A59	Input	
PERp13	A60		
PERn14	A62	Input	
PERp14	A63		
PERn15	A65	Input	
PERp15	A66		
PERSTO#	B10	Output	PCIe Reset #0, #1. Active low.
PERST1#	A11		
			When PERSTn# is deasserted, the signal shall indicate
			the applied power is within tolerance and stable for
			the add-in card.
			PERST# shall be deasserted at least 100ms after the
			power rails are within the operating limits per the
			PCIe CEM Specification. The PCIe REFCLKs shall also
			become stable within this period of time.
			PERST shall be pulled high to 3.3Vaux on the
			baseboard.
			For OCP NIC 3.0, PERST deassertion shall also indicate
			the full card power envelope is available to the add-in
			card.

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For baseboards, the PERST[0:1]# signals are required at the connector.
For add-in cards, the required PERST[0:1]# signals shall be connected to the endpoint silicon. <u>Unused</u> <u>PERST[0:1]# signals shall be left as a no connect.</u>
Note: For cards that only support 1 x16, PERSTO# is used. For cards that support 2 x8, PERSTO# is used for the first eight PCIe lanes, and PERST1# is used for the second eight PCIe lanes.
Refer to Section 2.2 in the PCIe CEM Specification, Rev 4.0 for details.

3.4.2 PCIe Present and Bifurcation Control Pins

This section provides the pin assignments for the PCIe present and bifurcation control signals. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure

The PRSNTA#/PRSNTB[0:3]# state shall be used to determine if a card has been physically plugged in. The BIF[0:2]# pins shall be latched before PWRDIS deassertion to ensure the correct values are detected by the system. Changing the pin states after this timing window is not allowed. Refer to the AC timing diagram in Section XXX for details.

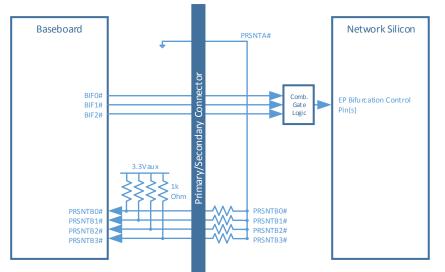
Signal Name	Pin #	Baseboard Direction	Signal Description
PRSNTA#	A12 A10	Output	Present A is used for add-in card presence and PCIe capabilities detection.
			For baseboards, this pin shall be directly connected to GND.
			For add-in cards, this pin shall be directly connected to the PRSNTB[3:0]# pins.
PRSNTBO# PRSNTB1# PRSNTB2#	B42 A42 <u>A10A12</u>	Input	Present B [0:3]# are used for add-in card presence and PCIe capabilities detection.
PRSNTB3#	B70		For baseboards, these pins shall be connected to the I/O hub and pulled up to +3.3Vaux using 1kOhm resistors.
			For add-in cards, these pins shall be strapped to PRSNTA# per the encoding definitions described in Section 3.6.

Table <u>1615</u>: Pin Descriptions – PCIe Present and Bifurcation Control Pins



			Note: PRSNTB3# is located at the bottom of the 4C connector and is only applicable for add-in cards with a PCIe width of x16 (or greater). Add-in cards that implement a 2C card edge do not use the PRSNTB3# pin for capabilities or present detection.
BIFO# BIF1# BIF2#	A7 <u>B7</u> A8 <u>B8</u> A9B9	Output	Bifurcation [0:2]# pins allow the baseboard to force configure the add-in card bifurcation.
0.12			For baseboards, these pins shall be outputs driven from the baseboard I/O hub and allow the system to force configure the add-in card bifurcation. The baseboard may optionally tie the BIF[0:2]# signals to 3.3Vaux or to ground per the definitions are described in Section 3.6 if no dynamic bifurcation configuration is required.
			For add-in cards, these signals shall connect to the endpoint bifurcation pins if it is supported.
			Note: the required combinatorial logic output for endpoint bifurcation is dependent on the specific silicon and is not defined in this specification.







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This section provides the pin assignments for the SMBus interface signals. The AC/DC specifications are defined in the SMBus 2.0 and I²C bus specifications. An example connection diagram is shown in Figure XXX.

Signal Name	Pin #	Baseboard Direction	Signal Description
SMCLK	A7	Output, OD	SMBus clock. Open drain, pulled up to 3.3Vaux on the baseboard.
			For baseboards, the SMCLK from the platform SMBus master shall be connected to the connector.
			For add-in cards, the SMCLK from the endpoint silicon shall be connected to the card edge gold fingers.
SMDAT	A8	Input / Output, OD	SMBus Data. Open drain, pulled up to 3.3Vaux on the baseboard.
			For baseboards, the SMDAT from the platform SMBus master shall be connected to the connector.
			For add-in cards, the SMDAT from the endpoint silicon shall be connected to the card edge gold fingers.
SMRST#	A9	Output, OD	SMBus reset. Open drain.
			For baseboards, this pin shall be pulled up to 3.3Vaux. The SMRST pin may be used to reset optional downstream SMBus devices (such as temperature sensors). The SMRST# implementation shall be mandatory for baseboard implementations.
			For add-in cards, SMRST# is optional and is dependent on the add-in card implementation. <u>The SMRST# signal shall be left as a no connect if it is not used on the add-in card.</u>

3.4.4 Power Supply Pins

This section provides the pin assignments for the power supply interface signals. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0 and amended in Section 3.10. An example connection diagram is shown in <u>Figure 61Figure 47</u>.

Table 1817: Pin Descriptions – Power

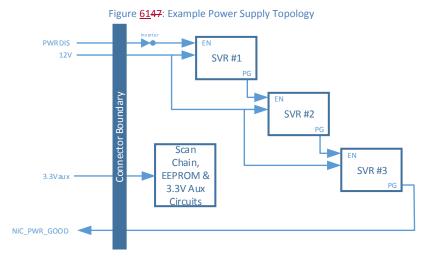
Signal Name	Pin #	Baseboard	Signal Description
		Direction	

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GND	Various	GND	Ground return; a total of 46 ground pins are on the
			main 140-pin connector area. <u>Refer to Section 3.3 for</u> details.
+12V/+12V_AUX	B1, B2, B3, B4, B5, B6	Power	12V main or 12V Aux power; total of 6 pins per connector. The 12V pins shall be rated to 1.1A per pin with a maximum derated power delivery of 80W.
			The +12V power pins shall be within the rail tolerances as defined in Section 3.10 when the PWRDIS pin is driven low by the baseboard.
+3.3V/3.3V_AUX	B11	Power	3.3V main or 3.3V Aux power; total of 1 pin per connector. The 3.3V pin shall be rated to 1.1A for a maximum derated power delivery of 3.63W. The 3.3Vaux/main power pin shall be within the rail tolerances as defined in Section 3.10 when the
PWRDIS	B12	Output, O/D	 PWRDIS pin is driven low by the baseboard. Power disable. Active high. Open-drain This signal shall be pulled up to 3.3V through a 10kOhm resistor on the baseboard. When high, all add-in card supplies shall be disabled. When low, add-in card supplies shall be enabled.



3.4.5 Miscellaneous Pins

This section provides the pin assignments for the miscellaneous interface signals.

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Table 1918: Pin Descriptions – Miscellaneous 1			
Signal Name	Pin #	Baseboard	Signal Description
		Direction	
RFU, N/C	B68,	Input /	Reserved future use pins. These pins shall be left as
	B69,	Output	no connect.
	A68,		
	A69, A70		

3.5 Signal Descriptions – OCP Bay (Primary Connector)

The following section describes the functions in the Primary Connector 28-pin OCP bay. This 28-pin bay is shown in Section 3.3 and have pin numbers designated as OCP_B[1:14], and OCP_A[1:14]. All pin directions on this OCP bay are from the perspective of the baseboard.

The add-in card shall implement protection methods to prevent leakage paths between the Vaux and Vmain power domains in the event that a NIC is powered down in a powered up baseboard.

Note: The pins that are common to both the Primary and Secondary Connectors are defined in Section 3.4.

3.5.1 PCIe Interface Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the PCIe interface signals on the Primary Connector OCP bay. The AC/DC specifications are defined in Section XXX. An example connection diagram that shows REFCLK2, REFCLK3, PERST2# and PERST3# is shown in Section 3.7.

		Table <u>20</u> 19: Pin	Descriptions – PCIe 2
Signal Name	Pin #	Baseboard	Signal Description
		Direction	
REFCLKn2	OCP_B11	Output	PCIe compliant differential reference clock #2, and
REFCLKp2	OCP_B12		#3. 100MHz reference clocks are used for the add-in
REFCLKn3	OCP_A11	Output	card PCIe core logic.
REFCLKp3	OCP_A12		
			For baseboards, the REFCLK2 and REFCLK3 signals
			are required at the Primary connector. Baseboards
			shall disable REFCLK2 and REFCLK3 if they are not
			used by the add-in card.
			For add-in cards, the required REFCLKs shall be
			connected per the endpoint datasheet. Unused
			REFCLKs on the add-in card shall be left as a no
			connect.
			Note: REFCLK2 and REFCLK3 are not used for cards
			that only support a 1 x16, 1 x8 or 2 x8 connection.



			Refer to Section 2.1 in the PCIe CEM Specification, Rev 4.0 for details.
PERST2#	OCP_A1	Output	PCIe Reset #2, #3. Active low.
PERST3#	OCP_A2		When PERSTn# is deasserted, the signal shall indicate the applied power is within tolerance and stable for the add-in card.
			PERST# shall be deasserted at least 100ms after the power rails are within the operating limits per the PCIe CEM Specification. The PCIe REFCLKs shall also become stable within this period of time.
			PERST shall be pulled high to 3.3Vaux on the baseboard.
			For OCP NIC 3.0, PERST deassertion shall also indicate the full card power envelope is available to the add-in card.
			For baseboards, the PERST[0:12:3]# signals are required at the connector.
			For add-in cards, the required PERST[0:12:3]# signals shall be connected to the endpoint silicon. Unused PERST[2:3]# signals shall be left as a no connect.
			Note: PERST2# and PERST3# are not used for cards that only support a 1 x16 or 2 x8 connection.
			Refer to Section 2.2 in the PCIe CEM Specification, Rev 4.0 for details.
WAKE#	OCP_A3	Input, OD	WAKE#. Open drain. Active low.
			This signal shall be driven by the add-in card to notify the baseboard to restore PCIe link. For add-in cards that support multiple WAKE# signals, their respective WAKE# pins may be tied together as the signal is open-drain to form a wired-OR.
			For baseboards, this signal shall be pulled up to +3.3V on the baseboard with a 10kOhm resistor. This signals shall be connected to the system WAKE# signal.
			For add-in cards, this signal shall be directly connected to the endpoint silicon WAKE# pin(s). This

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pin shall be left as a no connect if WAKE# is not supported by the silicon.
Refer to Section 2.3 in the PCIe CEM Specification, Rev 4.0 for details.



3.5.2 NC-SI Over RBT Interface Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the NC-SI over RBT interface signals on the Primary Connector OCP bay. The AC/DC specifications are defined in the NC-SI specification. An example connection diagram is shown in Figure 62Figure 48.

Table <u>21</u> 20: Pin Descriptions – NC-SI Over RBT			
Signal Name	Pin #	Baseboard Direction	Signal Description
RBT_CLK_IN	OCP_A14	Output	Reference clock input. Synchronous clock reference for receive, transmit and control interface. The clock shall have a nominal frequency of 50MHz ±100ppm. For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the Primary connector OCP bay. This signal requires a 100kOhm
			pull down resistor on the baseboard. If the baseboard does not support NC-SI over RBT, then this signal shall be terminated to ground through a 100kOhm pull down resistor.
			For add-in cards, this pin shall be connected between the gold finger to the endpoint silicon. This pin shall be left as a no connect if NC-SI is not supported.
RBT_CRS_DV	OCP_B14	Input	Carrier sense/receive data valid. This signal is used to indicate to the baseboard that the carrier sense/receive data is valid.
			For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull down resistor on the baseboard. If the baseboard does not support NC-SI over RBT, then this signal shall be terminated to ground through a 100kOhm pull down resistor.
			For add-in cards, this pin shall be connected between the gold finger to the endpoint silicon. This pin shall be left as a no connect if NC-SI is not supported.
RBT_RXD0 RBT_RXD1	OCP_B9 OCP_B8	Input	Receive data. Data signals from the network controller to the BMC.
			For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull-up resistor to 3.3Vaux on the baseboard. If the baseboard does not support NC-SI over RBT, then

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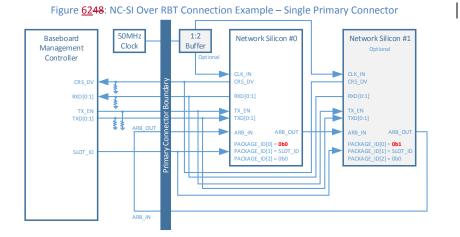
			Rev <u>0.55</u> 09550.50
			this signal shall be terminated to 3.3Vaux through a 100kOhm pull-up.
			For add-in cards, this pin shall be connected between the gold finger and the RBT_RXD[0:1] pins on endpoint silicon. This pin shall be left as a no connect if NC-SI is not supported.
RBT_TX_EN	OCP_A7	Output	Transmit enable.
			For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull down resistor to ground on the baseboard. If the baseboard does not support NC-SI over RBT, then this signal shall be terminated to ground through a 100kOhm pull down.
			For add-in cards, this pin shall be connected between the gold finger to the endpoint silicon. This pin shall be left as a no connect if NC-SI is not supported.
RBT_TXD0 RBT_TXD1	OCP_A9 OCP_A8	Output	Transmit data. Data signals from the BMC to the network controller.
			For baseboards, this pin shall be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull-up resistor to 3.3Vaux on the baseboard. If the baseboard does not support NC-SI over RBT, then this signal shall be terminated to 3.3Vaux through a 100kOhm pull-up.
			For add-in cards, this pin shall be connected between the gold finger to the RBT_TXD[0:1] pins on the endpoint silicon. This pin shall be left as a no connect if NC-SI is not supported.
RBT_ARB_OUT	OCP_A5	Output	NC-SI hardware arbitration output. This pin shall only be used if the endpoint silicon supports hardware arbitration. This pin shall be connected to the RBT_ARB_IN signal of an adjacent device in the hardware arbitration ring.
			The baseboard shall implement a multiplexing implementation that directs the RBT_ARB_OUT to the RBT_ARB_IN pin of the next NC-SI capable device in the ring, or back to the RBT_ARB_IN pin of the source device if there is a single device on the ring.



RBT_ARB_IN	OCP_A4	Input	For baseboards, this pin shall be connected between the baseboard OCP connector(s) to complete the hardware arbitration ring. If the baseboard does not support NC-SI over RBT, this signal shall be directly connected to the RBT_ARB_IN pin to allow a complete hardware arbitration ring on the add-in card. For add-in cards, this pin shall be connected from the gold finger to the RBT_ARB_IN pin on the endpoint silicon. This pin shall be left as a no connectdirectly connected to the card edge RBT_ARB_IN pin if NC-SI is not supported. This allows the hardware arbitration signals to pass through in a multi-primary connector baseboard. NC-SI hardware arbitration input. This pin shall only be used if the endpoint silicon supports hardware arbitration. This pin shall be connected to the RBT_ARB_OUT signal of an adjacent device in the hardware arbitration ring. The baseboard shall implement a multiplexing implementation that directs the RBT_ARB_IN to the RBT_ARB_OUT pin of the next NC-SI capable device in the ring, or back to the RBT_ARB_OUT pin of the source device if there is a single device on the ring. For baseboards, this pin shall be connected between the baseboard OCP connector(s) to complete the hardware arbitration ring. If the baseboard does not support NC-SI over RBT, this signal shall be directly connected to the RBT_ARB_OUT pin on the endpoint silicon. Leave this pin as a no connect if NC- SI is not supported_This pin shall be connected between the gold finger to the RBT_ARB_OUT pin on the endpoint silicon. Leave this pin as a no connect if NC- SI is not supported_This pin shall be directly connected to the card edge RBT ARB_OUT pin if NC- SI is not supported_This pin shall be directly connected to the card edge RBT ARB_OUT pin if NC- SI is not supported. This allows the hardware arbitration signals to pass through in a multi-primary connector baseboard.
SLOT_ID	OCP_B7	Output	NC-SI Address pin. This pin shall only be used if the end point silicon supports package identification.

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For baseboards, this pin shall be used to identify the slot ID value. This pin shall be directly to GND for SlotID = 0. This pin shall be pulled up to 3.3Vaux for SlotID = 1.
For add-in cards, this pin shall be connected to the endpoint device GPIO associated with the Package ID[1] field. Refer to Section <u>4.8.1</u> 4.9.1 and the device datasheet for details.
For add-in cards with multiple endpoint devices, the SLOT_ID pin may be used to configure a different Package ID value so long as the resulting combination does not cause addressing interferences.
For endpoint devices without NC-SI support, this pin shall be left as a no connect on the add-in card.





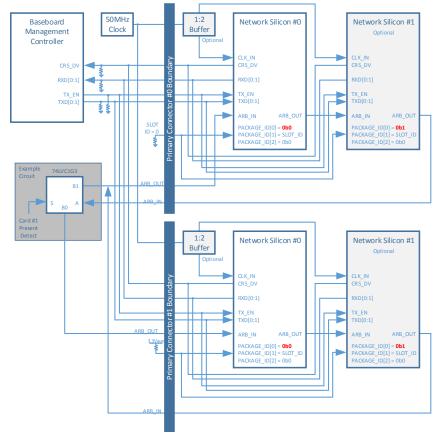


Figure <u>6349</u>: NC-SI Over RBT Connection Example – Dual Primary Connector

Note 1: For baseboard designs with a single Primary Connector, connect ARB_IN to ARB_OUT to complete the NC-SI hardware arbitration ring. For designs with multiple Primary Connectors, connect ARB_IN and ARB_OUT to an analog mux to complete the NC-SI arbitration ring based on the number of cards installed in the system. An example dual Primary Connector implementation is shown in Figure

Note 2: For add-in cards with two discrete endpoint silicon, the Package ID[0] bit shall be statically set based on its silicon instance. For example, the figure above shows Network Silicon #0 and Network Silicon #1. Network Silicon #0 has Package ID[0] = 0b0, Network Silicon #1 has Package ID[0] = 0b1.

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3.5.3 Scan Chain Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the Scan Bus interface signals on the Primary Connector OCP Bay. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in <u>Figure 64 Figure 50</u>.

Table 2221: Pin Descriptions – Scan Chain			
Signal Name	Pin #	Baseboard Direction	Signal Description
CLK	OCP_B6	Output	Scan clock. The CLK is an output pin from the baseboard to the add-in card. The CLK may run up to 12.5MHz. For baseboard implementations, the CLK pin shall be connected to the Primary Connector. The CLK pin shall be tied directly to GND if the scan chain is not
	OCD DE	Output	used. For NIC implementations, the CLK pin shall be connected to Shift Registers 0 & 1, and optionally connected to Shift Registers 2 & 3 (if implemented) as defined in the text and Figure 64Figure 50, below. The CLK pin shall be pulled up to 3.3Vaux through a 1kOhm resistor.
DATA_OUT	OCP_B5	Output	Scan clock data output from the baseboard to the add-in card. This bit stream is used to shift in NIC configuration data. For baseboard implementations, the DATA_OUT pin shall be connected to the Primary Connector. The DATA_OUT pin shall be tied directly to GND if the scan chain is not used. For NIC implementations, the DATA_OUT pin may be left floating if it is not used for add-in card configuration. The DATA_OUT pin shall be pulled up to 3.3Vaux through a 1kOhm resistor.
DATA_IN	OCP_B4	Input	Scan clock data input to the baseboard. This bit stream is used to shift out NIC status bits. For baseboard implementations, the DATA_IN pin shall be pulled up to 3.3Vaux through a 10kOhm resistor to prevent the input signal from floating if a card is not installed. This pin may be left as a no connect if the scan chain is not used. For NIC implementations, the DATA_IN scan chain is required. The DATA_IN pin shall be connected to Shift

Table 2221: Pin Descriptions – Scan Chain



			Registers 0 & 1, as defined in the text and <u>Figure</u> <u>64Figure 50</u> .
LD#	OCP_B3	Output	Scan clock shift register load. Used to latch configuration data on the add-in card.
			For baseboard implementations, the LD# pin shall be pulled up to 3.3Vaux through a 1kOhm resistor if the scan chain is not used to prevent the add-in card from erroneous data latching.
			For NIC implementations, the LD# pin implementation is required. The LD# pin shall be connected to Shift Registers 0 & 1 as defined in the text and <u>Figure 64</u> Figure 50. The LD# pin shall be pulled up to 3.3Vaux through a 1kOhm resistor.

The scan chain provides side band status indication between the add-in card and the baseboard. The scan chain bit definition is defined in the two tables below. The scan chain data stream is 32-bits in length for both the DATA_OUT and the DATA_IN streams. The scan chain implementation is optional on the host, but is mandatory on all OCP NIC 3.0 cards. The scan chain components operates on the 3.3Vaux power domain.

The DATA_OUT bus is an output from the host. The DATA_OUT bus provides initial configuration options to the add-in card. At the time of this writing, the default implementation does not use the DATA_OUT stream and is not implemented on the NIC. However, all baseboard systems that implement the Scan Chain shall connect DATA_OUT between the platform and the Primary Connector for future-proofing NIC implementations and subsequent revisions of this specification.

Table <u>23</u>2: Pin Descriptions – Scan Chain DATA_OUT Bit Definition

Byte.bit	DATA_OUT Field	Default	Description
	Name	Value	
0.[07]	RSVD	0b00000	Reserved. Byte 0 value is 0h00.
1.[07]	RSVD	0h00	Reserved. Byte 1 value is 0h00.
2.[07]	RSVD	0h00	Reserved. Byte 2 value is 0h00.
3.[07]	RSVD	0h00	Reserved. Byte 3 value is 0h00.

The DATA_IN bus is an input to the host and provides NIC status indication. The default implementation is completed with two 8-bit 74LV165 parallel in to serial out shift registers in a cascaded implementation. Up to four shift registers may be implemented to provide additional NIC status indication to the host platform.

DATA_IN shift registers 0 & 1 shall be mandatory for scan chain implementations. DATA_IN shift registers 2 & 3 are optional depending on the card type and fields being reported to the host. DATA_IN shift register 2 may be used to indicate future definitions of the scan chain bit stream. DATA_IN shift registers 3 (in conjunction with shift register 2) are required for reporting link/activity indication on card implementations with 5-8 ports.

Commented [TN10]: Need to discuss this (see Hamel's comment in prior sections regarding making the scan chain mandatory on the AIC)

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The host should read the DATA_IN bus multiple (TBD) times to qualify the incoming data stream.

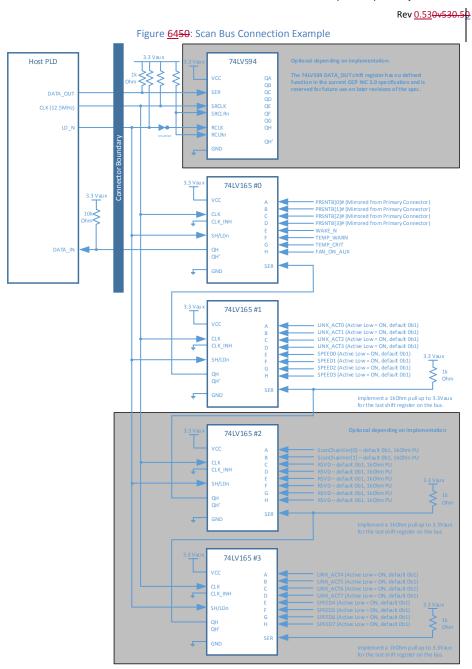
A 1kOhm pull up resistor shall be implemented on the NIC to the SER input of the last shift register on the DATA_IN scan chain to maintain a default bit value of 0b1 for unused bits for implementations using less than four shift registers.

Byte.bit	DATA_OUT Field	Default	Description
	Name	Value	
0.0	PRSNTB[0]#	0bX	PRSNTB[3:0]# bits shall reflect the same state as
0.1	PRSNTB[1]#	0bX	the signals on the Primary Connector.
0.2	PRSNTB[2]#	0bX	
0.3	PRSNTB[3]#	0bX	
0.4	WAKE_N	0bX	PCIe WAKE_N signal shall reflect the same state as the signal on the Primary Connector.
0.5	TEMP_WARN	0b0	Temperature monitoring pin from the on-card thermal solution. This pin shall be asserted high when temperature sensor exceeds the temperature warning threshold.
0.6	TEMP_CRIT	0b0	Temperature monitoring pin from the on-card thermal solution. This pin shall be asserted high when temperature sensor exceeds the temperature critical threshold.
0.7	FAN_ON_AUX	0b0	When high, FAN_ON_AUX shall request the system fan to be enabled for extra cooling in the S5 state.
1.0	LINK_ACT_P0	0b1	Port 03 link/activity indication. Active low.
1.1	LINK_ACT_P1	0b1	
1.2	LINK_ACT_P2	0b1	0b0 – Link LED is illuminated on the host platform.
1.3	LINK_ACT <u>P</u> 3	0b1	0b1 – Link LED is not illuminated on the host platform.
			 Steady = link is detected on the port. Blinking = activity is detected on the port. The blink rate should blink low for 50-500ms during activity periods. Off = the physical link is down or disabled
1.4	SPEED_A_P0	0b1	Port 03 speed A (max rate) indication. Active low.
1.5	SPEED_A_P1	0b1	
1.6	SPEED_A_P2	0b1	0b0 – Port is linked at maximum speed.
1.7	SPEED_A_P3	0b1	0b1 – Port is not linked at the maximum speed or no link is present.
2.0	ScanChainVer[0]	0b1	ScanChainVer[1:0] shall be used to indicate the
2.1	ScanChainVer[1]	0b1	scan chain bit definition version. The encoding shall be as follows:



			0b11 – Scan chain bit definition version 1 corresponding to OCP NIC 3.0 version 1.0.
			All other encoding values shall be reserved.
2.2	RSVD	0b1	Byte 2 bits [2:7] are reserved. These bits shall
2.3	RSVD	0b1	default to the value of 0b1. These bits may be used
2.4	RSVD	0b1	in future versions of the scan chain.
2.5	RSVD	0b1	
2.6	RSVD	0b1	
2.7	RSVD	0b1	
3.0	LINK_ACT_P4	0b1	Port 47 link/activity indication. Active low.
3.1	LINK_ACT_P5	0b1	
3.2	LINK_ACT_P6	0b1	0b0 – Link LED is illuminated on the host platform.
3.3	LINK_ACT_P7	Ob1	0b1 – Link LED is not illuminated on the host platform.
			Steady = link is detected on the port. Blinking = activity is detected on the port. The blink rate should blink low for 50-500ms during activity periods. Off = the physical link is down or disabled
3.4	SPEED_A <u>P</u> 4	0b1	Port 47 speed A (max rate) indication. Active low.
3.5	SPEED_A <u>P</u> 5	0b1	
3.6	SPEED_A_P6	0b1	0b0 – Port is linked at maximum speed.
3.7	SPEED_A_P7	0b1	0b1 – Port is not linked at the maximum speed or no link is present.

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3.5.4 Primary Connector Miscellaneous Pins – OCP Bay (Primary Connector)

This section provides the miscellaneous pin assignments for the pins on the Primary Connector OCP Bay. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0 and Section 3.12. An example connection diagram is shown in Figure XXX.

Signal Name	Pin #	Baseboard Direction	Signal Description
PWRBRK#	OCP_B2	Output, OD	Power break. Active low, open drain.
			This signal shall be pulled up to 3.3Vaux on the add in card with a minimum of 95kOhm. The pull up on the baseboard shall be a stiffer resistance in-order to meet the timing specs as shown in the PCIe CEM Specification.
			When this signal is driven low by the baseboard, the Emergency Power Reduction State is requested The add-in card shall move to a lower power consumption state.
NIC_PWR_GOOD	OCP_B1	Input	NIC Power Good. Active high. This signal is driven by the add-in card.
			When high, this signal shall indicate that all of the add-in card power rails are operating within nominal tolerances.
			When low, this signal shall indicate that the add-in card power supplies are not yet within nominal tolerances or are in a fault condition.
			For baseboards, this pin may be connected to the platform I/O hub as a NIC power health status indication. This signal shall be pulled down to ground with a 100kOhm resistor on the baseboard to prevent a false power good indication if no add- in card is present.
			For add-in cards this signal shall indicate the add-in card power is "good". This signal may be implemented by a cascaded power good or a discrete power good monitor output.
GND	OCP_A6 OCP_A10 OCP_A13 OCP B10	GND	Ground return; a total of 5 ground pins are on the OCP bay area.

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OCP_B13		

3.6 PCIe Bifurcation Mechanism

OCP3.0 baseboards and add-in cards support multiple bifurcation combinations. Single socket baseboards with a single or multiple root ports, as well as a multi-socket baseboards with a single or multiple root ports are supported. The bifurcation mechanism also supports add-in cards with a single or multiple end points. These features are accomplished via I/O pins on the Primary and Secondary connector:

- PRSNTA#, PRSNTB[3:0]#. The PRSNTA# pin shall connect to the PRSNTB# pins as a hard coded value on the add-in card. The encoding of the PRSNTB[3:0]# pins allows the baseboard to determine the PCIe Links available on the add-in card.
- BIF[3:0]#. The BIF# pin states shall be controlled by the baseboard to allow the baseboard to override the default end point bifurcation for silicon that support bifurcation. Additional combinatorial logic is required and is specific to the card silicon. The combinatorial logic is not covered in this specification. The BIF[3:0]# pins may optionally be hardcoded for baseboards that do not require a dynamic bifurcation override.

A high level bifurcation connection diagram is shown in Figure 65 Figure 51.

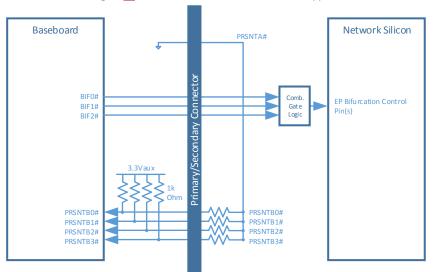


Figure 6551: PCIe Bifurcation Pin Connections Support



3.6.1 PCIe Add-in Card to Baseboard Bifurcation Configuration (PRSNTA#, PRSNTB[3:0]#)

The add-in card to baseboard configuration mechanism consists of four dual use pins (PRSNTB[3:0]#) on the add-in card and a grounded PRSNTA# pin on the baseboard. These pins provide card presence detection as well as mechanism to notify the baseboard of the pre-defined PCIe lane width capabilities. The PRSNTB[3:0]# pins are pulled up to 3.3Vaux on the baseboard and are active low signals. A state of 0b1111 indicates that no card is present in the system. Depending on the capabilities of the add-in card, a selection of PRSNTB[3:0]# signals may be strapped to the PRSNTA# signal and is pulled low by the baseboard. The encoding of the PRSTNB[3:0]# bits is shown in <u>Table 26Table 25</u> for x16 and x8 PCIe

3.6.2 PCIe Baseboard to Add-in Card Bifurcation Configuration (BIF[2:0]#)

Three signals (BIF[2:0]#) are driven by the baseboard to notify requested bifurcation on the add-in card silicon. This allows the baseboard to set the lane configuration on the add-in card that supports multiple bifurcation options.

For example, a baseboard that has four separate hosts that support a 4 x4 connection, should appropriately drive the BIF[2:0]# pins per <u>Table 26</u>Table 25 and indicate to the add-in card silicon to configuration.

As previously noted, the BIF[2:0]# signals require additional combinatorial logic to decode the BIF[2:0]# value and appropriately apply it to the end-point silicon. The combinatorial logic is not covered in the specification as its implementation is specific to the vendor silicon used.

3.6.3 PCIe Bifurcation Decoder

The combination of the PRSNTB[3:0]# and BIF[2:0]# pins deterministically sets the PCIe lane width for a given combination of baseboard and add-in cards. <u>Table 26</u>Table <u>25</u> shows the resulting number of PCIe its width for known combinations of baseboards and add-in cards.

*Note: The baseboard must disable PCIe lanes during the initialization phase if the number of detected PCIe links are greater than what is supported on the baseboard to prevent a nondeterministic solution. For example, if the baseboard only supports a 1 x16 connection, and the add-in card only supports a 2 x8 connection, the baseboard must disable PCIe lanes 8-15 to prevent any potential LTSSM issues during the discovery phase.

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Table 2625: PCIe Bifurcation Decoder for x16 and x8 Card Widths



Matrix functional Matrix functional <	_			-			Single Host	Host			RSVD		Quad Host	Quad Host
Number of the condition of the conditicon of the condition of the condition of the condition of the co				Host	1 Host	1 Host	1 Host	1 Host	1 Host		BSVD	2 Hosts	4 Hosts	4 Hosts
Memoricality functional function				Host CPU Sockets	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	2 Upstream Sockets	4 Upstream Sockets		UNSH	2 Upstream Sockets [1 Sooket per Host]		4 Sockets (1 Socket per Host) First 8 PCle lanes
Anticipation Second (1) Text (1)		Network Car Supported P	d - Ole Configurations	Total PCIe Links	1Link (No Bifurcation)	1 or 2 Links	1, 2, or 4 Links	2 Links	4 Links	4 x2 links	RSVD	2 Links	4 Links	4 x2 links
Note Section 2-2-10 Section 2-2-2-10 Section 2-2-2-2-10 Section 2-2-2-10				System Support	1x16, 1x6, 1x4, 1x2, 1x1	1x16, 1x8, 1x4, 1x2, 1x1	1x16, 1x6, 1x4, 1x2, 1x1	1x8,1x4,1x2,1x1			RSVD			
Current control						2 x8, 2 x4, 2 x2, 2 x1	2x8,2x4,2x2,2x1	2 k8, 2 k4, 2 k2, 2 k1				2x8,2x4,2x2,2x1		
Image: constraint of the	Minimum						4×4,4×2,4×1		4 ×4, 4 ×2, 4×1	4×2,4×1			4×4,4×2,4×1	4×2,4×1
Lot of Static	Required			System Encoding BIF[2:0]*	00000	0000	00000	00001	06010	06011	0b100	06101	06110	0b111
Me/Direct Diffic Diffic <thdiffic< th=""> <thdiffic< th=""> <thdiffic<< th=""><th>Card Edge</th><th>Card Short Name</th><th>Supported Bifurcation Modes</th><th></th><th>1</th><th></th><th></th><th>'</th><th></th><th></th><th>•</th><th></th><th></th><th></th></thdiffic<<></thdiffic<></thdiffic<>	Card Edge	Card Short Name	Supported Bifurcation Modes		1			'			•			
			Card Not Present		BSVD - Card not present in	hite sustem								
Indicator Indicator <t< th=""><th></th><th></th><th>1×8.1×4.1×2.1×1</th><th></th><th>1×8</th><th>120</th><th>1×8</th><th>1×8</th><th>4×1</th><th>12</th><th></th><th>1×8</th><th>1×4</th><th>1/2</th></t<>			1×8.1×4.1×2.1×1		1×8	120	1×8	1×8	4×1	12		1×8	1×4	1/2
	2C	1x8 Option A						(Sooket 0 only)	(Socket 0 only)	(Socket 0 only)		(Host 0 only)	(Host 0 only)	(Host 0 only)
			1x4,1x2,1x1	061110	1×4	ž	1x4	1:4	₩ ₩ 	12	1	184	1×4	1x2
	R	1×4						(Socket 0 only)	(Socket 0 only)	(Sacket 0 only)		(Host 0 only)	(Host 0 only)	(Host 0 only)
	30	1×2	182, 181	091110	1x2	24	182	1x2 (Socket 0 only)	1x2 (Socket 0 only)	1x2 (Socket 0 only)	•	1x2 (Host 0 only)	1x2 (Host 0 only)	1x2 (Host 0 only)
	50	1×1	1x1	061110	1x1	141	14	1x1 (Socket 0 only)	1x1 [Socket 0 only]	1x1 (Socket () only)		1x1 [Host 0 onlo]	1x1 [Host 0 only]	1x1 (Host 0 only)
			1x8, 1x4, 1x2, 1x1	061101	1×8	\$	1×8	1×8	2x4	2%2	•	1×8	2 H4	2×2
Jacquestion Calcade all conditiones Calcade all condit Calcade all conditiones	20	1×8 Option B	2x4,2x2,2x1					(Socket () only)		(Socket 0 & 2 only)		(Host 0 only)		(Host 0 8: 2 only)
	4	2 x8 Option B	2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	061101	<u>196</u>	2%8	2%8	2×8	4 %4	2x2 (Socket 0 & 2 only)	•	2%8	4 x4	2 x/2 [Host 0 8: 2 only]
Independ Control <			1x8,1x4	061100	1x8	8	1x8	1x8	2 144	4x2	•	1*8	2 x4	4 x2
Index (b) (c) (20	1x8 Option D	2 x4, 4 x2 (First 8 lanes), 4 x1					(Socket 0 only)				(Host 0 only)		
			1x16,1x8,1x4	061100	1×16	1x16	1×16	2×8	4 %4	4x2	•	2.48	4×4	4 x2
RNU RNU RNU RNU RNU RNU RNU RNU RNU 2.4.7.2.2.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1		1×16 Option D	4 x4, 4 x2 (First 8 lames), 4 x1											
		RSVD	RSVD		RSVD - The encoding of 0,	b1011 is reserved due to in	sufficient spacing between	- PRSNTA and PRSNTB2	pin to provide positive carr	d identification.				
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	ş		2x4,2x2,2x1	061010	1×4	<u>4</u>	2 x4	144	2x4	242	,	124	2 xd	2%2
	7	2 K4	4 v2 (Eves 8 Isone) 4 v1	061001	12	674	676	(Socket U only)	070	(Socket Uit 2 only) 4.42		(Host Uonly)	0.0	(Host Uits Forey) d.u/2
R500 R500 <th< th=""><th></th><th>4 x2</th><th>2x2,2x1 1x2,1x1</th><th></th><th>ł</th><th>ł</th><th>ę 2</th><th>(Socket 0 only)</th><th>ł</th><th>ţ</th><th></th><th>(Host 0 only)</th><th>e a</th><th>ţ</th></th<>		4 x2	2x2,2x1 1x2,1x1		ł	ł	ę 2	(Socket 0 only)	ł	ţ		(Host 0 only)	e a	ţ
URCUPACIA URCUPACIA Decimal		RSVD	RSVD for future x8 encoding	061000		,	,		,		•			
2.66 Dec. 2.66 Dec. <t< th=""><th>4</th><th>1×16 Option A</th><th></th><th>060111</th><th>1×16</th><th>1x16</th><th>1×16</th><th>1x8 (Socket 0 only)</th><th>1x4 (Socket 0 only)</th><th>1x2 (Socket 0 only)</th><th>•</th><th>1x8 (Host 0 onlu)</th><th>1x4 (Host 0 only)</th><th>1x2 [Host 0 onlo]</th></t<>	4	1×16 Option A		060111	1×16	1x16	1×16	1x8 (Socket 0 only)	1x4 (Socket 0 only)	1x2 (Socket 0 only)	•	1x8 (Host 0 onlu)	1x4 (Host 0 only)	1x2 [Host 0 onlo]
NBC Dist 3.4.4.2.1.1 0.001 1.6 1.6 1.6 1.6 2.6 0.2.61 1.6 2.66	Ą	2×8 Dption A		060110	1%	2%8	2.48	2x8	2x4 [Socket 0& 2 only]	2x2 [Socket 0&2 only]		2×8	2 x4 (Host 0 & 2 only)	1x2 (Host 0 & Toniv)
10 10 10 2.66 4.44 2.66 4.44 2.66 2.66 4.44 2.66<	Ą	1×16 Option B		060101	1×16	1×16	1×16	2x8	2x4 (Socket 0& 2 only)	1x2 [Socket () only)		2×8	2 x4 (Host 0 & 2 only)	2 x/2 (Host 0 & Tonly)
In Exerction (a field, statistic) Could (a field, statistic) Could (a field, statistic)	9		1x16,1x8,1x4 2x8,2x4,2x2,2x1	001030	1×16	1×16	1×16	2x8	4 24	2x2 (Socket 0 & 2 only)		2.48	4 14	2 x2 (Host 0 & 1 only)
44 November 1 November 2	J.	1x16 Uption C	4 ×4, 4 ×2, 4 ×1	0.0011			4.4	5.4	4.4	4.0		P. 6	4.4	4.0
Revior Decome - <th< th=""><th></th><td>ų</td><th>1 × 4 × 77 × 4 × 1</th><th></th><td>ŧ</td><td>5 X X</td><td>4 X 4</td><td>(EP 0 and 2 only)</td><td>to t</td><td>5ocket 0 & 2 only)</td><td>'</td><td>(EP 0 and 2 only)</td><td>* × *</td><td>(Host 08: 1 only)</td></th<>		ų	1 × 4 × 77 × 4 × 1		ŧ	5 X X	4 X 4	(EP 0 and 2 only)	to t	5ocket 0 & 2 only)	'	(EP 0 and 2 only)	* × *	(Host 08: 1 only)
			RSVD	060010		'	'				•	'		
DACH DACH			HSVU	10000 M	,		,	•	'			'		
	L.	L	DVCH UVCH	I neutro										

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					Single Hors				Ì		Dual Hast	Court Have	Track to Local
		Host	1 Host	1 Host	1 Host		1 Host	1 Host		RSVD RSVD	2 Hosts	4 Hosts	4 or 8 Hosts
		Host CPU Sockets	1 Upstream Socket 1 Upstream Socket		1 Upstream Spi	icket 2 U	pstream Sockets	1Upstream Speket 2 Upstream Sockets 4 Upstream Sockets	RSVD	RSVD	RSVD 2 Upstream Sockets 4 Upstream Sockets	4 Upstream Sockets	4/8 Upstream
											(1 Socket per Host)	(1 Socket per Host) (1 Socket per Host)	Sockets (1 Socket per Host)
Network Card - Supported PCI	Network Card - Supported PCIe Configurations	Total PCIe Links	1Link (No Bifurcation)	1 or 2 Links	1, 2, or 4 Links	ıks	2 Links	4 Links	RSVD	RSVD	2 Links	4 Links	4 or 8 x2 links
		System Support	1x16, 1x8, 1x4, 1x2, 1x1	1x16, 1x8, 1x4, 1x2, 1x1		2,1x1 1	1x8, 1x4, 1x2, 1x1		RSVD	RSVD			
				2x8,2x4,2x2,2x1	2 ×8, 2 ×4, 2 ×2	2x1 2;	2 x8, 2 x4, 2 x2, 2x1				2 x8,2 x4,2 x2,2 x1		
Minimum					4 x4, 4 x2, 4 x	12		4 x4, 4 x2, 4x1				4x4,4x2,4x1	4x2,4x1
_		System Encoding	00000	00090	00090		00001	0P010	06011	06100	06101	0P110	0b111
Card Short x16 Cards		Add-in-Card Encoding								i.			
Name	Cond Miss Descent	PHSNIB(3:U)		- des motors									
T			HOVU - Lard not present II	n the system		-							
1×8	2	00000	<u></u>	89 	2		1x8 (Socket 0 only)	1x4 (Socket 0 only)	•		1x8 (Host 0 only)	1x4 (Host 0 only)	1xZ (Host 0 only)
<u>18</u>	1x4,1x2,1x1	0b1110	ž	4×	24 44		1×4 [Secket 0 only]	1x4 [Socket 0 only]	1	1	1x4 [Host 0 only]	1x4 (Host 0 onlo)	1×2 (Host 0 onlu)
1×2	1x2,1x1	051110	24 24	142	142		1x2 (Socket 0 only)	1x2 (Socket 0 only)	r.	r.	1x2 [Host 0 only]	1x2 [Host () only]	1x2 [Host 0 only]
ž	1×1	001110	12	181	1×1		1x1 (Socket 0 only)	1x1 (Socket 0 only)			1×1 (Host 0 only)	1x1 (Host 0 only)	1x1 (Host 0 only)
1×8 Option B		061101	8	8	891		1x8 (Socket 0 only)	2 x4	i.	•	1x8 (Host 0 only)	2%4	2 x2 (Host 0 & Tonly)
2 ×8 Option B	2 x8,2 x4,2 x2,2 x1 2 x8 Option B 4 x4,4 x2,4 x1	061101	1×8*	2×8	248		2 x8	4 x4			2%8	4 x4	2 x2 (Host 0 & Tonly)
1x8 Option D	1x8,1x4 2x4, 1x8 Option D 4 x2 (First 8 lanes), 4 x1	061100	841	2 44	2x4		1x8 (Socket 0 only)	2 x4	ı.	1	1x8 (Host 0 only)	2.44	4x2
4C 1x16 Option D	1x16,1x8,1x4 2x8,2x4 1x16 Option D 4x4,4x2 (First 8 James),4x1		1×16	1×16			2 x8	4 x4			2,48	4%4	4%2
		061011	RSVD - The encoding of 0	RSVD - The encoding of 0b1011 is reserved due to insufficient spacin			SNTA and PRSNTB2	between PRSNTA and PRSNTB2 pin to provide positive oard identification.	didentifica	stion.			
2.4	2x4,2x2,2x1 1x4,1x2,1x1		ž	2×4	2×4		1x4 (Socket 0 only)	2 ×4	,		1x4 (Host 0 only)	2%4	2 x2 [Host 0 & Tonlv]
	RSVD for future x8 encoding 0b1001	061001											
RSVD	RSVD for future x8 encoding 0b1000	001000			•				•	•			
1x16	F.	060111	1×16	1×16	1×16		1x8 (Socket 0 only)	1x4 (Socket 0 only)		1	1x8 (Host 0 only)	1x4 (Host 0 only)	1x2 (Host 0 only)
2 x8 Option A		011090	1×8*	2×8	2 x8		2 x8	2 x4 (Socket 0 & 2 only)	1	1	2,48	2 x4 (Hozt 0 & 2 only)	1x2 (Host 0 & Tonly)
1x16 Option B	1x16 Option B 2x8, 2x4, 2x2, 2x1	0b0101	1×16	1×16	1×16		2 x8	2 x4 (Socket 0 & 2 only)	•	•	2%8	2 x4 [Host 0 & 2 only]	2 x2 (Host 0 & Tonly)
1x16 Option C	1x16,1x8,1x4 2x8,2x4,2x2,2x1 1x16 Option C 4x4,4x2,4x1	060100	1×16	1×16	1×16		2 x8	4 84			2%8	4 x4	2 x2 (Host 0 & 1 only)
4.4		0b0 011	1×4*	2×4*	4×4		2 x4 (EP 0 and 2 only)	4×4			2 x4 (EP 0 and 2 only)	4 4 4	4 x2 (Host 0 & 1 only)
		0b0010							•	•			
RSVD	DAPD	0b0001							•	•			
		000000											



3.6.53.6.4 Bifurcation Detection Flow

[Need input and clarification from system vendors]

The following detection flow shall be used to determine the resulting link count and lane width based on the baseboard and add-in card configurations.

- 1. The baseboard shall read the state of the PRSNTB[3:0]# pins. An add-in card is present in the system if the resulting value is not 0b1111.
- Firmware determines the add-in card PCIe lane width capabilities per <u>Table 26Table 25</u> by PRSNTB[3:0]# pins.
- 3. The baseboard reconfigures the PCIe bifurcation on its ports to match the highest common lane width and lowest common link count on the card.
- 4. For cases where the baseboard request a link count override (such as requesting a 4-host baseboard requesting 4 x4 operation on a supported card that would otherwise default to a 2 x8 case), the BIF[0:2]# pins shall be asserted as appropriate. Asserting the BIF[0:2]# pins assumes the add-in card supports the requested link override.
- 5. PERST# shall be deasserted after the >100ms window as defined by the PCIe specification. Refer to Section 3.12 for timing details.

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3.6.63.6.5 PCIe Bifurcation Examples

For illustrative purposes, the following figures show several common bifurcation permutations. Figure 66Figure 52 illustrates a single host baseboard that supports x16 with a single controller add-in card that supports x16. The PRSTNB[3:0]# state is 0b0111. The BIF[2:0]# state is 0b000 as there is no need to instruct the end-point network controller to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16. The single host baseboard determines that it is also capable of supporting 1 x16. The resulting link width is 1 x16.

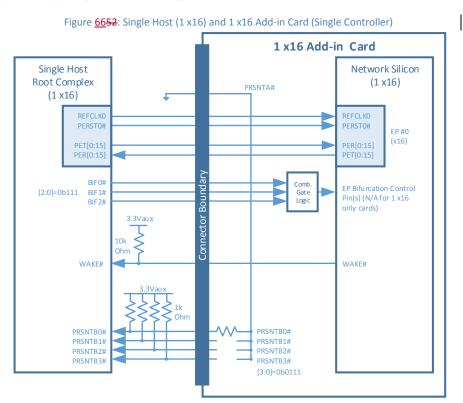




Figure 67Figure 53 illustrates a single host baseboard that supports 2 x8 with a single controller add-in also supports 2 x8. The PRSTNB[3:0]# state is 0b0110. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 2 x8. The single host baseboard determines that it is also capable of supporting 2 x8. The resulting link width is 2 x8.

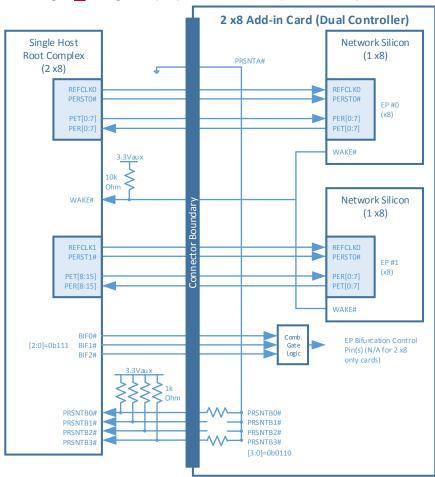


Figure 6753: Single Host (2 x8) and 2 x8 Add-in Card (Dual Controllers)

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Figure 68Figure 54 illustrates a four host baseboard that supports 4 x4 with a single controller add-in supports 1 x16, 2 x8 and 4 x4. The PRSTNB[3:0]# state is 0b0011. The BIF[2:0]# state is 0b101 as the end point network controller is forced to bifurcate to 4 x4. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16, 2 x8 and 4 x4. The four host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

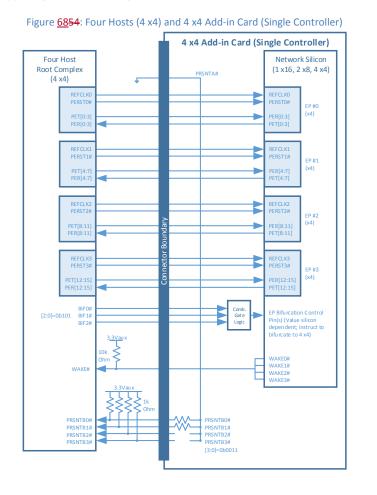




Figure 69Figure 55 illustrates a four host baseboard that supports 4 x4 with a four controller add-in card supports 4 x4. The PRSTNB[3:0]# state is 0b0011. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 4 x4. The four host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

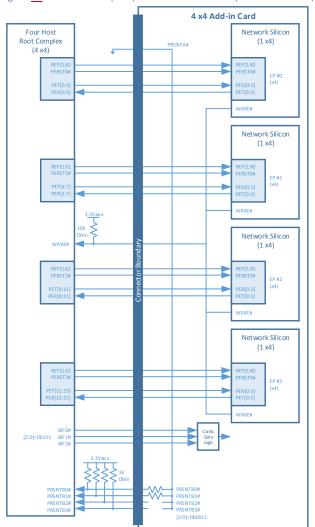
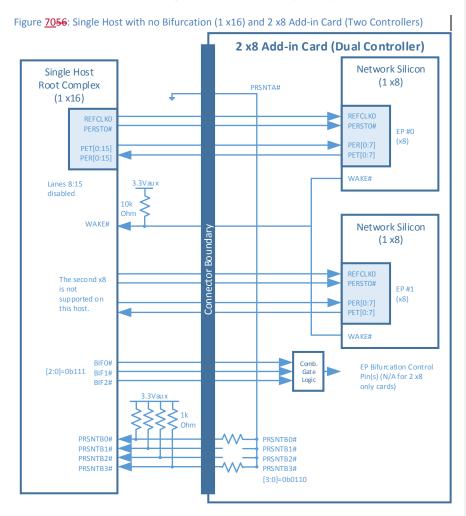


Figure 6955: Four Hosts (4 x4) and 4 x4 Add-in Card (Four Controllers)

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Figure 70-Figure 56 illustrates a single host baseboard that supports 1 x16 with a dual controller add-in supports 2 x8. The PRSTNB[3:0]# state is 0b0110. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 2 x8. The four host baseboard determines that it is capable of 1x 16, but down shifts to 1 x8. The resulting link width is 1 x8 and only on endpoint 0.





3.7 PCIe Clocking Topology

The OCP NIC 3.0 specification allows for up to four PCIe REFCLKs on the Primary Connector and up to two PCIe REFCLKs on the Secondary Connector. In general, the association of each REFCLK is based on the PCIe Link number on a per connector basis and is shown in <u>Table 27Table 26</u>. Cards that implement Primary and Secondary connectors have a total of up to 6 REFCLKs.

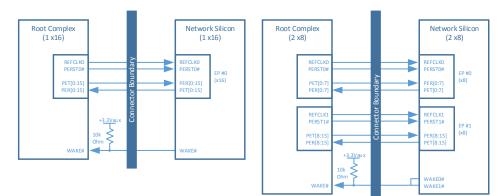
Table 2726: PCIe Clock Associations

REFCLK #	Description	Availability (Connector)
REFCLKO	REFCLK associated with Link 0.	Primary and Secondary Connectors.
REFCLK1	REFCLK associated with Link 1.	Primary and Secondary Connectors.
REFCLK2	REFCLK associated with Link 2.	Primary Connector only.
REFCLK3	REFCLK associated with Link 3.	Primary Connector only.

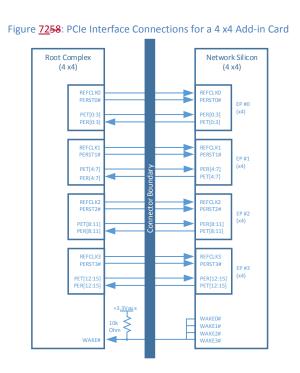
For each add-in card, the following REFCLK connection rules must be followed:

- For a 1 x16 capable add-in card, REFCLK0 shall be used for lanes [0:15].
- For a 2 x8 capable add-in card, REFCLKO shall be used for lanes [0:7] and REFCLK1 shall be used for lanes [8:15].
- For a 4 x4 capable add-in card, REFCLK0 shall be used for lanes [0:3], REFCLK1 shall be used for lanes [4:7], REFCLK2 shall be used for lanes [8:11] and REFCLK3 shall be used for lanes [12:15]. Pins for REFCLK2 and REFCLK3 are described in Section 3.5.1 and are located on the 28-pin OCP bay.

Figure 7157: PCIe Interface Connections for 1 x16 and 2 x8 Add-in Cards



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3.8 PCIe Bifurcation Results and REFCLK Mapping

For the cases where the baseboard and add-in card bifurcation are permissible, this section enumerates all of the supported PCIe link, lane and REFCLK mappings for each supported configuration. The bifurcation decoder is shown in Section 3.6.3.



Table 2827: Bifurcation for Single Host, Single Socket and Single Upstream Link (BIF[2:0]#=0b000)

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	5									Link O. Lone 15				Link 0, Lone 15		Link 0, Lane 15	Link O, Lone 15			
	Lare 2 Lare 3 Lare 5 Lare 6 Lare 7 Lare 3 Lare 10 Lare 11 Lare 12 Lare 13 Lare 14 Lare 5									Link 0, L Lane 14 Li			T	Link 0, L		Link 0, L Lane 14 L:				
	13 13									Link 0, 1 Lane 13 L			t	Link 0, 1 Lane 13 L		Link 0, 1 Lane 13 L	Link 0, Link 0, Lane 13 Lane 14			
	15 15									Link 0, Li Lone 12 Li			+	Link 0, L Lone 12 L		Link 0, L Lane 12 L:	Link O, L Lane 12 L:			-
	1									Link 0, L Lane 11 La			+	Link 0, L Lone 11 La		Link 0, L Lane 11 La				-
	10	-								Link 0, Li Lane 10 Le			+	Link 0, Li Lane 10 Le		Link 0, Li Lane 10 Ls	Link 0, Link 0, Lane 10 Lane 11			-
	1 1 1 2									Link O, L Lune 3 L:	$\left \right $		+	Link 0, L Lane 3 L		Link 0, L Lane 3 L:	Link 0, L Lune 3 L:			-
	8 -									Link 0, L Lane 8 L			+	Link 0, Li Lone 8 Li		Link 0, L Lane 8 L	Link O, L Lane 8 L			-
			Link 0, Lane 7				Link 0, Lane 7	Link 0, Lane 7	Link O. Lane T	Link 0, L Lane 7 L			+	Link 0, L	Link 0, Lone 7	Link 0, L Lane 7 L	Link O, L Lane 7 L			-
	ید و هد و		Link 0, Li Lane 6 L				Link 0, Li Lane 6 L	Link 0, Li Lanc 6 L	Link 0, Li Line 6 L	Link 0, Li Lano 6 L			+	Link 0, Li Lana 6 L	Link 0, Li Lane 6 L	Link 0, Li Lanc 6 L	Lane 6 L			-
	2 E		Link 0, L Lane 5 L				Link 0, Li Lane 5 Li	<u> </u>	Link O, Li Lune 5 L	Link 0, L Lone 5 L			+	Link 0, Li Lose 5 Li	Link 0, Li Lane 5 L	Link 0, Li Lane 5 Li	Link 0, L Lone 5 L			
	1		Link 0, L Lone 4 L				Link 0, L Lane 4 L	-	Link O. L Lone 4 L	Link 0, L Lane 4 L			+	Link 0, L		Link 0, L Lane 4 L	Link O, L Lane 4 L			-
	1 1 1 1		Link 0, L Lane 3 L	Link 0, Lane 3			Link 0, L Lane 3 L	Link O, L Lane 3 L	Link O, L Lane 3 L	Link O, L Lano 3 L		Link 0, Lane 3	T	Link 0, L	Link O, L Lane 3 L	Link 0, L Lane 3 L	Lane 3 L	Link O, Lane 3		
	1. 1. 1.		Link 0, L Lane 2 L	Link 0, L Lane 2 L			Link 0, L Lane 2 L	Link 0, L Lane 2 L	Link O, L Line 2 L	Link 0, L Line 2 L		Link 0, L Lane 2 L	+	Link 0, L	Link 0, L Lane 2 L	Link 0, L Lane 2 L	Link O, L Line 2 L	Link 0, L Lanc 2 L		
			Link 0, L Lane 1 L	Link 0, L Lane 1 L	Link 0, Lone 1		Link 0, L Lane 1 L	-	Link 0, L Lone 1 L	Link 0, L Lane 1 L		Link 0, L Lane 1 L		Link 0, L	Link 0, L Lone 1 L	Link 0, L Lane 1 L	Link 0, L Lone 1 L	Link 0, L Lane 1 L		
	ت ہ		Linco, L Laco, L	Linko, L Lako	Lineo, L Laco L	Linco. La co			o o	Lin (0)		o' 0,						Line 0, L Late 0 L		
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	Resulting Link Lare 0 Lane 1		1×8	1 x4	1×2	14	1×8	1×8*	1x8	1×16	•	1 ×4		1×16	1×8*	1×16	1×16	1×4*		•
	BIF[2:0] \$	000q0	00090	00090	00090	00090	00090	00090	00000	00000	00090	00090	00000	00000	00090	00090	00000	00000	0P000	00000
	Upstream	1 Link	1 Link	1 Link	1 Link	1 Link	1 Link	*	4		F		H						1 Link	1 Link
F					-	=	=	1 Link	1 Link	1 Link	1 Link	1 Link	1 Link	111	1Link	1 Link	1 Link	1 Link	=	
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x16. 1x8.1x4.1x2.	Ipstream Derices	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket 1	1 Upstream Socket 11	1 Upstream Socket 1L	1 Upptream Socket 1Lia	1 Upstream Socket 1 Li	1 Upstream Socket 1 Link	1 Upstream Socket 1 Link	1 Upstream Socket 1 Link	1Upstream Socket 1Link		1 Upstream Socket 1 Link	1 Upstream Socket 1Link	1 Upstream Socket 1 Link			_
1x16.1x8.1x4.1x2.1	Host Upstream Derices	-	1Host 1Upstream Socket				_				1 Upstream Socket		+	1 Upstream socket				1 Upstream Socket	1 Upstream Socket	1 Upstream Socket
	# Host	1 Host	1 Host	1 Host 1 Upstream Socket	1Host 1Upstream Socket	1Host 1Upstream Socket	1 Host 1 Upstream Socket	1 Host 1 Upstream Socket	1 Host 1 Upstream Socket	1 Host 1 Upstream Socket	1 Host 1 Upstream Socket	1 Host 1 Upstream Socket	1 Host 1 Upstream Socket	1 Host 1 Upstream Socket	1Host 1Upstream Socket	1 Host 1 Upstream Socket	1 Host 1 Upstream Secket	1 Host 1 Upstream Socket	1Host 1Upstream Socket	1 Hopt 1 Upstream Socket
	# Host	1 Host		1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Host 1 Upstream Socket	1 Upstream Socket	0biti00 1Host 1Upstream Socket	1 Upstream Socket	1 Host 1 Upstream Socket	1 Host 1 Upstream Socket	1 Host 1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Host 1 Upstream Socket	1Host 1Upstream Socket	_
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	# Host	Card Not Present 0b1111 1Host	1±8,1×4,1×2,1×1 0b1110 1Host	1x4,1x2,1x1 0b1110 1Host 1Upstream Socket	112,1 x1 0b1110 1Host 1Upstream Socket	1x1 0b1110 1Host 1Upptream Socket	x1 Obtion 1Host 1Upstream Socket	2 x1 0b1101 1 Host 1 Upstream Socket	0b1100 1Host 1Upstream Socket	0biti00 1Host 1Upstream Socket	1 Host 1 Upstream Socket	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1 1 x4, 1 x2, 1 x1	1 Upstream Socket	International and a second and a second	2 x8, 2 x4, 2 x2, 2 x1 0b0110 1 Host 1 Upetream Socket	1x1 0b0101 1Host 1Upstream Socket	2 x1 0b0100 1Host 1Upetream Socket	4 x4, 4 x2, 4 x1 0b0011 1Host 1Upetream Socket	0b00010 1Host 1Upstream Socket	0b0001 1 Hopt 1 Upstream Socket
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Add-In-Card					+0-010																
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0b1110 1 Host		t 1 Upstream Socket		1 Link	00090	1x2	Link 0, Lane 0	Link 0, Lane 1													
0b1110 1 Host		t 1 Upstream Socket		1 Link	00000	1x1	Link 0, Lane 0														
0b1101 1 Host		t 1 Upstream Socket		1 Link	00000	1 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7 D	Host Host Host Host Host Host Host Host	Host Isabled Di	Host sabled Di	Host sabled Di	Host F sabled Dis	Host Host sabled Disable	t Host led Disable
0b1101 1 Host		1 Upstream Socket		1 Link	00000	1×8*	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7 D	Host Host Host Host Host Host Host Host	Host isabled Di	Host sabled Di	Host Disabled Dis	Host F sabled Dis	Host Host Isabled Disable	t Host led Disable
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		_		1 Link	00000																
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Table 2928: Bifurcation for Single Host, Single Socket and Single/Dual Upstream Links (BIF[2:0]#=0b000]



	1		ne 15							Link 1. Lane 7		Link O. Lone 15					Link U. Lone 15	Link 1, Lone 7	Link 0, Lane 15	Link O, Lane 15				
	ł		ie 14 La	+	_				-	Link f, Li Lane 6 La		Link 0, Li Lane 14 La			┥	-	Link U. Lu Lane 14 La	Link 1, Li Lane 6 Le	Link 0, Li Lane 14 La	Link O, Li Lane 14 La				┝
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	$\left \right $		10 Lane							1, Link1, 2 Lane3						-		1, Link 1, 2 Lane 3			2, Link2, 2 Lane3			╞
			3 Lane							f, Link f, 1 Lone 2		0, Link 0, 9 Lone 10				+	 Lenk U. Lone 10 	t Link t 1 Lone 2	0. Link 0. 3 Lane 10	0, Link 0, 3 Lone 10	e, Linke, 1 Lance			
			8 Lane							Link 1. Lane 1		. Linko. 5 Lone 3			_	-	. Link U.	Link1. Lane1	. Link 0. 5 Lane 3	. Link O. 5 Lane 3	. Link 2, b Lane 1			
			7 Lane							Link 1, Lane 0		Link 0, Lane 8				+	Lane 8	Link 1, Lane 0	Link 0, Lane 8	Link O, Lane 8	Link 2, Lane 0			
			- Faire	_	Link 0, Lone 7				Link 0, Lane 7	Link 0, Lane 7	Link 0, Lone 7	Link O, Lone 7				-	Lone 7	Link 0, Lone 7	Link 0, Lane 7	Link 0, Lone 7				
			Lane 6	-	Link 0. Lone 6				Link 0. Lane 6	Link 0, Lane 6	Link O. Lane 6	Link O. Lane 6				-	Lane 6	Link 0. Lone 6	Link 0. Lane 6	Link O. Lane 6				
			Lane 5		Link 0, Lane 5				Link 0, Lane 5	Link O, Lane S	Link O, Lane 5	Link O, Lane 5				-	Lane 5	Link 0, Lane 5	Link 0, Lane 5	Link O, Line 5				
			Lane 4		Link 0. Lone 4				Link 0, Lone 4	Link 0, Lane 4	Link O, Lone 4	Link O, Lone 4					Link U.	Link 0, Lane 4	Link 0, Lane 4	Link O, Lane 4				
			Lane 3		Link 0, Lone 3	Link 0, Lane 3			Link 0. Lane 3	Link 0, Lane 3	Link O. Lane 3	Link O. Lane 3		Link 0, Lane 3			Lone 3	Link 0, Lane 3	Link 0, Lane 3	Link O. Lane 3	Link 0. Lane 3			
			Lane 2		Link 0, Lane 2	Link 0, Lane 2			Link 0, Lane 2	Link O, Lane 2	Link O, Line 2	Link O, Lane 2		Link 0, Lane 2			Lane 2	Link 0, Lane 2	Link 0, Lane 2	Link 0, Lane 2	Link 0, Lane 2			
			Lane 1		Link 0, Lone 1	Link 0, Lane 1	Link 0, Lone 1		Link 0, Lane 1	Link 0, Lane 1	Link O, Lone 1	Link 0, Lane 1		Link 0, Lane 1			Lone 1	Link 0, Lane 1	Link 0, Lane 1	Link O, Lone 1	Link 0, Lane 1			
			0		Ling 0. Lare 0.	Lin 0. Lare 0	Line 0. Lare 0	Lin 0.	Line 0.	Lin 0. Lar 0.	Line 0. Lare 0.	Lin 0. Laro 0.		Lina 0. Lare 0			10	Lin 0. 1 0.0	Lin 0. Lare 0	Line 0. Lare 0.	Lin 0. La 0.			
			Realting Link Lane 0 Lane 1 Lane 2 Lane 3 Lane 4 Lane 5 Lane 5 Lane 7 Lane 8 Lane 9 Lane 10 Lane 11 Lane 12 Lane 18 Lane 14 Lane 15		1×8	1×4	1x2	1×1	1×6	5 ×8	1x8	1×16		1×4		. :	4 I XI	2 x8	1×16	1×16	2 x 4 *			
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		-		+	1 or 2 Links	1 or 2 Linko	1 or 2 Links	1 or 2 Links	1 or 2 Links	1 or 2 Linko	1 or 2 Links	1 or 2 Links	1 or 2 Links	1 or 2 Links		+	1 or 2 Links	1 or 2 Links	1 or 2 Linko	1 or 2 Links	1 or 2 Links			1 or 2 Links
1x16, 1x8, 1x4, 1x2, 1	C TO, C X4, C XC, C XI		_	+	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1Upstream Socket	1 Upstream Socket	1 Upstream Socket			1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket		1 Upptream Socket	1 Upstream Socket
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	olingle frost, single upstream societ, the of Lwo upstream Links	Supported Bifurcation Modes			1x8, 1x4, 1x2, 1x1 0	1x4,1x2,1x1 0	1x2,1x1 0	1x1	1x6.1x4,1x2,1x1 0 1x8 Option B 2x4,2x2,2x1	2 x8, 2 x4, 2 x2, 2 x1 2 x8 Option B 4 x4, 4 x2, 4 x1	1 x8, 1 x4 2 x4, 1 x8 Option D 4 x2 (First 8 Isnes), 4 x1	1x16,1x8,1x4 2x6,2x4, 1x16 Option D 4x4,4x2(Firet 8 lance),4x1	RSVD 0	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	RSVD for future x8 ancoding 0b1001	Buil	1 x10, 1 x6, 1 x4, 1 x2, 1 x1	2 x8, 2 x4, 2 x2, 2 x1 0	1x16 Option B 2x8, 2x4, 1x2, 1x1 0	1 x15, 1 x8, 1 x4 2 x5, 2 x4, 2 x2, 2 x1 1 x15 Option C 4 x4, 4 x2, 4 x1	4 x4, 4 x2, 4 x1 0			RSVD 0
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اة	Single Host, Single Upstream Socket, One or Two Upstream Links	pstream Links		2 x8, 2 x4, 2 x2, 2 x1							ł									-		
10	Supported Bifurcation Modes Min Card Short	Add-in-Card Funding				RIFI2-01#																
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Table <u>3029</u>: Bifurcation for Single Host, Single Socket and Single/Dual/Quad Upstream Links (BIF[2:0]#=0b000)

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Matrix						A 100 A 100 A 100 A 100 A																		
Increase						1 X10, 1 X0, 1 X4, 1 X4, 1 2 v8 2 v6 2 v2 2 v1																		
	Single H	ost. Single Upsti	ream Socket. One. Two or Four	Upstream Links		4 x4. 4 x2. 4 x1																		
			Supported Bifurcation Modes	Add-In-Card						L			F	F	ŀ	╞	┝	╞	ŀ	╞	ŀ	ŀ	L	L
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ding Ob1000 1Host 1Upptream Socket 1, 2, or 4 Links	1 Host 1 Upstream Socket 1, 2, or 4 Links	1 Host 1 Upstream Socket 1, 2, or 4 Links	1 Upstream Socket 1, 2, or 4 Links	1, 2, or 4 Links		히	00000					+				+	+	+	+	4	4		+
1x16,1x8,1x8,1x2,1x1 0b0111 1Host 1Host 1Upstream Socket 1,2, or 4 Links 0 1x16	1x16, 1x8, 1x8, 1x2, 1x1 0b0111 1Host 1Host 1Upstream Socket 1, 2, or 4 Links	1 Host 1 Upstream Socket 1, 2, or 4 Links	1 Upstream Socket 1, 2, or 4 Links	1, 2, or 4 Links		8	00000	1x16	La 6.0	Link 0, Lane 1	Link 0, Lone 2	Link 0, Lane 3	_	_	_	_	Link O, Lir Lane 8 La	Link O, Lin Lane 9 Lan	Link 0, Lin Lane 10 Lar	Link 0, Lin Lane 11 Lan	Link 0, Link 0, Lane 12 Lane 13	(, Link 0, 3 Lane 14	Link 0, Lone 15
2 x8.2 x8.2 x4, 2 x2, 2 x1 2 x8 Option A 2 x8, 2 x4, 2 x2, 2 x1 2 x8 Option A	2 x8, 2 x4, 2 x2, 2 x1 00010 1Host 1Host 1.2, or 4 Links	1 Host 1 Upptream Socket 1, 2, or 4 Links	1 Upstream Socket 1, 2, or 4 Links	1, 2, or 4 Links		8	00000	5 x9	19 19 19 19	Link 0, Lane 1	Link 0, Lone 2	Link 0, Lane 3	Link 0, Lane 4	Link O, Lone 5	Link 0, Lane 6	Link 0, 1 Lane 7	Lak 1, Li Lane 0 La	Link 1, Lin Lane 1 Lar	Link 1, Lin Lane 2 Lar	Link 1, Lin Lane 3 Lan	Link 1, Link 1, Lane 4 Lane 5	Link 1, 5 Lane 6	_
1 Host 1 Upstream Socket 1, 2, or 4 Links	1x1 0b0101 1Host 1Upstream Socket 1, 2, or 4 Links	1 Host 1 Upstream Socket 1, 2, or 4 Links	1 Upstream Socket 1, 2, or 4 Links	1, 2, or 4 Links		•	00000	1±16	Lin c.o.	Link 0, Lane 1	Link O, Lone 2	Link 0, Line 3		Link O, Lone 5	Link 0, Lane 6	Link 0, L Lane 7	Lane 0. La	Link O, Lin Lane 3 Lan	Link 0, Lin Lane 10 Lar	Link O, Lin Lane 11 Lan	Link 0, Link 0, Lane 12 Lane 13	1, Link 0, 3 Lane 14	
1x16,156,156,154 0b01000 11host 1Uppercent/Societ 1.2, or 4 Links 0 1x16 Dptiono C 4x4, 4x2, 4x2 1 1 1 1 0 0	2 x1 0b0100 11Host 1Upptream Socket 1.2, or 4 Links	1 Host 1 Upstream Socket 1, 2, or 4 Links	1 Upstream Socket 1, 2, or 4 Links			8	00000	1±16	Lin (0)	Link O. Lane 1	Link O, Lone 2	Link 0, Lana 3	Link O. Lane 4	Link O, Lone 5	Link 0, Lana 6	Link O. L Lone 7 L	Link O, Lin Linne B Lin	Link O, Lin Lane 3 Lan	Link 0, Lin .ane 10 Lue	Link O, Lin Lano 11 Lan	Link 0, Link 0, Lane 12 Lane 13	link 0, 3 Lane 14	Link 0, Lone 15
4 x4, 4 x2, 4 x1 0050011 1 Host 1 Upstream Socket 1, 2, or 4 Links	x2, 4 x1 0b0011 1Host 1Upptream Socket 1, 2, or 4 Links	1 Host 1 Upstream Socket 1, 2, or 4 Links	1 Upstream Socket 1, 2, or 4 Links	1, 2, or 4 Links		0Pi	00090	4 14	Line 0. Lae 0	Link 0, Lane 1	Link O, Lone 2	Link 0, Lane 3	Link 1. Lane 0	Link 1, Lone 1	Link 1, Lane 2	Link 1, L Lone 3 L	Link 2, Lir Lone 0 Lo	Link 2, Lin Lane 1 Lar	Link 2, Lin Lane 2 Lar	Link 2, Link Lane 3 Lan	Link 3, Link 3, Lane 0 Lane 1	, Link 3, I Lane 2	Link 3, Lone 3
RSVD 060010 1Host 1Upptream Socket 1, 2, or 4 Links	060010 1Host 1Upstream Socket 1, 2, or 4 Links	1 Host 1 Upstream Socket 1, 2, or 4 Links	1 Upstream Socket 1, 2, or 4 Links	1 Upstream Socket 1, 2, or 4 Links 0	1, 2, or 4 Links 0	ျ	00090																
RSVD 0b0001 1Host 1Upstream Socket 1, 2, or 4 Links	0b0 001 1Host	1 Host		1 Upptream Socket 1, 2, or 4 Links 0	1, 2, or 4 Links 0	익	0009						1	1							+		
RSVD RSVD RSVD RSVD 00000 1Host 1Upstream Socket 1,2, or 4 Links	0b0000 1Host	1 Host	_	1 Upstream Socket 1, 2, or 4 Links	1, 2, or 4 Links		000q0										-		_	_			

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 Table <u>3130</u>: Bifurcation for Single Host, Dual Sockets and Dual Upstream Links (BIF[2:0]#=0b001)



	Single Host, Two Upstream Sockets, Two Upstream Links	5		2 x8, 2 x4, 2 x2, 2x1																		
S	upported Bifurcation Modes	Add-in-Card Encoding				BIF[2:0]#																
	Card Not Present	PRSNTB[3:0]# 0b1111	1 Host	Opstream Devices 2 Unstream Sockets	Upstream Links	0h001	Resulting Link	lane 0	ane 1	Lane 2	ane 3	lane 4	lane 5	lane 6	lane 7	Lane 8	lane 9	Lane 10 Lane	Lane 11 Lane 12	12 Lane 13	3 lane 14	lane 15
	1 x8, 1 x4, 1 x2, 1 x1	001110	1 Host	2 Upstream Sockets	2 Links	00001	1 x8 (Socket 0 onto)	Link 0,	Unk 0,	Link 0, 1	Link 0, 1	Link 0, L	Link 0, U	Link 0, Li	Link 0, Jane 7							
	1 x4, 1 x2, 1 x1	001110	1 Host	2 Upstream Sockets	2 Links	00001	1 x4 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1	-		-		_								
	1 x2, 1 x1	0b1110	1 Host	2 Upstream Sockets	2 Links	10090	1 x2 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1					\vdash			-					
	1x1	0b1110	1 Host	2 Upstream Sockets	2 Links	00001	1x1 (Socket 0 only)	Link 0, Lane 0														
	1 x8, 1 x4, 1 x2, 1 x1 1 x8 Option B 2 x4, 2 x2, 2 x1	0b1101	1 Host	2 Upstream Sockets	2 Links	00001	1 x8 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, 1 Lane 2 1	Link 0, 1 Lane 3 L	Link 0, L Lane 4 Li	Link 0, Li Lane 5 La	Link 0, Li Lane 6 La	Link 0, H Lane 7 Disi	Host Hc sabled Disa	Host Ho sabled Disa	Host Host isabled Disable	st Host bled Disable	Host Host Host Host Host Host Host Host	Host ed Disable	Host Disabled
	2 x8, 2 x4, 2 x2, 2 x1 2 x8 Option B 4 x4, 4 x2, 4 x1	0b1101	1 Host	2 Upstream Sockets	2 Links	00001	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, 1 Lane 2 1	Link 0, 1 Lane 3 L	Link 0, L Lane 4 Li	Link 0, Li Lane 5 La	Link 0, Li Lane 6 La	Link 0, Li Lane 7 La	Link 1, Lin Lane 0 Lan	Link 1, Lin Lane 1 Lan	Link 1, Lin Lane 2 Lan	Link 1, Link 1, Lane 3 Lane 4	1, Link 1, e 4 Lane 5	, Link 1, 5 Lane 6	Link 1, Lane 7
	1 x8, 1 x4	001100	1 Host	2 Upstream Sockets	2 Links		1×8	Link 0,	Link 0,	Link 0, 1		-	Link 0, Li		Link 0,							
	2 x4, 1 x8 Option D 4 x2 (First 8 lanes). 4 x1					06001	(Socket 0 only)	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4 Li	Lane 5 La	Lane 6 La	Lane 7							
	1 ×16, 1 ×8, 1 ×4	001100	1 Host	2 Upstream Sockets	2 Links		2.x8	Link 0,	Link 0,	-	-	-	-	-	-				-	-	-	-
	2 x8, 2 x9, 1 x16 Ontion D 4 x4 4 x2 (First 8 Janes) 4 x1					Innon		Lane U	Lane 1	Lane 2	rane 3	n + auer	cane >	rane 6 La	rane / La	rane o Fran	Lane 1 Lan	rane z lan	Lane 3 Lan	rane 4 Lane 2	o Lane 6	lane /
	RSVD	001011	1 Host	2 Upstream Sockets	2 Links	00001			T		t	╞	\vdash	╞		-		+	+			
	2 x4, 2 x2, 2 x1	001010	1 Host	2 Upstream Sockets	2 Links	0001	1 x4	Link 0,	Link 0,	-	Link 0,											
	1 x4, 1 x2, 1 x1						(Socket 0 only)	Lane 0	Lane 1	Lane 2	Lane 3		+	+	+		+	+	+	-		
	4 x2 (First 8 lanes), 4 x1 2 x2, 2 x1	001001	1 Host	2 Upstream Sockets	2 Links	00001	1 x2 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1													
	1x2, 1x1										_	_	_	_	_	_			_		_	
	RSVD for future x8 encoding	0b1000	1 Host	2 Upstream Sockets	2 Links	00001																
	1 x15, 1 x8, 1 x4, 1 x2, 1 x1	060111	1 Host	2 Upstream Sockets	2 Links	10090	1 x8 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, 1 Lane 2 1	Link 0, 1 Lane 3 L	Link 0, L Lane 4 Li	Link 0, Li Lane 5 La	Link 0, Li Lane 6 La	Link 0, Lane 7							
	2 x8, 2 x4, 2 x2, 2 x1	0b0110	1 Host	2 Upstream Sockets	2 Links	00001	2.x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, 1	Link 0, 1	Link 0, L	Link 0, Li	Link 0, Lii Iane 6 La	Link 0, Li	Link 1, Lin	Link 1, Lin	Link 1, Link	Link 1, Link 1, Lane 3 Lane 4	1, Link 1,	, Link 1,	Link 1, Lane 7
	1 x16, 1 x8, 1 x4, 1 x2, 1 x1	060101	1 Host	2 Upstream Sockets	2 Links	21.000	2 x8	Link 0,	Link 0,	+	+	+	+-		+	+-	+	+	-	-	+-	_
	1 x16 Option B 2 x8, 2 x4, 2 x2, 2 x1					TODOO		Lane 0	Lane 1	Lane 2 I	Lane 3 L	Lane 4 Li	Lane 5 La	Lane 6 La	Lane 7 La	Lane 0 Lan	Lane 1 Lan	Lane 2 Lane 3	e 3 Lane 4	e 4 Lane 5	5 Lane 6	-
	1 ×16, 1 ×8, 1 ×4	00100	1 Host	2 Upstream Sockets	2 Links		2 x8	Link 0,	Link 0,					_	Link 0, Lii	Link 1, Lin	Link 1, Lin	Unk 1, Un	Link 1, Link 1,	 Unk 1, 	Unk 1,	
	2 x8, 2 x4, 2 x2, 2 x1 1 x16 Option C 4 x4, 4 x2, 4 x1					00001		Lane 0	Lane 1	Lane 2	Lane 3	Lane 4 Li	Lane 5 La	Lane 6 La	Lane 7 La	Lane 0 Lar	Lane 1 Lan	Lane 2 Lan	Lane 3 Lane 4	e 4 Lane 5	5 Lane 6	Lane 7
	4 x4, 4 x2, 4 x1	060011	1 Host	2 Upstream Sockets	2 Links	0HAD1	2 x4	-	Link 0,	_	Link 0,				5	-	-	-	12,			
						-	(EP 0 and 2 only)	Lane 0	Lane 1	Lane 2 1	Lane 3		+	+	e	Lane 0 Lan	Lane 1 Lan	Lane 2 Lane 3	e 3		_	
	RSVD	0b0010	1 Host	2 Upstream Sockets	2 Links	0b001					1	+	+	+	+	+	+	+	+			
		000001	1 Host	2 Upstream Sockets	2 Links	00001									+			+	_	_		
		10000																				

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				1 x8, 1 x4, 1 x2, 1 x1																		
ingle Host, Two	Single Host, Two Upstream Sockets, Two Upstream Links	m Links		2 x8, 2 x4, 2 ±2, 2x1																		
1	Supported Bifurcation	ion Add-in-Card	7			BIF[2:0]															_	
Vidth Name		PESNTB(3:01#	# Host	Upstream Devices	<u> </u>	•	Resulting tink tarb 0 tare 1 tare 2 tare 3 tare 5 tare 5 tare 5 tare 3 tare 3 tare 0 tare 11 tare 12 tare 13 tare 14 tare 15		Lane 1	ane 2 La	ae 3 Las	• 4 Las	t 5 Lane	6 Lane 7	Lane 8	Lane 3	Lane 10	Lane 11	Lane 12	ane 13	ane 14 1	i ane li
n/a Not Present	ssent Card Not Prosent	001111	1 Host	2 Upstream Sockets	2 Linko	00001															ľ	
2C	1x8,1x4,1x2,1x1 x8	061110	1Host		2 Links	0090	1 x8 (Socket 0 calu)	Lin 0.	Link 0, 1 Lane 1	Link 0, Li Lane 2 La	Link 0, Lin Lone 3 Lon	Link 0, Link Lane 4 Lan	Link 0, Link 0, Lane 5 Lane 6	Link 0.								
	1×4,1×2,1×1	061110	1 Host	2 Upstream Sockets	2 Links	00-001		0 0	-	_		-	-	-								
╞	1x2,1x1	061110	1Host	2 Upstream Sockets	2 Linko	0090		0.0		-		-								T	t	
	1x1 1x1	061110	1Host	2 Upstream Sockets	2 Links	00001		La O														
2C 1×8 Op	1x8,1x4,1x2,1x1 1x8 Option B 2x4, 2x2, 2x1	061101	1Host	2 Upstream Sockets	2 Links	0090	1 x8 (Socket 0 only)	Lin 0.	Link 0, Lone 1	Link O, Li Lane 2 La	Link O. Lin Lone 3 Lan	Link 0, Link Lane 4 Lan	Link 0, Link 0, Lane 5 Lane 6	Link 0. b Lane 7								
4C 2x80e	2 x8, 2 x4, 2 x2, 2 x1 2 x8 Option B 4 x4, 4 x2, 4 x1	061101	1 Host	2 Upstream Sockets	2 Links	0090	5×8	Lin 0.0	Link 0, Lane 1	Link O, Li Lane 2 La	<u> </u>	Link O. Link Lans 4 Lan	Link 0, Link 0, Lane 5 Lane 6	Link 0. Lans 7	Link 1, Lone 0	Link 1, Lane 1	Link t. Lane 2	Link 1, Lans 3	Link 1. Lane 4	Link 1, Lone 5	Link 1. Lane 6	Link 1. Lone 7
	1 x8, 1 x4 2 x4, 1 x8 Option D 4 x2 (First 8 Issee), 4 x1	061100	1 Host	2 Upstream Sockets	2 Linko	09001	1 x6 (Socket 0 only) 1	Lango o	Link 0, Lane 1	Link O, Li Lane 2 La	<u> </u>	Link O, Link Lane 4 Lan	Link 0, Link 0, Lane 5 Lane 6	Link 0, Lane 7								
	1×16,1±8,1×4 2×8,2±4,	0b1 100	1 Host	2 Upstream Sockets	2 Links	0090	2×8	Lin 0. Lario 0.	Link 0, Lane 1	Link O, Li Lane 2 La	Link 0, Lin Lane 3 Lan	Link O, Link Lane 4 Lan	Link 0, Link 0, Lane 5 Lane 6	Link 0, Lane 7	Link 1, Lane 0	Link 1, Lane 1	Link 1. Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lone 5	Link 1, Lane 6	Link 1, Lone 7
4C 1x16 Op RSVD RSVD	1x16 Option D 4 x4, 4 x2 (First 8 lones), 4 x1 RSVD RSVD	L4 ×1 0b1011	1 Host	2 Hinstream Sockets	2 Links	06001															T	
		061010	1 Host		2 Links	0090	1 x4 (Socket 0 only)	Lin O.	Link 0, 1 Lans 1	Link O, Li Lane 2 La	Link 0, Lone 3											
RSVD RSVD		ding 0b1001	1Host		2 Links	06001																
RSVD RSVD	RSVD for future x8 encoding 0b1000 1 x16, 1 x8, 1 x4, 1 x2, 1 x1 0b0111	0b1000 0b0111	1Host 1Host	2 Upstream Sockets 2 Upstream Sockets	2 Links 2 Links	0000	1×8 L	Lin O.	Link 0, 1	Link O, Li	Link 0, Lin	Link O, Link	Link 0, Link 0,	Link 0,					T	T	t	
4C 1×16	16 2×6, 2×4, 2×2, 2×1	000110	1 Host	2 Upstream Sockets	2 Linko	innen	(Socket 0 only) L 2 x8	Lin 0.	Lane 1 Link 0,	Lane 2 La Link 0, Li	Lane 3 Lan Link 0, Lin	Lane 4 Lan Link 0, Link	Lone 5 Lone 6 Link 0, Link 0,	5 Lane 7	Link 1	Link 1,	Link t	Link 1,	Link 1,	Link 1,	Link 1,	Link 1
4C 2 x8 Option A				-		Innan			-	-	_	_	-	-	_	-	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7
4C 1×16 0p	1x16 Option B 2x8, 2x4, 2x2, 2x1		1 Host	2 Upstream Sockets	2 Links	06001	2×8 L	Lin 0. Larb 0	Link 0, Lane 1	Link O, Li Lane 2 La	_	_	_		Lane 0	Lane 1.	_	Link 1, Lone 3	Link 1. Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
4C 1×16 0p	1x16,1x8,1x4 2x6,2x4,2x2,2x1 1x16 Option C 4x4,4x2,4x1	000100	1 Host	2 Upstream Sockets	2 Links	10090	2x8	Lin 0. Lara 0	Link 0, 1 Lone 1	Link O, Li Lane 2 La	Link 0, Lin Lane 3 Lan	Link O, Link Lune 4 Lun	Link 0, Link 0, Lane 5 Lane 6	Link O, 5 Lane 7	Link 1. Lone O	Link I, Line 1	Link 1. Lone 2	Link 1, Lune 3	Link 1. Lane 4	Link 1. Lone 5	Link 1, Lano 6	Link 1, Lone 7
4C 4 ×4	×4	000011	1Host		2 Links	00001	2 X4 L (EP 0 and 2 only) L	Lin 0. Larb 0	Lane 1 L	Link O, Li Lane 2 La	Link 0, Lone 3				Link 2, Lone 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lone 3				
RSVD RSVD		000010	1Host		2 Links	06001	•															
RSVD RSVD		00000	1 Hogt		2 Linko	0000															1	
RSVD RSVD	RSVD	OBODOD I	1 Hook	O Hereson Contrate	Oliste	00000		ĺ			ļ											



 Table 3231: Bifurcation for Single Host, Four Sockets and Dual Four Upstream Links (BIF[2:0]#=0b010)

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		TYPE TO A LONG				ł	ŀ		ŀ	ŀ								İ	ŀ	
2																				
	PRSMTB(3:0)# Host	Uostream Devices	Unstream Links	#[0:7]+89	Resulting Link	Lane 0	I and 1	Lane 2 La	Lane 3 Lar	Lane 4 Lan	Lane 5 Lane 6	6 Lane 7	7 Lane 8	8 Lane 9	Lane 10		Lane 11 Lane 12	Lane 13	Lane 14	Lane 15
1		4	4 Links	00010		-		-	-	-	-		-							
	1 Host	4 Upstream Sockets	4 Links	09010	1 14	-	-	_	Link 0,											
				nTnon	(Socket 0 only)	Lane 0	Lane 1 L	Lane 2 La	Lane 3	_		_	_							
	1 Host	4 Upstream Sockets	4 Links	06010	1.54	_	_	_	Link 0,											
1					(pocket u only)	+	÷	raue 7 Pa	2	+			+					Ī	T	
	1 Host	4 Upstream Sockets	4 Unks	06010	1 x2 (Socket 0 only)	Lane 0	Link 0, Lane 1													
	1 Host	4 Upstream Sockets	4 Links	06010	1 x1 (Socket 0 only)	Link 0, Lane 0														
	1 Host	4 Upstream Sockets	4 Links	06010	2 x4	Link 0,	Link 0, L	Link 0, Li	Link 0, Lin	Unk 1, Un	Link 1, Link 1,	L Link L		Host Host Host Host Host Host Host Host	Host	Host	Host	Host	Host	Host
T	1 10.00	A Hartranan Contrate	Allake			+	+	+	-		+	_								Link a
	T HOSE	* Upstream sockets	* LINKS	0100	***	_	_	_	_	_	-	_	_	_	_	_	Lane 0	_	_	Lane 3
	1 Host	4 Upstream Sockets	4 Links		2 x4	Link 0,	Link 0, L	LINK 0, LI	Link 0, Lin	Link 1, Lin	Unk 1, Unk 1,									
				06010		Lane 0	Lane 1	Lane 2 La	Lane 3 Lar	Lane 0 Lan	Lane 1 Lane 2	2 lane 3	m							
	1 Host	4 Upstream Sockets	4 Links		4 x4	Link 0,	Link 0, L	Link 0, Li	Link 0, Lin	Unk 1, Uni	Link 1, Link 1,	 Link 1, 	Link 2,	2, Link 2,	Link 2,	Link 2,	Link 3,	Link 3,	Link 3, L	Link 3,
				01000		Lane 0	Lane 1 L	Lane 2 La	Lane 3 Lar	Lane 0 Lan	Lane 1 Lane 2	2 Lane 3	3 Lane 0	0 Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 2 L	Lane 3
1	1 Host	4 Upstream Sockets	4 Links	06010		F	F	╞		╞								F	F	
001010	1 Host	4 Upstream Sockets	4 Links	01010	2.84	-	-	-		_	-									
						-	-	Lane 2 La	Lane 3 Lar	Lane 0 Lan	Lane 1 Lane 2	2 Lane 3	90		_					
	1 Host	4 Upstream Sockets	4 Links	06010	2×2	Link 0, Lane 0	Link 0, Lane 1		5 3	Lane 0 Lan	Unk 1, Lane 1									
						1	1	+	+	+		+	+		4			1	1	
	1 Host	4 Upstream Sockets	4 Links	06010								_	_							
111090	1 Host	4 Upstream Sockets	4 Links	010010	1 x4 (Socket 0 only)	Link 0, Lane 0	Link 0, L	Link 0, Li Lane 2 La	Link 0, ane 3											
01100	1 Host	4 Upstream Sockets	4 Links	01000	2 x4 (Socket 0 & 2 only)	Link 0, Lane 0	Link 0, L	Link 0, Li Lane 2 La	Link 0, Lane 3				Link 2, Lane 0	2, Link 2, 0 Lane 1	Lane 2	Link 2, Lane 3				
101000	1 Host	4 Upstream Sockets	4 Links	01090	2 x4 (Socket 0 & 2 only)	Link 0, Lane 0	Link 0, L	Link 0, Li Lane 2 La	Link 0, Lane 3	-			Link 2, Lane 0	2, Link 2, 0 Lane 1	Link 2, Lane 2	Link 2, Lane 3				
00100	1 Host	4 Upstream Sockets	4 Links		4 x4	+	-	-	-	Link 1, Lin	Link 1, Link 1,	 Link 1, 	L, Link 2,	2, Link 2,	Link 2,	Link 2,	Link 3,	Link 3,	Link 3, 1	Link 3,
				0100		Lane 0	Lane 1 L	Lane 2 La	Lane 3 Lar	ane 0 Lan	Lane 1 Lane 2	2 lane 3	3 Lane 0	0 Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 2	Lane 3
110090	1 Host	4 Upstream Sockets	4 Links	010010	4 x4	Link 0, Lane 0	Link 0, L	Link 0, Li Lane 2 La	Link 0, Lin Lane 3 Lan	Link 1, Lin Lane 0 Lan	Link 1, Link 1, Lane 1 Lane 2	1, Link 1, 2 Lane 3	L Link 2, 3 Lane 0	2, Link 2, 0 Lane 1	Lane 2	Link 2, Lane 3	Link 3, Lane 0	Link 3, Lane 1	Link 3, 1 Lane 2	Link 3, Lane 3
	1 Host	4 Upstream Sockets	4 Links	00010		-	+	-	-	-	⊢		-	-	⊢	-			⊢	
L	1 Host	1 Host 4 Upstream Sockets	L	06010		t	ŀ	╞	$\left \right $	╞			L					t	t	
00000	1 HAGE	1 Host 4 Linstream Sockets	4 Links	00010																



t, Four Ups	Single Host, Four Upstream Sockets, Four Upstream Links	22		4 x4, 4 x2, 4x1																		
Min Card Card Short	Supported Bifurcation Modes					BIF[2:0]																
Vidth Name	Т	PRSMTB[3:0]#	Host	Host Upstream Devices	Links		Realting link lare 0 lane 1 lane 2 lane 3 lane 4 lane 5 lane 5 lane 7 lane 8 lane 9 lane 10 lane 11 lane 12 lane 13 lane 14 lane 15	•	ane	ane 2 La	ne 3		ne 5 La	e 6 La	е -	s Lane	3 Lane	0 Lane 1	1 Lane 12	E Lane 13	Lane 14	ane 15
Mot Propent	1	06111	1 Host	4 Upstream Sockets	4 Links	06010			-	+												
1%	1x8, 1x4, 1x2, 1x1	061110	1Host	4 Upstream Sockets	4 Links	06010	1×4 Li (Socket 0 only) Li	5 () 0 ()	Link 0, L Lone 1 L	Lane 2 L	Link 0, Lane 3											
1×4	1x4, 1x2, 1x1	0b1110	1 Host	4 Upstream Sockets	4 Links	06010	1 x4 Li (Socket 0 only) Le	Lin 0. La 6 0.	Link 0, L Lane 1 L	Link 0, Li Lane 2 Li	Link 0, Lane 3											
1×2	1x2, 1x1	061110	1 Host	4 Upstream Sockets	4 Links	0b010	1x2 Li (Socket 0 only) Le		Link 0, Lone 1													
ž	1x1	061110	1Host	4 Upstream Sockets	4 Links	06010	1x1 Li (Socket 0 only) Le	Line 0.														
1x8 Option	1x8.0ption B 2x4, 2x2, 2x1	061101	1 Host	4 Upstream Sockets	4 Links	06010	2×4	Lin 0.	Link 0, L Lane 1 L	Link 0, Li Lane 2 Li	Link 0, L Lane 3 Li	Link 1, Li Lane 0 Li	Link 1, Li Lane 1 La	Link t. Lin Lane 2 Lan	Link 1, Lane 3							
x8 Option	2 x6, 2 x4, 2 x2, 2 x1 2 x6 Option B 4 x4, 4 x2, 4 x1	061101	1 Host	4 Upstream Sockets	4 Links	06010	4 × 4 U	Lin 0. La 0.	Link 0, L Lane 1 L	Link 0, Li Lane 2 Li	Link O. L Lane 3 Li	Link 1, Li Lane 0 L:	Link 1, Li Lane 1 La	Link 1, Lin Lane 2 Lar	Link 1, Link 2, Lane 3 Lane 0	2, Link2, 0 Lane 1	t, Link 2, 1 Lane 2	Link 2, Lane 3	Link 3, Lane 0	Link 3, Lone 1	Link 3, Lane 2	Link 3. Lone 3
x8 Option	1x8,1x4 2x4, 1x8 Option D 4 x2 (First 8 Isnes), 4 x1	061100	1 Host	4 Upstream Sockets	4 Links	06010	2 ×4	Line 0. 0. 0	Link 0, L Lone 1 L	Link O, Li Lana 2 Li	Link 0, L Lane 3 L	Link 1, Li Lone 0 Li	Link 1. Line 1 Li	Link (Lin Lone 2 Lor	Link 1, Lone 3							
x16 Option	1±16,1±8,1±4 2±8,2±4, 1±16 Option D 4±4,4±2 (First 8 lance).4±1	0b1 100	1 Host	4 Upstream Sockets	4 Links	06010	4 × 4	Line 0. Lare 0	Link 0, L Lane 1 L	Link 0, Li Line 2 Li	Link 0, L Lane 3 Li	Link 1, Li Lone 0 Li	Link 1, Li Lane 1 La	Link 1. Lin Lone 2. Lor	Link 1, Link 2, Lone 3 Lone 0	Link 2, Link 2, Lane 0 Lane 1	e, Link2, 1 Lone2	Link 2, Lane 3	Link 3, Lone 0	Link 3, Linke 1	Link 3, Lane 2	Link 3. Lone 3
RSVD RSVD	RSVD	061011	1 Host	4 Upstream Sockets	4 Links	06010		t	t	t	t											
2 x4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1 010	1Host	4 Upstream Sockets	4 Links	06010	2 X4	Lin 0.	Link 0, L Lane 1 L	Link 0, Li Lane 2 Li	Link 0, L Lane 3 Li	Link 1, Li Lane 0 Li	Link 1, Li Lane 1 La	Link t. Lin Lane 2 Lar	Link 1, Lane 3							
RSVD RSVD	RSVD for future x8 encoding 0b1001	061001	1 Host	4 Upstream Sockets	4 Links	06010																
RSVD	RSVD for future x8 encoding 0b1000	001000	1 Host	4 Upstream Sockets	4 Links	0b010					$\left \right $		-									
1 x16	1±16, 1±8, 1±4, 1±2, 1±1	060111	1 Host	4 Upstream Sockets	4 Links	06010	1 x4 Li (Socket 0 only) Le	Lin 0. La 0.	Link 0, L Lone 1 L	Link O, Li Lana 2 Li	Link O, Lane 3											
2 x8 Option A	2x8,2x4,2x2,2x1	060110	1 Host	4 Upstream Sockets	4 Links	06010	2 x4 Li Socket 0 & 2 only] Le				Link 0, Lane 3				Link	Link 2, Link 2, Lane 0 Lane 1	e, Link 2, 1 Lone 2	Link 2, Lane 3				
x16 Option	1x16 Option B 2x8, 2x4, 2x2, 2x1	060101	1 Host	4 Upstream Sockets	4 Links	0b010	2 x4 Li (Socket 0 & 2 only) Ls	Lin 0. Larc 0.	Link 0, L Lane 1 L	Link 0, Li Lane 2 Li	Link O, Lane 3				Link 2, Lane 0	Link 2, Link 2, Lane 0 Lane 1	t, Link 2, 1 Lane 2	Link 2, Lane 3				
x16 Option	1 ±16, 1 ±6, 1 ±6, 1 ±4 2 ±6, 2 ±4, 2 ±2, 2 ±1 1 ±16 Option C 4 ±4, 4 ±2, 4 ±1	060100	1 Host	4 Upstream Sockets	4 Links	06.010	4 × 4	Lin 0. Lano 0.	Link 0, L Lone 1 L	Link 0, Li Line 2 Li	Link 0, L Lane 3 Li	Link 1, Li Lone 0 Li	Link 1, Li Line 1 Li	Link 1. Lin Lane 2. Lar	Link 1, Link 2, Lone 3 Lone 0	2, Link2, 10 Lane1	t, Link2, 1 Lone2	Link 2, 2 Lane 3	Link 3, Lane 0	Link 3, Lone 1	Link 3, Lane 2	Link 3, Lone 3
4 x4	4 x4, 4 x2, 4 x1	060 011	1 Host	4 Upstream Sockets	4 Links	0b010	4 x 4 []	Line 0. Lare 0	Link 0, L Lane 1 L	Lane 2 L	Link 0, L Lane 3 Li	Link 1, Li Lane 0 Li	Link 1, Li Lane 1 La	Link 1, Lin Lane 2 Lai	Link 1, Link 2, Lane 3 Lane 0	2, Link2, 0 Lane1	2, Link 2, 1 Lane 2	Link 2, Lane 3	Link 3, Lane 0	Link 3, Lone 1	Link 3, Lane 2	Link 3, Lane 3
RSVD RSVD	RSVD	060010	1 Host	1 Host 4 Upstream Sockets	4 Links	06010																
RSVD RSVD	RSVD	00001	1 Host	1 Host & Upstream Sockets	4 Links	0b010																
Devn Devn	Devn	00000																				

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Table 33: Bifurcatio	n fo	C	in	ماد	<u>,</u> ц		+ 1	Eo		Soc	kot			4 5	~	ur I	In	ctr	0.00	:	nl	~	First 8 BCIo Lanos	
Table 55. Birurcatio		<u>, 1</u>		gre	: 11	105	<i>i</i> ,			[2:0							<u>Jþ:</u>	SU	ean			(5)	- FIIST & FCIE Lalles	
			Lane 15									Ι			-									
			Lane 14			\vdash	\vdash	\vdash	t		<u> </u>	t	t	t	+	t	t	-			H	t		
			Lane 13			\vdash	\vdash		t			t	F	t	+	t	t					T		
			ane 12					\vdash	F		1	t	t		+	t	1				H	t		
			Lane 11			\vdash	\vdash	\vdash	F		\vdash	t	t	t	+	t	F				H	T		
			Lane 10			\vdash	\vdash	\vdash	F		<u> </u>	t	t	t	+	t	F				H	T		
			Lane 9				F		F			t	F	t	+	t	F	1				T		
			ane 8				F		F			T	F	t	t	F	t	1				T		
			lane 7				F		F	Link 3, Lane 1	Link 3, Lane 1	t	t	Link 3, Lane 1		t	F				Ħ	T		
			Lane 6						F	Link 3, Lane 0	Link 3, Lane 0	T	F	Link 3, Lane 0		T	T				Ħ	T		
			Same					Link 1, Lane 1	Link 1,	Link 2, Lane 1	Link 2, Lane 1		Link 1,	Link 2, Lane 1			Link 1, Lane 1		Link 1, Lane 1	Link 1, Lane 1				
			Lane 4					Link 1, Lane 0	Link 1,	Link 2, Lane 0	Link 2, Lane 0		Link 1,	Link 2, Lane 0			Link 1, Lane 0		Link 1, Lane 0	Link 1. Lane 0				
			Lane 3							Link 1, Lane 1	Link 1, Lane 1			Link 1, Lane 1										
			Lane 2							Link 1, Lane 0	Link 1, Lane 0			Link 1, Lane 0										
			- 64	_	Link 0, Lane 1	_	_		_	Link 0, Lane 1	Link 0, Lane 1			Link 0, Lane 1		-	Link 0, Lane 1	-		Link 0, Lane 1				
										Link 0, Lane 0	Link 0, Lane 0			Link 0, Lane 0		Link 0,	Link 0, Lane 0	Link 0, Lane 0	Link 0, Lane 0	Link 0, Lane 0	_			
			Resulting Link	1 x2 (Socket 0 only)	1 x2 (Socket 0 only)	1 x2 (Socket 0 on V)	1x1 (Socket 0 only)	2.X2 (Socket 0.8.2 only)	2 x2 (Sortient 0 & 2 control	4 ×2	4×2		2x2 (Eastern D 2 Activ	2×4		1x2 received colut	2x2 (Socket 0 & 2 only)	1 x2 (Socket 0 only)	2 x2 (Socket 0 & 2 only)	4 x2 (Socket 0 & 2 only)				
		BIF[2:0]#	06011	00011	06011	06011	06011	06011	06011	06011	06011	06011	06011	06011	0011		06011	0b011	00011	06011	06011	11090		
			A Links	4 Links	4 Links	4 Links	4 Links	4 Links	4 Links	4 Links	4 Links	4 Links	4 Links	4 Links	Alinke	4 Links	4 Links	4 Links	4 Links		4 Links 4 Linke			
	4 x2, 4x1		4 Upstream Devices	4 Upstream Sockets	4 Upstream Sockets	4 Upstream Sockets	4 Upstream Sockets	4 Upstream Sockets	4 Upstream Sockets	4 Upstream Sockets	4 Upstream Sockets	4 Unstream Sockets	4 Upstream Sockets	4 Upstream Sockets	4 Instraam Corkate	4 Upstream Sockets	4 Upstream Sockets	4 Upstream Sockets	4 Upstream Sockets	4 Upstream Sockets	4 Upstream Sockets	4 Upstream sockets 4 Upstream Sockets		
			Host 1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 MART	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host	1 Host		
	is - First 8 lanes	Add-In-Card Encoding			0b1110	061110	061110	001101	0b1101	001100	001100		0b1010	0b1001	Ch 1000		060110	060101	060100		000010			
	Sockets, Four Upstream Lin	sported Bifurcation Modes	Card Not Present		1 x4, 1 x2, 1 x1	1x2,1x1	14	1x8,1x4,1x2,1x1 2x4 2x2 2x1	2 x8, 2 x4, 2 x2, 2 x1 4 x4 4 x7 2 x1	1 x8, 1 x4 2 x4, 2 x4, 2 x4	1 x16, 1 x8, 1 x4 2 x8, 2 x4,	RSVD RSVD	2.84, 2.82, 2.81	4 x2 (First 8 lanes), 4 x1 2 x2-2 x1	1 x2, 1 x1 DSUD for future v8 enrodine	1×16, 1×8, 1×4, 1×2, 1×1	2 x8, 2 x4, 2 x2, 2 x1	1 x16, 1 x8, 1 x4, 1 x2, 1 x1 2 x8, 2 x4, 2 x2, 2 x1	1x16,1x8,1x4 2x8,2x4,2x2,2x1 C 4x4,4x2,4x1	4 x4, 4 x2, 4 x1	RSVD	RSVD		
	Single Host, Four Upstream	Min Card Short	Name Not Present	1 x8 Option A	1 x4	241			2 x8 Ontion 8			I XIB Uption D	100		4 x2 Bean	Detan		1 x16 Option B	1 x16 Oation C	4 X4	RSVD			
	Single h	Min Care	Width n/a	×	×	×	×	×	2	2		RSVD	2	4	2C Decun	5	2 2	- Q4	- J	40	RSVD	RSVD	_	



Table 3432: Bifurcation for Dual Host, Dual Sockets and Dual Upstream Links (BIF[2:0]#=0b101)

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I cubic Second function (a) (b) (b) (b) (b) (b) (b) (b) (b) (b) (b	Host, T	wo Upstream	Dual Host, Two Upstream Sockets, Two Upstream Links			2 x8, 2 x4, 2 x2, 2 x1																		
International Internat		1	Supported Bifurcation Modes	Add-in-Card																				
mutmente Calledit meter Dillion 7 (mod. 2000 (mod. mod. 2000) Dillion 2 (mod. 2000 (mod. 2000) Dillion Dillion <thdillion< th=""> <thdillion< th=""> Dil</thdillion<></thdillion<>	th Nar	ne ne		PRSNTB(3:0)#	Host	Upstream Devices	Upstream Links	=[0:7]-ma	Resulting Link	Lane 0	Lane 1	Lane 2	Lane 3 L	Lane 4 La	Lane 5 Lar	Lane 6 Lane 7	7 Lane 8	8 Lane 9		0 Lane 1	1 Lane 1	Lane 13	Lane 10 Lane 11 Lane 12 Lane 13 Lane 14	Lane 15
Hoffmind 1 Lat 14.1.4.1 Dull 2 Mode and and 2 Mode and	No			061111	2 Host	2 Upstream Sockets	2 Links	06101																
Model Model <th< td=""><td></td><td>& Option A</td><td>1 x8, 1 x4, 1 x2, 1 x1</td><td>001110</td><td>2 Host</td><td>2 Upstream Sockets</td><td>2 Links</td><td>00101</td><td>1 x8 (Host 0 only)</td><td>Link 0, Lane 0</td><td>Link 0, L</td><td>Link 0, L</td><td>Linko, Li Lane 3 La</td><td>Link 0, Lin Lane 4 La</td><td>Link 0, Lin Lane 5 Lar</td><td>Link 0, Link 0, Lane 6 Lane 7</td><td>0 5</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></th<>		& Option A	1 x8, 1 x4, 1 x2, 1 x1	001110	2 Host	2 Upstream Sockets	2 Links	00101	1 x8 (Host 0 only)	Link 0, Lane 0	Link 0, L	Link 0, L	Linko, Li Lane 3 La	Link 0, Lin Lane 4 La	Link 0, Lin Lane 5 Lar	Link 0, Link 0, Lane 6 Lane 7	0 5							
14.11.1. 0.119.0. 21.01.2. 21.01.2. 20.01.2.		-	1 x4, 1 x2, 1 x1	001110	2 Host	2 Upstream Sockets	2 Links	06101	1 x4 (Host 0 only)	-	-	-			-									
1(1) 1(1) <th< td=""><td>-</td><td></td><td>1×2,1×1</td><td>001110</td><td>2 Host</td><td>2 Upstream Sockets</td><td>2 Links</td><td>06101</td><td>1 x2 (Host 0 only)</td><td>-</td><td></td><td>-</td><td></td><td>-</td><td>-</td><td>-</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></th<>	-		1×2,1×1	001110	2 Host	2 Upstream Sockets	2 Links	06101	1 x2 (Host 0 only)	-		-		-	-	-								
10000000 10.11.0.1.1.1 0.0110 10.000 0.0100 0.0100 0.0100 2.000000 10.11.0.1.0.1.1.1 0.0100 2.0000 2.0000 0.0000 2.000000 10.11.0.1.0.1.1.1 0.000 2.0000 2.0000 0.0000 2.000000 10.11.0.1.0.1.1 0.000 2.0000 2.0000 0.0000 2.000000 10.0000 10.0000 2.0000 2.0000 0.0000 2.00000 10.0000 2.0000 2.00000 2.0000 0.0000 0.0000 10.0000 2.00000 2.00000 2.00000 2.0000 0.0000 0.0000 10.0000 2.00000 2.000000 2.00000 2.0000 0.0000 0.0000 2.00000 2.00000 2.00000 2.00000 2.0000 0.0000 0.0000 2.00000 2.00000 2.00000 2.0000 0.0000 0.0000 0.00000 2.00000 2.00000 2.00000 2.0000 0.0000 0.0000 0.0000 0.0000 <td></td> <td>-</td> <td>1×1</td> <td>001110</td> <td>2 Host</td> <td>2 Upstream Sockets</td> <td>2 Unks</td> <td>06101</td> <td>1 x1 (Host 0 only)</td> <td>Link 0, Lane 0</td> <td></td>		-	1×1	001110	2 Host	2 Upstream Sockets	2 Unks	06101	1 x1 (Host 0 only)	Link 0, Lane 0														
J A Chyoton B A A A A J A J A A A A A A A A A A A A	- -	8 Option B	1 x8, 1 x4, 1 x2, 1 x1 2 x4, 2 x2, 2 x1	001101	2 Host	2 Upstream Sockets	2 Links	06101	1 x8 (Host 0 only)	Link 0, Lane 0	Link 0, L Lane 1 L	Link 0, L Lane 2 Li	Link 0, Li Lane 3 La	Link 0, Lin Lane 4 La	Link 0, Lin Lane 5 Lar	Link 0, Link 0, Lane 6 Lane 7	0, Host 7 Disable	t Host ed Disable	Unk 0, Host Host Host Host Host Host Host Host	Host Disable	Host Disable	d Disable	Host Disabled	Host Disabled
No. 1 m (1 m) 2 m	3	& Option B	2 x8, 2 x4, 2 x2, 2 x1 6 x4, 4 x2, 4 x1	061101	2 Host	2 Upstream Sockets	2 Links	00101	2.x8	Link 0, Lane 0	Link 0, L Lane 1 L	Link 0, L Lane 2 Li	Link 0, Li Lane 3 La	Link 0, Lir Lane 4 La	Link 0, Lin Lane 5 Lar	Link 0, Link 0, Lane 6 Lane 7	Link 0, Link 1, Lane 7 Lane 0	1, Link 1, 0 Lane 1	, Link 1, 1 Lane 2	, Link 1, 2 Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
Lat Detecto Lat Protecto Late Protec			1 ×8, 1 ×4 2 ×4,	061100	2 Host	2 Upstream Sockets	2 Links	06101	1x8 (Host 0 only)	Link 0, Lane 0	Link 0, L Lane 1 L	Link 0, L Lane 2 Li	Link 0, Li Lane 3 La	Link 0, Lir Lane 4 La	Link 0, Lin Lane S Lar	Link 0, Link 0, Lane 6 Lane 7	° °							
Million Million <t< td=""><td>-</td><td>x8 Option D</td><td>4 x2 (First 8 lanes), 4 x1</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>_</td><td>-</td><td>-</td><td></td></t<>	-	x8 Option D	4 x2 (First 8 lanes), 4 x1								-	-	-	-	-	-	-	-	-	-	_	-	-	
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34 A.S. 2.2.4.1. Double 2 More 2 Mo		0	RSVD	001011	2 Host	2 Upstream Sockets	2 Links	00101		t	t	t	╞	╞	$\left \right $	+	+							
1 2.0.7 2.0.6 2.0			2 x4, 2 x2, 2 x1 1 x6, 1 x2, 1 x1	0b1010	2 Host	2 Upstream Sockets	2 Links	06101	1 x4 (Host 0 only)	Link 0, Lane 0	Link 0, L Lane 1 L	Link 0, L Lane 2 Li	Link 0, Lane 3											
15. 12. <td></td> <td></td> <td>4 x2 (First 8 lanes), 4 x1 2 x2, 2 x1</td> <td>001001</td> <td>2 Host</td> <td>2 Upstream Sockets</td> <td>2 Links</td> <td>06101</td> <td>1 x2 (Host 0 only)</td> <td>Link 0, Lane 0</td> <td>Link 0, Lane 1</td> <td></td>			4 x2 (First 8 lanes), 4 x1 2 x2, 2 x1	001001	2 Host	2 Upstream Sockets	2 Links	06101	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1													
100 Mol. M.		22		01-1000	3 More	3 Ilnetrasm Cochate	3 Linke	06101		t	t	t	+	+	+	+	+	+	+	+	+	-		
34 060.00 2 400 2 4001 2 400 2 4001		Option A		000111	2 Host	2 Upstream Sockets	2 Unks	06101	1 x8 (Host 0 only)	Link 0, Lane 0	Link 0, L Lane 1 L	Link 0, L Lane 2 Li	Link 0, Li Lane 3 La	Link 0, Lir Lane 4 La	Link 0, Lin Lane S Lar	Link 0, Link 0, Lane 6 Lane 7	0,0							
10.1.1.1. 0.001 2100 2000 2100 2000	5	4	2 x8, 2 x4, 2 x2, 2 x1	000110	2 Host	2 Upstream Sockets	2 Unks	06101	2,48	Link 0, Lane 0	Link 0, L Lane 1 L	Lane 2 L	Link 0, Li Lane 3 La	Link 0, Lir Lane 4 La	Link 0, Lin Lane 5 Lar	Link 0, Link 0, Lane 6 Lane 7	0, Unk1, 17 Lane 0	1, Link 1, 0 Lane 1	. Unk 1, 1 Lane 2	. Unk 1, 2 Lane 3	Lane 4	Link 1, Lane 5	Link 1, Lane 6	Unk 1, Lane 7
21 000100 2 Host 2 Uppreem Societs 2 Unixs 00101 2.11 00011 2 Host 2 Uppreem Societs 2 Unixs 00101	1×		1×16, 1×8, 1×4, 1×2, 1×1 2×8, 2×4, 2×2, 2×1	060101	2 Host	2 Upstream Sockets	2 Unks	06101	2.x8	Link 0, Lane 0	Link 0, L Lane 1 L	Link 0, L Lane 2 Li	Link 0, Li Lane 3 La	Link 0, Lin Lane 4 La	Link 0, Lin Lane S Lar	Link 0, Link 0, Lane 5 Lane 7	0, Unk 1, 7 Lane 0	1, Link 1, 0 Lane 1	. Unk 1, 1 Lane 2	Lane 3	Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
4 x4, 4 x2, 4 x1 000011 2 Host 2 Upstream Sockets 2 Links 0b101	â	16 Option C	1 x16, 1 x8, 1 x4 2 x8, 2 x4, 2 x2, 2 x1 8 x4, 4 x2, 4 x1	000100	2 Host	2 Upstream Sockets	2 Links	00101	2×8	Link 0, Lane 0	Link 0, L Lane 1 L	Link 0, L Lane 2 Li	Link 0, Li Lane 3 La	Link 0, Lir Lane 4 La	Link 0, Lin Lane 5 Lar	Link 0, Lane 6 Lane 7	0, Link 1, 7 Lane 0	1, Link 1, 0 Lane 1	, Link 1, 1 Lane 2	, Link 1, 2 Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
			4 x4, 4 x2, 4 x1	000011	2 Host	2 Upstream Sockets	2 Links	06101	2 x4 (EP 0 and 2 only)	Link 0, Lane 0	Link 0, L Lane 1 L	Link 0, L Lane 2 Li	Link 0, Lane 3				Link 1, Lane 0	1, Link 1, 0 Lane 1	. Unk I. 1 Lane 2	Link 1, Lane 3				
RSVD RSVD 00000 2 Host 2 Upstream Sockets 2 Unks				000010	2 Host	2 Upstream Sockets	2 Links	00101																
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l Host,	Two Upstream	Dual Hozt, Two Upstream Sockets, Two Upstream Links			2x8,2x4,2x2,2x1																			
Nin S	Min Card Short	Supported Bifurcation Modes	Add-in-Card Eacoding			Upstream	BIF[2:0]													-			-	
Vidth R	Name		PRSNTB(3:0)#	Host	Upstream Devices	Links		Resulting Link Lare 0	Las 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7	Lane 8	lane 3 L	ane 10 L	ane 11 La	Lame 1 Lame 2 Lame 3 Lame 4 Lame 5 Lame 5 Lame 7 Lame 8 Lame 9 Lame 10 Lame 11 Lame 12 Lame 13 Lame 14 Lame 15	ae 13 Lau	e 14 La	e 15
<	Mot Present	Card Not Propert	0b1111	2 Host	2 Upstream Sockets	2 Linko	0b101																	
-	1x8	1x8, 1x4, 1x2, 1x1	061110	2 Host	2 Upstream Sockets	2 Linko	06101	1x8 (Host 0 only)	Lin 0.	Link O. Lane 1	Link O. Lone 2	Link O, Lane 3	Link 0. Lane 4	Link O, Lone 5	Link O, Lane 6	Link 0, Lone 7								
	1×1	1x4, 1x2, 1x1	0b1 110	2 Host	2 Upstream Sockets	2 Links	05101		Linco. Lateo	Link O. Lane 1	Link 0. Lane 2	Link 0, Lane 3												
	27	1x2, 1x1	0b1 110	2 Hodt	2 Upstream Sockets	2 Linko	05101		Lin 0.	Link O, Lane 1														
	1×1	1x1	0b1110	2 Host	2 Upstream Sockets	2 Linko	0b101	1x1 (Host 0 only)	Line 0, Lare 0															
_	1 x8 Option B	1x8,1x4,1x2,1x1 1x8 Option B 2x4, 2x2, 2x1	061101	2 Host	2 Upstream Sockets	2 Linko	0b101	1±8 (Host 0 only)	Lin 0. La 0.	Link 0, Lane 1	Link 0, Lone 2	Link 0, Lane 3	Link O. Lane 4	Link O, Lone 5	Link 0, Lane 6	Link O. Lone 7								
.0	2 x8 Option B	2 x8, 2 x4, 2 x2, 2 x1 2 x8 Option B 4 x4, 4 x2, 4 x1	0b1 101	2 Host	2 Upstream Sockets	2 Linko	0P101	2 x8	Lin 0. La 0.	Link 0, Lane 1	Link 0, Lone 2	Link 0, Lane 3	Link 0. Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0. Lone 7	Link 1, Lane 0	Link 1. Lane 1	Link 1, Lone 2	Link 1, L Lane 3 L	Link (L Lane 4 L:	Link 1, Li Lone 5 Lo	Link 1, L Lane 6 L	Link 1. Lone 7
		1x8,1x4 2x4,	0b1 100	2 Host	2 Upstream Sockets	2 Linko	05101	1x8 [Host 0 only]	Lin 0. La 60	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0. Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0. Lane 7								
-	1x8 Option D	1 x8 Option D 4 x2 (First 8 Isnes), 4 x1																						
	0.000	1 216, 126, 124 2 28, 2 24, 2 26, 2 24, 2 24	061100	2 Host	2 Upstream Sockets	2 Links	06101	2 x8	Lin 0. Lare 0	Link 0, Lane 1	Link O, Lone 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lone 7	Link 1, Lane 0	Link 1, Lane 1	Link 1, Lone 2 I	Link 1, L Lane 3 L	Link (L Lane 4 L:	Link 1, Li Lane 5 La	Link 1, L Line 6 L	Link 1, Lone 7
14	RSVD RSVD	RSVD	061011	2 Host	2 Upstream Sockets	2 Links	05101																	
	2 ×4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1 010	2 Host	2 Upstream Sockets	2 Linko	05101	1 z4 [Host 0 only]	Line 0. Late 0	Link O, Lane 1	Link 0. Lane 2	Link O, Lane 3												
RSVD R	RSVD	BSVD for future x8 encoding	0b1001	2 Host	2 Upstream Sockets	2 Links	0b101																	
l"	RSVD RSVD	RSVD for future x8 encoding 0b1000	0b1000	2 Host	2 Upptream Sockets	2 Linko	0b101																	
	1 x16	1x16, 1x8, 1x4, 1x2, 1x1	060111	2 Host	2 Upstream Sockets	2 Linko	05101	1±8 [Host 0 only]	Lin 0. Lare 0.	Link 0, Lane 1	Link 0, Lone 2	Link O, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lone 7								
	2 x8 Option A	2 x6, 2 x4, 2 x2, 2 x1	060110	2 Host	2 Upstream Sockets	2 Linko	0b101	2 x8	Lin 0. La e 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Line 3	Link 0. Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7	Link 1, Lane 0	Link 1. Lane 1	Link 1, Lone 2	Link 1, L Lane 3 L	Link (Li Line 4 Li	Link 1, Li Lane 5 La	Link 1, L Lane 6 L	Link 1, Lane 7
-	1x16 Option B	1x16 Option B 2x8, 2x4, 2x2, 2x1 1x16 Option B 2x8, 2x4, 2x2, 2x1	060101	2 Host	2 Upstream Sockets	2 Linko	0b101	2 x8	Lin 0. La c 0	Link O, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link O, Lane 5	Link 0, Lane 6	Link O, Lane 7	Link 1, Lone 0	Link 1. Lane 1	Link 1, Lone 2	Link 1, L Lane 3 L	Link 1. L Lane 4. Li	Link 1, Li Lane 5 La	Link 1, L Lanc 6 L	Link 1, Lone 7
-	1x16 Option C	1 x 16, 1 x 6, 1 x 4 2 x 6, 2 x 4, 2 x 2, 2 x 1 1 x 16 Option C 4 x 4, 4 x 2, 4 x 1	060100	2 Host	2 Upstream Sockets	2 Linko	06101	2 x8	Line O, Line O	Link O, Lane 1	Link O. Lone 2	Link O, Lane 3	Link O, Lane 4	Link O, Lone 5	Link O, Lano 6	Link O. Lone 7	Link 1, Lune 0	Link 1, Lane 1	Link 1. Lone 2	Lane 3 L	Linkt, L Lone 4 Li	Lane 5 La	Link 1, L Lano 6 L	Link 1, Lone 7
	4 ×4	4 x4, 4 x2, 4 x1	060 011	2 Host	2 Upstream Sockets	2 Linko	0b101	2 x4 (EP 0 and 2 only)	Linco, Larco	Link O, Lane 1	Link O, Lane 2	Link 0, Lane 3					Link 1, Lone 0	Link 1, Lane 1	Link 1, Lone 2	Link 1, Lane 3				
4	RSVD RSVD	RSVD	060010	2 Host	2 Upstream Sockets	2 Linko	0b101																	
-	RSVD RSVD	RSVD	0b0 001	2 Host	2 Host 2 Upstream Sockets	2 Linko	0b101																	
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 Table 3533: Bifurcation for Quad Host, Quad Sockets and Quad Upstream Links (BIF[2:0]#=0b110)



Upperson Devices Upperson Upperson Devices Upperson 4 Upperson Society 1 Links 4 Upperson Society 4 Li	T District District <thdistright< th=""> District Di</thdistright<>	Late 0 Late 1 Late 0 Late 1 Late 0 Link 0, Late 0 Link 0, Late 0 Link 0, Link 0, Link 0, Link 0, Link 1	taer lane 2 lane 3 lane 4 lane 5 lane 6 lane 7 lane 8 lane 9 lane 10 lane 11 lane 12 lane 13 lane 14 lane 15												l
	144 144 (there 0 only) (there 0 only) 111 (there 0 only) 214 214 214 214 214 414			Lane 3	Lane 4	ane 5 L	ت هدو		19 19	e 3 Lane	10 Lane	1 Fare	IS Lane 13	1	Lane 15
	(hor 1 or 1 st (hor 2 or 1 st (hor 2 or 1 st (hor 2 or 1 st 2 st 2 st 2 st 4 st 4 st														
	(Host 0 cold) (Host 0 cold) (Host 0 cold) (Host 0 cold) 2 st 2 st 2 st 4 st 4 st 4 st		0, Link 0, 1 Lane 2	Link O, Lane 3											
	1 12 (Hoer 0 only) 1 21 (Hoer 0 only) 2 24 4 24 4 24		0. Link 0. 1 Lane 2	Link 0, Lane 3											
	1x1 (Hoct 0 coly) 2x4 4 x4 2 x4	Link O.	0.5												
	2 14 4 14 4 14														
	4 14 2 14 4 14	Linco, Linko, Laco Lane 1	0. Link 0. 1 Lane 2	Link O, Lane 3	Link 1. Lane 0	Link 1. L Lone 1 L	Link 1, L Lane 2 L	Link 1, Lane 3							
	2.14 2.14	Lint 0, Link 0, Late 0 Lane 1	0. Link 0. 1 Lane 2	Link O, Lane 3	Link 1, Lane 0	Link 1, L Lane 1 L	Link 1, L Lane 2 L	Link 1, Li Lane 3 Li	Link 2, Lin Lanc 0 Lar	Link 2, Link 2, Lane 1 Lane 2	Link 2, Link 2, Lane 2 Lane 3	Link3. bnc0	C Link 3, D Lane 1	Link 3, Lane 2	Link 3, Lane 3
	ſ	Linco, Linko, Lanco Lanco	0, Link 0, 1 Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, L Lone 1, L	Link 1, L Lane 2 L	Link 1, Lane 3							
		Link 0, Link 0, Lac 0 Lane 1	0, Link 0, 1 Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, L Lane 1, L	Link 1, L Lane 2 L	Link 1, Li Lane 3 Li	Link 2, Lin Lane 0 Lar	Link 2, Link Lane 1 Lan	Link 2, Link 2, Lane 2 Lane 3	Link 3, B Lane 0	Link 3, Lane 1	Link 3, Lane 2	Link 3, Lane 3
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	2.14	Linc 0, Link 0, Late 0 Lane 1	Link 0, Link 0, Lane 1 Lane 2	Link O, Lane 3	Link 1, Lone 0	Link 1, L Lane 1 L	Link 1, L Lane 2 L	Link 1, Lane 3		_					
	0b110 -			_											
	0b110 1x4 (Host 0 only)	Line 0, Link 0, Lare 0 Lane 1	Lane 1 Lane 2	Link 0, Lane 3											
4 Upstream Sockets 4 Links	0b110 2 x4 (Host 0 & 2 only)		_	Link O, Lane 3					Link 1, Lin Lane 0 Lar	Link 1, Link 1, Lane 1 Lane 2	Link 1, Link 1, Lane 2 Lane 3	- 0			
4 Upstream Sockets 4 Links	0b110 2 x4 (Host 0 & 2 only)	Link 0, Link 0, Loge 0 Lone 1		Link 0, Lane 3				22	Link 1, Lin Lone 0 Lor	Link 1, Link 1, Lane 1 Lane 2	Link 1, Link 1, Lane 2 Lane 3	- 0			
4 Upstream Sockets 4 Links	05110 4 x4	Linto, Linko, Lateo Lane1	0, Link 0, 1 Lane 2	Link 0, Lane 3	Link 1, Lanc 0	Link 1. Lane 1 L	Lane 2 L	Link 1, Li Lane 3 Li	Link 2, Lin Lane 0 Lar	Link 2, Link Lane 1 Lan	Link 2, Link 2, Lane 2 Lane 3	r. Link 3, 3 Lane O	 Link 3, Lane 1 	Link 3, Lane 2	Link 3, Lane 3
4 Upstream Sockets 4 Links	0b110 4 x4	Link 0, Link 0, Lare 0 Lane 1	0, Link 0, 1 Lane 2	Link 0, Lane 3	Link 1, Lone 0	Link 1, L Lone 1 L	Link 1, L Lane 2 L	Link 1, Li Lane 3 Li	Link 2, Lin Lone 0 Lor	Link 2, Link 2, Lane 1 Lane 2	Link 2, Link 2, Lane 2 Lane 3	Link 3, Lane 0	Link 3, 1 Lone 1	Link 3, Lone 2	Link 3, Lane 3
	0b110 -														
	0b110 -									_					
4 Host 4 Upstream Sockets 4 Links	0b110 -	_				-	-	-	_						

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| | | | 1 x4, 1 x2, 1 x1
 | 1x2,1x1

 | 1×1 | 1x1
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 | | 2 x4,
4 x2 (First 8 lanes), 4 x1 | | 2 x8, 2 x4,
4 x4, 4 x2 (First 8 lanes), 4 x1 | | | nes), 4 x1
 | 2x2,2x1
1x2,1x1 | RSVD for future x8 encoding | 1 x16, 1 x8, 1 x4, 1 x2, 1 x1 | 2 x8, 2 x4, 2 x2, 2 x1 | 1, 1x1 | 2x1
 | 4 x6, 4 x2, 4 x1 | | |
| Name | INOU PIESEIIL | 1 x8 Option A | 1 44
 |

 | 1x1 | 1 x8 Option B
 | 2 x8 Option B
 | | 1 x8 Option D | | 1 x16 Option D | RSVD | 2 x4 |
 | 4 ×2 | RSVD | 1 x16 Option A | 2 x8 Option A | 1 x16 Option B | 1 v16 Ontion C
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Table <u>3634</u>: Bifurcation for Quad Host, Quad Sockets and Quad Upstream Links (BIF[2:0]#=0b1100b111)

Open Compute Project • NIC • 3.0

Rev <u>0.53</u>0v530.50

Suad/Oct Ho:	ost, Four/Eig.	Quad/Oct Host, Four/Eight Upstream Sockets, Four/Eight Upstream links	ht Upstream links		4 x2, 4 x1	-				_														
Min Card Card Short Vidth Name	Short	Supported Bifurcation Add-in-Card Modes Encoding PRSMTB(3:0)#	Add-in-Card Encoding PRSMTB[3:0]#	Host	Upstream Devices	Upstream tiaks		BIF[2:0] 8	Resetting Link lave 0 Lave 1 Lave 2 Lave 4 Lave 5 Lave 6 Lave 7 Lave 8 Lave 9 Lave 10 Lave 11 Lave 12 Lave 13 Lave 13		Lane 1	ane 2	346.3	1	14 14 14	دو اي	1	8	9 Lane	1 1	Lane 12	Lane 13	1 1	12 m
n/a Not	Not Present	Card Not Present	0b1111	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	sts 4 or 8 m		0b111																
2 2	118	1±8,1×4,1×2,1×1	061110	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	ets 4 or 8 x	_	06111	1 x2 [Host 0 only]	Lin (). La e ().	Link 0, Lane 1													
SC	124	1±4,1×2,1×1	061110	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Link	ets 4 or 8 x		06111	1 x2 Host 0 only)	la c'o	Link O, Lane 1													
2 V2	112	1±2,1×1	0b1110	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	ets 4 or 8 x		06111	1 x2 [Host 0 only]	Linco. Laco.	Link 0, Lane 1													
SC	1x1	1x1	061110	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	ets 4 or 8 x		06111	1x1 Host 0 only]	Line 0. Lare 0														
2C 1x8	8 Option B	1x8 Option B 2x4, 2x2, 2x1 1x8 Option B 2x4, 2x2, 2x1	0b1101	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Link:	ets 4 or 8 x		0b111 (He	2 x2 (Host 0 & 1 only)	Ling 0, Lage 0	Link 0, Lane 1	Link 1, Lone 0	Link 1. Lane 1											
4C 2 x6	8 Option B	2 x6 Option B 4 x4, 2 x2, 2 x1 2 x6 Option B 4 x4, 4 x2, 4 x1	0b1 101	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	ets 4 or 8 x		0b111 (H	2 x2 (Host 0 & 1 only)	Lin co.	Link O, Lone 1	Link 1, Lone 0	Link 1. Lone 1											
		1x8,1x4 24	0b1100	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	ets 4 or 8 x		Old. eee	4 x2	0 0 11	Link 0, Lees 1	Link (. Lees 0	Link 1.	Link 2, L	Link 2, Lin	Link 3, Link	Link 3,							
2C 1×8	8 Option D	1 x8 Option D 4 x2 (First 8 lanes), 4 x1								3			_			_			_					
		1 ±16, 1 × 8, 1 ±4	0b1100	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	ots 4 or 8 x			4 x2	Lin LO.		Link 1.	_	_	_	_	Link 3,							
4C 1×16	16 Option D	2 x0, 2 x4, 1 x16 Option D 4 x4, 4 x2 [First 8 lanes], 4 x1								2	Lane 1	Lane U	Lane 1	Lane U	Lane 1 La	Lane U Lan	2							
RSVD RSVD		RSVD		4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	tts 4 or 8 m		0b111																
SC	2 x4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	051010	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	ets 4 or 8 x		0b111 [H	2 x2 [Host 0 & 1 only]	Lindo, Lade 0	Link 0, Lane 1	Link 1, Lone 0	Link 1. Lane 1											
RSVD RSVD		RSVD for future x8 encoding	0b1 001	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	sts 4 or 8 m		06111																
RSVD RSVD		RSVD for future x8 encoding	0b1000	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	Nts 4 or 8 x		0b111																
9	1±16	1±16, 1×8, 1±4, 1×2, 1×1	000111	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	ets 4 or 8 x		06111	1 x2 (Host 0 only)	Lingo, Lage 0,	Link 0, Lane 1													
4C 2 x8	2 x8 Option A	2 ±8, 2 ×4, 2 ±2, 2 ×1	0110	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	ets 4 or 8 x		0b111 (H	1 x2 [Host 0 & 1 only]	Lin c 0. La c 0	Link O, Lone 1						Link 1, Lane 0	Link 1, Link 1, Lane 0 Lane 1						
4C 1×16	16 Option B	1x16 Option B 2x8, 2x4, 2x2, 2x1	060101	4/8 Host	4/8 Host 4/8 Upstream Sockets	ets 4 or 8 x2 Linko		0b111 (H	2 x2 (Host 0 & 1 only)	Linco. Laco							Link 1, Lane 0	 Link 1, Lane 1 						
4C 1×16	16 Option C	1 x16 Option C 4 x2, 4 x2, 4 x1 2 x6, 2 x4, 2 x2, 2 x1 1 x16 Option C 4 x4, 4 x2, 4 x1	000100	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Link:	ets 4 or 8 a		06111 (Hc	2 x2 (Host 0 & 1 only)	Lin (0, Lin (0,	Link 0, Lane 1						Link 2, Lane 0	Link 2, Link 2, Lane 0 Lane 1	N T.			-		
ų V	4 24	4 ±4, 4 ×2, 4 ±1	0b0 011	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	ets 4 or 8 x		0b111 (H	4 x2 [Host 0 & 1 only]	1 1 1 1 1 1	Link 0, Lane 1			Link 1. L Lane 0 L	Link 1. Lone 1									
RSVD RSVD		RSVD		4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	tts 4 or 8 m		06111																
RSVD RSVD		RSVD		4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	sts 4 or 8 x		0b111																
RXVD RXVD		Devn	00000	A 10 11	100 - 100 - 0							Í												

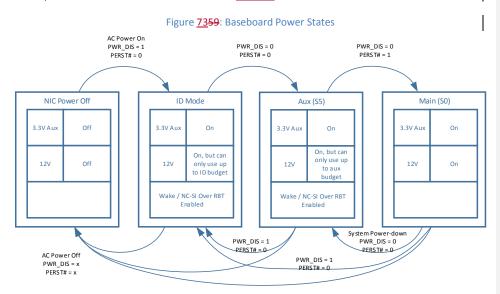


	", FOUT UDSUE	Quad Host, Four Upstream Sockets, Four Upstream links, First 8 PCIe lanes	5, First 8 PCIe lane:		4 x2, 4 x1																		
-		Supported Bifurcation Modes	Add-In-Card																				
<u>v 2</u>	Min Card Card Short Width Name		Encoding PRSNTB[3:0]#	Host	Upstream Devices	Upstream Links	BIF[2:0]#	Resulting Link	Lane 0	Lane 1	Lane 2	Lane 3 Lane 4	_	Lane S	Lane 6 La	Lane 7 La	Lane 8 Lan	Lane 9 Lane 10 Lane 11	10 Lane	11 Lane 12	12 Lane 13	5 Lane 14	Lane 15
1Ĕ	Not Present	Card Not Present	061111	4 Host	4 Upstream Sockets	4 x2 Links	06111						-				-						
	1 x8 Option A	1 ×8, 1 ×4, 1×2, 1 ×1	001110	4 Host	4 Upstream Sockets	4 x2 Links	00111	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1													
	1 x4	1 x4, 1 x2, 1 x1	001110	4 Host	4 Upstream Sockets	4 x2 Links	00111	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1													
-	1×2	1x2,1x1	001110	4 Host	4 Upstream Sockets	4 x2 Links	06111	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1													
-	1x1	1×1	001110	4 Host	4 Upstream Sockets	4 x2 Links	0b111	IXI (Host 0 only)	Link 0, Lane 0							_	-						
	1 x8 Option B	1 x8.1 x4, 1 x2, 1 x1 1 x8 Option B 2 x4, 2 x2, 2 x1	001 101	4 Host	4 Upstream Sockets	4 x2 Links	06111	2 x2 (Host 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1	Host Host Disabled	Host	Link 2, Lane 0	Link 2, 1 Lane 1 Dis	Host H sabled Disi	Host H sabled Dist	Host Ho sabled Disa	Host Host Host Host Host Host Host Host	st Host led Disable	t Host led Disable	t Host ed Disable	Host Disable	Host Disabled
	2 x8 Option B	2 x8.2 x4, 2 x2, 2 x1 2 x8 Option B 4 x4, 4 x2, 4 x1	0b1 101	4 Host	4 Upstream Sockets	4 x2 Links	0b111	2 x2 (Host 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1	Host Host Disabled	Host	Link 2, Lane 0	Link 2, 1 Lane 1 Dis	Host H sabled Disi	Host H Isabled Disi	Host Ho isabled Disa	Host Host Host Host Host Host Host Host	tt Host led Disable	t Host led Disable	t Host ed Disable	Host Disable	Host Disabled
		1 x8, 1 x4 2 x4,	001100	4 Host	4 Upstream Sockets	4 x2 Links	06111	4 x2	Link 0, Lane 0	Link 0, Lane 1	Link 1, Lane 0	Link 1, Lane 1	Link 2, Lane 0	Link 2, Li Lane 1 La	Link 3, Li Lane 0 La	Link 3, Lane 1							
	1 x8 Option D	1 x8 Option D 4 x2 (First 8 lanes), 4 x1															+	+					
		1 x16, 1 x8, 1 x4 2 x8 2 x4.	0b1100	4 Host	4 Upstream Sockets	4 x2 Links	06111	4 x2	Link 0, Lane 0	Link 0, Lane 1	Link 1, Lane 0	Link 1, Lane 1	Link 2, 1	Link 2, U	Link 3, Li Lane 0 La	Link 3, Lane 1							
-1	1 ×16 Option D	D 4 x4, 4 x2 (First 8 lanes), 4 x1											_	_	_								
Text	RSVD	RSVD	061011	4 Host	4 Upstream Sockets	4 x2 Links	0b111																
	2 x4	2 %4, 2 %2, 2 %1 1 %4, 1 %2, 1 %1	0D1010	4 Host	4 Upstream Sockets	4 x2 Links	00111	2 x2 (Host 0 & 1 only)	Link 0, Lane 0	Link 0, Lane 1	Link 1, Lane 0	Link 1, Lane 1											
		4 x2 (First 8 lanes), 4 x1	001001	4 Host	4 Upstream Sockets	4 x2 Links		4 x2	Link 0,	Link 0,	Link 1,	Link 1,	_	Link 2, Li	_	Link 3,							
	CA 2	2 x2, 2 x1 1 x2 1 x1					0b111		Lane 0	Lane 1	Lane 0	Lane 1	Lane 0	Lane 1 La	Lane 0 La	Lane 1							
1 ^{cc}	RSVD	RSVD for future x8 encoding	0b1000	4 Host	4 Upstream Sockets	4 x2 Links	06111					ľ	t	t	╞	╞	╞	╞	╞	╞	-		L
	1 x16 Option A	1 ×16, 1 ×8, 1 ×4, 1 ×2, 1 ×1	060111	4 Host	4 Upstream Sockets	4 x2 Links	06111	1 x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1													
-	2 x8 Option A	2 x8, 2 x4, 2 x2, 2 x1	00110	4 Host	4 Upstream Sockets	4 x2 Links	06111	1 x2 (Hett 0 only)	Link 0, Lane 0	Link 0, Lane 1													
-		1 x16, 1 x8, 1 x4, 1 x2, 1 x1	060101	4 Host	4 Upstream Sockets	4 x2 Links	01444	1×2	Link 0,	Link 0,		t	F	\vdash		\vdash	-			-			
-	1 x16 Option B	1 x16 Option B 2 x8, 2 x4, 2 x2, 2 x1					TITOO	(Host 0 only)	Lane 0	Lane 1			-			+	+				_		
		1 x16, 1 x8, 1 x4 2 x8, 2 x4, 2 x2, 2 x1	000100	4 Host	4 Upstream Sockets	4 x2 Links	00111	2 x2 (Host 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1			Link 2, Lane 0	Unk 2, Lane 1									
1		4 x6, 4 x2, 4 x1	000011	4 Host	4 Upstream Sockets	4 x2 Links	06111	2 x2	Link 0,	Link 0,	T	T	Link 2,	Link 2,	╞	╞	╞	╞	╞	-	+		
RSVD	RSVD	RSVD	000010	4 Host	4 Upstream Sockets	4 x2 Links	00111	-	10110.0	T allo	T	T	-	1	╞	╞	╞	╞	╞	╞	+		L
	RSVD	RSVD	00001	4 Host	4 Upstream Sockets	4 x2 Links	0b111																
											İ	ł	ł				I	I	I		I		ļ

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3.103.9 Power Capacity and Power Delivery

There are four permissible power states: NIC Power Off, ID Mode, Aux Power Mode (S5), and Main Power Mode (S0). The transition of these states is shown in Figure 73Figure 59. The max available power envelopes for each of these states are defined in Table 37Table 35.



	Tab	ole <u>3735: Po</u>	wer State	S			
Power State	PWRDIS	PERSTn	FRU	Scan Chain	RBT Link	3.3V	12V
NIC Power Off	Low	Low					
ID Mode	High	Low	Х	Х		Х	Х
Aux Power Mode (S5)	Low	Low	Х	Х	Х	Х	Х
Main Power Mode (S0)	Low	High	Х	Х	Х	Х	Х

3.10.13.9.1 NIC Power Off

In NIC power off mode, all power delivery has been turned off or disconnected from the baseboard. Transition to this state can be from any other state.

3.10.2<u>3.9.2</u> ID Mode

In the ID Mode, only 3.3V Aux is available for powering up management only functions. FRU accesses are only allowed in this mode. An add-in card shall transition to this mode when PWRDIS=1 and PERST#=0.

3.10.33.9.3 Aux Power Mode (S5)



In Aux Power Mode provides both 3.3V Aux as well as 12V Aux is available. 12V Aux may be used to deliver power to the add-in card, but only up to the Aux budget of 35W. An add-in card shall transition to this mode when PWRDIS=0 and PERST#=0.

3.10.43.9.4 Main Power Mode (S0)

In Main Power Mode provides both 3.3V and 12V (Main) across the OCP connector. The add-in card operates in full capacity. Up to 80W may be delivered on 12V, and 3.63W on the 3.3V pins. An add-in card shall transition to this mode when PWRDIS=0 and PERST#=1.

3.113.10 Power Supply Rail Requirements and Slot Power Envelopes

The baseboard provides 3.3Vaux and 12Vaux/main to both the Primary and Secondary connectors. The rail requirements are leveraged from the PCIe CEM 4.0 specification. For OCP NIC 3.0 cards, the requirements are as follows:

Power Rail	15W Slot Small Card Hot Aisle	25W Slot Small Card Hot Aisle	35W Slot Small Card Hot Aisle	80W Slot Small Card Cold Aisle	150W Large Card Cold Aisle
3.3V					
Voltage Tolerance	±9% (max)	±9% (max)	±9% (max)	±9% (max)	±9% (max)
Supply Current					
ID Mode	375mA (max)	375mA (max)	375mA (max)	375mA (max)	375mA (max)
Aux Mode	1.1A (max)	1.1A (max)	1.1A (max)	1.1A (max)	2.2A (max)
Main Mode	1.1A (max)	1.1A (max)	1.1A (max)	1.1A (max)	2.2A (max)
Capacitive Load	150µF (max)	150µF (max)	150µF (max)	150µF (max)	300µF (max)
12V					
Voltage Tolerance	±8% (max)	±8% (max)	±8% (max)	±8% (max)	±8% (max)
Supply Current					
ID Mode	100mA (max)	100mA (max)	100mA (max)	100mA (max)	100mA (max)
Aux Mode	0.7A (max)	1.1A (max)	1.5A (max)	3.3A (max)	6.3A (max)
Main Mode	1.25A (max)	2.1A (max)	2.9A (max)	6.6A (max)	12.5A (max)
Capacitive Load	500µF (max)	500µF (max)	1000µF (max)	1000µF (max)	2000µF (max)

Table <u>38</u>36: Baseboard Power Supply Rail Requirements – Slot Power Envelopes

Note: While cards may draw up to the published power ratings, the baseboard vendor shall evaluate its cooling capacity for each slot power envelope.

3.123.11 Hot Swap Considerations for 12V and 3.3V Rails

For baseboards that support system hot (powered on) add-in card insertions and extractions, the system implementer shall consider the use of hotswap controllers on both the 12Vmain/aux and 3.3Vaux pins to prevent damage to the baseboard or the add-in card. Hotswap controllers help with in-rush current limiting while also providing overcurrent protection, undervoltage and overvoltage protection capabilities.

The hotswap controller may gate the 12Vmain/aux and 3.3Vmain/aux based on the PRSNTB[3:0]# value. Per Section 3.6.3, a card is present in the system when the encoded value is not 0b1111. The PRSNTB[3:0]# may be AND'ed together and connected to the hotswap controller to accomplish this result. Per the OCP NIC 3.0 mechanical definition (Section XXX), the present pins are short pins and engage only when the card is positively seated.

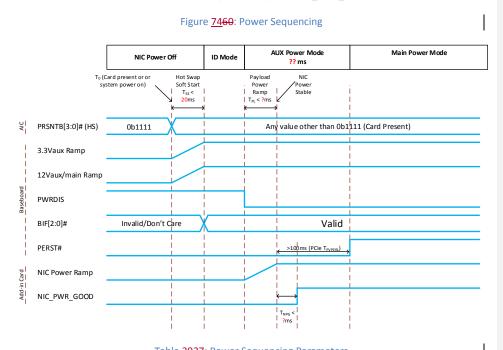
Commented [NT11]: 500uF/500uF/1000uF/1000uF/2000uF. Tentative. Waiting for recommended values from system vendors.

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Baseboards that do not support hot insertion, or hot extractions may opt to not implement these features.

3.133.12 Power Sequence Timing Requirements

The following figure shows the power sequence of PRSNTB[3:0]#, 3.3Vaux, 12Vaux/12Vmain relative to PWRDIS, BIF[2:0]#, PERSTn*, the add-in card power ramp and NIC_PWR_GOOD.



		la	able <u>39</u> 37: Power Sequencing Parameters
Parameter	Value	Units	Description
T _{ss}	20	ms	Max time between system 3.3Vaux and 12Vaux/main ramp to power stable.
T _{PL}	<mark><?</mark></mark>	ms	Max time between the NIC payload power ramp to NIC_PWR_GOOD assertion
T _{NPG}	<mark><?</mark></mark>	ms	Max time between NIC power stable and NIC_PWR_GOOD assertion.
T _{PVPERL}	>100	ms	Max time between PWRDIS deassertion and PERST# deassertion. This value is from the PCIe CEM Specification, Rev 4.0.



4 Management

OCP NIC 3.0 card management is an important aspect to overall system management. This section specifies a common set of management requirements for OCP NIC 3.0 implementations. There are three types of implementations (No Management Type, RBT Type, and MCTP Type) depending on the physical sideband management interfaces, transports, and traffic supported over different transports. An OCP NIC 3.0 implementation shall support at least one type of implementation for card management. A No Management implementation should not be used for an Ethernet add-in card.

4.1 Sideband Management Interface and Transport

OCP NIC 3.0 sideband management interfaces are used by a Management Controller (MC) or Baseboard Management Controller (BMC) to communicate with the NIC. <u>Table 40</u>Table 38 summarizes the management interface and transport requirements.

Table <u>40</u> 38: Sideband Management Interface and Tra	Insport Requirements
---	----------------------

Requirement	RBT Type	MCTP Type	
NC-SI 1.1 or later compliant RMII Based Transport (RBT)	Required		Commentee
including physical interface defined in Section 10 of DSP0222-			these cells bla but in this cas
Both SMBus 2.0 compliant of the following physical sideband		Required	what is require
interface s:			Commente
SMBus 2.0			that SMBUS is
PCIe VDM			stating that bo
Management Component Transport Protocol (MCTP) Base 1.3		Required	
(DSP0236 1.3 compliant) on both of the following physical			
bindings:			
MCTP/SMBus <u>Binding (</u> DSP0237 1.1 <u>compliant</u>)			Commente
MCTP/PCIe VDM (DSP0238 1.1)			support MCTP to create RBT
PCIe VDM compliant physical sideband interface	Optional	<u>Optional</u>	to create RBT
Management Component Transport Protocol (MCTP) Base 1.3	Optional	Optional	
(DSP0236 1.3 compliant) on MCTP/PCIe VDM Binding (DSP0238			
1.0 compliant)			

Commented [PCK12]: I think it's more clear to give the two manageability types names.

Commented [PCK13]: It maybe be more clear to leave these cells blank. This does not mean you can't implement them but in this case I think we need to focus the reader attention on what is required.

Commented [PCK14]: When PCIe is implemented, I expect that SMBUS is also required for the aux power state so I suggest stating that both SMBUS and PCIe are required for MCTP cards.

Commented [PCK15]: Many current Intel products do not support MCTP over PCIe at the same time as RBT. We would like to create RBT cards that don't require PCIe

4.2 NC-SI Traffic

DSP0222 defines two types of NC-SI traffic: Pass-Through and Control. <u>Table 41</u>Table 39 summarizes the NC-SI traffic requirements.

Table 4139: NC-SI Traffic Requirements

Requirement	RBT Type	MCTP Type
NC-SI Control over RBT (DSP0222 1.1 or later compliant)	Required	
NC-SI Control over MCTP (DSP0261 1.2 or later compliant)		Required
NC-SI Pass-Through over RBT (DSP0222 1.1 or later compliant)	Required	
NC-SI Pass-Through over MCTP (DSP0261 1.2 or later compliant)		Recommended

Commented [HS16]: For non-NIC use cases, put a caveat to allow the use of RBT without pass-through.

Note: A Management Controller (MC) implementation is allowed to use the RBT interface on an RBT Type card for NC-SI Control traffic without enabling NC-SI pass-through.

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4.3 Management Controller (MC) MAC Address Provisioning

An OCP NIC 3.0 <u>compliant card that supports NC-SI pass-through</u> -add in card shall provision one or more MAC addresses for Out-Of-Band (OOB) management traffic. The number of MC MAC addresses provisioned is implementation dependent. These MAC addresses are not exposed to the host(s) as available MAC addresses. The MC is not required to use these provisioned MAC addresses. <u>Table</u> summarizes MC MAC address provisioning requirements.

Table 4240:	MCMAC	Address Prov	isioning Re	quirements
		AUULESS FLUV	ISIUTITIE INC	uuirenienis

Requirement	RBT Type	MCTP Type
One or more MAC Addresses shall be provisioned for the MC-	Required	
 Support at least one of the following mechanism for provisioned MC MAC Address retrieval: NC-SI Control/RBT (DSP0222 1.1 or later compliant) NC-SI Control/MCTP (DSP0261 1.2 or later compliant) 	Required	

4.4 Temperature Reporting

An OCP NIC 3.0 implementation can have several silicon components including one or more ASICs implementing NIC functions and one or more optical-transceiver modules providing physical network media connectivity. It is important from the system management, it is important that temperatures of these components can be retrieved over sideband interfaces.

The temperature reporting interface is required for all OCP NIC 3.0 compliant cards with a TDP > 10W. The temperature reporting interface shall be accessible in Aux Power Mode (S5), and Main Power Mode (S0). Table 43Table 41 summarizes temperature reporting requirements. These requirements improve the system thermal management and allow the baseboard management device to access key component temperatures on an OCP NIC 3.0 card.

 Table <u>4341</u>: Temperature Reporting Requirements

Requirement	RBT Type	МСТР Туре
ASIC Temperature Reporting	Recommended	Recommended
Optical Transceiver Modules Temperature Reporting	Recommended	Recommended
 Support at least one of the following mechanisms for ASIC temperature reporting: NC SI Control (DSP0222 1.1 or later compliant) PLDM for Platform Monitoring and Control (DSP0248 1.1 compliant) 	Recommended	Recommended
Support at least one of the following mechanisms for optical modules temperature reporting: NC SI Control (DSP0222 1.1 or later compliant) PLDM for Platform Monitoring and Control (DSP0248 1.1 compliant)	Recommended	Recommended

Commented [PCK18]: I'd like to make this recommended. I want to be able to implement Intel's low power network controller that may not have this implemented.

Commented [HS17]: Add a conditional requirement that MAC address provisioning is required is NC-SI pass-through is supported. Applies to Type 2 mainly.



Where When the temperature sensor reporting function is	Required Recom	Recommended
implemented, the temperature reporting accuracy on the card	<u>mended</u>	Required
shall be within ±3°C		

4.5 Power Consumption Reporting

An OCP NIC 3.0 implementation may be able to report the power consumed by ASICs implementing NIC functions. It is important for the system management that the information about the power consumption can be retrieved over sideband interfaces. <u>Table 44</u> summarizes power consumption reporting requirements.

Table <u>4442</u>: Power Consumption Reporting Requirements

Requirement	RBT Type	MCTP Type
ASIC Power Consumption Reporting	Optional	Optional
Support at least one of the following mechanisms for ASIC-power consumption reporting: • NC-SI Control (DSP0222 1.1 or later compliant)	Optional	Optional
 PLDM for Platform Monitoring and Control (DSP0248 1.1 compliant) 		

4.6 Link Status/Speed Reporting

Link status (speed reporting is important for network oper	ations and link management. Table 42
Link status/speed reporting is important for network oper	ations and mix management. Table 45
summarizes link status and speed reporting requirements	
summarizes link status and speed reporting requirements	

Table 43: Link Status/Speed Reporting Requirements

Requirement	RBT Type	MCTP Type	
Link Status Reporting	Required	Required	
Support at least one of the following mechanisms for reporting the link status: • NC-SI Control (DSP0222 1.1 compliant) • PLDM for Platform Monitoring and Control (DSP0248 1.1 compliant)	Required	Required	
Link Speed Reporting	Required	Required	
Support at least one of the following mechanisms for reporting the link speed: CSI Control (DSP0222 1.1 compliant) PLDM for Platform Monitoring and Control (DSP0248 1.1 compliant)	Required	Required	

Commented [HS19]: Should we remove this section or

mandate PLDM only?

4.344.6 Pluggable Module Status Reporting

Pluggable modules like <u>an optical modules or a</u> direct attach<u>ed copper</u> cables are is used to connect <u>an</u> OCP NIC to <u>a physical mediamedium</u>. It is important to know the presence of pluggable modules and

Commented [HS20]: Should we make it mandatory?

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information about insertion/deletion of pluggable modules. <u>Table 45</u>Table 44 summarizes pluggable status reporting requirements.

Table <u>45</u>44: Pluggable Module Status Reporting Requirements

Requirement	RBT Type	MCTP Type
Pluggable Module Presence Reporting	Recommended	Recommended
		Recommended
Pluggable Module Insertions/Deletions Reporting	Recommended	Recommended
 Support at least one of the following mechanisms for reporting the pluggable module insertions/deletions: NC SI Control (DSP0222 1.1 or later compliant) PLDM for Platform Monitoring and Control (DSP0248 1.1 compliant) 	Recommended	Recommended

4.354.7 Out-Of-Band Firmware Inventory and Update

An OCP implementation can have different types of firmware components for data path, control path, and management path operations. It is desirable that OCP NIC 3.0 implementations support an OS-independent Out-Of-Band mechanism for the firmware update. <u>Table 46</u> summarizes out-of-band firmware update requirements.

 Table 4645
 Out-Of-Band Firmware Update Requirements

RBT Type	MCTP Type
Required	Required
Optional	Optional
	Required

Firmware Update

The OCP NIC 3.0 add in card shall support device firmware upgrades from the BMC controller.

4.7.1 Secure Firmware

The OCP NIC 3.0 add-in card shall support secured firmware.

Where When -the secured firmware feature is enabled, the OCP NIC 3.0 add-in card shall allow only update and execute signed firmware.

4.7.2 Firmware InventoryQueries

The OCP NIC 3.0 add-in card shall allow queries to obtain the firmware version, device model, and device ID via in-band and out-of-band interfaces without impacting NIC function and performance of said paths.

4.7.3 Firmware Inventory and Update in Multi-Host Firmware QueriesEnvironments

A multi-host capable OCP NIC 3.0 add-in card shall gracefully handle concurrent in-band queries from multiple hosts and out-of-band access from the BMC the management status and firmware, device model, and device ID information.

http://opencompute.org

Commented [HS21]: Make it mandatory



A multi-host capable OCP NIC 3.0 add-in card shall only permit one entity to perform write accesses to NIC firmware at a time, without creating contention.

<u>A multi-host capable OCP NIC 3.0 add-in card shall gracefully handle exceptions when more than one entity attempts to perform concurrent NIC firmware writes.</u>

4.364.8 NC-SI Over RBT Sideband InterfacePackage Addressing and Hardware Arbitration Requirements

NC-SI <u>o</u>Over RBT provides a low speed management path for the add in card. This is implemented via RMII pins between the BMC and the add in <u>OCP NIC 3.0</u> card. <u>NC SI Over RBT is the recommended</u> management method for OCP NIC 3.0 cards. Protocol and implementation <u>details of NC-SI over RBT</u> details can be found in the DMTF DSP0222 standard.

4.36.14.8.1 NC-SI Oover RBT Package Addressing

NC-SI Over-over RBT capable OCP NIC 3.0 devices cards must-shall use a unique Package ID per ASIC when multiple ASICs share the single NC-SI physical interconnect to ensure there are no addressing conflicts.

Baseboards use the Slot_ID pin on the Primary Connector for this identification. The Slot_ID value may be directly connected to GND (Slot ID = 0), or pulled up to 3.3Vaux (Slot ID = 1).

For add in cards, Package ID[2:0] is a 3-bit field and is encoded in the NC-SI Channel ID as bits [7:5]. Package ID[2] is-defaults to 0b0 in the NC-SI specification, but is optionally configurable if the target silicon supports configuring this bit. Package ID[1] is <u>directly</u> connected to the SLOT_ID pin-and is directly connected to the Slot_ID pin. Package ID[0] is set to 0b0 for Network <u>Controller ASIC Silicon #</u>0. For an OCP NIC 3.0 add-in cards with two discrete silicon instances, Package ID[10] <u>shall be is</u>-set to 0b1 <u>for</u> <u>Network Controller ASIC #1</u>. Refer to the <u>specific</u> endpoint device datasheet for details on the Package ID configuration options.

Up to four silicon devices are supported on the bus if only Package ID[1:0] is configurable (e.g. Package ID[2] is statically set to 0b0). Up to eight silicon devices are supported on the NC-SI bus if Package ID[2:0] are all configurable. Refer to the DMTF DSP0222 standard for more information <u>on package addressing</u> and Package ID.

4.36.24.8.2 Arbitration Ring Connections

For baseboards that implement two or more Primary Connectors, the NC-SI <u>Over-over</u> RBT arbitration ring may be connected to each other. The arbitration ring <u>must-shall</u> support operation with a one card, or both cards installed.

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Figure 63

Figure 49 shows an example connection with dual Primary Connectors.

4.374.9 SMBus 2.0 Addressing Requirements Interface

The SMBus provides a low speed management bus for the add inOCP NIC 3.0 card. The FRU EEPROM and on-board temperature sensors are connected on this bus. Additionally, network controllers may utilize the SMBus interface for NC SI over MCTP communications. Proper power domain isolation shall be implemented on the NIC.

Note: The preferred network controller management path is NC-SI Over RBT, as described in Section 4.9. Silicon devices may offer both a SMBus and NC-SI Over RBT interface. In such instances, the add-in card developer shall choose NC-SI Over RBT.

4.37.34.9.1 SMBus Address Map

All predefined SMBus addresses for OCP NIC 3.0 are shown in <u>Table 47Table 46</u>. Baseboard and add-in designers must ensure additional devices do not conflict. The addresses shown are in 8-bit format and represent the read/write address pair.

Commented [HS22]: Can we agree on one method for discovering SMBus slave address? SMBus ARP support? Hemal/Yuval to draft text.

Та	ble <u>47</u> 4 6 : Power S	Sequencing ParametersSMBus Address Map		
Address (8-bit)	Device	Notes]	
0x <mark>TBD</mark>	Network	Value dependent on NIC vendors.		Commented [TN23]: Should we pre-define a range?
	Controller IC			
0x98 / 0x99	Temperature Sensor	TMP422/423 Temperature sensor	-	
		Optional. Used for remote on-die thermal sensing. Optional.		
		Powered from Aux power domain.		
0x9E / 0x9F	Temperature	TMP421 Temperature sensor.		
	Sensor			
		Optional. Used for remote on die thermal sensing. Optional.		
		Powered from Aux power domain.		
0xA0 / 0xA1 – SLOT0	EEPROM	On-board FRU EEPROM.		
0xA2 / 0xA3 – SLOT1				Commented [JN24]: Ws#9: Need to add one address for 2x
		Mandatory. Powered from Aux power domain.	l	NIC on same bus with SLOT_ID
		The EEPROM ADDR0 pin shall be connected to the SLOT_ID pin on the add-in card gold finger to allow two NIC add-in cards to exist on the same I ² C bus.		

4.384.10 FRU EEPROM

4.38.14.10.1 FRU EEPROM Address, Size and Availability

The FRU EEPROM provided for the baseboard to determine the card type and is directly connected to the SMBus on the card edge. Only one EEPROM is required for a single physical add-in card regardless of the PCIe width or number of physical card edge connectors it occupies. The FRU EEPROM shall be connected to the Primary connector SMBus.

Commented [HS25]: Should PLDM for FRU data transfer be

specified? Hemal to take a look at PLDM for FRU spec mandatory requirements and optional requirements as they apply to OCP NIC 3.0.



The EEPROM is addressable at 0xA2/0xA3 for the write/read pair in 8-bit format. The size of EEPROM is shall be at least 4Kbits for the base EEPROM map. Add-in card suppliers may use a larger size EEPROM if needed to store vendor specific information.

The FRU EEPROM is readable in all three power states (ID mode, AUX(S5) mode, and MAIN(S0) mode.

4.38.24.10.2 FRU EEPROM Content Requirements

The FRU EEPROM shall follow the data format specified in the IPMI Platform Management FRU Information Storage Definition v1.2. Use OEM record 0xC0, offset 0x01 through 0x05 to store specific records for the OCP NIC.

Table <u>48</u>47: FRU EEPROM Record – OEM Record 0xC0, Offset 0x00

Offset 0	Description
	Manufacturer ID, LS Byte first (3 bytes total)

Table 4948: FRU EEPROM Record – OEM Record 0xC0, Offset 0x01

Offset 1	Primary Connector PRSNTB [3:0]#
Ob1110 (0x0E)	Follows Pinout; to be filled after the pinout table is fixed
0b1101 (0x0D)	
0b1100 (0x0C)	
0b1010 (0x0A)	
0b0111 (0x07)	
0b0110 (0x06)	
0b0101 (0x05)	
0b0100 (0x04)	
0b0011 (0x03)	
0b1011 (0x0B)	Not a valid reading – Wrong EEPROM programming
0b1111 (0x0F)	Not a valid reading – Wrong EEPROM programming
All others	RFU
No FRU device detected	No NIC connected / bad connection

explicitly states the number of PCIe REFCLKs used by the add-in card? The add-in card recommendation is to leave unused REFCLK pins as N/C and is consistent with the termination requirement on the baseboard only.

Commented [TN26]: Is there a FRU EEPROM record that

The baseboard should have some mechanism to disable PCIe REFCLKs to reduce EMI.

Commented [JN27]: To be refreshed; may match to present pin decode table.

Commented [HS28]: This allows a NIC implementation to declare what connector pins are populated.

Table 5049: FRU EEPROM Record – OEM Record 0xC0, Offset 0x02

Offset 2	Secondary Connector PRSNTB [3:0]#
0b1110 (0x0E)	Follows Pinout; to be filled after the pinout table is fixed
0b1101 (0x0D)	
0b1100 (0x0C)	
0b1010 (0x0A)	
0b0111 (0x07)	
0b0110 (0x06)	
0b0101 (0x05)	

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0b0100 (0x04)	
0b0011 (0x03)	
Ob1011 (0x0B)	Not a valid reading – Wrong EEPROM programming
0b1111 (0x0F)	Not a valid reading – Wrong EEPROM programming
All others	RFU
No FRU device detected	No NIC connected / bad connection

Table <u>51</u>50: FRU EEPROM Record – OEM Record 0xC0, Offset 0x03

Offset 3	Card max power in Aux(S5)
0x01 - 0xFE	Hex format in Watts when NIC is in AUX(S5) mode; LSB = 1x Watt; roundup to the nearest Watt for fractional values.
OxFF	Invalid entry
0x00	Invalid entry

Table <u>52</u> 51: FRU EEPROM Record – OEM Record 0xC0, Offset 0x04			
Offset 4	Card max power in Main(S0)		
0x01 - 0xFE	Hex format in Watts when NIC is in Main (S0) mode; LSB = 1x Watt; roundup to the nearest Watt for fractional values.		
0xFF	Invalid entry		
0x00	Invalid entry		

Table 52: FRU EEPROM Record – OEM Record 0xC0, Offset 0x05			
Offset 5	Thermal Reporting Interface		
0x01	Emulated thermal reporting on SMBus		
0x02	Remote on die sensor with TMP421 on SMBus		
0x04	PLDM thermal reporting via NC-SI over RBT		

4.39 FW Requirements

(Editors note (Jia): Tentative list; collecting feedback)

4.39.1<u>1.1.1</u>Firmware Update

The OCP NIC 3.0 add-in card shall support device firmware upgrades from the BMC controller.

1.1.1 Secure Firmware

The OCP NIC 3.0 add in card shall support secured firmware.

 Where the secured firmware feature is enabled, the OCP NIC 3.0 add-in card shall allow only update and execute signed firmware.

4.39.21.1.1 Firmware Queries

 The OCP NIC 3.0 add in card shall allow queries to obtain the firmware version, device model, and device ID via in band and out-of-band interfaces without impacting NIC function and performance of said paths. **Commented [HS29]:** Combine this section with 4.8. Define secure firmware including secure boot and secure firmware update. Refer to NIST spec. Need to specify it in the way that allows a NIC to be deployed in a platform where secure firmware updated in not allowed. Define firmware referred to here. For smart NIC type of use case, there are multiple types of firmware. Add text for ROM based firmware.

Commented [TN30]: From Jia in 12/20/2017 e-mail:

Hemal:

FB suggests to add these $\rm 2x$ requirements to the OCP NIC 3.0 specification.

Live firmware upgrade (ability for new firmware to kick in w/o reboot)
 "Flash ROM" support for firmware

Want to learn your take.

Thanks.

Jia



4.39.31.1.1 Multi-Host Firmware Queries

- —A multi-host capable OCP NIC 3.0 add in card shall gracefully handle concurrent in band queries from multiple hosts and out-of-band access from the BMC the management status and firmware, device model, and device ID information.
- A multi-host capable OCP NIC 3.0 add in card shall only permit one entity to perform write accesses to NIC firmware at a time, without creating contention.
- A multi host capable OCP NIC 3.0 add in card shall gracefully handle exceptions when more than one entity attempts to perform concurrent NIC firmware writes.

- Thermal Reporting Interface

The OCP NIC 3.0 thermal reporting interface is defined on the primary connector SMBus or via NC SI over RBT depending on the implementation method described in this section.

This requirement improves the system thermal management and allows the baseboard management device to access key component temperatures on an OCP NIC.

There are three defined methods to implement thermal reporting described in this section: emulated thermal reporting, remote on-die sensing and via Platform Level Data Model (PLDM).

Emulated thermal reporting and remote on die sensing the two methods defined in OCP NIC 2.0 and is used in the current 3.0 spec release. In both cases, the BMC treats the temperature sensors as a TI/TMP421 (or equivalent) device. The emulated temperature sensor is accessible at slave address 0x3E/0x3F as the read/write pair in 8 bit format over the SMBus.

The third reporting method is using PLDM. This is the recommend implementation for OCP NIC 3.0. PLDM uses the NC SI over RBT as the underlying protocol.

A thermal reporting interface is required for all OCP NIC 3.0 complaint cards with a TDP > 10W.

Thermal reporting interface shall be accessible in AUX(S5) mode, and MAIN(S0) mode.

Remote on-die sensing

Alternatively, one TMP421 sensor can be used to do on die temperature sensing for IC with thermal diode interface with TMP421 remote sensing channel; Connection diagram is shown in Figure 61. For add-in cards that require more than one remote on-die sense point, a TMP422/TMP423 can be used and slave address is ox98/ox99 (8 bit).

Figure 61: Block Diagram for Remote on die Sensing

Commented [HS31]: This section needs to be combined with 4.4.

Commented [HS32]: Should we remove this section? Need agreement pending Intel comments.

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Commented [JN33]: Update pin # of diagram



5 Data Network Requirements

5.1 Network Boot

OCP NIC 3.0 shall support network booting in uEFI system environment with both IPv4 and IPv6 network booting.

For UEFI booting, below features are required (tentative list; collecting feedback)

- EFI_DRIVER_BINDING_PROTOCOL (for starting and stopping the driver)
- EFI_DEVICE_PATH_PROTOCOL (provides location of the device)
- EFI_MANAGED_NETWORK_SERVICE_BINDING_PROTOCOL (asynchronous network packet I/O services)
- EFI_DRIVER_DIAGNOSTICS2_PROTOCOL & EFI_DRIVER_DIAGNOSTICS_PROTOCOL (driver will allow the UEFI shell command *drvdiag* to perform a cursory check of the connections managed by the driver)
- Human Interface Infrastructure (HII) protocols
- EFI_DRIVER_HEALTH_PROTOCOL
- EFI_FIRMWARE_UPDATE_PROTOCOL



Routing Guidelines and Signal Integrity Considerations 6

6.1 NC-SI Over RBT

For the purposes of this specification, the min and max electrical trace length of the NC-SI signals shall be between 2 inches and 4 inches. The traces shall be implemented as 50 Ohm impedance controlled nets.

6.2 PCIe

This section is a placeholder for the PCIe routing guidelines and SI considerations.

Add-in card suppliers shall follow the PCIe routing specifications. At this time, the OCP NIC subgroup is working to identify and agree to the channel budget for an add-in card and leave sufficient margin for the baseboard. Refer to the PCIe CEM and PCIe Base specifications for end-to-end channel signal integrity considerations.

Commented [JN34]: 1.Discussion point of 1st draft (define or not define in 1.00?) 2. Anything other than loss and impedance shall be defined to be complete

Commented [TN35]: Point to the PCIe spec for the electrical specs (See PCIe CEM Section 6.3.x. 4.7.x, 4.8) and SFF-TA-1002.

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7 Thermal and Environmental

7.1 Environmental Requirements

Specifics are not included to permit adoption of OCP 3.0 NIC in systems with varying thermal requirements and boundary conditions. The system adopting OCP NIC should define air flow direction, local approach air temperature and speed to the NIC, operational altitude and relative humidity.

For example, a system configured with I/O facing the cold aisle, can specify approach air temperature and speed of 35°C and 200 LFM respectively, with airflow impinging on the I/O modules first and an operational altitude of 6000 feet.

7.1.1 Thermal Reporting interface

[Link to 4.6; this session can be incorporated into Chapter 4.6] The NIC should support temperature reporting for key components on the card (including readings from active I/O modules). To improve thermal efficiency, the recommended accuracy for temperature sensors on the card is $\pm 3^{\circ}$ C. A power reporting interface is optional for low-power NICs (less than 10W), but strongly recommended for higher-powered NICs.

7.1.2 Thermal Simulation Boundary Example

Placeholder for the link to upcoming test fixture documentation (under development).

7.2 Shock & Vibration

This specification does not cover the shock and vibration testing requirements for an OCP NIC 3.0 add in card or its associated baseboard systems. OCP NIC 3.0 components are deployed in various environments. It is up to each add-in card and baseboard vendor to decide how the shock and vibration tests shall be done.

7.3 Regulatory

An OCP NIC 3.0 add-in card shall meet the following compliance requirements:

- **RoHS 2 Directive (2011/65/EU)** aims to reduce the environmental impact of electronic and electrical equipment (EEE) by restricting the use of certain hazardous materials. the substances banned under RoHS are lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls, polybrominated diphenyl ether, and four phthalates.
- REACH Regulation (EC) No 1907/2006 addresses the production and use of chemical substances and their potential impact on human health and the environment.
- Waste Electrical and Electronic Equipment ("WEEE") Directive (2012/19/EU) mandates the treatment, recovery and recycling of EEE.
- The Persistent Organic Pollutants Regulation (EC) No. 850/2004 bans production, placing on the market and use of certain persistent organic pollutants.
- The California Safe Drinking Water and Toxic Enforcement Act of 1986 ("Prop 65") sets forth a list of regulated chemicals that require warnings in the State of California.
- The Packaging and Packaging Waste Directive 94/62/EC limits certain hazardous substances in the packaging materials

http://opencompute.org

Commented [JN36]: Suggests edit here. Up to discussion



- **Batteries Directive 2006/66/EC** regulates the manufacture and disposal of all batteries and accumulators, including those included in appliances.
- CE
- FCC Class A

An OCP NIC 3.0 add-in card is recommended to meet below compliance requirements:

- Halogen Free: IEC 61249-2-21 Definition of halogen free: 900ppm for Br or Cl, or 1500ppm combined.
- Arsenic: 1000 ppm (or 0.1% by weight)
- Emerging: US Conflict Minerals law: section 1502 of the Dodd-Frank Act requires companies using tin, tantalum, tungsten, and gold ("3TG") in their products to verify and disclose the mineral source. While this does not apply to products that are used to provide services, such as Infrastructure hardware products, the OCP NIC Subgroup is considering voluntarily reporting of this information.

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8 Revision History

Author	Description	Revision	Date
Thomas Ng	Initial draft	0.5 <u>3</u>	12 01/ 22 03/ 2017 2018
Intel Corporation			1