

OCP NIC 3.0 Design Specification

Version 0.01

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Table of Contents

1	Overvie	ew	7
	1.1	License	7
	1.2	Background	8
	1.3	Acknowledgements	9
	1.4	Overview	9
	1.4.	1 Mechanical Form factor overview	9
	1.4.	2 Electrical overview	12
	1.5	References	12
2	Card Fo	orm Factor	14
	2.1	Overview	14
	2.2	Form Factor Options	14
	2.3	I/O bracket	16
	2.4	Line Side I/O Implementations	16
	2.5	LED Implementations	17
	2.5.	1 Baseboard LEDs Configuration Over the Scan Chain	17
	2.5.	2 Add-in Card LED Configuration	18
	2.5.	3 LED Ordering	20
	2.6	Mechanical Keepout Zones	20
	2.6.	Baseboard Keep Out Zones	20
	2.6.	2 Add-in Card Keep Out Zones	20
	2.7	Labeling Requirements	20
	2.8	Insulation Requirements	21
	2.9	NIC Implementation Examples	21
	<mark>2.10</mark>	Non-NIC Use Cases	21
	2.10	0.1 PCIe Retimer card	21
	<mark>2.1</mark> 0	0.2 Accelerator card	21
	<mark>2.1</mark> 0	0.3 Storage HBA / RAID card	21
3	Card Ed	dge and Baseboard Connector Interface	
	3.1	Gold Finger Requirement	

	3.1.1	Gold Finger Mating Sequence	22
3.2	Ва	seboard Connector Requirement	25
3.3	Pir	definition	26
3.4	Sig	nal Descriptions – Common	32
	3.4.1	PCIe Interface Pins	32
	3.4.2	PCIe Present and Bifurcation Control Pins	36
	3.4.3	SMBus Interface Pins	38
	3.4.4	Power Supply Pins	39
	3.4.5	Miscellaneous Pins	41
3.5	Sig	nal Descriptions – OCP Bay (Primary Connector)	41
	3.5.1	PCIe Interface Pins – OCP Bay (Primary Connector)	42
	3.5.2	NC-SI Over RBT Interface Pins – OCP Bay (Primary Connector)	44
	3.5.3	Scan Chain Pins – OCP Bay (Primary Connector)	50
	3.5.4	Primary Connector Miscellaneous Pins – OCP Bay (Primary Connector)	57
3.6	PC	Ie Bifurcation Mechanism	58
	3.6.1	PCIe Add-in Card to Baseboard Bifurcation Configuration (PRSNTA#,	
	PRSNT	3[3:0]#)	59
	3.6.2	PCIe Baseboard to Add-in Card Bifurcation Configuration (BIF[2:0]#)	59
	3.6.3	PCIe Bifurcation Decoder	60
	3.6.4	Bifurcation Detection Flow	62
	3.6.5	PCIe Bifurcation Examples	63
3.7	PC	Ie Clocking Topology	69
3.8	PC	Ie Bifurcation Results and REFCLK Mapping	71
3.9	Ро	wer Capacity and Power Delivery	80
	3.9.1	AC Power Off	80
	3.9.2	ID Mode	80
	3.9.3	Aux Power Mode (S5)	80
	3.9.4	Main Power Mode (S0)	81
3.10) Po	wer Supply Rail Requirements	81
3.13	1 Hc	t Swap Considerations for 12V and 3.3V Rails	81
3.12	2 Po	wer Sequence Timing Requirements	82
Ma		ent	
		IRus Interface	84

4



	4.2	NC-SI Sideband Interface	84
	4	1.2.1 NC-SI addressing and Arb#	84
	4.3	MAC Address Requirement	84
	4.4	FRU EEPROM	84
	4	1.4.1 Minimum EEPROM Size	84
	4	1.4.2 EEPROM Map Definition	84
	4	1.4.3 EEPROM Address	84
	4.5	FW Requirement (TBD)	84
	4.6	Thermal Reporting Interface	84
5	Data	Network Requirement	85
	5.1	Network Booting (collect view from OEMs and hyperscale)	85
6	Rout	ing Guidelines and Signal Integrity Considerations	86
	6.1	NC-SI Over RBT	86
7	Ther	mal and Environmental	86
	7.1	Environmental Requirements	86
	7	7.1.1 Thermal Simulation Boundary Example	86
	7.2	Shock & Vibration	86
	7.3	Regulation	86
8	Revis	sion History	87

List of Figures

Figure 1: Representative Small OCP NIC 3.0 Card with Quad SFP Ports	8
Figure 2: Representative Large OCP NIC 3.0 Card with Dual QSFP Ports and on-board DRAM	9
Figure 3: Small and Large Card Form-Factors (not to scale)	10
Figure 4: Example Small Card Form Factor	14
Figure 5: Example Large Card Form Factor	15
Figure 6: Primary Connector (4C + OCP Bay) with 4C and 2C Add-in Cards	16
Figure 7: LED Ordering – Example Small Card Link/Activity and Speed LED Placement	20
Figure 8: Small Size Primary Connector Gold Finger Mating Card Dimensions – x16 – Top Side	22
Figure 9: Small Size Primary Connector Gold Finger Mating Card Dimensions – x16 – Bottom Side	22
Figure 10: Large Size Card Gold Finger Mating Card Dimensions – x32 – Top Side	22
Figure 11: Large Size Card Gold Finger Mating Card Dimensions – x32 – Bottom SideSide	22
Figure 12: 168-pin Base Board Primary Connector – Right Angle	25
Figure 13: 140-pin Base Board Secondary Connector – Right Angle	25
Figure 14: 168-pin Base Board Primary Connector – Straddle Mount	25
Figure 15: 140-pin Base Board Secondary Connector – Straddle Mount	25
Figure 16: Primary and Secondary Connector Locations for Large Card Support	26
Figure 17: PCIe Present and Bifurcation Control Pins	37
Figure 18: Example Power Supply Topology	40
Figure 19: NC-SI Over RBT Connection Example	49
Figure 20: Scan Bus Connection Example	56
Figure 21: PCIe Bifurcation Pin Connections Support	59
Figure 22: Single Host (1 x16) and 1 x16 Add-in Card (Single Controller)	63
Figure 23: Single Host (2 x8) and 2 x8 Add-in Card (Dual Controllers)	64
Figure 24: Four Hosts (4 x4) and 4 x4 Add-in Card (Single Controller)	65
Figure 25: Four Hosts (4 x4) and 4 x4 Add-in Card (Four Controllers)	66
Figure 26: Single Host with no Bifurcation (1 x16) and 2 x8 Add-in Card (Two Controllers)	68
Figure 27: PCIe Interface Connections for 1 x16 and 2 x8 Add-in Cards	69
Figure 28: PCIe Interface Connections for a 4 x4 Add-in Card	70
Figure 29: Baseboard Power States	80
Figure 30: Power Seguencing	82



List of Tables

Table 1: OCP 3.0 Form Factor Dimensions	10
Table 2: Baseboard to OCP NIC Form factor Compatibility Chart	11
Table 3: OCP NIC 3.0 Card Definitions	16
Table 4: OCP 3.0 Line Side I/O Implementations	16
Table 5: Baseboard LED Configurations with Two Physical LEDs per Port	18
Table 6: Add-in Card LED Configuration with Two Physical LEDs per Port	19
Table 7: Contact Mating Positions for the Primary and Secondary Connectors	23
Table 8: Primary Connector Pin Definition (x16) (4C + OCP Bay)	26
Table 9: Secondary Connector Pin Definition (x16) (4C)	30
Table 10: Pin Descriptions – PCIe 1	32
Table 11: Pin Descriptions – PCIe Present and Bifurcation Control Pins	36
Table 12: Pin Descriptions – SMBus	38
Table 13: Pin Descriptions – Power	39
Table 14: Pin Descriptions – Miscellaneous 1	41
Table 15: Pin Descriptions – PCIe 2	42
Table 16: Pin Descriptions – NC-SI Over RBT	44
Table 17: Pin Descriptions – Scan Chain	50
Table 18: Pin Descriptions – Scan Chain DATA_OUT Bit Definition	52
Table 19: Pin Descriptions – Scan Bus DATA_IN Bit Definition	53
Table 20: Pin Descriptions – Miscellaneous 2	57
Table 21: PCIe Bifurcation Decoder for x16 and x8 Card Widths	
Table 22: PCIe Clock Associations	69
Table 23: Bifurcation for Single Host, Single Socket and Single Upstream Link (BIF[2:0]#=0b000)	72
Table 24: Bifurcation for Single Host, Single Socket and Single/Dual Upstream Links (BIF[2:0]#=0b000)	73
Table 25: Bifurcation for Single Host, Single Socket and Single/Dual/Quad Upstream Links (BIF[2:0]#=0b000)	74
Table 26: Bifurcation for Single Host, Dual Sockets and Dual Upstream Links (BIF[2:0]#=0b001)	75
Table 27: Bifurcation for Single Host, Four Sockets and Dual Upstream Links (BIF[2:0]#=0b010)	76
Table 28: Bifurcation for Dual Host, Dual Sockets and Dual Upstream Links (BIF[2:0]#=0b101)	77
Table 29: Bifurcation for Quad Host, Quad Sockets and Quad Upstream Links (BIF[2:0]#=0b110)	78
Table 30: Bifurcation for Quad Host, Quad Sockets and Quad Upstream Links (BIF[2:0]#=0b110)	79
Table 31: Power States	80
Table 32: Baseboard Power Supply Rail Requirements	81
Table 33: Power Sequencing Parameters	83

1 Overview

1.1 License

As of April 7, 2011, the following persons or entities have made this Specification available under the Open Web Foundation Final Specification Agreement (OWFa 1.0), which is available at http://www.openwebfoundation.org/legal/the-owf-1-0-agreements/owfa-1-0: Facebook, Inc.

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1.2 Background

The OCP NIC 3.0 specification is a follow-on to the OCP 2.0 form-factor for PCIe add-in cards. The OCP NIC 3.0 specification supports two basic card sizes: Small Card, and Large Card. The Small Card allows for up to 16 PCIe lanes on the card edge while a Large Card supports up to 32 PCIe. Compared to the OCP NIC 2.0 release, the updated specification provides a broader solution space for NIC and system vendors to support the following use case scenarios:

- NICs with a higher TDP
- Support up to 79W of power delivery to a single connector (Small) card; and 158W to a dual connector (Large) card
- PCIe Gen4 and Gen5 on the system and add-in card
- Support for upto 32 lanes of PCIe per add-in card
- Support for single host and multi-host environments
- Support a greater board area for more complex add-in card designs
- Support for Smart NIC implementations with on-board DRAM
- Simplification of FRU installation and removal while reducing overall down time

A representative Small Card OCP 3.0 NIC mezzanine card is shown in Figure 1 and a representative Large Card is shown in Figure 2.

Figure 1: Representative Small OCP NIC 3.0 Card with Quad SFP Ports

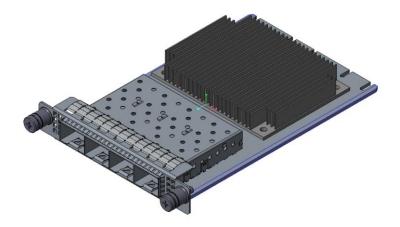
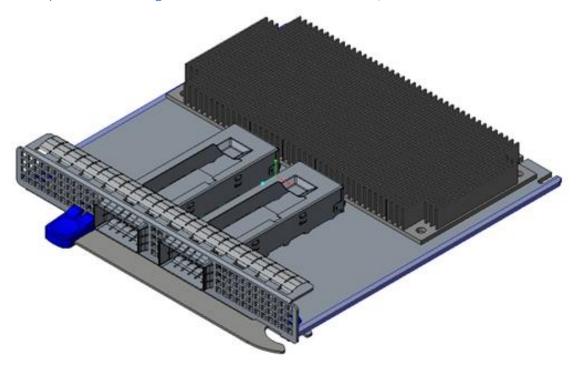


Figure 2: Representative Large OCP NIC 3.0 Card with Dual QSFP Ports and on-board DRAM



In order to achieve the features outlined in this specification, OCP 3.0 compliant cards are not backwards compatible to the 2.0 cards.

This specification is created under OCP Server workgroup – OCP NIC subgroup. An electronic copy of this specification can be found on the Open Compute Project website:

http://www.opencompute.org/wiki/Server/Mezz#Specifications_and_Designs

1.3 Acknowledgements

Placeholder

1.4 Overview

1.4.1 Mechanical Form factor overview

The OCP NIC 3.0 specification defines a third generation mechanical form factor that allows for interoperability between compliant baseboards and add-in cards.



OCP NIC 3.0 cards have two form factors – Small and Large. These cards are shown in Figure 3 below. The components shown in the figures are for illustrative purposes. The Small form factor card has one connector (Primary connector) on baseboard. The Large form factor card has two connectors (Primary Connector and Secondary Connector) on the baseboard. Both the Primary and Secondary connectors are defined in and compliant to SFF-TA-1002. [Editor's note: plan to submit change back to SFF-TA-1002]. On the NIC side, the card edge is implemented with gold fingers. The gold finger design follows SFF-TA-1002 as well.

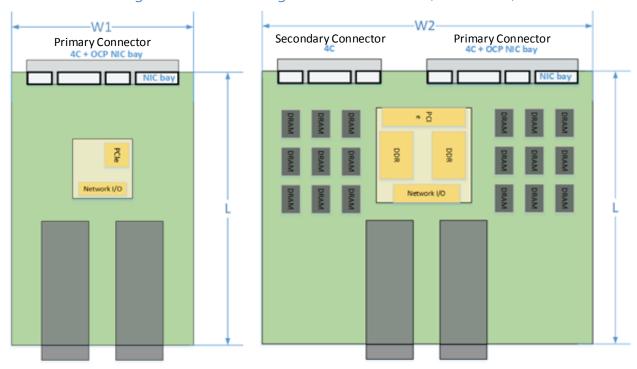


Figure 3: Small and Large Card Form-Factors (not to scale)

The two form factor dimensions are shown in Table 1.

Table 1: OCP 3.0 Form Factor Dimensions

Form	Width	Depth	Primary	Secondary	Typical Use Case
Factor			Connector	Connector	

Small	W1 = 76	L = 115	4C + OCP	N/A	Low profile and general NIC
	mm	mm	sideband		with a similar profile as an
			168 pins		OCP NIC 2.0 add-in card;
					up to x16 PCIe.
Large	W2 = 139	L = 115	4C + OCP	4C	Larger PCB width to
	mm	mm	sideband	140 pins	support feature rich NICs;
			168 pins		up to x32 PCIe.

The OCP NIC 3.0 design allows downward compatibility between the two card sizes. Table 2 shows the compatibility between the baseboard and NIC combinations. A small size baseboard slot may only accept a small sized NIC. A Large size baseboard slot may accept a small or large sized NIC.

Table 2: Baseboard to OCP NIC Form factor Compatibility Chart

Baseboard	NIC Size / Supported PCIe Width		
Slot Size	Small	Large	
Small	Up to x16	Not Supported	
Large	Up to x16	Up to x32	

There are two baseboard connector options available for system designers: straddle mount and right angle (RA). The straddle mount connector option allows the OCP NIC and baseboard to exist in a co-planer position. To achieve this, a cutout exists on the baseboard and is defined in this specification. Alternatively, the right angle option allows the OCP NIC to be installed on top of the baseboard. A baseboard cutout is not required for the right angle connector. The right angle option allows the baseboard to use this area for additional routing or backside component placement. The straddle mount and right angle connectors are shown in Section 3.2.

For both the baseboard and OCP card, this specification defines the component and routing keep out areas. Refer to Section 2.6 for details.

Both the straddle mount and right angle implementations shall accept the same OCP add-in card and shall be supported in the baseboard chassis regardless of the baseboard connector



selection (right angle or straddle mount) so long as the baseboard slot side and add-in card sizes are a supported combination as shown in Table 2.

This specification defines the form factor at the add-in card level, including the front panel, latching mechanism and card guide features [TBD; pending on the Mechanical work across stakeholders].

More details about the card form-factor is shown in Section 2.

1.4.2 Electrical overview

This specification defines the electrical interface between baseboard and the add-in card.

The electrical interface is implemented with a right angle or straddle mount connector on baseboard and gold finger on the add-in card. As previously noted in the mechanical overview, each card may implement a Primary Connector or Primary + Secondary Connector. Cards using only the Primary connector are suitable for both the Small and Large form-factors and may support up to x16 lanes of PCIe. The Secondary connector, when used in conjunction with the Primary connector, allows Large form-factor implementations and may support up to 32 lanes of PCIe.

1.4.2.1 Primary Connector

1.4.2.2 Secondary connector

1.5 References

- DMTF Standard. DSP0222, Network Controller Sideband Interface (NC-SI) Specification.
 Distributed Management Task Force, Inc, Rev 1.0.1, January 24th, 2013.
- EDSFF. *Enterprise and Datacenter SSD Form Factor Connector Specification*. Enterprise and Datacenter SSD Form Factor Working Group, Rev 0.9 (draft), August 2nd 2017.
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 April 4th, 2014.

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 http://www.opencompute.org/wiki/Server/Mezz
- PCIe Base Specification. PCI Express Base Specification, Revision 4.0 (draft).
- PCIe CEM Specification. PCI Express Card Electromechanical Specification, Revision 4.0 (draft).
- SMBus Management Interface Forum. *System Management Bus (SMBus) Specification.*System Management Interface Forum, Inc, Version 3.0, December 20th, 2014.
- SNIA. SFF-TA-1002, Specification for Protocol Agnostic Multi-Lane High Speed Connector. SNIA SFF TWG Technology Affiliate, Rev 0.0.9.1, September 9th, 2017.



2 Card Form Factor

2.1 Overview

2.2 Form Factor Options

OCP3.0 provides two fundamental form factor options: a small card (76mm \times 115mm) and a large card (139mm \times 115mm).

These form factors support a Primary Connector and optionally, a Secondary Connector. The Primary Connector is defined to be a SFF-TA-1002 compliant 4C connector plus a 28-pin bay for OCP 3.0 specific pins. The Secondary Connector is the 4C connector as defined in SFF-TA-1002. The 4C specification supports up to 32 differential pairs for a x16 PCIe connection per connector. For host platforms, the 28-pin OCP bay is required for the Primary connector. This is also mandatory for add-in cards.

The small card uses the 4C connector for up to a x16 PCIe interface. The small cards implement and additional 28-pin OCP bay for management functions and support for up to a four PCIe hosts. The small size card provides sufficient faceplate area to accommodate up to 2x QSFP modules, 4x SFP modules, or 4x RJ-45 for BASE-T operation. The small card form factor supports up to 79W of delivered power to the card edge.

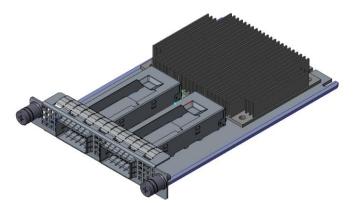


Figure 4: Example Small Card Form Factor

The large card uses provides the same functionality as the small card, but with support up to a x32 PCIe interface. The large card utilizes both the Primary and Secondary connectors. The large size card supports higher power envelopes and provides additional board area for more complex designs. The small card form factor supports up to 158W of delivered power to the card edge at 79W per connector.

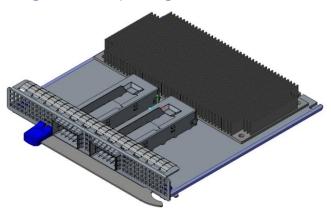


Figure 5: Example Large Card Form Factor

For both form-factors, an add-in card may optionally implement a subset of pins to support a x8 PCIe connection. This is implemented using a 2C card edge per SFF-TA-1002. The Primary Connector may support a 2C sized add-in card along with the 28 pin OCP bay. The following diagram from the SFF-TA-1002 specification illustrates the supported host Primary and Secondary Connectors and add-in card configurations.



Figure 6: Primary Connector (4C + OCP Bay) with 4C and 2C Add-in Cards

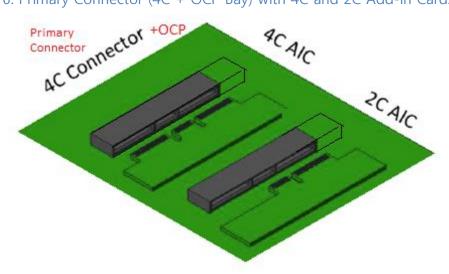


Table 3 summarizes the supported card form factors. Small form factors cards support the Primary Connector and up to 16 PCIe lanes. Large form factor cards support both the Primary and Secondary Connectors and up to 32 PCIe lanes.

Table 3: OCP NIC 3.0 Card Definitions

Add in Card Size and	Secondary Connector		Prir	nary Connector	
max PCIe Lane Count	4C Connector, x16 PCIe		4C Connect	or, x16 PCIe	OCP Bay
Small (x8)				2C	OCP Bay
Small (x16)			4C		OCP Bay
Large (x24)		2C	4C		OCP Bay
Large (x32)	4C		4C		OCP Bay

2.3 I/O bracket

TBD < need input from OCP mechanical groups>

2.4 Line Side I/O Implementations

At the time of this writing, the Small and Large form-factor cards may support the following standard line side I/O implementations:

Table 4: OCP 3.0 Line Side I/O Implementations

Form Factor	Max Topology Connector Count
Small	2x QSFP28
Small	4x SFP28
Small	4x RJ-45
Large	TBD
Large	TBD
Large	TBD

Additional combinations are permissible as I/O form-factor technologies and thermal capabilities evolve.

2.5 LED Implementations

LEDs must be implemented on the card Scan Chain (as defined in Section 3.5.3) for remote link/activity indication on the baseboard and may optionally be implemented on the OCP NIC 3.0 I/O bracket if there is sufficient space for local indication. These two cases are described below. In both cases, the actual link rate may be directly queried through the management interface.

2.5.1 Baseboard LEDs Configuration Over the Scan Chain

A small form-factor OCP NIC 3.0 with a fully populated I/O bracket (2x QSFP28, 4x SFP28, or 4x RJ-45) has insufficient space for discrete on-board (faceplate) LED indicators. In this case, the line side link and activity LED indicators are implemented on the baseboard system via the Scan Chain. The Scan Chain bit stream is defined in Section 3.5.3. This LED implementation is required for all add-in cards. The baseboard LED implementation uses two discrete LEDs (Link/Activity and Speed indication). Table 5 describes the baseboard LED configuration for baseboard implementations.



Table 5: Baseboard LED Configurations with Two Physical LEDs per Port

LED Pin	LED Color	Description
Link /	Green	Active low. Multifunction LED.
Activity		
		When lit and solid, this LED is used to indicate the link is up
		at the MAC level. Local and Remote Faults are clear and the
		link is ready for data transmission.
		When the LED is off, the physical link is down or disabled.
		The LED should blink low for 50-500 ms during Packet
		Activity.
		The Link/Activity LED shall be located on the left hand side for
		each port.
Speed	Green	Active low. Multifunction LED.
	Off	
		The LED is Green when the port is linked at its maximum
		speed.
		The LED is off when the device is linked at a speed lower than
		the highest capable speed, or no link is present.
		The bicolor speed LED shall be located on the right hand side
		for each port.

At the time of this writing, the Scan Chain definition allows for up to one link/activity and one speed LED per port. A total of up to 8 ports are supported in the Scan Chain. The bit stream defines the LEDs to be active low (ON). The Scan Chain LED implementation allows the NIC LED indicators to be remotely located on the OCP 3.0 compliant chassis (e.g. front LED indicators with rear I/O cards).

2.5.2 Add-in Card LED Configuration

For low I/O count small form-factor cards without built in light pipes (such as 1x QSFP28, 2x SFP28), or a large form-factor OCP 3.0 NIC, where additional I/O bracket area is available, the card may optionally implement on-board link/activity indications in addition to the Scan Chain LED stream. The recommended local (on-card) LED implementation uses two physical LEDs (a discrete Link/Activity LED and a bi-colored Speed A/Speed B LED). Table 6 describes the add-in card LED implementations.

Table 6: Add-in Card LED Configuration with Two Physical LEDs per Port

[T	<u> </u>
LED Pin	LED Color	Description
Link /	Green	Active low. Multifunction LED.
Activity		
		When lit and solid, this LED is used to indicate the link is up at
		the MAC level. Local and Remote Faults are clear and the link is
		ready for data transmission.
		Teacy for data transmission.
		When the LED is off, the physical link is down or disabled.
		When the LLD is on, the physical link is down or disabled.
		The LED should blink low for 50-500 ms during Packet Activity.
		The LLD should blink low for 30-300 his during racket Activity.
		The Link (Astrict of ED) shall be be eated on the left board side for
		The Link/Activity LED shall be located on the left hand side for
		each port.
Speed	Green	Active low. Bicolor multifunction LED.
	Amber	
	Off	The LED is Green when the port is linked at its maximum speed.
		The LED is Amber when the port is linked at it second highest
		speed.
		The LED is off when the device is linked at a speed lower than the
		second highest capable speed, or no link is present.
		The Amber Speed LED indicator may be used for port
		identification through vendor specific link diagnostic software.
		administration amough vendor specific link diagnostic software.

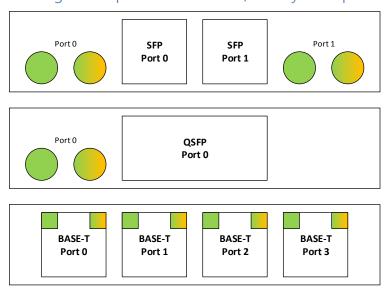


	The bicolor speed LED shall be located on the right hand side for
	each port.

2.5.3 LED Ordering

For all LED use cases, the green Link/Activity LED shall be located on the left side for each port. The bicolor green/amber speed A/B LED shall be located on the right side for each port. (Note Speed B is only available for local (on-card) LEDs. The placement of the LEDs may be to the side of the physical port for the case with add-in cards. The LED port association shall be clearly labeled on the add-in card and on the baseboard.

Figure 7: LED Ordering – Example Small Card Link/Activity and Speed LED Placement



2.6 Mechanical Keepout Zones

2.6.1 Baseboard Keep Out Zones

TBD – Need keepout drawings and envelopes for small / large size baseboard including primary/secondary/rail keepouts/cutout for straddle mount/keepout for right angle.

2.6.2 Add-in Card Keep Out Zones

TBD – need keepout drawings and envelopes for small / large size NIC including primary/secondary/rail keepouts.

2.7 Labeling Requirements

TBD

2.8 Insulation Requirements

All cards must implement a secondary side insulator to prevent the bottom side card components from shorting out to the chassis. The recommended insulator thickness is 0.25mm and must reside within the following mechanical envelope for the Small and Large size cards:

TBD < need 2D drawings >

2.9 NIC Implementation Examples

TBD

2.10 Non-NIC Use Cases

"PCIe interface with extra management sideband"

2.10.1 PCle Retimer card

2.10.2 Accelerator card

2.10.3 Storage HBA / RAID card

3 Card Edge and Baseboard Connector Interface

3.1 Gold Finger Requirement

The OCP NIC 3.0 add-in cards are compliant to the SFF-TA-1002 specification with respect to the gold fingers and connectors.

Small Size cards fit in the Primary Connector. Primary Connector compliant cards are 76mm x 115mm and may implement the full 168-pins. The Primary Connector cards may optionally implement a subset of gold finger pins if there is a reduced PCIe width requirement (such as 1 x8 and below). In this case, the card edge gold finger may implement a 2C design. The overall board thickness is 1.60mm. The gold finger dimensions for the Primary Connector compliant cards are shown below.

Large Size Cards support up to a x32 PCIe implementation and uses both the Primary and Secondary connectors.



For additional details, refer to the card and connector mechanical drawings located in XXX.

Note: The "B" pins on the connector are associated with the top side of the add-in card. The "A" pins on the connector are associated with the bottom side of the add-in card.

Figure 8: Small Size Primary Connector Gold Finger Mating Card Dimensions – x16 – Top Side

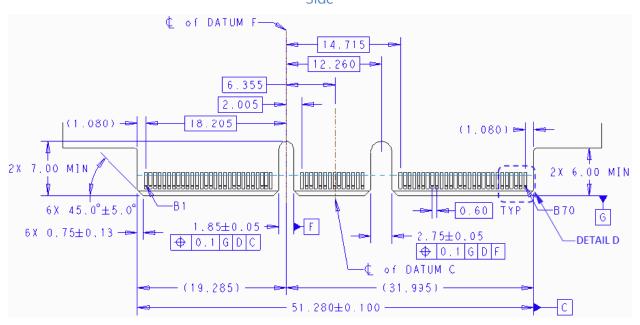


Figure 9: Small Size Primary Connector Gold Finger Mating Card Dimensions – x16 – Bottom

Side

TBD

Figure 10: Large Size Card Gold Finger Mating Card Dimensions – x32 – Top Side

TBD

Figure 11: Large Size Card Gold Finger Mating Card Dimensions – x32 – Bottom Side

TBD

3.1.1 Gold Finger Mating Sequence

Per the SFF-TA-1002 specification, the Primary and Secondary connectors are protocol agnostic and are optimized for high speed differential pairs. For use in the OCP NIC 3.0 application, some pin locations are used for single ended control nets or power and would benefit from a shorter pin length for staggering. As such, the recommended add-in card gold finger staging is shown in Table 7 for a two stage, first-mate, last-break functionality. The host connectors have a single stage mating and do not implement different pin lengths.

The AIC Plug (Free) side refers to the add-in card gold fingers; the receptacle (Fixed) side refers to the physical connector on the host platform. This table is based on the SFF-TA-1002 Table A-1 with modifications for OCP NIC 3.0. Refer to the mechanical drawings for pin the first-mate and second-mate lengths.

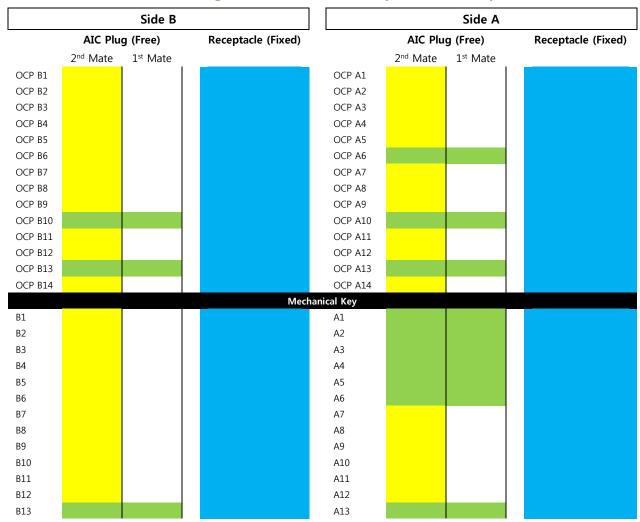
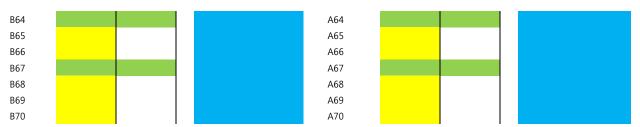


Table 7: Contact Mating Positions for the Primary and Secondary Connectors



14						
816 A16 A16 B17 A17 B18 A18 A18 B19 A19 B20 A20 A20 B21 A21 B22 A22 B23 A23 A25 B26 A26 B27 A27 A27 B28 A28 B29 A29 B30 A30 B31 A31 A31 B32 A32 A32 B33 A33 A33 B34 A34 A34 B35 A35 B36 A36 A36 B37 A37 A37 B38 A38 B39 A39 A39 B40 A40 A41 A41 B42 A42 A44 A44 B44 A44 A44 B44 A44 A44 B44 A44 A44 B44 A44 A44	B14			A14		
B16 A16 A17 A17 B18 A18 A18 A19 B20 A20 A20 A21 B22 A22 A22 A23 A23 A23 A25 A26 B27 A27 A27 B28 A28 A28 A28 A28 A28 A28 A28 A28 A31 A31 A31 A31 A32 A33 A33 A33 A34 A34 A34 A34 A34 A35 A35 A35 A35 A36 A36 A37 A37 A38 A38 A39 A40 A41 A44 A44	B15			A15		
817						
818						
B19						
820						
Page						
822						
823 A23 824 A24 825 A26 866 A26 827 A28 Mechanical Key 829 A28 830 A30 831 A31 832 A32 833 A33 834 A34 835 A35 836 A36 837 A37 838 A33 840 A44 841 A41 842 A39 837 A37 838 A38 840 A40 841 A41 842 A43 843 A44 844 A44 845 A43 846 A44 847 A47 848 A44 849 A46 840 A48 841 A47 842 A47 843 A48 844 <						
B24 A24 A25 B26 A26 A27 B27 A27 B28 Mechanical Key B29 A29 B30 A30 A31 B31 A31 A31 B32 A32 B33 B33 A33 A34 B35 A36 A36 B36 A36 A36 B37 A37 A37 B38 A38 A38 B39 A39 A39 B40 A40 A41 B41 A41 A42 B42 A42 A42 Mechanical Key B43 A43 A44 B44 A44 A45 B45 A46 A46 B47 A47 A47 B48 A48 A48 B49 A49 A54 B50 A50 A50 B51 A51 A52 B53 A53 A53 B54						
825 A25 826 A26 B27 A27 B28 A28 Mechanical Key B30 B31 A30 B31 A31 B32 A32 B33 A33 B34 A34 B35 A35 B36 A36 B37 A37 B38 A38 B39 A39 B40 A40 B41 A41 B42 A42 Mechanical Key **The Color of the						
B26						
B27						
B29						
Mechanical Key						
B29 A29 B30 A30 B31 A31 B32 A32 B33 A33 B34 A34 B35 A35 B36 A36 B37 A37 B38 A38 B39 A39 B40 A40 B41 A41 B42 A42 **Mechanical Key* *	DZO		Mod			
B30 A30 B31 A31 B32 A32 B33 A33 B34 A34 B35 A35 B36 A36 B37 A37 B38 A39 B40 A40 B41 A41 B42 A2 B43 A43 B44 A44 B45 A45 B46 A46 B47 A47 B48 A48 B49 A49 B50 A50 B51 A51 B52 A52 B53 A53 B54 A54 B55 A55 B66 A56 B57 A57 B58 A58 B59 A59 B60 A60 B61 A61 B62 A62	P20		ivieci			
831 A31 832 A32 834 A34 835 A35 836 A36 837 A37 838 A38 839 A39 841 A41 842 A42 **PRODUCT OF THE PRODUCT OF THE P						
832 A32 833 A33 834 A34 835 A35 836 A36 837 A37 838 A38 839 A39 840 A40 841 A41 842 A42 **Mechanical Key*						
833 A34 834 A34 835 A35 836 A36 837 A37 838 A39 840 A40 841 A41 842 A42 **Mechanical Key*						
834 A34 835 A35 836 A36 837 A37 838 A38 839 A39 B41 A41 842 A42 Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Mechanical Key Me						
B35 A35 B36 A36 B37 A37 B38 A38 B39 A39 B40 A40 B41 A41 B42 A42 **Methanical Key*						
836 A36 837 A37 838 A38 839 A39 840 A40 841 A41 842 Mechanical Key Mechanical Key Mechanical Key 844 A43 845 A43 846 A44 847 A47 848 A48 849 A49 850 A50 851 A51 852 A52 853 A53 854 A54 855 A55 856 A56 857 A57 858 A58 859 A59 860 A60 861 A61 862 A62						
837 A37 838 A38 840 A40 841 A41 842 A42 **Mechanical Key*						
838 A38 A39 840 A40 A41 841 A41 A42 Wechanical Key 843 A43 A44 844 A44 A44 845 A45 A46 847 A47 A47 848 A48 A49 850 A50 A51 852 A52 A52 853 A53 A54 855 A54 A54 855 A55 A56 857 A57 A58 859 A59 A60 861 A61 A61 A62						
839 A39 841 A41 842 A42 Mechanical Key 843 A43 844 A44 855 A45 846 A46 847 A47 848 A48 849 A49 850 A50 851 A51 852 A52 853 A53 854 A54 855 A55 856 A56 857 A57 858 A58 859 A60 861 A61 862 A62						
B40 A40 B41 A41 B42 A42 Mechanical Key B43 A43 B44 A44 B45 A45 B46 A46 B47 A47 B48 A48 B49 A49 B50 A50 B51 A51 B52 A52 B53 A53 B54 A54 B55 A55 B66 A56 B57 A57 B58 A58 B69 A59 B60 A60 B61 A61 B62 A62						
B41 A41 A42 Mechanical Key B43 A43 A44 B44 A44 A45 B45 A46 A46 B47 A47 A48 B48 A48 A49 B50 A50 A51 B51 A52 A52 B53 A53 A54 B54 A54 A54 B55 A55 A56 B57 A57 A58 B59 A59 A60 B61 A60 A61 B62 A62 A62						
B42 Mechanical Key B43 A43 B44 A44 B45 A45 B46 A46 B47 A47 B48 A48 B49 A49 B50 A50 B51 A51 B52 A52 B53 A53 B54 A54 B55 A55 B56 A56 B57 A57 B58 A59 B60 A60 B61 A61 B62 A62						
Mechanical Key B43 A43 B44 A44 B45 A45 B46 A46 B47 A47 B48 A48 B49 A49 B50 A50 B51 A51 B52 A52 B53 A53 B54 A54 B55 A55 B56 A56 B57 A58 B58 A59 B60 A60 B61 A61 B62 A62						
B43 A43 B44 A44 B45 A45 B46 A46 B47 A47 B48 A48 B49 A49 B50 A50 B51 A51 B52 A52 B53 A53 B54 A54 B55 A55 B56 A56 B57 A57 B58 A59 B60 A60 B61 A61 B62 A62	B42		Mod			
B44 A44 A45 B46 A46 A47 B48 A48 A49 B50 A50 A51 B51 A51 A52 B53 A53 A53 B54 A54 A54 B55 A55 A56 B57 A57 A58 B59 A59 A60 B61 A61 A62	D42		IVIECI			
845 A45 A46 847 A47 A48 848 A48 A49 850 A50 A51 851 A51 A52 853 A53 A53 854 A54 A54 855 A55 A55 856 A56 A57 858 A59 A59 860 A60 A61 862 A62 A62						
B46 A46 B47 A47 B48 A48 B49 A49 B50 A50 B51 A51 B52 A52 B53 A53 B54 A54 B55 A55 B56 A56 B57 A57 B58 A59 B60 A60 B61 A61 B62 A62						
B47 A47 B48 A48 B49 A49 B50 A50 B51 A51 B52 A52 B53 A53 B54 A54 B55 A55 B66 A56 B57 A57 B58 A59 B60 A60 B61 A61 B62 A62						
B48 A48 B49 A49 B50 A50 B51 A51 B52 A52 B53 A53 B54 A54 B55 A55 B66 A56 B57 A57 B58 A59 B60 A60 B61 A61 B62 A62						
B49 A49 B50 A50 B51 A51 B52 A52 B53 A53 B54 A54 B55 A55 B56 A56 B57 A57 B58 A59 B60 A60 B61 A61 B62 A62						
B50 A50 B51 A51 B52 A52 B53 A53 B54 A54 B55 A55 B56 A56 B57 A57 B58 A59 B60 A60 B61 A61 B62 A62						
B51 A51 B52 A52 B53 A53 B54 A54 B55 A55 B56 A57 B57 A57 B58 A58 B59 A60 B60 A61 B62 A62						
B52 A52 B53 A53 B54 A54 B55 A55 B56 A56 B57 A57 B58 A58 B59 A59 B60 A60 B61 A61 B62 A62						
B53 A53 B54 A54 B55 A55 B56 A56 B57 A57 B58 A58 B59 A59 B60 A60 B61 A61 B62 A62						
B54 A54 B55 A55 B56 A56 B57 A57 B58 A58 B59 A59 B60 A60 B61 A61 B62 A62						
B55 A55 B56 A56 B57 A57 B58 A58 B59 A59 B60 A60 B61 A61 B62 A62						
B56 A56 B57 A57 B58 A58 B59 A59 B60 A60 B61 A61 B62 A62						
B57 A57 B58 A58 B59 A59 B60 A60 B61 A61 B62 A62						
B58 A58 B59 A59 B60 A60 B61 A61 B62 A62						
B59 B60 B61 B62 A59 A60 A61 A62						
B60						
B61						
B62 A62						
B63 A63						
	B63			A63		

Rev0.01



3.2 Baseboard Connector Requirement

The OCP NIC 3.0 connectors are compliant to the "4C connector" as defined in the SFF-TA-1002 specification for a right angle or straddle mount form-factor. The 4C connector is 140-pins in width and includes support for up to 32 differential pairs to support a x16 PCIe connection. The connector also provides 6 pins of 12V for payload power. This implementation is common between both the Primary and Secondary Connectors. In addition, the Primary Connector has a 28-pin OCP Bay to the right of pin 1. These pins are used for management and support for up to a 4 x4 multi-host configuration on the Primary Connector. The Primary and Secondary Connector drawings are shown in Figure 12, Figure 13, Figure 14 and Figure 15 below.

Figure 12: 168-pin Base Board Primary Connector – Right Angle

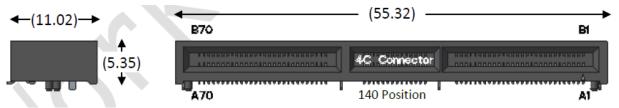


Figure 13: 140-pin Base Board Secondary Connector – Right Angle

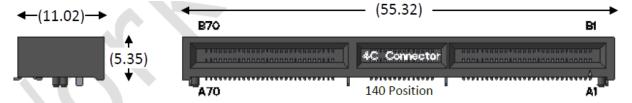


Figure 14: 168-pin Base Board Primary Connector – Straddle Mount

<mark>TBD</mark>

Figure 15: 140-pin Base Board Secondary Connector – Straddle Mount

<mark>TBD</mark>



In order to the support the large form factor, systems must locate the Primary and Secondary Connectors per the mechanical drawing shown in Figure 16.

Figure 16: Primary and Secondary Connector Locations for Large Card Support

<mark>TBD</mark>

3.3 Pin definition

The pin definitions of an OCP NIC 3.0 card with up to a x32 PCIe interface are shown in Table 8 and Table 9. All signal directions are shown from the perspective of the baseboard.

A baseboard system may provide a combination of Primary Connectors only, or Primary and Secondary Connectors to support multiple sizes of add-in cards. Both connectors share common functionality with power, SMBus, x16 PCIe Gen4 and bifurcation control. The Primary Connector has an additional OCP Bay (pins OCP_A[1:14], OCP_B[1:14]) with additional REFCLKs for supporting up to four PCIe hosts, NC-SI connectivity and a Scan Chain for information exchange between the host and card. The NIC is required to implement the Scan Chain, while the baseboard may choose to optionally implement it. Depending on the baseboard form-factor, multiple OCP NIC 3.0 compliant cards may be designed into the system.

The pins common to the Primary and Secondary Connectors are shown in Section 3.4. The OCP Bay pins on the Primary Connector only are shown in Section 3.5.

Cards or systems that do not require the use of a PCIe x16 connection may optionally implement a subset electrical connections as applicable to the design. For example, a x8 (or smaller) card using the first 8 PCIe lanes that is compliant with the Primary Connector pinout. Refer to Sections 3.1 and 3.2 for mechanical details. For these cases, the Primary Connector matches the 2C dimensions as defined in SFF-TA-1002.

In all cases, the physical baseboard connectors shall support x16 PCIe widths and must be implemented with the Primary (4C + OCP Bay) and Secondary (4C) connectors.

	Side B	Side A			
OCP_B1	NIC_PWR_GOOD	WAKE_N	OCP_A1	Pr	Pr
OCP_B2	PWRBRK#	PERST2#	OCP_A2	ima	ima
OCP_B3	LD#	PERST3#	OCP_A3	ŊΟ	ŊΟ
OCP_B4	DATA_IN	RBT_ARB_IN	OCP_A4	onn	onn
OCP_B5	DATA_OUT	RBT_ARB_OUT	OCP_A5	ecto	ecto
OCP_B6	CLK	GND	OCP_A6	or (x	or (x
OCP_B7	SLOT_ID0	RBT_TX_EN	OCP_A7	:16,	(8, 1
OCP_B8	RBT_RXD1	RBT_TXD1	OCP_A8	168	.12-
OCP_B9	RBT_RXD0	RBT_TXD0	OCP_A9	<u>p</u> .	pin
OCP_B10	GND	GND	OCP_A10	ı ad	add
OCP_B11	REFCLKn2	REFCLKn3	OCP_A11	d-in	-in
OCP_B12	REFCLKp2	REFCLKp3	OCP_A12	car	card
OCP_B13	GND	GND	OCP_A13	<u>o</u> . ≶	Wit
OCP_B14	RBT_CRS_DV	RBT_CLK_IN	OCP_A14	Primary Connector (x16, 168-pin add-in card with OCP	Primary Connector (x8, 112-pin add-in card with OCP bay)
	Mechan	ical Key		O Q	Ĝ.
B1	+12V/+12V_AUX	GND	A1	Вау)	bау)
B2	+12V/+12V_AUX	GND	A2	S	
В3	+12V/+12V_AUX	GND	A3		
B4	+12V/+12V_AUX	GND	A4		
B5	+12V/+12V_AUX	GND	A5		
В6	+12V/+12V_AUX	GND	A6		
В7	BIFO#	SMCLK	A7		
B8	BIF1#	SMDAT	A8		
В9	BIF2#	SMRST#	A9		
B10	PERST0#	PRSNTA#	A10		
B11	+3.3V/+3.3V_AUX	PERST1#	A11		
B12	PWRDIS	PRSNTB2#	A12		
B13	GND	GND	A13		
B14	REFCLKn0	REFCLKn1	A14		
B15	REFCLKp0	REFCLKp1	A15		
B16	GND	GND	A16		
B17	PETn0	PERn0	A17		
B18	PETp0	PERp0	A18		
B19	GND	GND	A19		
B20	PETn1	PERn1	A20		
B21	PETp1	PERp1	A21		
B22	GND	GND	A22		
B23	PETn2	PERn2	A23		



B24	PETp2	PERp2	A24	
B25	GND	GND	A25	
B26	PETn3	PERn3	A26	
B27	РЕТр3	PERp3	A27	
B28	GND	GND	A28	
	Mechan	ical Key		
B29	GND	GND	A29	
B30	PETn4	PERn4	A30	
B31	PETp4	PERp4	A31	
B32	GND	GND	A32	
B33	PETn5	PERn5	A33	
B34	PETp5	PERp5	A34	
B35	GND	GND	A35	
B36	PETn6	PERn6	A36	
B37	PETp6	PERp6	A37	
B38	GND	GND	A38	
B39	PETn7	PERn7	A39	
B40	PETp7	PERp7	A40	
B41	GND	GND	A41	
B42	PRSNTB0#	PRSNTB1#	A42	
	Mechan	ical Key		
B43	GND	GND	A43	
B44	PETn8	PERn8	A44	
B45	PETp8	PERp8	A45	
B46	GND	GND	A46	
B47	PETn9	PERn9	A47	
B48	PETp9	PERp9	A48	
B49	GND	GND	A49	
B50	PETn10	PERn10	A50	
B51	PETp10	PERp10	A51	
B52	GND	GND	A52	
B53	PETn11	PERn11	A53	
B54	PETp11	PERp11	A54	
B55	GND	GND	A55	
B56	PETn12	PERn12	A56	
B57	PETp12	PERp12	A57	
B58	GND	GND	A58	
B59	PETn13	PERn13	A59	

Rev0.01

B61	GND	GND	A61	
B62	PETn14	PERn14	A62	
B63	PETp14	PERp14	A63	
B64	GND	GND	A64	
B65	PETn15	PERn15	A65	
B66	PETp15	PERp15	A66	
B67	GND	GND	A67	
B68	RFU, N/C	RFU, N/C	A68	
B69	RFU, N/C	RFU, N/C	A69	
B70	PRSNTB3#	RFU, N/C	A70	



Table 9: Secondary Connector Pin Definition (x16) (4C)

	Side B	Side A			
B1	+12V/+12V_AUX	GND	A1	Se	Se
B2	+12V/+12V_AUX	GND	A2	con	con
В3	+12V/+12V_AUX	GND	A3	dan	dan
B4	+12V/+12V_AUX	GND	A4	y Cc	y Cc
B5	+12V/+12V_AUX	GND	A5	onne	onn€
В6	+12V/+12V_AUX	GND	A6	Secondary Connector (x16, 140-pin add-in card)	Secondary Connector (x8, 84-pin add-in card)
В7	BIFO#	SMCLK	A7	2	r (x
B8	BIF1#	SMDAT	A8	.6, 1	3, 84
В9	BIF2#	SMRST#	A9	140-	- pi
B10	PERSTO#	PRSNTA#	A10	pin	1 ad
B11	+3.3V/+3.3V_AUX	PERST1#	A11	add	d-in
B12	PWRDIS	PRSNTB2#	A12	₽.	ca
B13	GND	GND	A13	card	<u>a</u>
B14	REFCLKn0	REFCLKn1	A14		
B15	REFCLKp0	REFCLKp1	A15		
B16	GND	GND	A16		
B17	PETn0	PERn0	A17		
B18	PETp0	PERp0	A18		
B19	GND	GND	A19		
B20	PETn1	PERn1	A20		
B21	PETp1	PERp1	A21		
B22	GND	GND	A22		
B23	PETn2	PERn2	A23		
B24	PETp2	PERp2	A24		
B25	GND	GND	A25		
B26	PETn3	PERn3	A26		
B27	PETp3	PERp3	A27		
B28	GND	GND	A28		
	Mechan	nical Key			
B29	GND	GND	A29	-	
B30	PETn4	PERn4	A30		
B31	PETp4	PERp4	A31		
B32	GND	GND	A32		
B33	PETn5	PERn5	A33		
B34	PETp5	PERp5	A34		
B35	GND	GND	A35		
B36	PETn6	PERn6	A36		

Rev0.01

B37	РЕТр6	PERp6	A37	
B38	GND	GND	A38	
B39	PETn7	PERn7	A39	
B40	РЕТр7	PERp7	A40	
B41	GND	GND	A41	
B42	PRSNTB0#	PRSNTB1#	A42	
	Mechan	ical Key		
B43	GND	GND	A43	
B44	PETn8	PERn8	A44	
B45	PETp8	PERp8	A45	
B46	GND	GND	A46	
B47	PETn9	PERn9	A47	
B48	РЕТр9	PERp9	A48	
B49	GND	GND	A49	
B50	PETn10	PERn10	A50	
B51	PETp10	PERp10	A51	
B52	GND	GND	A52	
B53	PETn11	PERn11	A53	
B54	PETp11	PERp11	A54	
B55	GND	GND	A55	
B56	PETn12	PERn12	A56	
B57	PETp12	PERp12	A57	
B58	GND	GND	A58	
B59	PETn13	PERn13	A59	
B60	PETp13	PERp13	A60	
B61	GND	GND	A61	
B62	PETn14	PERn14	A62	
B63	PETp14	PERp14	A63	
B64	GND	GND	A64	
B65	PETn15	PERn15	A65	
B66	PETp15	PERp15	A66	
B67	GND	GND	A67	
B68	RFU, N/C	RFU, N/C	A68	
B69	RFU, N/C	RFU, N/C	A69	
B70	PRSNTB3#	RFU, N/C	A70	



3.4 Signal Descriptions – Common

The pins shown in this section are common to both the Primary and Secondary Connectors. All pin directions are from the perspective of the baseboard.

The add-in card shall implement protection methods to prevent leakage paths between the Vaux and Vmain power domains in the event that a NIC is powered down in a powered up baseboard.

Note: Pins that are only used on Primary Connector 28-pin OCP bay are defined in Section 3.5.

3.4.1 PCle Interface Pins

This section provides the pin assignments for the PCIe interface signals. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0. Example connection diagrams for are shown in Figure 28.

Table 10: Pin Descriptions - PCIe 1

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
REFCLKn0	B14	Output	PCIe compliant differential reference clock #0,
REFCLKp0	B15		and #1. 100MHz reference clocks are used for
REFCLKn1	A14	Output	the add-in card PCIe core logic.
REFCLKp1	A15		
			For baseboards, the REFCLK0 and REFCLK1
			signals are required at the connector.
			For add-in cards, the required REFCLKs shall be
			connected per the endpoint datasheet.
			Note: For cards that only support 1 x16,
			REFCLK0 is used. For cards that support 2 x8,
			REFCLK0 is used for the first eight PCIe lanes,

			and REFCLK1 is used for the second eight PCIe lanes.
			Refer to Section 2.1 in the PCIe CEM
			Specification, Rev 4.0 for electrical details.
PETn0	B17	Output	Transmitter differential pairs [0:15]. These pins
РЕТр0	B18		are connected from the baseboard transmitter
PETn1	B20	Output	differential pairs to the receiver differential
PETp1	B21		pairs on the add-in card.
PETn2	B23	Output	
PETp2	B24		The PCIe transmit pins are AC coupled on the
PETn3	B26	Output	baseboard with capacitors and are placed next
PETp3	B27		to the baseboard transmitters. The AC coupling
PETn4	B30	Output	capacitor must be between 176nF (min) and
PETp4	B31		265nF (max).
PETn5	B33	Output	
PETp5	B34		For baseboards, the PET[0:15] signals are
PETn6	B36	Output	required at the connector.
РЕТр6	B37		
PETn7	B39	Output	For add-in cards, the required PET[0:15] signals
РЕТр7	B40		shall be connected to the endpoint silicon. For
PETn8	B44	Output	silicon that uses less than a x16 connection, the
PETp8	B45		appropriate PET[0:15] signals shall be
PETn9	B47	Output	connected per the endpoint datasheet.
РЕТр9	B48		
PETn10	B50	Output	Refer to Section 6.1 in the PCIe CEM
PETp10	B51		Specification, Rev 4.0 for details.
PETn11	B53	Output	
PETp11	B54		
PETn12	B56	Output	
PETp12	B57		
PETn13	B59	Output	
PETp13	B60		



PETn14	B62	Output	
PETp14	B63		
PETn15	B65	Output	
PETp15	B66		
PERn0	A17	Input	Receiver differential pairs [0:15]. These pins are
PERp0	A18		connected from the add-in card transmitter
PERn1	A20	Input	differential pairs to the receiver differential
PERp1	A21		pairs on the baseboard.
PERn2	A23	Input	
PERp2	A24		The PCIe receive pins are AC coupled on the
PERn3	A26	Input	add-in card with capacitors and are placed next
PERp3	A27		to the add-in card transmitters. The AC
PERn4	A30	Input	coupling capacitor must be between 176nF
PERp4	A31		(min) and 265nF (max).
PERn5	A33	Input	
PERp5	A34		For baseboards, the PER[0:15] signals are
PERn6	A36	Input	required at the connector.
PERp6	A37		
PERn7	A39	Input	For add-in cards, the required PER[0:15] signals
PERp7	A40		shall be connected to the endpoint silicon. For
PERn8	A44	Input	silicon that uses less than a x16 connection, the
PERp8	A45		appropriate PER[0:15] signals shall be
PERn9	A47	Input	connected per the endpoint datasheet.
PERp9	A48		
PERn10	A50	Input	Refer to Section 6.1 in the PCIe CEM
PERp10	A51		Specification, Rev 4.0 for details.
PERn11	A53	Input	
PERp11	A54		
PERn12	A56	Input	
PERp12	A57		
PERn13	A59	Input	
PERp13	A60		

PERn14	A62	Input	
PERp14	A63		
PERn15	A65	Input	
PERp15	A66		
PERSTO#	B10	Output	PCIe Reset #0, #1. Active low.
PERST1#	A11		
			Indicates when the applied power is within
			tolerance and stable for the add-in card.
			PERST# goes high at least 100ms after the
			power rails are within operating limits per the
			PCIe CEM Specification. The PCIe REFCLKs also
			become stable within this period of time.
			PERST is pulled high on the baseboard.
			For OCP NIC 3.0, PERST deassertion also
			indicates the full card power envelope is
			available to the add-in card.
			For baseboards, the PERST[0:1]# signals are
			required at the connector.
			For add-in cards, the required PERST[0:1]#
			signals shall be connected to the endpoint
			silicon.
			Note: For cards that only support 1 x16,
			PERSTO# is used. For cards that support 2 x8,
			PERSTO# is used for the first eight PCIe lanes,
			and PERST1# is used for the second eight PCIe
			lanes.
			Refer to Section 2.2 in the PCIe CEM
			Specification, Rev 4.0 for details.



3.4.2 PCIe Present and Bifurcation Control Pins

This section provides the pin assignments for the PCIe present and bifurcation control signals. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure 17.

The PRSNTA#/PRSNTB[0:3]# state may be used to determine if a card has been physically plugged in. The BIF[0:2]# pins much be latched at least 1 ms before PWRDIS deassertion to ensure the correct values are detected by the system. Changing the pin states after this timing window is not allowed. Refer to the AC timing diagram in Section XXX for details.

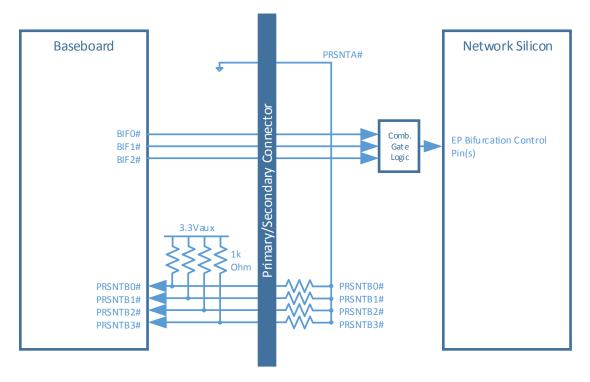
Table 11: Pin Descriptions – PCIe Present and Bifurcation Control Pins

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
PRSNTA#	A12	Output	Present A is used for add-in card presence and
			PCIe capabilities detection.
			For baseboards, this pin is directly connected
			to GND.
			For add-in cards, this pin is connected to the
			PRSNTB[3:0]# pins.
PRSNTB0#	B42	Input	Present B [0:3]# are used for add-in card
PRSNTB1#	A42		presence and PCIe capabilities detection.
PRSNTB2#	A10		
PRSNTB3#	B70		For baseboards, these pins are connected to
			the I/O hub and are pulled up to +3.3Vaux
			using 1kOhm resistors.
			For add-in cards, these pins are strapped to
			PRSNTA#. The encoding definitions are
			described in Section 3.6.

			PRSNTB3# is located at the bottom of the 4C connector and is only applicable for add-in cards with a PCIe width of x16 (or greater). Add-in cards that implement a 2C card edge do not use the PRSNTB3# pin for capabilities or present detection.
BIFO#	A7	Output	Bifurcation [0:2]# pins allow the baseboard to
BIF1#	A8		force configure the add-in card bifurcation.
BIF2#	A9		
			For baseboards, these pins are outputs driven from the baseboard I/O hub and allows the system to force configure the add-in card bifurcation. The baseboard may optionally tie the BIF[0:2]# signals to 3.3Vaux or to ground if no dynamic bifurcation configuration is required.
			For add-in cards, these signals connect to the endpoint bifurcation pins if it is supported.
			The BIF[0:2]# encoding definitions are described in Section 3.6.
			Note: the required combinatorial logic output for endpoint bifurcation is dependent on the specific silicon and is not defined in this specification.

Figure 17: PCIe Present and Bifurcation Control Pins





3.4.3 SMBus Interface Pins

This section provides the pin assignments for the SMBus interface signals. The AC/DC specifications are defined in the SMBus and I²C bus specifications. An example connection diagram is shown in Figure XXX.

Table 12: Pin Descriptions – SMBus

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
SMCLK	A7	Output,	SMBus clock. Open drain, pulled up to 3.3Vaux
		OD	on the baseboard.
			For baseboards, connect the SMCLK from the
			platform SMBus master to the connector.
			For add-in cards, connect the SMCLK from the
			endpoint silicon to the card edge gold fingers.

SMDAT	A8	Input /	SMBus Data. Open drain, pulled up to 3.3Vaux
		Output,	on the baseboard.
		OD	
			For baseboards, connect the SMDAT from the
			platform SMBus master to the connector.
			For add-in cards, connect the SMDAT from the
			endpoint silicon to the card edge gold fingers.
SMRST#	A9	Output,	SMBus reset. Open drain.
		OD	
			For baseboards, this pin is pulled up to
			3.3Vauxand is used to reset optional
			downstream SMBus devices (such as
			temperature sensors). SMRST# is a mandatory
			signal for baseboard implementations.
			For add-in cards, SMRST# is optional.

3.4.4 Power Supply Pins

This section provides the pin assignments for the power supply interface signals. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0 and amended in Section 3.10. An example connection diagram is shown in Figure 18.

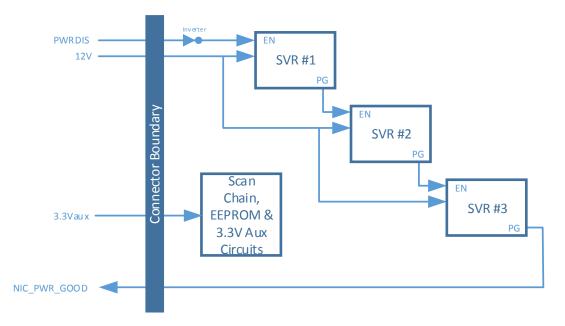
Table 13: Pin Descriptions – Power

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
GND	Various	GND	Ground return; a total of 46 ground pins are
			on the main 140-pin connector area.
+12V/+12V_AUX	B1, B2,	Power	12V main or 12V Aux power; total of 6 pins per
	B3, B4,		connector. The 12V pins are rated to 1.1A per
	B5, B6		pin with a maximum derated power delivery of
			79.2W.



_			·
			The +12V power pins must be within the rail
			tolerances (TBD tolerance for Aux) when the
			PWRDIS pin is driven low by the baseboard.
+3.3V/3.3V_AUX	B11	Power	3.3V main or 3.3V Aux power; total of 1 pin per
			connector. The 3.3V pin is rated to 1.1A for a
			maximum derated power delivery of 3.63W.
			The 3.3Vaux/main power pin must be within
			the rail tolerances when the PWRDIS pin is
			driven low by the baseboard.
PWRDIS	B12	Output,	Power disable. Active high. Open-drain
		O/D	
			This signal is pulled up to 3.3V through a
			10kOhm resistor on the baseboard.
			When high, all add-in card supplies are
			disabled.
			When low, add-in card supplies are enabled.

Figure 18: Example Power Supply Topology



3.4.5 Miscellaneous Pins

This section provides the pin assignments for the miscellaneous interface signals.

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
RFU, N/C	B68,	Input /	Reserved future use pins. Leave these pins as
	В69,	Output	no connect.
	A68,		
	A69,		
	A70		

Table 14: Pin Descriptions – Miscellaneous 1

3.5 Signal Descriptions – OCP Bay (Primary Connector)

The following section describes the functions in the Primary Connector 28-pin OCP bay. This 28-pin bay is shown in Section 3.3 and have pin numbers designated as OCP_B[1:14], and OCP_A[1:14]. All pin directions on this OCP bay are from the perspective of the baseboard.

The add-in card shall implement protection methods to prevent leakage paths between the Vaux and Vmain power domains in the event that a NIC is powered down in a powered up baseboard.



Note: The pins that are common to both the Primary and Secondary Connectors are defined in Section 3.4.

3.5.1 PCIe Interface Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the PCIe interface signals on the Primary Connector OCP bay. The AC/DC specifications are defined in Section XXX. An example connection diagram that shows REFCLK2, REFCLK3, PERST2# and PERST3# is shown in Section 3.7.

Table 15: Pin Descriptions – PCIe 2

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
REFCLKn2	OCP_B11	Output	PCIe compliant differential reference clock #2,
REFCLKp2	OCP_B12		and #3. 100MHz reference clocks are used for
REFCLKn3	OCP_A11	Output	the add-in card PCIe core logic.
REFCLKp3	OCP_A12		
			For baseboards, the REFCLK2 and REFCLK3
			signals are required at the Primary connector.
			For add-in cards, the required REFCLKs shall be
			connected per the endpoint datasheet.
			Note: REFCLK2 and REFCLK3 are not used for
			cards that only support a 1 x16 or 2 x8
			connection.
			Refer to Section 2.1 in the PCIe CEM
			Specification, Rev 4.0 for details.
PERST2#	OCP_A2	Output	PCIe Reset #2, #3. Active low.
PERST3#	OCP_A3		
			Indicates when the applied power is within
			tolerance and stable for the add-in card.

		,	This signal is driven by the add-in card to notify the baseboard restore the PCIe link. For add-in cards that support multiple WAKE# signals, their respective WAKE# pins may be tied together as the signal is open-drain to form a wired-OR.
WAKE#	OCP_A1	Input, OD	cards that only support a 1 x16 or 2 x8 connection. Refer to Section 2.2 in the PCIe CEM Specification, Rev 4.0 for details. WAKE#. Open drain. Active low.
			For add-in cards, the required PERST[0:1]# signals shall be connected to the endpoint silicon. Note: PERST2# and PERST3# are not used for
			For baseboards, the PERST[0:1]# signals are required at the connector.
			For OCP NIC 3.0, PERST deassertion also indicates the full card power envelope is available to the add-in card.
			PERST# goes high at least 100ms after the power rails are within operating limits per the PCIe CEM Specification. The PCIe REFCLKs also become stable within this period of time. PERST is pulled high on the baseboard.



For baseboards, this signal is pulled up to +3.3V on the baseboard with a 10kOhm resistor and is connected to the system WAKE# signal.
For add-in cards, this signal is connected directly to the endpoint silicon WAKE# pin(s).
Refer to Section 2.3 in the PCIe CEM Specification, Rev 4.0 for details.

3.5.2 NC-SI Over RBT Interface Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the NC-SI over RBT interface signals on the Primary Connector OCP bay. The AC/DC specifications are defined in the NC-SI specification. An example connection diagram is shown in Figure 19.

For the purposes of this specification, the min and max electrical trace length of the NC-SI signals shall be between 2 inches and 4 inches. The traces shall be implemented as 50 Ohm impedance controlled nets.

Table 16: Pin Descriptions – NC-SI Over RBT

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
RBT_CLK_IN	OCP_A14	Output	Reference clock input. Synchronous clock
			reference for receive, transmit and control
			interface. The clock has a nominal frequency of
			50MHz ±100ppm.
			For baseboards, connect this pin between the
			baseboard NC-SI over RBT PHY and the
			connector. This signal requires a 100kOhm pull
			down resistor on the baseboard. If the

			baseboard does not support NC-SI over RBT, then terminate this signal to ground through a 100kOhm pull down resistor. For add-in cards, connect this pin from the gold finger to the endpoint silicon. Leave this pin as a no connect if NC-SI is not supported.
RBT_CRS_DV	OCP_B14	Input	Carrier sense/receive data valid. This signal is used to indicate to the baseboard that the carrier sense/receive data is valid. For baseboards, connect this pin between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull down resistor on the baseboard. If the baseboard does not support NC-SI over RBT, then terminate this signal to ground through a 100kOhm pull down resistor. For add-in cards, connect this pin from the gold finger to the endpoint silicon. Leave this
RBT_RXD0 RBT_RXD1	OCP_B9 OCP_B8	Input	pin as a no connect if NC-SI is not supported. Receive data. Data signals from the network controller to the BMC. For baseboards, connect this pin between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull-up resistor to 3.3Vaux on the baseboard. If the baseboard does not support NC-SI over RBT, then terminate this signal to 3.3Vaux through a 100kOhm pull-up.



			For add-in cards, connect this pin from the
			gold finger to the endpoint silicon. Leave this
			pin as a no connect if NC-SI is not supported.
RBT_TX_EN	OCP_A7	Output	Transmit enable.
			For baseboards, connect this pin between the
			baseboard NC-SI over RBT PHY and the
			connector. This signal requires a 100kOhm pull
			down resistor to ground on the baseboard. If
			the baseboard does not support NC-SI over
			RBT, then terminate this signal to ground
			through a 100kOhm pull down.
			For add-in cards, connect this pin from the
			gold finger to the endpoint silicon. Leave this
			pin as a no connect if NC-SI is not supported.
RBT_TXD0	OCP_A9	Output	Transmit data. Data signals from the BMC to
RBT_TXD1	OCP_A8		the network controller.
			For baseboards, connect this pin between the
			baseboard NC-SI over RBT PHY and the
			connector. This signal requires a 100kOhm
			pull-up resistor to 3.3Vaux on the baseboard. If
			the baseboard does not support NC-SI over
			RBT, then terminate this signal to 3.3Vaux
			through a 100kOhm pull-up.
			For add-in cards, connect this pin from the
			gold finger to the endpoint silicon. Leave this
			pin as a no connect if NC-SI is not supported.
RBT_ARB_OUT	OCP_A5	Output	NC-SI hardware arbitration output. Used only if
INDI_AND_OOT	OCI_A3	σαιραί	the end point silicon supports hardware
I		1	the end point sincon supports hardware

			arbitration. Connects to the ARB_IN signal of an adjacent device.
			The ARB_IN pin is also routed to the card edge to allow multiple devices and OCP slots on the baseboard to share the NC-SI ring. The baseboard shall implement a multiplexing implementation that directs the RBT_ARB_OUT to the RBT_ARB_IN pin of the next NC-SI capable device in the ring, or back to the RBT_ARB_IN pin of the source device if there is a single device on the ring.
			For baseboards, connect this pin between the baseboard OCP connector(s) to complete the hardware arbitration ring. If the baseboard does not support NC-SI over RBT, connect this signal directly to the RBT_ARB_IN pin.
			For add-in cards, connect this pin from the gold finger to the endpoint silicon. Leave this pin as a no connect if NC-SI is not supported.
RBT_ARB_IN	OCP_A4	Input	NC-SI hardware arbitration input. Used only if the end point silicon supports hardware arbitration. Connects to the ARB_OUT signal of an adjacent device.
			The ARB_OUT pin is also routed to the card edge to allow multiple devices and OCP slots on the baseboard to share the NC-SI ring. The baseboard shall implement a multiplexing implementation that directs the RBT_ARB_IN to the RBT_ARB_OUT pin of the next NC-SI

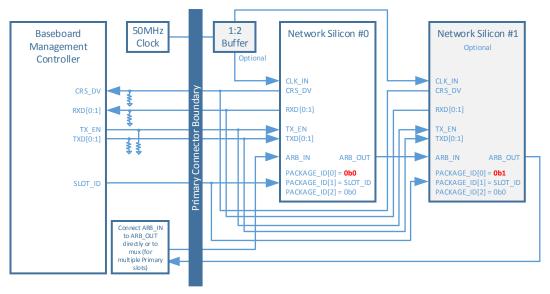


			capable device in the ring, or back to the
			RBT_ARB_OUT pin of the source device if there
			is a single device on the ring.
			For baseboards, connect this pin between the
			baseboard OCP connector(s) to complete the
			hardware arbitration ring. If the baseboard
			does not support NC-SI over RBT, connect this
			signal directly to the RBT_ARB_OUT pin.
			For add in souds compact this min from the
			For add-in cards, connect this pin from the
			gold finger to the endpoint silicon. Leave this
0.07.75	0.65.57		pin as a no connect if NC-SI is not supported.
SLOT_ID	OCP_B7	Output	NC-SI Address pin. Used only if the end point
			silicon supports package identification.
			For baseboards, this pin is used to identify the
			slot ID value. Connect this pin directly to GND
			for SlotID = 0; or pull this pin up to 3.3Vaux
			for SlotID = 1.
			For add-in cards, connect this pin to the
			endpoint Package ID[1] field. Refer to the
			endpoint device datasheet for details.
			The Package ID[2:0] is a 3-bit field and is
			encoded in the NC-SI Channel ID as bits [7:5].
			Package ID[2] is defaults to 0b0 in the NC-SI
			specification, but is optionally configurable if
			the target silicon supports configuring this bit.
			Package ID[1] is connected to the SLOT_ID pin.

Package ID[0] is set to 0b0 for Network Silicon #0. Package ID[1] is set to 0b1 for Network Silicon #1 in the case of an OCP NIC 3.0 card with two discrete silicon instances. As written in the NC-SI specification, up to four silicon devices are supported on the bus if only Package ID[1:0] is configurable (e.g. Package ID[2] is statically set to 0b0). Up to eight silicon devices are supported on the NC-SI bus if Package ID[2:0] are all configurable. For add-in cards with multiple endpoint devices, the SLOT_ID pin may be used to configure a different Package ID value so long as the resulting combination does not cause addressing interferences. For endpoint devices without NC-SI support, leave this pin as a no connect on the add-in card.

Figure 19: NC-SI Over RBT Connection Example





Note 1: For baseboard designs with a single Primary Connector, connect ARB_IN to ARB_OUT to complete the NC-SI hardware arbitration ring. For designs with multiple Primary Connectors, connect ARB_IN and ARB_OUT to an analog mux to complete the NC-SI arbitration ring based on the number of cards installed in the system.

Note 2: For add-in cards with two discrete endpoint silicon, the Package ID[0] bit shall be statically set based on its silicon instance. For example, the figure above shows Network Silicon #0 and Network Silicon #1. Network Silicon #0 has Package ID[0] = 0b0, Network Silicon #1 has Package ID[0] = 0b1.

3.5.3 Scan Chain Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the Scan Bus interface signals on the Primary Connector OCP Bay. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure 20.

Table	e 17:	Pin	Descript	tions –	Scan	Chain
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Signal Name	Pin #	Baseboard	Signal Description
		Direction	
CLK	OCP_B6	Output	Scan clock. The CLK is an output pin from the baseboard to the add-in card. The CLK may run up to 12.5MHz.

			For baseboard implementations, connect the CLK pin to the Primary Connector. Tie the CLK pin directly to GND if the scan chain is not used. For NIC implementations, the CLK pin must be connected to Shift Registers 0 & 1, and optionally to Shift Registers 2 & 3 (if implemented) as defined in the text and Figure 20, below. Pull the CLK pin up to 3.3Vaux through a 1kOhm resistor.
DATA_OUT	OCP_B5	Output	Scan clock data output from the baseboard to the add-in card. This bit stream is used to shift in NIC configuration data. For baseboard implementations, connect the DATA_OUT pin to the Primary Connector. Tie the DATA_OUT pin directly to GND if the scan chain is not used. For NIC implementations, the DATA_OUT pin may be left floating if it is not used for add-in card configuration. Pull the DATA_OUT pin up
DATA_IN	OCP_B4	Input	to 3.3Vaux through a 1kOhm resistor. Scan clock data input to the baseboard. This bit stream is used to shift out NIC status bits. For baseboard implementations, the DATA_IN pin shall be pulled up to 3.3Vaux through a 10kOhm resistor to prevent the input signal from floating if a card is not installed. This pin may be left as a no connect if the scan chain is not used.



			For NIC implementations, the DATA_IN scan chain is required. The DATA_IN connection to Shift Registers 0 & 1, as defined in the text and Figure 20, are required.
LD# OO	OCP_B3	Output	Scan clock shift register load. Used to latch configuration data on the add-in card. For baseboard implementations, the LD# pin shall be pulled up to 3.3Vaux through a 1kOhm resistor if the scan chain is not used to prevent the add-in card from erroneous data latching. For NIC implementations, the LD# pin implementation is required. The LD# pin must be connected to Shift Registers 0 & 1 as defined in the text and Figure 20. Pull the LD# pin up to 3.3Vaux through a 1kOhm resistor.

The scan chain provides side band status indication between the add-in card and the baseboard. The scan chain bit definition is defined in the two tables below. The scan chain data stream is 32-bits in length for both the DATA_OUT and the DATA_IN streams. The scan chain implementation is optional on the host, but is mandatory on all OCP NIC 3.0 cards. The scan chain components operates on the 3.3Vaux power domain.

The DATA_OUT bus is an output from the host. The DATA_OUT bus provides initial configuration options to the add-in card. At the time of this writing, the default implementation does not use the DATA_OUT stream and is not implemented on the NIC. However, all baseboard systems that implement the Scan Chain shall connect DATA_OUT between the platform and the Primary Connector for future-proofing NIC implementations and subsequent revisions of this specification.

Byte.bit	DATA_OUT Field	Default	Description
	Name	Value	
0.[07]	RSVD	0b000000	Reserved. Byte 0 value is 0h00.
1.[07]	RSVD	0h00	Reserved. Byte 1 value is 0h00.
2.[07]	RSVD	0h00	Reserved. Byte 2 value is 0h00.
3.[07]	RSVD	0h00	Reserved. Byte 3 value is 0h00.

The DATA_IN bus is an input to the host and provides NIC status indication. The default implementation is completed with two 8-bit 74LV165 parallel in to serial out shift registers in a cascaded implementation. Up to four shift registers may be implemented to provide additional NIC status indication to the host platform.

DATA_IN shift registers 0 & 1 are mandatory for all cards. DATA_IN shift registers 2 & 3 are optional depending on the card type and fields being reported to the host. DATA_IN shift register 2 may be used to indicate future definitions of the scan chain bit stream. DATA_IN shift registers 3 (in conjunction with shift register 2) are required for reporting link/activity indication on card implementations with 5-8 ports.

The host should read the DATA_IN bus multiple (TBD) times to qualify the incoming data stream.

A 1kOhm pull up resistor shall be implemented on the NIC to the SER input of the last shift register on the DATA_IN scan chain to maintain a default bit value of 0b1 for unused bits for implementations using less than four shift registers.

Table 19: Pin Descriptions – Scan Bus DATA_IN Bit Definition

Byte.bit	DATA_OUT Field	Default	Description
	Name	Value	
0.0	PRSNTB[0]#	0bX	PRSNTB[3:0]# value is mirrored from the
0.1	PRSNTB[1]#	0bX	Primary Connector.
0.2	PRSNTB[2]#	0bX	
0.3	PRSNTB[3]#	0bX	



0.4	WAKE_N	0bX	PCIe WAKE_N signal is mirrored from the
			Primary Connector.
0.5	TEMP_WARN	0b0	Temperature monitoring pin from the on-
			card thermal solution. This pin is asserted
			high when temperature sensor exceeds the
			temperature warning threshold.
0.6	TEMP_CRIT	0b0	Temperature monitoring pin from the on-
			card thermal solution. This pin is asserted
			high when temperature sensor exceeds the
			temperature critical threshold.
0.7	FAN_ON_AUX	0b0	When high, FAN_ON_AUX requests the
			system fan to be enabled for extra cooling in
			the S5 state.
1.0	LINK_ACT0	0b1	Port 03 link/activity indication. Active low.
1.1	LINK_ACT1	0b1	
1.2	LINK_ACT2	0b1	0b0 – Link LED is illuminated on the host
1.3	LINK_ACT3	0b1	platform.
			0b1 – Link LED is not illuminated on the host
			platform.
			Steady = link is detected on the port.
			Blinking = activity is detected on the port.
			The blink rate should blink low for 50-500ms
			during activity periods.
			Off = the physical link is down or disabled
1.4	SPEED0	0b1	Port 03 speed indication. Active low.
1.5	SPEED1	0b1	
1.6	SPEED2	0b1	0b0 – Port is linked at maximum speed.
1.7	SPEED3	0b1	0b1 – Port is not linked at the maximum
			speed or no link is present.
2.0	ScanChainVer[0]	0b1	ScanChainVer[1:0] is used to indicate the scan
2.1	ScanChainVer[1]	0b1	chain bit definitions. The encoding is as
			follows:

			0b11 – Scan chain bit definitions version 1 corresponding to OCP 3.0 spec version 1.0.
			All other encodings are reserved.
2.2	RSVD	0b1	Byte 2 bits [2:7] are reserved. These bits shall
2.3	RSVD	0b1	default to the value of 0b1. These bits may
2.4	RSVD	0b1	be used in future versions of the scan chain.
2.5	RSVD	0b1	
2.6	RSVD	0b1	
2.7	RSVD	0b1	
3.0	LINK_ACT4	0b1	Port 47 link/activity indication. Active low.
3.1	LINK_ACT 5	0b1	
3.2	LINK_ACT 6	0b1	0b0 – Link LED is illuminated on the host
3.3	LINK_ACT 7	0b1	platform. 0b1 – Link LED is not illuminated on the host platform.
			Steady = link is detected on the port. Blinking = activity is detected on the port. The blink rate should blink low for 50-500ms
			during activity periods. Off = the physical link is down or disabled
3.4	SPEED4	0b1	Port 47 speed indication. Active low.
3.5	SPEED5	0b1	
3.6	SPEED6	0b1	0b0 – Port is linked at maximum speed.
3.7	SPEED7	0b1	0b1 – Port is not linked at the maximum
			speed or no link is present.



Host PLD 74LV594 The 74LV594 DATA_OUTs hift register has no defined function in the current OCP NIC 3.0 specification and is reserved for future use on later revisions of the spec. VCC QA QB QC SER DATA_OUT QD QE QF CLK (12.5MHz) SRCLK SRCLRn RCLK LD_N QH RCLRn Connector Boundary QH GND 74LV165 #0 VCC PRSNTB[0]# (Mirrored from Primary Connector) PRSNTB[1]# (Mirrored from Primary Connector)
 PRSNTB[2]# (Mirrored from Primary Connector) CL K CLK INH PRSNTB[3]# (Mirrored from Primary Connector) - WAKE_N
- TEMP_WARN
- TEMP_CRIT
- FAN_ON_AUX SH/LDn G H QH QH' DATA_IN SER GND 74LV165 #1 LINK_ACTO (Active Low = ON, default 0b1) LINK_ACT1 (Active Low = ON, default 0b1) CLK LINK_ACT2 (Active Low = ON, default 0b1) LINK_ACT3 (Active Low = ON, default 0b1) CLK_INH D SPEED0 (Active Low = ON, default 0b1) SH/LDn SPEED1 (Active Low = ON, default 0b1) SPEED2 (Active Low = ON, default 0b1) G H 1k QH SPEED3 (Active Low = ON, default 0b1) QH SER GND Implement a 1kOhm pull up to 3.3Vaux for the last shift register on the bus. 74LV165 #2 VCC A B CLK C D CLK_INH SH/LDn G QH SER GND 74LV165 #3 VCC CLK_INH D SH/LDn G QH SER GND

Figure 20: Scan Bus Connection Example

3.5.4 Primary Connector Miscellaneous Pins – OCP Bay (Primary Connector)

This section provides the miscellaneous pin assignments for the pins on the Primary Connector OCP Bay. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0 and Section 3.12. An example connection diagram is shown in Figure XXX.

Table 20: Pin Descriptions – Miscellaneous 2

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
PWRBRK#	OCP_B2	Output,	Power break. Active low, open drain.
		OD	
			This signal is pulled up to 3.3Vaux on the
			add-in card with a minimum of 95kOhm and
			the baseboard with a stiffer resistance in-
			order to meet the timing specs as shown in
			the PCIe CEM Specification.
			This signal is driven low by the baseboard
			and is used to notify that an Emergency
			Power Reduction State is requested. The add-
			in card shall move to a lower power
			consumption state.
NIC_PWR_GOOD	OCP_B1	Input	NIC Power Good. Active high. This signal is
			driven by the add-in card.
			When high, this signal indicates that all of the
			add-in card power rails are operating within
			nominal tolerances.
			When low the add-in card power supplies are
			not yet ready or are in a fault condition.
			For baseboards, this pin may be connected to
			the platform I/O hub as a NIC power health



			status indication. This signal is pulled down to ground with a 100kOhm resistor on the baseboard to prevent a false power good indication if no add-in card is present.
			For add-in cards this signal may be
			implemented by a cascaded power good or a
			discrete power good monitor output.
GND	OCP_A6	GND	Ground return; a total of 5 ground pins are
	OCP_A10		on the OCP bay area.
	OCP_A13		
	OCP B10		
	OCP_B13		

3.6 PCIe Bifurcation Mechanism

OCP3.0 baseboards and add-in cards support multiple bifurcation combinations. Single socket baseboards with a single or multiple root ports, as well as a multi-socket baseboards with a single or multiple root ports are supported. The bifurcation mechanism also supports add-in cards with a single or multiple end points. These features are accomplished via I/O pins on the Primary and Secondary connector:

- PRSNTA#, PRSNTB[3:0]#. The PRSNTA# pin connects to the PRSNTB# pins as a hard coded value on the add-in card. The encoding of the PRSNTB[3:0]# pins allows the baseboard to determine the PCIe Links available on the add-in card.
- BIF[3:0]#. The BIF# pin states are controlled by the baseboard and allows the baseboard
 to override the default end point bifurcation for silicon that support bifurcation.
 Additional combinatorial logic is required and is specific to the card silicon. The
 combinatorial logic is not covered in this specification.

The high level bifurcation connections are shown in Figure 21.

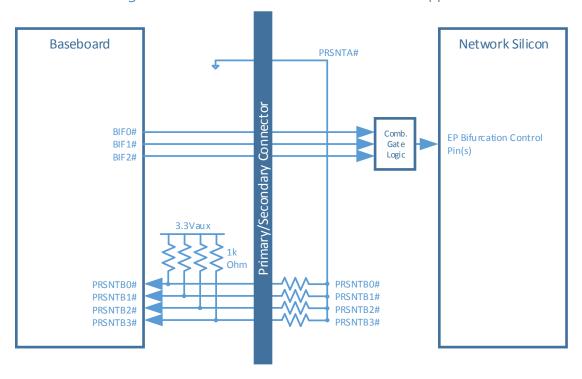


Figure 21: PCIe Bifurcation Pin Connections Support

3.6.1 PCIe Add-in Card to Baseboard Bifurcation Configuration (PRSNTA#, PRSNTB[3:0]#)

The add-in card to baseboard configuration mechanism consists of four dual use pins (PRSNTB[3:0]#) on the add-in card and a grounded PRSNTA# pin on the baseboard. These pins provide card presence detection as well as mechanism to notify the baseboard of the pre-defined PCIe lane width capabilities. The PRSNTB[3:0]# pins are pulled up to 3.3Vaux on the baseboard and are active low signals. A state of 0b1111 indicates that no card is present in the system. Depending on the capabilities of the add-in card, a selection of PRSNTB[3:0]# signals may be strapped to the PRSNTA# signal and is pulled low by the baseboard. The encoding of the PRSTNB[3:0]# bits is shown in Table 21 for x16 and x8 PCIe cards.

3.6.2 PCIe Baseboard to Add-in Card Bifurcation Configuration (BIF[2:0]#)

Three signals (BIF[2:0]#) are driven by the baseboard to notify requested bifurcation on the add-in card silicon. This allows the baseboard to set the lane configuration on the add-in card that supports multiple bifurcation options.



For example, a baseboard that has four separate hosts that support a 4 x4 connection, should appropriately drive the BIF[2:0]# pins per Table 21 and indicate to the add-in card silicon to setup a 4 x4 configuration.

As previously noted, the BIF[2:0]# signals require additional combinatorial logic to decode the BIF[2:0]# value and appropriately apply it to the end-point silicon. The combinatorial logic is not covered in the specification as its implementation is specific to the vendor silicon used.

3.6.3 PCIe Bifurcation Decoder

The combination of the PRSNTB[3:0]# and BIF[2:0]# pins deterministically sets the PCIe lane width for a given combination of baseboard and add-in cards. Table 21 shows the resulting number of PCIe links and its width for known combinations of baseboards and add-in cards.

*Note: The baseboard must disable PCIe lanes during the initialization phase if the number of detected PCIe links are greater than what is supported on the baseboard to prevent a nondeterministic solution. For example, if the baseboard only supports a 1 x16 connection, and the add-in card only supports a 2 x8 connection, the baseboard must disable PCIe lanes 8-15 to prevent any potential LTSSM issues during the discovery phase.

Table 21: PCIe Bifurcation Decoder for x16 and x8 Card Widths

					Single Host			RSVD		Dual Host	Liuad Host	Quadruct nost
		Host		1Host	1 Host	1 Host	1 Host				4 Hosts	4 or 8 Hosts
		Host CPU Sockets	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	2 Upstream Sockets	2 Upstream Sockets 4 Upstream Sockets	RSVD	RSVD	2 Upstream Sockets (1 Socket per Host)	4 Upstream Sockets (1 Socket per Host)	4/8 Upstream Sockets (1 Socket per Host)
Network Card - Supported PCk	Network Card – Supported PCIe Configurations	Total PCle Links	1Link (No Bifurcation)	1 or 2 Links	1, 2, or 4 Links	2 Links	4 Links	RSVD	RSVD	2 Links	4 Links	4 or 8 x2 links
		System Support	1x16, 1x8, 1x4, 1x2, 1x1	1x16,1x8,1x4,1x2,1x1	÷	1x8,1x4,1x2,1x1		RSVD	BSVD			
				2x8,2x4,2x2,2x1	2x8,2x4,2x2,2x1	2 x8, 2 x4, 2 x2, 2x1				2 x8, 2 x4, 2 x2, 2 x1		
					4 x4, 4 x2, 4 x1		4 x4, 4 x2, 4x1				4×4, 4×2, 4×1	4×2, 4×1
		System Encoding	00000	00000	00000	06001	0b010	05011	0P100	05101	0b110	0b111
Card Short x16 Cards	16 Cards	Add-in-Card Encoding			-			ı	ı			
┪		B[3:0]#										
Not Present C.	Card Not Present		HSVD - Card not present in the system	the system								
97	1x8,1x4,1x2,1x1	0b1 110	9%	2×8 8×1	1%8	1x8 (Socket Donly)	1x4 (Socket Donly)		1	1x8 (Host 0 only)	1x4 (Host Donly)	1x2 (Host Donlu)
	1×4, 1×2, 1×1	0b1110	1×4	1×4	1 %+	1x4 (Sooket Donly)	1x4 (Sooket Dooks)			1x4 (Host Donly)	1×4 (Host Donly)	1x2 (Host Donly)
	182,181	061110	182	182	182	1,2	182			1,82	182	182
182	4.4	01:4440	100	1.0	F1 12	(Sooket Uonly)	(Socket Uonly)			(Host Uonly)	(Host Uonly)	(Host Uonly)
Ę	×	2	Ē	ž	Ē	(Sooket Donly)	(Socket 0 only)	'		(Host 0 only)	(Host 0 only)	(Host Donly)
1x8,1x4,1x2,1 1x8 Option B 2x4,2x2,2x1	1x8, 1x4, 1x2, 1x1 2x4, 2x2, 2x1	0b11 01	1×8	1×8	1×8	1x8 (Socket 0 only)	2 84	1		1x8 (Host 0 only)	2 84	2x2 (Host 0 & 1 only)
2 x8, 2 x4, 2 x2 2 x8 Option B 4 x4, 4 x2, 4 x1	2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1	0b1 101	1887	2 x8	2×8	2 x8	4 84		ı	2 48	4 84	2x2 (Host 0 & 1 only)
1 2 1 4 1 4	1x8,1x4 2x4, 1v8 Detice D 4 v2 First 8 lance) 4 v1	0b1100	1×8	2 *4	2×4	1x8 (Socket 0 only)	2 84	-	-	1x8 (Host 0 only)	2×4	4×2
1-15 Detion 4	148 Detect Barses 4 of	061100	1x16	1×16	1×16	2 48	4×4	1	1	2 **8	4×4	4 82
RSVD R	RSVD	0b1 011	BSVD - The encoding of 0b 1011 is reserved due to insufficient spacing between PRSMTA and PRSMTB2 pin to provide positive card identification.	b1011 is reserved due to in	sufficient spacing between	n PRSNTA and PRSNTB2	pin to provide positive card	didentifica	ation.			
4	2 x4, 2 x2, 2 x1 1x4, 1x2, 1x1	051 010	4×1	284	2×4	1x4 (Sooket 0 only)	284		1	1x4 (Host 0 only)	2×4	2x2 (Host 0 & 1only)
	RSVD for future x8 encoding 0b1001	0b1 001										
RSVD R	RSVD for future x8 encoding 0b1000	0b1 000		-	-	-	-	-			-	-
1,816	1x16,1x8,1x4,1x2,1x1	060111	1x16	1×16	1x16	1x8 (Socket 0 only)	1x4 (Socket 0 only)	1		1x8 (Host 0 only)	1x4 (Host 0 only)	1x2 (Host 0 only)
2×8 Option A	2x8,2x4,2x2,2x1	060110	1881	2 x8	2×8	2 x8	2 x4 (Sooket 0 & 2 only)	1	ı	2.48	2x4 (Host 0 & 2 only)	1x2 (Host 0 & 1 only)
1; 1x16 Option B 2.	1x16,1x8,1x4,1x2,1x1 1x16 Dption B 2x8,2x4,2x2,2x1	0601 01	1x16	1×16	1x16	2 x8	2x4 (Socket 0 & 2 only)	1	ı	2.48	2x4 (Host 0 & 2 only)	2x2 (Host 0 & 1only)
1x16,1x8,1x4 2x8,2x4,2x2 1x16 Option C 4x4,4x2,4x1	1x16,1x8,1x4 2x8,2x4,2x2,2x1 4x4,4x2,4x1	0b0 100	1x16	1×16	1x16	2 x8	4×4	1	1	2 48	4×4	2 x2 (Host 0 & 1 only)
4×4	к2, 4 к1	060011	184*	2×4*	4×4	2×4 (EP 0 and 2 only)	4 × 4		1	2 x4 (EP 0 and 2 only)	4 84	4 x2 (Host 0 & 1 only)
		060010						-	1			
	RSVD	060 001								-		
ă CP (CA		0F0 00 0	•		,		,	,				



3.6.4 Bifurcation Detection Flow

[Need input and clarification from system vendors]

The following detection flow shall be used to determine the resulting link count and lane width based on the baseboard and add-in card configurations.

- 1. The baseboard reads the state of the PRSNTB[3:0]# pins. If the resulting value is not 0b1111, an add-in card is present.
- 2. Firmware determines the add-in card PCIe lane width capabilities per Table 21 by reading the PRSNTB[3:0]# pins.
- 3. The baseboard reconfigures the PCIe bifurcation on its ports to match the highest common lane width and lowest common link count on the card.
- 4. For cases where the baseboard request a link count override (such as requesting a 4-host baseboard requesting 4 x4 operation on a supported card that would otherwise default to a 2 x8 case), the BIF[0:2]# pins would be asserted as appropriate. Doing so assumes the add-in card supports the requested link override.
- 5. PERST# is deasserted after the >100ms window as defined by the PCIe specification.

 Refer to Section 3.12 for timing details.

3.6.5 PCIe Bifurcation Examples

For illustrative purposes, the following figures show several common bifurcation permutations.

Figure 22 illustrates a single host baseboard that supports x16 with a single controller add-in card that also supports x16. The PRSTNB[3:0]# state is 0b0111. The BIF[2:0]# state is 0b000 as there is no need to instruct the end-point network controller to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16. The single host baseboard determines that it is also capable of supporting 1 x16. The resulting link width is 1 x16.

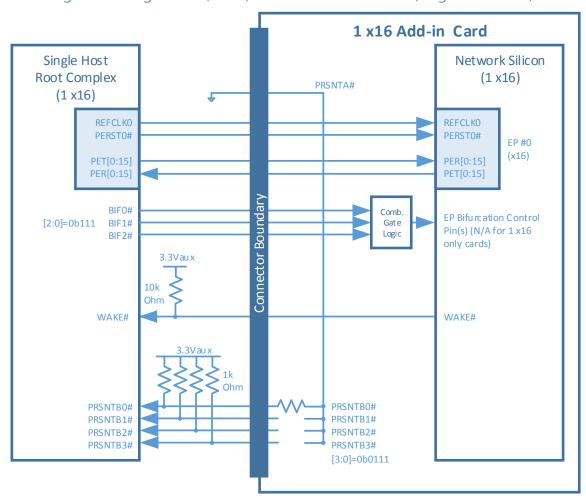


Figure 22: Single Host (1 x16) and 1 x16 Add-in Card (Single Controller)

Figure 23 illustrates a single host baseboard that supports 2 x8 with a single controller addin card that also supports 2 x8. The PRSTNB[3:0]# state is 0b0110. The BIF[2:0]# state is



0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 2 x8. The single host baseboard determines that it is also capable of supporting 2 x8. The resulting link width is 2 x8.

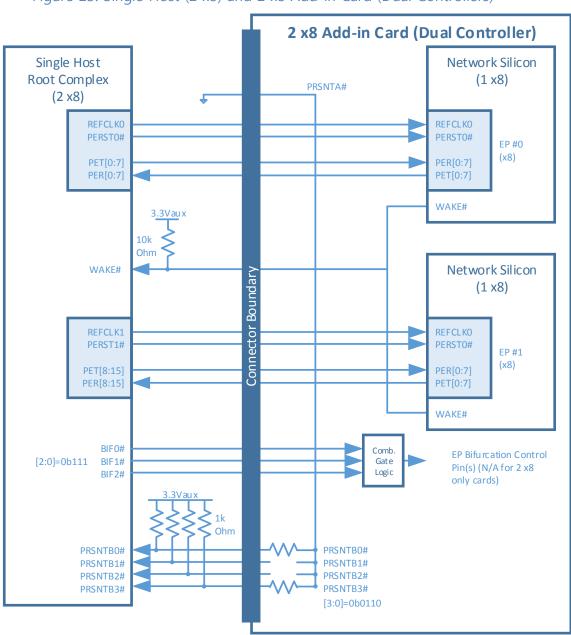


Figure 23: Single Host (2 x8) and 2 x8 Add-in Card (Dual Controllers)

Figure 24 illustrates a four host baseboard that supports 4 x4 with a single controller add-in card that supports 1 x16, 2 x8 and 4 x4. The PRSTNB[3:0]# state is 0b0011. The BIF[2:0]# state is 0b101 as the end point network controller is forced to bifurcate to 4 x4. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16, 2 x8 and 4 x4. The four host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

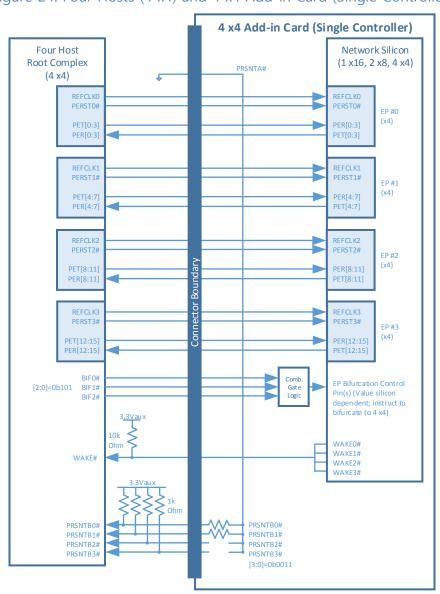


Figure 24: Four Hosts (4 x4) and 4 x4 Add-in Card (Single Controller)



Figure 25 illustrates a four host baseboard that supports 4 x4 with a four controller add-in card that supports 4 x4. The PRSTNB[3:0]# state is 0b0011. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 4 x4. The four host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

Figure 25: Four Hosts (4 x4) and 4 x4 Add-in Card (Four Controllers)

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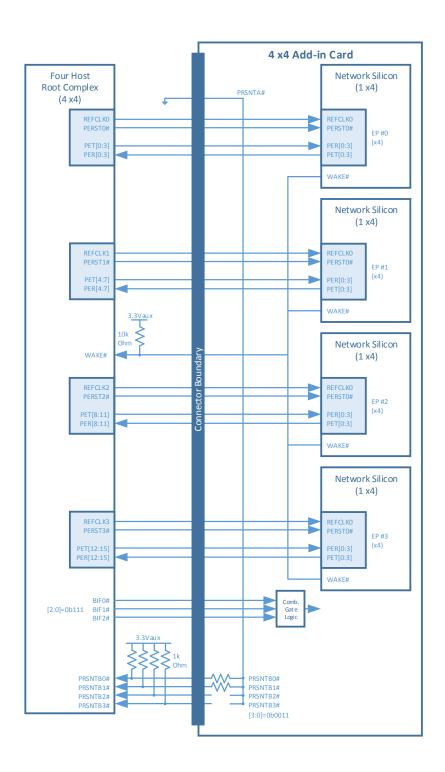




Figure 26 illustrates a single host baseboard that supports 1 x16 with a dual controller addin card that supports 2 x8. The PRSTNB[3:0]# state is 0b0110. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 2 x8. The four host baseboard determines that it is capable of 1x 16, but down shifts to 1 x8. The resulting link width is 1 x8 and only on endpoint 0.

Figure 26: Single Host with no Bifurcation (1 x16) and 2 x8 Add-in Card (Two Controllers) 2 x8 Add-in Card (Dual Controller) Network Silicon Single Host (1 x8)**Root Complex** PRSNTA# (1 x 16)**REFCLKO** REFCLKO PERSTO# PERSTO# EP #0 (x8) PER[0:7] PET[0:15] PET[0:7] PER[0:15] WAKE# Lanes 8:15 3.3Vaux disabled WAKE# Network Silicon Connector Boundary (1 x8)**REFCLKO** The second x8 PERSTO# EP #1 is not supported on (x8) PER[0:7] this host. PET[0:7] WAKE# BIFO# Comb. **EP Bifurcation Control** [2:0]=0b111 BIF1# Gate Pin(s) (N/A for 2 x8 Logic BIF2# only cards) PRSNTB0# PRSNTB0# PRSNTB1# PRSNTB1# PRSNTB2# PRSNTB2# PRSNTB3# PRSNTB3# [3:0]=0b0110

3.7 PCIe Clocking Topology

The OCP NIC 3.0 specification allows for up to four PCIe REFCLKs on the Primary Connector and up to two PCIe REFCLKs on the Secondary Connector. In general, the association of each REFCLK is based on the PCIe Link number on a per connector basis and is shown in Table 22. Cards that implement both the Primary and Secondary connectors have a total of up to 6 REFCLKs.

REFCLK #	Description	Availability (Connector)
REFCLK0	REFCLK associated with Link 0.	Primary and Secondary Connectors.
REFCLK1	REFCLK associated with Link 1.	Primary and Secondary Connectors.
REFCLK2	REFCLK associated with Link 2.	Primary Connector only.
REFCLK3	REFCLK associated with Link 3.	Primary Connector only.

Table 22: PCIe Clock Associations

For each add-in card, the following REFCLK connection rules must be followed:

- For a 1 x16 capable add-in card, REFCLKO is used for lanes [0:15].
- For a 2 x8 capable add-in card, REFCLK0 is used for lanes [0:7] and REFCLK1 is used for lanes [8:15].
- For a 4 x4 capable add-in card, REFCLK0 is used for lanes [0:3], REFCLK1 is used for lanes [4:7], REFCLK2 is used for lanes [8:11] and REFCLK3 is used for lanes [12:15]. Pins for REFCLK2 and REFCLK3 are described in Section 3.5.1 and are located on the 28-pin OCP bay.

Figure 27: PCIe Interface Connections for 1 x16 and 2 x8 Add-in Cards



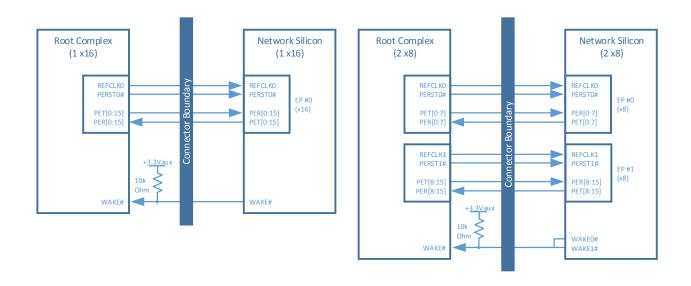
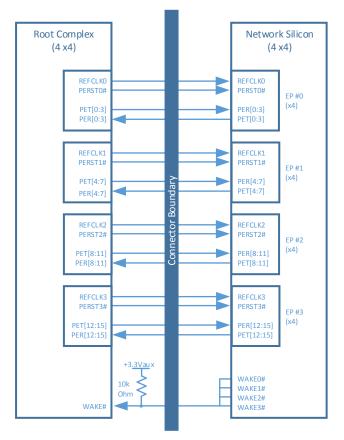


Figure 28: PCIe Interface Connections for a 4 x4 Add-in Card



3.8 PCIe Bifurcation Results and REFCLK Mapping

For the cases where the baseboard and add-in card bifurcation are permissible, this section enumerates all of the supported PCIe link, lane and REFCLK mappings for each supported configuration. The bifurcation decoder is shown in Section 3.6.3.



Table 23: Bifurcation for Single Host, Single Socket and Single Upstream Link (BIF[2:0]#=0b000)

Single H	'ost, Single Ups	Single Host, Single Upstream Socket, One Upstream Link, no bifurcation	no bifurcation,		1x16, 1x8, 1x4, 1x2, 1																		
i P	Min Suppor Card Card Short Modes Width Name	Supported Bifurcation Add-in-Card Modes Encoding	Add-in-Card Encoding PRSMTB(3:0)#	Host	Instress Devices	Upstream	BIF[2:0]	Recelling link Jane 1 Jane 2 Jane 3 Jane 4 Jane 7 Jane 7 Jane 7 Jane 12 Jane 13 Jane 14 Jane 14	9	-			1						9	- 1	-	-	- 1
c _l u	Not Present	Card Not Present	0b1 111	1 Host	1 Upstream Socket	1 Link	00090																
		1x8,1x4,1x2,1x1	0b1 110	1 Host		1 Link	00000	1x8	Link 0,	Н	-	-	Н	-	-	Link 0,							
SC	1×8								Lane 0	\dashv	-	-	Lone 4	Lane 5 Lt	Lane 6 Lar	Lone 7							
8	1×4	1x4,1x2,1x1	0P1 110	1Host	1 Upstream Socket	1Link	00090	1×4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3				_						_	
ရွ	5X	1x2,1x1	061110	1 Host	1 Upstream Socket	1Link	00090	1x2	Link 0, Lane 0	Link 0, Lane 1													
28	72	1x1	0b1 110	1 Host	1 Upstream Socket	1Link	00090	1x1	Link 0, Lane 0														
ç	1 v8 Option B	1x8,1x4,1x2,1x1	0b1 101	1 Host	1 Upstream Socket	1Link	00090	1x8	Link 0,	Link 0, Lone 1	Link 0,	Link 0, 1	Link 0, L	Link 0, Li	Link O, Lin	Link 0, Lone 7							
9		2 x8,2 x4,2 x2,2 x1	061101	1 Host	1 Upstream Socket	1Link	00090	1×8*	Link 0,	+	-	-	-	-	+	Link 0,		-				L	
2	a vo opdon s	108 104	081100	1 House	11 Incheses Cookst	4154		87.0	o alle o	+	+	+	+	+	+	Lame	+	+	+	+	+	1	1
g	1x8 Option D	2 x4, 1x8 Option D 4 x2 (First 8 lanes), 4 x1		Í			00090		Lane							Lane 7							
		1x16,1x8,1x4	0P1100	1 Host	1 Upstream Socket	1 Link		1×16	Link 0,	⊢	⊢	⊢	⊢	⊢	⊢	⊢	⊢	Link O, Link O,	⊢	⊢	-	-	Link 0,
ş	1x16 Option E	1x16 Option D 4x4, 4x2 (First 8 lanes), 4x1					00000		Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5 Lt	Lane 6 Lar	Lane 7 Lar	Lane 8 Lar	Lane 9 Lane	.10 Lane 11	11 Lane 12	2 Lane 13	Lane 14	
RSVD	RSVD RSVD	RsvD	0b1 011	1 Host	1 Upstream Socket	1 Link	00090																
ပ္လ	2×4	2x4,2x2,2x1 1x4,1x2,1x1	051 010	1 Host	1 Upstream Socket	1Link	00090	1x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3											
BSVD	RSVD RSVD	BSVD for future x8 encoding 0b1001	061001	1 Host	1 Upstream Socket	1Link	00090			Н	H								-	-	-	L	L
RSVD	RSVD RSVD	RSVD for future x8 encoding	0P1000	1Host	1 Upstream Socket	1 Link	00090																
ĝ	1×16	1x16,1x8,1x4,1x2,1x1	060111	1 Host	1 Upstream Socket	1 Link	00090	1×16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, L	Link O, L	Link O, Li Lane S L:	Link O, Lin Lane 6 Lar	Link O, Lin Lane 7 Lar	Link O, Lin Lane 8 Lar	Link 0, Link 0, Lane 3 Lane 10	Link O, Link O, Lane 10 Lane 11	0, Link 0, 11 Lane 12	0, Link 0, 12 Lane 13	Link 0,	Link 0, Lane 15
Q.	2 x8 Option A	2x8,2x4,2x2,2x1 4	011090	1 Host	1 Upstream Socket	1Link	00090	1×8*	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, Lane 3	Link O, L	Link O, Li Lane S L:	Link O, Lin Lane 6 Lar	Link O, Lane 7							
ĝ	1x16 Option E	1x16,1x6,1x4,1x2,1x1 1x16 Option B 2x8,2x4,2x2,2x1	060101	1 Host	1 Upstream Socket	1 Link	00090	1×16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, L	Link 0, L	Link O, Li Lane S L:	Link O, Lin Lane 6 Lar	Link O, Lin Lane 7 Lar	Link O, Lin Lane 8 Lar	Link 0, Link 0, Lane 3 Lane 10	Link O, Link O, Lane 10 Lane 11	0, Link 0, 11 Lane 12	o, Linko, I2 Lane 13	Lane 14	Link 0, Lane 15
û	1x16 Option C	1x16,1x8,1x4 2x8,2x4,2x2,2x1 1x16 Option C 4x4,4x2,4x1	0001000	1Host	1 Upstream Socket	1 Link	00090	1x16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, L	Link 0, L	Link O, Li Lane 5 Lr	Link O, Lin Lanc 6 Lar	Link O, Lin Lane 7 Lar	Link O, Lin Lane 8 Lar	Link O, Link Lane 9 Lane	Link O, Link O, Lane 10 Lane 11	0, Link 0, 11 Lane 12	o, Linko, I2 Lane 13	Link 0,	Link 0, Lane 15
Q‡	4 ×4	4 x4, 4 x2, 4 x1	050011	1 Host	1 Upstream Socket	1Link	00090	1×4*	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3											
BSVD	RSVD RSVD	RSVD	0P0 010	1 Host	1 Upstream Socket	1 Link	00090																
RSVD	RSVD RSVD	RSVD	000 001	1 Host	1 Upstream Socket	1 Link	00090																
RSVD	RSVD RSVD	RSVD	000000	1Host	1 Upstream Socket	1Link	00090															_	_

Table 24: Bifurcation for Single Host, Single Socket and Single/Dual Upstream Links
(BIF[2:0]#=0b000)

Single H	ost, Single Upst	Single Host, Single Upstream Socket, One or Two Upstream Links	eam Links		1x16,1x8,1x4,1x2,1 2x8,2x4,2x2,2x1																		
Min Card Card	Min Suppor Card Card Short Modes	Supported Bifurcation Add-in-Card Modes Encoding PRENTERSON	Add-in-Card Encoding PRSMTBI3:01#	Host	Upstream Devices	Upstream	BIF[2:0]	Reculting link lane 0 lane 2 lane 3 lane 4	0 46	1 26	300.2	986 3	7 346	2 346	9 9 6	3 arc 13 arc 13 arc 13 arc 10 arc 10 arc 12 arc 13 arc 15 a	8 4	6 94	9		12	51	7
c/u	Not Present	Card Not Present	0b1 111	1 Host		1 or 2 Links	00090																
ρ N	- ×-	1x8,1x4,1x2,1x1	0P1110	1 Host	1 Upotream Socket	1 or 2 Links	00090	1x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link 0, Lane 7							
S	1×4	1x4,1x2,1x1	0P1110	1Host	1 Upotream Socket	1 or 2 Links	00090	1x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3											
g	ź,	1x2,1x1	0b1 110	1Host	1 Upstream Socket	1 or 2 Links	00090	1x2	Link 0, Lane 0	Link 0, Lane 1													
S	2	1x1	0b1 110	1 Host	1 Upstream Socket	1 or 2 Links	00090	1×1	Link 0, Lane 0														
ပ္လ	1x8 Option B	1x8,1x4,1x2,1x1 1x8 Option B 2x4,2x2,2x1	0b1101	1 Host	1 Upstream Socket	1 or 2 Links	00090	1x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, 1 Lane 6	Link 0, Lane 7							
û	2 x8 Option B	2x8,2x4,2x2,2x1 2x8 Option B 4x4,4x2,4x1	0b1101	1Host	1 Upstream Socket	1 or 2 Links	00090	2 x8	Link O, Lane O	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link O, L	Link O, L	Link 1, L	Link 1, L	Link 1, L	Link 1, Li Lane 3 La	Link 1, Lir Lane 4 La	Link 1, Link 1, Lane 5 Lane 6	1, Link 1, 6 Lane 7
ಲ್ಲ	1x8 Option D	1x8,1x4 2x4, 1x8 Option D 4x2 (First 8 lanes), 4x1	061 100	1 Host	1 Upotream Socket	1 or 2 Links	00000	1x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, 1 Lane 6	Link 0, Lane 7							
û	1x16 Option D	1x16,1x8,1x4 2x8,2x4, 1x16 Option D 4x4,4x2 (First 8 lanes),4x1	061 100	1 Host	1 Upotream Socket	1 or 2 Links	00090	1x16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, 1 Lane 6	Link O, L Lane 7 L	Link O, Lane 8	Link O, L Lane 3 L:	Link O, L	Link O, Lin Lane 11 La	Link O, Lin Lane 12 Lan	Link 0, Link 0, Lane 13 Lane 14	0, Link 0, 14 Lane 15
_	RSVD RSVD	BSVD	0b1 011	1Host	1 Upstream Socket	1 or 2 Links	00000																
28	2×4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1 010	1 Host	1 Upstream Socket	1 or 2 Links	00090	1x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3											
RSVD	RSVD	RSVD for future x8 encoding 0b1001	0b1001	1 Host	Ц	1 or 2 Links	00090																Н
HSVD HSVD	HSVD	HSVD for future x8 encoding	0001000	1 Hoot	1 Upstream Socket	1 or 2 Links	npngn	. 57	0.450	0.451	0.451	0.451	0.4%1	0.441	0.751	0.451	0.451	0.451	0.451	0.451	0.451	0.451	0 4 5 1
\$	1×16	1210, 120, 124, 136, 131		1000	1 Opercean sooner	I Of & Links	00090	olx.	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	_		_	_		_		_	_	
9	2 x8 Option A	2x8,2x4,2x2,2x1	0P0110	1 Host	1 Upstream Socket	1 or 2 Links	00090	2×8	Link O, Lane O	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link O, Lane 4	Link O,	Link O, L	Link O, L	Link 1, L	Link 1, L	Link 1, L	Link 1, Lii Lane 3 La	Link 1, Lin Lane 4 La	Link 1, Link 1, Lane 5 Lane 6	1, Link 1, 6 Lane 7
Q	1x16 Option E	1x16,1x8,1x4,1x2,1x1 1x16 Option B 2x8,2x4,2x2,2x1	0b0 101	1 Host	1 Upstream Socket	1 or 2 Links	00090	1x16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, L Lane 6	Link O, L Lane 7 L	Link O, L Lane 8 L	Link O, L	Link 0, L	Link O, Li Lane 11 La	Link O, Lin Lane 12 Lan	Link 0, Link 0, Lane 13 Lane 14	0, Link 0, 14 Lane 15
û	1x16 Option C	1x16,1x6,1x4 2x8,2x4,2x2,2x1 1x16 Option C 4x4,4x2,4x1	000100	1Host	1 Upotream Socket	1 or 2 Links	00000	1x16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link 0, Lane 5	Link 0, Lane 6	Link O, L Lane 7 L	Link 0, L Lane 8 L	Link 0, L	Link O, L	Link O, Link Lane 11 La	Link O, Lin Lane 12 Lan	Link 0, Link 0, Lane 13 Lane 14	0, Link 0, 14 Lane 15
Q.	4 ×4	4 x4, 4 x2, 4 x1	050 011	1 Host	1 Upstream Socket	1 or 2 Links	00090	2×4*	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3					Link 2, L Lane 0 L	Link 2, Li Lane 1 L	Link 2, Li Lane 2 Li	Link 2, Lane 3			
RSVD	RSVD	RSVD	000010	1Host	1 Upstream Socket	1 or 2 Links	00090																
RSVD RSVD	RSVD	RSVD	000001	1Host		1 or 2 Links	00090																
RSVD RSVD	RSVD	BSVD	0P0 00	Hoose	Alle services of the		00000																l



Table 25: Bifurcation for Single Host, Single Socket and Single/Dual/Quad Upstream Links (BIF[2:0]#=0b000)

4 M.						1x16, 1x8, 1x4, 1x2, 1																		
Cond Short Modes	Single Ho	vet Single Hos	tream Socket Ope Two or Four I	Instroom Links		2 x8, 2 x4, 2 x2, 2 x1 4 x4, 4 x2, 4 x1																		
Card Short Medical Difference Card No. Card Short Card Short Card No. Card		and all the con-	Service of the servic							-	-	-	-	ŀ	-	ŀ				ŀ	ŀ		ŀ	T
	ا ا	Card Short	Modes	Encoding				BIF[2:0]	1	•									9		9	9	-	٠
1.05 1.04 1.02 1.14 1.02 1.14 1.02	e III	Man December	Control No. December	#fo:cla	+	Upstream Devices	4 0 av 4 links	00000	Resulting Link	200	2	7 2	2				2	Lane O Lane J Lane IO Lane II Lane IZ Lane IS Lane I4 Lane IS	Labe 10		3 age	2 2	-	
145 145, 142, 143 141 142 141 14	ш	MOCEICEGIC	Cald Not Flesciit		1001	I Operi calli socuer	1, 2, 01 + LIIInv	00000		4	+	+	+	4	+	+				İ	l			
144, 142, 141 October 15, or 4 Links October	S		1x8,1x4,1x2,1x1	0P1 110	1Host	1 Upstream Socket	1, 2, or 4 Links	00090		Link 0, Lane 0	Link 0, Lin Lane 1 La	Link O, Link Lane 2 Lan	Link 0, Link 0, Lane 3 Lane 4	0, Link 0,), Link 0, 5 Lane 6	Link 0. 5 Lane 7								
142 142 141 142 141 141 141 141 141 141 141 141 142	ş	3	1x4,1x2,1x1	0b1 110	1Host	1 Upstream Socket	1, 2, or 4 Links	00090		Link O.	Link O, Lin	Link O, Link	Link 0,											
142, 141 141 142, 141 142, 141 142, 141 142, 141 142, 141 142, 141 142, 141 142, 141 142, 141 142, 141 142, 141 142, 141 142, 141 142, 141 142, 141 142, 141 142, 141 143	3	**				7			ı	4	+	+	2		+					İ	l			
147 148	8	1x2	1x2,1x1	0P1 110	1Host		1, 2, or 4 Links	00090		Link 0, Lane 0	Link 0, Lane 1													
150 Deficion 105, 154. 12.1 Obt Ob	28	1×1	1x1	0b1 110	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090		Link 0, Lane 0														
1.6 Option B 2.6.2 44, 22.4.2.4.4. 2.6.0 Option B 2.6.4.2.4.2.4.4.4. 2.6.0 Option B 2.6.4.2.4.2.4.4.4.4.4.4.4.4.4.4.4.4.4.4.			1x8,1x4,1x2,1x1	0b1 101	1 Host	1 Upstream Socket	1, 2, or 4 Links	00000		Link O,	Link O, Lin	Link O, Link	Link O, Link O,	0, Link 0,), Link O,	Link O,								
2.80 Options 2.45 24.2 2.2 4.	S	1x8 Option B	3 2x4, 2x2, 2x1					nonan		Lane 0	Lane 1 La	Lane 2 Lan	Lane 3 Lane 4	4 Lane 5	5 Lane 6	5 Lane 7								
14.00 14.0		2 v8 Option B	2 x 8, 2 x 4, 2 x 2, 2 x 1 2 A x 4 A x 2 A x 1	0b1 101	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090		Link 0, L	Link O, Lin	Link O, Link	Link 0, Link 0,	O, Link O,	D. Link O.	Link 0,	Link 1,	Link 1,	Link 1,	Link 1,	Link 1,	Link 1, I	Link 1,	Link 1,
1.86 Option 2.42 Fleet States) 4.41 Obtion 110-prices Societ 12. or 4 Links Obcood 1.86 Option 2.42 Fleet States) 4.41 Obtion 110-prices Societ 12. or 4 Links Obcood 1.86 Option 2.42 2.14 2.44	Т	Tondoor a	1.6 1.4	061100	1 Host	\top	12 or 4 links			٠	+	٠	+	+	+	F			4		٠	+	٠	
1.866 point 1.866 point	ç	1 v8 Option D	2 x4, 4 v2 (First Shape) 4 v1					00000																
116 Option 2 × 6 × 6 × 6 × 6 × 6 × 6 × 6 × 6 × 6 ×	3	10000000	1x16.1x8.1x4	061100	1 Host	1 Upstream Socket	1.2. or 4 Links		T	Link 0.	Link 0. Lin	Link O. Link	Link 0. Link 0.	O. Link O.	Link 0.	Linko	Link 0.	Link 0.	Link 0.	Link 0.	Link 0.	Link 0.	Link 0.	Link 0.
REVO REVO			2x8,2x4,					00090									_	Lane 3	Lane 10	Lane 11				Lane 15
PSYCO PSYC		1x16 Option L	0 4 x4, 4 x2 (First 8 lanes), 4 x1																					
2.44 2.44 2.42 2.41	RSVD	RSVD	RSVD	0b1 011	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090																
RSYD RSYD RSYD Revealed Revealed RSYD	۶	77.0	2 x4, 2 x2, 2 x1	051 010	1 Host		1, 2, or 4 Links	00090		Link O. L	Link O, Lin	Link O, Link	Link 0, Link 1,	t Link t	Link1	Link 1,								
1875 1875	0.00	0,00	2 0 17 7000	ı				00000		+	+	+	٠	+	+	٠				İ	t	t	t	I
1456 1454, 145, 144, 142, 141 141 141 141 141 142 144 142 143	HSVD HSVD	RSVD	RSVD for future x8 encoding	061000	1 Host	1 Upstream Socket	1, 2, or 4 Links	00000						+	+	1	1			Ť	t	t	t	
1.16 2.16 2.14 2.12 2.1 0.00110 110-st 11.0-st 0.00010 1.2 0.14 Links 0.00010 1.2 0.00110 1.2 0.04 Links 0.00010 0.00010 1.2 0.04 Links 0.00010 0.00010 1.2 0.04 Links 0.00010 0			1x16,1x8,1x4,1x2,1x1	050111	1 Host	П	1, 2, or 4 Links	00000	r	Link 0,	Link O, Lin	Link O, Link	Link O, Link O,	0, Link 0,), Link 0,	Link 0,	Link 0,	Link 0,	Link 0,	Link 0,	Link 0,	Link 0,	Link 0,	Link 0,
2.86 Delites A 2.2.2 x1 0.00100	ş	1×16						nonan			Lane 1 La	Lane 2 Lan	Lane 3 Lane 4	4 Lane 5	5 Lane 6	5 Lane 7	Lane 8	Lane 3	Lane 10	Lane 11	Lane 12	Lane 13 L	Lane 14	Lane 15
1145 Option E 248 244 22 131 Ob0100		2 x8 Option A		000110	1Host		1, 2, or 4 Links	00090		Link 0, L	Link O, Lin	Link O, Link Lane 2 Lan	Link O, Link O, Lane 3 Lane 4	O, Linko, 4 Lane 5), Link 0, 5 Lane 6	Link 0, 5 Lane 7	Link 1,	Link 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, L	Link 1, Lane 6	Link 1, Lane 7
1456 Debica B 26 244, 242, 241 1456 TH 245 Debica B 26 244, 242, 241 1456 Debica B 26 244, 242, 241 1456 Debica B 244, 242, 241 1456 Debica B 244, 242, 241 1456 Debica B 244, 242, 241 1456 Debica B 244, 242, 241 1456 Debica B 245 Debica B 250 Debica	Г		-	000101	1 Host	-	1, 2, or 4 Links	00000		⊢	⊢	⊢	H	⊢	⊢	F	H	Link 0,	Link 0,	Link 0,	Link 0,	⊢	\vdash	Link 0,
18th 1.65 1.45 18th 1.45 18th 1.65 1.45 18th 1.65 1.45 18th 1.65 1.45 18th 1.65	Ç	1x16 Option E	5 2 x8, 2 x4, 2 x2, 2 x1					00000			Lane 1 La	Lane 2 Lan	Lane 3 Lane 4	4 Lane 5	5 Lane 6	5 Lane 7	Lane 8	Lone 3	Lane 10	Lane 11	Lane 12			Lane 15
1216 Option C			1x16,1x8,1x4	0P01090	1 Host		1, 2, or 4 Links										Link 0,	Link 0,	Link 0,	Link 0,		_		Link 0,
4 x4, 4 x2, 4 x1 000011 1Hour 1Upatream Socket 1,2, or 4 Links 00000 00000 00000 1Hour 1Upatream Socket 12, or 4 Links 00000 00000 00000 1Hour 1Upatream Socket 12, or 4 Links 00000 00000 00000 1Hour 1Upatream Socket 12, or 4 Links 00000 00000 00000 00000 1Hour 1Upatream Socket 12, or 4 Links 00000 00000 00000 00000 00000 00000 0000		1x16 Option C	2x8,2x4,2x2,2x1 3 4x4,4x2,4x1					00000		lane 0	Lane 1 La	Lane 2 Lan	Lane 3 Lane 4	4 Lane 5	2 Lane 6	Lane 7	Lane 8	Lane 3	Lane 10	Lane 11	Lane 12	Lane 13	Lane 14	Lane 15
85'VD 85'VD 80'0000 100'00 10	Г		4 x4, 4 x2, 4 x1	050 011	1 Host	1 Upstream Socket	1, 2, or 4 Links	00000		⊢	⊢	⊢	⊢	\vdash	\vdash	\vdash			Link 2,	Link 2,	Link 3,	Н	\vdash	Link 3,
RSVD 0b0010 1Host 1Uperteam Socket 1,2, or 4 Links 0b000 RSVD 0b0001 1Host 1Uperteam Socket 0,2, or 4 Links 0b000 Ob000 Ob	Ç	4 ×4				╗				Lane 0	Lane 1 La	Lane 2 Lan	Lane 3 Lane 0	0 Lane 1	1 Lane 2	Lane 3	Lane 0	Lane 1	Lone 2	Lane 3	Lone 0	Lane 1	Lane 2	Lone 3
RSVD 0b0001 1Host 1Upstream Socket 1,2, or 4 Links	RSVD	RSVD	RSVD	00000	1 Host	7	1, 2, or 4 Links	00090																
	RSVD	RSVD	RSVD		Hoot	\neg	1, 2, or 4 Links	00000						+	+	-					1			
HSVD UDOUGO THOSE TOPACTES Socket 1, 2, or 4 Links	RSVD	RsvD	RsvD		1 Host	1 Upstream Socket	1, 2, or 4 Links	00000																

Table 26: Bifurcation for Single Host, Dual Sockets and Dual Upstream Links
(BIF[2:0]#=0b001)

. T #	Card Stort Modes Supported Bifercation	Additional And Additional And Additional And Additional And Additional And And And And And And And And And And		Upstream Devices 2 Upstream Sockets 2 Upstream Sockets	•	BIF[2:0]			H						-	L			ŀ	ŀ	
20 118 Option D	Cond Not Present 156, 154, 152, 151 156, 154, 152, 151 152, 151 152, 151 152, 151 152, 151 153, 154, 152, 251 156, 154, 252, 251 256, 254, 252, 251 256, 254, 252, 251 256, 254, 252, 251 256, 254, 252, 251 256, 254, 252, 251 256, 254, 252, 251 256, 254, 252, 251 256, 254, 252, 251 256, 254, 252, 251 256, 254, 252, 251 256, 254, 252, 251 256, 254, 252, 251 256, 254, 252, 251 256, 254, 252, 251 256, 254, 252, 252 256, 252, 252	06:1100		2 Upstream Sockets	- 4	•					-	7	9			-	<u> </u>	0			-
	114, 114, 114, 114, 114, 114, 114, 114,	0b:1110 0b:1110 0b:1110 0b:1101 0b:1001		2 Upstream Sockets	2 Links	00001															
	194, 192, 191 192, 191 192, 191 193, 194, 192, 191 194, 192, 201 194, 201 194	0b:1110 0b:1110 0b:1101 0b:1101	Thost Thost		2 Links		1x8	Link 0.	Link O. Li	Link O.	Link O. Lin	Link O, Link O,	O, Link O.	C. Link O.							t
	154, 152, 151 152, 151 151 152, 151 153, 154, 152, 151 155, 154, 252, 251 155, 154, 452, 451 254, 452, 451 254, 452, 451 254, 452, 451	0b:1110 0b:1110 0b:1101 0b:1100	1 Hogt 1 H			00001	(Socket 0 only)	Lane 0	\dashv	$\overline{}$	\rightarrow	\dashv	\dashv	\dashv							
	114.141 114.142.141 114.142.141 114.142.241 114.45.241 114.45.241 114.45.241 115.144 115.144 115.144 115.144 114.145.441	06:1100 06:1101 06:1101 06:1100	1Host 1Host	2 Upstream Sockets	2 Links	009001	1x4 (Socket 0 only)	Link 0,	Link O, Li	Link 0, Li	Link 0,										
	1x1 1x2 1x4, x2, x1 2x4, 2x2, 2x1 2x6, 2x4, 2x2, 2x1 1x6, 1x4 1x6, 1x4 2x4, x2, 4x1 1x6, 1x4 2x4, x2, 4x1 1x6, 1x4 2x4, x2, 4x2 first blasses 4x1	0b1110 0b1101 0b1100	1 Host	2 Upstream Sockets	2 Links	00001	1x2	Link 0,	Н	-											
	1x1 1x8,1x4,1x2,1x1 128,1x4,1x2,1x1 2x6,2x4,2x2,2x1 2x6,2x4,2x2,2x1 1x6,1x4 1x6,1x4 1x6,1x4 1x6,1x4 1x6,1x4 1x6,1x4 1x6,1x4 1x6,1x4 1x6,1x4	0b/1101 0b/1101 0b/1100	1Host				(Socket 0 only)	Lane 0	Lane 1												
	1x6,1x4,1x2,1x1 2 xx4,2x2,2x1 2 xx4,2x2,2x1 B 4 xx4,4x2,4x1 1x6,1x4 1x6,1x4 2 xx4, 2 xx4, 2 xx4,	06/101	1 Host	2 Upstream Sockets	2 Links	009001	1x1 (Socket 0 only)	Link 0, Lane 0													
	2x8,2x4,2x2,2x1 3 4x4,4x2,4x1 1x8,1x4 2x4, 2x4, 0 4x2 (First Share),4x1	061101		2 Upstream Sockets	2 Links	00001	1x8 (Socket Donlin)	Link 0, Lanc 0	Link O, Li	Link O, Li	Link O, Lin	Link O, Link	Link 0, Link 0, Lanc 5 Lanc 6), Link 0, 6 Lanc 7							
	1x8,1x4 2x4, 2 4x2 (First 8 lanes), 4 x1	061100	1005	2 Upstream Sockets	2 Links	00001	2 x8	Link 0,	\vdash	-	+	+	+	-	Link 1	Link 1	Link 1,	Link 1,	Link 1,	Link 1,	Link 1, Link 1,
	2 x4, 0 4 x2 (First 8 lanes), 4 x1		1 Host	2 Unstream Sockets	2 Links		1.08	Linko	+	+	+	+	+	Ŧ	٠	+	+	C alle	+ olle	+	+
						10090	(Socket 0 only)	Lane 0													
	1x16,1x8,1x4	0b1100	1 Host	2 Upstream Sockets	2 Links		2 x8	Link 0,	Н	Н	Н	H	Н	_		H	⊢	Link 1,	Link 1,	Н	⊢
4C 1x16 Option E	2 x8, 2 x4, 1 x16 Option D 4 x4, 4 x2 (First 8 lanes), 4 x1					00001		Lane 0	Lane 1	Lane 2	Lane 3 Lan	Lane 4 Lan	Lane 5 Lane 6	6 Lane 7	Lane 0	Lane 1	Lane 5	Lane 3	Lane 4	Lane 5	Lane 6 Lane 7
RSVD RSVD	RSVD	061 011	1 Host	2 Upstream Sockets	2 Links	00001															
2C 2x4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1 010	1 Host	2 Upstream Sockets	2 Links	00001	1x4 (Socket 0 only)	Link 0, Lane 0	Link 0, Li Lane 1 L:	Link O, Li Lane 2 Lt	Link O, Lane 3										
RSVD RSVD	RSVD for future x8 encoding	0b1 001	1 Host	2 Upstream Sockets	2 Links	00001															
RSVD RSVD	RSVD for future x8 encoding	001000	1Host	2 Upstream Sockets	2 Links	00001															
4C 1x16	1x16,1x8,1x4,1x2,1x1	050111	1 Host	2 Upstream Sockets	2 Links	00001	1x8 (Socket 0 only)	Link 0, Lane 0	Link O, Li Lane 1 L:	Link O, Li Lane 2 L:	Link O, Lin Lane 3 Lan	Link O, Link O, Lane 4 Lane 5	Link O, Link O, Lane 5 Lane 6	0, Link 0, 6 Lane 7							
4C 2x8 Option A	2 x8, 2 x4, 2 x2, 2 x1	000110	1 Host	2 Upstream Sockets	2 Links	00001	2 x8	Link 0, Lane 0	Link O, Li Lane 1 L:	Link O, Li Lane 2 L:	Link O, Lin Lane 3 Lan	Link 0, Link 0, Lane 4 Lane 5	Link O, Link O, Lane 5 Lane 6	0, Link 0, 6 Lane 7	Link 1,	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Link 1, Lane 6 Lane 7
4C 1x16 Option E	1x16 Option B 2x8, 2x4, 2x2, 2x1	000101	1 Host	2 Upstream Sockets	2 Links	00001	2 x8	Link 0, Lane 0	Link O, Li Lane 1 L:	Link O, Li Lane 2 L:	Link O, Lin Lane 3 Lan	Link O, Link O, Lane 4 Lane 5	Link O, Link O, Lane 5 Lane 6	0, Link 0, 6 Lane 7	Link1,	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Link 1, Lane 6 Lane 7
4C 1x16 Option C	1x16,1x8,1x4 2x8,2x4,2x2,2x1 1x16 Option C 4x4,4x2,4x1	000100	1 Host	2 Upotream Sockets	2 Links	00001	2 x8	Link 0, Lane 0	Link O, Li Lane 1 Li	Link O, Li Lane 2 Lr	Link O, Lin Lane 3 Lan	Link O, Link Lane 4 Lan	Link O, Link O, Lane 5 Lane 6), Link 0, 6 Lane 7	Link 1,	Link 1, Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Link 1, Lane 6 Lane 7
4C 4×4	4 x4, 4 x2, 4 x1	060011	1 Host	2 Upstream Sockets	2 Links	00000	2 x4 (EP 0 and 2 only)	Link 0, Lane 0	Link O, Li Lane 1 Lt	Link O, Li Lane 2 Lt	Link 0, Lane 3				Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3			
RSVD RSVD	RSVD	000000	1 Host	2 Upstream Sockets	2 Links	00001															
RSVD RSVD	RSVD	000 001		2 Upstream Sockets	2 Links	00001															
RSVD RSVD	RSVD	000000	1 Host	2 Upstream Sockets	2 Links	009001															



Table 27: Bifurcation for Single Host, Four Sockets and Dual Upstream Links (BIF[2:0]#=0b010)

Single H	ost, Four Upstra	Single Host, Four Upstream Sockets, Four Upstream Links	يو		4 x4, 4 x2, 4x1																		
Card Side	Min Suppor Card Card Short Modes Width Name	Supported Bifurcation Modes	Add-in-Card Encoding PBSMTBf3:01#	Host	Upstream Devices	Upstream	BIF[2:0]	Receiting Link Jane 1 Jane 2 Jane 3 Jane 4 Jane 5 Jane 7 Jane 8 Jane 10 Jane 11 Jane 12 Jane 13 Jane 14 Jane 15 Jane 14 Jane 15 Jane 16 Jane 17 Jane 16 Jane 17 Jane 17 Jane 18 Jane 17 Jane 18 Jane 17 Jane 18 Jane 1	0 46	l age	2	3	4 900	1	9 6 6	7	8 94	6	10		12	13	7
c/u	Not Present	Card Not Present	0b1 111	1 Host	4 Upstream Sockets	4 Links	05010																
		1x8,1x4,1x2,1x1	0b1 110	1 Host	4 Upstream Sockets	4 Links	00000	1×4	Link 0,	Link 0,	Link 0,	Link 0,											
S S	1x8							(Socket 0 only)	Lone 0	Lane 1	-	Lane 3								+			$\frac{1}{1}$
28	1×4	1x4,1x2,1x1	0P1 110	1Host	4 Upstream Sockets	4 Links	00000	1x4 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3										_	_
S S	1x2	1x2,1x1	0b1 110	1 Host	4 Upstream Sockets	4 Links	05010	1x2 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1													
S S	ž	1x1	0b1 110	1 Host	4 Upstream Sockets	4 Links	05010	1x1 (Socket 0 only)	Link 0, Lane 0														
ပ္လ	1x8 Option B	1x8,1x4,1x2,1x1 1x8 Option B 2x4,2x2,2x1	0b1 101	1 Host	4 Upstream Sockets	4 Links	0090	2 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lanc 2	Link 0, Lane 3	Link 1, Lane 0	Link 1,	Link 1, Li Lane 2 Li	Link 1, Lane 3							
9	2 x8 Option B	2 x8,2 x4,2 x2,2 x1 2 x8 Option B 4 x4, 4 x2, 4 x1	0b11 01	1 Host	4 Upstream Sockets	4 Links	00000	\$ × \$	Link 0, Lane 0		-		\vdash	Link 1,	\vdash	Link 1, L	Link 2, L	Link 2, Li	Link 2, Link 2, Link 2	Link 2, Lii Lane 3 La	Link 3, Li	Link 3, Lin	Link 3, Link 3, Lane 2 Lane 3
		1x8,1x4	0b1100	1 Host	4 Upstream Sockets	4 Links		2 x4	Link 0,	Link 0,	\vdash	Н	⊢	+	+	Н	Н	Н	Н	\vdash	⊢	Н	\vdash
ပ္လ	1x8 Option D	2 x4, 1x8 Option D 4 x2 (First 8 lancs), 4 x1					00000		Lane 0	Lane 1	Lane 2	Lane 3	Lone 0	Lane 1	Lane 2	Lane 3						_	_
		1x16,1x8,1x4	0b1100	1 Host	4 Upstream Sockets	4 Links		\$ x \$	Link 0,	Link 0,	Н		⊢	Н	Н				-		Н	Н	Н
ð.	1x16 Option D	2 x 8, 2 x 4, 1 x 16 Option D 4 x 4, 4 x 2 (First 8 lanes), 4 x 1					00010		Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	lane 2 lane 3
RSVD	RSVD RSVD	RSVD	0b1 011	1Host	4 Upstream Sockets	4 Links	00000																
ړ	Pr-0	2 x4, 2 x2, 2 x1 1 x4 1 x2 1 x1	0b1 010	1 Host	4 Upstream Sockets	4 Links	00000	2×4	Link 0,	Link 0, Land 1	Link 0,	Link 0,	Link 1,	Link 1,	Link 1, Li	Link 1, Land 3							
0//00	Devin Devin	DOVO for future v8 according Obtions	061001	1 Hoer	A Unchrosm Sockate	Alisha	05040				4	۰		٠	٠			-		ł	+		ł
RSVD	RSVD RSVD	RSVD for future x8 encoding	061000	1Host	4 Upstream Sockets	4 Links	00000																
1	1×16	1x16,1x8,1x4,1x2,1x1	050111	1 Host	4 Upstream Sockets	4 Links	01040	1x4 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3											
ů,	2 x8 Option A	2x8,2x4,2x2,2x1	000110	1 Host	4 Upstream Sockets	4 Links	0090	2 x4 (Socket 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3					Link 2, L Lane 0 L	Link 2, Li Lane 1 La	Link2, Li Lane 2 La	Link 2, Lane 3			
ĝ	1x16 Option B	1x16,1x6,1x4,1x2,1x1 1x16 Option B 2x8,2x4,2x2,2x1	000101	1Host	4 Upstream Sockets	4 Links	00000	2 x4 (Socket 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3					Link 2, L Lane 0 L	Link 2, Li Lane 1 Ls	Link 2, Li Lane 2 La	Link 2, Lane 3			
ů	1x16 Option C	1x16,1x8,1x4 2x8,2x4,2x2,2x1 1x16 Option C 4x4,4x2,4x1	0001000	1Host	4 Upstream Sockets	4 Links	00010	4 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1,	Link 1, Lane 2 L:	Link 1, L Lane 3 L	Link 2, L Lane 0 L	Link 2, Li Lane 1 La	Link 2, Lii Lane 2 La	Link 2, Lin Lane 3 La	Link 3, Li Lane 0 Li	Link 3, Lin Lane 1 Lar	Link 3, Link 3, Lane 2 Lane 3
å	\$x \$	4x4,4x2,4x1	000011	1Host	4 Upstream Sockets	4 Links	00000	4 ×4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, Lane 1	Link 1, Li Lane 2 Li	Link 1, L Lane 3 L	Link 2, L Lane 0 L	Link 2, Li Lane 1 Ls	Link2, Li Lane2 La	Link 2, Lin Lane 3 La	Link 3, Li Lane 0 L	Link 3, Lin Lane 1 Lar	Link 3, Link 3, Lane 2 Lane 3
RSVD RSVD	RSVD	RSVD	000010	1Host		4 Links	0000																
RSVD	RSVD RSVD	RSVD	000 001	1Host		4 Links	0000																
RSVD	RSVD RSVD	RSVD	000000	1Host	4 Upstream Sockets	4 Links	00000		ĺ														

Table 28: Bifurcation for Dual Host, Dual Sockets and Dual Upstream Links (BIF[2:0]#=0b101)

1.00 1.00				2x8,2x4,2x2,2x1																		
1x6 1x6 1x8 1x8 1x8 1x8 1x8 1x8 1x8 1x8 1x8 1x8	Supported Bifurcation Modes	Add-in-Card Encoding PRSNTB[3:0]#	Host	Upstream Devices	Upstream	BIF[2:0]	Resulting Link	Lane 0	Lanc 0 Lane 1 Lane 2 Lane 3 Lane 4 Lane 5	ane 2 L:	ne 3 La	1 to 1	ne 5 Lan	Lane 6 Lane	7 Lane	8 Lane	Lane 7 Lane 8 Lane 9 Lane 10 Lane 12 Lane 13 Lane 14 Lane 15	Lane 11	Lane 12	Lane 13	38e 14	ane 15
1x6 1x2 1x2 1x2 1x8 1x8 1x8 Option B 1x8 Opt	Card Not Present				2 Links	06101																
1x4 1x2 1x1 1x1 1x1 1x8 Option B 2x8 Option B 1x8 Option B 1x8 Option D 1x8 Option	1x8,1x4,1x2,1x1	0P1 110	2 Host		2 Links	10140	1x8 (Host 0 only)	Link 0, Lane 0	Link O, L	Link O, L	Linko, Li Lane 3	Link O, Li	Link O, Lin Lanc 5 Lar	Link 0, Link 0, Lanc 6 Lanc 7	o r-							
1x1 1x1 1x2 1x6 Option B 2 x6 Option B 1x8 Option D 1x6 Option D 1x8 Option D 1x8 Option D 1x8 Option D 1x8 Option D 1x8 Option D 1x8 Option D 1x8 Option D 1x8 Option D 1x8 Option D 1x8 Option D 1x8 Option D 1x8 Option D	1x4, 1x2, 1x1	0P1 110	2 Host	2 Upstream Sockets	2 Links	10140	1x4 (Host 0 only)	-	-	-			_									
1x1 1x6 Option B 2 x6 Option B 1x6 Option D 1x6 Option D 1x6 Option D 1x76 Option D 1x	1x2,1x1	0b1110	2 Host	2 Upstream Sockets	2 Links	10140	1x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1													
1x6 Option B 2 x6 Option B 1x8 Option D 1x8		0b1 110	2 Host	2 Upstream Sockets	2 Links	10140	1x1 (Host 0 only)	Link 0, Lane 0														
2 x8 Option B 1x8 Option D 1x8 Option D 1x16	x8,1x4,1x2,1x1 2x4,2x2,2x1	0b1 101	2 Host	2 Upstream Sockets	2 Links	10140	1x8 (Host 0 only)		Link 0, L Lane 1 L	Link O, L Lane 2 L	Link O, Li Lane 3 L:	Link O, Li Lane 4 L:	Link O, Lin Lane 5 Lar	Link O, Link O, Lane 6 Lane 7	o ~							
1x6 Option D 1x16 Option D 1 RSVD 1 RSVD 1 RSVD 1 RSVD 1 RSVD 1 RSVD	2x8,2x4,2x2,2x1 4x4,4x2,4x1	0b1 101	2 Host	2 Upstream Sockets	2 Links	0b101	2×8	Link 0, Lane 0	Link O, L	Link O, L Lane 2 L	Link O, Li Lane 3 L:	Link O, Li Lane 4 L:	Link O, Lin Lane 5 Lar	Link O, Link O, Lane 6 Lane 7	0, Link1,	1. Link 1, 0 Lane 1	t Link t, 1 Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
1x16 Option D RSVD	1x8,1x4 2x4, 1x8 Option D 4x2 (First 8 lanes), 4x1	061 100	2 Host	2 Upstream Sockets	2 Links	06101	1x8 (Host 0 only)	Link 0, Lane 0	Link 0, L Lane 1	Link 0, Lane 2	Link O, Li Lane 3 L;	Link 0, Li Lane 4 L:	Link O, Lin Lane 5 Lar	Link O, Link O, Lane 6 Lane 7	° €							
2 x4 10 RSVD 10 RSVD 11x16	1x16,1x8,1x4 2x8,2x4, 1x16 Option D 4x4,4x2 (First 8 lanes),4x1	0b1100	2 Host	2 Upstream Sockets	2 Links	06101	85 × 63	Link 0, Lane 0	Link O, L Lane 1 L	Link 0, Lane 2	Link O, Li Lane 3 L;	Link O, Li	Link O, Lin Lane 5 Lar	Link O, Link O, Lane 6 Lane 7	0, Link 1,	1, Link 1, 0 Lane 1	1. Link 1, 1. Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
2 x4 70 RSVD 70 RSVD 1 x16	0	0b1 011	2 Host	2 Upstream Sockets	2 Links	0b101																
70 RSVD 1x16	2x4,2x2,2x1 1x4,1x2,1x1	061 010	2 Host	2 Upstream Sockets	2 Links	0b101	1x4 (Host 0 only)	Link 0, Lane 0	Link O, L	Link O, L Lane 2 L	Link 0, Lane 3											
1x16	BSVD for future x8 encoding BSVD for future x8 encoding	061 001	2 Host	2 Upstream Sockets 2 Hostream Sockets	2 Links	06101																
	1x16,1x8,1x4,1x2,1x1	060111	2 Host	2 Upstream Sockets	2 Links	10140	1x8 (Host 0 only)	Link 0, Lane 0	Link O, L	Link O, L	Link O, Li Lane 3 L:	Link O, Li	Link O, Lin Lane 5 Lar	Link 0, Link 0, Lanc 6 Lanc 7	o 1-							
4C 2 x8 Option A	2 x8, 2 x4, 2 x2, 2 x1	000110	2 Host	2 Upstream Sockets	2 Links	10140	2 x8	Link 0, Lane 0	Link O, L	Link O, L	Link O, Li Lane 3 L;	Link O, Li Lane 4 L:	Link O, Lin Lane 5 Lar	Link 0, Link 0, Lane 6 Lane 7	0, Link 1,	1, Link 1, 0 Lane 1	1, Link 1, 1 Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lanc 6	Link 1, Lane 7
1x16,1x8,1x4,1x2, 4C 1x16 Option B 2x8,2x4,2x2,2x1	1x16, 1x8, 1x4, 1x2, 1x1 2x8, 2x4, 2x2, 2x1	000101	2 Host	2 Upstream Sockets	2 Links	10140	2 x8	Link 0, Lane 0	Link O, L	Link O, L Lane 2 L	Link O, Li Lane 3 L:	Link O, Li Lane 4 L:	Link O, Lin Lane 5 Lar	Link O, Link O, Lane 6 Lane 7	0, Link 1,	1 Link 1, 0 Lane 1	1, Link 1, 1 Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
1x16,1x8,1x4 2x8,2x4,2x2 4C 1x16 Option C 4x4,4x2,4x1	1x16,1x8,1x4 2x8,2x4,2x2,2x1 4x4,4x2,4x1	000100	2 Host	2 Upstream Sockets	2 Links	10140	2 x8	Link 0, Lane 0	Link O, L Lane 1 L	Link O, L	Link O, Li Lane 3 L:	Link O, Li Lane 4 L:	Link O, Lin Lane 5 Lar	Link O, Link O, Lane 6 Lane 7	0, Link 1, 17 Lane 0	1, Link 1, 0 Lane 1	1, Link 1, 1 Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
×đ	4 x4, 4 x2, 4 x1		2 Host	2 Upstream Sockets	2 Links	10140	2 x4 (EP 0 and 2 only)	Link 0, Lane 0	Link O, L Lane 1 L	Link O, L Lane 2 L	Link 0, Lane 3				Link 1, Lane 0	1, Link 1, 0 Lane 1	1, Link 1, 1 Lane 2	Link 1, Lane 3				
		0P0 010	2 Host		2 Links	0b101																
			2 Hoot	- 1	2 Links	0b101																
RSVD RSVD RSVD	Q	000000	2 Host	2 Upstream Sockets	2 Links	0b101																



Table 29: Bifurcation for Quad Host, Quad Sockets and Quad Upstream Links (BIF[2:0]#=0b110)

Mia Card Card S Vidth Name		55			1 Y 4 YE' 4 YE'																		
	Min Suppor	ted Bifurcation	Add-in-Card Encoding			Upstream	BIF[2:0]						-		,		,						
L	Not Present	Card Not Present	061111	4 Host	4 Host 4 Unstream Sockets	4 Links	09440	Mesuring Line Lane U			7 200	Take I Take 2 Take 3 Take 4 Take 0 Take 0 Take 0 Take 10 Take 11 Take 12 Take 13 Take 14 Take 15 Take 15 Take 15		200	0		0	2			7	2	
_		_		4 Host	4 Upstream Sockets	4 Links	08.40	1×4	Link 0,	Link 0,	Link 0,	Link 0,						ŀ	H	-	H	-	ļ
20	1x8						OLI OLI	(Host 0 only)	Lone 0	Lane 1	\dashv	Lane 3											
S	1×4	1x4,1x2,1x1	0b1 110	4 Host	4 Upstream Sockets	4 Links	01140	1x4 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3											
S	1x2	1x2,1x1	0b1 110	4 Host	4 Upstream Sockets	4 Links	0110	1x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1													
200	1x1	1x1	0b1 110	4 Host	4 Upstream Sockets	4 Links	01140	1x1 (Host 0 only)	Link 0, Lane 0														
20	x8 Option B	1x8,1x4,1x2,1x1 1x8 Option B 2x4,2x2,2x1	0b1 101	4 Host	4 Upstream Sockets	4 Links	01140	2 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, L	Link1, L Lane 0 L	Link 1, Li Lane 1 Li	Link 1, Li Lane 2 La	Link 1, Lane 3							
	x8 Option B	2 x 8, 2 x 4, 2 x 2, 2 x 1 2 x 8 Option B 4 x 4, 4 x 2, 4 x 1	061101	4 Host	4 Upstream Sockets	4 Links	01140	4 ×4	Link 0, Lane 0	Link 0, Lane 1	-	Link O, L	Link 1, L	Link 1, Li Lane 1 L:	Link 1, Lii Lane 2 La	Link 1, Lin Lane 3 La	Link 2, Lin Lane 0 La	Link 2, Lin Lane 1 La	Link 2, Link Lane 2 Lan	Link 2, Link 3, Lane 3 Lane 0	3, Link 3, s 0 Lane 1	3, Link 3,	Link3, Lane3
		1x8,1x4	001100	4 Host	4 Upstream Sockets	4 Links		2×4	Link 0,	Link 0,	-		\vdash	\vdash	\vdash		-		-	-	-	-	Н
8	x8 Option D	2 x4, 1x8 Option D 4 x2 (First 8 lanes), 4 x1					0P410		Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	lane 2	Lane 3			_	_	_	_	_
		1x16,1x8,1x4	0b11 00	4 Host	4 Upstream Sockets	4 Links		4 × 4	Link 0,	Н	⊢		⊢	⊢	⊢		H	Н	Н		Н	Н	Н
40 1	:16 Option D	2x8, 2x4, 1x16 Option D 4x4, 4x2 (First 8 lancs), 4x1					08110		Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	el Sonel	Lane 3	lane 0	Lane 1 La	Lane 2 Lan	Lane 3 Lane 0	Lane 1	- Lane 2	Lane 3
I	G/S		0b1 011	4 Host	4 Upstream Sockets	4 Links	06110												_				
٥	20.4	2 x4, 2 x2, 2 x1	051 010	4 Host	4 Upstream Sockets	4 Links	0P410	2×4	Link 0,	Link 0,	Link 0,	Link 0, L	Link 1, L	Link 1, Li	Link 1, Li	Link 1,							
e	RSVD	re x8 encodina	0b1 001	4 Host	4 Upstream Sockets	4 Links	06110				۰	٠	+	٠	+			H	H		H	+	ļ
RSVD RSVD	SVD	RSVD for future x8 encoding	0b1 000	4 Host		4 Links	09410												H		H		L
9	1×16	1x16,1x8,1x4,1x2,1x1	060111	4 Host	4 Upstream Sockets	4 Links	01140	1x4 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3											
 0	2 x8 Option A	2 x8, 2 x4, 2 x2, 2 x1	000110	4 Host	4 Upstream Sockets	4 Links	01140	2 x4 (Host 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3				= <u>\$</u>	Link 1, Lin Lane 0 La	Link 1, Lir Lane 1 Lau	Link 1, Link 1, Lane 2 Lane 3	k1.			
	1000	1x16,1x6,1x4,1x2,1x1	000101	4 Host	4 Upstream Sockets	4 Links	0110	2×4	Link 0,	Link O,	\vdash	Link 0,				3	-	\vdash		e			
	a notion of	2x6,2x4,2x2,2x1	000100	4 Host	4 Upstream Sockets	4 Links	06110	(nost u & z only) 4 x 4	Link 0,	Link 0,	Link 0, Lane 2	Link 0, L	Link 1, L	Link 1, Li Lane 1 Li	Link 1, Li Lane 2 La	Link 1, Lin Lane 3 La	Link 2, Lin Lane 0 La	Link 2, Lin Lane 1 La	Link 2, Link Lane 2 Lan	Link 2, Link 3, Lanc 3 Lanc 0	3, Link 3, s 0 Lane 1	3, Link 3,	Link 3, Lane 3
<u>-</u> ي	x16 Option C	1x16 Option C 4x4, 4x2, 4x1 4x4, 4x2, 4x1	000011	4 Host	4 Upstream Sockets	4 Links	00,440	4 × 4	Link 0,	Link 0,	-	Link 0,	Link 1,	Link 1, Li	Link 1, Li	Link 1, Lin	Link 2, Lin	Link 2, Lin	Link 2, Link	Link 2, Link 3,	3, Link3,	3, Link 3,	Link 3,
ç	×¢						2100		Lane 0	Lane 1	Lane 2	_	Lane 0 L	Lane 1 Lt	Lane 2 La	Lane 3 La	_	Lane 1 La	_	Lane 3 Lane 0	a Lane 1	1 Lane 2	2 Lane 3
RSVD RSVD		RSVD		4 Host	4 Host 4 Upstream Sockets	4 Links	0P#0											+	+	+	+	+	1
HSVD HSVD		RSVD	I	4 Host	4 Upstream Sockets	4 Links	000		Ī	ĺ	1			1	1	1	1	+	+	+	+	+	1
RSVD RSVD		RSVD	000000	4 Host	4 Upstream Sockets	4 Links	0P110																

Table 30: Bifurcation for Quad Host, Quad Sockets and Quad Upstream Links (BIF[2:0]#=0b110)

1	22			Ī					T														T				T		Ţ
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	- 5			+				\vdash	+	_				_	H					+		_	+	_			ł		
	- 01			+				H	+			_			H					+		_	+	_			+	H	
	2			1					1						L									_			1		
	1																			Link 1,	Lane 1	Link 1	Lane 1	Land A	į		L		
	Lane 8																			Link 1,	Lane 0	Link 1	Lane 0	Land A	, ,				
	Lane 7										Link 3,	Lane 1	Link 3,	Lane 1													Ī		
İ	9 94 6			Ī					Ī		Link 3,	Lane 0	Link 3,	Lane 0	Ī								T				T		
	200			İ					Ť		Link 2,	Lane 1		Lane 1									Ť			Link 1,	- aue	Ī	
	7			t				T	t		H	Lane 0	⊢	Lane 0						t			†	_		Link 1,	+		
				+				Link 1,	Lane 1	Lane 1		Lane 1		Lane 1	H	Link 1, Lane 1							+	_			1	H	
	2			+				\vdash	+	Link 1, Lane 0 Li	⊢	Lane 0	-	Lane 0		Link 1, Li Lane 0 La				+		_	+	_			ł		
			o ,	= 4	6 T.	o 7		-	+										o •	. 0	-	o .	- 0	5 7		o ·		H	
	20		⊢	+), Link O, 0 Lane 1), Link 0,	-	-	+	Lane 1	H	0 Lane 1	-	0 Lane 1	H), Link 0, 0 Lane 1	H		Link O.	+	\dashv		+	o and), Linko,	+		
	2		Link 0,	n auc n	Link 0, Lane 0	Link 0,	Link 0,		+	Lane 0	Link 0,	Lane 0	Link 0,	Lane 0		Link 0, Lane 0	Н		Link 0,	Link 0,		-	+	5 G		Link 0,	٠		
	Resulting Line 0 Line 1 Line 2 Line 3 Line 4 Line 5 Line 6 Line 6 Line 9 Line 10 Line 11 Line 12 Line 13 Line 15		1x2	Host U only	1x2 (Host 0 only)	1x2 (Host 0 only)	fx1 (Host 0 only)	2 x 5	(Hoot 0 & Lonly)	2 x2 (Host 0 & 1 only)	4 x2		4 x2			2 x 2 (Host 0 & 1 only)			1x2	1x2	(Host 0 & Lonly)	2 × 2	(Host U & Lonly)	A XA (Hoot 0 & Looku)	(d	4 x2	105t U.B. 1 OHINY		
	BIF[2:0]	06111	06111		0b111	0b111	0b111	06111	+	Obtiff [0b111			06111	06111	06111	06111	05111	Objected		06111	7	08444		06111	06111	06111	
	_			1					4			_	L	_			ı	Ш		┺			14.7					ı	
	Upstream	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links		Host 4/8 Upstream Sockets 4 or 8 x2 Links	Host 4/8 Upstream Sockets 4 or 8 x2 Links	Host 4/8 Upstream Sockets 4 or 8 x2 Links	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	0	Host 476 Upstresm Sockets 4 or 6 x2 Links	Host 4/8 Upstream Sockets 4 or 8 x2 Links		Host 4/8 Upstream Sockets 4 or 8 x2 Links		Host 4/8 Upstream Sockets 4 or 8 x2 Links	Host 4/8 Upstream Sockets 4 or 8 x2 Links	\$ or 8 x21	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	t or 8 x2 l	Host 4/8 Upstream Sockets 4 or 8 x2 Links		Host 4/8 Upstream Sockets 4 or 8 x2 Links	0.0	nost 4ro Upstream sockets 4 of 6 xz Links		Host 4/8 Upstream Sockets 4 or 8 x2 Links	t or 8 x21	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	-
	Varices	ockets	ockets		ockets	ockets	ockets	ockets		ockets	ockets		ockets		ockets	ockets	ockets	ockets	ockets	ockets		ockets	1	ockets		ockets	cockets	ockets	- Company
4 x2, 4 x1	Unstream Devices	potream S	potreamS		potreomo	pstream 8	potream S	potream	Ì	potream	potream S		potream S		potream S	pstreams	pstream S	potream S	potreamS	petream		potresm 3	1	potream		potream S	Dotream S	Dotresm S	-
	S S	ot 4/8∪	ot 4/8∪		ot 4780	ot 4/8∪	at 4/8 U	at 4/8 U		76 - 4/8 C	at 4/8∪	_	ot 4/8 U	_	at 4/8∪	34 4/8 U	ot 4/8 U	ot 478 U	ot 4/8∪	34 4/8 U		7 4 78∪	1017	0		at 4/8∪	34 4/8 ∪	A18U	1
	Host	_	4/8 Ho		4/8 Ho	4/8 Ho	4/8 Ho	4/8 Ho	1017	4/8 Ho	4/8 Ho		4/8 Ho		4/8 Ho	478 Ho	4/8 Ho	4/8 Ho	4/8 Ho	4/8 Ho		4/8 Ho	20.0	6 0 0 0		4/8 Ho	4/8 Ho	4/8 Ho	-
stream links	Add-in-Card Encoding PRSNTBf3:01#	Ξ	2		9	10	19	101	3	5	00		001		111	010	100	000	Ξ	110		₫	000000	3		011	000010	00000	
Eight Up:	E A	0b1111	0P1110	- 1	0P1110	0P1110	0P1110	0b11 0 1	3	6	0P1100		0P1100	7		001010	10 0b1001		000111	000110		000 10	9	9		0090	090	090	-
Quad/Oct Host, Four/Eight Upstream Sockets, Four/Eight Upstream links	Supported Bifurcation Add-in-Card Modes Encoding PRSNTBI3:01#	Card Not Present	1x8,1x4,1x2,1x1		1x4,1x2,1x1	1x2,1x1		1x8, 1x4, 1x2, 1x1	1x8 Option B 2x4, 2x2, 2x1	2 x8 Option B 4 x4, 4 x2, 4 x1	1x8,1x4	2 x4, 1 x8 Option D 4 x2 (First 8 lanes), 4 x1	1x16,1x8,1x4	2 x 8, 2 x 4, 1 x 15 Option D 4 x 4, 4 x 2 (First 8 lance) 4 x 1	9	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	RSVD for future x8 encoding	RSVD for future x8 encoding	1x16, 1x8, 1x4, 1x2, 1x1	2 x8, 2 x4, 2 x2, 2 x1		1x16, 1x8, 1x4, 1x2, 1x1	1x16 Option B 2x6, 2x4, 2x2, 2x1	1XIO, 1XO, 1X4 2x8 2x4 2x2 2x4	1x16 Option C 4 x4, 4 x2, 4 x1	4 x4, 4 x2, 4 x1	Q	9	
"/Eight U	E S		-	T			ž	1×8	0 B 2 X	20 A	1×8	2 × 4	1xt	20 O O	RSVD			RS		T		Ž.	z z z	× 3	on C 4 x4	*	RSVD	RSVD	2
t Host, Fou	Min Suppor Card Card Short Modes Width Name	Not Present	,	×	1×4	-	<u> </u>		1x8 Optic	2 x8 Optic		1x8 Optic		1×16 Optic	RSVD RSVD	2 x4	RSV	RSVD RSVD	op. y	OX.	2 x8 Option A		1×16 Upts		1x16 Optiv	3	RSV	RSVD RSVD	200
	Mis Card Vide			ı		1	1		-11								RSVD		1	1	Ī		-1			1	RSVD		ø



3.9 Power Capacity and Power Delivery

There are four permissible power states: AC Power Off, ID Mode, Aux Power Mode (S5), and Main Power Mode (S0). The transition of these states is shown in Figure 29. The max available power envelopes for each of these states are defined in Table 31.

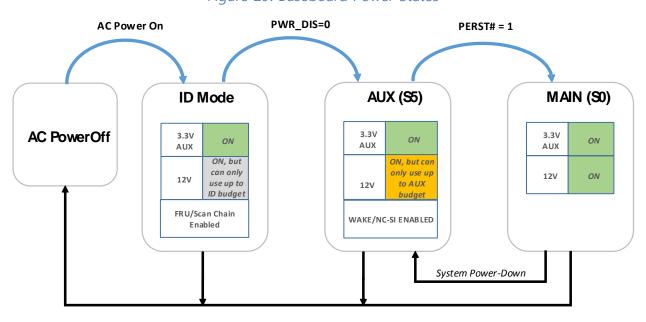


Figure 29: Baseboard Power States

Table 31: Power States

Power State	PWRDIS	PERSTn	FRU	Scan	RBT	3.3V	12V
				Chain	Link		
AC Power Off	Low	Low					
ID Mode	High	Low	Χ	Х		Χ	Х
Aux Power Mode (S5)	Low	Low	Χ	Χ	Χ	Χ	Χ
Main Power Mode (S0)	Low	High	Χ	Х	Χ	Х	Х

3.9.1 AC Power Off

In AC power off mode, all power delivery has been turned off or disconnected from the baseboard.

3.9.2 ID Mode

In the ID Mode, only 3.3V Aux is available for powering up management only functions. FRU accesses are only allowed in this mode.

3.9.3 Aux Power Mode (S5)

In Aux Power Mode provides both 3.3V Aux as well as 12V Aux is available. 12V Aux may be used to deliver power to the add-in card, but only up to the Aux budget of 35W.

3.9.4 Main Power Mode (S0)

In Main Power Mode provides both 3.3V and 12V (Main) across the OCP connector. The add-in card operates in full capacity. Up to 79.2W may be delivered on 12V, and 3.63W on the 3.3V pins.

3.10 Power Supply Rail Requirements

The baseboard provides 3.3Vaux and 12Vaux/main to both the Primary and Secondary connectors. The rail requirements are leveraged from the PCIe CEM 4.0 specification. For OCP NIC 3.0 cards, the requirements are as follows:

Power Rail 30W Slot 80W Slot 150W **Small Card Hot Aisle Small Card Cold Aisle Large Card Cold Aisle** 3.3V Voltage Tolerance ±9% (max) ±9% (max) ±9% (max) Supply Current **ID** Mode 375mA (max) 375mA (max) 375mA (max) Aux Mode 1.1A (max) 1.1A (max) 2.2A (max) Main Mode 1.1A (max) 1.1A (max) 2.2A (max) Capacitive Load $150\mu F$ (max) $150\mu F$ (max) $300\mu F$ (max) 12V Voltage Tolerance ±8% (max) ±8% (max) ±8% (max) Supply Current ID Mode 100mA (max) 100mA (max) 100mA (max) Aux Mode 1.3A (max) 3.3A (max) 6.3A (max) Main Mode 2.5A (max) 6.6A (max) 12.5A (max) Capacitive Load $1000\mu F$ (max) 2000µF (max) $4000 \mu F (max)$

Table 32: Baseboard Power Supply Rail Requirements

3.11 Hot Swap Considerations for 12V and 3.3V Rails

For baseboards that support system hot (powered on) add-in card insertions and extractions, the system implementer shall consider the use of hotswap controllers on both



the 12Vmain/aux and 3.3Vaux pins to prevent damage to the baseboard or the add-in card. Hotswap controllers help with in-rush current limiting while also providing overcurrent protection, undervoltage and overvoltage protection capabilities.

The hotswap controller may gate the 12Vmain/aux and 3.3Vmain/aux based on the PRSNTB[3:0]# value. Per Section 3.6.3, a card is present in the system when the encoded value is not 0b1111. The PRSNTB[3:0]# can be AND'ed together and connected to the hotswap controller to accomplish this result. Per the OCP NIC 3.0 mechanical definition (Section XXX), the present pins are short pins and engage only when the card is positively seated.

Baseboards that do not support hot insertion, or hot extractions may opt to not implement these features.

3.12 Power Sequence Timing Requirements

The following figure shows the power sequence of PRSNTB[3:0]#, 3.3Vaux, 12Vaux/12Vmain relative to PWRDIS, BIF[2:0]#, PERSTn*, the add-in card power ramp and NIC_PWR_GOOD.

Figure 30: Power Sequencing

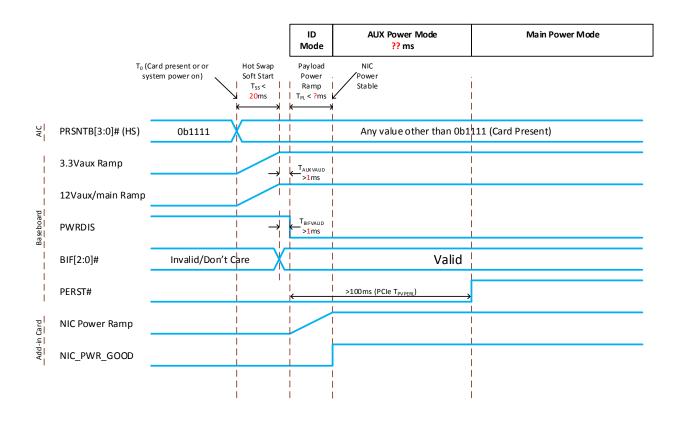


Table 33: Power Sequencing Parameters

Parameter	Value	Units	Description
T_{ss}	20	ms	Max time between system 3.3Vaux and 12Vaux/main ramp
			to power stable.
T _{AUXVALID}	>1	ms	Min time between 3.3Vaux valid to PWRDIS assertion.
T _{BIFVALID}	>1	ms	Min time between BIF[2:0]# valid to PWRDIS assertion. The
			BIF[2:0]# value sets the add-in card bifurcation mode (if
			applicable)
T_{PL}	</td <td>ms</td> <td>Max time between the NIC payload power ramp to</td>	ms	Max time between the NIC payload power ramp to
			NIC_PWR_GOOD assertion
T _{PVPERL}	>100	ms	Max time between PWRDIS deassertion and PERST#
			deassertion. This value is from the PCIe CEM Specification,
			Rev 4.0.



4 Management

4.1 SMBus Interface

The SMBus provides manageability of the add-in card.

4.2 NC-SI Sideband Interface

4.2.1 NC-SI addressing and Arb#

4.3 MAC Address Requirement

4.4 FRU EEPROM

4.4.1 Minimum EEPROM Size

4.4.2 **EEPROM Map Definition**

Editor's note [TN, 20171208]: the EEPROM map definition should include the card power class (e.g. be able to identify the max power required for 12V to the baseboard). This allows the baseboard to intelligently enable/disable the card based on the available baseboard power budget.

4.4.3 EEPROM Address

4.5 FW Requirement (TBD)

4.6 Thermal Reporting Interface

5 Data Network Requirement

5.1 Network Booting (collect view from OEMs and hyperscale)

Mezzanine NIC shall support network booting in uEFI system environment. Mezzanine NIC shall support both IPv4 and IPv6 network booting.



6 Routing Guidelines and Signal Integrity Considerations

6.1 NC-SI Over RBT

Min Length: 2" Max length: 4"

Impedance: 50 Ohm single ended

7 Thermal and Environmental

7.1 Environmental Requirements

The specific environment requirement is removed to allow the adoption of OCP Mezzanine NIC in systems with very different thermal requirement and boundary condition.

This Mezzanine card shall meet the same environmental requirements specified in the OCP systems that the Mezzanine card is in. The OCP system that uses OCP Mezzanine card shall define air flow direction, inlet air temperature, air flow (or speed) to the local area where Mezzanine card is at, and simulation boundary.

7.1.1 Thermal Simulation Boundary Example

Placeholder for Thermal Simulation Method. Using Facebook Intel® Motherboard V3.0 as example. Not covered by this update.

7.2 Shock & Vibration

This Mezzanine card shall meet the same shock & vibration requirements specified in updated Facebook OCP Intel® Motherboard V2.0 and V3.0 Design Specification.

7.3 Regulation

This Mezzanine card shall meet CE, CB, FCC Class A, WEEE, ROHS requirements.

8 Revision History

Author	Description	Revision	Date
Thomas Ng	Initial draft	0.1	12/xx/2017