

OCP NIC 3.0 Design Specification

Version 0.01

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1 Overview

1.1 License

As of April 7, 2011, the following persons or entities have made this Specification available under the Open Web Foundation Final Specification Agreement (OWFa 1.0), which is available at http://www.openwebfoundation.org/legal/the-owf-1-0-agreements/owfa-1-0: Facebook, Inc.

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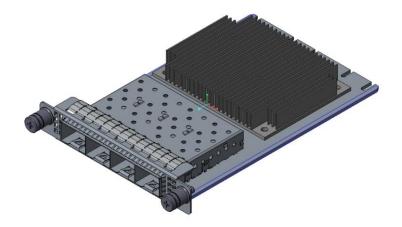
1.2 Background

The OCP NIC 3.0 specification is a follow-on to the OCP 2.0 form-factor for PCIe add-in cards. The OCP NIC 3.0 specification supports two basic card sizes: Small Card, and Large Card. The Small Card allows for up to 16 PCIe lanes on the card edge while a Large Card supports up to 32 PCIe. Compared to the OCP NIC 2.0 release, the updated specification provides a broader solution space for NIC and system vendors to support the following use case scenarios:

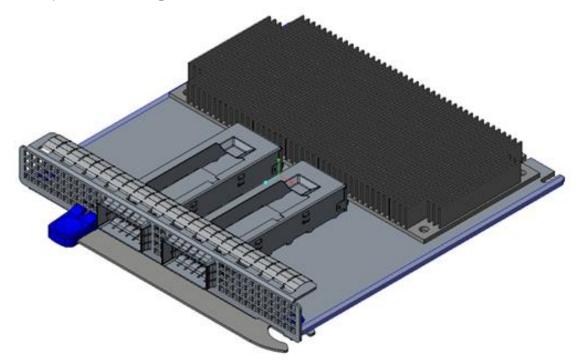
- NICs with a higher TDP
- Support up to 79W of power delivery to a single connector (Small) card; and 158W to a dual connector (Large) card
- PCIe Gen4 and Gen5 on the system and add-in card
- Support for upto 32 lanes of PCIe per add-in card
- Support for single host and multi-host environments
- Support a greater board area for more complex add-in card designs
- Support for Smart NIC implementations with on-board DRAM
- Simplification of FRU installation and removal while reducing overall down time

A representative Small Card OCP 3.0 NIC mezzanine card is shown in Figure 1 and a representative Large Card is shown in Figure 2.

Figure 1: Representative Small OCP NIC 3.0 Card with Quad SFP Ports







In order to achieve the features outlined in this specification, OCP 3.0 compliant cards are not backwards compatible to the 2.0 cards.

This specification is created under OCP Server workgroup – OCP NIC subgroup. An electronic copy of this specification can be found on the Open Compute Project website:

http://www.opencompute.org/wiki/Server/Mezz#Specifications_and_Designs

1.3 Acknowledgements

Placeholder

1.4 Overview

1.4.1 Mechanical Form factor overview

The OCP NIC 3.0 specification defines a third generation mechanical form factor that allows for interoperability between compliant baseboards and add-in cards.



OCP NIC 3.0 cards have two form factors – Small and Large. These cards are shown in Figure 3 below. The components shown in the figures are for illustrative purposes. The Small form factor card has one connector (Primary connector) on baseboard. The Large form factor card has two connectors (Primary Connector and Secondary Connector) on the baseboard. Both the Primary and Secondary connectors are defined in and compliant to SFF-TA-1002. [Editor's note: plan to submit change back to SFF-TA-1002]. On the NIC side, the card edge is implemented with gold fingers. The gold finger design follows SFF-TA-1002 as well.

Primary Connector
4C + OCP NIC bay

NIC bay

NIC bay

NIC bay

Network I/O

Network

Figure 3: Small and Large Card Form-Factors (not to scale)

The two form factor dimensions are shown in Table 1.

Table 1: OCP 3.0 Form Factor Dimensions

Form	Width	Depth	Primary	Secondary	Typical Use Case
Factor			Connector	Connector	

Small	W1 = 76	L = 115	4C + OCP	N/A	Low profile and general NIC
	mm	mm	sideband		with a similar profile as an
			168 pins		OCP NIC 2.0 add-in card;
					up to x16 PCIe.
Large	W2 = 139	L = 115	4C + OCP	4C	Larger PCB width to
	mm	mm	sideband	140 pins	support feature rich NICs;
			168 pins		up to x32 PCIe.

The OCP NIC 3.0 design allows downward compatibility between the two card sizes. Table 2 shows the compatibility between the baseboard and NIC combinations. A small size baseboard slot may only accept a small sized NIC. A Large size baseboard slot may accept a small or large sized NIC.

Table 2: Baseboard to OCP NIC Form factor Compatibility Chart

Baseboard	NIC Size / Suppo	orted PCIe Width		
Slot Size	Small	Large		
Small	Up to x16	Not Supported		
Large	Up to x16	Up to x32		

There are two baseboard connector options available for system designers: straddle mount and right angle (RA). The straddle mount connector option allows the OCP NIC and baseboard to exist in a co-planer position. To achieve this, a cutout exists on the baseboard and is defined in this specification. Alternatively, the right angle option allows the OCP NIC to be installed on top of the baseboard. A baseboard cutout is not required for the right angle connector. The right angle option allows the baseboard to use this area for additional routing or backside component placement. The straddle mount and right angle connectors are shown in Section 3.2.

For both the baseboard and OCP card, this specification defines the component and routing keep out areas. Refer to Section 2.6 for details.

Both the straddle mount and right angle implementations shall accept the same OCP add-in card and shall be supported in the baseboard chassis regardless of the baseboard connector



selection (right angle or straddle mount) so long as the baseboard slot side and add-in card sizes are a supported combination as shown in Table 2.

This specification defines the form factor at the add-in card level, including the front panel, latching mechanism and card guide features [TBD; pending on the Mechanical work across stakeholders].

More details about the card form-factor is shown in Section 2.

1.4.2 Electrical overview

This specification defines the electrical interface between baseboard and the add-in card.

The electrical interface is implemented with a right angle or straddle mount connector on baseboard and gold finger on the add-in card. As previously noted in the mechanical overview, each card may implement a Primary Connector or Primary + Secondary Connector. Cards using only the Primary connector are suitable for both the Small and Large form-factors and may support up to x16 lanes of PCIe. The Secondary connector, when used in conjunction with the Primary connector, allows Large form-factor implementations and may support up to 32 lanes of PCIe.

1.4.2.1 Primary Connector

1.4.2.2 Secondary connector

1.5 References

- DMTF Standard. DSP0222, Network Controller Sideband Interface (NC-SI) Specification.
 Distributed Management Task Force, Inc, Rev 1.0.1, January 24th, 2013.
- EDSFF. Enterprise and Datacenter SSD Form Factor Connector Specification. Enterprise and Datacenter SSD Form Factor Working Group, Rev 0.9 (draft), August 2nd 2017.
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 http://www.opencompute.org/wiki/Server/Mezz
- PCIe Base Specification. PCI Express Base Specification, Revision 4.0 (draft).
- PCIe CEM Specification. PCI Express Card Electromechanical Specification, Revision 4.0 (draft).
- SMBus Management Interface Forum. *System Management Bus (SMBus) Specification.*System Management Interface Forum, Inc, Version 3.0, December 20th, 2014.
- SNIA. SFF-TA-1002, Specification for Protocol Agnostic Multi-Lane High Speed Connector. SNIA SFF TWG Technology Affiliate, Rev 0.0.9.1, September 9th, 2017.



2 Card Form Factor

2.1 Overview

2.2 Form Factor Options

OCP3.0 provides two fundamental form factor options: a small card (76mm \times 115mm) and a large card (139mm \times 115mm).

These form factors support a Primary Connector and optionally, a Secondary Connector. The Primary Connector is defined to be a SFF-TA-1002 compliant 4C connector plus a 28-pin bay for OCP 3.0 specific pins. The Secondary Connector is the 4C connector as defined in SFF-TA-1002. The 4C specification supports up to 32 differential pairs for a x16 PCIe connection per connector. For host platforms, the 28-pin OCP bay is required for the Primary connector. This is also mandatory for add-in cards.

The small card uses the 4C connector for up to a x16 PCIe interface. The small cards implement and additional 28-pin OCP bay for management functions and support for up to a four PCIe hosts. The small size card provides sufficient faceplate area to accommodate up to 2x QSFP modules, 4x SFP modules, or 4x RJ-45 for BASE-T operation. The small card form factor supports up to 79W of delivered power to the card edge.

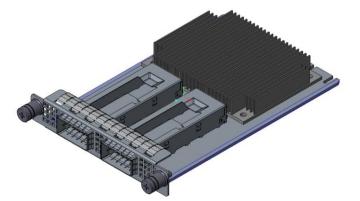


Figure 4: Example Small Card Form Factor

The large card uses provides the same functionality as the small card, but with support up to a x32 PCIe interface. The large card utilizes both the Primary and Secondary connectors. The large size card supports higher power envelopes and provides additional board area for more complex designs. The small card form factor supports up to 158W of delivered power to the card edge at 79W per connector.

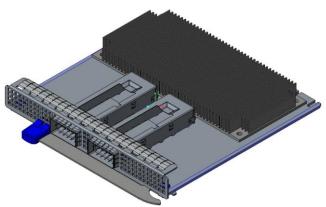


Figure 5: Example Large Card Form Factor

For both form-factors, an add-in card may optionally implement a subset of pins to support a x8 PCIe connection. This is implemented using a 2C card edge per SFF-TA-1002. The Primary Connector may support a 2C sized add-in card along with the 28 pin OCP bay. The following diagram from the SFF-TA-1002 specification illustrates the supported host Primary and Secondary Connectors and add-in card configurations.



Figure 6: Primary Connector (4C + OCP Bay) with 4C and 2C Add-in Cards

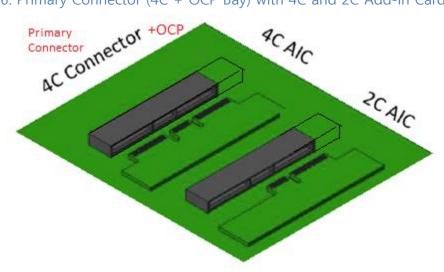


Table 3 summarizes the supported card form factors. Small form factors cards support the Primary Connector and up to 16 PCIe lanes. Large form factor cards support both the Primary and Secondary Connectors and up to 32 PCIe lanes.

Table 3: OCP NIC 3.0 Card Definitions

Add in Card Size and	Secondary Connector		Primary Connector		
max PCIe Lane Count	4C Connector, x16 PCIe		4C Connector, x16 PCIe		OCP Bay
Small (x8)				2C	OCP Bay
Small (x16)	5)		4	C	OCP Bay
Large (x24) 2C		4	С	OCP Bay	
Large (x32)	4C		4	C	OCP Bay

2.3 I/O bracket

TBD < need input from OCP mechanical groups>

2.4 Line Side I/O Implementations

At the time of this writing, the Small and Large form-factor cards may support the following standard line side I/O implementations:

Table 4: OCP 3.0 Line Side I/O Implementations

Form Factor	Max Topology Connector Count
Small	2x QSFP28
Small	4x SFP28
Small	4x RJ-45
Large	TBD
Large	TBD
Large	TBD

Additional combinations are permissible as I/O form-factor technologies and thermal capabilities evolve.

2.5 LED Implementation

A small form-factor OCP NIC 3.0 with a fully populated I/O bracket (2x QSFP28, 4x SFP28, or 4x RJ-45) has insufficient space for on-board (faceplate) LED indicators. In this case, the line side link and activity LED indicators are implemented on the baseboard system via the Scan Chain. The Scan Chain bit stream is defined in Section 3.5.3.

For small form-factor low I/O count cards (such as 1x QSFP28, 2x SFP28, or 2x RJ-45), or a large form-factor OCP 3.0 NIC, where additional I/O bracket area is available, the card may optionally implement on-board link/activity indications in addition to the Scan Chain.

For both cases, the OCP NIC 3.0 specification recommends the following LED definitions:

Table 5: Default LED Configuration

LED Pin	LED Color	Description
Link	Green	Active low. Multifunction LED.
		When lit and solid, this LED is used to indicate the link is up at
		the MAC level. Local and Remote Faults are clear and the link is
		ready for data transmission. When the LED is off, the physical link
		is down or disabled.



		This LED indicator may also be used for port identification
		through vendor specific link diagnostic software.
		The link LED shall be located on the left hand side of each port.
Activity	Green	Active low.
		The Activity LED shall only be illuminated when the Link LED is
		illuminated.
		When lit and solid, this LED is used to indicate the port is "idle"
		and no data is being transmitted or received.
		When lit and blinking, this LED is used to indicate the port is
		"active" and data is either being transmitted or received.
		When the LED is off, no link is detected.
		The activity LED shall be located on the right hand side of each
		port.

At the time of this writing, the Scan Chain definition allows for up to one link and one activity LED per port. A total of up to 8 ports are supported in the Scan Chain. The bit stream defines the LEDs to be active low (ON). The Scan Chain LED implementation allows the NIC LED indicators to be remotely located on the OCP 3.0 compliant chassis (e.g. front LED indicators with rear I/O cards).

2.6 Mechanical Keepout Zones

2.6.1 Baseboard Keep Out Zones

TBD – Need keepout drawings and envelopes for small / large size baseboard including primary/secondary/rail keepouts/cutout for straddle mount/keepout for right angle.

2.6.2 Add-in Card Keep Out Zones

TBD – need keepout drawings and envelopes for small / large size NIC including primary/secondary/rail keepouts.

2.7 Labeling Requirements

TBD

2.8 Insulation Requirements

All cards must implement a secondary side insulator to prevent the bottom side card components from shorting out to the chassis. The recommended insulator thickness is 0.25mm and must reside within the following mechanical envelope for the Small and Large size cards:

TBD <need 2D drawings>

2.9 NIC Implementation Examples

TBD

2.10 Non-NIC Use Cases

"PCIe interface with extra management sideband"

2.10.1 PCIe Retimer card

2.10.2 Accelerator card

2.10.3 Storage HBA / RAID card

3 Card Edge and Baseboard Connector Interface

3.1 Gold Finger Requirement

The OCP NIC 3.0 add-in cards are compliant to the SFF-TA-1002 specification with respect to the gold fingers and connectors.

Small Size cards fit in the Primary Connector. Primary Connector compliant cards are 76mm x 115mm and may implement the full 168-pins. The Primary Connector cards may optionally implement a subset of gold finger pins if there is a reduced PCIe width requirement (such as 1 x8 and below). In this case, the card edge gold finger may implement a 2C design. The



overall board thickness is 1.60mm. The gold finger dimensions for the Primary Connector compliant cards are shown below.

Large Size Cards support up to a x32 PCIe implementation and uses both the Primary and Secondary connectors.

For additional details, refer to the card and connector mechanical drawings located in XXX.

Note: The "B" pins on the connector are associated with the top side of the add-in card. The "A" pins on the connector are associated with the bottom side of the add-in card.

Figure 7: Small Size Primary Connector Gold Finger Mating Card Dimensions – x16 – Top Side

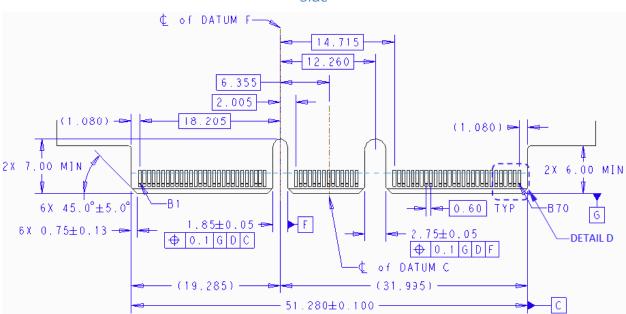


Figure 8: Small Size Primary Connector Gold Finger Mating Card Dimensions – x16 – Bottom Side

<mark>TBD</mark>

Figure 9: Large Size Card Gold Finger Mating Card Dimensions – x32 – Top Side

Figure 10: Large Size Card Gold Finger Mating Card Dimensions – x32 – Bottom Side

TBD

3.1.1 Gold Finger Mating Sequence

Per the SFF-TA-1002 specification, the Primary and Secondary connectors are protocol agnostic and are optimized for high speed differential pairs. For use in the OCP NIC 3.0 application, some pin locations are used for single ended control nets or power and would benefit from a shorter pin length for staggering. As such, the recommended add-in card gold finger staging is shown in Table 6 for a two stage, first-mate, last-break functionality. The host connectors have a single stage mating and do not implement different pin lengths.

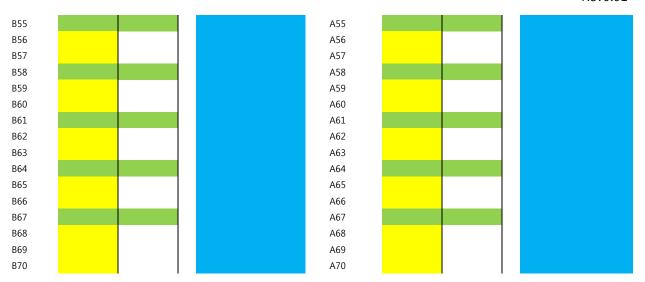
The AIC Plug (Free) side refers to the add-in card gold fingers; the receptacle (Fixed) side refers to the physical connector on the host platform. This table is based on the SFF-TA-1002 Table A-1 with modifications for OCP NIC 3.0. Refer to the mechanical drawings for pin the first-mate and second-mate lengths.

Side B Side A AIC Plug (Free) Receptacle (Fixed) AIC Plug (Free) Receptacle (Fixed) 2nd Mate 1st Mate 2nd Mate 1st Mate OCP B1 OCP A1 OCP B2 OCP A2 OCP B3 OCP A3 OCP B4 OCP A4 OCP B5 OCP A5 OCP B6 OCP A6 OCP B7 OCP A7 OCP B8 OCP A8 OCP B9 OCP A9 OCP B10 OCP A10 OCP B11 OCP A11 OCP B12 OCP A12 OCP B13 OCP A13 OCP B14 OCP A14 Mechanical Key В1 Α1 Α2 B2 В3 АЗ Α4

Table 6: Contact Mating Positions for the Primary and Secondary Connectors



B5			A5		
B6			A6		
B7			A7		
B8			A7 A8		
В9			A6 A9		
B10			A10		
B11			A11		
B12			A12		
B13			A13		
B14			A14		
B15			A15		
B16			A16		
B17			A17		
B18			A18		
B19			A19		
B20			A20		
B21			A21		
B22			A22		
B23			A23		
B24			A24		
B25			A25		
B26			A26		
B27			A27		
B28			A28		
		Mecl	nanical Key		
B29			A29		
B30			A30		
B31			A31		
B32			A32		
B33			A33		
B34			A34		
B35			A35		
B36			A36		
B37			A37		
B38			A38		
B39			A39		
B40			A40		
B41			A41		
B42			A42		
D.42		Mecl	nanical Key		
B43			A43		
B44			A44		
B45			A45		
B46			A46		
B47			A47		
B48			A48		
B49			A49		
B50			A50		
B51			A51		
B52			A52		
B53			A53		
B54			A54		



3.2 Baseboard Connector Requirement

The OCP NIC 3.0 connectors are compliant to the "4C connector" as defined in the SFF-TA-1002 specification for a right angle or straddle mount form-factor. The 4C connector is 140-pins in width and includes support for up to 32 differential pairs to support a x16 PCIe connection. The connector also provides 6 pins of 12V for payload power. This implementation is common between both the Primary and Secondary Connectors. In addition, the Primary Connector has a 28-pin OCP Bay to the right of pin 1. These pins are used for management and support for up to a 4 x4 multi-host configuration on the Primary Connector. The Primary and Secondary Connector drawings are shown in Figure 11, Figure 12, Figure 13 and Figure 14 below.

Figure 11: 168-pin Base Board Primary Connector – Right Angle

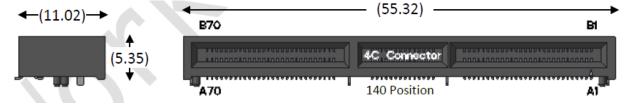


Figure 12: 140-pin Base Board Secondary Connector – Right Angle

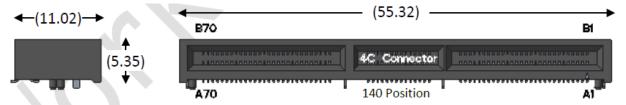


Figure 13: 168-pin Base Board Primary Connector – Straddle Mount



<mark>TBD</mark>

Figure 14: 140-pin Base Board Secondary Connector – Straddle Mount

TBD

In order to the support the large form factor, systems must locate the Primary and Secondary Connectors per the mechanical drawing shown in Figure 15.

Figure 15: Primary and Secondary Connector Locations for Large Card Support

<mark>TBD</mark>

3.3 Pin definition

The pin definitions of an OCP NIC 3.0 card with up to a x32 PCIe interface are shown in Table 7 and Table 8. All signal directions are shown from the perspective of the baseboard.

A baseboard system may provide a combination of Primary Connectors only, or Primary and Secondary Connectors to support multiple sizes of add-in cards. Both connectors share common functionality with power, SMBus, x16 PCIe Gen4 and bifurcation control. The Primary Connector has an additional OCP Bay (pins OCP_A[1:14], OCP_B[1:14]) with additional REFCLKs for supporting up to four PCIe hosts, NC-SI connectivity and a Scan Chain for information exchange between the host and card. The NIC is required to implement the Scan Chain, while the baseboard may choose to optionally implement it. Depending on the baseboard form-factor, multiple OCP NIC 3.0 compliant cards may be designed into the system.

The pins common to the Primary and Secondary Connectors are shown in Section 3.4. The OCP Bay pins on the Primary Connector only are shown in Section 3.5.

Cards or systems that do not require the use of a PCIe x16 connection may optionally implement a subset electrical connections as applicable to the design. For example, a x8 (or smaller) card using the first 8 PCIe lanes that is compliant with the Primary Connector pinout. Refer to Sections 3.1 and 3.2 for mechanical details. For these cases, the Primary Connector matches the 2C dimensions as defined in SFF-TA-1002.

In all cases, the physical baseboard connectors shall support x16 PCIe widths and must be implemented with the Primary (4C + OCP Bay) and Secondary (4C) connectors.

Table 7: Primary Connector Pin Definition (x16) (4C + OCP Bay)

	Side B	Side A			
OCP_B1	NIC_PWR_GOOD	WAKE_N	OCP_A1	-	-
OCP_B2	PWRBRK#	PERST2#	OCP_A2	rim	rim
OCP_B3	LD#	PERST3#	OCP_A3	ary	ary
OCP_B4	DATA_IN	RBT_ARB_IN	OCP_A4	Con	Con
OCP_B5	DATA_OUT	RBT_ARB_OUT	OCP_A5	nect	nect
OCP_B6	CLK	GND	OCP_A6	Ö,	tor (
OCP_B7	SLOT_ID0	RBT_TX_EN	OCP_A7	×16	X8,
OCP_B8	RBT_RXD1	RBT_TXD1	OCP_A8	, 16	112
OCP_B9	RBT_RXD0	RBT_TXD0	OCP_A9	8- <u>p</u> .	-pin
OCP_B10	GND	GND	OCP_A10	n ac	ado
OCP_B11	REFCLKn2	REFCLKn3	OCP_A11	dd-i	d-in
OCP_B12	REFCLKp2	REFCLKp3	OCP_A12	n ca	car
OCP_B13	GND	GND	OCP_A13	rd v	d wi
OCP_B14	RBT_CRS_DV	RBT_CLK_IN	OCP_A14	Primary Connector (x16, 168-pin add-in card with OCP Bay)	Primary Connector (x8, 112-pin add-in card with OCP bay)
	Mechan	ical Key		<u>8</u>	ЭСР
B1	+12V/+12V_AUX	GND	A1	Ва	bay
B2	+12V/+12V_AUX	GND	A2	હ)
В3	+12V/+12V_AUX	GND	A3		
B4	+12V/+12V_AUX	GND	A4		
B5	+12V/+12V_AUX	GND	A5		
В6	+12V/+12V_AUX	GND	A6		
В7	BIFO#	SMCLK	A7		
B8	BIF1#	SMDAT	A8		
В9	BIF2#	SMRST#	A9		
B10	PERSTO#	PRSNTA#	A10		
B11	+3.3V/+3.3V_AUX	PERST1#	A11		
B12	PWRDIS	PRSNTB2#	A12		
B13	GND	GND	A13		
B14	REFCLKn0	REFCLKn1	A14		
B15	REFCLKp0	REFCLKp1	A15		
B16	GND	GND	A16		
B17	PETn0	PERn0	A17		
B18	PETp0	PERp0	A18		



			1	
B19	GND	GND	A19	
B20	PETn1	PERn1	A20	
B21	PETp1	PERp1	A21	
B22	GND	GND	A22	
B23	PETn2	PERn2	A23	
B24	PETp2	PERp2	A24	
B25	GND	GND	A25	
B26	PETn3	PERn3	A26	
B27	PETp3	PERp3	A27	
B28	GND	GND	A28	
	Mechan	ical Key		
B29	GND	GND	A29	
B30	PETn4	PERn4	A30	
B31	PETp4	PERp4	A31	
B32	GND	GND	A32	
B33	PETn5	PERn5	A33	
B34	PETp5	PERp5	A34	
B35	GND	GND	A35	
B36	PETn6	PERn6	A36	
B37	PETp6	PERp6	A37	
B38	GND	GND	A38	
B39	PETn7	PERn7	A39	
B40	РЕТр7	PERp7	A40	
B41	GND	GND	A41	
B42	PRSNTB0#	PRSNTB1#	A42	
	Mechan	ical Key		
B43	GND	GND	A43	
B44	PETn8	PERn8	A44	
B45	PETp8	PERp8	A45	
B46	GND	GND	A46	
B47	PETn9	PERn9	A47	
B48	PETp9	PERp9	A48	
B49	GND	GND	A49	
B50	PETn10	PERn10	A50	
B51	PETp10	PERp10	A51	
B52	GND	GND	A52	
B53	PETn11	PERn11	A53	
B54	PETp11	PERp11	A54	
B55	GND	GND	A55	
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B56	PETn12	PERn12	A56	
B57	PETp12	PERp12	A57	
B58	GND	GND	A58	
B59	PETn13	PERn13	A59	
B60	PETp13	PERp13	A60	
B61	GND	GND	A61	
B62	PETn14	PERn14	A62	
B63	PETp14	PERp14	A63	
B64	GND	GND	A64	
B65	PETn15	PERn15	A65	
B66	PETp15	PERp15	A66	
B67	GND	GND	A67	
B68	RFU, N/C	RFU, N/C	A68	
B69	RFU, N/C	RFU, N/C	A69	
B70	PRSNTB3#	RFU, N/C	A70	



Table 8: Secondary Connector Pin Definition (x16) (4C)

	Side B	Side A			
B1	+12V/+12V_AUX	GND	A1	Š	S
B2	+12V/+12V_AUX	GND	A2	Secondary Connector (x16, 140-pin add-in card)	Secondary Connector (x8, 84-pin add-in card)
В3	+12V/+12V_AUX	GND	A3	idar	ıdar
B4	+12V/+12V_AUX	GND	A4	λ (y Co
B5	+12V/+12V_AUX	GND	A5	onne	onne
В6	+12V/+12V_AUX	GND	A6	cto	ecto
В7	BIFO#	SMCLK	A7	2	r (xg
B8	BIF1#	SMDAT	A8	[6, 1	8, 8
В9	BIF2#	SMRST#	A9	40-	-pi
B10	PERSTO#	PRSNTA#	A10	pin	n ad
B11	+3.3V/+3.3V_AUX	PERST1#	A11	add	d-in
B12	PWRDIS	PRSNTB2#	A12	₽ .	car
B13	GND	GND	A13	card	g
B14	REFCLKn0	REFCLKn1	A14		
B15	REFCLKp0	REFCLKp1	A15		
B16	GND	GND	A16		
B17	PETn0	PERn0	A17		
B18	РЕТр0	PERp0	A18		
B19	GND	GND	A19		
B20	PETn1	PERn1	A20		
B21	PETp1	PERp1	A21		
B22	GND	GND	A22		
B23	PETn2	PERn2	A23		
B24	PETp2	PERp2	A24		
B25	GND	GND	A25		
B26	PETn3	PERn3	A26		
B27	РЕТр3	PERp3	A27		
B28	GND	GND	A28		
	Mechan	ical Key			
B29	GND	GND	A29		
B30	PETn4	PERn4	A30		
B31	PETp4	PERp4	A31		
B32	GND	GND	A32		
B33	PETn5	PERn5	A33		
B34	PETp5	PERp5	A34		
B35	GND	GND	A35		
B36	PETn6	PERn6	A36		

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B37	PETp6	PERp6	A37	
B38	GND	GND	A38	
B39	PETn7	PERn7	A39	
B40	РЕТр7	PERp7	A40	
B41	GND	GND	A41	
B42	PRSNTB0#	PRSNTB1#	A42	
	Mechan	ical Key		
B43	GND	GND	A43	
B44	PETn8	PERn8	A44	
B45	PETp8	PERp8	A45	
B46	GND	GND	A46	
B47	PETn9	PERn9	A47	
B48	PETp9	PERp9	A48	
B49	GND	GND	A49	
B50	PETn10	PERn10	A50	
B51	PETp10	PERp10	A51	
B52	GND	GND	A52	
B53	PETn11	PERn11	A53	
B54	PETp11	PERp11	A54	
B55	GND	GND	A55	
B56	PETn12	PERn12	A56	
B57	PETp12	PERp12	A57	
B58	GND	GND	A58	
B59	PETn13	PERn13	A59	
B60	PETp13	PERp13	A60	
B61	GND	GND	A61	
B62	PETn14	PERn14	A62	
B63	PETp14	PERp14	A63	
B64	GND	GND	A64	
B65	PETn15	PERn15	A65	
B66	PETp15	PERp15	A66	
B67	GND	GND	A67	
B68	RFU, N/C	RFU, N/C	A68	
B69	RFU, N/C	RFU, N/C	A69	
B70	PRSNTB3#	RFU, N/C	A70	
	<u> </u>			



3.4 Signal Descriptions – Common

The pins shown in this section are common to both the Primary and Secondary Connectors. All pin directions are from the perspective of the baseboard.

The add-in card shall implement protection methods to prevent leakage paths between the Vaux and Vmain power domains in the event that a NIC is powered down in a powered up baseboard.

Note: Pins that are only used on Primary Connector 28-pin OCP bay are defined in Section 3.5.

3.4.1 PCIe Interface Pins

This section provides the pin assignments for the PCIe interface signals. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0. Example connection diagrams for are shown in Figure 26.

Table 9: Pin Descriptions - PCIe 1

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
REFCLKn0	B14	Output	PCIe compliant differential reference clock #0,
REFCLKp0	B15		and #1. 100MHz reference clocks are used for
REFCLKn1	A14	Output	the add-in card PCIe core logic.
REFCLKp1	A15		
			For baseboards, the REFCLK0 and REFCLK1
			signals are required at the connector.
			For add-in cards, the required REFCLKs shall be
			connected per the endpoint datasheet.
			Note: For cards that only support 1 x16,
			REFCLK0 is used. For cards that support 2 x8,
			REFCLK0 is used for the first eight PCIe lanes,

	1	1	1
			and REFCLK1 is used for the second eight PCIe
			lanes.
			Refer to Section 2.1 in the PCIe CEM
			Specification, Rev 4.0 for electrical details.
PETn0	B17	Output	Transmitter differential pairs [0:15]. These pins
РЕТр0	B18		are connected from the baseboard transmitter
PETn1	B20	Output	differential pairs to the receiver differential
PETp1	B21		pairs on the add-in card.
PETn2	B23	Output	
PETp2	B24		The PCIe transmit pins are AC coupled on the
PETn3	B26	Output	baseboard with capacitors and are placed next
PETp3	B27		to the baseboard transmitters. The AC coupling
PETn4	B30	Output	capacitor must be between 176nF (min) and
PETp4	B31		265nF (max).
PETn5	B33	Output	
PETp5	B34		For baseboards, the PET[0:15] signals are
PETn6	B36	Output	required at the connector.
РЕТр6	B37		
PETn7	B39	Output	For add-in cards, the required PET[0:15] signals
РЕТр7	B40		shall be connected to the endpoint silicon. For
PETn8	B44	Output	silicon that uses less than a x16 connection, the
РЕТр8	B45		appropriate PET[0:15] signals shall be
PETn9	B47	Output	connected per the endpoint datasheet.
РЕТр9	B48		
PETn10	B50	Output	Refer to Section 6.1 in the PCIe CEM
PETp10	B51		Specification, Rev 4.0 for details.
PETn11	B53	Output]
PETp11	B54		
PETn12	B56	Output]
PETp12	B57		
PETn13	B59	Output	
PETp13	B60		



PETn14	B62	Output	
PETp14	B63		
PETn15	B65	Output	
PETp15	B66		
PERn0	A17	Input	Receiver differential pairs [0:15]. These pins are
PERp0	A18		connected from the add-in card transmitter
PERn1	A20	Input	differential pairs to the receiver differential
PERp1	A21		pairs on the baseboard.
PERn2	A23	Input	
PERp2	A24		The PCIe receive pins are AC coupled on the
PERn3	A26	Input	add-in card with capacitors and are placed next
PERp3	A27		to the add-in card transmitters. The AC
PERn4	A30	Input	coupling capacitor must be between 176nF
PERp4	A31		(min) and 265nF (max).
PERn5	A33	Input	
PERp5	A34		For baseboards, the PER[0:15] signals are
PERn6	A36	Input	required at the connector.
PERp6	A37		
PERn7	A39	Input	For add-in cards, the required PER[0:15] signals
PERp7	A40		shall be connected to the endpoint silicon. For
PERn8	A44	Input	silicon that uses less than a x16 connection, the
PERp8	A45		appropriate PER[0:15] signals shall be
PERn9	A47	Input	connected per the endpoint datasheet.
PERp9	A48		
PERn10	A50	Input	Refer to Section 6.1 in the PCIe CEM
PERp10	A51		Specification, Rev 4.0 for details.
PERn11	A53	Input	
PERp11	A54		
PERn12	A56	Input	
PERp12	A57		
PERn13	A59	Input	
PERp13	A60		

PERn14	A62	Input	
PERp14	A63		
PERn15	A65	Input	
PERp15	A66		
PERSTO#	B10	Output	PCIe Reset #0, #1. Active low.
PERST1#	A11		
			Indicates when the applied power is within
			tolerance and stable for the add-in card.
			PERST# goes high at least 100ms after the
			power rails are within operating limits per the
			PCIe CEM Specification. The PCIe REFCLKs also
			become stable within this period of time.
			PERST is pulled high on the baseboard.
			For OCP NIC 3.0, PERST deassertion also
			indicates the full card power envelope is
			available to the add-in card.
			For baseboards, the PERST[0:1]# signals are
			required at the connector.
			For add-in cards, the required PERST[0:1]#
			signals shall be connected to the endpoint
			silicon.
			333
			Note: For cards that only support 1 x16,
			PERSTO# is used. For cards that support 2 x8,
			PERSTO# is used for the first eight PCIe lanes,
			and PERST1# is used for the second eight PCIe
			lanes.
			Refer to Section 2.2 in the PCIe CEM
			Specification, Rev 4.0 for details.
			Specification, Nev 4.0 for details.



3.4.2 PCIe Present and Bifurcation Control Pins

This section provides the pin assignments for the PCIe present and bifurcation control signals. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure 16.

The PRSNTA#/PRSNTB[0:3]#/BIF[0:2]# pins much be latched at least 1 ms of the system AC power on to ensure the correct values are detected by the system. Changing the pin states after this timing window is not allowed. Refer to the AC timing diagram in Section XXX for details.

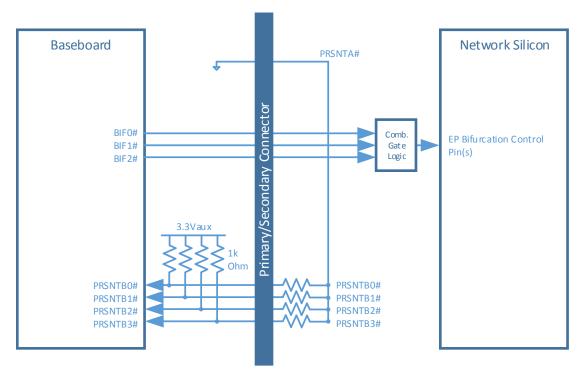
Table 10: Pin Descriptions – PCIe Present and Bifurcation Control Pins

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
PRSNTA#	A12	Output	Present A is used for add-in card presence and
			PCIe capabilities detection.
			For baseboards, this pin is directly connected
			to GND.
			For add-in cards, this pin is connected to the
			PRSNTB[3:0]# pins.
PRSNTB0#	B42	Input	Present B [0:3]# are used for add-in card
PRSNTB1#	A42		presence and PCIe capabilities detection.
PRSNTB2#	A10		
PRSNTB3#	B70		For baseboards, these pins are connected to
			the I/O hub and are pulled up to +3.3Vaux
			using 1kOhm resistors.
			For add-in cards, these pins are strapped to
			PRSNTA#. The encoding definitions are
			described in Section 3.6.

	1	ı	Ţ
			PRSNTB3# is located at the bottom of the 4C connector and is only applicable for add-in cards with a PCIe width of x16 (or greater). Add-in cards that implement a 2C card edge do not use the PRSNTB3# pin for capabilities or present detection.
BIFO#	A7	Output	Bifurcation [0:2]# pins allow the baseboard to
BIF1#	A8	•	force configure the add-in card bifurcation.
BIF2#	A9		
			For baseboards, these pins are outputs driven from the baseboard I/O hub and allows the system to force configure the add-in card bifurcation. The baseboard may optionally tie the BIF[0:2]# signals to 3.3Vaux or to ground if no dynamic bifurcation configuration is required.
			For add-in cards, these signals connect to the endpoint bifurcation pins if it is supported.
			The BIF[0:2]# encoding definitions are described in Section 3.6.
			Note: the required combinatorial logic output for endpoint bifurcation is dependent on the specific silicon and is not defined in this specification.

Figure 16: PCIe Present and Bifurcation Control Pins





3.4.3 SMBus Interface Pins

This section provides the pin assignments for the SMBus interface signals. The AC/DC specifications are defined in the SMBus and I²C bus specifications. An example connection diagram is shown in Figure XXX.

Table 11: Pin Descriptions – SMBus

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
SMCLK	A7	Output,	SMBus clock. Open drain, pulled up to 3.3Vaux
		OD	on the baseboard.
			For baseboards, connect the SMCLK from the
			platform SMBus master to the connector.
			For add-in cards, connect the SMCLK from the
			endpoint silicon to the card edge gold fingers.

SMDAT	A8	Input /	SMBus Data. Open drain, pulled up to 3.3Vaux
		Output,	on the baseboard.
		OD	
			For baseboards, connect the SMDAT from the
			platform SMBus master to the connector.
			For add-in cards, connect the SMDAT from the
			endpoint silicon to the card edge gold fingers.
SMRST#	A9	Output,	SMBus reset. Open drain.
		OD	
			For baseboards, this pin is pulled up to
			3.3Vauxand is used to reset optional
			downstream SMBus devices (such as
			temperature sensors). SMRST# is a mandatory
			signal for baseboard implementations.
			For add-in cards, SMRST# is optional.

3.4.4 Power Supply Pins

This section provides the pin assignments for the power supply interface signals. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0 and amended in Section 3.10. An example connection diagram is shown in Figure XXX.

Table 12: Pin Descriptions – Power

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
GND	Various	GND	Ground return; a total of 46 ground pins are
			on the main 140-pin connector area.
+12V/+12V_AUX	B1, B2,	Power	12V main or 12V Aux power; total of 6 pins per
	B3, B4,		connector. The 12V pins are rated to 1.1A per
	B5, B6		pin with a maximum derated power delivery of
			79.2W.



	T.		
			The +12V power pins must be within the rail
			tolerances (TBD tolerance for Aux) when the
			PWRDIS pin is driven low by the baseboard.
+3.3V/3.3V_AUX	B11	Power	3.3V main or 3.3V Aux power; total of 1 pin per
			connector. The 3.3V pin is rated to 1.1A for a
			maximum derated power delivery of 3.63W.
			The 3.3Vaux/main power pin must be within
			the rail tolerances when the PWRDIS pin is
			driven low by the baseboard.
PWRDIS	B12	Output	Power disable. Active high.
			This signal is driven by the baseboard.
			When high, this signal notifies the add-in card
			to turn off all supplies connected to +12V
			power.
			When low, this signal notifies the add-in card
			to enable the on-card power supplies.

3.4.5 Miscellaneous Pins

This section provides the pin assignments for the miscellaneous interface signals.

Table 13: Pin Descriptions – Miscellaneous 1

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
RFU, N/C	B68,	Input /	Reserved future use pins. Leave these pins as
	B69,	Output	no connect.
	A68,		

A69,	
A70	

3.5 Signal Descriptions – OCP Bay (Primary Connector)

The following section describes the functions in the Primary Connector 28-pin OCP bay. This 28-pin bay is shown in Section 3.3 and have pin numbers designated as OCP_B[1:14], and OCP_A[1:14]. All pin directions on this OCP bay are from the perspective of the baseboard.

The add-in card shall implement protection methods to prevent leakage paths between the Vaux and Vmain power domains in the event that a NIC is powered down in a powered up baseboard.

Note: The pins that are common to both the Primary and Secondary Connectors are defined in Section 3.4.

3.5.1 PCle Interface Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the PCIe interface signals on the Primary Connector OCP bay. The AC/DC specifications are defined in Section XXX. An example connection diagram that shows REFCLK2, REFCLK3, PERST2# and PERST3# is shown in Section 3.7.

Table 14: Pin Descriptions – PCIe 2

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
REFCLKn2	OCP_B11	Output	PCIe compliant differential reference clock #2,
REFCLKp2	OCP_B12		and #3. 100MHz reference clocks are used for
REFCLKn3	OCP_A11	Output	the add-in card PCIe core logic.
REFCLKp3	OCP_A12		
			For baseboards, the REFCLK2 and REFCLK3
			signals are required at the Primary connector.
			For add-in cards, the required REFCLKs shall be
			connected per the endpoint datasheet.



			Note: REFCLK2 and REFCLK3 are not used for cards that only support a 1 x16 or 2 x8 connection. Refer to Section 2.1 in the PCIe CEM Specification, Rev 4.0 for details.
PERST3#	OCP_A3	Output	PCIe Reset #2, #3. Active low. Indicates when the applied power is within tolerance and stable for the add-in card. PERST# goes high at least 100ms after the power rails are within operating limits per the PCIe CEM Specification. The PCIe REFCLKs also become stable within this period of time. PERST is pulled high on the baseboard. For OCP NIC 3.0, PERST deassertion also indicates the full card power envelope is available to the add-in card. For baseboards, the PERST[0:1]# signals are required at the connector. For add-in cards, the required PERST[0:1]# signals shall be connected to the endpoint silicon. Note: PERST2# and PERST3# are not used for cards that only support a 1 x16 or 2 x8 connection.

			Refer to Section 2.2 in the PCIe CEM
			Specification, Rev 4.0 for details.
WAKE#	OCP_A1	Input, OD	WAKE#. Open drain. Active low.
			This signal is driven by the add-in card to
			notify the baseboard restore the PCIe link. For
			add-in cards that support multiple WAKE#
			signals, their respective WAKE# pins may be
			tied together as the signal is open-drain to
			form a wired-OR.
			For baseboards, this signal is pulled up to
			+3.3V on the baseboard with a 10kOhm
			resistor and is connected to the system WAKE#
			signal.
			For add-in cards, this signal is connected
			directly to the endpoint silicon WAKE# pin(s).
			Refer to Section 2.3 in the PCIe CEM
			Specification, Rev 4.0 for details.

3.5.2 NC-SI Over RBT Interface Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the NC-SI over RBT interface signals on the Primary Connector OCP bay. The AC/DC specifications are defined in the NC-SI specification. An example connection diagram is shown in Figure 17.

For the purposes of this specification, the min and max electrical trace length of the NC-SI signals shall be between 2 inches and 4 inches. The traces shall be implemented as 50 Ohm impedance controlled nets.

Table 15: Pin Descriptions – NC-SI Over RBT



Signal Name	Pin #	Baseboard	Signal Description
		Direction	
RBT_CLK_IN	OCP_A14	Output	Reference clock input. Synchronous clock reference for receive, transmit and control interface. The clock has a nominal frequency of 50MHz ±100ppm.
			For baseboards, connect this pin between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull down resistor on the baseboard. If the baseboard does not support NC-SI over RBT, then terminate this signal to ground through a 100kOhm pull down resistor.
			For add-in cards, connect this pin from the gold finger to the endpoint silicon. Leave this pin as a no connect if NC-SI is not supported.
RBT_CRS_DV	OCP_B14	Input	Carrier sense/receive data valid. This signal is used to indicate to the baseboard that the carrier sense/receive data is valid.
			For baseboards, connect this pin between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull down resistor on the baseboard. If the baseboard does not support NC-SI over RBT, then terminate this signal to ground through a 100kOhm pull down resistor.
			For add-in cards, connect this pin from the gold finger to the endpoint silicon. Leave this pin as a no connect if NC-SI is not supported.

RBT_RXD0 RBT_RXD1	OCP_B9 OCP_B8	Input	Receive data. Data signals from the network controller to the BMC.
			For baseboards, connect this pin between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull-up resistor to 3.3Vaux on the baseboard. If the baseboard does not support NC-SI over RBT, then terminate this signal to 3.3Vaux through a 100kOhm pull-up.
			For add-in cards, connect this pin from the gold finger to the endpoint silicon. Leave this pin as a no connect if NC-SI is not supported.
RBT_TX_EN	OCP_A7	Output	Transmit enable.
			For baseboards, connect this pin between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm pull down resistor to ground on the baseboard. If the baseboard does not support NC-SI over RBT, then terminate this signal to ground through a 100kOhm pull down.
			For add-in cards, connect this pin from the gold finger to the endpoint silicon. Leave this pin as a no connect if NC-SI is not supported.
RBT_TXD0	OCP_A9	Output	Transmit data. Data signals from the BMC to
RBT_TXD1	OCP_A8		the network controller.
			For baseboards, connect this pin between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100kOhm



			pull-up resistor to 3.3Vaux on the baseboard. If
			the baseboard does not support NC-SI over
			RBT, then terminate this signal to 3.3Vaux
			through a 100kOhm pull-up.
			For add-in cards, connect this pin from the
			gold finger to the endpoint silicon. Leave this
			pin as a no connect if NC-SI is not supported.
RBT_ARB_OUT	OCP_A5	Output	NC-SI hardware arbitration output. Used only if
			the end point silicon supports hardware
			arbitration. Connects to the ARB_IN signal of
			an adjacent device.
			The ARB_IN pin is also routed to the card edge
			to allow multiple devices and OCP slots on the
			baseboard to share the NC-SI ring. The
			baseboard shall implement a multiplexing
			implementation that directs the RBT_ARB_OUT
			to the RBT_ARB_IN pin of the next NC-SI
			capable device in the ring, or back to the
			RBT_ARB_IN pin of the source device if there is
			a single device on the ring.
			For baseboards, connect this pin between the
			baseboard OCP connector(s) to complete the
			hardware arbitration ring. If the baseboard
			does not support NC-SI over RBT, connect this
			signal directly to the RBT_ARB_IN pin.
			For add-in cards, connect this pin from the
			gold finger to the endpoint silicon. Leave this
			pin as a no connect if NC-SI is not supported.
L	I	1	1 -

RBT_ARB_IN	OCP_A4	Input	NC-SI hardware arbitration input. Used only if the end point silicon supports hardware arbitration. Connects to the ARB_OUT signal of an adjacent device.
			The ARB_OUT pin is also routed to the card edge to allow multiple devices and OCP slots on the baseboard to share the NC-SI ring. The baseboard shall implement a multiplexing implementation that directs the RBT_ARB_IN to the RBT_ARB_OUT pin of the next NC-SI capable device in the ring, or back to the RBT_ARB_OUT pin of the source device if there is a single device on the ring.
			For baseboards, connect this pin between the baseboard OCP connector(s) to complete the hardware arbitration ring. If the baseboard does not support NC-SI over RBT, connect this signal directly to the RBT_ARB_OUT pin.
			For add-in cards, connect this pin from the gold finger to the endpoint silicon. Leave this pin as a no connect if NC-SI is not supported.
SLOT_ID	OCP_B7	Output	NC-SI Address pin. Used only if the end point silicon supports package identification.
			For baseboards, this pin is used to identify the slot ID value. Connect this pin directly to GND for SlotID = 0; or pull this pin up to 3.3Vaux for SlotID = 1.



For add-in cards, connect this pin to the endpoint SLOT_ID pin for device address selection.

For add-in cards with multiple end point devices, the SLOT_ID pin may be used to configure a different PHYAD bit so long as the resulting combination does not cause addressing interferences.

For end point devices without NC-SI support, leave this pin as a no connect.

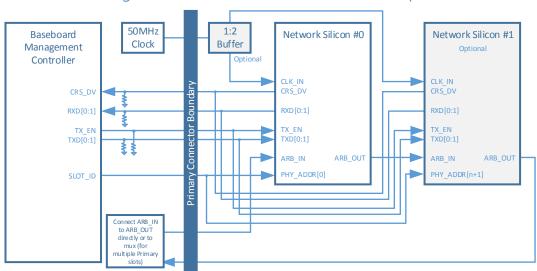


Figure 17: NC-SI Over RBT Connection Example

For baseboard designs with a single primary connector, connect ARB_IN to ARB_OUT to complete the NC-SI hardware arbitration ring. For Designs with multiple Primary Connectors, connect ARB_IN and ARB_OUT to an analog mux to complete the NC-SI arbitration ring based on the number of cards installed in the system.

3.5.3 Scan Chain Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the Scan Bus interface signals on the Primary Connector OCP Bay. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure 18.

Table 16: Pin Descriptions – Scan Chain

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
CLK	OCP_B6	Output	Scan clock. The CLK is an output pin from the baseboard to the add-in card. The CLK may run up to 12.5MHz.
			For baseboard implementations, connect the CLK pin to the Primary Connector. Tie the CLK pin directly to GND if the scan chain is not used.
			For NIC implementations, the CLK pin must be connected to Shift Registers 0 & 1, and optionally to Shift Registers 2 & 3 (if implemented) as defined in the text and Figure 18, below. Pull the CLK pin up to 3.3Vaux through a 1kOhm resistor.
DATA_OUT	OCP_B5	Output	Scan clock data output from the baseboard to the add-in card. This bit stream is used to shift in NIC configuration data. For baseboard implementations, connect the DATA_OUT pin to the Primary Connector. Tie the DATA_OUT pin directly to GND if the scan chain is not used. For NIC implementations, the DATA_OUT pin
			may be left floating if it is not used for add-in card configuration. Pull the DATA_OUT pin up to 3.3Vaux through a 1kOhm resistor.
DATA_IN	OCP_B4	Input	Scan clock data input to the baseboard. This bit stream is used to shift out NIC status bits.



		ı	1
			For baseboard implementations, the DATA_IN
			pin shall be pulled up to 3.3Vaux through a
			10kOhm resistor to prevent the input signal
			from floating if a card is not installed. This pin
			may be left as a no connect if the scan chain is
			not used.
			For NIC implementations, the DATA_IN scan
			chain is required. The DATA_IN connection to
			Shift Registers 0 & 1, as defined in the text and
			Figure 18, are required.
LD#	OCP_B3	Output	Scan clock shift register load. Used to latch
			configuration data on the add-in card.
			For baseboard implementations, the LD# pin
			shall be pulled up to 3.3Vaux through a 1kOhm
			resistor if the scan chain is not used to prevent
			the add-in card from erroneous data latching.
			For NIC implementations, the LD# pin
			implementation is required. The LD# pin must
			be connected to Shift Registers 0 & 1 as
			defined in the text and Figure 18. Pull the LD#
			pin up to 3.3Vaux through a 1kOhm resistor.

The scan chain provides side band status indication between the add-in card and the baseboard. The scan chain bit definition is defined in the two tables below. The scan chain data stream is 32-bits in length for both the DATA_OUT and the DATA_IN streams. The scan chain implementation is optional on the host, but is mandatory on all OCP NIC 3.0 cards. The scan chain components operates on the 3.3Vaux power domain.

The DATA_OUT bus is an output from the host. The DATA_OUT bus provides initial configuration options to the add-in card. At the time of this writing, the default

implementation does not use the DATA_OUT stream and is not implemented on the NIC. However, all baseboard systems that implement the Scan Chain shall connect DATA_OUT between the platform and the Primary Connector for future-proofing NIC implementations and subsequent revisions of this specification.

Byte.bit	DATA_OUT Field	Default	Description
	Name	Value	
0.[07]	RSVD	0b000000	Reserved. Byte 0 value is 0h00.
1.[07]	RSVD	0h00	Reserved. Byte 1 value is 0h00.
2.[07]	RSVD	0h00	Reserved. Byte 2 value is 0h00.
3.[07]	RSVD	0h00	Reserved. Byte 3 value is 0h00.

Table 17: Pin Descriptions – Scan Chain DATA_OUT Bit Definition

The DATA_IN bus is an input to the host and provides NIC status indication. The default implementation is completed with two 8-bit 74LV165 parallel in to serial out shift registers in a cascaded implementation. Up to four shift registers may be implemented to provide additional NIC status indication to the host platform.

DATA_IN shift registers 0 & 1 are mandatory for all cards. DATA_IN shift registers 2 & 3 are optional depending on the card type and fields being reported to the host. DATA_IN shift register 2 may be used to indicate future defintions of the scan chain bit stream. DATA_IN shift registers 3 (in conjunction with shift register 2) are required for reporting link/activity indication on card implementations with 5-8 ports.

The host should read the DATA_IN bus multiple (TBD) times to qualify the incoming data stream.

A 1kOhm pull up resistor shall be implemented on the NIC to the SER input of the last shift register on the DATA_IN scan chain to maintain a default bit value of 0b1 for unused bits for implementations using less than four shift registers.

Table 18: Pin Descriptions – Scan Bus DATA_IN Bit Definition



Byte.bit	DATA_OUT Field	Default	Description
	Name	Value	
0.0	PRSNTB[0]#	0bX	PRSNTB[3:0]# value is mirrored from the
0.1	PRSNTB[1]#	0bX	Primary Connector.
0.2	PRSNTB[2]#	0bX	
0.3	PRSNTB[3]#	0bX	
0.4	WAKE_N	0bX	PCIe WAKE_N signal is mirrored from the
			Primary Connector.
0.5	TEMP_WARN	0b0	Temperature monitoring pin from the on-
			card thermal solution. This pin is asserted
			high when temperature sensor exceeds the
			temperature warning threshold.
0.6	TEMP_CRIT	0b0	Temperature monitoring pin from the on-
			card thermal solution. This pin is asserted
			high when temperature sensor exceeds the
			temperature critical threshold.
0.7	FAN_ON_AUX	0b0	When high, FAN_ON_AUX requests the
			system fan to be enabled for extra cooling in
			the S5 state.
1.0	LINK0	0b1	Port 03 link indication. Active low.
1.1	LINK1	0b1	
1.2	LINK2	0b1	0b0 – Link LED is illuminated on the host
1.3	LINK3	0b1	platform.
			0b1 – Link LED is not illuminated on the host
			platform.
			Steady = link is detected on the port.
			Off = no link is detected on the port.
1.4	ACT0	0b1	
1.5	ACT1	0b1 0b1	Port 03 activity indication. Active low.
		0b1 0b1	
1.6	ACT2		platform.
1.7	ACT3	0b1	μιατιοιτιι.

		0b1 – Link LED is not illuminated on the host
		platform.
		Steady = no activity is detected on the port
		Blink = activity is detected on the port.
		Off = no link, see also LINK[3:0] LED bits.
		The LED blink duty cycle is dependent on the
		add-in card implementation. The
		recommended duty cycle is 50%.
ScanChainVer[0]	0b1	ScanChainVer[1:0] is used to indicate the scan
ScanChainVer[1]	0b1	chain bit definitions. The encoding is as
		follows:
		0b11 – Scan chain bit definitions version 1
		corresponding to OCP 3.0 spec version 1.0.
		All all li
DCVD	Ol- 1	All other encodings are reserved.
		Byte 2 bits [2:7] are reserved. These bits shall
		default to the value of 0b1. These bits may be used in future versions of the scan chain.
		be used in future versions of the scan chain.
		Don't 4.7 link in direction. A stine law
		Port 47 link indication. Active low.
		0b0 – Link LED is illuminated on the host
		platform.
LIINN/	ODI	0b1 – Link LED is not illuminated on the host
		platform.
		piationii.
		Steady = link is detected on the port.
		Off = no link is detected on the port.
	1	ScanChainVer[1] Ob1



3.4	ACT4	0b1	Port 47 activity indication. Active low.
3.5	ACT5	0b1	
3.6	ACT6	0b1	0b0 – Link LED is illuminated on the host
3.7	ACT7	0b1	platform.
			0b1 – Link LED is not illuminated on the host
			platform.
			Steady = no activity is detected on the port
			Blink = activity is detected on the port.
			Off = no link, see also LINK[3:0] LED bits.

Host PLD 74LV594 The 74LV594 DATA_OUTs hift register has no defined function in the current OCP NIC 3.0 specification and is VCC QB SER DATA OUT QD QE CLK (12.5MHz) SRCLRn QF OG LD_N QH **RCLRn** Connector Boundary QH' 74LV165 #0 PRSNTB[0]# (Mirrored from Primary Connector) PRSNTB[1]# (Mirrored from Primary Connector) C D PRSNTB[2]# (Mirrored from Primary Connector) CLK_INH PRSNTB[3]# (Mirrored from Primary Connector) SH/LDn TEMP_WARN
TEMP_CRIT G DATA_IN FAN_ON_AUX QH' SER 3.3 Vaux 74LV165 #1 VCC LINK1 (Active Low = ON, default 0b1) LINK2 (Active Low = ON, default 0b1) C D CLK INH LIN K3 (Active Low = ON, default 0b1) ACTO (Active Low = ON, default 0b1) ACT1 (Active Low = ON, default 0b1) 3.3 Vaux SH/LDn G ACT2 (Active Low = ON, default 0b1) ACT3 (Active Low = ON, default 0b1) Н Ohm QH' SER GND Implement a 1kOhm pull up to 3.3Vau x for the last shift register on the bus Optional depending on implementation 74LV165 #2 VCC CLK INH D SH/LDn н OH' SER GND 74LV165#3 VCC CLK CLK_INH SH/LDn G н QH' SFR GND

Figure 18: Scan Bus Connection Example



3.5.4 Primary Connector Miscellaneous Pins – OCP Bay (Primary Connector)

This section provides the miscellaneous pin assignments for the pins on the Primary Connector OCP Bay. The AC/DC specifications are defined in the PCIe CEM Specification, Rev 4.0 and Section 3.12. An example connection diagram is shown in Figure XXX.

Table 19: Pin Descriptions – Miscellaneous 2

Signal Name	Pin #	Baseboard	Signal Description
		Direction	orginal z esempaten
PWRBRK#	OCP_B2	Output,	Power break. Active low, open drain.
		OD	This signal is pulled up to 3.3Vaux on the add-in card with a minimum of 95kOhm and the baseboard with a stiffer resistance inorder to meet the timing specs as shown in the PCIe CEM Specification.
			This signal is driven low by the baseboard and is used to notify that an Emergency Power Reduction State is requested. The addin card shall move to a lower power consumption state.
NIC_PWR_GOOD	OCP_B1	Input	NIC Power Good. Active high. This signal is driven by the add-in card.
			When high, this signal indicates that all of the add-in card power rails are operating within nominal tolerances.
			When low the add-in card power supplies are not yet ready or are in a fault condition.
			For baseboards, this pin may be connected to the platform I/O hub as a NIC power health

			status indication. This signal is pulled down to ground with a 100kOhm resistor on the baseboard to prevent a false power good indication if no add-in card is present.
			For add-in cards this signal may be implemented by a cascaded power good or a discrete power good monitor output.
GND	OCP_A6	GND	Ground return; a total of 5 ground pins are
	OCP_A10		on the OCP bay area.
	OCP_A13		
	OCP B10		
	OCP_B13		

3.6 PCIe Bifurcation Mechanism

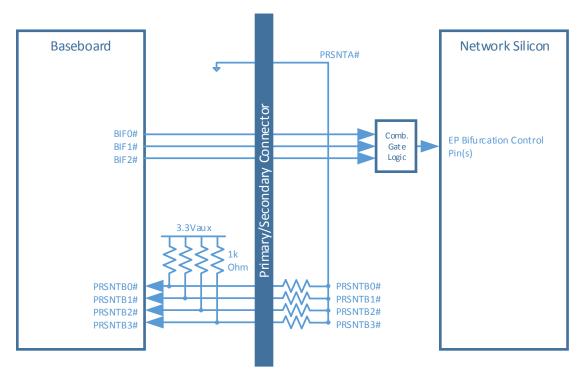
OCP3.0 baseboards and add-in cards support multiple bifurcation combinations. Single socket baseboards with a single or multiple root ports, as well as a multi-socket baseboards with a single or multiple root ports are supported. The bifurcation mechanism also supports add-in cards with a single or multiple end points. These features are accomplished via I/O pins on the Primary and Secondary connector:

- PRSNTA#, PRSNTB[3:0]#. The PRSNTA# pin connects to the PRSNTB# pins as a hard coded value on the add-in card. The encoding of the PRSNTB[3:0]# pins allows the baseboard to determine the PCIe Links available on the add-in card.
- BIF[3:0]#. The BIF# pin states are controlled by the baseboard and allows the baseboard
 to override the default end point bifurcation for silicon that support bifurcation.
 Additional combinatorial logic is required and is specific to the card silicon. The
 combinatorial logic is not covered in this specification.

The high level bifurcation connections are shown in Figure 19.

Figure 19: PCIe Bifurcation Pin Connections Support





3.6.1 PCIe Add-in Card to Baseboard Bifurcation Configuration (PRSNTA#, PRSNTB[3:0]#)

The add-in card to baseboard configuration mechanism consists of four dual use pins (PRSNTB[3:0]#) on the add-in card and a grounded PRSNTA# pin on the baseboard. These pins provide card presence detection as well as mechanism to notify the baseboard of the pre-defined PCIe lane width capabilities. The PRSNTB[3:0]# pins are pulled up to 3.3Vaux on the baseboard and are active low signals. A state of 0b1111 indicates that no card is present in the system. Depending on the capabilities of the add-in card, a selection of PRSNTB[3:0]# signals may be strapped to the PRSNTA# signal and is pulled low by the baseboard. The encoding of the PRSTNB[3:0]# bits is shown in Table 20 for x16 and x8 PCIe cards.

3.6.2 PCIe Baseboard to Add-in Card Bifurcation Configuration (BIF[2:0]#)

Three signals (BIF[2:0]#) are driven by the baseboard to notify requested bifurcation on the add-in card silicon. This allows the baseboard to set the lane configuration on the add-in card that supports multiple bifurcation options.

For example, a baseboard that has four separate hosts that support a 4 x4 connection, should appropriately drive the BIF[2:0]# pins per Table 20 and indicate to the add-in card silicon to setup a 4 x4 configuration.

As previously noted, the BIF[2:0]# signals require additional combinatorial logic to decode the BIF[2:0]# value and appropriately apply it to the end-point silicon. The combinatorial logic is not covered in the specification as its implementation is specific to the vendor silicon used.

3.6.3 PCIe Bifurcation Decoder

The combination of the PRSNTB[3:0]# and BIF[2:0]# pins deterministically sets the PCIe lane width for a given combination of baseboard and add-in cards. Table 20 shows the resulting number of PCIe links and its width for known combinations of baseboards and add-in cards.

*Note: The baseboard must disable PCIe lanes during the initialization phase if the number of detected PCIe links are greater than what is supported on the baseboard to prevent a nondeterministic solution. For example, if the baseboard only supports a 1 x16 connection, and the add-in card only supports a 2 x8 connection, the baseboard must disable PCIe lanes 8-15 to prevent any potential LTSSM issues during the discovery phase.



Table 20: PCIe Bifurcation Decoder for x16 and x8 Card Widths

		Host		1 Host	1 Host	1 Host	1 Host	RSVD	RSVD	2 Hosts	4 Hosts	4 or 8 Hosts
		Host CPU Sockets	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	2 Upstream Sockets	1 Upstream Socket 2 Upstream Sockets 4 Upstream Sockets	RSVD	RSVD	2 Upstream Sockets (1 Socket per Host)	4 Upstream Sockets (1 Socket per Host)	418 Upstream Sockets (1 Socket per Host)
Supp	Network Card – Supported PCle Configurations	Total PCIe Links	1 Link (No Bifurcation)	1 or 2 Links	1, 2, or 4 Links	2 Links	4 Links	RSVD	RSVD	2 Links	4 Links	4 or 8 x2 links
		System Support	ž	÷	٦	1x8,1x4,1x2,1x1		BSVD	RSVD			
				2x8,2x4,2x2,2x1	2x8,2x4,2x2,2x1	2 x8, 2 x4, 2 x2, 2x1				2x8,2x4,2x2,2x1		
Minimum					4×4, 4×2, 4×1		4 x4, 4 x2, 4x1				4 84, 4 82, 4 x1	4×2,4×1
Required		System Encoding	00090	00090	00090	00001	00010	00011	0P100	05101	01110	0b111
Card Card	Card Short x16 Cards	Add-in-Card Encoding		1								
	esent Card Not Present		BSVD - Card not present in the sustem	the custom								
			1x8	1×8	9*	1,8	1,4	ŀ	[1,88	1,4	1x2
_	1.8					(Sooket 0 only)	(Socket 0 only)			(Host 0 only)	(Host 0 only)	(Host 0 only)
	1x4,1x2,1x1 1x4	0b1 110	1x4	1×4	184	1x4 (Sooket 0 only)	1x4 (Socket 0 only)		1	1x4 (Host 0 only)	1x4 (Host 0 only)	1x2 (Host 0 only)
	1x2,1x1	0b1 110	1,42	1×2	182	1x2 (Sooket 0 only)	1x2 (Sooket 0 only)			1x2 (Host 0 only)	1x2 (Host 0 only)	1x2 (Host 0 only)
	181	0b1 110	181	is.	181	1x1 (Sooket 0 only)	1x1 (Sooket 0 only)			1x1 (Host 0 only)	181 (Host 0 only)	1k1 (Host 0 only)
1,80	1x8,1x4,1x2,1x1 1x8 Option B 2x4,2x2,2x1	0b1 101	1,88	8×.	188	1x8 (Socket 0 only)	2×4			1x8 (Host 0 only)	2×4	2×2 (Host 0& 1 only)
2 ×80	2 x8,2 x4,2 x2,2 x1 2 x8 Option B 4 x4,4 x2,4 x1	0b1 101	1×8*	2×8	2 x8	2 x8	4×4			2×8	484	2 x2 (Host 0 & 1 only)
1,80	1x8,1x4 2x4, 1x8 Option D 4x2 (First 8 lanes), 4x1	0b11 00	1×8	2×4	5×4	1x8 (Socket 0 only)	2×4	-		1x8 (Host 0 only)	2×4	4 8 2
	ption D	0b1 100	1×16	1×16	1x16	2 x8	4 84	-	-	2 x8	4×4	4 82
RSVD RSVD			BSVD - The encoding of 0b1011 is reserved due to insufficient spacing between PRSNTA and PRSNTB2 pin to provide positive card identification.	51011 is reserved due to in	sufficient spacing between	on PRSNTA and PRSNTB2	pin to provide positive care	Identifica	tion.			
2	2 x4, 2 x2, 2 x1 2 x4 1 x4, 1 x2, 1 x1	051 010	1,4	2×4	2×4	1x4 (Socket 0 only)	2×4			1x4 (Host 0 only)	2 ×4	2 x2 (Host 0 & 1 only)
RSVD RSVD		1 0b1 001	-	-	-	-	-	-	-	-	-	-
RSVD RSVD		001 000			-			-				
1,	1x16,1x8,1x4,1x2,1x1 1x16	060111	1×16	1×16	1×16	1x8 (Sooket 0 only)	1x4 (Socket 0 only)			1x8 (Host 0 only)	1×4 (Host 0 only)	1x2 (Host 0 only)
2 *80	2x8,2x4,2x2,2x1 2x8 Dption A	050 110	1×8.	2×8	2×8	2,48	2×4 (Socket 0 & 2 only)			2×8	2 x4 (Host 0 & 2 only)	1x2 (Host 0 & 1only)
1×16 C	1x16,1x8,1x4,1x2,1x1 1x16 Dption B 2x8,2x4,2x2,2x1	050 101	1×16	1×16	1×16	2 x8	2×4 (Socket 0 & 2 only)			2×8	2 x4 (Host 0 & 2 only)	2 x2 (Host 0 & 1 only)
1×16 C	1x16,1x8,1x4 2x8,2x4,2x2,2x1 1x16 Option C 4x4,4x2,4x1	0b0 100	1×16	1×16	1816	2 x8	4 × 4	-	1	2 48	4×4	2 x2 (Host 0 & 1 only)
	4	060 011	1×4	2×4*	4×4	2x4 (EP 0 and 2 only)	4 84	ı		2x4 (EP 0 and 2 only)	4×4	4 x2 (Host 0 & 1 only)
		000010	-	-	-	-	-	-	-	-	-	-
		000 001			-							
RSVD RSVD	RSVD	000000	-	1	1	1	,	ı	ı	,	•	

3.6.4 Bifurcation Detection Flow

[Need input and clarification from system vendors]

The following detection flow shall be used to determine the resulting link count and lane width based on the baseboard and add-in card configurations.

- 1. The baseboard reads the state of the PRSNTB[3:0]# pins. If the resulting value is not 0b1111, an add-in card is present.
- 2. Firmware determines the add-in card PCIe lane width capabilities per Table 20 by reading the PRSNTB[3:0]# pins.
- 3. The baseboard reconfigures the PCIe bifurcation on its ports to match the highest common lane width and lowest common link count on the card.
- 4. For cases where the baseboard request a link count override (such as requesting a 4-host baseboard requesting 4 x4 operation on a supported card that would otherwise default to a 2 x8 case), the BIF[0:2]# pins would be asserted as appropriate. Doing so assumes the add-in card supports the requested link override.
- 5. PERST# is deasserted after the >100ms window as defined by the PCIe specification.

 Refer to Section 3.12 for timing details.



3.6.5 PCle Bifurcation Examples

For illustrative purposes, the following figures show several common bifurcation permutations.

Figure 20 illustrates a single host baseboard that supports x16 with a single controller add-in card that also supports x16. The PRSTNB[3:0]# state is 0b0111. The BIF[2:0]# state is 0b000 as there is no need to instruct the end-point network controller to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16. The single host baseboard determines that it is also capable of supporting 1 x16. The resulting link width is 1 x16.

1 x16 Add-in Card Network Silicon Single Host **Root Complex** (1 x16) PRSNTA# (1 x16) **REFCLKO REFCLKO** PERSTO# PERSTO# EP #0 (x16)PER[0:15] PET[0:15] PER[0:15] PET[0:15] Boundar∖ BIFO# Comb. **EP Bifurcation Control** [2:0]=0b111 BIF1# Gate Pin(s) (N/A for 1 x16 Logic BIF2# only cards) Connector 3.3Vaux 10k Ohm WAKE# WAKE# PRSNTB0# PRSNTRO# PRSNTB1# PRSNTB1# PRSNTB2# PRSNTB2# PRSNTB3# PRSNTB3# [3:0]=0b0111

Figure 20: Single Host (1 x16) and 1 x16 Add-in Card (Single Controller)

Figure 21 illustrates a single host baseboard that supports 2 x8 with a single controller addin card that also supports 2 x8. The PRSTNB[3:0]# state is 0b0110. The BIF[2:0]# state is

0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 2 x8. The single host baseboard determines that it is also capable of supporting 2 x8. The resulting link width is 2 x8.

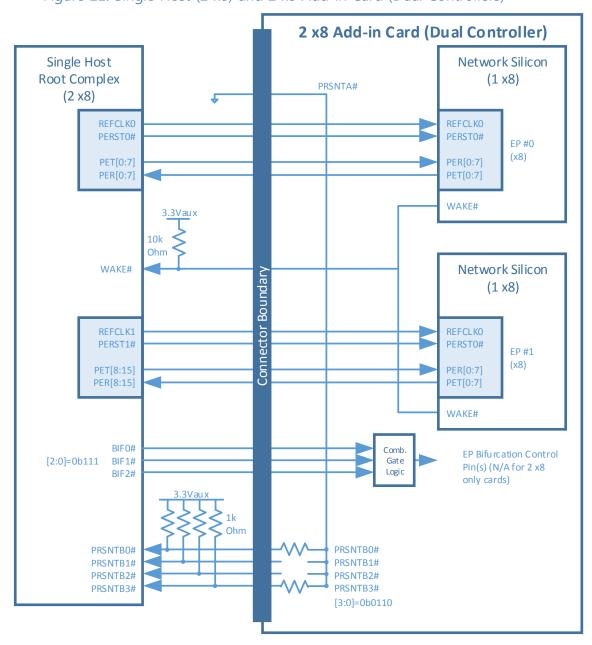


Figure 21: Single Host (2 x8) and 2 x8 Add-in Card (Dual Controllers)



Figure 22 illustrates a four host baseboard that supports 4 x4 with a single controller add-in card that supports 1 x16, 2 x8 and 4 x4. The PRSTNB[3:0]# state is 0b0011. The BIF[2:0]# state is 0b101 as the end point network controller is forced to bifurcate to 4 x4. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16, 2 x8 and 4 x4. The four host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

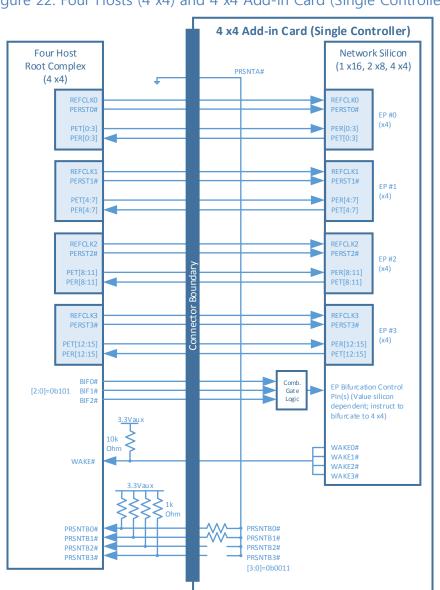


Figure 22: Four Hosts (4 x4) and 4 x4 Add-in Card (Single Controller)

Rev0.01

Figure 23 illustrates a four host baseboard that supports 4 x4 with a four controller add-in card that supports 4 x4. The PRSTNB[3:0]# state is 0b0011. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 4 x4. The four host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

Figure 23: Four Hosts (4 x4) and 4 x4 Add-in Card (Four Controllers)



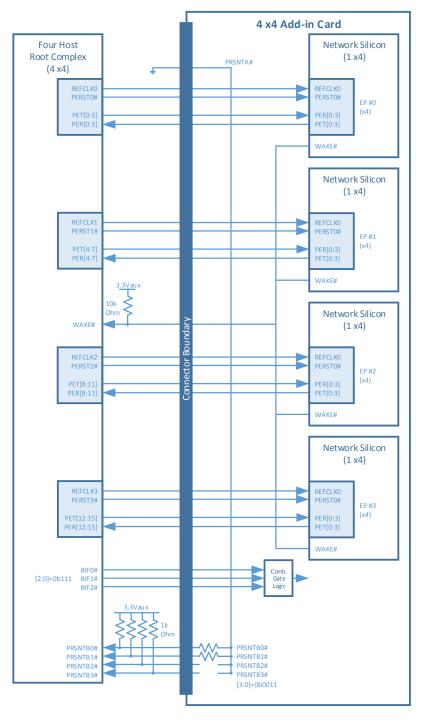


Figure 24 illustrates a single host baseboard that supports 1 x16 with a dual controller addin card that supports 2 x8. The PRSTNB[3:0]# state is 0b0110. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 2 x8. The four host baseboard determines that it is capable of 1x 16, but down shifts to 1 x8. The resulting link width is 1 x8 and only on endpoint 0.

2 x8 Add-in Card (Dual Controller) Network Silicon Single Host (1 x8)**Root Complex** PRSNTA# (1×16) **REFCLKO REFCLKO** PERSTO# PERSTO# EP #0 (x8) PER[0:7] PET[0:15] PET[0:7] PER[0:15] WAKE# 3.3Vaux Lanes 8:15 disabled 10k Ohm WAKE# Network Silicon Connector Boundary (1 x8)**REFCLKO** The second x8 PERSTO# EP #1 is not supported on (x8) PER[0:7] this host. PET[0:7] WAKE# BIFO# Comb. **EP Bifurcation Control** [2:0]=0b111 BIF1# Gate Pin(s) (N/A for 2 x8 Logic BIF2# only cards) PRSNTB0# PRSNTB0# PRSNTB1# PRSNTB1# PRSNTB2# PRSNTB2# PRSNTB3# PRSNTB3# [3:0]=0b0110

Figure 24: Single Host with no Bifurcation (1 x16) and 2 x8 Add-in Card (Two Controllers)



3.7 PCIe Clocking Topology

The OCP NIC 3.0 specification allows for up to four PCIe REFCLKs on the Primary Connector and up to two PCIe REFCLKs on the Secondary Connector. In general, the association of each REFCLK is based on the PCIe Link number on a per connector basis and is shown in Table 21. Cards that implement both the Primary and Secondary connectors have a total of up to 6 REFCLKs.

REFCLK #	Description	Availability (Connector)
REFCLK0	REFCLK associated with Link 0.	Primary and Secondary Connectors.
REFCLK1	REFCLK associated with Link 1.	Primary and Secondary Connectors.
REFCLK2	REFCLK associated with Link 2.	Primary Connector only.
REFCLK3	REFCLK associated with Link 3.	Primary Connector only.

Table 21: PCIe Clock Associations

For each add-in card, the following REFCLK connection rules must be followed:

- For a 1 x16 capable add-in card, REFCLK0 is used for lanes [0:15].
- For a 2 x8 capable add-in card, REFCLK0 is used for lanes [0:7] and REFCLK1 is used for lanes [8:15].
- For a 4 x4 capable add-in card, REFCLK0 is used for lanes [0:3], REFCLK1 is used for lanes [4:7], REFCLK2 is used for lanes [8:11] and REFCLK3 is used for lanes [12:15]. Pins for REFCLK2 and REFCLK3 are described in Section 3.5.1 and are located on the 28-pin OCP bay.

Figure 25: PCIe Interface Connections for 1 x16 and 2 x8 Add-in Cards

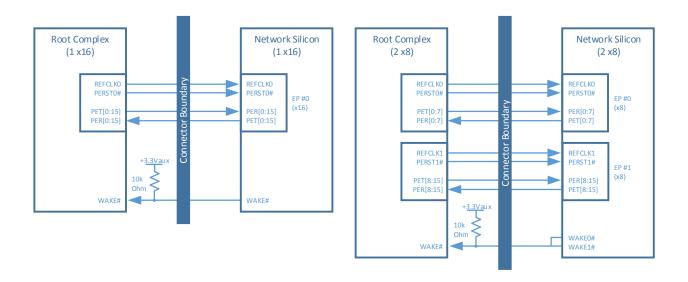
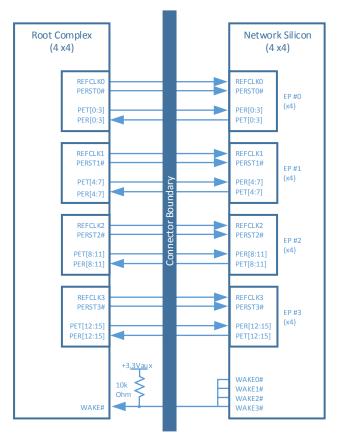


Figure 26: PCIe Interface Connections for a 4 x4 Add-in Card





3.8 PCIe Bifurcation Results and REFCLK Mapping

For the cases where the baseboard and add-in card bifurcation are permissible, this section enumerates all of the supported PCIe link, lane and REFCLK mappings for each supported configuration. The bifurcation decoder is shown in Section 3.6.3.

Table 22: Bifurcation for Single Host, Single Socket and Single Upstream Link
(BIF[2:0]#=0b000)

Single Ho.	et, Single Upet	Single Host, Single Upstresm Socket, One Upstresm Link, no bifurestion	, no bifurcation		1x16, 1x8, 1x4, 1x2, 1																		
Í		Supported Bifurcation	Add-in-Card				10.61310																
Card Card	Card Card Short Modes	Modes	Encoding PREMTRIS-01#	Host	Hostresa Desires	Upstream		Reculting Link	1	1	6 146		7 1	2 2 2	9 9 9 6	2 24	Special Stone Stone	<u>.</u>	9	-	2	2	- 1
- Sa	Not Present	Card Not Present	0b1 111	1 Host	1 Upstream Socket	1Link	00090																
		1x8,1x4,1x2,1x1	0b1 110	1 Host	1 Upstream Socket	1 Link	OPOU	1x8	Link 0,	⊢	Link 0,	Link 0,	⊢	⊢	⊢	Link 0,							
20	1×8								Lane 0	Lane 1	Lane 2	Lone 3	Lone 4	Lane 5 L:	Lane 6 Lt	one 7							
, N	1×4	1x4,1x2,1x1	0P1 110	1 Host	1 Upstream Socket	1 Link	00090	1×4	Link 0.	Link 0, Lane 1	Link 0, Lane 2	Lane 3							_	_	_		_
S	1x2	1x2, 1x1	061110	1 Host	1 Upstream Socket	1 Link	00090	1x2	Link 0, Lane 0	Link 0, Lane 1													
og o	ž	1x1	0b1 110	1 Host	1 Upstream Socket	1 Link	00090	1x1	Link 0, Lane 0														
og Og	1x8 Option B	1x8,1x4,1x2,1x1 1x8 Option B 2x4, 2x2, 2x1	0b1 101	1 Host	1 Upstream Socket	1 Link	00090	1x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link O, Li Lane 5 L	Link O, Lin Lane 6 Lt	Link 0, Lane 7							
	2 x8 Option B	2 x8 Option B 4 x4, 4 x2, 4 x1	0b1 101	1 Host	1 Upstream Socket	1Link	00090	1x8*	Link 0,	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0,	Link O, Li Lane 5 Li	Link O, Lin Lanc 6 Lt	Link 0, Lane 7							
		1x8,1x4	0b1100	1 Host	1 Upstream Socket	1 Link		1x8	Link 0,	Link 0,	Link 0,	Link 0,	⊢	Н	-	Link O,							
2	1x8 Option D	2 x4, 1 x8 Option D 4 x2 (First 8 lanes), 4 x1					00000		Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5 Li	Lane 6 Li	Lane 7			_	_	_		
		1x16,1x8,1x4	0P1100	1 Host	1 Upstream Socket	1Link		1x16	Link 0,	Link 0,	Link 0,	⊢	Link 0,	Link O,	Link O, Lin	Н	Link O, Lin	Link O, Lin	Link O, Lin	⊢	O, Link O,	⊢	-
	4.46 0.45.1	2.x8,2.x4,					00000		Lane 0	Lane 1	Lane 2	Lane 3				Lane 7 La				Lane 11 Lane 12		3 Lane 14	t Lane 15
9	BSVD BSVD		061011	1 Host	1 Unetream Socket	Trink	00000											ŀ	ł	ł	+	ļ	l
		5	0b1 010	1 Host	1 Upstream Socket	1Link	00000	1x4	Link 0,	Link 0,	Link 0,	Link 0,											
20	2 x4	1x4,1x2,1x1					opogo		Lane 0	Lane 1	Lane 2	Lane 3											
9	RSVD RSVD	RSVD for future x8 encoding 0b1001	0b1 001	1 Host	1 Upstream Socket	1 Link	00090																
9	RSVD RSVD	RSVD for future x8 encoding 0b1000	0b1000	1 Host	1 Upstream Socket	1 Link	00090										=						
40	1x16	1x16,1x8,1x4,1x2,1x1	050111	1 Host	1 Upstream Socket	1 Link	00090	1x16	Link O, Lane O	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0, Lane 4	Link O, Li Lane 5 Li	Link O, Lin Lane 6 Lt	Link O, Lin Lane 7 La	Link O, Lin Lane 8 Lar	Link O, Lin Lane 9 Lan	Link O, Lin Lane 10 Lan	Link O, Link O, Lane 11 Lane 12	0, Link 0, 12 Lane 13), Link 0, 13 Lane 14	Link 0,
ţc.	2 x8 Option A	2x8,2x4,2x2,2x1	000110	1 Host	1 Upstream Socket	1 Link	00090	1x8"	Link O, Lane O	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 0,	Link O, Li Lane 5 L	Link O, Lin Lane 6 Lt	Link 0, Lane 7							
Г		1x16,1x8,1x4,1x2,1x1	050 101	1 Host	1 Upstream Socket	1Link	00000	1x16	Link 0,	⊢	Link 0,	⊢	⊢	⊢	⊢	H	Н	-		\vdash	_	_	-
į	1x16 Uption E	1x1b Uption B 2x6, 2x4, 2x2, 2x1 1x16, 1x8, 1x4	001090	1 Host	1 Upstream Socket	1Link		1x16	Link 0,	Link 0,	Link 0,	+	+	+	+	+	+	+	Link 0, Lin	-			Link 0,
Q.	1x16 Option C	2 x8, 2 x4, 2 x2, 2 x1 1 x16 Option C 4 x4, 4 x2, 4 x1					00090		Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5 Li	Lane 6 Lt	Lane 7 La	Lane 8 La	Lane 9 Lan		Lane 11 Lane 12	12 Lane 13	3 Lane 14	_
tc.	4 x 4	4x4,4x2,4x1	000011	1 Host	1 Upstream Socket	1 Link	00090	1x 4 *	Link O, Lane O	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3											
9	RSVD RSVD	RSVD	000010	1 Host	1 Upstream Socket	1Link	00090																
0,	RSVD RSVD	RSVD	000 001	1 Host	1 Upstream Socket	1 Link	00090																
2,0	RSVD	RSVD	000000	1 Host	1 Upstream Socket	1 Link	00000																



Table 23: Bifurcation for Single Host, Single Socket and Single/Dual Upstream Links (BIF[2:0]#=0b000)

Single Hoet, Single Upetream Sock Min Suppor Card Card Short Modes Vidth Name n/a Not Present Card Not				1x16, 1x8, 1x4, 1x2, 1																		
d Card Sho th Name Not Present	Single Host, Single Upstream Socket, One or Two Upstream Links	eam Links		2 x8, 2 x4, 2 x2, 2 x1																		
th Name Not Present	Supported Bifurcation Add-in-Card	Add-in-Card			Unstream	BIF[2:0]																
		PRSMTB[3:0]#	Host	Upstream Devices	Links		Resulting Link Lane 0 Lane 1	Cane 0	Lane 1	Lane 2 Lane 3	ne 3 Lan	T Page	Lane 4 Lane 5 Lane 6	6 Lane i	Lane 7 Lane 8		Lane 3 Lane 10 Lane 11 Lane 12 Lane 13 Lane 14	Lane 11	Lane 12	ane 13 L:		Lane 15
	t Card Not Present	061111	_	1 Upstream Socket	1 or 2 Links	00090																
	1x8,1x4,1x2,1x1	0b1 110	1 Host	1 Upstream Socket	1 or 2 Links	00000	1x8	Link 0,	Link O,	Link O, Lin	Link O, Link O,	c0, Link 0,	O, Link O,	O, Link O,								
1x8						nongo		_	_	Lane 2 La	Lane 3 Lane 4	-	_	-								
7	1x4,1x2,1x1	0P1110	1 Host	1 Upstream Socket	1 or 2 Links	00090	1×4	Link 0,	Link O, Li	Link O, Lin	Link 0,											
**								4	+	+	2							Ī	İ	l	1	
1x2	1x2,1x1	0P1 110	1 Host	1 Upstream Socket	1 or 2 Links	00090	1x2	_	Link 0, Lane 1													
5	1x1	0P1110	1 Host	1 Upstream Socket	1 or 2 Links	00090	1×1	Link 0, Lane 0														
	1x8,1x4,1x2,1x1	0b11 01	1 Host	1 Upstream Socket	1 or 2 Links	00000	1x8	Link 0,	Link 0, Li	⊢	Н	c O, Link O,	0, Link 0,	O, Link O,								
1x8 Option	1x8 Option B 2 x4, 2 x2, 2 x1					00000		Lane 0	Lane 1 L:	Lane 2 La	Lane 3 Lane 4	e4 Lane 5	e S Lane 6	6 Lane 7								
o v8 Ostion	2 x8, 2 x4, 2 x2, 2 x1	0b1 101	1 Host	1 Upstream Socket	1 or 2 Links	00090	2 x8	Link 0,	Link 0, Li	Link 0, Lin	Link O, Link O,	Link 0, Link 0,	O, Linko,	0, Link 0,	Link 1,	Link 1,	Link 1,	Link 1,	Link 1	Link 1,	Link 1,	Link 1,
Oldo ox a	1x8.1x4	061100	1 Host	1 Upstream Socket	1 or 2 Links		1x8	۰	۰	+	۰	+	+	+	۰	+	1	0		٠	+	
1x8 Option	2 x4, 1x8 Option D 4 x2 (First 8 lancs), 4 x1					00090																
	1x16,1x8,1x4	0b1100	1 Host	1 Upstream Socket	1 or 2 Links		1x16	Link 0,	Link O, Li	⊢	⊢	⊢	⊢	⊢	⊢	⊢	Link 0,	Link 0,	Link 0,	-	-	Link 0,
1 vf6 Ontion	2.x8, 2.x4, 1.x16 Operion D. 4.x4, 4.x2 (First 8 Issue), 4.x1					00000			Lane 1 Li	Lane 2 La	Lane 3 Lane 4	e4 Lane 5	e S Lane 6	6 Lane 7	Lane 8	Lane 3	Lane 10	Lane 11	Lane 12	Lane 13	Lane 14 L	one 15
BSVD RSVD	BsvD	061011	1 Host	1 Upstream Socket	1 or 2 Links	00090													İ	l		
	2 x4, 2 x2, 2 x1	0b1 010	1 Host	1 Upstream Socket	1 or 2 Links	00000	1×4	Link 0,	Н	⊢	Link 0,											
2C 2x4	1x4,1x2,1x1							-	Lane 1 L:	Lane 2 La	Lane 3											
RSVD	RSVD for future x8 encoding 0b1001	0b1 001	1 Host	1 Upstream Socket	1 or 2 Links	00090																
RSVD RSVD	RSVD for future x8 encoding	000190	1 Host	1 Upstream Socket	1 or 2 Links	00090																
1×16	1x16,1x8,1x4,1x2,1x1	060111	1 Host	1 Upstream Socket	1 or 2 Links	00090	1×16	Link 0, Lane 0	Link O, Li Lane 1 Li	Link O, Lin Lane 2 La	Link 0, Link 0, Lane 3 Lane 4	c 4 Link 0,	0, Link 0, c5 Lane 6	0, Link 0, 6 Lane 7	Link 0, Lane 8	Link 0, Lane 3	Link 0, Lane 10	Link 0, Lane 11	Link 0, Lane 12	Link 0, Lane 13 L	Link 0, 1 Lane 14 L	Link O, Lane 15
2 v8 Option A	2 x 8, 2 x 4, 2 x 2, 2 x 1	000110	1 Host	1 Upstream Socket	1 or 2 Links	00090	2 x8	Link 0,	Link 0, Li	Link O, Lin	Link 0, Link 0,	Link 0, Link 0,	O, Linko,	O, Link O, 6 Long 7		Link 1,	Link 1,	Link 1,	Link 1,	Link 1,	Link 1,	Link 1,
200	1x16.1x8.1x4.1x2.1x1	000101	1 Host	1 Upstream Socket	1 or 2 Links	1	1x16	+	۰	╀	+	F	╀	+	+	+	Link 0.	Link 0.	Link 0.	+	+	Link 0.
1x16 Option	1x16 Option B 2x8, 2x4, 2x2, 2x1					00000				_	_	_		_			Lane 10	Lane 11	Lane 12			Lane 15
	1x16,1x8,1x4	0001000	1Host	1 Upstream Socket	1 or 2 Links	0000	1×16	Link 0,		⊢	Link O, Link O,	co, Linko,	⊢	O, Link O,	\vdash	⊢	Link O.	Link 0,	Link 0,	_	⊢	Link O.
1x16 Option	1x16 Option C 4x4, 4x2, 4x1					00000		ranco		=			_				Lane 10	Lane	Fanc 16		_	ane io
4 x4	4x4,4x2,4x1	000011	1 Host	1 Upstream Socket	1 or 2 Links	00090	5 × 4.	Link 0, Lane 0	Link O, Li	Link O, Lin Lanc 2 La	Link 0, Lane 3				Link 2, Lane 0	Link 2, Lane 1	Link 2, Lane 2	Link 2, Lane 3				
RSVD RSVD	RSVD	000010	1 Host	1 Upstream Socket	1 or 2 Links	00090																
RSVD RSVD	RSVD	000001	1 Host	Н	1 or 2 Links	00090																
RSVD RSVD	RSVD	000090	1 Host	1 Upstream Socket	1 or 2 Links	00090																

Table 24: Bifurcation for Single Host, Single Socket and Single/Dual/Quad Upstream Links
(BIF[2:0]#=0b000)

				1x16, 1x8, 1x4, 1x2, 1																	
څ	Single Host, Single Upstream Socket, One, Two or Four Upstream Links	Jpstream Links		4 x4, 4 x2, 4 x1																	
	ted Bifurcation					BIFT2:01															_
2	Card Card Short Modes	Escoding PRSNTB[3:0]#	Host	Upstream Devices	Upstream		Resulting Link	Lane 0	Lane	Lane 2	Lane 3 La	Lane 4 La	Lane 5 Lane 6	e 6 Lane 7	7 Lane 8		Lane 10	Lane 11	Lane 12	Lane 9 Lane 10 Lane 11 Lane 12 Lane 13 Lane 14	ne 14 Lane 15
Not Present	Card Not Present	0b1111	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090										-					
1x8	1x8,1x4,1x2,1x1	0b1 110	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	1x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, Lii Lane 3 La	Link O, Lir Lane 4 La	Link O, Link Lane 5 Lan	Link O, Link O, Lane 6 Lane 7	o ~						
1×1	1x4,1x2,1x1	061110	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	1x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3										
1×2	1x2,1x1	001110	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	1x2	Link 0, Lane 0	Link 0, Lane 1	_											
Ξ	121	001110	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	1×1	Link 0, Lane 0													
ption B	1x8, 1x4, 1x2, 1x1 1x8 Option B 2x4, 2x2, 2x1	0b1 101	1Host	1 Upstream Socket	1, 2, or 4 Links	00090	1x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, Li Lane 3 La	Link O, Lir Lanc 4 La	Link 0, Link 0, Lane 5 Lane 6	Link 0, Link 0, Lanc 6 Lanc 7	o ~						
ption B	2 x8, 2 x4, 2 x2, 2 x1 2 x8 Option B 4 x4, 4 x2, 4 x1	0b1 101	1Host	1 Upstream Socket	1, 2, or 4 Links	00090	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, Lin Lane 3 La	Link O, Lir Lane 4 La	Link O, Link Lanc 5 Lan	Link 0, Link 0, Lane 6 Lane 7	0, Link 1, 7 Lane 0	Link 1,	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1,	Link 1, Link 1, Lane 6 Lane 7
ptionD	1x8,1x4 2x4, 1x8 Option D 4x2 (First 8 lancs), 4x1	0b11 00	1Host	1 Upstream Socket	1, 2, or 4 Links	00090	1x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, Link Clane 3 La		Link O, Link Lanc 5 Lan	Link O, Link O, Lane 6 Lane 7	o ~						
	1x16,1x8,1x4	061100	1 Host	1 Upstream Socket	1, 2, or 4 Links	00000	1×16	Link 0,	Link 0,	Link O,	Link O, Li	Link O, Lin	Link O, Link	Link O, Link O,	0, Link 0,	Link 0,	Link 0,	Link O,	Link 0,	Link O,	Link O, Link O,
ption [1x16 Option D 4x4, 4x2 (First 8 lanes), 4x1					00000		Lane	Lane										Lane 12		
RSVD RSVD	BSVD	0b1 011	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090															
S X A	2x4,2x2,2x1 1x4,1x2,1x1	0b1 010	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	2 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, Li Lane 3 La	Link 1, Lin Lane 0 La	Link 1, Link 1, Lane 1 Lane 2	Link 1, Link 1, Lane 2 Lane 3	- ∞						
RSVD RSVD	RSVD for future x8 encoding 0b1001	0b1 001	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090															
RSVD RSVD	RSVD for future x8 encoding	001000	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090															
1x16	1x16,1x8,1x4,1x2,1x1	000111	1Host	1 Upstream Socket	1, 2, or 4 Links	00090	1×16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, Lii Lane 3 La	Link O, Lir Lane 4 La	Link O, Lind Lane 5 Lan	Link O, Link O, Lane 6 Lane 7	0, Link 0, 7 Lane 8	Link 0,	Link 0, Lane 10	Link 0, Lane 11	Link 0, Lane 12	Link 0, Lane 13 L	Link O, Link O, Lane 14 Lane 15
2 x8 Option A	2x8,2x4,2x2,2x1	000110	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, Lin Lane 3 La	Link O, Lir Lane 4 La	Link O, Link Lane 5 Lan	Link 0, Link 0, Lane 6 Lane 7	0, Link 1, 7 Lane 0	Link 1,	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1,	Link 1, Link 1, Lane 6 Lane 7
otion	1x16,1x8,1x4,1x2,1x1 1x16 Option B 2x8,2x4,2x2,2x1	060101	1Host	1 Upstream Socket	1, 2, or 4 Links	00000	1x16	Link 0, Lane 0	Link 0, Lane 1	-	-	\vdash	-	-					Link 0, Lane 12	_	
ption	1x16,1x8,1x4 2x8,2x4,2x2,2x1 1x16 Option C 4x4,4x2,4x1	000100	1Host	1 Upstream Socket	1, 2, or 4 Links	00090	1×16	Link 0, Lane 0	Link 0, Lane 1						_	_			Link 0, Lane 12	_	
4 × 4	4x4,4x2,4x1	060011	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	4 x 4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, Li Lane 3 La	Link 1, Lin Lane 0 La	Link 1, Lin Lane 1 Lan	Link 1, Link 1, Lane 2 Lane 3	1, Link 2, 3 Lane 0	Link 2,	Link 2, Lane 2	Link 2, Lane 3	Link 3, Lane 0	Link 3, L	Link 3, Link 3, Lane 2 Lane 3
RSVD RSVD	RSVD	000010	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090															
RSVD RSVD	RSVD	0P0 001	1 Host		1, 2, or 4 Links	00090															
BSVD BSVD	RSVD	000000	1 Hoet	11 Inchesom Cocket	1 2 or 4 links	00000		l				l									



Table 25: Bifurcation for Single Host, Dual Sockets and Dual Upstream Links (BIF[2:0]#=0b001)

					to the total total																		
Single H	lost, Two Upstro	Single Host, Two Upstream Sockets, Two Upstream Links	9		2 x8, 2 x4, 2 x2, 2x1																		
i,		Supported Bifurcation					BIF[2:0]																
ž ž	Card Card Short Modes	Modes	PRSNTB[3:0]#	Host	Upstream Devices	Upstream		Resulting link Lane 0 Lane 1 Lane 2 Lane 3 Lane 4 Lane 5 Lane 6 Lane 7 Lane 8 Lane 9 Lane 10 Lane 12 Lane 13 Lane 14 Lane 15	tane 0	Lane 1	ane 2	ane 3	ane 4	ane 5 L:	ne 6 La	7 - L2	1 P	e 9 Lan	10 Lane	1 Lane	2 Lane 1:	Lane 1	Lane 15
eye	Not Present	Card Not Present		1 Host	2 Upstream Sockets	2 Links	00001																
ç	1.0	1x8,1x4,1x2,1x1	0P1110	1 Host	2 Upstream Sockets	2 Links	10090	1x8 (Socket (Looks)	Link 0,	Link 0, I	Link 0,	Link 0, L	Link O, I	Link O, Li	Link O, Lin	Link 0, Lanc 7							
8	1×1	1x4,1x2,1x1	061110	1 Host	2 Upstream Sockets	2 Links	009001	1x4 (Socket 0 only)	Link 0,	+	-		-										
ន្ត	1x5	1x2,1x1	061110	1 Host	2 Upstream Sockets	2 Links	10090	1x2 (Socket 0 only)	Link 0, Lane 0														
S	1×1	1x1	0b1110	1 Host	2 Upstream Sockets	2 Links	00001	1x1 (Socket 0 only)	Link 0, Lane 0														
S	1x8 Option B	1x8,1x4,1x2,1x1 1x8 Option B 2x4,2x2,2x1	0b1 101	1 Host	2 Upstream Sockets	2 Links	10090	1x8 (Socket 0 only)	Link 0, Lane 0	Link 0, Lanc 1	Link O, Lanc 2	Link O, L Lane 3	Link O, L	Link O, Li Lane 5 L	Link O, Lin Lanc 6 La	Link 0, Lane 7							
ð	2 x8 Option B	2x8.2x4,2x2,2x1 2x8.0ption B 4x4,4x2,4x1	0b1 101	1 Host	2 Upstream Sockets	2 Links	10090	2 x8	Link 0, Lane 0	Link 0, 1	Link 0, Lane 2	Link O, L	Link O, L	Link O, Li Lane 5 L	Link O, Lin Lanc 6 La	Link O, Lir Lane 7 La	Link 1, Lii Lanc 0 La	Link 1, Lin	Link 1, Link 1, Lane 2 Lane 3	1, Link 1, 3 Lane 4	Link 1,	Link 1, Lanc 6	Link 1, Lane 7
S	1x8 Option D	1x8,1x4 2x4, 1x8 Option D 4x2 (First 8 lanes), 4x1	061 100	1Host	2 Upstream Sockets	2 Links	00001	1x8 (Socket 0 only)	Link 0, Lane 0		Link O, Lane 2	Link 0, L	Link 0, 1 Lane 4	Link O, Li Lane 5 Li	Link O, Lin Lane 6 La	Link 0, Lane 7							
Q q	1v16 Option D	1x16,1x8,1x4 2x8,2x4, 1x16 Detion D. 4x4, 4x2 (First 8 lones), 4x1	061 100	1Host	2 Upstream Sockets	2 Links	00001	2 x8	Link 0, Lane 0	Link 0, 1 Lane 1	Link O, Lane 2	Link 0, L	Link 0, L	Link O, Li Lane 5 Li	Link O, Lin Lane 6 La	Link O, Lir Lane 7 La	Link 1, Lii Lane 0 La	Link 1, Lin Lane 1 Lan	Link 1, Link 1, Lane 2 Lane 3	1, Link 1, 3 Lane 4	Link 1,	Link 1, Lane 6	Link 1, Lane 7
BSVD	RSVD RSVD	RSVD	0b1 011	1 Host	2 Upstream Sockets	2 Links	00000																
į Ω	2×4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1 010	1 Host	2 Upstream Sockets	2 Links	10090	1x4 (Socket 0 only)	Link 0, Lane 0	Link 0,	Link 0, Lane 2	Link 0, Lane 3											
BSVD	RSVD RSVD	BSVD for future x8 encoding 0b1001	061 001	1 Host	2 Upstream Sockets	2 Links	00001																
g	9	1x16,1x8,1x4,1x2,1x1	000111	1 Host	2 Upotream Sockets	2 Links	10090	1x8 (Socket 0 only)	Link 0,	Link 0,	Link 0,	Link 0, L	Link 0, L	Link O, Li	Link O, Lin	Link O, Lane 7	H	H		L			
ş	2 x8 Option A	2x8,2x4,2x2,2x1	000110	1Host	2 Upstream Sockets	2 Links	10090	2 x8	Link 0, Lane 0	-	-	-	-	-	-		Link 1, Lii Lane 0 La	Link 1, Lin Lane 1 Lan	Link 1, Link 1, Lane 2 Lane 3	1, Link 1, 3 Lane 4	Link 1,	Link 1, Lane 6	Link 1,
ĝ	1x16 Option B	1x16,1x8,1x4,1x2,1x1 1x16 Option B 2x8,2x4,2x2,2x1	060101	1Host	2 Upstream Sockets	2 Links	009001	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, L Lane 3	Link O, L	Link O, Li Lane 5 L	Link O, Lin Lane 6 La	Link O, Lir Lane 7 La	Link 1, Lin Lane 0 La	Link 1, Lin Lane 1 Lan	Link 1, Link 1, Lane 2 Lane 3	1, Link 1, 3 Lane 4	Link 1,	Link 1, Lane 6	Link 1, Lane 7
û	1x16 Option C	1x16,1x8,1x4 2x8,2x4,2x2,2x1 1x16 Option C 4x4,4x2,4x1	0001000	1 Host	2 Upetream Sockets	2 Links	009001	2 x 8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, L	Link 0, L	Link 0, Li Lane 5 Li	Link O, Lin Lane 6 La	Link O, Lir Lane 7 La	Link 1, Lane 0 La	Link 1, Lin Lane 1 Lan	Link 1, Link 1, Lane 2 Lane 3	1, Link 1, 3 Lane 4	Link 1,	Link 1, Lane 6	Link 1, Lane 7
4	4 ×4	4 x4, 4 x2, 4 x1	060011	1 Host	2 Upstream Sockets	2 Links	00001	2 x4 (EP 0 and 2 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3				Li Li	Link 2, Lir Lane 0 La	Link 2, Link Lane 1 Lan	Link 2, Link 2, Lane 2 Lane 3	പ്ര			
BSVD	RSVD RSVD	RSVD	000 010	1 Host	2 Upotream Sockets	2 Links	00001												+	+			
HSVD	RSVD RSVD	RSVD	00001	1 Host	2 Upstream Sockets	2 Links	00000								+	+	+	+	+	+	1		
HOVE	HSVD HSVD	Havu	nenene	1 Host	Z Upotream Sockets	Z LINKS	npgn																

Table 26: Bifurcation for Single Host, Four Sockets and Dual Upstream Links
(BIF[2:0]#=0b010)

Single Ho	set, Four Upetre	Single Hozt, Four Upstream Sockets, Four Upstream Links	2		4 x4, 4 x2, 4x1																		
£ }	Min Suppor	Supported Bifurcation	Add-in-Card			Hactran	BIF[2:0]																
Vidth Hame	Hame		PRSMTB[3:0]#	Host	Upstream Devices	Links		Resulting Link	Lane 0		Lane 1 Lane 2	Lane 3	Lane 4	Lane 5 Lane 6	ane 6 La	Lane 7 Lan	Lane 8 Lan	e 9 Lan	10 Lane	Lane 9 Lane 10 Lane 11 Lane 12 Lane 13 Lane 14 Lane 15	12 Lane	3 Lane 1	4 Lane
- c _l u	Not Present	Card Not Present	0b1 111	1 Host	4 Upstream Sockets	4 Links	05010																
20	1x8	1x8,1x4,1x2,1x1	0b1 110	1 Host	4 Upstream Sockets	4 Links	05010	1x4 (Socket 0 only)	Link O, Lane O	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3											
8		1x4,1x2,1x1	0b1 110	1 Host	4 Upstream Sockets	4 Links	05010	1x4	Link 0,	₩	Link 0,	Link 0,											
	ŧX.	1x2.1x1	051110	1 Host	4 Upstream Sockets	4 Links	-	1x2	Link 0.	+	Tauc C	raue o							H	+	+		-
S	1x2				compounds.		00010	(Socket 0 only)	Lane 0	_													
3C	1×1	1x1	0b1 110	1 Host	4 Upstream Sockets	4 Links	00000	1x1 (Socket 0 only)	Link O, Lane O														
200	1x8 Option B	1x8,1x4,1x2,1x1 1x8 Option B 2x4,2x2,2x1	0b1101	1 Host	4 Upstream Sockets	4 Links	00000	2 x4	Link O, Lane O	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, L	Link 1, Li Lane 2 La	Link 1, Lane 3							
Q.	2 x8 Option B	2x8.2x4,2x2,2x1 2x8 Option B 4x4,4x2,4x1	0b1 101	1 Host	4 Upstream Sockets	4 Links	00000	4 x4	Link O, Lane O	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, L	Link 1, Li Lane 2 La	Link 1, Lin Lane 3 La	Link 2, Lin Lane 0 La	Link 2, Link 2, Lane 1 Lane 2	Link 2, Link 2, Lane 2 Lane 3	2, Link3,	3, Link 3, 0 Lane 1	Link3, Lane2	Link 3, Lane 3
٤	0.00	2.x4,	0P1100	1Host	4 Upstream Sockets	4 Links	0090	2 x 4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, L	Link 1, Li Lane 2 La	Link 1, Lane 3							
T	a lloydo ox -	1x16,1x8,1x4	061100	1 Host	4 Upstream Sockets	4 Links		\$×\$	Link 0,	Link 0,	Link 0,	Link 0,	Link 1,	+	+	-	-	-	-	-	-	+	+
Ş	1 v16 Option D	2 x8, 2 x4, 1 x16 Option D 4 x4, 4 x2 (First 8 lance) 4 x1					000010		Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 2 La	Lane 3 La	Lane 0 Lan	Lane 1 Lan	Lane 2 Lane 3	2 Lane 0	0 Lane 1	Lane 2	Lane 3
6	RSVD	RSVD	0b1 011	1 Host	4 Upstream Sockets	4 Links	05010												H	L			L
,	2 x4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1 010	1 Host	4 Upstream Sockets	4 Links	05010	2 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, L	Link 1, Li	Link 1, Lane 3							
e	Г	RSVD for future x8 encoding 0b1001	061001	1 Host	4 Upstream Sockets	4 Links	00010							Н	\vdash							L	L
9	RSVD RSVD	RSVD for future x8 encoding	0b1 000	1 Host	4 Upstream Sockets	4 Links	05010																
- Q	1x16	1x16,1x8,1x4,1x2,1x1	050111	1 Host	4 Upstream Sockets	4 Links	00000	1x4 (Socket 0 only)	Link O, Lane O	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3											
Q.	2 x8 Option A	_	000110	1 Host	4 Upstream Sockets	4 Links	00000	2 x4 (Socket 0 & 2 only)	Link O, Lane O	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3				5 5	Link 2, Lin Lane 0 La	Link 2, Link 2, Lane 1 Lane 2	.2, Link2, c.2 Lane3	ର ପ୍ର			
Q.	1x16 Option B	1x16.0ption B 2x8,2x4,2x2,2x1	000101	1 Host	4 Upstream Sockets	4 Links	00000	2 x4 (Socket 0 & 2 only)	Link O, Lane O		Link 0, Lane 2	Link 0, Lane 3				5 5	Link 2, Lin Lane 0 Lan	Link 2, Link 2, Lane 1 Lane 2	Link 2, Link 2, Lane 2 Lane 3	ର ପ୍ର			
û	1x16 Option C	1x16,1x8,1x4 2x8,2x4,2x2,2x1 1x16 Option C 4x4,4x2,4x1	000100	1 Host	4 Upstream Sockets	4 Links	00000	4 x 4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, L	Link 1, Li Lane 2 La	Link 1, Lin Lane 3 La	Link 2, Lin Lane 0 La	Link 2, Link 2, Lane 1 Lane 2	Link 2, Link 2, Lane 2 Lane 3	2, Link3, 3 Lane 0	3, Link 3, 0 Lane 1	Link 3,	Link 3,
	×4	4 x4, 4 x2, 4 x1	000 011	1 Host		4 Links	05010	4 ×4	Link O, Lane O	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, Lane 0	Link 1, I Lane 1 L	Link 1, Li Lane 2 La	Link 1, Lin Lane 3 La	Link 2, Lin Lane 0 La	Link 2, Link 2, Lane 1 Lane 2	Link 2, Link 2, Lane 2 Lane 3	2, Link 3, 3 Lane 0	3, Link 3, 0 Lane 1	Link 3, Lane 2	Link 3, Lane 3
RSVD		RSVD	000010	1 Host		4 Links	05010																
2	RSVD RSVD	RSVD	000001	1Host	-	4 Links	06010												1				
000	RSVO	Bsvo	000000	Host	A Instruction Nockets	d inke	05040																



Table 27: Bifurcation for Dual Host, Dual Sockets and Dual Upstream Links (BIF[2:0]#=0b101)

the Card Short dth Name And Precent 1x8 1x8 1x8 1x8 1x8 1x8 1x8 1x	Supported Bifurcation Additional Models Add-in-Card															ŀ		ļ				
1x8 1x4 1x8 ind Not Present xe, 1x4, 1x2, 1x1 x4, 1x2, 1x1	Encoding			Upstream	BIF[2:0]																	
1x8 1x2 1x2 1x1 1x1 1x8 Option B	ard Not Prezent x8, 1x4, 1x2, 1x1 x4, 1x2, 1x1	PRSMTB[3:0]#	Host	Upstream Devices	Links		Resulting Link	Lane 0	Lane 0 Lane 1	Lane 2	Lane 3 Lane 4	ae 4 La	ne 5 Lan	Lane 5 Lane 6 Lane 7 Lane 8 Lane 9 Lane 10 Lane 11 Lane 12 Lane 13 Lane 14 Lane 15	7 Lane	8 Lane 5	Lane 10	Lane 11	Lane 12	Lane 13	38e 14 L	ane 15
1x8 1x2 1x2 1x8 Option B	x8,1x4,1x2,1x1 x4,1x2,1x1 x2,1x1		2 Host	2 Upstream Sockets	2 Links	0b101							ш									
1x2 1x1 1x1 1x8 Option B	x4,1x2,1x1 x2,1x1	0b1 110	2 Host	2 Upstream Sockets	2 Links	06101	1x8 (Host 0 only)	Link O, Lane O	Link O, Lane 1	Link 0, L	Link O, Li Lane 3 Lt	Link O, Lir Lanc 4 La	Link O, Link Lane 5 Lan	Link O, Link O, Lane 6 Lane 7	· -							
1x2 1x1 1x8 Option B 2 x8 Option B	x2,1x1	0b1 110	2 Host	2 Upstream Sockets	2 Links	10140	1x4 (Host 0 only)	Link O, Lane O	Link 0, Lane 1	Link 0, L	Link 0, Lane 3											
1x8 Option B 2x8 Option B		061110	2 Host	2 Upstream Sockets	2 Links	10140	1x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1													
1x8 Option B 2x8 Option B	LX	061110	2 Host	2 Upstream Sockets	2 Links	10140	1x1 (Host 0 only)	Link 0, Lane 0														
4C 2 x8 Option B 4:	1x8,1x4,1x2,1x1 2x4,2x2,2x1	0b1 101	2 Host	2 Upstream Sockets	2 Links	10140	1x8 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, L	Link O, Li Lane 3 L;	Link O, Lir Lane 4 La	Link O, Link Lane 5 Lan	Link 0, Link 0, Lane 6 Lane 7	- °							
	2x8,2x4,2x2,2x1 4x4,4x2,4x1	0b1 101	2 Host	2 Upstream Sockets	2 Links	10140	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, L	Link O, Li Lane 3 L;	Link O, Lir Lane 4 La	Link O, Link Lane 5 Lan	Link 0, Link 0, Lane 6 Lane 7	0, Link 1,	Link1,	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
	1x8,1x4	0b1100	2 Host	2 Upstream Sockets	2 Links		1x8	Link O,	Н	Н	-				0,		-	Н	-			
2C 1x8 Option D 4:	2 x4, 1x8 Option D 4 x2 (First 8 lanes), 4 x1					1040	(Host 0 only)	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4 La	Lane 5 Lan	Lane 6 Lane 7	-							
T	1x16,1x8,1x4	0b1100	2 Host	2 Upstream Sockets	2 Links		2 x8	Link O,	-	Н	-	Н	-	Н		-	-	-	_	Link 1,	-	Link 1,
4C 1x16 Option D 4:	2 x8, 2 x4, 1 x16 Option D 4 x4, 4 x2 (First 8 lanes), 4 x1					10140		Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5 Lan	Lane 6 Lane 7	7 Lane 0	0 Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7
RSVD RSVD R	RSVD		2 Host	2 Upotream Sockets	2 Links	0b101																
2C 2x4 1x	2x4,2x2,2x1 1x4,1x2,1x1	0b1 010	2 Host	2 Upstream Sockets	2 Links	10140	1x4 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, L	Link 0, Lane 3											
	RSVD for future x8 encoding 0b1001	061001	2 Host	2 Upotream Sockets	2 Links	06101														Ī	i	
HSVU HSVU HS	RSVD for future x8 encoding	000190	2 Host	2 Upstream Sockets	STINKS	10140				4	+	4	+	+								I
4C 1x16 1x	1x16, 1x8, 1x4, 1x2, 1x1	060111	2 Host	2 Upstream Sockets	2 Links	0b101	1x8 (Host 0 only)	Link 0, Lane 0							٦.							
4C 2 x8 Option A	2x8,2x4,2x2,2x1	000110	2 Host	2 Upstream Sockets	2 Links	06101	2 x8	Link O, Lane O		Link 0, L	Link O, Li Lane 3 Lt	Link O, Lir Lane 4 La	Link O, Link Lane 5 Lan	Link O, Link O, Lane 6 Lane 7	O, Link 1,	Link 1, 0 Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
1x 4C 1x16 Option B 2:	1x16.0ption B 2x8, 2x4, 2x2, 2x1	000101	2 Host	2 Upstream Sockets	2 Links	10140	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, L	Link O, Li Lane 3 L;	Link O, Lir Lane 4 La	Link O, Link Lane 5 Lan	Link O, Link O, Lane 6 Lane 7	0, Link 1,	Link1,	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
1x16,1x8,1x4 2x6,2x4,2x2 4C 1x16 Option Claims 4x2 4x1	1x16, 1x8, 1x4 2x8, 2x4, 2x2, 2x1 4x4, 4x2, 4x1	0001000	2 Host	2 Upstream Sockets	2 Links	10140	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link O, L Lane 2	Link O, Li Lane 3 Lt	Link O, Lir Lane 4 La	Link O, Link Lane 5 Lan	Link O, Link O, Lane 6 Lane 7	0, Link 1,	l. Link 1, 0 Lane 1	Link 1, Lane 2	Link 1, Lane 3	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
	4 x 4, 4 x 2, 4 x 1	000011	2 Host	2 Upstream Sockets	2 Links	10140	2 x4 (EP 0 and 2 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, L	Link 0, Lane 3				Link 1, Lane 0	Link 1,	Link 1, Lane 2	Link 1, Lane 3				
	RSVD			2 Upstream Sockets	2 Links	05101																
	BSVD			2 Upstream Sockets	2 Links	0b101														Ī		
RSVD RSVD R8	RSVD	000000	2 Host	2 Upstream Sockets	2 Links	0b101																

Table 28: Bifurcation for Quad Host, Quad Sockets and Quad Upstream Links (BIF[2:0]#=0b110)

å	Quad Host, Four Upstream Sockets, Four Upstream Links	20		4 x4, 4 x2, 4 x1																		
Mis Card Card Sho Vidth Name	Min Supported Bifurcation Card Card Short Modes Width Name	Add-in-Card Encoding PRSMTBf3:01#	Host	Unstream Devices	Upstream	BIF[2:0]	Besulting Link Lane 0 Lane 1	0 346		2000	lane 3 Lane 4 Lane 5 Lane 6	7	2		lane 7 Lane 8	8	6	9	1 anc 9 1 anc 10 1 anc 11 1 anc 12 1 anc 14 1 anc 15	130	130	1386 15
Not Present	t Card Not Present	0b1 111		4 Upstream Sockets	4 Links	06110																
×		0b1 110	4 Host	4 Upstream Sockets	4 Links	01110	1x4 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lanc 3											
1×4	1x4,1x2,1x1	0P1 110	4 Host	4 Upstream Sockets	4 Links	01110	1x4 (Host 0 only)	Link 0, Lane 0	-	-	Link 0, Lane 3											
, Si	1x2,1x1	0b1 110	4 Host	4 Upstream Sockets	4 Links	01110	1x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1													
ž	1x1	0b1110	4 Host	4 Upstream Sockets	4 Links	01110	1x1 (Host 0 only)	Link 0, Lane 0														
Option	1x8.0ption B 2x4, 2x2, 2x1	0b1 101	4 Host	4 Upstream Sockets	4 Links	01110	2×4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, L	Link 1, L Lane 0 L	Link 1, Lir Lane 1 La	Link 1, Lin Lanc 2 Lan	Link 1, Lane 3							
Option	2 x 8, 2 x 4, 2 x 2, 2 x 1 2 x 8 Option B 4 x 4, 4 x 2, 4 x 1	0b1 101	4 Host	4 Upstream Sockets	4 Links	01110	4 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, L	Link 1, L	Link 1, Lir Lane 1 Lar	Link 1, Lin	Link 1, Link 2, Lane 3 Lane 0	2, Link 2, .0 Lane 1	2, Link 2, 1 Lane 2	c. Link2, 2 Lane3	Link 3,	Link 3, Lane 1	Link 3, Lane 2	Link 3, Lane 3
Option	1x8,1x4 2x4, 1x8 Option D 4x2 (First 8 lancs), 4x1	061 100	4 Host	4 Upstream Sockets	4 Links	01110	2 x 4	Link 0, Lane 0	Link 0, Lane 1		Link 0, L	Link 1, L Lane 0 L	Link 1, Lir Lane 1 La	Link 1, Lin Lane 2 Lan	Link 1, Lane 3							
Optio	1x16,1x8,1x4 2x8,2x4, 1x16 Option D 4x4,4x2 (First 8 lance), 4x1	061 100	4 Host	4 Upstream Sockets	4 Links	01110	4×4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Li Lane 3 Li	Link 1, Lane 0	Link 1, Lin Lane 1 La	Link 1, Lin Lane 2 Lan	Link 1, Link 2, Lane 3 Lane 0	2, Link 2, .0 Lane 1	2, Link 2, 1 Lane 2	2. Link 2, 2. Lane 3	Link 3.	Link 3, Lane 1	Link 3, Lane 2	Link 3. Lane 3
RSVD RSVD	RsvD	0b1 011	4 Host	4 Upstream Sockets	4 Links	06110										H		ŀ	L			
2 ×4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	0b1 010	4 Host	4 Upstream Sockets	4 Links	06110	2 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, L	Link 1, L Lane 0 L	Link 1, Lir Lane 1 Lar	Link 1, Lin Lane 2 Lan	Link 1, Lane 3							
BSVD	RSVD for future x8 encoding		4 Host	4 Upstream Sockets	4 Links	06110							+	H		H	4					
HSVD HSVD	1x16, 1x8, 1x4, 1x2, 1x1	060111	4 Host	4 Upstream Sockets 4 Upstream Sockets	4 Links	06110	1×4	Link 0,	Link 0,	Link 0,	Link 0,	t	t	+	+	+	+		-			
1×16	2 x 8, 2 x 4, 2 x 2, 2 x 1	050110	4 Host	4 Upstream Sockets	4 Links	06110	(Host 0 only) 2 x4	Link 0,	+	+	Link 0,				Link 1,			_				
2 x8 Option A	1x16,1x6,1x4,1x2,1x1	060 101	4 Host	4 Upstream Sockets	4 Links	06110	(Host 0 & 2 only)	Link 0,	+	+	Link 0,	t	+	+	Link 1,	+	+	+				
e de la composição de l	1x16 Option B 2x8, 2x4, 2x2, 2x1 1x16 Option B 1x16, 1x8, 1x4 1x16, 1x8, 1x4 2x8, 2xx, 2xx, 2x1 4x8, 0x1, 0x1, 0x2, 0x3, 0x4, 0x2, 0x1	000100	4 Host	4 Upstream Sockets	4 Links	09410	(Host 0 & 2 only) 4 x4	Link 0, Line 0	Link 0, Line 1	Link 0, Lane 2	Link 0, L	Link 1, L	Link 1, Lir Lane 1 La	Link 1, Lin	Link 1, Link 2, Lane 3 Lane 0	2, Link2, 0 Lane1	Link2, Link2,	2 Link2, 2 Link2, 2 Lane 3	Lane 0	Link 3, Lane 1	Link 3, Lane 2	Link 3, Lane 3
**	4 x4, 4 x2, 4 x1	050 011	4 Host	4 Upstream Sockets	4 Links	01110	4 x 4	Link 0,	Link 0, Lane 1	Link 0, Lane 2	Link O, L	Link 1, L	Link 1, Lir Lane 1 La	Link 1, Link 1, Lane 2 Lane 3	Link 1, Link 2, Lane 3 Lane 0	2, Link 2, 0 Lane 1	2, Link 2, 1 Lane 2	tink 2,	Link 3,	Link 3, Lane 1	Link 3, Lane 2	Link 3, Lane 3
RSVD RSVD	RSVD		4 Host	4 Upstream Sockets	4 Links	01110			Н	Н	Н	Н	Н	Н	₩	Н	Н	Н	Н	Н		
RSVD RSVD	RSVD		4 Host	4 Upstream Sockets	4 Links	01110																
RSVD RSVD	RSVD	000000	4 17 17	Alle street Contract															I			



Table 29: Bifurcation for Quad Host, Quad Sockets and Quad Upstream Links (BIF[2:0]#=0b110)

δ	t Host, Four/Ex		at Operteam links		4 XZ, 4 XI																		
. 7 1	Min Suppor Card Card Short Modes Vidth Name	rted Bifurcation	Add-in-Card Encoding PRSMTBf3:01#	Host	Unstress Devices	Upstream	BIF[2:0]	Recentive List Description	1 3 4	3	6	7	-	9	-			9	-	Jane 13	1	1	
ç _u	Not Present	Card Not Present	0b1 111			t or 8 x2 Links	06111																
Г		1x8.1x4.1x2.1x1	0b1110	478 Host	Host 4/8 Upstream Sockets 4 or 8 x2 Links	s 4 or 8 x2 Links		1x2	Link 0.	Link 0.													
	1x8						06111	(Host 0 only)	Lane 0	Lane 1													
	1x4	1x4,1x2,1x1	0b1 110	4/8 Host	4/8 Upstream Sockets 4 or 8 x2 Links	a 4 or 8 x2 Links	06111	1x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1													
	1x2	1x2,1x1	061110	4/8 Host	Host 4/8 Upstream Sockets 4 or 8 x2 Links	a 4 or 8 x2 Links	06111	1x2 (Host 0 only)	Link 0, Lanc 0	Link 0, Lane 1													
	ž	1x1	061110	4/8 Host	4/8 Upstream Sockets 4 or 8 x2 Links	a 4 or 8 x2 Links	06111	fx1 (Host 0 only)	Link 0, Lane 0														
	1 v8 Option B	1x8.1x4,1x2,1x1 1x8.0ntion B 2x4 2x2 2x1	0b1 101	4/8 Host	Host 4/8 Upstream Sockets 4 or 8 x2 Links	s 4 or 8 x2 Links	06111	2 x 2 (Hoot 0 & Looku)	Link 0, Lanc 0	Link 0, Lone 1	Link 1,	Link 1, Land 1											
		2 x6, 2 x4, 2 x2, 2 x1	061101	4/8 Host	Host 4/8 Upstream Sockets 4 or 8 x2 Links	s 4 or 8 x2 Links	06111	2 x 2	Link 0,	\vdash	Link 1	Link 1				H	H						
1	a notido ex a	4 x4, 4 x6, 4 x1	081100	478 Hoes	Hoer A38 Hoercom Sockete A or 8 v2 Lisks	A or 8 v2 links		(nost 0 & Lonly)	Link O	Lanel	Link 1	٠	C dail	0.441	Link 3	Link 3	+	t	+	+		Ī	
	1x8 Option D	2 x4, 1x8 Option D 4 x2 (First 8 lanes), 4 x1			out of the second of the secon	200	0b111	3v *	Lane 0	Lane 1	Lane 0					Lane 1							
		1x16,1x8,1x4	0P1100	4/8 Host	Host 4/8 Upstream Sockets 4 or 8 x2 Links	a 4 or 8 x2 Links		4 x2	Link 0,	Link O,	Link 1,		⊢		⊢	Link 3,							
	1x16 Option D	2x8, 2x4, 1x16 Option D 4x4, 4x2 (First 8 lance), 4x1					0P##		Lane 0	Lane 1	Lane 0	Lane 1	Lane 0	Lane 1	Lane 0 Fi	Lane 1			_	_			
ĺ.	RSVD RSVD			4/8 Host	Host 4/8 Upstream Sockets 4 or 8 x2 Links	a 4 or 8 x2 Links	06111								l	H		H	H	ŀ			
	90.0	2 x4, 2 x2, 2 x1 1 x4 1 x2 1 x1	001010	4/8 Hos	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	s 4 or 8 x2 Links	0b111	2 x 2 (Hoot 0 & Looks)	Link 0,	Link 0,	Link 1,	Link 1, Land 1											
1	BSVD	BSVD for future x8 encoding		478 Host	478 Upstream Socket	a 4 or 8 x2 Links	05111												<u> </u>				
آھ	RSVD RSVD	RSVD for future x8 encoding 0b1000		4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	a 4 or 8 x2 Links																	
	1×16	1x16,1x8,1x4,1x2,1x1	060111	4/8 Hos	4/8 Upstream Socket	a 4 or 8 x2 Links	06111	1x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1													
	2 x8 Option A	2x8,2x4,2x2,2x1	000110	4/8 Host	Host 4/8 Upstream Sockets 4 or 8 x2 Links	a 4 or 8 x2 Links	06111	1x2 (Host 0 & 1 only)	Link 0, Lane 0	Link 0, Lane 1						22	Link 1, L Lane 0 L	Link 1, Lane 1					
	0 000	1x16,1x6,1x4,1x2,1x1	000101	478 Host	Host 4/8 Upstream Sockets 4 or 8 x2 Links	s 4 or 8 x2 Links	06111	2 x 2	Link 0,	Link 0,							Link 1, L	Link 1,					
		1x16,1x6,1x4 2x8,2x4,2x2,2x1	001000	4/8 Host	4/8 Upotream Sockets 4 or 8 x2 Links	4 or 8 x2 Links	06111	2x2 (Hogt 0 & 1 only)	Linko	Link 0,						100		Link 2, Lane 1					
	1x16 Option C	1x16 Option C 4x4, 4x2, 4x1															-						
	4 ×4	4x4, 4x2, 4x1	050 011	4/8 Host	Host 4/8 Upstream Sockets 4 or 8 x2 Links	a 4 or 8 x2 Links	0b111	4 x2 (Host 0 & 1 only)	Link 0, Lane 0	Link 0, Lane 1			Link 1, Lane 0	Link 1, Lane 1									
				4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	s 4 or 8 x2 Links																	
	RSVD RSVD	RSVD	000 001	4/8 Hos	478 Upstream Socket	d or 8 x2 Links	0b111		Ī										_	_			
0				AUS HAN	Allo la street Control	A 0 0 1																i	

3.9 Power Capacity and Power Delivery

There are four permissible power states: AC Power Off, Management (FRU Only Mode), Aux Power Mode (S5), and Main Power Mode (S0). The transition of these states is shown in . The max available power envelopes for each of these states are defined in Table 30.

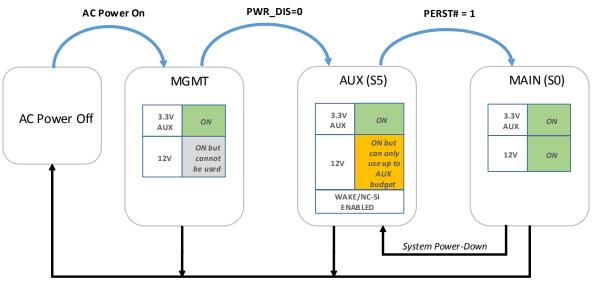


Figure 27: Baseboard Power Sequencing

Table 30: Power Envelopes

Power State	Max Power	Notes
AC Power Off	0W	AC power removed; board off
Management (FRU only mode)	1W	Used only for board identification
		purposes.
Aux Power Mode (S5)	35W	
Main Power Mode (S0)	79.2W	Add-in card may use up to the 79.2W
		limit per connector. The connector is
		derated 1.1A of current per pin (6 pins
		total) for a 30degC rise in the
		thermoplastic connector shell.

3.9.1 AC Power Off

In AC power off mode, all power delivery has been turned off or disconnected from the baseboard.



3.9.2 Management (FRU Only Mode)

In the Management (FRU Only Mode), only 3.3V Aux is available for powering up management only functions. FRU accesses are only allowed in this mode.

3.9.3 Aux Power Mode (S5)

In Aux Power Mode provides both 3.3V Aux as well as 12V Aux is available. 12V Aux may be used to deliver power to the add-in card, but only up to the Aux budget of 35W.

3.9.4 Main Power Mode (S0)

In Main Power Mode provides both 3.3V and 12V (Main) across the OCP connector. The add-in card operates in full capacity. Up to 79.2W may be delivered on 12V, and 3.63W on the 3.3V pins.

3.10 Add-in Card Input Capacitance

The baseboard provides 3.3Vaux and 12Vaux/main to both the Primary and Secondary connectors. The rail requirements are leveraged from the PCIe CEM 4.0 specification. For OCP NIC 3.0 cards, the requirements are as follows:

Power Rail	35W (Aux Only Mode)	79.2W (Main Power Mode)
3.3Vaux		
Voltage Tolerance	±9% (max)	±9% (max)
Supply Current	1.1A (max)	1.1A (max)
Capacitive Load	150µF (max)	150μF (max)
12V		
Voltage Tolerance	±8% (max)	±8% (max)
Supply Current	2.92A (max)	6.6A (max)
Capacitive Load	2000μF (max)	2000μF (max)

Table 31: Power Supply Rail Requirements

3.11 Hot Swap Considerations for 12V and 3.3V Rails

For baseboards that support system hot (powered on) add-in card insertions and extractions, the system implementer shall consider the use of hotswap controllers on both the 12Vmain/aux and 3.3Vaux pins to prevent damage to the baseboard or the add-in card.

Hotswap controllers help with in-rush current limiting while also providing overcurrent protection, undervoltage and overvoltage protection capabilities.

The hotswap controller may gate the 12Vmain/aux and 3.3Vmain/aux based on the PRSNTB[3:0]# value. Per Section 3.6.3, a card is present in the system when the encoded value is not 0b1111. The PRSNTB[3:0]# can be AND'ed together and connected to the hotswap controller to accomplish this result. Per the OCP NIC 3.0 mechanical definition (Section XXX), the present pins are short pins and engage only when the card is positively seated.

Baseboards that do not support hot insertion, or hot extractions may opt to not implement these features.

3.12 Power Sequence Timing Requirements

The following figure shows the power sequence of PRSNTB[3:0]#, 3.3Vaux, 12Vaux/12Vmain relative to PWRDIS, BIF[2:0]#, PERSTn*, the add-in card power ramp and NIC_PWR_GOOD.

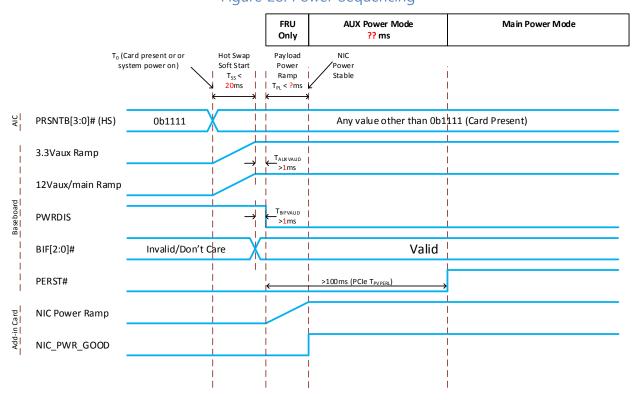


Figure 28: Power Sequencing



Table 32: Power Sequencing Parameters

Parameter	Value	Units	Description
T_{ss}	20	ms	Max time between system 3.3Vaux and 12Vaux/main ramp
			to power stable.
T _{AUXVALID}	>1	ms	Min time between 3.3Vaux valid to PWRDIS assertion.
T _{BIFVALID}	>1	ms	Min time between BIF[2:0]# valid to PWRDIS assertion. The
			BIF[2:0]# value sets the add-in card bifurcation mode (if
			applicable)
T _{PL}	</td <td>ms</td> <td>Max time between the NIC payload power ramp to</td>	ms	Max time between the NIC payload power ramp to
			NIC_PWR_GOOD assertion
T _{PVPERL}	>100	ms	Max time between PWRDIS deassertion and PERST#
			deassertion. This value is from the PCIe CEM Specification,
			Rev 4.0.

4 Management

4.1 SMBus Interface

The SMBus provides manageability of the add-in card.

4.2 NC-SI Sideband Interface

4.2.1 NC-SI addressing and Arb#

4.3 MAC Address Requirement

4.4 FRU EEPROM

4.4.1 Minimum EEPROM Size

4.4.2 EEPROM Map Definition

Editor's note [TN, 20171208]: the EEPROM map definition should include the card power class (e.g. be able to identify the max power required for 12V to the baseboard). This allows

the baseboard to intelligently enable/disable the card based on the available baseboard power budget.

- 4.4.3 **EEPROM Address**
- 4.5 FW Requirement (TBD)
- **4.6 Thermal Reporting Interface**



5 Data Network Requirement

5.1 Network Booting (collect view from OEMs and hyperscale)

Mezzanine NIC shall support network booting in uEFI system environment. Mezzanine NIC shall support both IPv4 and IPv6 network booting.

6 Routing Guidelines and Signal Integrity Considerations

6.1 NC-SI Over RBT

Min Length: 2" Max length: 4"

Impedance: 50 Ohm single ended

7 Thermal and Environmental

7.1 Environmental Requirements

The specific environment requirement is removed to allow the adoption of OCP Mezzanine NIC in systems with very different thermal requirement and boundary condition.

This Mezzanine card shall meet the same environmental requirements specified in the OCP systems that the Mezzanine card is in. The OCP system that uses OCP Mezzanine card shall define air flow direction, inlet air temperature, air flow (or speed) to the local area where Mezzanine card is at, and simulation boundary.

7.1.1 Thermal Simulation Boundary Example

Placeholder for Thermal Simulation Method. Using Facebook Intel® Motherboard V3.0 as example. Not covered by this update.

7.2 Shock & Vibration

This Mezzanine card shall meet the same shock & vibration requirements specified in updated Facebook OCP Intel® Motherboard V2.0 and V3.0 Design Specification.

7.3 Regulation

This Mezzanine card shall meet CE, CB, FCC Class A, WEEE, ROHS requirements.



8 Revision History

Description	Revision	Date
Initial draft	0.1	12/xx/2017