

OCP NIC 3.0 Design Specification

Version 0.01

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Table of Contents

1	Overv	/iew	7				
	1.1	License	7				
	1.2 Background						
	1.3	Acknowledgements	9				
	1.4	Overview	9				
	1.4	.4.1 Mechanical Form factor overview	9				
	1.4	.4.2 Electrical overview	12				
	1.5	References	12				
2	Card I	Form Factor	14				
	2.1	Overview	14				
	2.2	Form Factor Options	14				
	2.3	I/O bracket	16				
	2.4	Line Side I/O Implementations	16				
	2.5	LED Implementation	17				
	2.6	Mechanical Keepout Zones	18				
	2.	.6.1 Baseboard Keep Out Zone	18				
	2.	.6.2 Add-in Card Keep Out Zone	18				
	2.7	Labeling Requirements	19				
	2.8	Insulation Requirements	19				
	2.9	NIC Implementation Examples	19				
	<mark>2.10</mark>	Non-NIC Use Cases	19				
	2 <u>.</u>	.10.1 PCIe Retimer card	19				
	<mark>2.</mark>	.10.2 Accelerator card	19				
	<mark>2.</mark>	<mark>.10.3</mark> Storage HBA / RAID card	19				
3	Card I	Edge and Baseboard Connector Interface	19				
	3.1	Gold Finger Requirement	19				
	3.2	Baseboard Connector Requirement	21				
	3.3	Pin definition	22				
	3.4	Signal Descriptions – Common	28				

	3.4.1	PCIe Interface Pins	28
	3.4.2	PCIe Present and Bifurcation Control Pins	31
	3.4.3	SMBus Interface Pins	33
	3.4.4	Power Supply Pins	34
	3.4.5	Miscellaneous Pins	35
3.5	Sig	nal Descriptions – OCP Bay (Primary Connector)	35
	3.5.1	PCIe Interface Pins – OCP Bay (Primary Connector)	35
	3.5.2	NC-SI Over RBT Interface Pins – OCP Bay (Primary Connector)	37
	3.5.3	Scan Chain Pins – OCP Bay (Primary Connector)	39
	3.5.4	Primary Connector Miscellaneous Pins – OCP Bay (Primary Connector)	46
3.6	PC.	e Bifurcation Mechanism	47
	3.6.1	PCIe Add-in Card to Baseboard Bifurcation Configuration (PRSNTA#,	
	PRSNTE	3[3:0]#)	48
	3.6.2	PCIe Baseboard to Add-in Card Bifurcation Configuration (BIF[2:0]#)	48
	3.6.3	PCIe Bifurcation Decoder	49
	3.6.4	Bifurcation Detection Flow	51
	3.6.5	PCIe Bifurcation Examples	52
3.7	PC:	e Clocking Topology	56
3.8	PC:	e Bifurcation and REFCLK Mapping	58
3.9	Pov	ver Capacity and Power Delivery	67
	3.9.1	AC Power Off	67
	3.9.2	Management (FRU Only Mode)	67
	3.9.3	Aux Power Mode (S5)	68
	3.9.4	Main Power Mode (S0)	68
3.10	0 Pov	ver Sequence Timing Requirements	68
Ма	nageme	nt	69
4.1	SM	Bus Interface	69
4.2	NC	-SI Sideband Interface	69
	4.2.1	NC-SI addressing and Arb#	69
4.3	MA	C Address Requirement	69
4.4	FRU	J EEPROM	69
	4.4.1	Addressing(TBD)	69
4.5	FW	Requirement (TBD)	69

4



	4.6	Thermal Reporting Interface	69
5	Data	Network Requirement	70
	5.1	Network Booting (collect view from OEMs and hyperscale)	70
6	Routi	ng Guidelines and Signal Integrity Considerations	71
	6.1	NC-SI Over RBT	71
7	Therr	nal and Environmental	71
	7.1	Environmental Requirements	71
	7	.1.1 Thermal Simulation Boundary Example	71
	7.2	Shock & Vibration	71
	7.3	Regulation	71
8	Revis	ion History	72

List of Figures

Figure 1: Representative Small OCP 3.0 NIC Card with Quad SFP Ports	8
Figure 2: Representative Large OCP 3.0 NIC Card with Dual QSFP Ports and on-board DRAM	9
Figure 3: Small and Large Card Form-Factors (not to scale)	10
Figure 4: Example Small Card Form Factor	14
Figure 5: Example Large Card Form Factor	15
Figure 6: Primary Connector (4C + OCP Bay) with 4C and 2C Add in Cards	16
Figure 7: Small Size Primary Connector Gold Finger Mating Card Dimensions – x16 – Top Side	20
Figure 8: Small Size Primary Connector Gold Finger Mating Card Dimensions – x16 – Bottom Side	20
Figure 9: Small Size Secondary Connector Gold Finger Mating Card Dimensions – x16 – Top Side	21
Figure 10: Small Size Secondary Connector Gold Finger Mating Card Dimensions – x16 – Bottom Side	21
Figure 11: Large Size Card Gold Finger Mating Card Dimensions – x32 – Top Side	21
Figure 12: Large Size Card Gold Finger Mating Card Dimensions – x32 – Bottom SideSide	21
Figure 13: 168-pin Base Board Primary Connector – Right Angle	22
Figure 14: 140-pin Base Board Secondary Connector – Right Angle	22
Figure 15: 168-pin Base Board Primary Connector – Straddle Mount	22
Figure 16: 140-pin Base Board Secondary Connector – Straddle Mount	22
Figure 17: Primary and Secondary Conenctor Locations for Large Card Support	22
Figure 18: PCIe Present and Bifurcation Control Pins	32
Figure 19: NC-SI Over RBT Connection Example	38
Figure 20: Scan Bus Connection Example	45
Figure 21: PCIe Bifurcation Pin Connections Support	47
Figure 22: Single Host (1 x16) and 1 x16 Add-in Card (Single Controller)	52
Figure 23: Single Host (2 x8) and 2 x8 Add-in Card (Dual Controllers)	53
Figure 24: Four Hosts (4 x4) and 4 x4 Add-in Card (Single Controller)	54
Figure 25: Four Hosts (4 x4) and 4 x4 Add-in Card (Four Controllers)	55
Figure 26: Single Host with no Bifurcation (1 x16) and 2 x8 Add-in Card (Two Controllers)	56
Figure 27: PCIe Interface Connections for 1 x16 and 2 x8 Add-in Cards	57
Figure 28: PCIe Interface Connections for a 4 x4 Add-in Card	58
Figure 29: Baseboard Power Sequencing	67
Figure 30: Baseboard Power Sequencing	68



List of Tables

Table 1: OCP 3.0 Form Factor Dimensions	10
Table 2: Baseboard to OCP NIC Form factor Compatibility Chart	11
Table 3: OCP 3.0 Card Definitions	16
Table 4: OCP 3.0 Line Side I/O Implementations	16
Table 5: Default LED Configuration	17
Table 6: Primary Connector Card Pin Definition (x16) (4C + OCP Bay)	23
Table 7: Secondary Connector Card Pin Definition (x16) (4C)	26
Table 8: Card Pin Descriptions – PCIe	28
Table 9: Card Pin Descriptions – PCIe Present and Bifurcation Control Pins	31
Table 10: Card Pin Descriptions – SMBus	33
Table 11: Card Pin Descriptions – Power	34
Table 12: Card Pin Descriptions – Miscellaneous	35
Table 13: Card Pin Descriptions – PCIe	35
Table 14: Card Pin Descriptions – NC-SI Over RBT	37
Table 15: Card Pin Descriptions – Scan Bus	39
Table 16: Card Pin Descriptions – Scan Bus DATA_OUT Bit Definition	41
Table 17: Card Pin Descriptions – Scan Bus DATA_IN Bit Definition	42
Table 18: Card Pin Descriptions – Miscellaneous	46
Table 19: PCIe Bifurcation Decoder for x16 and x8 Card Widths	50
Table 20: PCIe Clock Associations	57
Table 21: Bifurcation for Single Host, Single Upstream Socket and Single Upstream Link (BIF[2:0]#=0b000)	59
Table 22: Bifurcation for Single Host, Single Upstream Socket and Single/Dual Upstream Links (BIF[2:0]#=0b0	000)
	60
Table 23: Bifurcation for Single Host, Single Upstream Socket and Single/Dual/Quad Upstream Links	
(BIF[2:0]#=0b000)	61
Table 24: Bifurcation for Single Host, Dual Upstream Sockets and Dual Upstream Links (BIF[2:0]#=0b001)	62
Table 25: Bifurcation for Single Host, Four Upstream Sockets and Dual Upstream Links (BIF[2:0]#=0b010)	63
Table 26: Bifurcation for Dual Host, Dual Upstream Sockets and Dual Upstream Links (BIF[2:0]#=0b101)	64
Table 27: Bifurcation for Quad Host, Quad Upstream Sockets and Quad Upstream Links (BIF[2:0]#=0b110)	65
Table 28: Bifurcation for Quad Host, Quad Upstream Sockets and Quad Upstream Links (BIF[2:0]#=0b110)	66
Table 29: Power Envelopes	67
Table 30: Power Sequencing Parameters	68

1 Overview

1.1 License

As of April 7, 2011, the following persons or entities have made this Specification available under the Open Web Foundation Final Specification Agreement (OWFa 1.0), which is available at http://www.openwebfoundation.org/legal/the-owf-1-0-agreements/owfa-1-0: Facebook, Inc.

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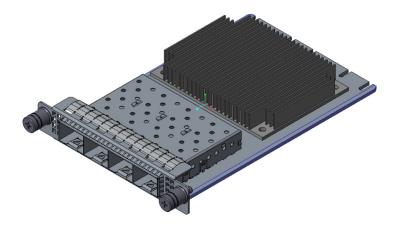
1.2 Background

The OCP NIC 3.0 specification is a follow-on to the OCP 2.0 form-factor for PCIe add-in cards. The OCP NIC 3.0 specification supports two basic card sizes: Small Card, and Large Card. The Small Card allows for up to 16 PCIe lanes on the card edge while a Large Card supports up to 32 PCIe lanes on the card edge. Compared to the OCP NIC 2.0 release, the updated specification provides a broader solution space for NIC and system vendors to support the following use cases scenarios:

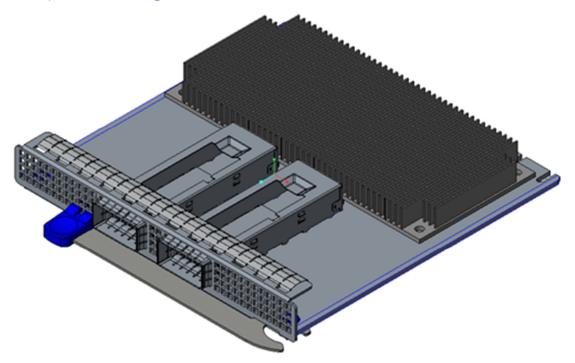
- NICs with a higher TDP
- Support up to 79W of power delivery to a single connector (Small) card; and 158W to a dual connector (Large) card
- PCIe Gen4 and Gen5 on the system and card
- Support for upto 32 lanes of PCIe per card
- Support for single host and multi-host environments
- Support a greater board area for more complex add-in card designs
- Support for Smart NIC implementations with on-board DRAM
- Simplification of FRU installation and removal while reducing overall down time

A representative Small Card OCP 3.0 NIC mezzanine card is shown in Figure 1 and a representative Large Card is shown in Figure 2

Figure 1: Representative Small OCP 3.0 NIC Card with Quad SFP Ports







OCP 3.0 compliant cards are not backwards compatible to the 2.0 cards in order to achieve the features outlined in this specification.

This specification is created under OCP Server workgroup – OCP NIC subgroup. An electronic copy of this specification can be found on the Open Compute Project website:

http://www.opencompute.org/wiki/Server/Mezz#Specifications_and_Designs

1.3 Acknowledgements

Placeholder

1.4 Overview

1.4.1 Mechanical Form factor overview

The OCP NIC 3.0 specification defines a third generation mechanical form factor that allows for interoperability between specification compliant systems and cards.



OCP NIC 3.0 cards have two form factors – Small and Large. These cards are shown in Figure 3 below. The components shown in the figures are for illustrative purposes. The Small form factor card has one connector (Primary connector) on baseboard. The Large form factor card has two connectors (Primary Connector and Secondary Connector) on the baseboard. Both the Primary and Secondary connectors are defined in and compliant to SFF-TA-1002. [Editor's note: plan to submit change back to SFF-TA-1002]. On the NIC side, the card edge is implemented with gold fingers. The gold finger design follows SFF-TA-1002 as well.

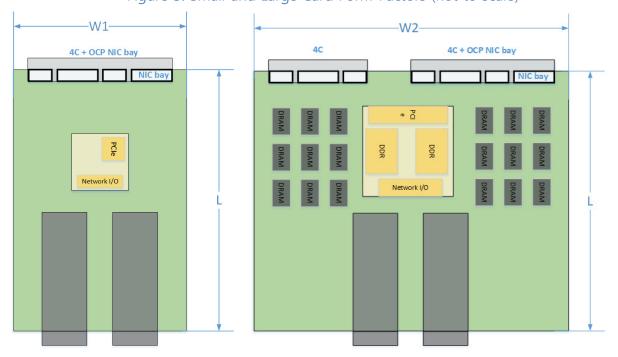


Figure 3: Small and Large Card Form-Factors (not to scale)

The two form factor dimensions are shown in Table 1.

lable	T:	OCP	3.0	Form	Factor	Dimensions	

Form	Width	Depth	Primary	Secondary	Typical Use Case
Factor			Connector	Connector	
Small	W1=76	115mm	4C+ OCP	N/A	Low profile and general NIC
			sideband		in similar profile as OCP

					NIC 2.0; up to x16 PCIe
					lanes
Large	W2=139	115mm	4C+ OCP	4C	Largest PCB width to
	[to be		sideband		support feature rich NICs,
	confirmed]		168 pins		and up to x32 PCIe lanes

The OCP 3.0 NIC design allows downward compatibility between the two sizes. Table 2 shows the compatibility between the baseboard and NIC combinations. A Large size baseboard slot may accept a small or large sized NIC. A small size baseboard slot may only accept a small sized NIC.

Table 2: Baseboard to OCP NIC Form factor Compatibility Chart

Baseboard	NIC Size / Supported PCIe Width			
Slot Size	Small	Large		
Small	Up to x16	Not Supported		
Large	Up to x16	Up to x32		

There are two baseboard connector options available for system designers: straddle mount and right angle (RA). The straddle mount connector option allows the OCP NIC and baseboard to exist in a co-planer position. To achieve this, a cutout exists on the baseboard and is defined in this specification. Alternatively, the right angle option allows the OCP NIC to be installed on top of the baseboard. A baseboard cutout is not required for the right angle connector. The right angle option allows the base board to use this area for additional baseboard routing. The straddle mount and right angle connectors are shown in Section 3.2.

For both the baseboard and OCP card, this specification defines the component and routing keep out areas. Refer to Section 2.6 for details.

Both the straddle mount and right angle implementations shall use the same OCP NIC and shall be supported in the baseboard chassis regardless of the baseboard connector selection (right angle or straddle mount) so long as the baseboard slot side and NIC size are a supported combination as shown in Table 2.



This specification defines form factor at NIC module level, including the front panel, latches and card guide features [TBD; pending on the Mechanical work across stakeholders].

More details about the card form-factor is shown in Section 2.

1.4.2 Electrical overview

This specification defines electrical interface between baseboard/system and card/NIC module.

The electrical interface is implemented with a right angle or straddle mount connector on baseboard and gold finger on the add-in card. As previously noted in the mechanical overview, each card may implement a Primary Connector or Primary + Secondary Connector. Cards using only the Primary connector are suitable for both the Small and Large form-factors and may support up to x16 lanes of PCIe. The Secondary connector in conjunction with the Primary allows Large form-factor implementations and may support up to 32 lanes of PCIe.

1.4.2.1 Primary Connector

1.4.2.2 Secondary connector

1.5 References

DMTF Standard. *DSP0222, Network Controller Sideband Interface (NC-SI) Specification.*Distributed Management Task Force, Inc, Rev 1.0.1, January 24th, 2013.

Open Compute Project. OCP NIC Subgroup. Online.

http://www.opencompute.org/wiki/Server/Mezz

PCIe Base Specification. PCI Express Base Specification, Revision 4.0 (draft).

PCIE CEM Specification. PCI Express Card Electromechanical Specification, Revision 4.0 (draft).

SMBus specification

SNIA. *SFF-TA-1002, Specification for Protocol Agnostic Multi-Lane High Speed Connector.*SNIA SFF TWG Technology Affiliate, Rev 0.0.9.1, September 9th, 2017.



2 Card Form Factor

2.1 Overview

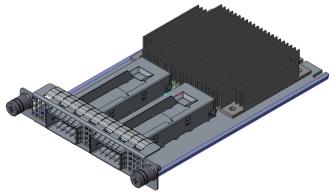
2.2 Form Factor Options

OCP3.0 provides two fundamental form factor options: a small card (76mm \times 115mm) and a large card (139mm \times 115mm).

These form factors support a Primary Connector and optionally, a Secondary Connector. The Primary Connector is defined to be a SFF-TA-1002 compliant 4C connector plus a 28-pin bay for OCP 3.0 specific pins. The Secondary Connector is the 4C connector as defined in SFF-TA-1002. The 4C specification supports up to 32 differential pairs for a x16 PCIe connection per connector. For host platforms, the 28-pin OCP bay is required for the Primary connector. This is also mandatory for add-in cards.

The small card uses the 4C connector for up to a x16 PCIe interface. The small cards implement the 28 pin OCP bay for management functions and support for up to a four PCIe hosts. The small size card provides sufficient faceplate area to accommodate up to 2x QSFP modules, 4x SFP modules, or 4x RJ-45 for BASE-T operation. The small card form factor supports up to 79W of delivered power to the card edge.





The large card uses provides the same functionality as the small card, but with support up to a x32 PCIe interface. The large card utilizes both the Primary and Secondary connectors. The large size card supports higher power envelopes and provides additional board area for more complex designs. The small card form factor supports up to 158W of delivered power to the card edge at 79W per connector.

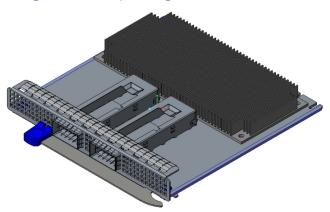


Figure 5: Example Large Card Form Factor

For both form-factors, an add-in card may optionally implement a subset of pins to support a x8 PCIe connection. This is implemented using a 2C connector per SFF-TA-1002. The Primary Connector may support a 2C sized add in card along with the 28 pin OCP bay. The following diagram from the SFF-TA-1002 specification illustrates the supported host Primary and Secondary Connectors and add in card configurations.



Figure 6: Primary Connector (4C + OCP Bay) with 4C and 2C Add in Cards

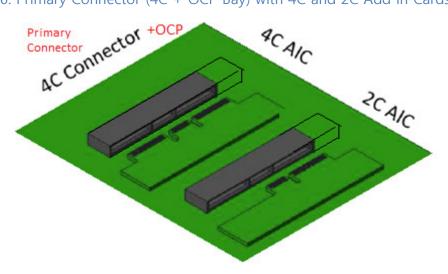


Table 3 summarizes the supported card form factors. Small form factors cards support the Primary Connector and up to 16 PCIe lanes. Large form factor cards support both the Primary and Secondary Connectors and up to 32 PCIe lanes.

Table 3: OCP 3.0 Card Definitions

Add in Card Size and	Secondary Connector		Primary Connector		
max PCIe Lane Count	4C Connector, x16 PCIe		4C Connector, x16 PCIe		OCP Bay
Small (x8)				2C	OCP Bay
Small (x16)		4	C	OCP Bay	
Large 1 (x24)		2C	4	С	OCP Bay
Large 2 (x32)	4C		4	C	OCP Bay

2.3 I/O bracket

TBD < need input from OCP mechanical groups>

2.4 Line Side I/O Implementations

At the time of this writing, the Small and Large form-factor cards may support the following standard line side I/O implementations:

Table 4: OCP 3.0 Line Side I/O Implementations

Form Factor	Max Topology Connector Count
Small	2x QSFP28
Small	4x SFP28
Small	4x RJ-45
Large	TBD
Large	TBD
Large	TBD

Additional combinations are permissible as I/O technologies and thermal capabilities evolve.

2.5 LED Implementation

A small form-factor OCP 3.0 NIC with a fully populated I/O bracket (2x QSFP28, 4xSFP28, or 4xRJ-45), there is insufficient space for on-board LED indicators. In this case, the line side link and activity LED indicators are implemented on the baseboard system via the Scan Chain. The Scan Chain bit stream is defined in Section 3.5.3.

For small form-factor low I/O count cards (such as 1x QSFP28, 2xSFP28, or 2xRJ-45), or a large form-factor OCP 3.0 NIC, where additional I/O bracket area is available, the card may optionally implement on-board link/activity indications in addition to the Scan Chain LED.

For both cases, the OCP3.0 specification recommends the following LED definitions:

Table 5: Default LED Configuration

LED Pin	LED Color	Description
Link	Green	Active low. Multifunction LED.
		When lit and solid, this LED is used to indicate the link is up at
		the MAC level. Local and Remote Faults are clear and the link is
		ready for data transmission. When the LED is off, the physical link
		is down or disabled.
		This LED indicator may also be used for port identification
		through vendor specific link diagnostic software.



		The link LED shall be located on the left hand side of each port.
Activity	Green	Active low.
		The Activity LED shall only be illuminated when the Link LED is illuminated.
		When lit and solid, this LED is used to indicate the port is "idle" and no data is being transmitted or received.
		When lit and blinking, this LED is used to indicate the port is "active" and data is either being transmitted or received.
		When the LED is off, no link is detected.
		The activity LED shall be located on the right hand side of each port.

At the time of this writing, the Scan Chain definition allows for up to one link and one activity LED per port. A total of up to 8 ports are supported in the Scan Chain. The bit stream defines the LEDs to be active low (ON). The Scan Chain LED implementation allows the NIC LED indicators to be remotely located on the OCP3.0 compliant chassis (e.g. front LED indicators with rear I/O cards).

2.6 Mechanical Keepout Zones

2.6.1 Baseboard Keep Out Zone

TBD – Need keepout drawings and envelopes for small / large size baseboard including primary/secondary/rail keepouts/cutout for straddle mount/keepout for right angle.

2.6.2 Add-in Card Keep Out Zone

TBD – need keepout drawings and envelopes for small / large size NIC including primary/secondary/rail keepouts.

2.7 Labeling Requirements

TBD

2.8 Insulation Requirements

All cards must implement a secondary side insulator to prevent the bottom side card components from shorting out to the chassis. The recommended insulator thickness is 0.25mm and must reside within the following mechanical envelope for the Small and Large size cards:

TBD < need 2D drawings>

2.9 NIC Implementation Examples

TBD

2.10 Non-NIC Use Cases

"PCIe interface with extra management sideband"

2.10.1 PCle Retimer card

2.10.2 Accelerator card

2.10.3 Storage HBA / RAID card

3 Card Edge and Baseboard Connector Interface

3.1 Gold Finger Requirement

Editor's note: Connector vendors to provide input and all detailed views from the mechanical drawing. First stab at it is below. Diagrams are copied from SFF-TA-1002. The OCP NIC 3.0 add-in cards are compliant to the SFF-TA-1002 specification with respect to the gold fingers and connectors.

Small Size cards may fit in the Primary Connector or the Secondary Connector. Primary Connector compliant cards are 76mm x 115mm and may implement the full 168-pins. Secondary Connector compliant cards are XXXmm x 115mm and may implement the 140-pin gold finger. Both the Primary and Secondary Connector cards may optionally implement



a subset of gold finger pins if there is a reduced PCIe width requirement (such as 1 x8 and below). In this case, the card edge gold finger may implement a 2C design. The overall board thickness is 1.60mm. The gold finger dimensions for the Primary Connector and Secondary Connector compliant cards are shown below.

Large Size Cards support up to a x32 PCIe implementation and uses both the Primary and Secondary connectors.

For additional details, refer to the card and connector mechanical drawings located in XXX.

Note: The "B" pins on the connector are associated with the top side of the add-in card. The "A" pins on the connector are associated with the bottom side of the add-in card.

Figure 7: Small Size Primary Connector Gold Finger Mating Card Dimensions – x16 – Top Side

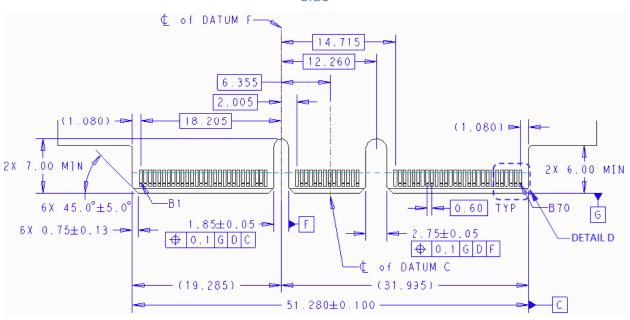


Figure 8: Small Size Primary Connector Gold Finger Mating Card Dimensions – x16 – Bottom Side

Figure 9: Small Size Secondary Connector Gold Finger Mating Card Dimensions – x16 – Top Side

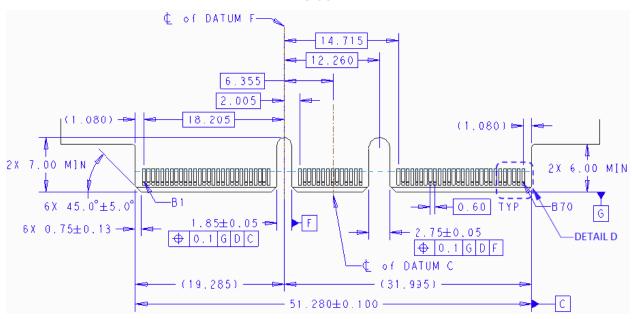


Figure 10: Small Size Secondary Connector Gold Finger Mating Card Dimensions – x16 – Bottom Side

TBD

Figure 11: Large Size Card Gold Finger Mating Card Dimensions – x32 – Top Side

TBD

Figure 12: Large Size Card Gold Finger Mating Card Dimensions – x32 – Bottom Side

TBD

3.2 Baseboard Connector Requirement

Editor's note: Connector vendors to provide input.

The OCP3.0 connector is compliant to the "4C connector" as defined in the SFF-TA-1002 specification for a right angle or straddle mount form-factor. The 4C connector is 140-pins in width and includes support for up to 32 differential pairs to support a x16 PCIe connection. The connector also provides 6 pins of 12V for payload power. This implementation is common between both the Primary and Secondary Connector. In



addition, the Primary Connector has a 28-pin OCP Bay to the right of pin 1. These pins are used for management and support for up to a 4 x4 multi-host configuration on the Primary Connector. The Primary and Secondary Connector drawings are shown in Figure 13 and Figure 14, below.

Figure 13: 168-pin Base Board Primary Connector – Right Angle

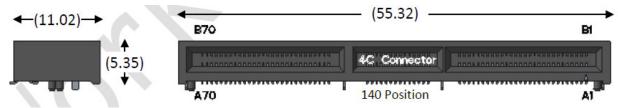


Figure 14: 140-pin Base Board Secondary Connector – Right Angle

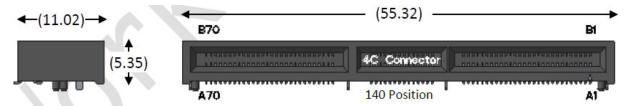


Figure 15: 168-pin Base Board Primary Connector – Straddle Mount

<mark>TBD</mark>

Figure 16: 140-pin Base Board Secondary Connector – Straddle Mount

TBD

In order to the support the large form factor, systems must locate the Primary and Secondary Connectors per the mechanical drawing shown in Figure 17.

Figure 17: Primary and Secondary Conenctor Locations for Large Card Support

TBE

3.3 Pin definition

Editor's note: The pin map aligns with OCP 3.0 Pinout Proposal 20171121a_TN.xlsx. The pin definitions of an OCP NIC 3.0 card with up to a x32 PCIe interface are shown in Table 6 and Table 7. All signal directions are shown from the perspective of the baseboard.

A baseboard system may provide a combination of Primary Connectors only, or Primary and Secondary Connectors to support multiple add-in cards. Both connectors share common functionality with power, SMBus, x16 PCIe Gen4 and bifurcation control. The Primary Connector has an additional OCP Bay (pins OCP_A[1:14], OCP_B[1:14]) with additional REFCLKs for supporting up to four PCIe hosts, NC-SI connectivity and a scan chain for information exchange between the host and card. The NIC is required to implement the Scan Chain, while the baseboard may choose to optionally implement it. Depending on the baseboard form-factor, multiple OCP NIC 3.0 compliant cards may be designed into the system.

The pins common to the Primary and Secondary Connector are shown in Section 3.4. The OCP Bay for the Primary Connector only are shown in Section 3.5.

Cards or systems that do not require the use of a PCIe x16 connection may optionally implement a subset electrical connections as applicable to the design (for example, a x8 (or smaller) card using the first 8 PCIe lanes that is compliant with the Primary Connector pinout). Refer to Sections 3.1 and 3.2 for mechanical details. For these cases, the Primary Connector matches the "2C" dimensions as defined in SFF-TA-1002.

In all cases, the physical baseboard connectors shall support x16 PCIe widths and must be implemented with the Primary (4C + OCP Bay) and Secondary (4C) connectors.

	Side B	Side A			
OCP_B1	NIC_PWR_GOOD	WAKE_N	OCP_A1	in Pri	Pri in
OCP_B2	PWRBRK#	PERST2#	OCP_A2	Primary in card	Primary in card
OCP_B3	LD#	PERST3#	OCP_A3	< `	<
OCP_B4	DATA_IN	RBT_ARB_IN	OCP_A4		_
OCP_B5	DATA_OUT	RBT_ARB_OUT	OCP_A5	nector OCP B	necto OCP
OCP_B6	CLK	GND	OCP_A6		
OCP_B7	SLOT_ID0	RBT_TX_EN	OCP_A7	(x16, ay)	,ω
OCP_B8	RBT_RXD1	RBT_TXD1	OCP_A8	168	112-pin
OCP_B9	RBT_RXD0	RBT_TXD0	OCP_A9	pi pi	
OCP_B10	GND	GND	OCP_A10	ı add-	add-
OCP_B11	REFCLKn2	REFCLKn3	OCP_A11	d-	•

Table 6: Primary Connector Card Pin Definition (x16) (4C + OCP Bay)



OCP_B12	REFCLKp2	REFCLKp3	OCP_A12	
OCP_B13	GND	GND	OCP_A13	
OCP_B14	RBT_CRS_DV	RBT_CLK_IN	OCP_A14	
	Mechan	ical Key		
B1	+12V/+12V_AUX	GND	A1	
B2	+12V/+12V_AUX	GND	A2	
В3	+12V/+12V_AUX	GND	A3	
B4	+12V/+12V_AUX	GND	A4	
B5	+12V/+12V_AUX	GND	A5	
В6	+12V/+12V_AUX	GND	A6	
В7	BIFO#	SMCLK	A7	
B8	BIF1#	SMDAT	A8	
В9	BIF2#	SMRST#	A9	
B10	PERSTO#	PRSNTA#	A10	
B11	+3.3V/+3.3V_AUX	PERST1#	A11	
B12	PWRDIS	PRSNTB2#	A12	
B13	GND	GND	A13	
B14	REFCLKn0	REFCLKn1	A14	
B15	REFCLKp0	REFCLKp1	A15	
B16	GND	GND	A16	
B17	PETn0	PERn0	A17	
B18	PETp0	PERp0	A18	
B19	GND	GND	A19	
B20	PETn1	PERn1	A20	
B21	PETp1	PERp1	A21	
B22	GND	GND	A22	
B23	PETn2	PERn2	A23	
B24	PETp2	PERp2	A24	
B25	GND	GND	A25	
B26	PETn3	PERn3	A26	
B27	РЕТр3	PERp3	A27	
B28	GND	GND	A28	
	Mechan	ical Key		
B29	GND	GND	A29	
B30	PETn4	PERn4	A30	
B31	PETp4	PERp4	A31	
B32	GND	GND	A32	
B33	PETn5	PERn5	A33	
B34	РЕТр5	PERp5	A34	

Rev0.01

B35	GND	GND	A35	
B36	PETn6	PERn6	A36	
B37	PETp6	PERp6	A37	
B38	GND	GND	A38	
B39	PETn7	PERn7	A39	
B40	РЕТр7	PERp7	A40	
B41	GND	GND	A41	
B42	PRSNTB0#	PRSNTB1#	A42	
	Mechan	nical Key		
B43	GND	GND	A43	
B44	PETn8	PERn8	A44	
B45	PETp8	PERp8	A45	
B46	GND	GND	A46	
B47	PETn9	PERn9	A47	
B48	PETp9	PERp9	A48	
B49	GND	GND	A49	
B50	PETn10	PERn10	A50	
B51	PETp10	PERp10	A51	
B52	GND	GND	A52	
B53	PETn11	PERn11	A53	
B54	PETp11	PERp11	A54	
B55	GND	GND	A55	
B56	PETn12	PERn12	A56	
B57	PETp12	PERp12	A57	
B58	GND	GND	A58	
B59	PETn13	PERn13	A59	
B60	PETp13	PERp13	A60	
B61	GND	GND	A61	
B62	PETn14	PERn14	A62	
B63	PETp14	PERp14	A63	
B64	GND	GND	A64	
B65	PETn15	PERn15	A65	
B66	PETp15	PERp15	A66	
B67	GND	GND	A67	
B68	RFU, N/C	RFU, N/C	A68	
B69	RFU, N/C	RFU, N/C	A69	
B70	PRSNTB3#	RFU, N/C	A70	



Table 7: Secondary Connector Card Pin Definition (x16) (4C)

	Side B	Side A			
B1	+12V/+12V_AUX	GND	A1	S	S
B2	+12V/+12V_AUX	GND	A2	ecor	ecoi
В3	+12V/+12V_AUX	GND	A3	ndar	ndai
B4	+12V/+12V_AUX	GND	A4	Secondary Connector (x16, 140-pin add-in card)	Secondary Connector (x8, 84-pin add-in card)
B5	+12V/+12V_AUX	GND	A5	onne	onne
В6	+12V/+12V_AUX	GND	A6	ecto	ecto
В7	BIFO#	SMCLK	A7	r X	r (x
B8	BIF1#	SMDAT	A8	16, :	δ α
В9	BIF2#	SMRST#	A9	140-	1-pi
B10	PERSTO#	PRSNTA#	A10	Ď.	n ac
B11	+3.3V/+3.3V_AUX	PERST1#	A11	add	ld-ir
B12	PWRDIS	PRSNTB2#	A12	ੂ.	ı caı
B13	GND	GND	A13	carc	<u>a</u>
B14	REFCLKn0	REFCLKn1	A14		
B15	REFCLKp0	REFCLKp1	A15		
B16	GND	GND	A16		
B17	PETn0	PERn0	A17		
B18	РЕТр0	PERp0	A18		
B19	GND	GND	A19		
B20	PETn1	PERn1	A20		
B21	PETp1	PERp1	A21		
B22	GND	GND	A22		
B23	PETn2	PERn2	A23		
B24	PETp2	PERp2	A24		
B25	GND	GND	A25		
B26	PETn3	PERn3	A26		
B27	PETp3	PERp3	A27		
B28	GND	GND	A28		
	Mechar	nical Key			
B29	GND	GND	A29		
B30	PETn4	PERn4	A30		
B31	PETp4	PERp4	A31		
B32	GND	GND	A32		
B33	PETn5	PERn5	A33		
B34	PETp5	PERp5	A34		
B35	GND	GND	A35		
B36	PETn6	PERn6	A36		

Rev0.01

B37	PETp6	PERp6	A37	
B38	GND	GND	A38	
B39	PETn7	PERn7	A39	
B40	РЕТр7	PERp7	A40	
B41	GND	GND	A41	
B42	PRSNTB0#	PRSNTB1#	A42	
	Mechan	ical Key		
B43	GND	GND	A43	
B44	PETn8	PERn8	A44	
B45	PETp8	PERp8	A45	
B46	GND	GND	A46	
B47	PETn9	PERn9	A47	
B48	PETp9	PERp9	A48	
B49	GND	GND	A49	
B50	PETn10	PERn10	A50	
B51	PETp10	PERp10	A51	
B52	GND	GND	A52	
B53	PETn11	PERn11	A53	
B54	PETp11	PERp11	A54	
B55	GND	GND	A55	
B56	PETn12	PERn12	A56	
B57	PETp12	PERp12	A57	
B58	GND	GND	A58	
B59	PETn13	PERn13	A59	
B60	PETp13	PERp13	A60	
B61	GND	GND	A61	
B62	PETn14	PERn14	A62	
B63	PETp14	PERp14	A63	
B64	GND	GND	A64	
B65	PETn15	PERn15	A65	
B66	PETp15	PERp15	A66	
B67	GND	GND	A67	
B68	RFU, N/C	RFU, N/C	A68	
B69	RFU, N/C	RFU, N/C	A69	
B70	PRSNTB3#	RFU, N/C	A70	
				•



3.4 Signal Descriptions – Common

The pins shown in this section are common to both the Primary and Secondary Connectors. All pin directions are from the perspective of the baseboard.

Note: Pins that are only used on Primary Connector 28-pin OCP bay are defined in Section 3.5.

3.4.1 PCle Interface Pins

This section provides the pin assignments for the PCIe interface signals. The AC/DC specifications are defined in Section XXX. Example connection diagrams for are shown in Figure 28.

Table 8: Card Pin Descriptions – PCIe

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
REFCLKn0	B14	Output	PCIe compliant differential reference clock #0,
REFCLKp0	B15		and #1. 100MHz HCSL reference clocks are
REFCLKn1	A14	Output	used for the add-in card PCIe core logic.
REFCLKp1	A15		
			Note: For cards that only support 1 x16,
			REFCLK0 is used. For cards that support 2 x8,
			REFCLK0 is used for the first eight PCIe lanes,
			and REFCLK1 is used for the second eight PCIe
			lanes.
			Refer to Section 2.1 in the PCIe CEM
			Specification, Rev 4.0 for electrical details.
PETn0	B17	Output	Transmitter differential pair [0:15]. These pins
PETp0	B18		are connected from the baseboard transmitter
PETn1	B20	Output	differential pairs to the receiver differential
PETp1	B21		pairs on the add-in card.
PETn2	B23	Output	
PETp2	B24		

PETn3	B26	Output	The PCIe Transmit pins are AC coupled on the
РЕТр3	B27		baseboard with capacitors and are placed next
PETn4	B30	Output	to the baseboard transmitters. The AC coupling
PETp4	B31		capacitor must be between 176nF (min) and
PETn5	B33	Output	265nF (max).
PETp5	B34		
PETn6	B36	Output	Refer to Section 6.1 in the PCIe CEM
РЕТр6	B37		Specification, Rev 4.0 for details.
PETn7	B39	Output	
РЕТр7	B40		
PETn8	B44	Output	
PETp8	B45		
PETn9	B47	Output	
PETp9	B48		
PETn10	B50	Output	
PETp10	B51		
PETn11	B53	Output	
PETp11	B54		
PETn12	B56	Output	
PETp12	B57		
PETn13	B59	Output	
PETp13	B60		
PETn14	B62	Output	
PETp14	B63		
PETn15	B65	Output	
PETp15	B66		
PERn0	A17	Input	Receiver differential pair [0:15]. These pins are
PERp0	A18		connected from the add-in card transmitter
PERn1	A20	Input	differential pairs to the receiver differential
PERp1	A21		pairs on the baseboard.
PERn2	A23	Input	
PERp2	A24		The PCIe Receive pins are AC coupled on the
PERn3	A26	Input	add-in card with capacitors and are placed next



PERp3	A27		to the add-in card transmitters. The AC
PERn4	A30	Input	coupling capacitor must be between 176nF
PERp4	A31		(min) and 265nF (max).
PERn5	A33	Input	
PERp5	A34		Refer to Section 6.1 in the PCIe CEM
PERn6	A36	Input	Specification, Rev 4.0 for details.
PERp6	A37		
PERn7	A39	Input	
PERp7	A40		
PERn8	A44	Input	
PERp8	A45		
PERn9	A47	Input	
PERp9	A48		
PERn10	A50	Input	
PERp10	A51		
PERn11	A53	Input	
PERp11	A54		
PERn12	A56	Input	
PERp12	A57		
PERn13	A59	Input	
PERp13	A60		
PERn14	A62	Input	
PERp14	A63		
PERn15	A65	Input	
PERp15	A66		
PERSTO#	B10	Output	PCIe Reset #0, #1. Active low.
PERST1#	A11		
			Indicates when the applied power is within
			tolerance and stable for the add-in card.
			PERST# goes high after 100ms per the PCI CEM
			Specification when the power rails are within

operating limits. The PCIe REFCLKs also become stable within this period of time. PERST is pulled high on the baseboard.
Note: For cards that only support 1 x16, PERSTO# is used. For cards that support 2 x8, PERSTO# is used for the first eight PCIe lanes, and PERST1# is used for the second eight PCIe lanes. Refer to Section 2.2 in the PCIe CEM
Specification, Rev 4.0 for details.

3.4.2 PCIe Present and Bifurcation Control Pins

This section provides the pin assignments for the PCIe present and bifurcation control signals. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure 18.

The PRSNTA#/PRSNTB[0:3]#/BIF[0:2]# pins much be latched within TBD ms of the system AC power on to ensure the correct values are latched by the system. Changing the pin states after this timing window is not allowed. Refer to the AC timing diagram in Section XXX for details.

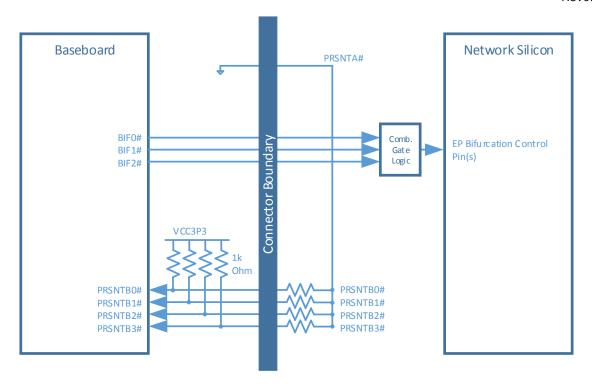
Table 9: Card Pin Descriptions – PCIe Present and Bifurcation Control Pins

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
PRSNTA#	A12	Output	Present A is used for card presence and add-in
			card PCIe capabilities detection. This pin is
			connected to GND on the baseboard. This pin
			is connected to the Present B pins on the add-
			in card.



PRSNTB0#	B42	Input	Present B [0:3]# are used for card presence
PRSNTB1#	A42		detection and PCIe capabilities detection.
PRSNTB2#	A10		
PRSNTB3#	B70		For baseboards, these pins are connected to
			the I/O hub and are pulled up to +3.3V using
			1kOhm resistors.
			For add-in cards, these pins are strapped to
			PRSNTA#. The encoding definitions are
			described in Section 3.6.
			PRSNTB3# is located at the bottom of the 4C
			connector and is only applicable for add-in
			cards with a PCIe width of x16 (or greater).
			Add-in cards that implement a 2C card edge
			do not use the PRSNTB3# pin for capabilities
			or present detection.
BIFO#	A7	Output	Bifurcation [0:2]# are outputs driven from the
BIF1#	A8		baseboard I/O hub and allows the system to
BIF2#	A9		force configure the add-in card bifurcation.
			The BIF[0:2]# encoding definitions are
			described in Section 3.6.
			Note: the required combinatorial logic output
			for endpoint bifurcation is dependent on the
			specific silicon and is not defined in this
			specification.
	I	l	ı ·

Figure 18: PCIe Present and Bifurcation Control Pins



3.4.3 SMBus Interface Pins

This section provides the pin assignments for the SMBus interface signals. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure XXX.

Table 10: Card Pin Descriptions – SMBus

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
SMCLK	A7	Output	SMBus clock. Open drain, pulled up to +3.3V
			on the baseboard.
SMDAT	A8	Input /	SMBus Data. Open drain, pulled up to +3.3V
		Output	on the baseboard.
SMRST#	A9	Output	SMBus reset. Open drain, pulled up to +3.3V
			on the baseboard. Used to reset optional
			downstream SMBus devices (such as
			temperature sensors).



3.4.4 Power Supply Pins

This section provides the pin assignments for the power supply interface signals. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure XXX.

Table 11: Card Pin Descriptions – Power

Signal Name	Pin #	Baseboard	Signal Description
		Direction	Joseph Lands and
GND	Various	GND	Ground return; a total of 46 ground pins are
			on the main 140-pin connector area.
+12V/+12V_AUX	B1, B2,	Power	+12V main or 12V Aux power; total of 6 pins
	B3, B4,		per connector. The 12V pins are rated to 1.1A
	B5, B6		per pin with a maximum derated power
			delivery of 79.2W.
			The +12V power pins must be within the rail
			tolerances when the PWRDIS pin is driven low
			by the baseboard.
+3.3V/3.3V_AUX	B11	Power	+3.3V main or +3.3V Aux power; total of 1 pin
			per connector. The 3.3V pin is rated to 1.1A for
			a maximum derated power delivery of 3.63W.
			The +3.3V power pin must be within the rail
			tolerances when the PWRDIS pin is driven low
			by the baseboard.
PWRDIS	B12	Output	Power disable. Active high.
			This signal is driven by the baseboard.
			When high, this signal notifies the add-in card
			to turn off all systems connected to +12V
			power.

	When low, this signal notifies the add-in card
	to enable the on-card power supplies.

3.4.5 Miscellaneous Pins

This section provides the pin assignments for the miscellaneous interface signals. The AC/DC specifications are defined in Section XXX.

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
RFU, N/C	B68,	Input /	Reserved future use pin. Leave these pins as no
	В69,	Output	connect.
	A68,		
	A69,		
	A70		

Table 12: Card Pin Descriptions – Miscellaneous

3.5 Signal Descriptions – OCP Bay (Primary Connector)

The following section describes the functions in the Primary Connector 28-pin OCP bay. This 28 pin bay is shown in Section 3.3 and have pin numbers designated as OCP_B[1:14], and OCP_A[1:14]. All pin directions on this OCP bay are from the perspective of the baseboard.

Note: The pins that are common to both the Primary and Secondary Connectors are defined in Section 3.4.

3.5.1 PCIe Interface Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the PCIe interface signals on the Primary Connector OCP bay. The AC/DC specifications are defined in Section XXX. An example connection diagram that shows REFCLK2, REFCLK3, PERST2# and PERST3# is shown in Section 3.7.

Table 13: Card Pin Descriptions – PCIe



Signal Name	Pin #	Baseboard	Signal Description
		Direction	
REFCLKn2	OCP_B11	Output	PCIe compliant differential reference clock #2,
REFCLKp2	OCP_B12		and #3. 100MHz HCSL reference clocks are
REFCLKn3	OCP_A11	Output	used for the add-in card PCIe core logic.
REFCLKp3	OCP_A12		
			Note: REFCLK2 and REFCLK3 are not used for
			cards that only support a 1 x16 or 2 x8
			connection.
			Defends Costion 2.1 in the DCIs CEM
			Refer to Section 2.1 in the PCIe CEM
DEDCT2#	OCD 43	Outrout	Specification, Rev 4.0 for details.
PERST2#	OCP_A2 OCP_A3	Output	PCIe Reset #2, #3. Active low.
PERST3#	OCP_AS		Indicates when the applied power is within
			Indicates when the applied power is within tolerance and stable for the add-in card.
			PERST# goes high after 100ms per the PCI CEM Specification when the power rails are
			within operating limits. The PCIe REFCLKs also
			become stable within this period of time.
			PERST is pulled high on the baseboard.
			TENST is pulled high on the baseboard.
			Note: PERST2# and PERST3# are not used for
			cards that only support a 1 x16 or 2 x8
			connection.
			Refer to Section 2.2 in the PCIe CEM
			Specification, Rev 4.0 for details.
WAKE#	OCP_A1	Input	WAKE#. Active low. This signal is pulled up to
			+3.3V on the baseboard with a 10kOhm
			resistor.

This signal is driven by the add-in card to notify the baseboard restore the PCIe link. For add-in cards that support multiple WAKE# signals, their respective WAKE# pins may be tied together as the signal is open-drain to form a wired-OR.
Refer to Section 2.3 in the PCIe CEM Specification, Rev 4.0 for details.

3.5.2 NC-SI Over RBT Interface Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the NC-SI over RBT interface signals on the Primary Connector OCP bay. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure 19.

Refer to the NC-SI Specification for implementation and timing details. For the purposes of this specification, the min and max length of the NC-SI signals shall be between 2 inches and 4 inches. The traces shall be implemented as impedance controlled 50 Ohm nets.

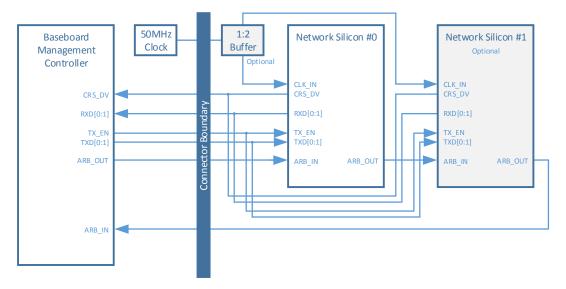
Table 14: Card Pin Descriptions – NC-SI Over RBT

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
RBT_CLK_IN	OCP_A14	Output	Reference clock input. Synchronous clock
			reference for receive, transmit and control
			interface. The clock has a nominal frequency of
			50MHz ±100ppm.
RBT_CRS_DV	OCP_B14	Input	Carrier sense/receive data valid. Signal is used
			to indicate to the baseboard that the carrier
			sense/receive data is valid.
RBT_RXD0	OCP_B9	Input	Receive data. Data signals from the network
RBT_RXD1	OCP_B8		controller to the BMC.
RBT_TX_EN	OCP_A7	Output	Transmit enable.



RBT_TXD0	OCP_A9	Output	Transmit data. Data signals from the BMC to
RBT_TXD1	OCP_A8		the network controller.
RBT_ARB_OUT	OCP_A5	Output	NC-SI hardware arbitration output. Used only if
			the end point silicon supports hardware
			arbitration. Connects to the ARB_IN signal of
			an adjacent device.
			The ARB_IN pin is also routed to the card edge
			to allow multiple devices and OCP slots on the
			baseboard to share the NC-SI ring.
RBT_ARB_IN	OCP_A4	Input	NC-SI hardware arbitration input. Used only if
			the end point silicon supports hardware
			arbitration. Connects to the ARB_OUT signal of
			an adjacent device.
			The ARB_OUT pin is also routed to the card
			edge to allow multiple devices and OCP slots
			on the baseboard to share the NC-SI ring.
SLOT_ID0	OCP_B7	Output	NC-SI Address pin. Used only if the end point
			silicon supports package identification. N/C on
			NIC if not supported.
			Tie to GND for Slot ID = 0
			Tie to +3.3Vaux for Slot ID = 1

Figure 19: NC-SI Over RBT Connection Example



3.5.3 Scan Chain Pins – OCP Bay (Primary Connector)

This section provides the pin assignments for the Scan Bus interface signals on the Primary Connector OCP Bay. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure 20.

Table 15: Card Pin Descriptions – Scan Bus

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
CLK	OCP_B6	Output	Scan clock. The CLK is an output pin from the
			baseboard to the add-in card. The CLK may run
			up to 12.5MHz.
			For baseboard implementations, tie the CLK pin
			directly to GND if the scan chain is not used.
			For NIC implementations, the CLK pin must be
			connected to Shift Registers 0 & 1 as defined
			in the text and Figure 20, below.
DATA_OUT	OCP_B5	Output	Scan clock data output from the baseboard to
			the add-in card. This bit stream is used to shift
			in NIC configuration data.



			For baseboard implementations, tie the DATA_OUT pin directly to GND if the scan chain is not used. For NIC implementations, the DATA_OUT pin may be left floating if it is not used on the add-in card.
DATA_IN	OCP_B4	Input	Scan clock data input to the baseboard. This bit stream is used to shift out NIC status bits. For baseboard implementations, the DATA_IN pin shall be pulled up to 3.3Vaux through a 10kOhm resistor to prevent the signal from floating if a card is not installed. For NIC implementations, the DATA_IN scan chain is required. Shift Registers 0 & 1, as defined in the text and Figure 20 below are required.
LD#	OCP_B3	Output	Scan clock shift register load. Used to latch configuration data on the add-in card. For baseboard implementations, the LD# pin shall be pulled up to 3.3Vaux through a 10kOhm resistor if the scan chain is not used For NIC implementations, the LD# pin must be connected to Shift Registers 0 & 1 as defined in the text and Figure 20, below.

The scan chain bit definition is defined in the two tables below. The scan chain data stream is 32-bits in length for both the DATA_OUT and the DATA_IN streams. The scan chain

implementation is optional on the host, but is mandatory on all OCP NIC 3.0 cards. The scan chain provides side band status indication between the add-in card and the baseboard.

The DATA_OUT bus is an output from the host. The DATA_OUT bus provides initial configuration options to the add-in card. At the time of this writing, the default implementation does not use the DATA_OUT stream and is not implemented on the NIC. However, all baseboard systems that implement the Scan Chain shall connect DATA_OUT between the platform and the Primary Connector for future-proofing NIC implementations.

Byte.bit	DATA_OUT Field	Default	Description
	Name	Value	
0.[07]	RSVD	0b000000	Reserved. Byte 0 value is 0h00.
1.[07]	RSVD	0h00	Reserved. Byte 1 value is 0h00.
2.[07]	RSVD	0h00	Reserved. Byte 2 value is 0h00.
3.[07]	RSVD	0h00	Reserved. Byte 3 value is 0h00.

Table 16: Card Pin Descriptions – Scan Bus DATA_OUT Bit Definition

The DATA_IN bus is an input to the host. The DATA_IN bus provides NIC status indication to the host. The default implementation is completed with two 8-bit 74LV165 parallel in to serial out shift registers in a cascaded implementation. Up to four shift registers may be implemented to provide additional NIC status indication to the host platform.

DATA_IN shift registers 0 & 1 are mandatory for all cards. DATA_IN shift registers 2 & 3 are optional depending on the card type. DATA_IN shift register 2 may be used for future revisions of the scan chain. DATA_IN shift registers 2 & 3 are required for card implementations with 5-8 ports.

The host should read the DATA_IN bus multiple (TBD) times to qualify the incoming data stream.

A 1kOhm pull up resistor shall be implemented on the NIC to the SER input of the last shift register on the DATA_IN scan chain to maintain a default bit value of 0b1 for unused bits for implementations using less than four shift registers.



Table 17: Card Pin Descriptions – Scan Bus DATA_IN Bit Definition

Byte.bit	DATA_OUT Field	Default	Description
	Name	Value	
0.0	PRSNTB[0]#	0bX	PRSNTB[3:0]# value mirrored from the
0.1	PRSNTB[1]#	0bX	Primary Connector.
0.2	PRSNTB[2]#	0bX	
0.3	PRSNTB[3]#	0bX	
0.4	WAKE_N	0bX	PCIe WAKE_N signal mirrored from the Primary Connector.
0.5	TEMP_WARN	0b0	Temperature monitoring pin from on-card thermal solution. Asserted high when temperature sensor exceeds the warning threshold.
0.6	TEMP_CRIT	0b0	Temperature monitoring pin from on-card thermal solution. Asserted high when temperature sensor exceeds the critical threshold.
0.7	FAN_ON_AUX	0b0	When high, FAN_ON_AUX requests the system fan to be enabled for extra cooling when the card is in the S5 state.
1.0	LINK0	0b1	Port 03 link indication. Active low.
1.1	LINK1	0b1	
1.2	LINK2	0b1	0b0 – Link LED is illuminated on the host
1.3	LINK3	0b1	platform. 0b1 – Link LED is not illuminated on the host platform. Steady – link is detected on the port
			Steady = link is detected on the port. Off = no link is detected on the port.
1.4	ACT0	0b1	Port 03 activity indication. Active low.
1.5	ACT1	0b1 0b1	1 3.1 3.13 delivity indication. Active low.

1.6	ACT2	0b1	0b0 – Link LED is illuminated on the host
1.7	ACT3	0b1	platform.
			0b1 – Link LED is not illuminated on the host
			platform.
			Steady = no activity is detected on the port
			Blink = activity is detected on the port.
			Off = no link, see also LINK[3:0] LED bits.
			The LED blink duty cycle is dependent on the
			add-in card implementation TBD.
2.0	ScanChainVer[0]	0b1	ScanChainVer[1:0] is used to indicate the scan
2.1	ScanChainVer[1]	0b1	chain bit definitions. The encoding is as
			follows:
			0b11 – Scan chain bit definitions version 1
			corresponding to OCP 3.0 spec version 1.0.
			All other encodings are reserved.
2.2	RSVD	0b1	Byte 2 bits [2:7] are reserved. These bits shall
2.3	RSVD	0b1	default to the value of 0b1.
2.4	RSVD	0b1	
2.5	RSVD	0b1	
2.6	RSVD	0b1	
2.7	RSVD	0b1	
3.0	LINK4	0b1	Port 47 link indication. Active low.
3.1	LINK5	0b1	
3.2	LINK6	0b1	0b0 – Link LED is illuminated on the host
3.3	LINK7	0b1	platform.
			0b1 – Link LED is not illuminated on the host
			platform.
			Steady = link is detected on the port.



			Off = no link is detected on the port.
3.4	ACT4	0b1	Port 47 activity indication. Active low.
3.5	ACT5	0b1	
3.6	ACT6	0b1	0b0 – Link LED is illuminated on the host
3.7	ACT7	0b1	platform.
			0b1 – Link LED is not illuminated on the host
			platform.
			Steady = no activity is detected on the port
			Blink = activity is detected on the port.
			Off = no link, see also LINK[3:0] LED bits.

Host PLD 74LV594 The 74LV594 DATA_OUTs hift register has no defined function in the current OCP NIC 3.0 specification and is QA QB QC SER DATA OUT QD QE QF QG SRCLK CLK (12.5MHz) SRCLRn QH **RCLRn** Connector Boundary QH GND 3.3 Vau 74LV165#0 VCC PRSNTB[0]# (Mirrored from Primary Connector) PRSNTB[1]# (Mirrored from Primary Connector) PRSNTB[2]# (Mirrored from Primary Connector) CLK INH PRSNTB[3]# (Mirrored from Primary Connector) SH/LDn TEMP_WARN
TEMP_CRIT G DATA_IN QH FAN_ON_AUX QH' SER 3.3 Vau: 74LV165 #1 VCC LINK1 (Active Low = ON, default 0b1) LINK2 (Active Low = ON, default 0b1) C D CLK INH LINK3 (Active Low = ON, default 0b1) ACTO (Active Low = ON, default 0b1) 3.3 Vaux SH/LDn ACT1 (Active Low = ON, default 0b1) ACT2 (Active Low = ON, default 0b1) ACT3 (Active Low = ON, default 0b1) QH' SER GND Implement a 1kOhm pull up to 3.3Vau x for the last shift register on the bus. Optional depending on implementation 74LV165 #2 VCC CLK CLK_INH SH/LDn QH QH' SER GND 74LV165#3 VCC CLK CLK_INH SH/LDn G QH н QH' SER GND

Figure 20: Scan Bus Connection Example



3.5.4 Primary Connector Miscellaneous Pins – OCP Bay (Primary Connector)

This section provides the miscellaneous pin assignments for the pins on the Primary Connector OCP Bay. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure XXX.

Table 18: Card Pin Descriptions – Miscellaneous

Signal Name	Pin #	Baseboard	Signal Description
		Direction	
PWRBRK#	OCP_B2	Output	Power break. Active low, open drain.
			This signal is pulled up to +3.3V on the add-
			in card with a minimum of 95kOhm and the
			baseboard with a stiffer resistance in-order to
			meet the timing specs as shown in CEM.
			This signal is driven low by the baseboard
			and is used to notify that an Emergency
			Power Reduction State is requested.
NIC_PWR_GOOD	OCP_B1	Input	NIC power good. Active high. This signal is
			driven by the add-in card.
			When high, this signal indicates that all of the
			add-in card power rails are operating within
			nominal tolerances.
			When low the add-in card power supplies are
			not yet ready or are in a fault condition.
			Add-in cards may implemented a cascaded
			power good output or use a discrete power
			good monitor on the card. This signal is
			pulled down to ground with a 100kOhm
			resistor on the baseboard to prevent a false

			power good indication if no add-in card is present.
GND	OCP_A6 OCP_A10	GND	Ground return; a total of 5 ground pins are on the OCP bay area.
	OCP_A13		
	OCP B10		
	OCP_B13		

3.6 PCIe Bifurcation Mechanism

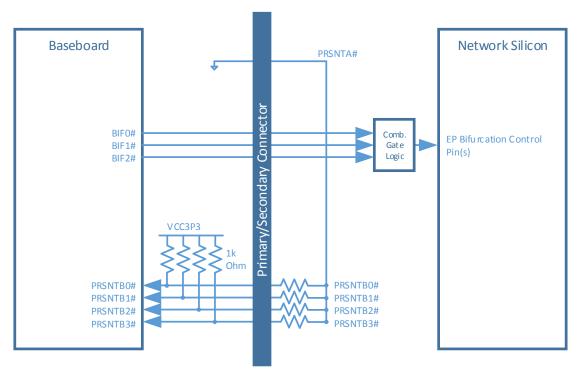
OCP3.0 baseboards and add-in cards support multiple bifurcation combinations. Single socket baseboards with a single or multiple root ports, as well as a multi-socket baseboards with a single or multiple root ports cases are supported. The bifurcation mechanism also supports add-in cards with a single or multiple end points. These features are accomplished via I/O pins on the Primary and Secondary connector:

- PRSNTA#, PRSNTB[3:0]#. The PRSNTA# pin connects to the PRSNTB# pins as a hard coded value on the add-in card. The encoding of the PRSNTB[3:0]# pins allows the baseboard to determine the PCIe Links available on the add-in card.
- BIF[3:0]#. The BIF# pin states are controlled by the baseboard and allows the
 baseboard to override the default end point bifurcation for silicon that support
 bifurcation. Additional combinatorial logic is required and is specific to the card
 silicon. The combinatorial logic is not covered in this specification.

The high level bifurcation connections are shown in Figure 21.

Figure 21: PCIe Bifurcation Pin Connections Support





3.6.1 PCIe Add-in Card to Baseboard Bifurcation Configuration (PRSNTA#, PRSNTB[3:0]#)

The add-in card to baseboard configuration mechanism consists of four dual use pins (PRSNTB[3:0]#) on the add-in card and a grounded PRSNTA# pin on the baseboard. These pins provide card presence detection as well as mechanism to notify the baseboard of the pre-defined PCIe lane width capabilities. The PRSNTB[3:0]# pins are pulled up to +3.3V on the baseboard and are active low signals. A state of 0b1111 indicates that no card is present in the system. Depending on the capabilities of the add-in card, a selection of PRSNTB[3:0]# signals may be strapped to the PRSNTA# signal and is pulled low by the baseboard. The encoding of the PRSTNB[3:0]# bits is shown in Table 19 for x16 and x8 PCIe cards.

3.6.2 PCIe Baseboard to Add-in Card Bifurcation Configuration (BIF[2:0]#)

Three signals (BIF[2:0]#) are driven by the baseboard to notify requested bifurcation on the add-in card silicon. This allows the baseboard to set the lane configuration on the add-in card that supports multiple bifurcation options.

For example, a baseboard that has four separate hosts that support a 4 x4 connection, should appropriately drive the BIF[2:0]# pins per Table 19 and indicate to the add-in card silicon to setup a 4 x4 configuration.

As previously noted, the BIF[2:0]# signals require additional combinatorial logic to decode the BIF[2:0]# value and appropriately apply it to the end-point silicon. The combinatorial logic is not covered in the specification as its implementation is specific to the vendor silicon used.

3.6.3 PCIe Bifurcation Decoder

The state combination of each of the PRSNTB[3:0]# and BIF[2:0]# pins deterministically sets the PCIe lane width for a given combination of baseboard and add-in cards. Table 19 shows the resulting number of PCIe links and its width for known combinations of baseboards and add-in cards.

*Note: The baseboard must disable PCIe lanes during the initialization phase if the number of detected PCIe links are greater than what is supported on the baseboard to prevent a nondeterministic solution. For example, if the baseboard only supports a 1 x16 connection, and the add-in card only supports a 2 x8 connection, the baseboard must disable PCIe lanes 8-15 to prevent any potential LTSSM issues during the discovery phase.



Table 19: PCIe Bifurcation Decoder for x16 and x8 Card Widths

					Single Host				CACC	Dual Host	Contract to the contract to th	Quadricot 110st
		Host		1Host	1 Host	1 Host	1 Host	RSVD	RSVD	2 Hosts	4 Hosts	4 or 8 Hosts
		Host CPU Sockets	1 Upstream Socket	1 Upstream Socket	1 Upstream Socket	2 Upstream Sockets	1 Upstream Socket 2 Upstream Sockets 4 Upstream Sockets	RSVD		ckets Host)	4 Upstream Sockets (1 Socket per Host)	418 Upstream Sockets (1 Socket per Host)
Supp	Network Card – Supported PCIe Configurations	Total PCle Links	1 Link (No Bifurcation)	1 or 2 Links	1, 2, or 4 Links	2 Links	4 Links	RSVD	RSVD	2 Links	4 Links	4 or 8 x2 links
		System Support	75	1x16,1x8,1x4,1x2,1x1	1x16, 1x8, 1x4, 1x2, 1x1	1x8,1x4,1x2,1x1		RSVD	RSVD			
			-	2x8,2x4,2x2,2x1	2x8,2x4,2x2,2x1	2x8,2x4,2x2,2x1				2x8,2x4,2x2,2x1		
Minimum					4×4,4×2,4×1		4 x4, 4 x2, 4x1				4×4,4×2,4×1	4×2,4×1
Required		System Encoding	00000	00090	00090	00001	00010	06011	06100	06101	05110	0b111
Card Card S Edge Name	Card Short x16 Cards	Add-in-Card Encoding	,	ı			-				,	
	esent Card Not Present		BSVD - Card not present in the sustem	The custom								
			1%8	1×8	1%8	1×8	1×4			1×8	1×4	1,42
1	1×8					(Socket 0 only)	(Socket 0 only)			(Host 0 only)	(Host 0 only)	(Host 0 only)
-	1x4,1x2,1x1 1x4	0b1 110	1×4	1×4	1×4	1x4 (Socket 0 only)	1x4 (Socket 0 only)			1x4 (Host 0 only)	1x4 (Host 0 only)	1x2 (Host 0 only)
-	1x2,1x1 1x2	0b1 110	1×2	142	1×2	1 _x 2 (Socket 0 only)	1 _k 2 (Socket 0 only)			1x2 (Host 0 only)	1 _K 2 (Host 0 only)	1x2 (Host 0 only)
	14 14	061110	181	181	181	1x1 (Socket 0 only)	1x1 (Socket 0 only)			1x1 (Host 0 only)	1x1 (Host 0 only)	1x1 (Host 0 only)
1,80	1x8,1x4,1x2,1x1 1x8 Option B 2x4,2x2,2x1	0b1 101	1×8	9×L	1x8	1x8 (Socket 0 only)	2×4			1x8 (Host 0 only)	2 44	2x2 (Host 0& 1only)
2,48	2x8,2x4,2x2,2x1 2x8 Option B 4x4,4x2,4x1	0b11 01	1%8.	2 ×8	2x8	2×8	4×4			2×8	4×4	2 x2 (Host 0 & 1 only)
1,80	1x8,1x4 2x4, 1x8 Option D 4x2 (First 8 lanes), 4x1	0b1100	1%8	2 1/4	2×4	1x8 (Socket 0 only)	2×4			1x8 (Host 0 only)	2×4	4 x2
1×16 G	1x16, 1x8, 1x4 2x8, 2x4, 1x16 Option D 4x4, 4x2 (First 8 lanes), 4x1	06/1100	1x16	1×16	1×16	2 x8	4 %4			2 x8	4×4	4%2
RSVD RSVD	RSVD	0b1 011	RSVD - The encoding of 0	51011 is reserved due to in	RSVD - The encoding of 0b1011 is reserved due to insufficient spacing between PRSNTA and PRSNTB2 pin to provide positive oard identification.	n PRSNTA and PRSNTB2	pin to provide positive care	identifical	ion.			
2	2 x4, 2 x2, 2 x1 2 x4 1 x4, 1 x2, 1 x1	0b1 010	1×4	2×4	2×4	1x4 (Socket 0 only)	2×4			1x4 (Host 0 only)	2×4	2x2 (Host 0& 1only)
RSVD RSVD		1 0b1 001										
BSVD RSVD		001000 t						,	,			
1,	1x16, 1x8, 1x4, 1x2, 1x1 1x16	060111	1×16	1×16	1×16	1x8 (Socket 0 only)	1×4 (Socket 0 only)		-	1x8 (Host 0 only)	1x4 (Host 0 only)	1x2 (Host 0 only)
2 *8 □	2 x8, 2 x4, 2 x2, 2 x1 2 x8 Option A	060110	1%8.	2 **8	2 **8	2×8	2 x4 (Socket 0 & 2 only)			2 **8	2 x4 (Host 0 & 2 only)	1x2 (Host 0 & 1only)
1×16C	1x16.7x8,7x4,7x2,7x1 1x16.0ption B 2x8,2x4,2x2,2x1	060101	1×16	1×16	1×16	2×8	2 x4 (Socket 0 & 2 only)		,	2 **8	2 x4 (Host 0 & 2 only)	2x2 (Host 0 & 1only)
1×16 G	1x16, 1x8, 1x4 2x8, 2x4, 2x2, 2x1 1x16 Option C 4x4, 4x2, 4x1	060 100	1×16	1×16	1×16	2 **8	4×4			2 48	4×4	2 x 2 (Host 0 & 1 only)
	4×4, 4×2, 4×1	060 011	1×4.	2×4*	4×4	2x4 (EP 0 and 2 only)	4×4			2 x4 (EP 0 and 2 only)	4×4	4 x2 (Host 0 & 1 only)
RSVD RSVD		060010						,	,			
		060 001							,			
RSVD RSVD	RSVD	000000		-				,				,

3.6.4 Bifurcation Detection Flow

[Need input and clarification from system vendors]

The following detection flow shall be used to determine the resulting link count and lane width based on the baseboard and add-in card configurations.

- 1. The baseboard reads the state of the PRSNTB[3:0]# pins. If the resulting value is not 0b1111, a card is present.
- 2. Firmware determines the add-in card PCIe lane width capabilities per Table 19 by reading the PRSNTB[3:0]# pins.
- 3. The baseboard reconfigures the PCIe bifurcation on its ports to match the highest common lane width and lowest link count on the card.
- 4. For cases where the baseboard request a link count override (such as requesting a 4-host baseboard requesting 4 x4 operation on a supported card that would otherwise default to a 2 x8 case), the BIF[0:2]# pins would be asserted as appropriate. Doing so assumes the add-in card supports the requested link override.
- 5. PERST# is deasserted after the 100ms window as defined by the PCIe specification.

 Refer to Section/Figure XXX for timing details.



3.6.5 PCle Bifurcation Examples

For illustrative purposes, the following figures show several common bifurcation permutations.

Figure 22 illustrates a single host baseboard that supports x16 with a single controller add-in card that also supports x16 (Type 6). The PRSTNB[3:0]# state is 0b0111. The BIF[2:0]# state is 0b000 as there is no need to instruct the end-point network controller to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16. The single host baseboard determines that it is also capable of supporting 1 x16. The resulting link width is 1 x16.

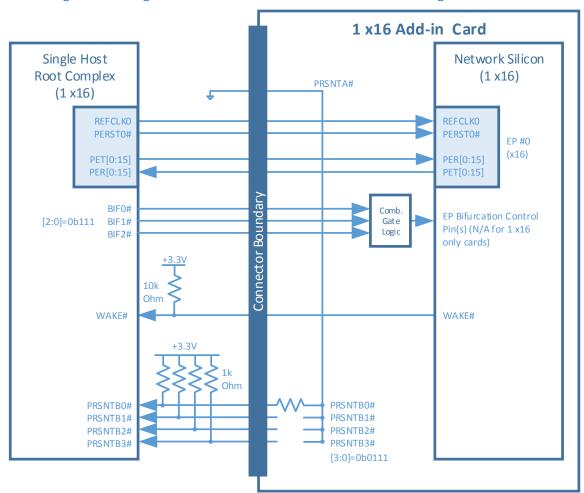


Figure 22: Single Host (1 x16) and 1 x16 Add-in Card (Single Controller)

Figure 23 illustrates a single host baseboard that supports 2 x8 with a single controller add-in card that also supports 2 x8 (Type 2). The PRSTNB[3:0]# state is 0b0110. The BIF[2:0]#

state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 2 x8. The single host baseboard determines that it is also capable of supporting 2 x8. The resulting link width is 2 x8.

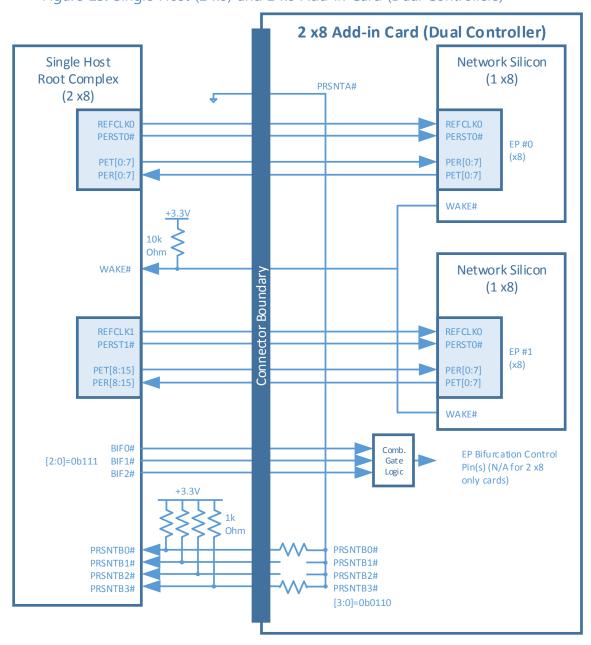


Figure 23: Single Host (2 x8) and 2 x8 Add-in Card (Dual Controllers)



Figure 24 illustrates a four host baseboard that supports 4 x4 with a single controller add-in card that supports 1 x16, 2 x8 and 4 x4 (Type 4). The PRSTNB[3:0]# state is 0b0011. The BIF[2:0]# state is 0b101 as the end point network controller is forced to bifurcate to 4 x4. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16, 2 x8 and 4 x4. The four host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

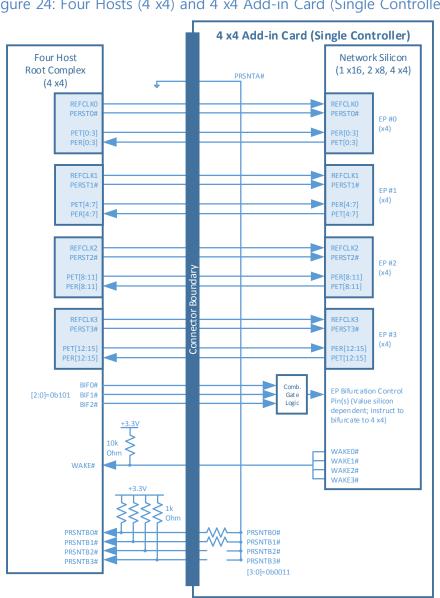


Figure 24: Four Hosts (4 x4) and 4 x4 Add-in Card (Single Controller)

Figure 25 illustrates a four host baseboard that supports 4 x4 with a four controller add-in card that supports 4 x4 (Type 3). The PRSTNB[3:0]# state is 0b0011. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 4 x4. The four host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

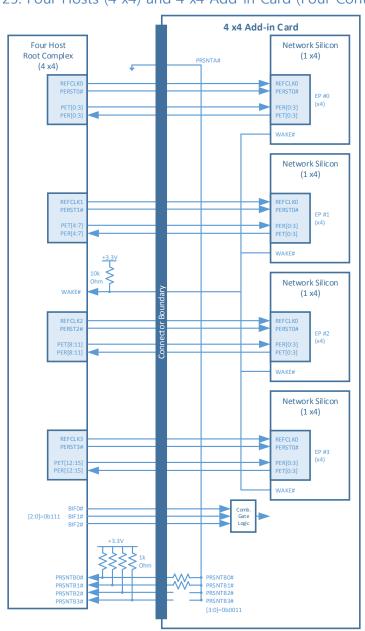


Figure 25: Four Hosts (4 x4) and 4 x4 Add-in Card (Four Controllers)



2 x8 Add-in Card (Dual Controller) Network Silicon Single Host (1 x8)**Root Complex** PRSNTA# (1 x16) **REFCLKO** REFCLKO PERSTO# PERSTO# EP #0 (x8) PER[0:7] PET[0:15] PET[0:7] PER[0:15] WAKE# Lanes 8:15 disabled WAKE# Network Silicon Connector Boundary (1 x8)**REFCLKO** The second x8 PERSTO# EP #1 is not supported on (x8) PER[0:7] this host. PET[0:7] WAKE# BIFO# Comb **EP Bifurcation Control** [2:0]=0b111 BIF1# Gat e Pin(s) (N/A for 2 x8 Logic BIF2# only cards) +3.3V PRSNTB0# PRSNTB0# PRSNTB1# PRSNTB1# PRSNTB2# PRSNTB2# PRSNTB3# PRSNTB3# [3:0]=0b0110

Figure 26: Single Host with no Bifurcation (1 x16) and 2 x8 Add-in Card (Two Controllers)

3.7 PCIe Clocking Topology

The OCP NIC 3.0 specification allows for up to four PCIe REFCLKs on the Primary Connector and up to two PCIe REFCLKs on the Secondary Connector. In general, the association of each REFCLK is based on the PCIe Link number on a per connector basis and is shown in Table 20.

REFCLK #	Description	Availability (Connector)
REFCLK0	REFCLK associated with Link 0.	Primary and Secondary Connectors.
REFCLK1	REFCLK associated with Link 1.	Primary and Secondary Connectors.
REFCLK2	REFCLK associated with Link 2.	Primary Connector only.
REFCLK3	REFCLK associated with Link 3.	Primary Connector only.

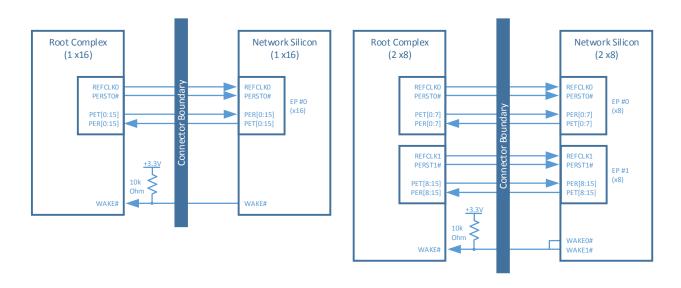
Table 20: PCIe Clock Associations

As noted in the Pin Definition (Section 3.3), cards that only implement the Primary Connector have up to four PCIe REFCLKS (0-3). Cards that implement both the Primary and Secondary connectors have a total of up to 6 REFCLKs.

For each add-in card, the following REFCLK connection rules must be followed:

- For a 1 x16 capable add-in card, REFCLK0 is used for lanes [0:15].
- For a 2 x8 capable add-in card, REFCLK0 is used for lanes [0:7] and REFCLK1 is used for lanes [8:15].
- For a 4 x4 capable add-in card, REFCLK0 is used for lanes [0:3], REFCLK1 is used for lanes [4:7], REFCLK2 is used for lanes [8:11] and REFCLK3 is used for lanes [12:15].
 Pins for REFCLK2 and REFCLK3 are described in Section 3.5.1 and are located on the 28-pin OCP bay.

Figure 27: PCIe Interface Connections for 1 x16 and 2 x8 Add-in Cards





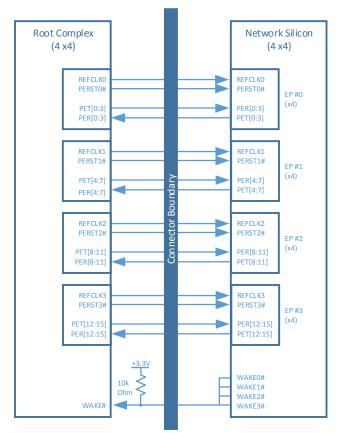


Figure 28: PCIe Interface Connections for a 4 x4 Add-in Card

3.8 PCIe Bifurcation Results and REFCLK Mapping

For the cases where bifurcation is permissible, this section enumerates all of the supported PCIe link, lane and REFCLK mappings for each supported configuration. The bifurcation decoder is shown in Section 3.6.3.

Table 21: Bifurcation for Single Host, Single Upstream Socket and Single Upstream Link
(BIF[2:0]#=0b000)

Part Care	Single	Host, Single Ups	Single Host, Single Upstream Socket, One Upstream Link, no bifurcation	no bifurcation		1x16, 1x8, 1x4, 1x2, 1																		
186, 187, 187, 187, 187, 187, 187, 187, 187	i C	Card Short	Supported Bifarcation Modes	Add-in-Card Encoding	1		Upstream	BIF[2:0]	Description link	3	-	Ş	;					-						
145, 142, 141 141	e/a	Not Present		061111	1 Hoot		1Link	00000																
145, 122, 131 Children Chil	S	1x8	-	061110	1 Host	1 Upstream Socket	1 Link	00090	1x8	Link 0, Lane 0	-	-	-	-	-	-	nk O.							
142,141 Objie Ob	28	1×4	1x4,1x2,1x1	0b1 110	1 Host	1 Upstream Socket	1 Link	00090	1x4	Link 0, Lane 0	-	-	_											
141 141	20	1x2		0b1 110	1Host	1 Upstream Socket	1 Link	00090	1x2	Link 0, Lane 0	Link 0, Lane 1													
146 146	8	1x1		0b1 110	1Host	1 Upstream Socket	1 Link	00090	1×1	Link 0, Lane 0														
10.00 1.00	2	1x8 Option B	×	0b1 101	1Host	1 Upstream Socket	1 Link	00090	1x8	Link 0, Lane 0							nk O,							
146,144 146,	Q.	2 x8 Option E	.2 x1	0b1 101	1 Host	1 Upstream Socket	1 Link	00090	1x8*	Link 0, Lane 0							nk O, ne 7							
1765 1244 200	S	1x8 Option D		061 100	1Host	1 Upstream Socket	1 Link	00090	1x6	Link 0, Lane 0							nk 0, ne 7							
SEYON Debte Higher Updates Secket Light Debte High Higher Updates Secket Light Debte High	ô,	1x16 Option C		0b1 100	1Host		1 Link	00090	1×16	Link 0, Lane 0									Link O, Link O, Lane 3 Lane 10	r 0, Link 0, r 10 Lane 11	O, Link O, 11 Lane 12	0, Link 0, 12 Lane 13	Link 0, 3 Lane 14	Link 0, Lane 15
124 122 131 124 122 131	RSVD	RSVD		0b1 011	1 Host	╙	1 Link	00090																
SSY/D for foreware Seconding DNOOT Thorax Libertonn Socket Liber DNOOD The Color Liber Liber DNOOD The Color Liber L	SS	2×4		0b1 010	1Host		1 Link	00090	1×4	Link 0, Lane 0			Link O, Lane 3											
150 150	RSVD	RSVD	RSVD for future x8 encoding	0b1 001	1 Host		1Link	00000													+			Ц
2.06, 2.04, 2.02, 2.14 2.06, 2.04, 2.02, 2.14 2.06, 2.04, 2.02, 2.14 2.06, 2.04, 2.02, 2.14 2.06, 2.04, 2.02, 2.14 2.06, 2.04, 2.02, 2.14 2.06, 2.04, 2.02, 2.14 2.06, 2.04, 2.02, 2.14 2.06, 2.04, 2.02, 2.14 2.06, 2.04, 2.14 2.06, 2.04, 2.14 2.06, 2.04, 2.14 2.06, 2.04, 2.14 2.06, 2.04, 2.14 2.06, 2.04, 2.14 2.06, 2.04, 2.14 2.06, 2.04, 2.14 2.06, 2.04 2.06, 2.04 2.06, 2.04 2.06, 2.04 2.06, 2.04 2.06, 2.04 2.06, 2.04 2.06, 2.04 2.06, 2.04 2.06, 2.04 2.06, 2.04 2.06, 2.04 2.06, 2.04 2.06, 2.04 2.06, 2.04 2.06, 2.04 2.06, 2.04 2.06, 2.04 2.06, 2.06 2.06, 2.06 2.06, 2.06 2.06, 2.06 2.06, 2.06 2.06, 2.06 2.06, 2.06 2.06, 2.06 2.06, 2.06 2.06, 2.06 2.06, 2.06 2.06	4c 0	1xt6	1x16,1x8,1x4,1x2,1x1	000111	1Host		1 Link	00000	1x16	Link 0,	-	-	-	-	-		-	-	Link 0, Link 0, Lane 3 Lane 10	Link 0, Link 0, Lane 10 Lane 11	0, Link 0,	0, Link 0, 12 Lane 13	Link 0,	Link 0,
145 1-52 1-54 1-52,1-54 Deb010-1 Host Uperream Societ Ulaik Deb000 1345 Liako	Ç	2 x8 Option A		000110	1Host	1 Upstream Socket	1 Link	00090	1x8*	Link 0, Lane 0	-	-	-	-		-				_				
1786, 158, 154 1880,	Q	1x16 Option E	1x1	000101	1 Host	1 Upstream Socket	1 Link	00090	1×16	Link 0, Lane 0									Link O, Link O, Lone 3 Lone 10			0, Link 0, 12 Lane 13	. Link 0, 3 Lane 14	
4 4.4.4.2,4.71 0b0011 Hott Upstream Sectet 11th 0b000 174* Link 0, Lin	40	1×16 Option C	1x16,1x8,1x4 2x8,2x4,2x2,2x1 5 4x4,4x2,4x1	0001000	1 Host	1 Upstream Socket	1 Link	00090	1×16	Link 0, Lane 0									Link O, Link O, Lane 3 Lane 10	Link O, Link O, Lane 10 Lane 11	0, Link 0, 11 Lane 12	0, Link 0, 12 Lane 13	Unk 0,	Link O,
RSVD 0b.0000 Histor Upgrteam Socket Ulink RSVD 0b.0000 Histor Upgrteam Socket Ulink RSVD 0b.0000 Histor Upgrteam Socket Ulink	4c	4 ×4		050 011	1 Host	1 Upstream Socket	1 Link	00090	1×4*	Link 0, Lane 0			Link 0, Lane 3											
RSVD	RSVD	RSVD		0b0 010	1 Host	1 Upstream Socket	1Link	00090																
RSVD 060000 1Host 1Upstream Socket 1Link	RSVD	RSVD		000 001	1 Host	4	1Link	00090														-		
	RSVD	RSVD	RSVD	000000	1 Host		1 Link	00090																



Table 22: Bifurcation for Single Host, Single Upstream Socket and Single/Dual Upstream
Links (BIF[2:0]#=0b000)

Single H	set, Single Upet	Single Host, Single Upstream Socket, One or Two Upstream Links	sam Links		1x16,1x8,1x4,1x2,1 2x8,2x4,2x2,2x1																		
E C	Min Support	rted Bifurcation	Add-in-Card Encoding	1		Upstream	BIF[2:0]		9		-				-	-	-						
ela	Not Present	Card Not Present	061111	_	1 Upstream Socket	1 or 2 Links	00000	· ·			7								2		2		
		1x8,1x4,1x2,1x1	0b1110	1Host	1 Upstream Socket	1 or 2 Links	0000	1x8	Link 0,	Link 0,	Н	⊢	Link 0,	⊢	⊢	,0 ×					L		L
20	1x8						nnnan		Lone 0	Lone 1	_	_	Lone 4	-	Lane 6 La	Lone 7			_				
30	1×4	1x4,1x2,1x1	0b1 110	1 Host	1 Upstream Socket	1 or 2 Links	00090	1×4	Link 0, Lane 0	Link 0, Lane 1	Link O, L	Link 0, Lane 3											
20	1x2	1x2,1x1	061110	1 Host	1 Upstream Socket	1 or 2 Links	00090	1x2	Link 0, Lane 0	Link 0, Lane 1													
20	1×1	121	051110	1Host	1 Upstream Socket	1 or 2 Links	00090	121	Link 0, Lane 0														
ပ္လ	1x8 Option B	1x8,1x4,1x2,1x1 1x8 Option B 2x4,2x2,2x1	0b1 101	1 Host	1 Upstream Socket	1 or 2 Links	00090	1x8	Link 0, Lane 0	Link 0,	Link O, L	Link O, L	Link O, L	Link O, Li Lane 5 La	Link O, Lin Lanc 6 La	Link O, Lone 7							
9	2 x8 Option B	2 x 8, 2 x 4, 2 x 2, 2 x 1 2 x 8 Option B 4 x 4, 4 x 2, 4 x 1	0b1 101	1 Host	1 Upstream Socket	1 or 2 Links	00090	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link O, L	Link O, L Lane 3 L	Link O, L	Link O, Li Lane 5 La	Link O, Lin Lanc 6 La	Link O, Lin Lane 7 Lar	Link 1, Lin Lane 0 Lar	Link 1, Link 1, Lane 1 Lane 2	1, Link 1, 2 Lane 3	1, Link 1, 3 Lane 4	Link 1,	Link 1, Lane 6	Link 1, Lane 7
S	1x8 Option D	1x8,1x4 2x4, 1x8 Option D 4x2 (First 8 lanes), 4x1	0b1100	1 Host	1 Upstream Socket	1 or 2 Links	00090	1x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, 1 Lane 2 1	Link 0, L Lane 3 L	Link 0, L Lane 4 L	Link O, Li Lane 5 La	Link O, Lin Lane 6 La	Link 0, Lane 7							
ĵ.	1x16 Option D	1x16,1x8,1x4 2x8,2x4, 1x16 Option D 4x4,4x2 (First 8 lance),4x1	0b1100	1 Host	1 Upstream Socket	1 or 2 Links	00090	1×16	Link 0, Lane 0	Link 0, Lane 1	Link O, L	Link 0, L Lane 3 L	Link 0, L Lane 4 L	Link O, Li Lane 5 La	Link O, Lin Lane 6 La	Link O, Lin Lane 7 Lar	Link O, Lin Lane 8 Lan	Link O, Link O, Lane 3 Lane 10	0, Link 0, 10 Lane 11	0, Link 0, 11 Lane 12	1, Link 0, 2 Lane 13	Link 0,	Link 0, Lane 15
RSVD RSVD	RSVD	RSVD	061011	1 Host	1 Upstream Socket	1 or 2 Links	00090																
S	2 x4	2 x 4, 2 x 2, 2 x 1 1 x 4, 1 x 2, 1 x 1	0b1 010	1Host	1 Upstream Socket	1 or 2 Links	00090	1×4	Link 0, Lane 0	Link 0, Lane 1	Link O, L	Link 0, Lane 3											
RSVD RSVD	RSVD	RSVD for future x8 encoding 0b1001	0b1001	1 Host	1 Upstream Socket	1 or 2 Links	00000									H	H						
2	Dave	1x16,1x8,1x4,1x2,1x1	000111	1Host	1 Upotream Socket	1 or 2 Links	00000	1×16	Link 0,	+	-	-	-	-	-	-	-	+	-	+		-	+
ų ų	1x16 2x8 Option A	2x8,2x4,2x2,2x1	000110	1Host	1 Upstream Socket	1 or 2 Links	00090	2 x8	Link 0,	Link 0,	Link 0, L	Link 0, L	Link 0, L	Link O, Li	Link O, Lin Lanc 6 La	Link O, Lin	Link 1, Lin Lane 0 Lar	Link 1, Link 1, Lane 1 Lane 2	1, Link1,	1, Link 1, 3 Lane 4	Link 1,	Link 1,	Link 1,
Ç	1x16 Option B	1x16,1x8,1x4,1x2,1x1 1x16 Option B 2x8,2x4,2x2,2x1	000101	1 Host	1 Upstream Socket	1 or 2 Links	00090	1x16	Link 0, Lane 0		-	-		-	-						_		
Ç.	1×16 Option C	1x16,1x8,1x4 2x8,2x4,2x2,2x1 1x16 Option C 4x4,4x2,4x1	0001000	1 Host	1 Upstresm Socket	1 or 2 Links	00090	1×16	Link 0, Lane 0	Link 0, Lane 1	Link O, L	Link O, L	Link O, L	Link O, Li Lane 5 La	Link O, Lin Lane 6 La	Link O, Lin Lane 7 Lar	Link O, Lin Lane 8 Lan	Link O, Link O, Lane 3 Lane 10	0, Link 0, 10 Lane 11	0, Link 0, 11 Lane 12	t. Link 0, 2 Lane 13	Link 0,	Link O, Lane 15
40	4×4	4 x4, 4 x2, 4 x1	050 011	1 Host	1 Upstream Socket	1 or 2 Links	00090	2×4*	Link 0, Lane 0	Link 0, Lane 1	Link O, L	Link 0, Lane 3				Lin	Link 2, Lin Lone 0 Lor	Link 2, Link 2, Lane 1 Lane 2	2, Link2, 2 Lane3	പ്ര			
RSVD RSVD	RSVD	RSVD		1 Host	1 Upstream Socket	1 or 2 Links	00090																
RSVD RSVD	RSVD	RSVD	Ì	1 Host	_	1 or 2 Links	00000				1	1	1	1	+	+	+	+	+	1	4		
RSVD RSVD	RSVD	RSVD	000090	140%	1 Upotresm Socket	1 or 2 Links	00090																

Table 23: Bifurcation for Single Host, Single Upstream Socket and Single/Dual/Quad

Upstream Links (BIF[2:0]#=0b000)

					1x16,1x8,1x4,1x2,1																		
					2 x8, 2 x4, 2 x2, 2 x1																		
Single	Host, Single Up:	Single Host, Single Upstream Socket, One, Two or Four Upstream Links	Jostream Links		4 x4, 4 x2, 4 x1							-	-	-	-	-	-		-	-	-	-	-
į	Mia Suppor	Supported Bifurcation	Add-in-Card			-	BIF[2:0]																
į	Vidth Name	Spoul	PRSNTB[3:0]#	Host	Upstream Devices	Links		Resulting Link	Lane 0	Lane 1	Lane 2	Lane 3 L	Lane 4	Lane 5 La	Lane 6	Lane 7 Lan	e 8 Lar	Lane 8 Lane 9 Lane 10 Lane 11 Lane 12 Lane 13 Lane 14 Lane 15	10 Lane	t 11 Lane	12 Lane	13 Lane	14 138
c/u	Not Present	Card Not Present	0b1111	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090																
ပ္လ	1x8	1x8,1x4,1x2,1x1	051110	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	1x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, 1 Lane 3	Link O, L	Link O, Lin Lane 5 La	Link O, Lin Lane 6 La	Link 0, Lane 7							
ပ္လ	1×4	1x4,1x2,1x1	061110	1Host	1 Upstream Socket	1, 2, or 4 Links	00090	1×4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3											
ပ္လ	1x2	1x2,1x1	061110	1Host	1 Upstream Socket	1, 2, or 4 Links	00090	1x2	Link 0, Lane 0	Link 0, Lane 1													
28	ž	1x1	061110	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	1x1	Link 0, Lane 0														
ပ္လ	1x8 Option E	1x8,1x4,1x2,1x1 1x8 Option B 2x4, 2x2, 2x1	0b11 01	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	1x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, 1 Lane 3	Link O, L	Link O, Lin Lane 5 La	Link O, Lin Lane 6 La	Link 0, Lane 7							
û	2 x8 Option E	2 x8, 2 x4, 2 x2, 2 x1 2 x8 Option B 4 x4, 4 x2, 4 x1	0b11 01	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	2 x8	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, 1 Lane 3	Link O, L	Link O, Lin Lane 5 La	Link O, Lin Lane 6 La	Link O, Lin Lane 7 Lar	Link 1, Lin Lane 0 Lar	Link 1, Link 1, Lane 1 Lane 2	k1, Link1, c2 Lane3	k1, Link1, e3 Lane4	11. Link 1, 5.4 Lane 5	1, Link 1,	Link1, b Lane7
		1x8,1x4 2x4,	001100	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	1x8	Link O, Lane O								_	_	_	_		-	_
S	1x8 Option L	1x8 Option D 4x2 (First 8 lanes), 4x1	0000	17.00	Т			3	0.171	+	+	+	+	+	+	+	+	-	_	-	-	-	-
		2x8,2x4,	9	ПОЭТ	Opercean socket	1, 4, of 4 LIBKS	00090	2 ×	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5 La	Lanc 6 La	Lane 7 Lan	Lane 8 Lan	Lane 3 Lane	Link O, Link O,	e ff Lane 12	12 Lane 13	13 Lane 14	Lane 15
40		1x16 Option D 4x4, 4x2 (First 8 lanes), 4x1					00000																+
HSVD	RSVD	RSVD	0b1 011	1 Host	7	1, 2, or 4 Links	00090			+	+	+	+	+	+		1	+	1	1	1	1	+
S	2 x4	2x4, 2x2, 2x1 1x4, 1x2, 1x1	051 010	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	2×4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, L	Link 1, Li Lane 1 La	Link 1, Lir Lane 2 Lar	Link 1, Lane 3							
RSVD	RSVD	RSVD for future x8 encoding 0b1001	0b1 001	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090																
RSVD	RSVD RSVD	RSVD for future x8 encoding	0P1000	1Host	1 Upstream Socket	1, 2, or 4 Links	00000			4	4	4	+	+	+	+	+	4	4	4	4	4	4
Ç	1×16	1x16, 1x8, 1x4, 1x2, 1x1	060111	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	1×16	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2				Link O, Lin Lanc 6 La		Link O, Lin Lanc 8 Lan	Link O, Link Lanc 3 Lanc	Link O, Link Lone 10 Lone	Link O, Link O, Lone 11 Lone 12	: 0, Link 0, : 12 Lane 13	0, Link 0, 13 Lane 14), Link 0, 4 Lane 15
û	2 x8 Option A	2x8,2x4,2x2,2x1 A	000110	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	2 x8	Link 0, Lane 0	Link 0,	Link 0, Lane 2	Linko, L	Link O, L	Link O, Lin Lane 5 La	Link O, Lin Lanc 6 La	Link O. Lin	Link 1, Lin Lanc 0 Lar	Link 1, Link 1, Lane 1 Lane 2	k1, Link1, c2 Lane 3	k1, Link1, e3 Lane4	1. Link 1, 2.4 Lane 5	1, Link 1,	Link 1, 6 Lane 7
		1x16,1x8,1x4,1x2,1x1	000101	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090	1×16	Link O,	⊢	⊢	⊢	⊢	⊢	⊢			-	-				
ņ	1x16 Option	1x16 Option B 2x8, 2x4, 2x2, 2x1	000000	4 March	41 Instrum Carles	4 O and links		4.46	Lane O	Lanel	Lane 2	Lane 3	Lane 4	Lane 5	Lane 5	Lane 7 Lan	Lane 8 Lan	Lane 3 Lane	Lane 10 Lane 11	e II Lane 12	12 Lane 13	13 Lane 14	+
Ş	1x16 Option (1x10, 1x0, 1x0, 1x0 2x8, 2x4, 2x2, 2x1 1x16 Option C 4 x4, 4 x2, 4 x1	0000	1000	Opercean socket	1, 2, of 4 LIBKS	00000	oix.	Lane 0	Lane 1													t Lane 15
Ç	4 ×4	4 x4, 4 x2, 4 x1	060 011	1 Host	1 Upstresm Socket	1, 2, or 4 Links	00090	4×4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, Lane 3	Link 1, I	Link 1, Li	Link 1, Lir Lone 2 Lor	Link 1, Lin Lane 3 Lar	Link 2, Lin Lane 0 Lar	Link 2, Link Lone 1 Lone	Link 2, Link 2, Lone 2 Lone 3	c2, Link3, c3 Lane 0	3, Link3, 50 Lane1	3, Link 3,	f. Link3, 2 Lane3
RSVD	RSVD	RSVD	000010	1 Host	1 Upstream Socket	1, 2, or 4 Links	00090																
RSVD	RSVD RSVD	RSVD	000001	1 Host		1, 2, or 4 Links	00090																
RSVD	RSVD RSVD	RSVD	000090	1Host	1 Upstream Socket	1, 2, or 4 Links	00090																



Table 24: Bifurcation for Single Host, Dual Upstream Sockets and Dual Upstream Links (BIF[2:0]#=0b001)

				-																			
Single He	oct. Two Upstre	Single Host, Two Upstream Sockets, Two Upstream Links	5		2 x8. 2 x4. 2 x2. 2x1																		
Í		Supported Bifurcation	Add-in-Card				RIFE2-01					-	-	_		L	L						
Card Vidt	Card Card Short Modes	Modes	Encoding PRSNTB(3:0)#	Host	Upstream Devices	Upstream		Reculting link Lanc 0 Lanc 1 Lanc 2 Lanc 3 Lanc 4 Lanc 5 Lanc 6 Lanc 7 Lanc 8 Lanc 10 Lanc 12 Lanc 13 Lanc 14 Lanc 15	1386	13061	38¢ 2	300 3	4 94	22	150	- 1 - 1 - 1	6.8	e 3	10 Lane	TI Lane	I2 Lane 1	Lane	1
epu	Not Present	Card Not Present	0b1111	1 Host	2 Upstream Sockets	2 Links	00001																
ç	9	1x8,1x4,1x2,1x1	0b1 110	1 Host	2 Upstream Sockets	2 Links	10090	1x8	Link 0,	Link 0,	Link 0,	Link O, L	Link O, Li	Link O, Lin	Link O, Link	Link 0,							
3	ox-	1x4, 1x2, 1x1	061110	1 Host	2 Upstream Sockets	2 Links	00001		Link 0,	+	+	-	-	-	-							L	ļ
S	1×4						10000	(Socket 0 only)	Lone 0	-	Lane 2	Lone 3											
30	1x2	1x2,1x1	0b1 110	1 Host	2 Upstream Sockets	2 Links	00001	1x2 (Socket 0 only)	Link O, Lane O	Link 0, Lane 1													
30	1×1	1x1	0b1 110	1 Host	2 Upstream Sockets	2 Links	00001	1x1 (Socket 0 only)	Link 0, Lane 0														
ပ္လ	1x8 Option B	1x8,1x4,1x2,1x1 1x8 Option B 2x4,2x2,2x1	0b1101	1 Host	2 Upstream Sockets	2 Links	10090	1x8 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O, L Lane 3 L	Link O, Li	Link O, Lin Lanc 5 La	Link O, Link Lanc 6 Lan	Link O, Lane 7							
Q.	2 x8 Option B	2 x 8, 2 x 4, 2 x 2, 2 x 1 2 x 8 Option B 4 x 4, 4 x 2, 4 x 1	0b1101	1 Host	2 Upstream Sockets	2 Links	009001		Link 0,	-	-	-	-	-	-	\vdash	Link 1, Link 1, Lane 0 Lane 1	ct, Linkt,	1, Link1,	1, Link 1,	Link 1,	Link 1,	Link 1,
		1x8,1x4	0b1100	1 Host	2 Upstream Sockets	2 Links		1x8	Link 0,	+	Н	+	н	н	н	Н	Н	Н	Н	Н	Н	Н	+
S	1x8 Option D	2 x 4, 1 x 8 Option D 4 x 2 (First 8 lanes), 4 x 1					00000	(Socket 0 only)	Lane 0	Lane 1	Lane 2	Lane 3 L	Lane 4 L	_	Lanc 6 Lan	Lane 7							
		1x16,1x8,1x4	061 100	1 Host	2 Upstream Sockets	2 Links		2 x8	Link 0,	Link 0,	⊢	⊢	⊢	⊢	⊢	Н	⊢	Н	⊢	1, Link 1,	Н	⊢	Link 1,
û	1x16 Option D	1x16 Option D 4x4, 4x2 (First 8 lanes), 4x1					00001		Lane 0	Lane 1	Lane 2	Lane 3 L	Lane 4 L	Lane 5 La	Lanc 6 Lan	Lane 7 Lan	Lane 0 Lane 1	e1 Lane 2	2 Lane 3	3 Lane 4	t Lane 5	Lane 6	
٥	RSVD	RSVD	0b1 011	1 Host	2 Upstream Sockets	2 Links	00001																
ç	77.0	2 x4, 2 x2, 2 x1 1 x4 1 x2 1 x1	061010	1 Host	2 Upstream Sockets	2 Links	10090	1x4 (Socker Deale)	Link 0,	Link 0,	Link 0,	Link 0,											
ę	750	DOVD for future v8 according	081001	1 Hoer	2 Hestram Cockete	Olisho	00001	۰		۰	۰		-	-		-	1	+	ł	+	+	ļ	ļ
RSVD RSVD	RSVD	RSVD for future x8 encoding	061000	1 Host	2 Upstream Sockets	2 Links	00001											+		+		L	
ç	97.7	1x16,1x8,1x4,1x2,1x1	050111	1Host	2 Upstream Sockets	2 Links	10090	1x8	Link 0,	Link 0,	Link O,	Link O, Li	Link O, Li	Link O, Lin	Link O, Link	Link 0,							
3		2 x8, 2 x4, 2 x2, 2 x1	000110	1 Host	2 Upstream Sockets	2 Links	00001	2 x8	Link 0,	+	₩	-	+	+	-	Н	Н	+	\vdash	\vdash	Н	-	-
ပ္	2 x8 Option A	-							Lane 0	+	+	+	+	+	+	+	+	+	+	+	+	+	+
Q.	1x16 Option B	1x16 Option B 2x8, 2x4, 2x2, 2x1	101010	1 Host	2 Upstream Sockets	2 Links	00001	2 x 8	Link 0.	Lane 1	Link 0, Lane 2	Link O, L	Link O, Li	Link O, Lin Lane 5 La		Link O, Link Lane 7 Lan	Link 1, Link Lanc 0 Lan	Link 1, Link 1, Lane 1 Lane 2	1, Link1,	1, Link1, 3 Lane 4	Link1,	Link 1, Lanc 6	Link 1, Lane 7
		1x16,1x8,1x4	0001000	1 Host	2 Upstream Sockets	2 Links	00000	2 x8	Link O,	Link 0,	Link 0,	Link O, L	Link O, Li	Link O, Lin	Link O, Link	Link 0, Link 1,	Link 1, Link 1,	ct, Linkt,	of Link t	1 Link1,	Link 1,	Link 1,	Link 1,
Ç	1x16 Option C	1x16 Option C 4x4, 4x2, 4x1					10000							_					_			_	_
ĵ,	7 × 7	4x4,4x2,4x1	060 011	1 Host	2 Upstream Sockets	2 Links	10090	2 x4 (EP 0 and 2 only)	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3				Lin	Link 2, Link 2, Lane 0 Lane 1	(2, Link2,	2, Link2,	പ്ര			
RSVD RSVD	RSVD	RSVD	000010	1 Host	2 Upstream Sockets	2 Links	00001	Н		Н	Н												
RSVD RSVD	RSVD	RSVD	000 001	1 Host	2 Upstream Sockets	2 Links	00001																
RSVD RSVD	RSVD	RSVD	000000	1 Host	2 Upstream Sockets	2 Links	00001		ĺ											_			

Table 25: Bifurcation for Single Host, Four Upstream Sockets and Dual Upstream Links
(BIF[2:0]#=0b010)

ingle nos	t, Four Upstre	Single Host, Four Upstream Sockets, Four Upstream Links	93		4 x4, 4 x2, 4x1																		
Mis Card Card: Vidth Name	Card Short Modes	Supported Bifurcation Add-in-Card Modes Encoding PRSNTBI3:01#	Add-in-Card Encoding PRSMTB[3:0]#	Host	Upstream Devices	Upstream	BIF[2:0]	Reculting Link Lane 0 Lane 2 Lane 3 Lane 4 Lane 5 Lane 6 Lane 8 Lane 9 Lane 10 Lane 17 Lane 13 Lane 14 Lane 15	Lane 0	Lage 1	Lane 2	Lane 3	2 4 au	ane 5		7 12	8 6 6 15	6 9	6 to	11 1386	12 Lane	3 Lane	1
N c/u	Not Present	Card Not Present	0b1111	1 Host	4 Upstream Sockets	4 Links	05010																
	,	1x8,1x4,1x2,1x1	0b1 110	1 Host	4 Upstream Sockets	4 Links	00010	1x4	Link O,	Link 0,	Link 0,	Link 0,											
2	1×6							(Socket U only)	Couc O	Lanel	Z oue Z	Lane 3			+	+	+	+	+	+	+	1	1
30	1×4	1x4,1x2,1x1	001110	1 Hoot	4 Upstream Sockets	4 Links	05010	1x4 (Socket 0 only)	Lane 0	Link U.	Lane 2	Lane 3											
3C	1x2	1x2,1x1	051110	1 Host	4 Upstream Sockets	4 Links	01040	1x2 (Socket 0 only)	Link 0, Lane 0	Link 0, Lane 1													
20	1×1	1x1	061110	1 Host	4 Upstream Sockets	4 Links	01040	1x1 (Socket 0 only)	Link 0, Lane 0														
20	x8 Option B	1x8,1x4,1x2,1x1 1x8 Option B 2x4,2x2,2x1	061101	1 Host	4 Upstream Sockets	4 Links	01040	2 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, L	Link 1, Li Lane 1 La	Link 1, Li Lane 2 L:	Link 1, Lane 3							
4C	x8 Option B	2 x 8, 2 x 4, 2 x 2, 2 x 1 2 x 8 Option B 4 x 4, 4 x 2, 4 x 1	0b1 101	1 Host	4 Upstream Sockets	4 Links	01040	\$x \$	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link O,	Link 1, L	Link 1, Li Lane 1 La	Link 1, Li Lane 2 L:	Link 1, Lir Lane 3 La	Link 2, Lin Lane 0 La	Link 2, Lin Lane 1 Lan	Link 2, Link 2, Lane 2 Lane 3	.2, Link3, s3 Lane 0	3, Link 3, 0 Lane 1	Link3, Lane2	Link 3, Lane 3
2	x8 Option D	1x8,1x4 2x4, 1x8 Option D 4x2 (First 8 lanes), 4x1	061 100	1 Host	4 Upstream Sockets	4 Links	01040	2 x4	Link 0, Lane 0	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, L	Link 1, Li Lane 1 La	Link 1, Li Lane 2 Lr	Link 1, Lane 3							
5	x16 Option D	1x16,1x6,1x4 2x8,2x4, 1x16 Option D 4x4,4x2 (First 8 lance),4x1	061 100	1 Host	4 Upstream Sockets	4 Links	01040	4 x 4	Link 0, Lane 0	Link 0, Lane 1	Link O, Lane 2	Link O, Lane 3	Link 1, L	Link 1, Li Lane 1 La	Link 1, Li Lane 2 Le	Link 1, Lir Lane 3 La	Link 2, Lin Lane 0 La	Link 2, Lin Lane 1 Lan	Link 2, Link 2, Lane 2 Lane 3	2, Link3, c3 Lane 0	3, Link 3, 0 Lane 1	Link3, I Lane 2	Link 3, Lane 3
RSVD RSVD	SVD	RSVD	0b1 011	1 Host	4 Upstream Sockets	4 Links	05010																
200	2 x4	2x4,2x2,2x1 1x4,1x2,1x1	051 010	1 Host	4 Upstream Sockets	4 Links	01040	2 x4	Link O, Lane O	Link 0, Lane 1	Link 0, Lane 2	Link 0, Lane 3	Link 1, L	Link 1, Li Lane 1 La	Link 1, Li Lane 2 L:	Link 1, Lane 3							
RSVD R	RSVD	RSVD for future x8 encoding	0b1 001	1 Host	4 Upstream Sockets	4 Links	05010																
RSVD RSVD	SVD	1x16.1x8.1x4.1x2.1x1	0b1000	1 Host	4 Upstream Sockets	4 Links	05010	1x4	Link O.	Link 0.	Link 0.	Link O.		-	\dagger	\dagger	\dagger	+	+	+	+	1	1
4c	1×16						05010	(Socket 0 only)	Lane 0	Lane 1	Lane 2	Lane 3											
40 2	2 x8 Option A	_	000110	1 Host	4 Upstream Sockets	4 Links	01000	2 x4 (Socket 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1	Link O, Lane 2	Link O, Lane 3				Li.		Link 2, Lin Lone 1 Lon	Link 2, Link 2, Lane 2 Lane 3	. S. S.			
4C 1	x16 Option B	1x16.1x8,1x4,1x2,1x1 1x16.0ption B 2x8,2x4,2x2,2x1	000101	1 Host	4 Upstream Sockets	4 Links	01000	2 x4 (Socket 0 & 2 only)	Link 0, Lane 0	Link 0, Lane 1	Link O, Lane 2	Link O, Lane 3				Li.		Link 2, Lin Lone 1 Lon	Link 2, Link 2, Lone 2 Lone 3				
40	x16 Option C	1x16,1x8,1x4 2x8,2x4,2x2,2x1 1x16 Option C 4x4,4x2,4x1	000100	1 Host	4 Upstream Sockets	4 Links	01040	4×4	Link O, Lane O	Link 0, Lane 1	Link O, Lane 2	Link 0, Lane 3	Link 1, L	Link 1, Li	Link 1, Li Lane 2 L:	Link 1, Lir Lane 3 La	Link 2, Lin Lane 0 La	Link 2, Lin Lane 1 Lan	Link 2, Link 2, Lane 2 Lane 3	Link 2, Link 3, Lane 3 Lane 0	3, Link 3, 0 Lane 1	Link3,	Link 3, Lane 3
40	×4	x2,4x1	000011	1 Host	4 Upstream Sockets	4 Links	01040	4×4	Link 0, Lane 0	Link 0, Lane 1	Link O, Lane 2	Link O,	Link 1, L	Link 1, Li Lone 1 Lo	Link 1, Li Lone 2 Lt	Link 1, Lir Lane 3 La	Link 2, Lin Lane 0 La	Link 2, Lin Lone 1 Lon	Link 2, Link Lone 2 Lon	Link 2, Link 3, Lane 3 Lane 0	3, Link 3, 0 Lane 1	Link 3, Lane 2	Link 3, Lane 3
RSVD RSVD		RSVD	000000	1 Host	4 Upstream Sockets	4 Links	05010																
RSVD RSVD			000001	1 Host	_	4 Links	05010																
RSVD RSVD	SAVD	RSVD	000000	1 Host	4 Upstream Sockets	4 Links	00010																



Table 26: Bifurcation for Dual Host, Dual Upstream Sockets and Dual Upstream Links (BIF[2:0]#=0b101)

Mile	F(3:0)#																				
No Precent Card Not Precent 1186 184, 142, 141 114 142, 141 114 142, 141 115 Debiso B 214, 22, 141 116 Debiso B 214, 22, 241 117 Debiso B 214, 22, 241 118 214, 142, 141 118 214, 142, 141 118 214, 142, 141 118 214, 142, 141 118 214, 142, 141 118 214, 142, 141 118 214, 142, 141 218 218 218, 22, 241 218 218 218, 24, 22, 241 218 218 218, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24		Host U	Upstream Devices	Upstream B	BIF[2:0]	Resulting Link Lane 2 Lane 3 Lane 4 Lane 5 Lane 6 Lane 9 Lane 10 Lane 12 Lane 13 Lane 14 Lane 15	0 9 4	1986	2 Pe 2			5 5	. 6 Lane	- Lane	8 Lane) Lane 1	0 Lane 11	Lane 12	Lane 13	Lane 14	Lane 15
185 145, 145, 141 194 14, 142, 141 195 140 197 141 198 0ption B 244, 242, 241 198 0ption B 44, 242, 441 198 0ption B 44, 242, 141 198 141 198 141 198 141 198 141 198 141 198 142, 141 198 142, 141 198 144, 124, 144, 122, 141 198 144, 124, 144, 122, 141 198 144, 124, 144, 122, 141 198 144, 144, 142, 144 198 144, 144, 142, 144 198 144, 144, 142, 144 198 144, 144, 142, 144 198 144, 144, 142, 144 198 144, 144, 142, 144 198 144, 144, 142, 144 198 144, 144, 144, 142, 144 198 144, 144, 142, 144 198 144, 144, 142, 144 198 144, 144, 142, 144 198 144, 144, 144, 144, 144, 144, 144, 144			2 Upotream Sockets	2 Links	05101																
134 144, 132, 131 132 141 133 144 12, 131 134 145, 132, 131 135 0ption B 244, 252, 231 2 35 0ption B 44, 452, 431 135 0ption B 44, 452, 131 135 0ption B 44, 452, 131 135 0ption B 135, 135, 132, 131 135 135 135, 135, 135, 135, 131 135 135 135, 135, 135, 131 135 135 135, 135, 135, 131 135 135 135, 135, 135, 131 135 135 135, 135, 135, 131 135 135 135, 135, 135, 131 135 135 135, 135, 135, 131 135 135 135, 135, 135, 131 135 135 135, 135, 135, 131 135 135 135, 135, 135, 131 135 135 135, 135, 135, 131 135 135 135, 135, 135, 131 135 135 135, 135, 135, 131 135 135 135, 135, 135, 131 135 135 135, 135, 135, 131 135 135 135, 135, 135, 131 135 135 135, 135, 135, 135, 135, 135, 13			2 Upstream Sockets	2 Links	10140	1x8 L	Link 0, 1	Link O, Li	Link O, Lin Lane 2 La	Link O, Lin Lane 3 Lar	Link O, Link Lanc 4 Lan	Link 0, Link 0, Lane 5 Lane 6	.0, Link 0, a 6 Lane 7	o' ~							
142, 141 151 151 151 152 153 154 155 155 155 155 155 155		2 Host 2	2 Upstream Sockets	2 Links	06101		-	-	-												
141 142 141 143 144 142 141 143 144 142 141 143 144 142 141 143 144 142 141 143 144 143		2 Host 2	2 Upstream Sockets	2 Links	10140	1x2 L (Host 0 only)	Link O, I	Link 0, Lane 1													
145 Option B 244 22 2 11 2 2 0 Option B 244 22 2 11 2 2 0 Option B 244 22 2 11 2 2 0 Option B 244 22 2 14 115 Option D 242 [First 8 bees], 411 115 Option D 242 [First 8 bees], 411 115 Option D 242 [First 8 bees], 411 115 Option D 244 22 [First 8 bees], 411 115 Option D 242 [First 8 bees], 411 115 Option D 242 [First 8 bees], 411 115 Option D 244 22 [First 8 bees], 411 115 Option D 252 [First 8 bees], 412 [First 8 bees], 412 115 Option D 252 [First 8 bees], 412 [First 8 bees], 412 115 Option D 252 [First 8 bees], 412 115 Opt			2 Upstream Sockets	2 Links	06101	1x1 L (Host 0 only) L	Link 0, Lane 0														
2.05 Opioio B 4.04.22.2.1 2.05 Opioio B 4.04.22.2.1 3.05 Opioio B 4.04.02.4.1 3.05 Opioio B 4.05 (First 8 base), 4.31 3.05 Opioio B 4.05 (First 8 base), 4.31 5.05 Opioio B 5.05 (First 8 base), 4.31 5.05 Opioio B 5.05 (First 8 base), 4.31 5.05 Opioio B 5.05 (First 8 base) 5.05 C 4.05 C 4.05 C 2.31 5.05 Opioio B 5.05 (First 8 base) 5.05 C 4.05 C 2.21 5.05 Opioio B 5.05 (First 8 base) 5.05 C 4.05 C 2.21 5.05 Opioio B 5.05 (First 8 base) 5.05 C 4.05 C 2.21 5.05 Opioio B 5.05 C 2.22 5.05 C 4.05 C 2.21 5.05 C 4.05 C 2.21		2 Host 2	2 Upstream Sockets	2 Links	10140	1x8 L	Link 0, 1 Lanc 0	Link O, Li Lane 1 L:	Link O, Lin Lane 2 La	Link O, Lin Lane 3 Lar	Link O, Link Lanc 4 Lan	Link 0, Link 0, Lane 5 Lane 6	.0, LinkO,	o							
165 165	061101 2	2 Host 2	2 Upstream Sockets	2 Links	10140	2x8	Link O, 1 Lane O	Link O, Li Lane 1 L:	Link O, Lin Lane 2 La	Link O, Lin Lane 3 Lar	Link O, Link Lane 4 Lan	Link 0, Link 0, Lane 5 Lane 6	.0, Link 0, s 6 Lane 7	0, Link 1, 7 Lane 0	Link 1,	Link 1,	Link 1,	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
146 Option 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		2 Host	2 Upotresm Sockets	2 Links	06101	1x8 (Host 0 only)	Link 0, 1 Lane 0	Link O, Li Lane 1 L;	Link O, Lin Lane 2 La	Link O, Lin Lane 3 Lar	Link O, Link Lanc 4 Lan	Link O, Link O, Lane 5 Lane 6	0, Link 0, s 6 Lane 7	o							
RSVD RSVD	061100	2 Hoot	2 Upotresm Sockets	2 Links	06101	2 x8	Link 0, 1 Lane 0	Link O, Li Lane 1 L;	Link O, Lin Lane 2 La	Link O, Lin Lane 3 Lar	Link O, Link Lane 4 Lan	Link O, Link O, Lane 5 Lane 6	0, Link 0, s 6 Lane 7	0, Link 1, 7 Lane 0	Link 1, D Lane 1	Lane 2	Link 1,	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
2.44 2.42.2.2.1		2 Hoot 2	2 Upstream Sockets	2 Links	06101																
Description	061010		2 Upstream Sockets	2 Links	10140	1x4 L (Host 0 only)	Link O, 1 Lane O	Link O, Li Lane 1 L:	Link O, Lin Lane 2 La	Link O, Lane 3											
2 ± 6 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		2 Host 2	2 Upstream Sockets	2 Links	06101								1								
2.00 Option A 2.00 2.04 2.02 2.11 1.00 Option B 2.00 2.04 2.02 2.11 1.00 Option B 2.00 2.00 2.01 1.00 Option C 4.04 4.2 2.02 2.11		-	2 Upstream Sockets	2 Links	10140	1x8 (Host Dealu)	Link 0, 1	Link O, Li	Link O, Lin	Link 0, Lin	Link O, Link	Link O, Link O,	O. Link O.	c: 10							
1x16 Option B 2x8, 2x4, 1x2, 1x1 1x16 Option B 2x8, 2x4, 2x2, 2x1 1x16, 1x6, 1x4 2x6, 2x4, 2x2, 2x1 1x16 Option C 4x4, 4x2, 4x1	000110	2 Host 2	2 Upstream Sockets	2 Links	10140		-	-	-	-	-	-	-	0, Link 1, 7 Lane 0	Link 1,	Link 1,	Link 1,	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
1x16,1x6,1x4 2x8,2x4,2x2,2x1 1x16 Option C 4x4, 4x2,4x1	060101	2 Host 2	2 Upstream Sockets	2 Links	10140	2x8	Link O, 1 Lane O	Link O, Li Lane 1 L:	Link O, Lin Lane 2 La	Link O, Lin Lane 3 Lar	Link O, Link Lane 4 Lan	Link 0, Link 0, Lane 5 Lane 6	.0, Link 0, s 6 Lane 7	0, Link 1, 7 Lane 0	Link 1,	Link 1,	Link 1,	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
	0001000	2 Host 2	2 Upstream Sockets	2 Links	06101	2 x8	Link 0, 1 Lane 0	Link O, Li Lane 1 L:	Link O, Lin Lane 2 La	Link O, Lin Lane 3 Lar	Link O, Link Lanc 4 Lan	Link O, Link O, Lane 5 Lane 6	o, Linko, o 6 Lane 7	0, Link 1, 7 Lane 0	Link 1,	Link 1,	Link 1,	Link 1, Lane 4	Link 1, Lane 5	Link 1, Lane 6	Link 1, Lane 7
4 x4, 4 x2, 4 x1			2 Upstream Sockets	2 Links		EP 0 and 2 only) L	Link O, I	Link O, Li Lane 1 L:	Link O, Lin Lane 2 La	Link O, Lane 3				Link 1, Lane 0	Link 1, D Lane 1	Link 1,	Link 1,				
RSVD RSVD RSVD 0b0016	000010 2	2 Hoot 2	2 Upstream Sockets	2 Links	06101																
BSVD			2 Unstream Sockets	2 Links	08101																

Table 27: Bifurcation for Quad Host, Quad Upstream Sockets and Quad Upstream Links (BIF[2:0]#=0b110)



Table 28: Bifurcation for Quad Host, Quad Upstream Sockets and Quad Upstream Links (BIF[2:0]#=0b110)

O/peng	ct Host, FourlEig	Quad/Oct Host, Four/Eight Upstream Sockets, Four/Eight Upstream links	ht Upstream links		4 x2, 4 x1																		
Card Mi	Min Suppor Card Card Short Modes Vidth Name	Supported Bifurcation Add-in-Card Modes Encoding PRSMTBI3:01#	Add-in-Card Encoding PRSMTBf3:01#	Host	Unetresa Devices	Upstream	BIF[2:0]	Receiting tak lane 0 lane 1 lane 2 lane 3 lane 5 lane 6 lane 7 lane 8 lane 3 lane 11 lane 12 lane 13 lane 14 lane 15	0 246	1	2 346	300	7	2 2 2 2	9			- 6	10	1	1 346 1	1	-
cla	Not Present	Card Not Present	-	478 Host	478 Upstream Sockets	4 or 8 x2 Links	0b111																
é	9,1	1x8,1x4,1x2,1x1	061110	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	4 or 8 x2 Links	06111	1x2 (Host 0 only)	Link 0, Lane 0	Link 0,													
S	1×1	1x4,1x2,1x1	061110	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	4 or 8 x2 Links	0b111	1x2 (Host 0 only)	Link 0,	Link 0,													
N N	1x2	1x2,1x1	061110	478 Host	Host 4/8 Upstresm Sockets 4 or 8 x2 Links	4 or 8 x2 Links	06111	1x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1													
S,	1×1	1x1	061110	478 Host	478 Upstream Sockets	4 or 8 x2 Links	06111	tx1 (Host 0 only)	Link 0, Lane 0														
o _N	1x8 Option B	1x8.1x4,1x2,1x1 1x8.0ption B 2x4,2x2,2x1	0b1 101	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	4 or 8 x2 Links	06111	2 x2 (Host 0 & 1 only)	Link 0, Lane 0	Link 0, Lane 1	Link 1, Lane 0	Link 1, Lane 1											
å	2 x8 Option B	2 x 8, 2 x 4, 2 x 2, 2 x 1 2 x 8 Option B 4 x 4, 4 x 2, 4 x 1	0b1 101	478 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	4 or 8 x2 Links	06111	2 x2 (Hoxt 0 & 1 only)	Link 0, Lane 0		Link 1, Lane 0	Link 1, Lane 1											
8		1x8,1x4 2x4,	0P1100	4/8 Host	Host 4/8 Upstream Sockets 4 or 8 x2 Links	4 or 8 x2 Links	Ob##	4 x2	Link 0, Lane 0	Link 0, Lane 1	Link 1, Lane 0	Link 1, L	Link 2, L Lane 0 L	Link 2, Lii Lane 1 La	Link 3, Lin Lane 0 La	Link 3, Lane 1							
ા	nondo ox i	1x16,1x8,1x4	061100	4/8 Host	Host 4/8 Upstream Sockets 4 or 8 x2 Links	4 or 8 x2 Links		4 x2	Link O,	+	Link 1,	+	+	+	+	Link 3,	+	+	H	-	L	L	
Ş	1x16 Option D	1x16 Option D 4x4, 4x2 (First 8 lanes), 4x1					E g		Lane U	Lane 1	Cane O	Lanel	Lane U	Lane 1	Lane U	Lone 1				_			
RSVD	RSVD RSVD	RSVD		478 Host	478 Upstream Sockets	4 or 8 x2 Links	0b111																
S	2 x4	2 x4, 2 x2, 2 x1 1 x4, 1 x2, 1 x1	051 010	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	4 or 8 x2 Links	06111	2 x2 (Host 0 & 1 only)	Link 0, Lane 0	Link 0, Lane 1	Link 1, Lane 0	Link 1, Lane 1											
RSVD	RSVD	RSVD for future x8 encoding	0b1 001	478 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	4 or 8 x2 Links	06111																
RSVD	RSVD RSVD	RSVD for future x8 encoding	0P1 000	4/8 Host	478 Upstream Sockets	4 or 8 x2 Links	06111										+						
Q.	1x16	1x16, 1x8, 1x4, 1x2, 1x1	050111	478 Host	4/8 Upstream Sockets	4 or 8 x2 Links	06111	1x2 (Host 0 only)	Link 0, Lane 0	Link 0, Lane 1													
ů,	2 x8 Option A	2x6,2x4,2x2,2x1	0P0 110	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	4 or 8 x2 Links	06111	1x2 (Host 0 & 1 only)	Link 0, Lane 0	Link 0, Lane 1						Lin La	Link 1, Lir Lane 0 La	Link 1, Lane 1					
ដ្	1x16 Option B	1x16,1x8,1x4,1x2,1x1 1x16 Option B 2x8,2x4,2x2,2x1	0b0 101	4/8 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	4 or 8 x2 Links	06111	2 x2 (Host 0 & 1 only)	Link 0, Lane 0	Link 0, Lane 1						ri La	Link 1, Lin Lane 0 La	Link 1, Lane 1					
û	1x16 Option C	1x16,1x8,1x4 2x8,2x4,2x2,2x1 1x16 Option C 4x4,4x2,4x1	0001000	4/8 Host	Host 4/8 Upetresm Sockets 4 or 8 x2 Links	4 or 8 x2 Links	0b111	2 x 2 (Host 0 & 1 only)	Link 0, Lane 0	Link 0, Lane 1						Lin	Link 2, Lin Lane 0 La	Link 2, Lane 1					
û	4 x4	4x4,4x2,4x1	060011	4/8 Host	Host 4/8 Upstream Sockets 4 or 8 x2 Links	4 or 8 x2 Links	06111	4 x2 (Host 0 & 1 only)	Link 0, Lane 0	Link 0, Lane 1			Link 1, L	Link 1, Lane 1									
RSVD	RSVD			478 Host	4/8 Host 4/8 Upstream Sockets 4 or 8 x2 Links	4 or 8 x2 Links	0b111																
RSVD RSVD	RSVD	RSVD	000 001	478 Host	478 Upstream Sockets	4 or 8 x2 Links	05111																
RSVD	RSVD			4/8 Host	478 Upstream Sockets	4 or 8 x2 Links	0b111									_	_						

3.9 Power Capacity and Power Delivery

There are four permissible power states: AC Power Off, Management (FRU Only Mode), Aux Power Mode (S5), and Main Power Mode (S0). The transition of these states is shown in Figure 29. The main/aux power domains are switched on the baseboard and uses the power pins defined in Table 11. For each of these states, the max power envelopes are defined as follows:

Table 29: Power Envelopes

Power State	Max Power	Notes
AC Power Off	0W	AC power removed; board off
Management (FRU only mode)	TBD	Used only for board identification
		purposes.
Aux Power Mode (S5)	35W	
Main Power Mode (S0)	79.2W	Add-in card may use up to the 79.2W
		limit per connector.

PWR_DIS=0 AC Power On PERST# = 1 MAIN (SO) **MGMT** AUX (S5) AC Power Off 3.3V ON ON AUX AUX AUX ON but ON but can only 12V cannot 12V use up to be used AUX WAKE/NC-SI System Power-Down

Figure 29: Baseboard Power Sequencing

3.9.1 AC Power Off

In AC power off mode, all power delivery has been turned off or disconnected from the baseboard.

3.9.2 Management (FRU Only Mode)



In the Management (FRU Only Mode), only +3.3V Aux is available for powering up management only functions. FRU accesses are only allowed in this mode.

3.9.3 Aux Power Mode (S5)

In Aux Power Mode provides both +3.3V Aux as well as +12V Aux is available. +12V Aux may be used to deliver power to the add-in card, but only up to the Aux budget of 35W.

3.9.4 Main Power Mode (S0)

In Main Power Mode provides both +3.3V and +12V (Main) across the OCP connector. The add-in card operates in full capacity. Up to 79.2W may be delivered on +12V, and 3.63W on the +3.3V pins.

3.10 Power Sequence Timing Requirements

The following figure shows the power sequence of 3.3V/3.3V_AUX, 12VMain/Aux relative to PWRDIS, PERSTn* and NIC_PWR_GOOD.

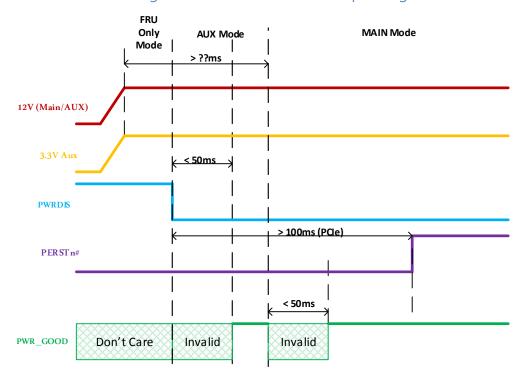


Figure 30: Baseboard Power Sequencing

Table 30: Power Sequencing Parameters

Parameter	Value	Units	Description
Name			

4 Management

4.1 SMBus Interface

The SMBus provides manageability of the add-in card.

4.2 NC-SI Sideband Interface

4.2.1 NC-SI addressing and Arb#

4.3 MAC Address Requirement

4.4 FRU EEPROM

4.4.1 Addressing(TBD)

4.5 FW Requirement (TBD)

4.6 Thermal Reporting Interface



5 Data Network Requirement

5.1 Network Booting (collect view from OEMs and hyperscale)

Mezzanine NIC shall support network booting in uEFI system environment. Mezzanine NIC shall support both IPv4 and IPv6 network booting.

6 Routing Guidelines and Signal Integrity Considerations

6.1 NC-SI Over RBT

Min Length: 2" Max length: 4"

Impedance: 50 Ohm single ended

7 Thermal and Environmental

7.1 Environmental Requirements

The specific environment requirement is removed to allow the adoption of OCP Mezzanine NIC in systems with very different thermal requirement and boundary condition.

This Mezzanine card shall meet the same environmental requirements specified in the OCP systems that the Mezzanine card is in. The OCP system that uses OCP Mezzanine card shall define air flow direction, inlet air temperature, air flow (or speed) to the local area where Mezzanine card is at, and simulation boundary.

7.1.1 Thermal Simulation Boundary Example

Placeholder for Thermal Simulation Method. Using Facebook Intel® Motherboard V3.0 as example. Not covered by this update.

7.2 Shock & Vibration

This Mezzanine card shall meet the same shock & vibration requirements specified in updated Facebook OCP Intel® Motherboard V2.0 and V3.0 Design Specification.

7.3 Regulation

This Mezzanine card shall meet CE, CB, FCC Class A, WEEE, ROHS requirements.



8 Revision History

Author	Description	Revision	Date
Thomas Ng	Initial draft	0.1	12/xx/2017