

OCP NIC 3.0 Design Specification

**Version 0.01**

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# Overview

## License

As of April 7, 2011, the following persons or entities have made this Specification available under the Open Web Foundation Final Specification Agreement (OWFa 1.0), which is available at <http://www.openwebfoundation.org/legal/the-owf-1-0-agreements/owfa-1-0>:

Facebook, Inc.

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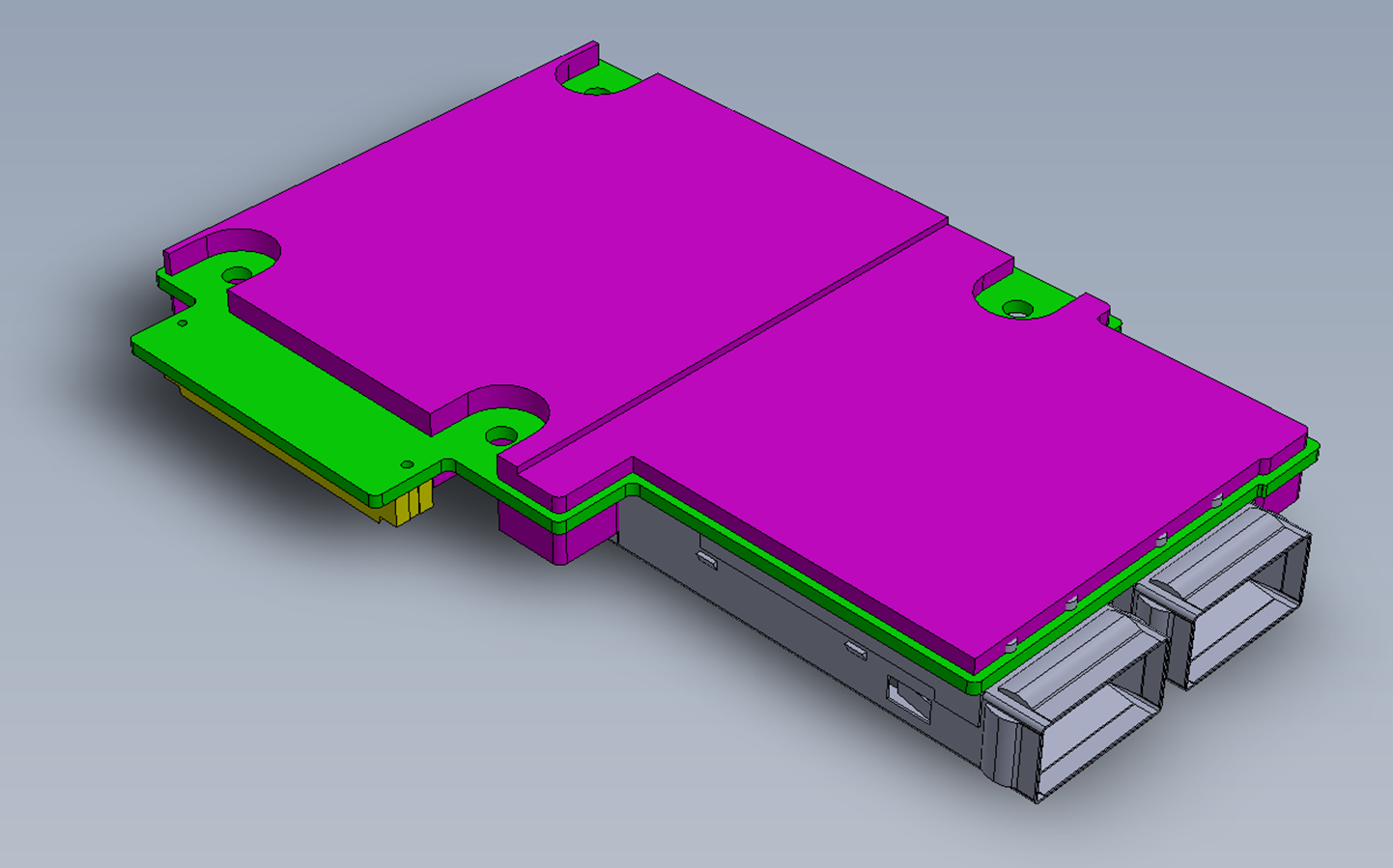
## Background

The OCP Mezzanine Card v0.5 and v2.0 specifications were created in 2012 and 2015 to standardize low profile PCIe NIC modules. These specifications are publically available and can be found at:

http://www.opencompute.org/wiki/Server/Mezz#Specifications\_and\_Designs

Compared to a NIC in in the standard PCIe CEM form factor, an OCP 2.0 Mezzanine is generally smaller in size with additional signals for NIC management, and support for multi-host use cases.

Figure 1: A Representative OCP 2.0 Mezzanine Card With Dual QSFP Ports



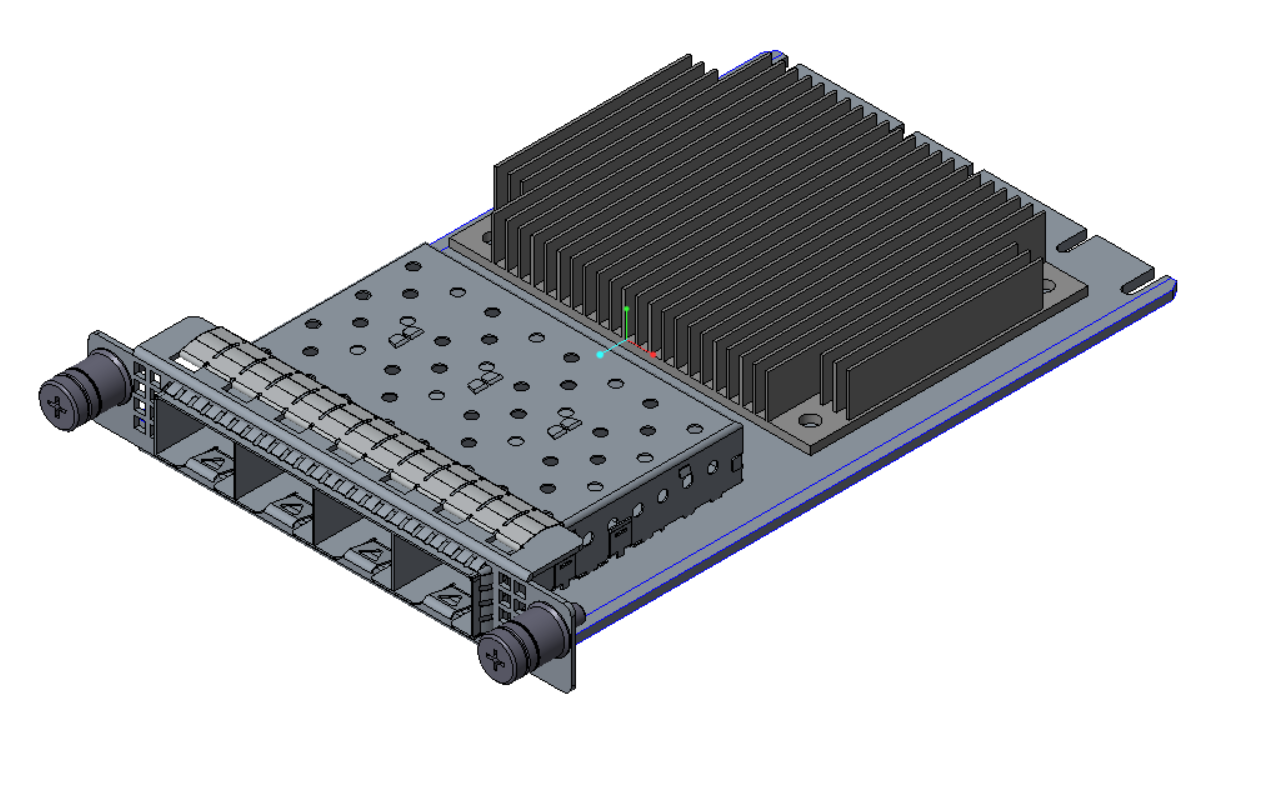
In the 2016 and 2017 OCP Summit, there was a healthy adoption of the OCP Mezzanine Card 2.0 form factor from both NIC and system suppliers. With this broader adoption, the OCP community raised the request to refresh the specification to support new and broader use cases, such as:

* Support NICs with Higher TDP
* Support for PCIe Gen4/5
* Support for more than x16 lanes of PCIe per card
* Support for Smart NIC implementations with on-board DRAM
* Support for greater board area for more complex add-in card designs
* Simplification of FRU installation and removal while reducing overall down time

The OCP NIC 3.0 specification aims to support these use cases. This specification was created under OCP Server workgroup - OCP NIC subgroup.

A representative OCP 3.0 NIC mezzanine card is shown in Figure 2.

Figure 2: A Representative OCP 3.0 NIC Mezzanine Card with Quad SFP Ports



OCP 3.0 compliant cards are not backwards compatible to the 2.0 form-factor. Backward compatibility was considered during the specification process. However, after evaluating 14 major design concepts, the NIC and system suppliers converged on not supporting backward compatibility in order to achieve better features in this specification.

## Acknowledgement

Placeholder

## Overview

### Form factor overview

### Electrical overview

## References

DMTF Standard. *DSP0222, Network Controller Sideband Interface (NC-SI) Specification.* Distributed Management Task Force, Inc, Rev 1.0.1, January 24th, 2013.

Open Compute Project. *OCP NIC Subgroup*. Online. <http://www.opencompute.org/wiki/Server/Mezz>

PCIe Base Specification. *PCI Express Base Specification, Revision 4.0 (draft)*.

PCIE CEM Specification. *PCI Express Card Electromechanical Specification, Revision 4.0 (draft)*.

SMBus specification

SNIA. *SFF-TA-1002, Specification for Protocol Agnostic Multi-Lane High Speed Connector*. SNIA SFF TWG Technology Affiliate, Rev 0.0.9.1, September 9th, 2017.

# Card form factor

## Overview

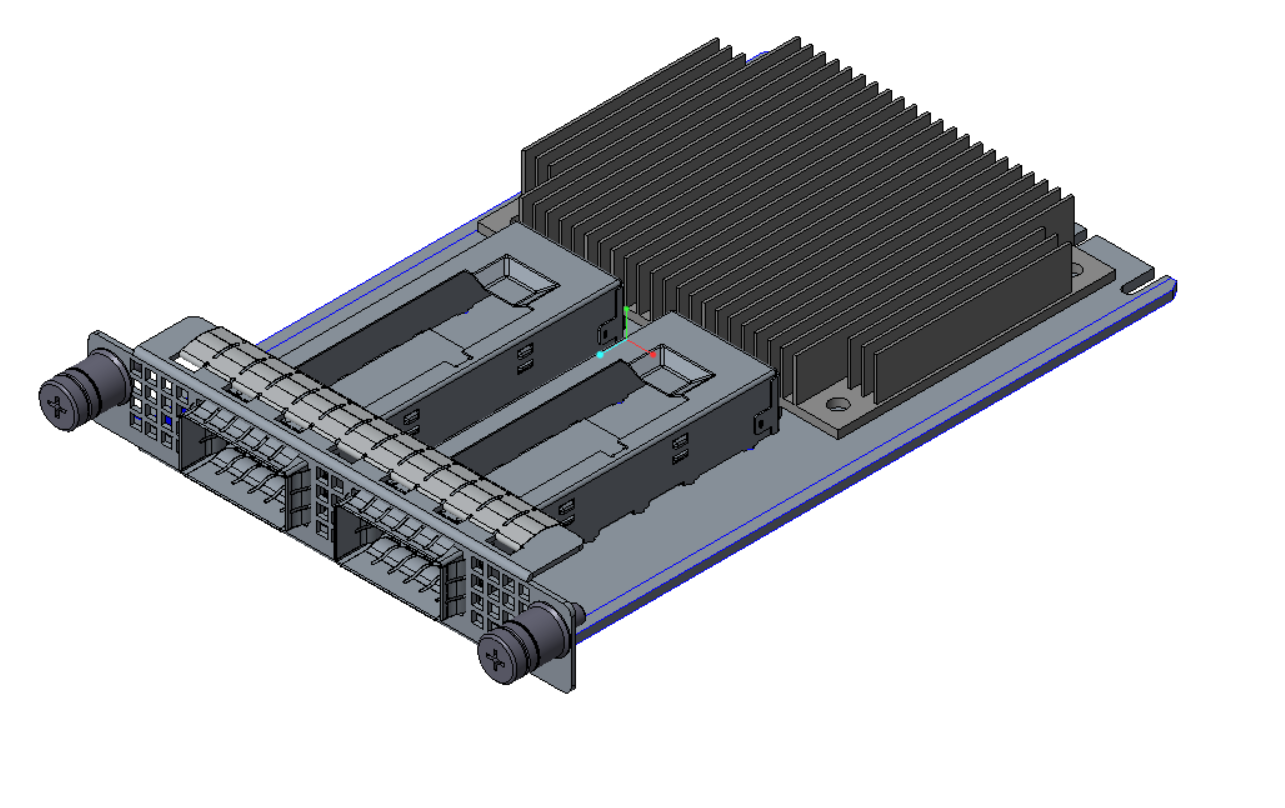
## Form factor options

OCP3.0 provides two fundamental form factor options: a small card (76mm x 115mm) and a large card (142mm x 115mm).

These form factors support a Primary Connector and optionally, a Secondary Connector. The Primary Connector is defined to be a SFF-TA-1002 compliant 4C connector plus a 28-pin bay extension for OCP 3.0 specific pins. The Secondary Connector is the 4C connector as defined in SFF-TA-1002. The 4C specification supports up to 32 differential pairs for a x16 PCIe connection per connector. For host platforms, the 28-pin OCP bay is required for the Primary connector. This is also mandatory for add-in cards.

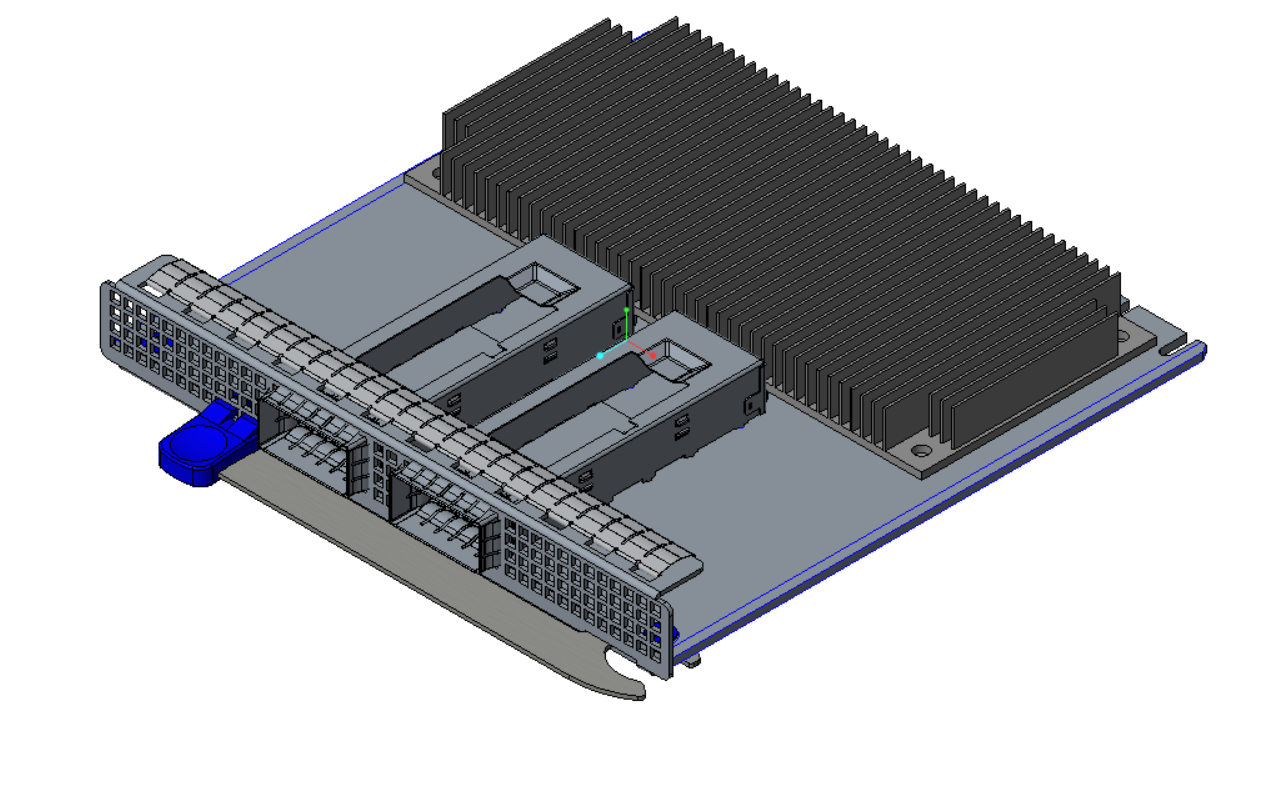
The small card uses the 4C connector for up to a x16 PCIe interface. The small cards implement the 28 pin OCP bay for management functions and support for up to a four PCIe hosts. The small size card provides sufficient faceplate area to accommodate up to 2x QSFP modules, 4x SFP modules, or 4x RJ-45 for BASE-T operation. The small card form factor supports up to 79W of delivered power to the card edge.

Figure 3: Example Small Card Form Factor



The large card uses provides the same functionality as the small card, but with support up to x32 PCIe interface. The large card utilizes both the Primary and Secondary connectors. The large size card supports higher power envelopes and provides additional board area for more complex designs. The small card form factor supports up to 158W of delivered power to the card edge at 79W per connector.

Figure 4: Example Large Card Form Factor



For both form-factors, an add-in card may optionally implement a subset of pins support a x8 PCIe connection. This is implemented using a 2C connector per SFF-TA-1002. The Primary Connector may support a 2C sized add in card along with the 28 pin OCP bay. The Secondary Connector cards may also support a 2C sized add in card. The following diagram from the SFF-TA-1002 specification illustrates the supported host Primary and Secondary Connectors and add in card configurations.

Figure 4: Primary Connector (4C + OCP Bay) with 4C and 2C Add in Cards

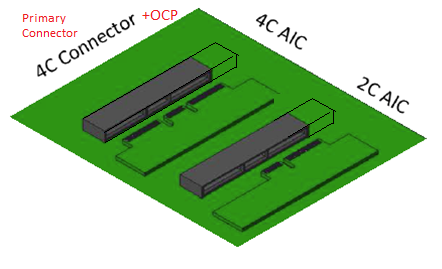


Figure 5: Secondary Connector (4C) with 4C and 2C Add in Cards

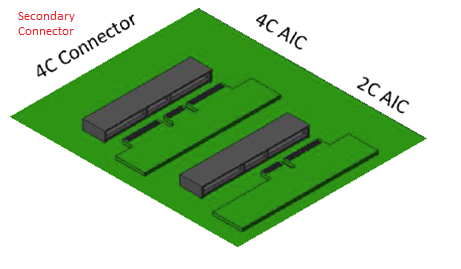


Table 1 summarizes the supported card form factors. Small form factors cards may support the Primary Connector, or the Secondary Connector and support up to 16 lanes of PCIe. Large form factor cards may support both the Primary and Secondary Connectors and support up to 32 lanes of PCIe.

Table 1: OCP 3.0 Card Definitions

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Host Connectors:** | **Secondary** | | **Primary** | | |
|  | Max: 4C Connector, x16 PCIe  Min: 2C Connector, x8 PCIe | | Max: 4C Connector, x16 PCIe  Min: 2C Connector, x8 PCIe | | OCP Bay |
| **Add in Cards:** |  | |  | |  |
| Small (x8) – Primary |  |  |  | 2C | OCP Bay |
| Small (x16) – Primary |  |  | 4C | | OCP Bay |
| Small (x8) – Secondary |  | 2C |  | |  |
| Small (x16) – Secondary | 4C | |  | |  |
| Large 1 (x24) |  | 2C | 4C | | OCP Bay |
| Large 2 (x32) | 4C | | 4C | | OCP Bay |

## I/O bracket

## Port and LED

## Labeling

## Insulation requirement

## NIC Implementation examples

## Non-NIC Use cases

“PCIe interface with extra management sideband”

### PCIe Retimer card

### Accelerator card

### Storage HBA / RAID card

# Card edge – Baseboard connector Interface

## Gold Finger Requirement

**Editor’s note:** Connector vendors to provide input and all detailed views from the mechanical drawing. First stab at it is below. Diagrams are copied from SFF-TA-1002.

The OCP 3.0 mezzanine add-in cards are compliant to the SFF-TA-1002 specification with respect to the gold fingers and connectors.

Small Size cards may fit in the Primary Connector or the Secondary Connector. Primary Connector compliant cards are 76mm x 115mm and may implement the full 168-pins. Secondary Connector compliant cards are XXXmm x 115mm and may implement the 140-pin gold finger. Both the Primary and Secondary Connector cards may implement a subset of gold finger pins if there is a reduced PCIe width requirement (such as 1 x8). In this case, the card edge gold finger may implement a 2C design. The overall board thickness is 1.60mm. The gold finger dimensions for the Primary Connector and Secondary Connector compliant cards are shown below.

Large Size Cards support up to a x32 PCIe implementation and uses both the Primary and Secondary connectors.

For additional details, refer to the card and connector mechanical drawings located in XXX.

Note: The “B” pins on the connector are associated with the primary (top) side of the add-in card. The “A” pins on the connector are associated with the secondary (bottom) side of the add-in card.

Figure 6: Small Size Primary Connector Gold Finger Mating Card Dimensions – x16 – Primary Side

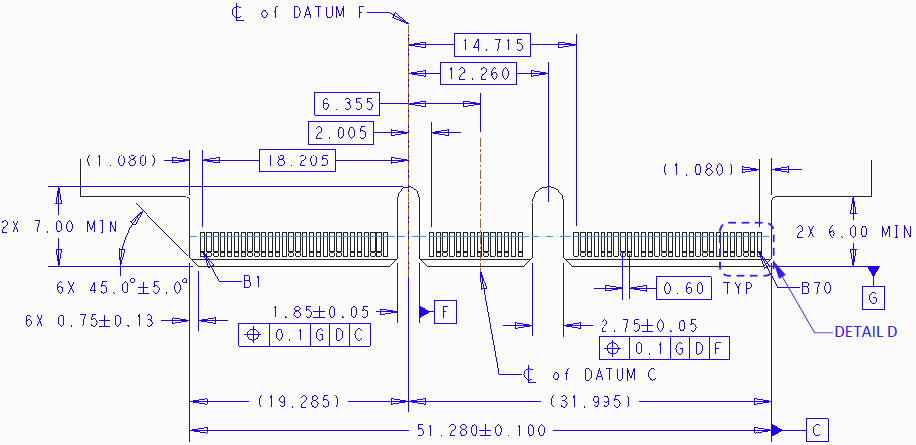


Figure 7: Small Size Primary Connector Gold Finger Mating Card Dimensions – x16 – Secondary Side

TBD

Figure 8: Small Size Secondary Connector Gold Finger Mating Card Dimensions – x16 – Primary Side

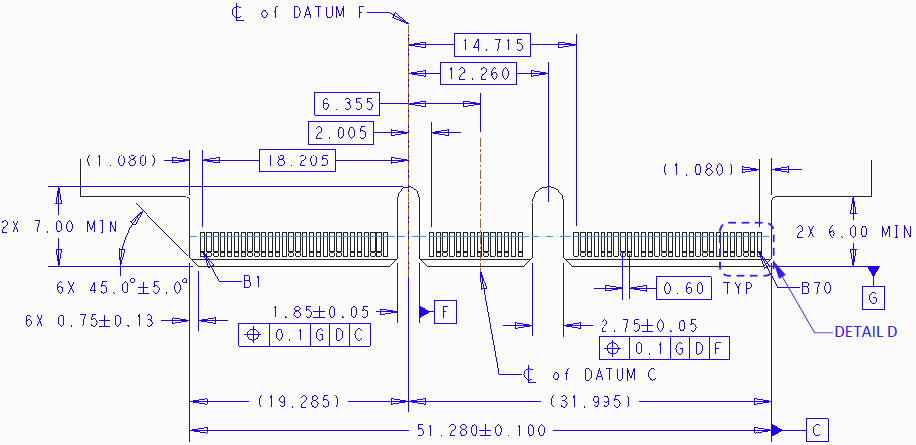


Figure 9: Small Size Secondary Connector Gold Finger Mating Card Dimensions – x16 – Secondary Side

TBD

Figure 10: Large Size Card Gold Finger Mating Card Dimensions – x32 – Primary Side

TBD

Figure 11: Large Size Card Gold Finger Mating Card Dimensions – x32 – Secondary Side

TBD

## Baseboard Connector Requirement

**Editor’s note:** Connector vendors to provide input.

The OCP3.0 connector is compliant to the “4C connector” as defined in the SFF-TA-1002 specification for a right angle or straddle mount form-factor. The 4C connector is 140-pins in width and includes support for up to 32 differential pairs to support a x16 PCIe connection. The connector also provides 6 pins of 12V for payload power. This implementation is common between both the Primary and Secondary Connector. In addition, the Primary Connector has a 28-pin OCP Bay to the right of pin 1. These pins are used for management and support for a 4 x4 multi-host configuration. The Primary and Secondary Connector drawings are shown in Figure 5 and Figure 6, below.

Figure 12: 168-pin Base Board Primary Connector – Right Angle

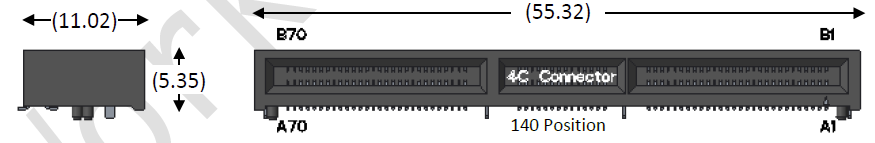


Figure 13: 140-pin Base Board Secondary Connector – Right Angle

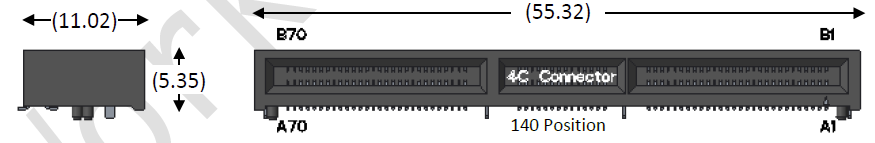


Figure 12: 168-pin Base Board Primary Connector – Straddle Mount

TBD

Figure 13: 140-pin Base Board Secondary Connector – Straddle Mount

TBD

## Pin definition

**Editor’s note:** The pin map aligns with OCP 3.0 Pinout Proposal 20171121a\_TN.xlsx.

The pin definition of a mezzanine card with up to a x32 PCIe interface are shown in Table 1 and Table 2. All signal directions are shown from the perspective of the baseboard.

A baseboard system may provide a combination of Primary Connectors, and Secondary Connectors. Both connectors have common functionality with power, SMBus, x16 PCIe Gen4 connections and bifurcation control. Baseboards that implement both the Primary Connector and Secondary Connector (located adjacent to each other) can support up to 32 PCIe lanes or can be mechanically implemented as two standalone x16 cards. Depending on the baseboard form-factor, multiple Primary Connector or Secondary Connector compliant cards may be designed into the system.

The Primary Connector has an additional OCP Bay (pins OCP\_A[1:14], OCP\_B[1:14]) with additional REFCLKs for supporting up to four PCIe hosts as well as NC-SI connectivity and a scan chain for information exchange between the host and card.

The pins common to the Primary and Secondary Connector are shown in Section 4.4. The OCP Bay for the Primary Connector only are shown in Section 4.5.

Cards or systems that do not require the use of a PCIe x16 connection may optionally implement a subset electrical connections as applicable to the design (for example, a x8 card using the first 8 PCIe lanes that is compliant with the Primary or Secondary Connector pinout). Please refer to Sections 4.1 and 4.2 for mechanical details. For these cases, the Primary and Secondary Connector matches the “2C” dimensions as defined in SFF-TA-1002.

In all cases, the host shall implement the Primary and Secondary Connector supporting x16 PCIe widths. Add-in cards may implement a x8 interface at the card edge.

Table 1: Primary Connector Mezzanine Card Pin Definition (x16) (4C + OCP Bay)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Side B** | | **Side A** | |  | |
| OCP\_B1 | LD# | CLK | OCP\_A1 | **Primary Connector (x16, 168-pin add-in card with OCP Bay)** | **Primary Connector (x8, 112-pin add-in card with OCP bay)** |
| OCP\_B2 | DATA\_IN | DATA\_OUT | OCP\_A2 |
| OCP\_B3 | PERST2# | PERST3# | OCP\_A3 |
| OCP\_B4 | NIC\_PWR\_GOOD | RBT\_ARB\_IN | OCP\_A4 |
| OCP\_B5 | PWRBRK# | RBT\_ARB\_OUT | OCP\_A5 |
| OCP\_B6 | RFU, N/C | GND | OCP\_A6 |
| OCP\_B7 | RBT\_RXD1 | RBT\_TXD1 | OCP\_A7 |
| OCP\_B8 | RBT\_RXD0 | RBT\_TXD0 | OCP\_A8 |
| OCP\_B9 | RBT\_CLK\_IN | RBT\_TX\_EN | OCP\_A9 |
| OCP\_B10 | GND | GND | OCP\_A10 |
| OCP\_B11 | REFCLKn2 | REFCLKn3 | OCP\_A11 |
| OCP\_B12 | REFCLKp2 | REFCLKp3 | OCP\_A12 |
| OCP\_B13 | GND | GND | OCP\_A13 |
| OCP\_B14 | RBT\_CRS\_DV | WAKE\_N | OCP\_A14 |
| **Mechanical Key** | | | |
| B1 | +12V/+12V\_AUX | GND | A1 |
| B2 | +12V/+12V\_AUX | GND | A2 |
| B3 | +12V/+12V\_AUX | GND | A3 |
| B4 | +12V/+12V\_AUX | GND | A4 |
| B5 | +12V/+12V\_AUX | GND | A5 |
| B6 | +12V/+12V\_AUX | GND | A6 |
| B7 | BIF0# | SMCLK | A7 |
| B8 | BIF1# | SMDAT | A8 |
| B9 | BIF2# | SMRST# | A9 |
| B10 | PERST0# | PRSNTB2# | A10 |
| B11 | +3.3V/+3.3V\_AUX | PERST1# | A11 |
| B12 | PWRDIS | PRSNTA# | A12 |
| B13 | GND | GND | A13 |
| B14 | REFCLKn0 | REFCLKn1 | A14 |
| B15 | REFCLKp0 | REFCLKp1 | A15 |
| B16 | GND | GND | A16 |
| B17 | PETn0 | PERn0 | A17 |
| B18 | PETp0 | PERp0 | A18 |
| B19 | GND | GND | A19 |
| B20 | PETn1 | PERn1 | A20 |
| B21 | PETp1 | PERp1 | A21 |
| B22 | GND | GND | A22 |
| B23 | PETn2 | PERn2 | A23 |
| B24 | PETp2 | PERp2 | A24 |
| B25 | GND | GND | A25 |
| B26 | PETn3 | PERn3 | A26 |
| B27 | PETp3 | PERp3 | A27 |
| B28 | GND | GND | A28 |
| **Mechanical Key** | | | |
| B29 | GND | GND | A29 |
| B30 | PETn4 | PERn4 | A30 |
| B31 | PETp4 | PERp4 | A31 |
| B32 | GND | GND | A32 |
| B33 | PETn5 | PERn5 | A33 |
| B34 | PETp5 | PERp5 | A34 |
| B35 | GND | GND | A35 |
| B36 | PETn6 | PERn6 | A36 |
| B37 | PETp6 | PERp6 | A37 |
| B38 | GND | GND | A38 |
| B39 | PETn7 | PERn7 | A39 |
| B40 | PETp7 | PERp7 | A40 |
| B41 | GND | GND | A41 |
| B42 | PRSNTB0# | PRSNTB1# | A42 |
| **Mechanical Key** | | | |  |
| B43 | GND | GND | A43 |  |
| B44 | PETn8 | PERn8 | A44 |  |
| B45 | PETp8 | PERp8 | A45 |  |
| B46 | GND | GND | A46 |  |
| B47 | PETn9 | PERn9 | A47 |  |
| B48 | PETp9 | PERp9 | A48 |  |
| B49 | GND | GND | A49 |  |
| B50 | PETn10 | PERn10 | A50 |  |
| B51 | PETp10 | PERp10 | A51 |  |
| B52 | GND | GND | A52 |  |
| B53 | PETn11 | PERn11 | A53 |  |
| B54 | PETp11 | PERp11 | A54 |  |
| B55 | GND | GND | A55 |  |
| B56 | PETn12 | PERn12 | A56 |  |
| B57 | PETp12 | PERp12 | A57 |  |
| B58 | GND | GND | A58 |  |
| B59 | PETn13 | PERn13 | A59 |  |
| B60 | PETp13 | PERp13 | A60 |  |
| B61 | GND | GND | A61 |  |
| B62 | PETn14 | PERn14 | A62 |  |
| B63 | PETp14 | PERp14 | A63 |  |
| B64 | GND | GND | A64 |  |
| B65 | PETn15 | PERn15 | A65 |  |
| B66 | PETp15 | PERp15 | A66 |  |
| B67 | GND | GND | A67 |  |
| B68 | RFU, N/C | RFU, N/C | A68 |  |
| B69 | RFU, N/C | RFU, N/C | A69 |  |
| B70 | PRSNTB3# | RFU, N/C | A70 |  |

Table 2: Secondary Connector Mezzanine Card Pin Definition (x16) (4C)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Side B** | | **Side A** | |  | |
| B1 | +12V/+12V\_AUX | GND | A1 | **Secondary Connector (x16, 140-pin add-in card)** | **Secondary Connector (x8, 84-pin add-in card)** |
| B2 | +12V/+12V\_AUX | GND | A2 |
| B3 | +12V/+12V\_AUX | GND | A3 |
| B4 | +12V/+12V\_AUX | GND | A4 |
| B5 | +12V/+12V\_AUX | GND | A5 |
| B6 | +12V/+12V\_AUX | GND | A6 |
| B7 | BIF0# | SMCLK | A7 |
| B8 | BIF1# | SMDAT | A8 |
| B9 | BIF2# | SMRST# | A9 |
| B10 | PERST0# | PRSNTB2# | A10 |
| B11 | +3.3V/+3.3V\_AUX | PERST1# | A11 |
| B12 | PWRDIS | PRSNTA# | A12 |
| B13 | GND | GND | A13 |
| B14 | REFCLKn0 | REFCLKn1 | A14 |
| B15 | REFCLKp0 | REFCLKp1 | A15 |
| B16 | GND | GND | A16 |
| B17 | PETn0 | PERn0 | A17 |
| B18 | PETp0 | PERp0 | A18 |
| B19 | GND | GND | A19 |
| B20 | PETn1 | PERn1 | A20 |
| B21 | PETp1 | PERp1 | A21 |
| B22 | GND | GND | A22 |
| B23 | PETn2 | PERn2 | A23 |
| B24 | PETp2 | PERp2 | A24 |
| B25 | GND | GND | A25 |
| B26 | PETn3 | PERn3 | A26 |
| B27 | PETp3 | PERp3 | A27 |
| B28 | GND | GND | A28 |
| **Mechanical Key** | | | |
| B29 | GND | GND | A29 |
| B30 | PETn4 | PERn4 | A30 |
| B31 | PETp4 | PERp4 | A31 |
| B32 | GND | GND | A32 |
| B33 | PETn5 | PERn5 | A33 |
| B34 | PETp5 | PERp5 | A34 |
| B35 | GND | GND | A35 |
| B36 | PETn6 | PERn6 | A36 |
| B37 | PETp6 | PERp6 | A37 |
| B38 | GND | GND | A38 |
| B39 | PETn7 | PERn7 | A39 |
| B40 | PETp7 | PERp7 | A40 |
| B41 | GND | GND | A41 |
| B42 | PRSNTB0# | PRSNTB1# | A42 |
| **Mechanical Key** | | | |  |
| B43 | GND | GND | A43 |  |
| B44 | PETn8 | PERn8 | A44 |  |
| B45 | PETp8 | PERp8 | A45 |  |
| B46 | GND | GND | A46 |  |
| B47 | PETn9 | PERn9 | A47 |  |
| B48 | PETp9 | PERp9 | A48 |  |
| B49 | GND | GND | A49 |  |
| B50 | PETn10 | PERn10 | A50 |  |
| B51 | PETp10 | PERp10 | A51 |  |
| B52 | GND | GND | A52 |  |
| B53 | PETn11 | PERn11 | A53 |  |
| B54 | PETp11 | PERp11 | A54 |  |
| B55 | GND | GND | A55 |  |
| B56 | PETn12 | PERn12 | A56 |  |
| B57 | PETp12 | PERp12 | A57 |  |
| B58 | GND | GND | A58 |  |
| B59 | PETn13 | PERn13 | A59 |  |
| B60 | PETp13 | PERp13 | A60 |  |
| B61 | GND | GND | A61 |  |
| B62 | PETn14 | PERn14 | A62 |  |
| B63 | PETp14 | PERp14 | A63 |  |
| B64 | GND | GND | A64 |  |
| B65 | PETn15 | PERn15 | A65 |  |
| B66 | PETp15 | PERp15 | A66 |  |
| B67 | GND | GND | A67 |  |
| B68 | RFU, N/C | RFU, N/C | A68 |  |
| B69 | RFU, N/C | RFU, N/C | A69 |  |
| B70 | PRSNTB3# | RFU, N/C | A70 |  |

## Signal Descriptions – Common

The pins shown in this section are common to both the Primary and Secondary Connectors. All pin directions are from the perspective of the baseboard.

**Note:** Pins that are only used on Primary Connector 28-pin OCP bay are defined in Section 4.5.

### PCIe Interface Pins

This section provides the pin assignments for the PCIe interface signals. The AC/DC specifications are defined in Section XXX. Example connection diagrams for are shown in Figure 7 and Figure 8.

Table 2: Mezzanine Card Pin Descriptions – PCIe

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Name** | **Pin #** | **Baseboard Direction** | **Signal Description** |
| REFCLKn0  REFCLKp0 | B14  B15 | Output | PCIe compliant differential reference clock #0, and #1. 100MHz HCSL reference clocks are used for the add-in card PCIe core logic.  **Note:** For cards that only support 1 x16, REFCLK0 is used. For cards that support 2 x8, REFCLK0 is used for the first eight PCIe lanes, and REFCLK1 is used for the second eight PCIe lanes.  Refer to Section 2.1 in the PCIe CEM Specification, Rev 4.0 for electrical details. |
| REFCLKn1  REFCLKp1 | A14  A15 | Output |
| PETn0  PETp0 | B17  B18 | Output | Transmitter differential pair [0:15]. These pins are connected from the baseboard transmitter differential pairs to the receiver differential pairs on the add-in card.  The PCIe Transmit pins are AC coupled on the baseboard with capacitors and are placed next to the baseboard transmitters. The AC coupling capacitor must be between 176nF (min) and 265nF (max).  Refer to Section 6.1 in the PCIe CEM Specification, Rev 4.0 for details. |
| PETn1  PETp1 | B20  B21 | Output |
| PETn2  PETp2 | B23  B24 | Output |
| PETn3  PETp3 | B26  B27 | Output |
| PETn4  PETp4 | B30  B31 | Output |
| PETn5  PETp5 | B33  B34 | Output |
| PETn6  PETp6 | B36  B37 | Output |
| PETn7  PETp7 | B39  B40 | Output |
| PETn8  PETp8 | B44  B45 | Output |
| PETn9  PETp9 | B47  B48 | Output |
| PETn10  PETp10 | B50  B51 | Output |
| PETn11  PETp11 | B53  B54 | Output |
| PETn12  PETp12 | B56  B57 | Output |
| PETn13  PETp13 | B59  B60 | Output |
| PETn14  PETp14 | B62  B63 | Output |
| PETn15  PETp15 | B65  B66 | Output |
| PERn0  PERp0 | A17  A18 | Input | Receiver differential pair [0:15]. These pins are connected from the add-in card transmitter differential pairs to the receiver differential pairs on the baseboard.  The PCIe Receive pins are AC coupled on the add-in card with capacitors and are placed next to the add-in card transmitters. The AC coupling capacitor must be between 176nF (min) and 265nF (max).  Refer to Section 6.1 in the PCIe CEM Specification, Rev 4.0 for details. |
| PERn1  PERp1 | A20  A21 | Input |
| PERn2  PERp2 | A23  A24 | Input |
| PERn3  PERp3 | A26  A27 | Input |
| PERn4  PERp4 | A30  A31 | Input |
| PERn5  PERp5 | A33  A34 | Input |
| PERn6  PERp6 | A36  A37 | Input |
| PERn7  PERp7 | A39  A40 | Input |
| PERn8  PERp8 | A44  A45 | Input |
| PERn9  PERp9 | A47  A48 | Input |
| PERn10  PERp10 | A50  A51 | Input |
| PERn11  PERp11 | A53  A54 | Input |
| PERn12  PERp12 | A56  A57 | Input |
| PERn13  PERp13 | A59  A60 | Input |
| PERn14  PERp14 | A62  A63 | Input |
| PERn15  PERp15 | A65  A66 | Input |
| PERST0#  PERST1# | B10  A11 | Output | PCIe Reset #0, #1. Active low.  Indicates when the applied power is within tolerance and stable for the add-in card. PERST# goes high after 100ms per the PCI CEM Specification when the power rails are within operating limits. The PCIe REFCLKs also become stable within this period of time.  PERST is pulled high on the baseboard.  **Note:** For cards that only support 1 x16, PERST0# is used. For cards that support 2 x8, PERST0# is used for the first eight PCIe lanes, and PERST1# is used for the second eight PCIe lanes.  Refer to Section 2.2 in the PCIe CEM Specification, Rev 4.0 for details. |

For each add-in card, the following REFCLK connection rules must be followed:

* For a 1 x16 capable add-in card, REFCLK0 is used for the PCIe end-point.
* For a 2 x8 capable add-in card, REFCLK0 is used for lanes [0:7] and REFCLK1 is used for lanes [8:15].
* For a 4 x4 capable add-in card, REFCLK0 is used for lanes [0:3], REFCLK1 is used for lanes [4:7], REFCLK2 is used for lanes [8:11] and REFCLK3 is used for lanes [12:15]. Pins for REFCLK2 and REFCLK3 are described in Section 4.5.1 and are located on the 28-pin OCP bay.

Figure 14: PCIe Interface Connections for 1 x16 and 2 x8 Add-in Cards



Figure 15: PCIe Interface Connections for a 4 x4 Add-in Card



### PCIe Present and Bifurcation Control Pins

This section provides the pin assignments for the PCIe present and bifurcation control pins. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure 9.

Table 3: Mezzanine Card Pin Descriptions – PCIe Present and Bifurcation Control Pins

|  |  |  |  |
| --- | --- | --- | --- |
| PRSNTA# | A12 | Output | Present A is used for card presence and add-in card PCIe capabilities detection. This pin is connected to GND on the baseboard. This pin is connected to the Present B pins on the add-in card. |
| PRSNTB0#  PRSNTB1#  PRSNTB2#  PRSNTB3# | B42  A42  A10  B70 | Input | Present B [0:3]# are used for card presence detection and PCIe capabilities detection.  For baseboards, these pins are connected to the I/O hub and are pulled up to +3.3V using 1kOhm resistors.  For add-in cards, these pins are strapped to PRSNTA#. The encoding definitions are described in Section 4.6.  PRSNTB3# is located at the bottom of the 4C connector and is only applicable for add-in cards with a PCIe width of x16 (or greater). Add-in cards that implement a 2C card edge do not use the PRSNTB3# pin for capabilities or present detection. |
| BIF0#  BIF1#  BIF2# | A7  A8  A9 | Output | Bifurcation [0:2]# are outputs driven from the baseboard I/O hub and allows the system to force configure the add-in card bifurcation.  The encoding definitions are described in Section 4.6. |

Figure 16: PCIe Present and Bifurcation Control Pins



### SMBus Interface Pins

This section provides the pin assignments for the SMBus interface signals. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure XXX.

Table 4: Mezzanine Card Pin Descriptions – SMBus

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Name** | **Pin #** | **Baseboard Direction** | **Signal Description** |
| SMCLK | A7 | Output | SMBus clock. Open drain, pulled up to +3.3V on the baseboard. |
| SMDAT | A8 | Input / Output | SMBus Data. Open drain, pulled up to +3.3V on the baseboard. |
| SMRST# | A9 | Output | SMBus reset. Open drain, pulled up to +3.3V on the baseboard. Used to reset optional downstream SMBus devices (such as I/O expanders or thermal sensors). |

### Power Supply Pins

This section provides the pin assignments for the power supply interface signals. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure XXX.

Table 5: Mezzanine Card Pin Descriptions – Power

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Name** | **Pin #** | **Baseboard Direction** | **Signal Description** |
| GND | Various | GND | Ground return; a total of 46 ground pins are on the main 140-pin connector area. |
| +12V/+12V\_AUX | B1, B2, B3, B4, B5, B6 | Power | +12V main or 12V Aux power; total of 6 pins per connector. The 12V pins are rated to 1.1A per pin with a maximum derated power delivery of 79.2W.  The +12V power pins must be within the rail tolerances when the PWRDIS pin is driven low by the baseboard. |
| +3.3V/3.3V\_AUX | B11 | Power | +3.3V main or +3.3V Aux power; total of 1 pin per connector. The 3.3V pin is rated to 1.1A for a maximum derated power delivery of 3.63W.  The +3.3V power pin must be within the rail tolerances when the PWRDIS pin is driven low by the baseboard. |
| PWRDIS | B12 | Output | Power disable. Active high.  This signal is driven by the baseboard.  When high, this signal notifies the add-in card to turn off all systems connected to +12V power.  When low, this signal notifies the add-in card to enable the on-card power supplies. |

### Miscellaneous Pins

This section provides the pin assignments for the miscellaneous interface signals. The AC/DC specifications are defined in Section XXX.

Table 6: Mezzanine Card Pin Descriptions – Miscellaneous

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Name** | **Pin #** | **Baseboard Direction** | **Signal Description** |
| RFU, N/C | B68, B69, A68, A69, A70 | Input / Output | Reserved future use pin. Leave these pins as no connect. |

## Signal Descriptions – OCP Bay (Primary Connector Only)

The following section describes the functions in the Primary Connector 28-pin OCP bay. This 28 pin bay is shown in Section 4.3 and have pin numbers designated as OCP\_B[1:14], and OCP\_A[1:14]. All pin directions on this OCP bay are from the perspective of the baseboard.

**Note:** The pins that are common to both Connectors A and B are defined in Section 4.4.

### PCIe Interface Pins – OCP Connector A only

This section provides the pin assignments for the PCIe interface signals on the Primar Connector OCP bay. The AC/DC specifications are defined in Section XXX. An example connection diagram that shows REFCLK2, REFCLK3, PERST2# and PERST3# is shown in Figure 8.

Table 7: Mezzanine Card Pin Descriptions – PCIe

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Name** | **Pin #** | **Baseboard Direction** | **Signal Description** |
| REFCLKn2  REFCLKp2 | OCP\_B11  OCP\_B12 | Output | PCIe compliant differential reference clock #2, and #3. 100MHz HCSL reference clocks are used for the add-in card PCIe core logic.  **Note:** REFCLK2 and REFCLK3 are not used for cards that only support a 1 x16 or 2 x8 connection.  Refer to Section 2.1 in the PCIe CEM Specification, Rev 4.0 for details. |
| REFCLKn3  REFCLKp3 | OCP\_A11  OCP\_A12 | Output |
| PERST2#  PERST3# | OCP\_B3  OCP\_A3 | Output | PCIe Reset #2, #3. Active low.  Indicates when the applied power is within tolerance and stable for the add-in card. PERST# goes high after 100ms per the PCI CEM Specification when the power rails are within operating limits. The PCIe REFCLKs also become stable within this period of time.  PERST is pulled high on the baseboard.  **Note:** PERST2# and PERST3# are not used for cards that only support a 1 x16 or 2 x8 connection.  Refer to Section 2.2 in the PCIe CEM Specification, Rev 4.0 for details. |
| WAKE# | OCP\_A14 | Input | WAKE#. Active low. This signal is pulled up to +3.3V on the baseboard with a 10kOhm resistor.  This signal is driven by the add-in card to notify the baseboard restore the PCIe link. For add-in cards that support multiple WAKE# signals, their respective WAKE# pins may be tied together as the signal is open-drain to form a wired-OR.  Refer to Section 2.3 in the PCIe CEM Specification, Rev 4.0 for details. |

### NC-SI Over RBT Interface Pins – OCP Primary Connector only

This section provides the pin assignments for the NC-SI over RBT interface signals on the Primary Connector OCP bay. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure 10.

Refer to the NC-SI Specification for implementation and timing details.

Table 8: Mezzanine Card Pin Descriptions – NC-SI Over RBT

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Name** | **Pin #** | **Baseboard Direction** | **Signal Description** |
| RBT\_CLK\_IN | OCP\_B9 | Output | Reference clock input. Synchronous clock reference for receive, transmit and control interface. The clock has a nominal frequency of 50MHz ±100ppm. |
| RBT\_CRS\_DV | OCP\_B14 | Input | Carrier sense/receive data valid. Signal is used to indicate to the baseboard that the carrier sense/receive data is valid. |
| RBT\_RXD0  RBT\_RXD1 | OCP\_B8  OCP\_B7 | Input | Receive data. Data signals from the network controller to the BMC. |
| RBT\_TX\_EN | OCP\_A9 | Output | Transmit enable. |
| RBT\_TXD0  RBT\_TXD1 | OCP\_A8  OCP\_A7 | Output | Transmit data. Data signals from the BMC to the network controller. |
| RBT\_ARB\_OUT | OCP\_A5 | Output | NC-SI hardware arbitration output. Used only if the end point silicon supports hardware arbitration. Connects to the ARB\_IN signal of an adjacent device. |
| RBT\_ARB\_IN | OCP\_A4 | Input | NC-SI hardware arbitration input. Used only if the end point silicon supports hardware arbitration. Connects to the ARB\_OUT signal of an adjacent device. |

Figure 17: NC-SI Over RBT Connection Example



### Scan Chain Pins – OCP Primary Connector only

This section provides the pin assignments for the Scan Bus interface signals on the Primary Connector OCP Bay. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure 17.

Table 9: Mezzanine Card Pin Descriptions – Scan Bus

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Name** | **Pin #** | **Baseboard Direction** | **Signal Description** |
| CLK | OCP\_A1 | Output | Scan clock. The SS\_CLK is an output pin from the baseboard to the add-in card. |
| DATA\_OUT | OCP\_A2 | Output | Scan clock data output from the baseboard to the add-in card. This bit stream is used to shift in NIC configuration data. |
| DATA\_IN | OCP\_B2 | Input | Scan clock data input to the baseboard. This bit stream is used to shift out NIC status bits. |
| LD# | OCP\_B1 | Output | Scan clock shift register load. Used to latch configuration data on the add-in card. |

The scan chain bit definition is defined in the two tables below. The scan chain data stream is 32-bits in length.

The DATA\_OUT bus is an output from the host. The DATA\_OUT bus provides initial configuration options to the add-in card. The default implementation is completed with a single 8-bit 74LV594 serial in to parallel out shift register for the first 8 bytes. The remaining 3 bytes are padded with 0’s in the data stream.

The DATA\_IN bus is an input to the host. The DATA\_IN bus provides NIC status indication to the host. The default implementation is completed with two 8-bit 74LV165 parallel in to serial out shift registers in a cascaded implementation. Up to four shift registers may be implemented to provide additional NIC status indication to the host platform.

Shift registers 0 & 1 are mandatory for all cards. Shift registers 2 & 3 are optional depending on the card type. Shift register 2 may be used for future revisions of the scan chain. Shift registers 2 & 3 are required for card implementations with 5-8 ports.

A 1kOhm pull up resistor shall be connected to the SER input of the last shift register in the DATA\_IN scan chain to maintain a default bit value of 0b1 for unused bits.

Table 9: Mezzanine Card Pin Descriptions – Scan Bus DATA\_OUT Bit Definition

|  |  |  |  |
| --- | --- | --- | --- |
| **Byte.bit** | **DATA\_OUT Field Name** | **Default Value** | **Description** |
| 0.0 | SLOT\_ID[0] | 0b0 | Used to set the two LSB of the RBT Device address  SLOT\_ID[1:0] = 0b00 – RBT Address 0b00  SLOT\_ID[1:0] = 0b01 – RBT Address 0b01  SLOT\_ID[1:0] = 0b10 – RBT Address 0b10  SLOT\_ID[1:0] = 0b11 – RBT Address 0b11 |
| 0.1 | SLOT\_ID[1] | 0b0 |
| 0.[2..7] | RSVD | 0b000000 | Reserved. Bits 2..7 default to zero. |
| 1.[0..7] | RSVD | 0h00 | Reserved. Byte 1 value is 0h00. |
| 2.[0..7] | RSVD | 0h00 | Reserved. Byte 2 value is 0h00. |
| 3.[0..7] | RSVD | 0h00 | Reserved. Byte 3 value is 0h00. |

Table 9: Mezzanine Card Pin Descriptions – Scan Bus DATA\_IN Bit Definition

|  |  |  |  |
| --- | --- | --- | --- |
| **Byte.bit** | **DATA\_OUT Field Name** | **Default Value** | **Description** |
| 0.0 | PRSNTB[0]# | 0bX | PRSNTB[3:0]# value mirrored from the Primary Connector. |
| 0.1 | PRSNTB[1]# | 0bX |
| 0.2 | PRSNTB[2]# | 0bX |
| 0.3 | PRSNTB[3]# | 0bX |
| 0.4 | WAKE\_N | 0bX | PCIe WAKE\_N signal mirrored from the Primary Connector. |
| 0.5 | TEMP\_WARN | 0b0 | Temperature monitoring pin from on-card thermal solution. Asserted high when temperature sensor exceeds the warning threshold. |
| 0.6 | TEMP\_CRIT | 0b0 | Temperature monitoring pin from on-card thermal solution. Asserted high when temperature sensor exceeds the critical threshold. |
| 0.7 | FAN\_ON\_AUX | 0b0 | When high, FAN\_ON\_AUX requests the system fan to be enabled for extra cooling when the card is in the S5 state. |
| 1.0 | LINK0 | 0b1 | Port 0..3 link indication. Active low.  0b0 – Link LED is illuminated on the host platform.  0b1 – Link LED is not illuminated on the host platform.  Steady = link is detected on the port.  Off = no link is detected on the port. |
| 1.1 | LINK1 | 0b1 |
| 1.2 | LINK2 | 0b1 |
| 1.3 | LINK3 | 0b1 |
| 1.4 | ACT0 | 0b1 | Port 0..3 activity indication. Active low.  0b0 – Link LED is illuminated on the host platform.  0b1 – Link LED is not illuminated on the host platform.  Steady = no activity is detected on the port  Blink = activity is detected on the port.  Off = no link, see also LINK[3:0] LED bits. |
| 1.5 | ACT1 | 0b1 |
| 1.6 | ACT2 | 0b1 |
| 1.7 | ACT3 | 0b1 |
| 2.0 | ScanChainVer[0] | 0b1 | ScanChainVer[1:0] is used to indicate the scan chain bit definitions. The encoding is as follows:  0b11 – Scan chain bit definitions version 1 corresponding to OCP 3.0 spec version 1.0.  All other encodings are reserved. |
| 2.1 | ScanChainVer[1] | 0b1 |
| 2.2 | RSVD | 0b1 | Byte 2 bits [2:7] are reserved. These bits shall default to the value of 0b1. |
| 2.3 | RSVD | 0b1 |
| 2.4 | RSVD | 0b1 |
| 2.5 | RSVD | 0b1 |
| 2.6 | RSVD | 0b1 |
| 2.7 | RSVD | 0b1 |
| 3.0 | LINK4 | 0b1 | Port 4..7 link indication. Active low.  0b0 – Link LED is illuminated on the host platform.  0b1 – Link LED is not illuminated on the host platform.  Steady = link is detected on the port.  Off = no link is detected on the port. |
| 3.1 | LINK5 | 0b1 |
| 3.2 | LINK6 | 0b1 |
| 3.3 | LINK7 | 0b1 |
| 3.4 | ACT4 | 0b1 | Port 4..7 activity indication. Active low.  0b0 – Link LED is illuminated on the host platform.  0b1 – Link LED is not illuminated on the host platform.  Steady = no activity is detected on the port  Blink = activity is detected on the port.  Off = no link, see also LINK[3:0] LED bits. |
| 3.5 | ACT5 | 0b1 |
| 3.6 | ACT6 | 0b1 |
| 3.7 | ACT7 | 0b1 |

Figure 18: Scan Bus Connection Example

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### Connector A Miscellaneous Pins – OCP Connector A only

This section provides the miscellaneous pin assignments for the pins on the Connector A OCP Bay. The AC/DC specifications are defined in Section XXX. An example connection diagram is shown in Figure XXX.

Table 10: Mezzanine Card Pin Descriptions – Miscellaneous

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Name** | **Pin #** | **Baseboard Direction** | **Signal Description** |
| PWRBRK# | OCP\_B5 | Output | Power break. Active low, open drain.  This signal is pulled up to +3.3V on the add-in card with a minimum of 95kOhm and the baseboard with a stiffer resistance in-order to meet the timing specs as shown in CEM.  This signal is driven low by the baseboard and is used to notify that an Emergency Power Reduction State is requested. |
| NIC\_PWR\_GOOD | OCP\_B4 | Input | NIC power good. Active high. This signal is driven by the add-in card.  When high, this signal indicates that all of the add-in card power rails are operating within nominal tolerances.  When low the add-in card power supplies are not yet ready or are in a fault condition.  This signal is pulled down to ground with a 10kOhm resistor on the baseboard to prevent a false power good indication if no add-in card is present. |
| RFU, N/C | OCP\_B6 | Input / Output | Reserved future use pin. Leave this pin as a no connect. |
| GND | OCP\_A6  OCP\_A10 OCPA13 OCP B10  OCP\_B13 | GND | Ground return; a total of 5 ground pins are on the OCP bay area. |

## PCIe Bifurcation mechanism

OCP3.0 cards support use cases with multiple root ports on a baseboard connected to a single add-in card; or a single root port with multiple end points on the same add-in card. To accomplish this, there are two PCIe bifurcation configuration mechanisms via I/O pins:

* Add-in card to baseboard configuration (PRSNTA#, PRSNTB[3:0]#). The PRSNTA# and PRSNTB# pins are hard strapped on the add-in card.
* Baseboard to add-in card configuration (BIF[3:0]#). The BIF# pin states are controlled by the baseboard.

The bifurcation mechanism is connected as follows on a system implemented with both Connector A and Connector B.

Figure 19: PCIe Bifurcation Support



### PCIe Add-in Card to Baseboard Bifurcation Configuration (PRSNTA#, PRSNTB[3:0]#)

The add-in card to baseboard configuration mechanism consists of four dual use pins (PRSNTB[3:0]#). These pins provide card presence detection as well as mechanism to notify the baseboard of the pre-defined PCIe lane width capabilities. The PRSNTB[3:0]# pins are pulled up to +3.3V on the baseboard and are active low signals. A state of 0b1111 indicates that no card is present in the system. Depending on the capabilities of the add-in card, the PRSNTB[3:0]# signals may be strapped to the PRSNTA# signal. The encoding of the PRSTNB[3:0]# bits is shown in left hand column of Table xxx below.

### PCIe Baseboard to Add-in Card Bifurcation Configuration (BIF[2:0]#)

Three signals (BIF[2:0]#) are driven by the baseboard to notify requested bifurcation on the add-in card silicon. This allows the baseboard to set the lane configuration on the add-in card that supports multiple bifurcation options.

For example, a baseboard that has four separate hosts that support a 4 x4 connection, should appropriately drive the BIF[2:0]# pins per Table XXX and indicate to the add-in card silicon to setup a 4 x4 configuration.

### PCIe Bifurcation Decoder

The state combination of each of the PRSNTB[3:0]# and BIF[2:0]# pins deterministically sets the PCIe lane width for a given combination of baseboard and add-in cards.

For ease of reference, the negation of each binary encoding of the PRSNTB[3:0]# is designated with a Card Type value. The encoding 0b1111 is Card Type 0, encoding 0b1110 is Card Type 1, encoding 0b1101 is Card Type 2, etc.

[**Editor’s note:** Generate table directly in the specification once the encoding is locked down. Screen shot image quality may degrade due to publishing options]

Table 11: PCIe Bifurcation Decoder for x16 Width Cards

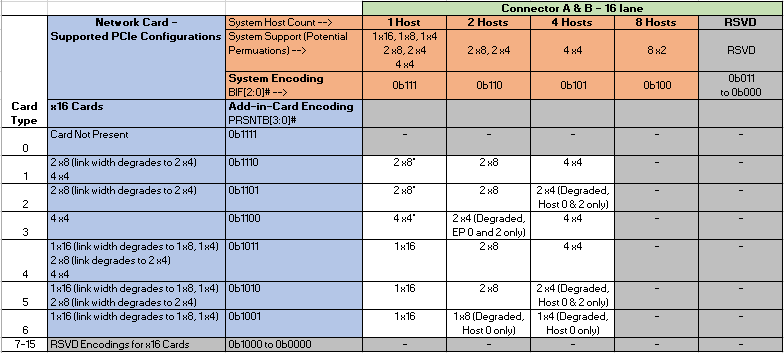
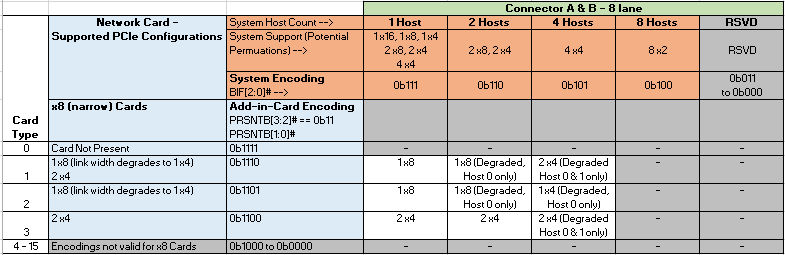


Table 11: PCIe Bifurcation Decoder for x8 Width Cards



\***Note:** The baseboard must disable PCIe lanes during the initialization phase if the number of detected PCIe links are greater than what is supported to prevent a nondeterministic solution.

For example, if the baseboard only supports a 1 x16 connection, and the add-in card only supports a 2 x8 connection, the baseboard must disable PCIe lanes 8-15 to prevent any LTSSM issues.

### Bifurcation Detection Flow

**[Need input and clarification]**The following detection flow shall be followed to determine the resulting link width based on both the baseboard and add-in card configurations.

1. The baseboard reads the state of the PRSNTB[3:0]# pins. If the resulting value is not 0b1111, a card is present. Firmware determines the add-in card PCIe lane width capabilities per Table 11.
2. The baseboard reconfigures the PCIe bifurcation on its ports to match the highest common lane width and lowest link count on the card.
3. For cases where the baseboard request a link count override (such as requesting a 4-host baseboard requesting 4 x4 operation on a supported card that would otherwise default to a 2 x8 case), the BIF[0:2]# pins would be asserted as appropriate.
4. PERST# is deasserted after the 100ms window as defined by the PCIe specification.

### PCIe Bifurcation Examples

For illustrative purposes, the following figures show several common bifurcation permutations.

Figure 13 illustrates a single host baseboard that supports x16 with a single controller add-in card that also supports x16 (Type 6). The PRSTNB[3:0]# state is 0b1001. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controller to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16. The single host baseboard determines that it is also capable of supporting 1 x16. The resulting link width is 1 x16.

Figure 20: Single Host (1 x16) and Type 6 Add-in Card (Single Controller, 1 x16 only)



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Figure 14 illustrates a single host baseboard that supports 2 x8 with a single controller add-in card that also supports 2 x8 (Type 2). The PRSTNB[3:0]# state is 0b1101. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 2 x8. The single host baseboard determines that it is also capable of supporting 2 x8. The resulting link width is 2 x8.

Figure 21: Single Host (2 x8) and Type 2 Add-in Card (Dual Controllers, 2 x8 only)



Figure 15 illustrates a four host baseboard that supports 4 x4 with a single controller add-in card that supports 1 x16, 2 x8 and 4 x4 (Type 4). The PRSTNB[3:0]# state is 0b1011. The BIF[2:0]# state is 0b101 as the end point network controller is forced to bifurcate to 4 x4. The PRSNTB encoding notifies the baseboard that this card is only capable of 1 x16, 2 x8 and 4 x4. The four host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

Figure 22: Four Hosts (4 x4) and Type 4 Add-in Card (Single Controller, 4 x4)



Figure 16 illustrates a four host baseboard that supports 4 x4 with a four controller add-in card that supports 4 x4 (Type 3). The PRSTNB[3:0]# state is 0b1100. The BIF[2:0]# state is 0b111 as there is no need to instruct the end-point network controllers to a specific bifurcation. The PRSNTB encoding notifies the baseboard that this card is only capable of 4 x4. The four host baseboard determines that it is also capable of supporting 4 x4. The resulting link width is 4 x4.

Figure 23: Four Hosts (4 x4) and Type 3 Add-in Card (Four Controllers, 4 x4)



Figure 24: Single Host with no Bifurcation (1 x16) and Type XXX Add-in Card (Two Controllers, 2 x8)

TBD

## PCIe Clocking Topology

Place holder section to discuss clocking requirements; topology (if not previously covered in the pin section)

## (high pri) Power capacity and power delivery

[Editors note: Jon Lewis to contribute; need to get updated Visio diagrams since we removed AUX\_ENABLE from the pin list]

There are four permissible power states: AC Power Off, Management Only Mode, Aux Power Mode (S5), and Main Power Mode (S0). The transition of these states is shown in Figure 13. The main/aux power domains are switched on the baseboard and uses the power pins defined in Table 5.

Figure 25: Baseboard Power Sequencing 

### AC Power Off

In AC power off mode, all power delivery has been turned off or disconnected from the baseboard.

### Management Mode

In Management Only Mode only provides +3.3V Aux for powering up management only functions.

### Aux Power Mode (S5)

In Aux Power Mode provides both +3.3V Aux as well as +12V Aux is available. +12V Aux may be used to deliver power to the add-in card, but only up to the Aux budget.

### Main Power Mode (S0)

In Main Power Mode provides both +3.3V and +12V (Main) across the OCP connector. The add-in card operates in full capacity. Up to 79.2W may be delivered on +12V, and 3.63W on the +3.3V pins.

Figure 26: Baseboard Power Aux/Main Muxing



## (high pri) Timing / sequence of power rails and signals

The following figure shows the power sequence of 3.3V/3.3V\_AUX, 12VMain/Aux relative to AUX\_ENABLE, MAIN\_ENABLE and NIC Power Good.

Figure 27: Baseboard Power Sequencing



# Management

## SMBus Interface

The SMBus provides manageability of the add-in card.

### SMBus I/O Expander

For additional GPIO, an I/O expander may be added to the SMBus on the add-in card. The I/O expander is a 16-bit PCA9575, the I2C address is 0x40/0x41 (8-bit write/read address pair). The I/O expander bit definition is TBD.

## NC-SI Sideband Interface

### NC-SI addressing and Arb#

## MAC Address Requirement

## FRU EEPROM

### Addressing(TBD)

## FW Requirement (TBD)

## Thermal Reporting Interface

# Data Network Requirement

## Network Booting (collect view from OEMs and hyperscale )

Mezzanine NIC shall support network booting in uEFI system environment. Mezzanine NIC shall support both IPv4 and IPv6 network booting.

# Thermal and Environmental

## Environmental Requirements

The specific environment requirement is removed to allow the adoption of OCP Mezzanine NIC in systems with very different thermal requirement and boundary condition.

This Mezzanine card shall meet the same environmental requirements specified in the OCP systems that the Mezzanine card is in. The OCP system that uses OCP Mezzanine card shall define air flow direction, inlet air temperature, air flow (or speed) to the local area where Mezzanine card is at, and simulation boundary.

### Thermal Simulation Boundary Example

**Placeholder for Thermal Simulation Method. Using Facebook Intel® Motherboard V3.0 as example. Not covered by this update.**

## Shock & Vibration

This Mezzanine card shall meet the same shock & vibration requirements specified in updated Facebook OCP Intel® Motherboard V2.0 and V3.0 Design Specification.

## Regulation

This Mezzanine card shall meet CE, CB, FCC Class A, WEEE, ROHS requirements.

# Revision History

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| Author | Description | Revision | Date |
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