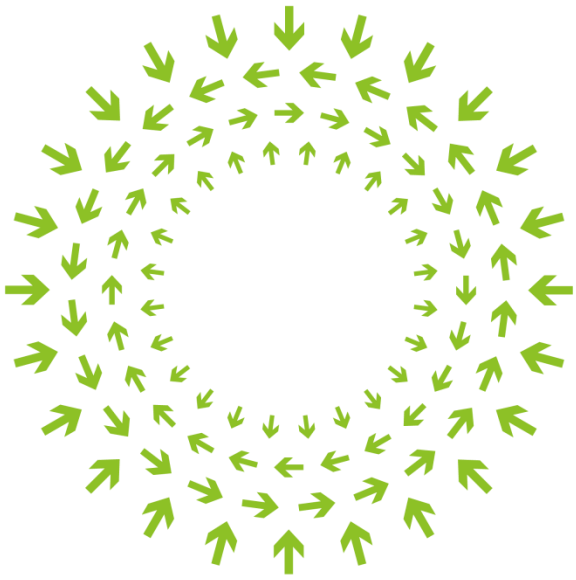

OPEN

Compute Project

OCP Mezzanine card 2.0 Design Specification

Version 1.1~~0100~~.~~95~~

~~Draft~~ Draft

~~for OCP community~~

~~Public review on 2015/11/2~~

Author: Jia Ning, Engineer, Facebook

1 Contents

2 Overview

2.1 License

2.2 Background

The original OCP Mezzanine Card for Intel v2.0 Motherboard specification[1] have been developed mainly to serve the use case of Single and Dual port 10G Ethernet card. Adoption of this specification has been seen in OCP community on different server and storage platforms. Over the recent two years, demand of supporting new use cases were raised and the original Mezzanine card specification cannot support those new use cases without modification in order to support different I/O types, increase bandwidth of data and management, and support higher power controller IC.

Mezzanine card 2.0 specification is developed based on original OCP Mezzanine card. It extends the card mechanical and electrical interface to enable new uses cases for Facebook and other users in OCP community. The extension takes backward compatibility to existing OCP platforms designed for original OCP Mezzanine card specification V0.5 into consideration, and some tradeoffs are made between backward compatibility and new requirements.

2.3 New Use Cases

These new major use cases are taken into consideration in this specification.

- Single and Dual QSFP+ port 40G/50G/100G Ethernet NIC
- Single and Dual SFP+ port 25G Ethernet NIC
- Quad SFP+ Port 10G NIC
- Single, Dual and Quad port 10GBase-T NIC
- x16 PCIe lane to baseboard
- 16x KR to baseboard

[1] http://www.opencompute.org/assets/download/Intel-Mezzanine-Card-Design-Specification-v0.5.pdf

- NIC controller with high TDP that needs more heatsink volume
- Management side band to support use case such as remote System Firmware update
- Baseboard and Mezzanine card identification
- KR Mezzanine card design with low speed and I2C signals that cannot be fit in original OCP Mezzanine
- System design to support x16 PCIe and KR without BOM change
- System design that has more limited vertical space

The Mezzanine card 2.0 specification makes change on as needed base to maximize backward compatibility to existing OCP platforms. Some modification impacts backward compatibility to existing OCP platforms and compatibility check need to be done.

2.4 Major Changes to Form Factor

To accommodate the new uses cases above, major changes to form factor are listed as below. More detailed description can be found in Chapter 3.

- Extend PCB area to support Connector B to baseboard
- Extend PCB area to support I/O interface
- Add option to have I/O on Secondary side to support I/O interface
- Add 12mm stacking option to support higher volume heatsink
- Add 5mm stacking option to support system with limited vertical space
- Add Connector C option for KR Mezz

2.5 Major Changes to Electrical Interface

To accommodate the new uses cases above, major changes to electrical interface are listed as below. More detailed description can be found in chapter 3.83.84

- Modify original 120 pin connector to have NC-SI signals; this is the original OCP Mezzanine card connector; it is referred to Connector A in this specification
- Add 80 pin connector on Mezzanine card interface in order to expend PCIe lane width from x8 to x16; it is referred to Connector B in this specification
- Add 64 pin connector on Mezzanine card interface in order to support KR Mezzanine card design with low speed and I2C signals; it is referred to Connector C in this specification.
- Add card ID mechanism for baseboard to identify different types of Mezzanine cards
- Add definition of thermal reporting interface to support temperature based system fan speed control

3 Mezzanine Card Form Factor

Mezzanine card form factor is described in this chapter. Vendor should refer to 2D DXF and 3D files for dimension, tolerance, and height restriction details.

3.1 Primary and Secondary Side Definition

Primary side and secondary side are used to refer to the two sides of mezzanine card in this document. Primary side is the side with Mezzanine board to board connector. Example of primary side and secondary side is shown in Figure 1Figure 1Figure 1.

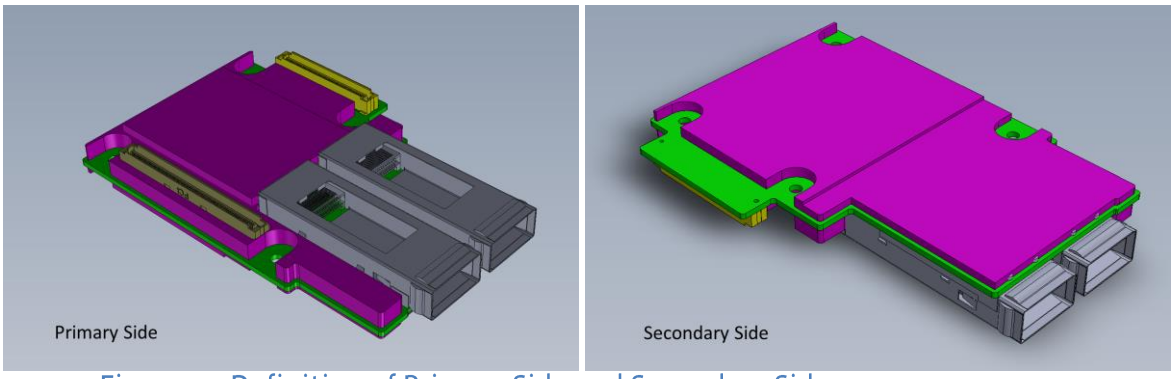

Figure 11: Definition of Primary Side and Secondary Side

3.2 Mezzanine Card Connectors

120 pin Connector A is the original OCP Mezzanine card connector. The pin assignment of Connector A has PCI-E x8 Gen3, I2C and NC-SI side band signals, and power pins. Connector A can also be used for up to 8x KR. Connector A can be used independently.

80 pin Connector B is added in Mezzanine card 2.0 Rev0.40 (initial release). The pin assignment of Connector B has PCI-E x8 Gen3, which can be combined to x16 with Connector A. Connector B can also be used for up to 8x KR. Connector B cannot be used independently and has to be used together with Connector A.

64 pin Connector C is added in Mezzanine card 2.0 Rev0.45. The pin assignment of Connector C has up to 4x KR, their low speed and I2C signals, and power pins. It is created to support the use case of KR only. Connector C can be used independently on Mezzanine card side. The typical KR Mezzanine card implementation with Connector C does not have Connector A and Connector B on card side.

Vendor shall refer to table below for the connector part number in different stack height for Connector A, B and C.

	Mezzanine card (5mm stack)	Mezzanine card (8/12mm stack)	Baseboard (5/8mm stack)	Baseboard (12mm stack)
Connector A	FCI/61083-121402LF	FCI/61083-124402LF	FCI/61082-121402LF	FCI/61082-122402LF
Connector B	FCI/61083-081402LF	FCI/61083-084402LF	FCI/61082-081402LF	FCI/61082-082402LF
Connector C	FCI/10135584-641402LF	FCI/10135584-644402LF	FCI/10135583-641402LF	FCI/10135583-642402LF

Baseboard can implement the following connector options:

- Connector A only for up to PCIe Gen3 x8
- Connector A and B for up to PCIe Gen3 x16, or up to 16x KR, or a combination of PCIe and KR
- Connector C only for up to 4x KR and low-speed and I2C signals
- Connector A, B and C for up to x16 PCIe, plus up to 4x KR, with low-speed and I2C signals

Connector A and Connector B is shown in Figure 2Figure 2Figure 2, viewing from secondary side. Connector C is shown in Figure 3 , viewing from primary side.

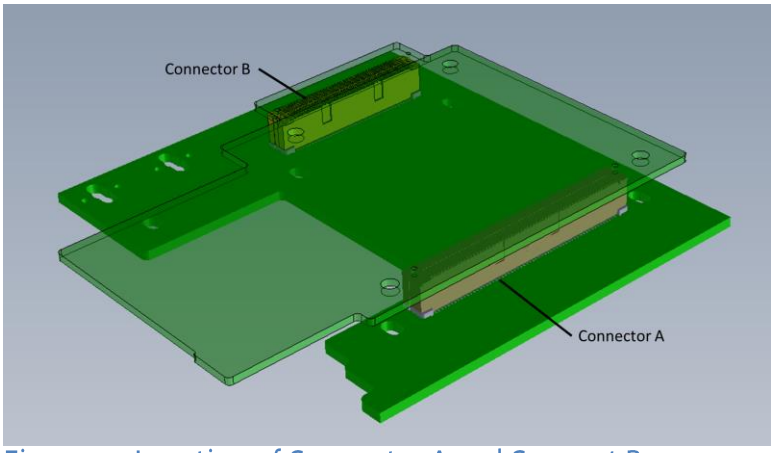

Figure 22: Location of Connector A and Connect B

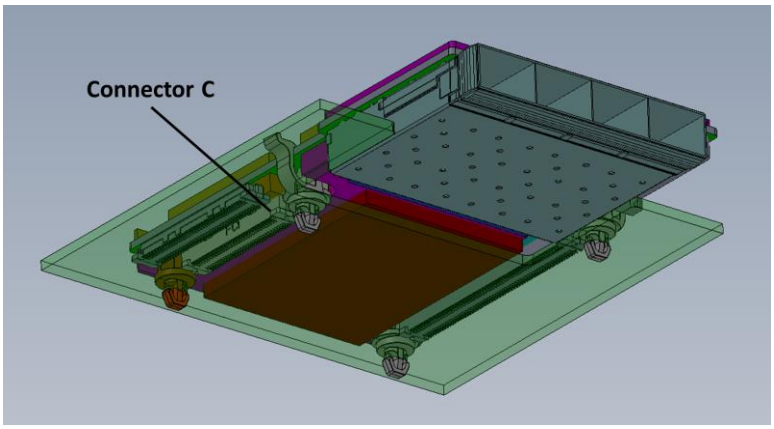

Figure 33: Location of Connector C

3.3 Form Factor Definition in Horizontal Plane

This section defines the Mezzanine card form factor in horizontal direction, i.e. from top or bottom view.

Figure 4 shows the horizontal plane of the original OCP Mezzanine Card for Intel v2.0 Motherboard specification as a reference.

For OCP Mezzanine card 2.0, there are two optional PCB areas, and the usage depends on the connection needed for host interface side, and I/O. Figure 5Figure 5Figure 5 illustrates Mezzanine PCB from primary side with two optional PCB area shown.
By default vendor should implement the Mezzanine card in form factor in Figure 6Figure 6Figure 6. In order to maximize
The mechanical compatibility to existing platforms, vendors should not extend Mezzanine card PCB to the optional areas unless the extension is necessary to achieve the purposes mentioned below in this section.

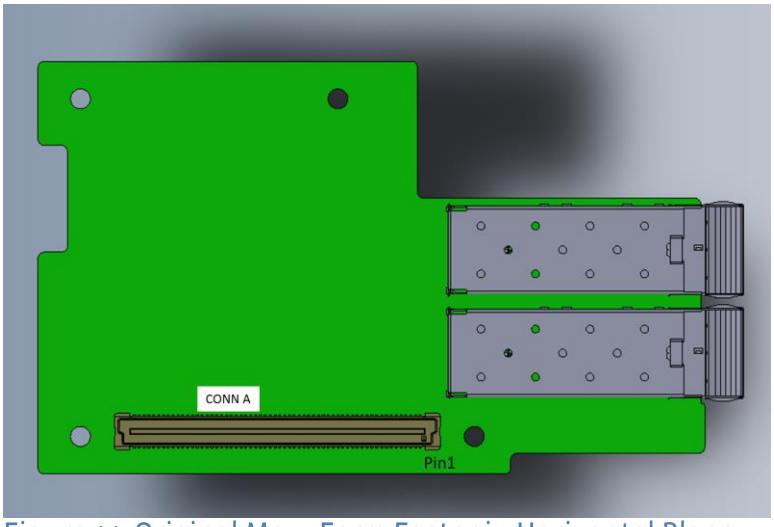

Figure 44: Original Mezz Form Factor in Horizontal Plane

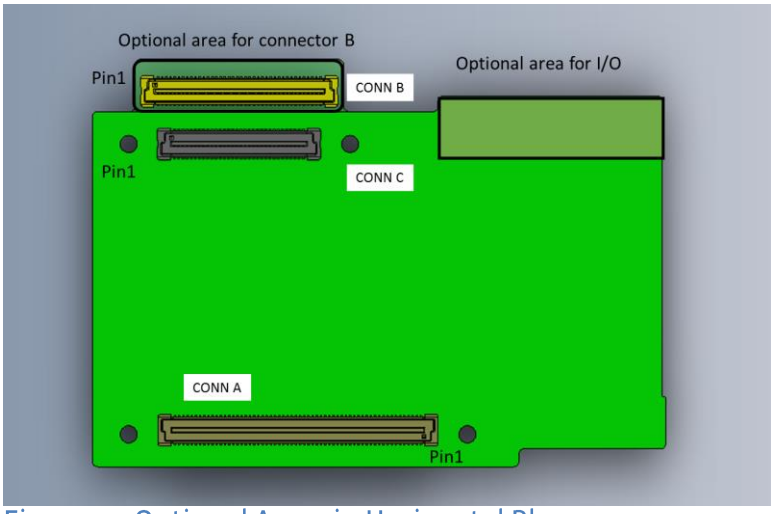

Figure 55: Optional Areas in Horizontal Plane

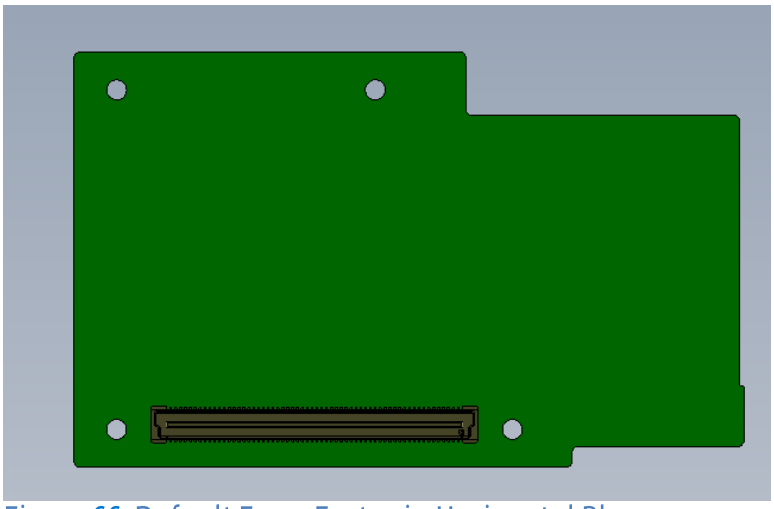

Figure 66: Default Form Factor in Horizontal Plane

3.3.1 Optional Area for Connector B

This area is extended to increase channels or lanes to baseboard.

Connector B is an 80 pin connector (FCI/61083-084402) and provides extra x8 PCIe lanes (or 8x KR for KR Mezzanine card), PERST# signals and clocks. Definition of the Connector B is in Chapter 4.2.

Mezzanine card that only uses signals in Connector A should not extend PCB to this area.

Mezzanine card that uses more than x8 PCIe lane should extend PCB to this area.

3.3.2 Optional Area for I/O

This area is extended to accommodate more I/O types.

Mezzanine cards with Single/Dual port 10G/25G SFP+, Single/Dual port RJ45, Single/Dual port 40G/50G/100G QSFP+/QFSFP28 is preferred to follow implementation examples and not extend PCB to optional I/O area. Extending PCB to optional I/O area may break compatibility of existing platforms, extra caution shall be taken to check mechanical design in system.

Mezzanine card that uses 4x 10G/25G SFP+ ports or 4x 10G Base-T ports is allowed to extend PCB to this area to accommodate I/O connector placement. By doing so, it may break mechanical compatibility of existing platforms.

3.3.3 Connector C Area

For KR Mezzanine card, a 64 pin connector C is used to provide interconnect to board.

For PCIe Mezzanine card, vendor may use the area of Connector C for component placement. The component height shall stay within the height restriction of updated 3D.

There is a mechanical change in Rev0.45 spec update for height restriction near connector area to allow Mezzanine card without connector C to be plugged into Baseboard with Connector C (3.7mm) at 8mm stack-up use case. Therefore, the height restriction is reduced from 4.5mm in Rev0.40 Specification to 4mm in the area around Connector C. it is shown as New in Figure 7.

For all new Mezzanine card 2.0 design, it is strongly recommend to consider taking 4mm height limitation to be compatible to future baseboards with Connector C populated.

For existing Mezzanine card 1.0 and 2.0 design with component exceeding than 4mm but lower than 4.5mm, system and baseboard vendors are responsible for checking the mechanical confliction, and depopulate Connector C on baseboard side.

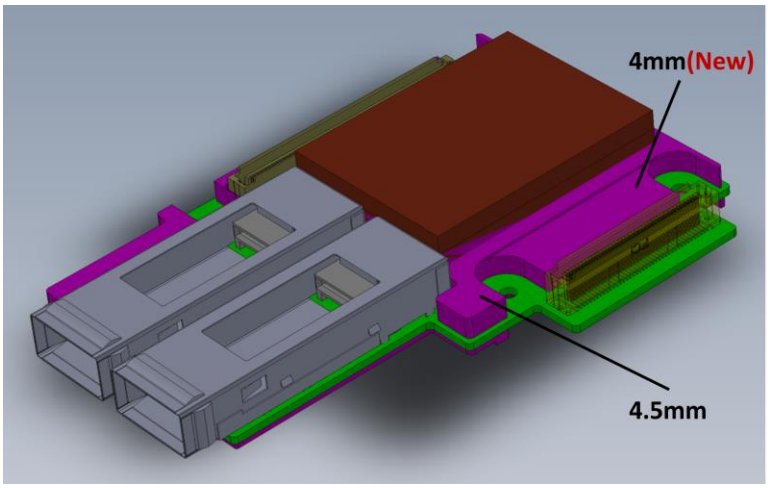

Figure 77: New reduced keep out in Rev0.45 Specification

3.4 Form Factor Vertical Stack Definition

There are 4 options to implement mezzanine card with different placement height restriction, I/O connectors' location, and mezzanine connector stacking height to baseboard.

A front view of the types are shown in Figure 8Figure 8Figure 8, Figure 9Figure 9Figure 9, and Figure 10Figure 10Figure 10, and Figure 11 and Figure 12: Type 5 Vertical Stack Front View for Type 1, 2, 3, 4, 5 vertical stack.

Type 1 is the original OCP Mezzanine 1.0 stack with 8mm stacking. This is also the most widely adopted stacking Type. The baseboard needs to have a cut out with in the I/O area since most network connector is taller than 8mm.

Type 2 is based on Type 1, but change stacking to 12mm for taller heatsink. Baseboard and system does not have strict height constrain can take this stacking with the benefit to avoid have cut out in baseboard, and having taller heatsink on Mezzanine card side.

Type 3 is to allow the placement of controller IC on the secondary side with 8mm stacking.

Type 4 is enabled in Mezzanine 2.0 Rev0.45 for 5mm stacking. It is for system with most strict height constrain. Since the Mezzanine card heatsink is 7.5mm and network connectors are taller than 5mm, a cut out is required on baseboard to avoid confliction of Mezzanine card heatsink and connector to baseboard. The cut out size on baseboard is larger to support Type 4 stack, comparing to support the original Type 1 stack. Besides, baseboard need to provide clearance under the mezzanine card's 4mm/4.5mm component keep out area.

Type 5 is based on Type 2, but ASIC is on secondary side and allow up to 42mm tall heatsink. Baseboard and system that has ample space on secondary side can take this stacking with the benefit of allowing high power ASIC and/or more efficient cooling solution.

For Figure 8~~Figure 8~~~~Figure 8~~ and Figure 9~~Figure 9~~~~Figure 9~~, it shows a possible placement of 4xQSFP+/QSFP28 connectors. This it is not a current use case; the placement has manufacture concern due to using belly to belly placement of QSFP+/QSFP28 cage on 1.57mm PCB. It may need a customized QSFP+/QSFP28 connector for the use case of 4xQSFP+/QSFP28.

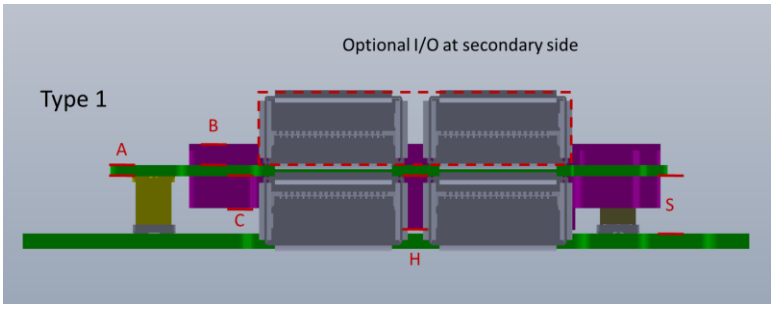

Figure ~~8~~8: Type 1 Vertical Stack Front View

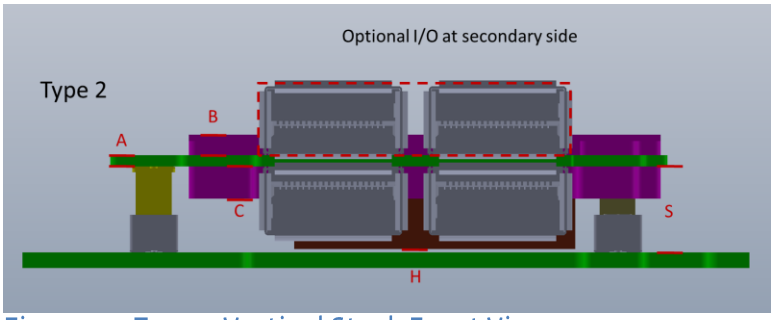

Figure ~~9~~9: Type 2 Vertical Stack Front View

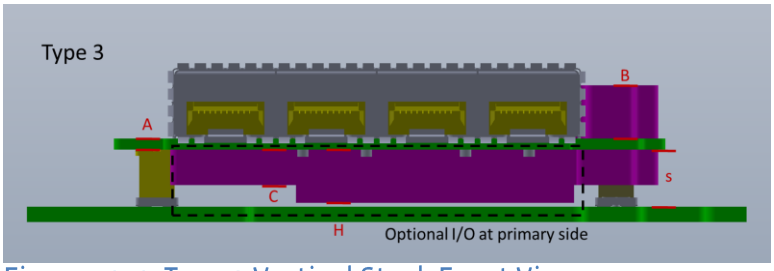

Figure ~~10~~10: Type 3 Vertical Stack Front View

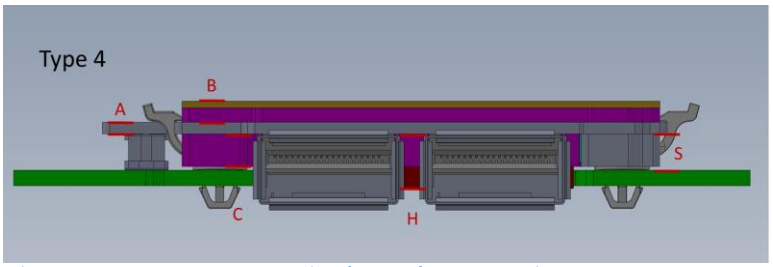

Figure ~~11~~11: Type 4 Vertical Stack Front View

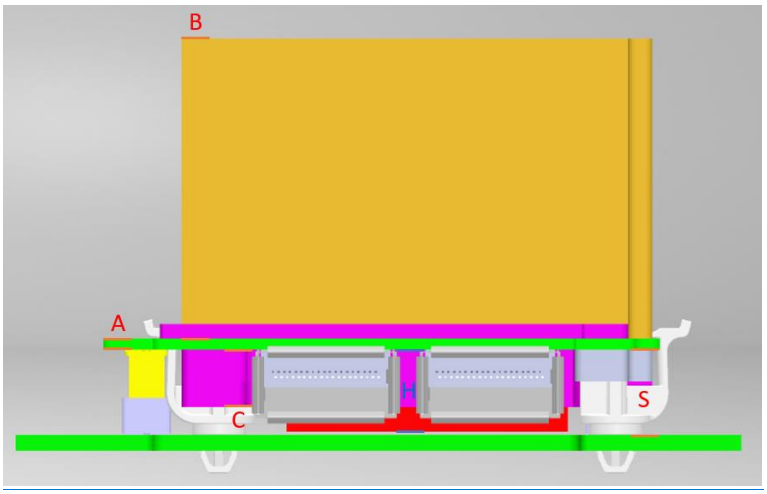

Figure 12: Type 5 Vertical Stack Front View

A summary of major dimension and height restriction across 3 types are shown in Table 1 ~~Table 1~~ ~~Table 1~~.

Table 1: Mezzanine Card Vertical Stack Types Dimension Comparison

TYPE	A(typ)	B(max)	C(max)	H(max)	S(typ)	I/O	Controller IC
TYPE 1	1.57mm	2.9mm /2.0mm	4.5mm /4mm	7.5mm	8mm	Primary side /Secondary side optional	Primary side
TYPE 2	1.57mm	2.9mm /2.0mm	4.5mm /4mm	11.5mm	12mm	Primary side /Secondary side optional	Primary side
TYPE 3	1.57mm	7.5mm	4.5mm /4mm	7.5mm	8mm	Primary side optional /Secondary side	Primary side/ secondary side
TYPE~~ype~~ 4	1.57mm	2.9mm /2mm	4.5mm /4mm	7.5mm	5mm	Primary side /Secondary side optional	Primary side
TYPE 5	1.57mm	42mm /2mm	4.5mm /4mm	11.5mm	12mm	Primary side /Secondary side optional	Secondary side

Figure 13~~Figure 12~~Figure 12 describes the connector selection for baseboard and mezzanine card to achieve different vertical stack types.[2]

[2] Refer to complete drawing for more detail for Connector A and Connector B:
http://portal.fciconnect.com/Comergent//fci/drawing/61082.pdf (Receptacle-Baseboard side)
http://portal.fciconnect.com/Comergent//fci/drawing/61083.pdf (Plug-Mezzanine card)
Link with drawing of connector C will be updated in future release.

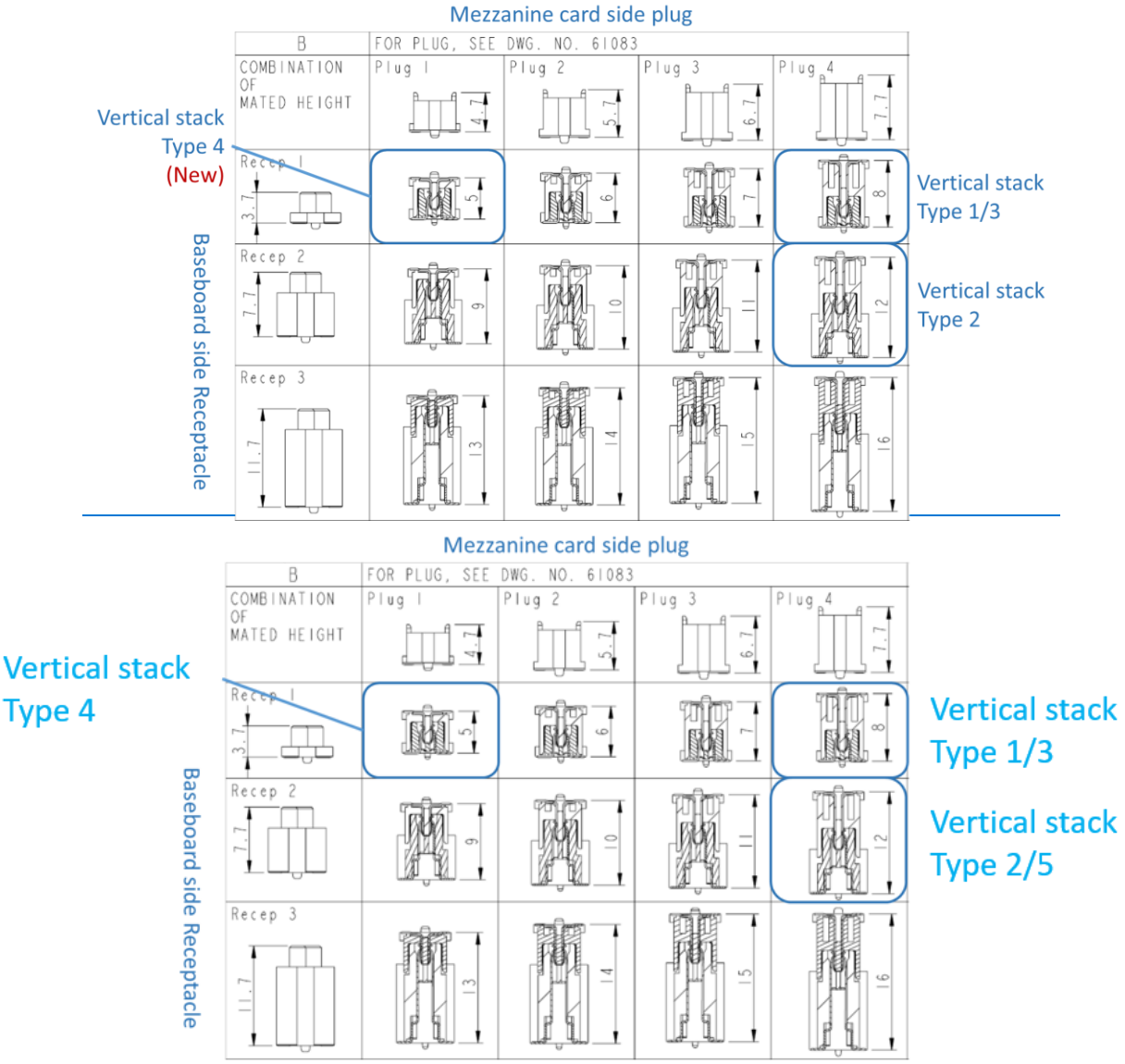

Figure 13~~12~~: Mezzanine Connector Selection Matrix

3.5 Implementation Examples

This section gives examples of Mezzanine 2.0 implementation. The implementation is not limited to the examples given here as long as it follows the specification.

Table 2: Mezzanine card implementation examples

	Description	Network Port Shown	Mezzanine card Connectors			Baseboard Connectors			Vertical Stacking	Heatsink keepout Height	File name
			A	B	C	A	B	C			
ID	PCIe Mezz NIC										
P1	Single/Dual ports 10G/25G SFP+/SFP28	2x SFP+/SFP28	X	N/A	N/A	X	X	X	Type 1(8mm)	7.5mm	P1_T1_10G_SFP+_25G_SFP28_10232015
P2	Single/Dual ports 40G QSFP	2x QSFP+	X	N/A	N/A	X	X	X	Type 1(8mm)	7.5mm	P2_T1_40G_QSFP+_10232015
P3	Single/Dual ports 50G/100G QSFP28_B	2x SFF-8672(QSFP+ 28Gbps Style B)	X	X	N/A	X	X	X	Type 1(8mm)	7.5mm	P3_T1_50G_100G_QSFP28_B_10232015
P4	Single/Dual ports 50G/100G QSFP28_A	2x SFF-8662(QSFP+ 28Gbps Style A)	X	X	N/A	X	X	X	Type 1(8mm)	7.5mm	P4_T1_50G_100G_QSFP28_A_10232015
P5	Single/Dual ports 50G/100G QSFP28_B	2x SFF-8672(QSFP+ 28Gbps Style B)	X	X	N/A	X	X	X	Type 2(12mm)	11.5mm	P5_T2_50G_100G_QSFP28_B_10232015
P6	Quad ports 10G/25G SFP+	1x 1x4 SFP+	X	X	N/A	X	X	X	Type 3 (8mm)	7.5mm	P6_T3_4x10G_4xSFP+_10232015
P7	Single/Dual ports 50G/100G QSFP28_B	2x SFF-8672(QSFP+ 28Gbps Style B)	X	X	N/A	X	X	X	Type 4(5mm)	7.5mm	P7_T4_50G_100G_QSFP28_B_10232015
P8	Single/Dual ports 50G/100G QSFP28_A	2x SFF-8662(QSFP+ 28Gbps Style A)	X	X	N/A	X	X	X	Type 4(5mm)	7.5mm	P8_T4_50G_100G_QSFP28_A_10232015
P9	Single/Dual ports 10G/25G SFP+/SFP28	2x SFP+/SFP28	X	N/A	N/A	X	X	X	Type 4(5mm)	7.5mm	P9_T4_10G_SFP+_25G_SFP28_10232015
	KR Mezz										
K1	4x KR Mezz in Connector A+B	1x QSFP	X	X	N/A	X	X	X	Type 2(12mm)	11.5mm	K1_T2_4x10G_QSFP+_10232015
K2	Quad SFP+ KR Mezz in Connector C	1x 1x4 SFP+	N/A	N/A	X	X	X	X	Type 1(8mm)	7.5mm	K2_T1_4x10G_4xSFP+_10232015
K3	Quad 10GBaseT KR Mezz in Connector C	1x 1x4 RJ45	N/A	N/A	X	X	X	X	Type 1(8mm)	7.5mm	K3_T1_4x10G_4xRJ45_10232015
K4	Quad SFP+ KR Mezz in Connector C	1x 1x4 SFP+	N/A	N/A	X	X	X	X	Type 2(12mm)	11.5mm	K4_T2_4x10G_4xSFP+_10232015
K5	Quad 10GBaseT KR Mezz in Connector C	1x 1x4 RJ45	N/A	N/A	X	X	X	X	Type 2(12mm)	11.5mm	K5_T2_4x10G_4xRJ45_10232015
	Max Mezz Profile										
M1	Max Mezz Profile of all Type 1		X	X	X	X	X	X	Type 1(8mm)	7.5mm	TBD
M2	Max Mezz Profile of all Type 2		X	X	X	X	X	X	Type 2(12mm)	11.5mm	TBD

	Description	Network Port Shown	Mezzanine card Connectors shown			Baseboard Connectors shown			Vertical Stacking	Heatsink keepout Height	File name
			A	B	C	A	B	C			
ID	PCIe Mezz NIC										
P1	Single/Dual ports 10G/25G SFP+/SFP28	2x SFP+/SFP28	X	N/A	N/A	X	X	X	Type 1(8mm)	7.5mm	P1_T1_10G_SFP+_25G_SFP28_10232015
P2	Single/Dual ports 40G QSFP	2x QSFP+	X	N/A	N/A	X	X	X	Type 1(8mm)	7.5mm	P2 T1_40G_QSFP+10232015
P3	Single/Dual ports 50G/100G QSFP28_B	2x SFF-8672(QSFP+ 28Gbps Style B)	X	X	N/A	X	X	X	Type 1(8mm)	7.5mm	P3 T1_50G100G_QSFP2813_10232015
P4	Single/Dual ports 50G/100G QSFP28_A	2x SFF-8662(QSFP+ 28Gbps Style A)	X	X	N/A	X	X	X	Type 1(8mm)	7.5mm	P4 T1_50G_100G_QSFP28_A_10232015
P5	Single/Dual ports 50G/100G QSFP28_B	2x SFF-8672(QSFP+ 28Gbps Style B)	X	X	N/A	X	X	X	Type 2(12mm)	11.5mm	P5 T2_50G100G_QSFP2813_10232015
P6	Quad ports 10G/25G SFP+	lx 1x4 SFP+	X	X	N/A	X	X	X	Type 3 (8mm)	7.5mm	P6 T3_4x10G_4xSFP+_10232015
P7	Single/Dual ports 50G/100G QSFP28_B	2x SFF-8672(QSFP+ 28Gbps Style B)	X	X	N/A	X	X	N/A	Type 4(5mm)	7.5mm	P7 T4_50G100G_QSFP2813_11172015
P8	Single/Dual ports 50G/100G QSFP28_A	2x SFF-8662(QSFP+ 28Gbps Style A)	X	X	N/A	X	X	N/A	Type 4(5mm)	7.5mm	P8 T4_50G_100G_QSFP28_A_11172015
P9	Single/Dual ports 10G/25G SFP+/SFP28	2x SFP+/SFP28	X	N/A	N/A	X	X	N/A	Type 4(5mm)	7.5mm	P9_T4_10G_SFP+_25G_SFP28_11172015
P10	Single/Dual ports 50G/100G QSFP28_B	2x SFF-8662(QSFP+ 28Gbps Style B)	X	X	X	X	X	X	Type 5(12mm)	42.0mm	P10_T5_50G_100G_QSFP28_B_08302019
	KR Mezz										
K1	4x KR Mezz in Connector A+13	lx QSFP	X	X	N/A	X	X	X	Type 2(12mm)	11.5mm	K1 T2_4x10G_QSFP+_10232015
K2	Quad SFP+ KR Mezz in Connector C	lx 1x4 SFP+	N/A	N/A	X	X	X	X	Type 1(8mm)	7.5mm	K2 T1_4x10G_4xSFP+_10232015
K3	Quad 10GBaseT KR Mezz in Connector C	lx 1x4 RJ45	N/A	N/A	X	X	X	X	Type 1(8mm)	7.5mm	K3 T1_4x10G_4xRJ45_10232015
K4	Quad SFP+ KR Mezz in Connector C	lx 1x4 SFP+	N/A	N/A	X	X	X	X	Type 2(12mm)	11.5mm	K4 T2_4x10G_4xSFP+_10232015
K5	Quad 10GBaseT KR Mezz in Connector C	lx 1x4 R145	N/A	N/A	X	X	X	X	Type 2(12mm)	11.5mm	K5_T2_4x10G_4xR145_10232015
	Max Mezz Profile										
M1	Max Mezz Profile of all Type 1		X	X	X	X	X	X	Type 1(8mm)	7.5mm	MI_TI_MM MEZZ PROFILE_20151130
M2	Max Mezz Profile of all Type 2		X	X	X	X	X	X	Type 2(12mm)	11.5mm	M2_T2_MM MEZZ PROFILE_20151130

	Description	Network Port Shown	Mezzanine card Connectors shown			Baseboard Connectors shown			Vertical Stacking	Heatsink keepout Height	File name
			A	B	C	A	B	C			
ID	PCIe Mezz NIC										
P1	Single/Dual ports 10G/25G SFP+/SFP28	2x SFP+/SFP28	X	N/A	N/A	X	X	X	Type 1(8mm)	7.5mm	P1_T1_10G_SFP+_25G_SFP28_10232015
P2	Single/Dual ports 40G QSFP	2x QSFP+	X	N/A	N/A	X	X	X	Type 1(8mm)	7.5mm	P2_T1_40G_QSFP+_10232015
P3	Single/Dual ports 50G/100G QSFP28_B	2x SFF-8672(QSFP+ 28Gbps Style B)	X	X	N/A	X	X	X	Type 1(8mm)	7.5mm	P3_T1_50G_100G_QSFP28_B_10232015
P4	Single/Dual ports 50G/100G QSFP28_A	2x SFF-8662(QSFP+ 28Gbps Style A)	X	X	N/A	X	X	X	Type 1(8mm)	7.5mm	P4_T1_50G_100G_QSFP28_A_10232015
P5	Single/Dual ports 50G/100G QSFP28_B	2x SFF-8672(QSFP+ 28Gbps Style B)	X	X	N/A	X	X	X	Type 2(12mm)	11.5mm	P5_T2_50G_100G_QSFP28_B_10232015
P6	Quad ports 10G/25G SFP+	1x 1x4 SFP+	X	X	N/A	X	X	X	Type 3 (8mm)	7.5mm	P6_T3_4x10G_4xSFP+_10232015
P7	Single/Dual ports 50G/100G QSFP28_B	2x SFF-8672(QSFP+ 28Gbps Style B)	X	X	N/A	X	X	N/A	Type 4(5mm)	7.5mm	P7_T4_50G_100G_QSFP28_B_11172015
P8	Single/Dual ports 50G/100G QSFP28_A	2x SFF-8662(QSFP+ 28Gbps Style A)	X	X	N/A	X	X	N/A	Type 4(5mm)	7.5mm	P8_T4_50G_100G_QSFP28_A_11172015
P9	Single/Dual ports 10G/25G SFP+/SFP28	2x SFP+/SFP28	X	N/A	N/A	X	X	N/A	Type 4(5mm)	7.5mm	P9_T4_10G_SFP+_25G_SFP28_11172015
	KR Mezz										
K1	4x KR Mezz in Connector A+B	1x QSFP	X	X	N/A	X	X	X	Type 2(12mm)	11.5mm	K1_T2_4x10G_QSFP+_10232015
K2	Quad SFP+ KR Mezz in Connector C	1x 1x4 SFP+	N/A	N/A	X	X	X	X	Type 1(8mm)	7.5mm	K2_T1_4x10G_4xSFP+_10232015
K3	Quad 10GBaseT KR Mezz in Connector C	1x 1x4 RJ45	N/A	N/A	X	X	X	X	Type 1(8mm)	7.5mm	K3_T1_4x10G_4xRJ45_10232015
K4	Quad SFP+ KR Mezz in Connector C	1x 1x4 SFP+	N/A	N/A	X	X	X	X	Type 2(12mm)	11.5mm	K4_T2_4x10G_4xSFP+_10232015
K5	Quad 10GBaseT KR Mezz in Connector C	1x 1x4 RJ45	N/A	N/A	X	X	X	X	Type 2(12mm)	11.5mm	K5_T2_4x10G_4xRJ45_10232015
	Max Mezz Profile										
M1	Max Mezz Profile of all Type 1		X	X	X	X	X	X	Type 1(8mm)	7.5mm	M1_T1_MAX MEZZ PROFILE_20151130
M2	Max Mezz Profile of all Type 2		X	X	X	X	X	X	Type 2(12mm)	11.5mm	M2_T2_MAX MEZZ PROFILE_20151130

The 3D screen shots shown below is to illustrate the design. Vendor should follow 3D models for detail height restrictions.

Some implementations may ~~results~~result in mechanical conflict with existing OCP platforms. It may trigger modification of mechanical design, or limitation on configuration. System vendors are responsible to perform system mechanical check when planning to use or enable a Mezzanine 2.0 with existing OCP platforms, or enabling a new Mezzanine 2.0 card.

M1 and M2 are the overlay of all typical Type 1 and Type 2 mezzanine card implementations explicitly listed in Table 2. M1 and M2 are NOT the maximal profile of all possible mezzanine card implementations.

System and baseboard vendors may take M1 and M2 as a reference for mechanical compatibility of different mezzanine card implementations. This does NOT replace the mechanical check of mezzanine card to system compatibility during planning, designing, and validation.

3.5.1 Single/Dual Port SFP+ 10G/SFP28 25G Ethernet Mezzanine Card (Type 1)

This is the original OCP 10G Mezzanine card. Specification can be found at the link below as "OCP Mezzanine card v0.5, original defacto standard, V0.5":
http://www.opencompute.org/wiki/Server/SpecsAndDesigns#OCP_Mezzanine_Cards

3.5.2 Dual QSFP+ Port 40G Mezzanine Card (Type 1)

This is a single/dual port QSFP+, 40G Ethernet Mezzanine card. Depopulate 2nd port makes it a single port 40G Ethernet Mezzanine card. For single port card which need extra space for component placement, placement of component in the volume of 2nd QSFP+ port is allowed.

On the primary side, there is a component height restriction of 4mm, 4.5mm and 7.5mm. The 7.5mm height restriction area is intended for heatsink of controller IC; placement of components other than controller IC and heatsink is allowed in this area. 7.5mm max height makes this card fit Type 1 vertical stack, with 8mm stack height. 4mm height restriction is applied in the area around connector C allow Mezzanine card to be used in baseboard with Connector A/B/C populated at the same time. Other areas are with 4.5mm height restriction on primary side.

On the secondary side, there is a component height restriction of 2.0mm and 2.9mm in different areas.

As the electrical interface to baseboard, connector A and connector B provide up to x16 PCIe connection. Connector A is mandatory for this SKU. Connector B provides extra x8 PCIe lanes. Connector B is optional for this SKU.

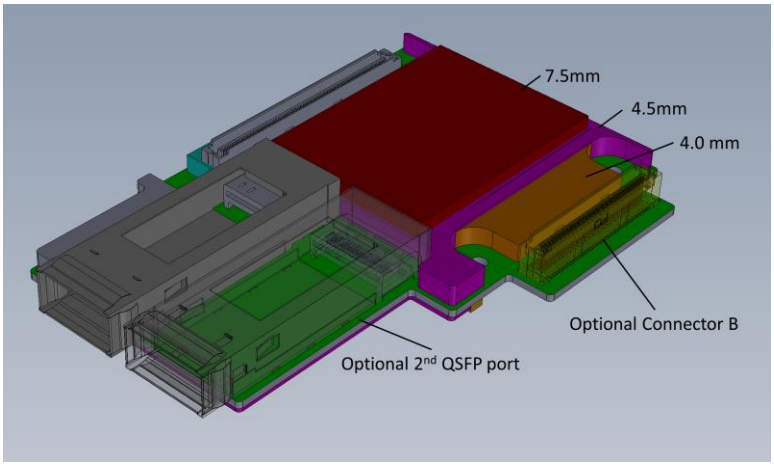

Figure 1413: Primary side veiw of dual port QSFP+ Mezzanine card

3.5.3 Dual QSFP+ Port 40G Mezzanine card (Type 2)

Due to the 8mm stack limitation in Type 1 vertical stack, heat sink height is limited to 7.5mm max and may not be able to provide sufficient cooling to some controller IC. Type 2 vertical stack allows 11.5mm max for heatsink and provide more freedom to thermal design.

This implementation has limitation in system mechanical compatibility due to taking extra volume. Vendor may need to modify mechanical design in order to support it.

Vendor should plan the components in the 11.5mm heatsink area accordingly, if there is a plan to use BOM option to make Type 2 vertical stack fit into Type 1 vertical stack.

The Mezzanine connector is the same for Type 1 and Type 2 on the mezzanine card side. Baseboard side need to use different connectors to support different stacking height for Type 1 and Type 2 as described in section 3.4.

Screen capture of an implementation example is shown in Figure 15~~Figure 14~~.

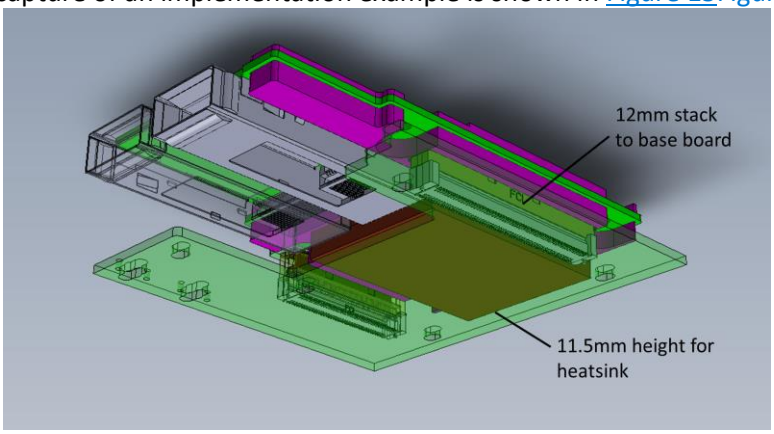

Figure 15~~14~~: Dual Port QSFP+ Mezzanine card mounted on a baseboard with 12mm stacking height

Dual port 50G/100G QSFP28 implementation may share same mechanical with this implementation, and discussed in section 3.5.7~~3.5.6~~.

3.5.4 Quad SFP+ port 10G Mezzanine card (Type 3)

Quad SFP+ port 10G Mezzanine card can be implement in Type 3 vertical stack up as shown in Figure 16~~Figure 15~~Figure 15 and Figure 17~~Figure 16~~Figure 16.

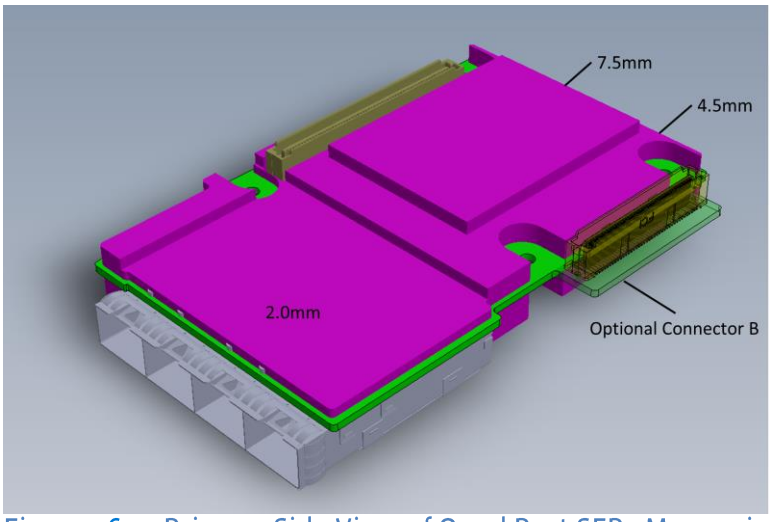

Figure 1615: Primary Side View of Quad Port SFP+ Mezzanine Card

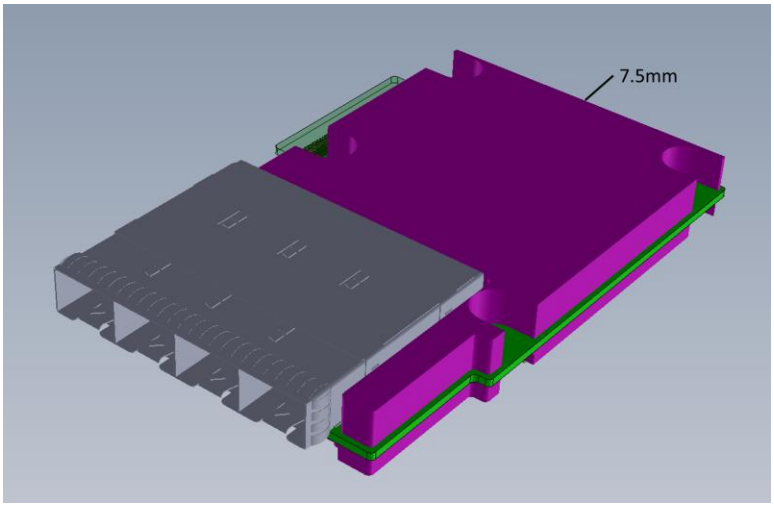

Figure 1716: Secondary Side View of Quad Port SFP+ Mezzanine Card

3.5.5 Quad port 10G Base-T Mezzanine Card (Type 3)

Quad 10G Base-T Mezzanine card can be implement in Type 3 vertical stack up as shown in Figure 18Figure 17Figure 17 and Figure 19Figure 18Figure 18.

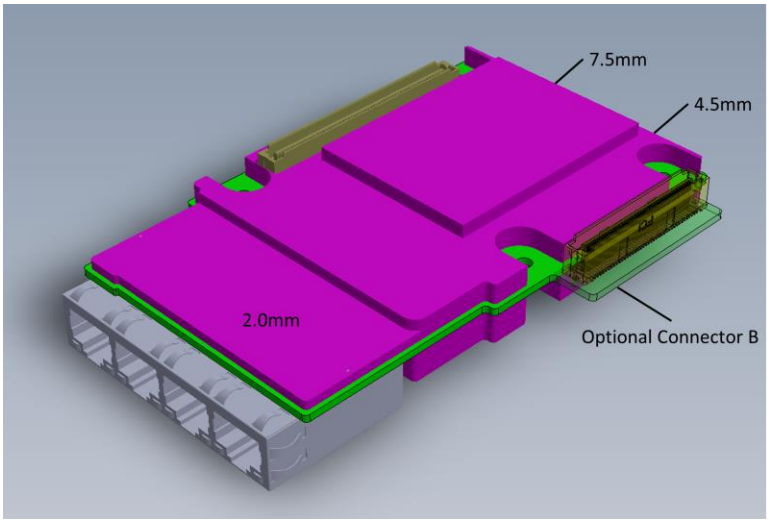

Figure 18~~17~~: Primary Side View of Quad port 10G Base-T Mezzanine card

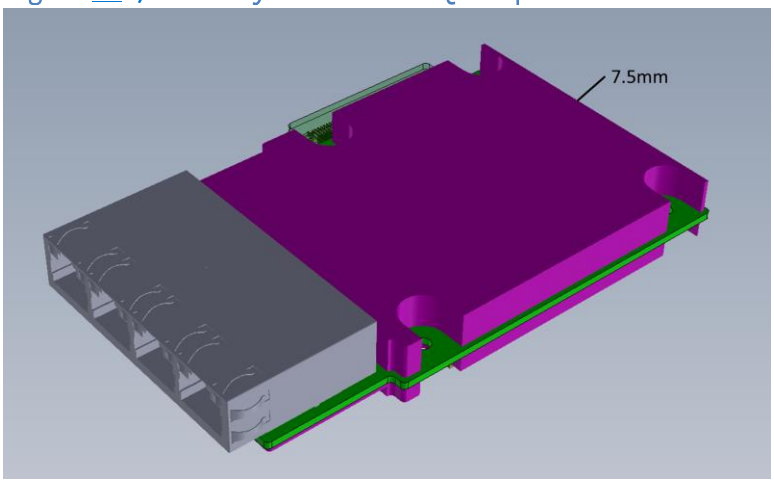

Figure 19~~18~~: Secondary Side View of Quad port 10G Base-T Mezzanine card

3.5.6 Single/Dual QSFP+ Port Mezzanine card with ASIC on secondary side (Type 5)

Single/Dual QSFP+ Port Mezzanine card with ASIC on secondary size can be implemented in Type 5 vertical stack up as shown in Figure 20: Primary Side View of Single port Type 5 Mezzanine card and Figure 21: Secondary Side View of Single port Type 5 Mezzanine card.

Type 5 form factor is largest of Mezz 2.0 form factor till date. System integrator should be aware that system designed for Type 1, 2, 3 or 4, may or may not fit Type-5 NIC.

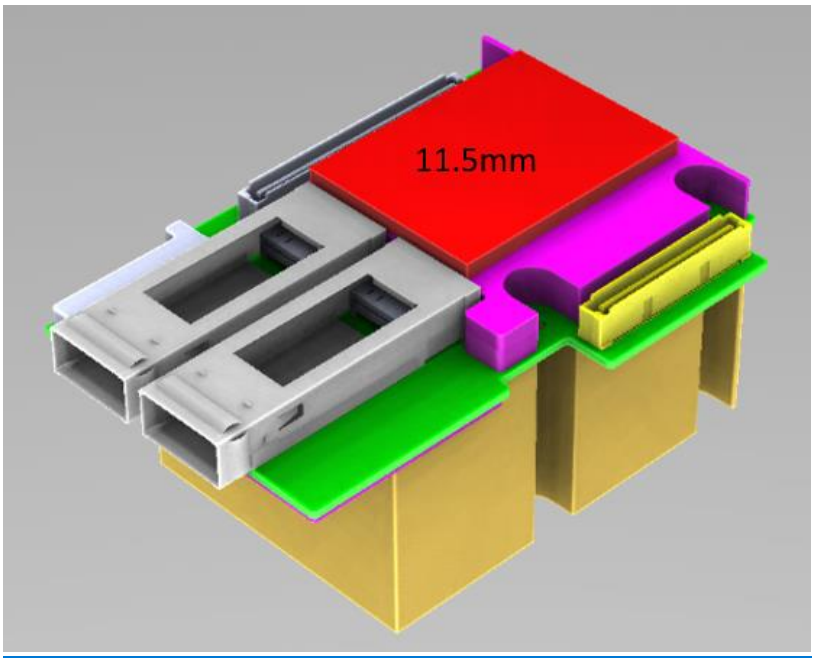

Figure 20: Primary Side View of Single port Type 5 Mezzanine card

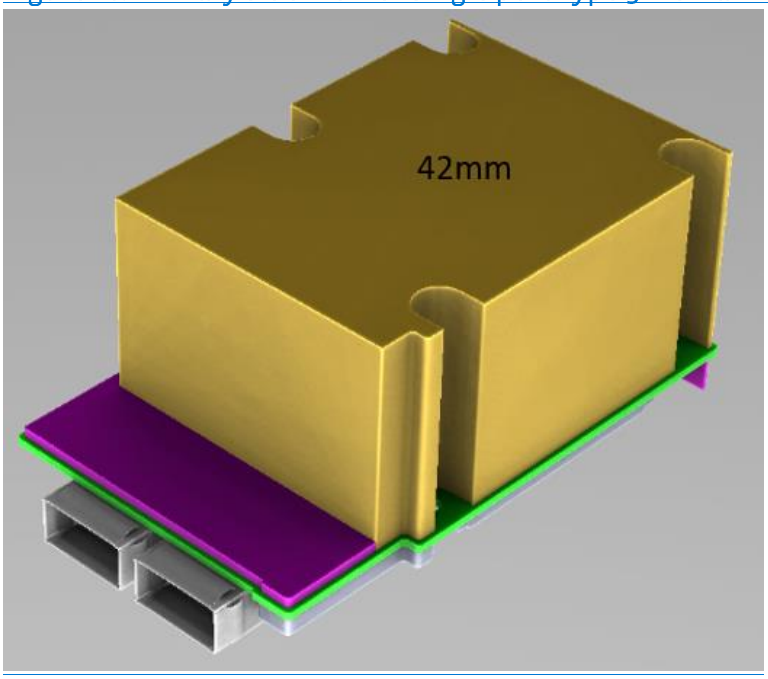

Figure 21: Secondary Side View of Single port Type 5 Mezzanine card

3.5.63.5.7 Dual Port QSFP28 Style A/Style B 50G/100G Mezzanine Card (Type 1)

Based on Dual QSFP+ Port 40G Mezzanine card (Type 1), 50G/100G connection is supported in this implementation.

For 50G and 100G, QSFP+ connector need to be replaced by either SFF-8672(QSFP+ 28Gbps Style B) or SFF-8662(QSFP+ 28Gbps Style A) QSFP28 connector.

SFF-8672(QSFP+ 28Gbps Style B) has the same size cage as QSFP+ and the placement of SFF-8672(QSFP+ 28Gbps Style B) is same as QSFP+.

SFF-8662(QSFP+ 28Gbps Style A) has a larger SMT connector, and the cage is 2.19mm longer than QSFP+. The placement of SFF-8662(QSFP+ 28Gbps Style A) Cage keeps the location of cage pin at rear side same as QSFP+; The SMT post and front edge of SFF-8662(QSFP+ 28Gbps Style A) has a 2.19mm shift compare to QSFP+. The placement is to avoid a deeper cutoff in baseboard for backward compatibility to baseboards designed for 40G QSFP+ application.

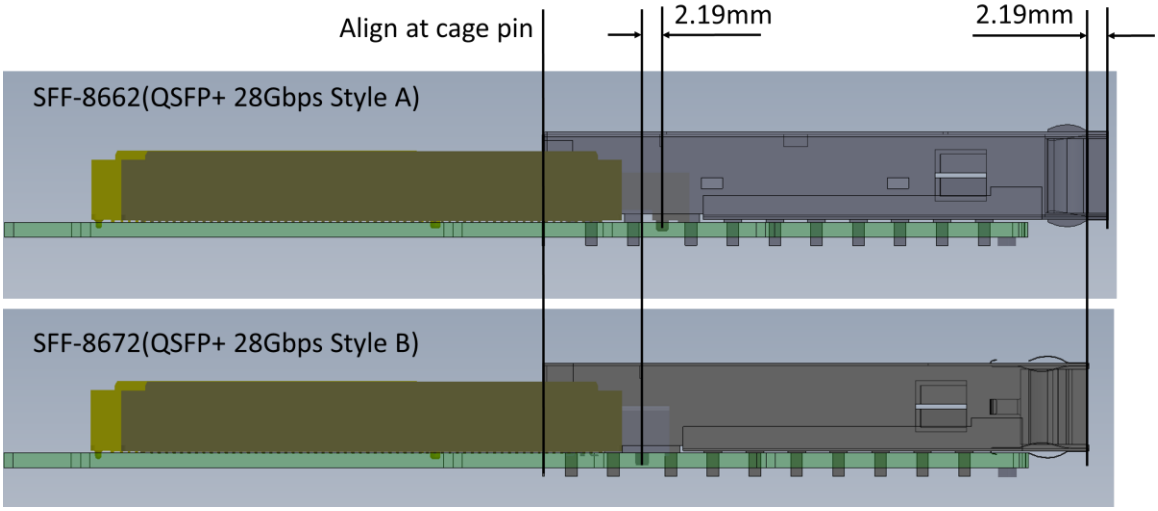

Figure 2219: Placement of QSFP+ 28Gbps Type A and Type B

For 50G in QSFP28 connector, Lane 1 and Lane 2 out of Lane 1,2,3,4 shall be used.

3.5.73.5.8 Quad Port 10GBaseT RJ45 KR Mezzanine card with Connector C (Type 2)

This implementation has 4x KR interfaces to baseboard, with low speed and I2C signals. On network side, it is able to support up to 4x RJ45 10GBaseT.

Due to lack of industry standard, the RJ45 10GBaseT connector may have different mechanical dimension. The using of 10GBaseT connectors other than the one used in this example is allowed, as long as the mezzanine card PCB size stays with the horizontal plane defined in section 3.3.

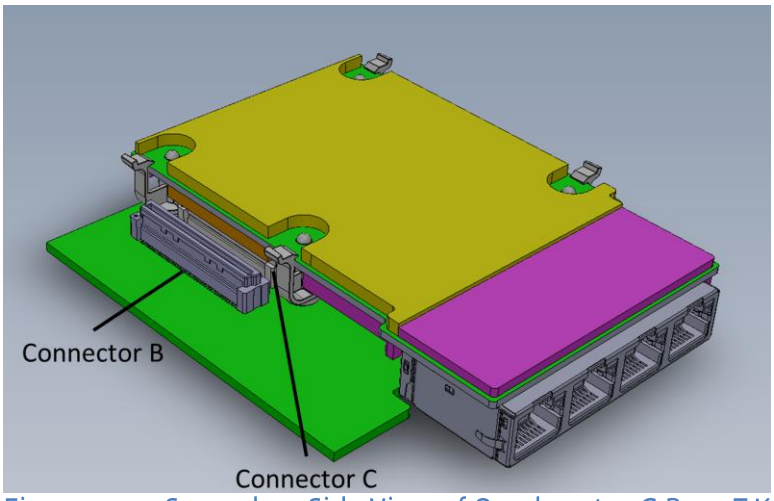

Figure 2320: Secondary Side View of Quad port 10G Base-T KR Mezzanine Card

3.5.83.5.9 Quad Port 10G SFP+ KR Mezzanine card with Connector C (Type 2)

This implementation has 4x KR interfaces to baseboard, with low speed and I2C signals. On network side, it is able to support up to 4x 10G in SFP+.

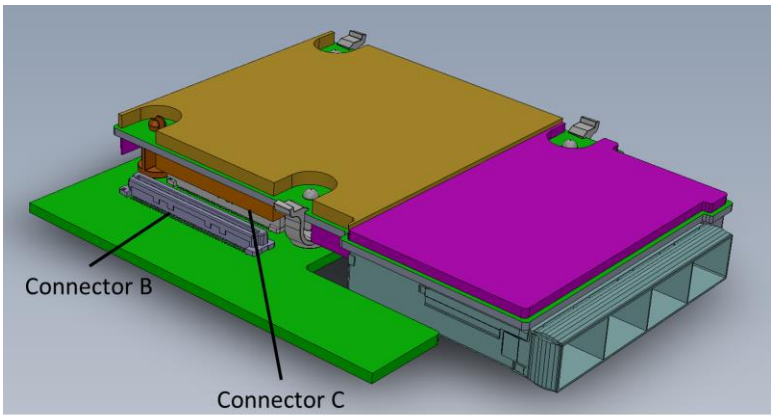

Figure 2421: Secondary Side View of Quad port 10G SFP+ KR Mezzanine Card

3.6 Port and LED Location

This section defines network side port location of a few typical implementations. It also includes the LED information for SFP+/SFP28 and QSFP+/QSFP28 since the OCP Mezzanine card does not have light pipe in cage in typical application.

3.6.1 Port and LED location for Single/Dual SFP+/SFP28 Mezzanine card

The port and LED location is shown in Figure 25Figure 22 for single and dual port SFP+/SFP28 Mezzanine card.

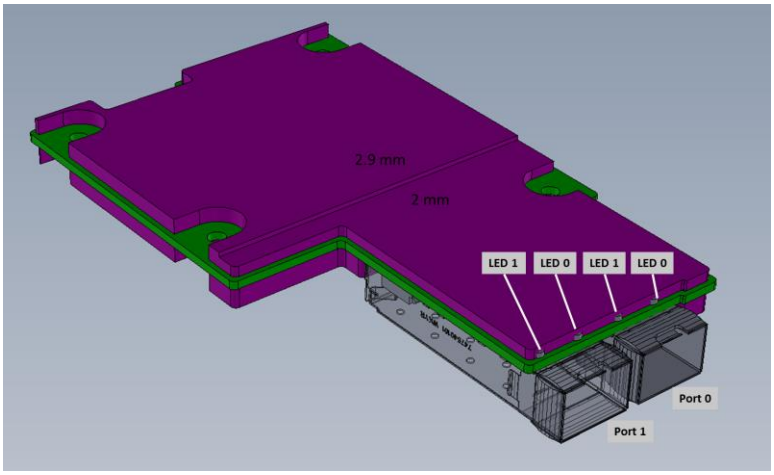

Figure 2522: Single/Dual SFP+/SFP28 port Mezzanine card port and LED location

Port 0 and Port1 each has 2 LEDs to indicate link status and speed. The definition is as below:
LED0: Physical link speed (Green/Yellow dual color)
Green Stay on- physical link on with highest rated speed
Yellow stay on- physical link on with degraded speed
Off- physical link off

LED1: Logic Link/Activity, Green
Green Stay on- logic link up, no activity
Green blinking- logic link up, activity
Off- logic link off

3.6.2 Port and LED location for PCIe/KR QSFP+/QSFP28 Mezzanine card

The port and LED location is shown in Figure 26Figure 23Figure 23 for single and dual port QSFP+/QSFP28 Mezzanine card. Mezzanine card can depopulated Port 1 to become a single port card.

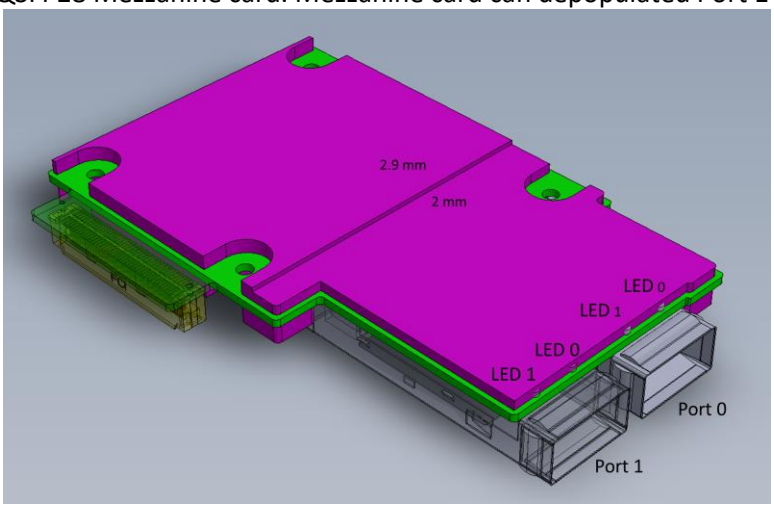

Figure 2623: Single/Dual QSFP/QSFP28 port Mezzanine card port and LED location

Port 0 and Port1 each has 2 LEDs to indicate link status and speed. The definition is as below:

LED0: Physical link speed (Green/Yellow dual color)
Green Stay on- physical link on with highest rated speed
Yellow stay on- physical link on with degraded speed
Off- physical link off

LED1: Logic Link/Activity, Green
Green Stay on- logic link up, no activity
Green blinking- logic link up, activity
Off- logic link off

3.6.3 Port and LED location for 4x KR interfaces via a single QSFP+ cage

The LED location is shown in Figure 27~~Figure 24~~ for the use case of having 4x KR lanes in one QSFP+ cage.

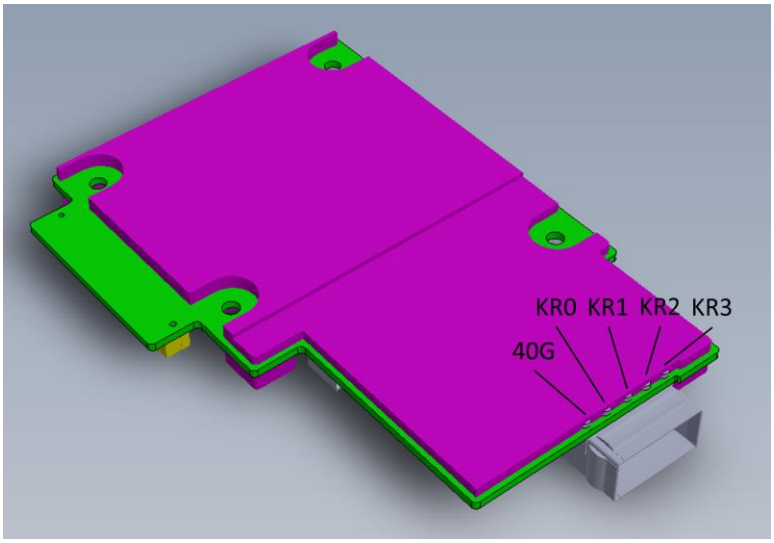

Figure 27~~24~~: 4x KR Mezzanine card port and LED location

KR0/KR1/KR2/KR3 LED (Green):
Off- No link
On- Link as one 10G port
Blink- Link as one 10G port with activity

40G LED (Green):
Off- No link
On- Link as one 40G port
Blink- Link as one 40G port with activity

3.6.4 Port and LED location for Quad RJ45 Mezzanine card

The port and LED location is shown in Figure 28~~Figure 25~~ for the use case of quad RJ45 ports Mezzanine card. The example here shows the RJ45 with build in LED.

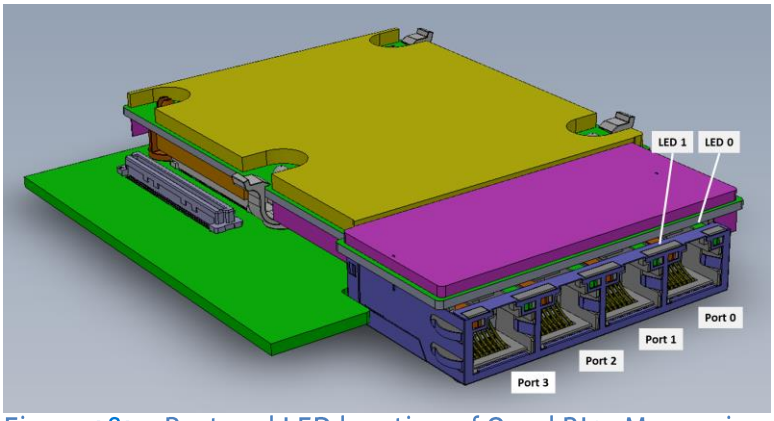

Figure 2825: Port and LED location of Quad RJ45 Mezzanine card

Each port has 2 LEDs to indicate link status and speed. The definition is as below:

LED0: Physical link speed (Green/Yellow dual color)
Green Stay on- physical link on with highest rated speed
Yellow stay on- physical link on with degraded speed
Off- physical link off

LED1: Logic Link/Activity, Green
Green Stay on- logic link up, no activity
Green blinking- logic link up, activity
Off- logic link off

Another option to implement LED with Quad Port RJ45 is to design in LED on Mezzanine card, in the similar with as the LED for other Mezzanine card.

3.7 MAC Address label requirement

MAC address label(s) must be scannable when Mezzanine card is installed in server, rack, etc. by system vendor, rack integrator, and DC user without interrupt of normal operation.

For 2x MAC addresses, 2x 2D bar codes and 2x human readable texts for MAC address need to be placed within 10mm from Mezzanine card PCB edge as shown in Figure 29Figure 26.

For 3x MAC addresses, 3x 2D bar codes and 3x human readable texts for MAC address need to be placed within 18mm from Mezzanine card PCB edge.

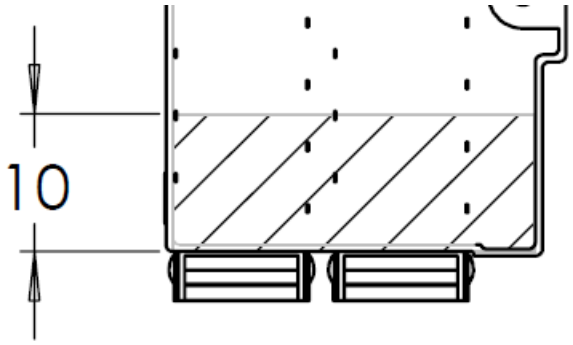

Figure 2926: MAC address label placement

The scanned bar code should not include ".". Example: "AA.BB.CC.00.11.20" should scan as "AABBCC001120". Implementation example is shown in Figure 30Figure 27.

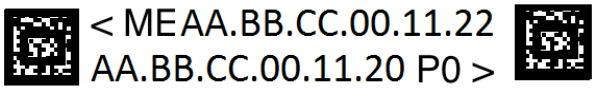

Figure 3027: MAC address label implementation example

3.8 Plastic Insulation Sheet

A plastic Insulation sheet is preferred to be used to protect the secondary side from short circuit with chassis metal or other components. When a plastic insulation sheet is used, the thickness of plastic insulation sheet shall be included in the Mezzanine card vertical height restriction, and shall not exceed the maximum profile in this specification and 3D models.

Plastic Insulation sheet shall not block any labeling for visual identification and scanning.

4 Mezzanine Card to Baseboard Electrical Interface

4.1 Power Capability and Status on Connector

Baseboard supplies power to power pins on Mezzanine card connectors. The current capability and power status is as the table below. Normal power is available at on state S0 only. Auxiliary power is available at all power states including hibernate state S4 or off state S5.

The tables below is to define the maximum current for each rail. The thermal capability of system and thermal requirements of the mezzanine card shall be evaluated while planning the usage of current capability of rails.

Table 3: Power Pins on Connector A

Power Rail	Voltage Tolerance	# of pins	Current Capability	Status
P12V_AUX/P12V	±8%(max)	3	2.4A	Auxiliary Power/Normal Power
P5V_AUX	±9%(max)	3	2.4A	Auxiliary power
P3V3_AUX	±5%(max)	2	1.6A	Auxiliary power
P3V3	±5%(max)	8	6.4A	Normal power

Table 4: Power Pins on Connector B

Power Rail	Voltage Tolerance	# of pins	Current Capability	Status
P12V_AUX/P12V	±8%(max)	2	1.6A	Auxiliary Power/Normal Power

Table 5: Power Pins on Connector C

Power Rail	Voltage Tolerance	# of pins	Current Capability	Status
P12V_AUX/P5V_AUX-P12V	±8%(max)	3	2.4A	Auxiliary Power/Normal Power

To accommodate systems without P12V_AUX, two special mixed power rails are defined: P12V_AUX/P12V for Connector A and B, and P12V/P12V_AUX/P5V_AUX for Connector C. Detail implementation guide and compatibility limitation is as below:

Table 6: Baseboard Implementation Matrix for Mezzanine Connector Power Pins

	Baseboard with P12V_AUX (Preferred implementation)	**Baseboard without P12V_AUX**
Connector A A61, A62, A63	P12V_AUX @all power states	Power off @S4/S5 P12V@S0
Connector B B41, B42	P12V_AUX @all power states	Power off @S4/S5 P12V@S0
Connector C C33, C34, C35	P12V_AUX @all power states	P5V_AUX@S4/S5 P12V@S0 Baseboard side implement Diode-OR from P5V_AUX and P12V to supply power to pin C33, C34, C35
Compatibility	Compatible with all mezzanine card power pins implementation	Compatible with mezzanine card with preferred power pins implementation

Table 7: Prefered Power Pins Implementation of Mezzanine card

	Mezzanine card With Connector A or A+B	**Mezzanine card With Connector C**
Connector A A61, A62, A63	Diode-OR with P5V_AUX on connector A, then regulate down to other rails. VR shall cover Vin range accordingly and be able to track the Vin transition between 12V and 5V	N/A
Connector B B41, B42	Same net as A61, A62, A63	N/A
Connector C C33, C34, C35	N/A	Regulate from P12V_AUX/P5V_AUX-P12V down to other rails.

		VR shall cover Vin range accordingly and be able to track the Vin transition between 12V and 5V
Compatibility	Compatible with all Types of baseboard with Connector A or A+B	Compatible with all Types of baseboard with Connector C

Table 8: Legacy Implementation of Mezzanine Card and Compatibility Limitation

	Mezzanine card With Connector A and/or B	**Mezzanine card With Connector C**
Connector A A61, A62, A63	P12V_AUX	N/A
Connector B B41, B42	Same net as A61, A62, A63	N/A
Connector C C33, C34, C35	N/A	P12V_AUX
Compatibility	May not work with baseboard without P12V_AUX	Does not work with baseboard without P12V_AUX

4.2 Pin Definition of Mezzanine Connector

4.2.1 x16 PCIe Mezzanine Card with Connector A and B

Pin definition of a mezzanine card with up to x16 PCIe lanes is in Table 9Table 9Table 9. The direction of the signals are from the perspective of the baseboard.

For mezzanine card with x8 or less PCIe lanes, only Connector A is required. Connector B and its optional PCB area should not be implemented as mentioned in 3.3.1.

Table 9: x16 PCIe Mezzanine Card Pin Definition

Connector A				**Connector B**			
Signal	**Pin**	**Pin**	**Signal**	**Signal**	**Pin**	**Pin**	**Signal**
P12V_AUX/P12V	A61	A1	MEZZ_PRSNTA1_N /BASEBOARD_A_ID	P12V_AUX/P12V	B41	B1	MEZZ_PRSNTB1_N /BASEBOARD_B_ID
P12V_AUX/P12V	A62	A2	P5V_AUX	P12V_AUX/P12V	B42	B2	GND
P12V_AUX /P12V	A63	A3	P5V_AUX	RSVD	B43	B3	MEZZ_RX_DP<8>
GND	A64	A4	P5V_AUX	GND	B44	B4	MEZZ_RX_DN<8>
GND	A65	A5	GND	MEZZ_TX_DP<8>	B45	B5	GND
P3V3_AUX	A66	A6	GND	MEZZ_TX_DN<8>	B46	B6	GND
GND	A67	A7	P3V3_AUX	GND	B47	B7	MEZZ_RX_DP<9>
GND	A68	A8	GND	GND	B48	B8	MEZZ_RX_DN<9>
P3V3	A69	A9	GND	MEZZ_TX_DP<9>	B49	B9	GND
P3V3	A70	A10	P3V3	MEZZ_TX_DN<9>	B50	B10	GND
P3V3	A71	A11	P3V3	GND	B51	B11	MEZZ_RX_DP<10>
P3V3	A72	A12	P3V3	GND	B52	B12	MEZZ_RX_DN<10>
GND	A73	A13	P3V3	MEZZ_TX_DP<10>	B53	B13	GND
LAN_3V3STB_ALERT_N	A74	A14	NCSI_CRSDV	MEZZ_TX_DN<10>	B54	B14	GND
SMB_LAN_3V3STB_CLK	A75	A15	NCSI_RCLK	GND	B55	B15	MEZZ_RX_DP<11>
SMB_LAN_3V3STB_DAT	A76	A16	NCSI_TXEN	GND	B56	B16	MEZZ_RX_DN<11>
PCIE_WAKE_N	A77	A17	PERST_N0	MEZZ_TX_DP<11>	B57	B17	GND
NCSI_RXER	A78	A18	MEZZ_SMCLK	MEZZ_TX_DN<11>	B58	B18	GND

GND	A79	A19	MEZZ_SMDATA	GND	B59	B19	MEZZ_RX_DP<12>
NCSI_TXD0	A80	A20	GND	GND	B60	B20	MEZZ_RX_DN<12>
NCSI_TXD1	A81	A21	GND	MEZZ_TX_DP<12>	B61	B21	GND
GND	A82	A22	NCSI_RXD0	MEZZ_TX_DN<12>	B62	B22	GND
GND	A83	A23	NCSI_RXD1	GND	B63	B23	MEZZ_RX_DP<13>
CLK_100M_MEZZ0_DP	A84	A24	GND	GND	B64	B24	MEZZ_RX_DN<13>
CLK_100M_MEZZ0_DN	A85	A25	GND	MEZZ_TX_DP<13>	B65	B25	GND
GND	A86	A26	CLK_100M_MEZZ1_DP	MEZZ_TX_DN<13>	B66	B26	GND
GND	A87	A27	CLK_100M_MEZZ1_DN	GND	B67	B27	MEZZ_RX_DP<14>
MEZZ_TX_DP_C<0>	A88	A28	GND	GND	B68	B28	MEZZ_RX_DN<14>
MEZZ_TX_DN_C<0>	A89	A29	GND	MEZZ_TX_DP<14>	B69	B29	GND
GND	A90	A30	MEZZ_RX_DP<0>	MEZZ_TX_DN<14>	B70	B30	GND
GND	A91	A31	MEZZ_RX_DN<0>	GND	B71	B31	MEZZ_RX_DP<15>
MEZZ_TX_DP_C<1>	A92	A32	GND	GND	B72	B32	MEZZ_RX_DN<15>
MEZZ_TX_DN_C<1>	A93	A33	GND	MEZZ_TX_DP<15>	B73	B33	GND
GND	A94	A34	MEZZ_RX_DP<1>	MEZZ_TX_DN<15>	B74	B34	GND
GND	A95	A35	MEZZ_RX_DN<1>	GND	B75	B35	CLK_100M_MEZZ2_DP
MEZZ_TX_DP_C<2>	A96	A36	GND	GND	B76	B36	CLK_100M_MEZZ2_DN
MEZZ_TX_DN_C<2>	A97	A37	GND	CLK_100M_MEZZ3_DP	B77	B37	GND
GND	A98	A38	MEZZ_RX_DP<2>	CLK_100M_MEZZ3_DN	B78	B38	PERST_N1
GND	A99	A39	MEZZ_RX_DN<2>	GND	B79	B39	PERST_N2
MEZZ_TX_DP_C<3>	A100	A40	GND	MEZZ_PRSNTB2_N	B80	B40	PERST_N3
MEZZ_TX_DN_C<3>	A101	A41	GND				
GND	A102	A42	MEZZ_RX_DP<3>				
GND	A103	A43	MEZZ_RX_DN<3>				
MEZZ_TX_DP_C<4>	A104	A44	GND				
MEZZ_TX_DN_C<4>	A105	A45	GND				
GND	A106	A46	MEZZ_RX_DP<4>				
GND	A107	A47	MEZZ_RX_DN<4>				
MEZZ_TX_DP_C<5>	A108	A48	GND				
MEZZ_TX_DN_C<5>	A109	A49	GND				
GND	A110	A50	MEZZ_RX_DP<5>				
GND	A111	A51	MEZZ_RX_DN<5>				
MEZZ_TX_DP_C<6>	A112	A52	GND				
MEZZ_TX_DN_C<6>	A113	A53	GND				
GND	A114	A54	MEZZ_RX_DP<6>				
GND	A115	A55	MEZZ_RX_DN<6>				
MEZZ_TX_DP_C<7>	A116	A56	GND				
MEZZ_TX_DN_C<7>	A117	A57	GND				
GND	A118	A58	MEZZ_RX_DP<7>				
GND	A119	A59	MEZZ_RX_DN<7>				
MEZZ_PRSNTA2_N	A120	A60	GND				

For x16 PCIe, lane 0~7 is mapped to connector A and lane 8~15 is mapped to connector B.

For the case of multiple root ports are connected to Mezzanine interface on baseboard, or the case of multiple end points are connected to Mezzanine interface on Mezzanine card, follow bifurcation rule as showing in Table 10.

Table 10: Bifuracation rule of PCIe in connector A and Connect B

Bifurcation		Lane numbering															
# of ports	lane/port	*Pin 1 Connector A								*Pin 1 Connector B							
1	x16	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
2	x8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
1	x8	0	1	2	3	4	5	6	7								
4	x4	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
2	x4	0	1	2	3	0	1	2	3								
1	x4	0	1	2	3												
8	x2	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
4	x2	0	1	0	1	0	1	0	1								
2	x2	0	1	0	1												
16	x1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

4.2.2 16x KR Mezzanine card with Connector A and B

Pin definition of a Mezzanine card with up to 16 KR lanes from a baseboard. There are PHY or retimer on this Mezzanine card for connecting to rack level network.

Pin definition of 16x KR Mezzanine card is shown in Table 11~~Table 11~~~~Table 11~~. The direction of the signals are from the perspective of the baseboard.

Table 11: 16x KR Mezzanine Card Pin Definition

Connector A				Connector B			
Signal	**Pin**	**Pin**	**Signal**	**Signal**	**Pin**	**Pin**	**Signal**
P12V_AUX/P12V	A61	A1	MEZZ_PRSNTA1_N /BASEBOARD_A_ID	P12V_AUX/P12V	B41	B1	MEZZ_PRSNTB1_N /BASEBOARD_B_ID
P12V_AUX/P12V	A62	A2	P5V_AUX	P12V_AUX/P12V	B42	B2	GND
P12V_AUX /P12V	A63	A3	P5V_AUX	RSVD	B43	B3	KR_RX_DP<0>
GND	A64	A4	P5V_AUX	GND	B44	B4	KR_RX_DN<0>
GND	A65	A5	GND	KR_TX_DP<0>	B45	B5	GND
P3V3_AUX	A66	A6	GND	KR_TX_DN<0>	B46	B6	GND
GND	A67	A7	P3V3_AUX	GND	B47	B7	KR_RX_DP<1>
GND	A68	A8	GND	GND	B48	B8	KR_RX_DN<1>
P3V3	A69	A9	GND	KR_TX_DP<1>	B49	B9	GND
P3V3	A70	A10	P3V3	KR_TX_DN<1>	B50	B10	GND
P3V3	A71	A11	P3V3	GND	B51	B11	KR_RX_DP<2>
P3V3	A72	A12	P3V3	GND	B52	B12	KR_RX_DN<2>
GND	A73	A13	P3V3	KR_TX_DP<2>	B53	B13	GND
LAN_3V3STB_ALERT_N	A74	A14	NCSI_CRSDV	KR_TX_DN<2>	B54	B14	GND
SMB_LAN_3V3STB_CLK	A75	A15	NCSI_RCLK	GND	B55	B15	KR_RX_DP<3>
SMB_LAN_3V3STB_DAT	A76	A16	NCSI_TXEN	GND	B56	B16	KR_RX_DN<3>
RSVD	A77	A17	RSVD	KR_TX_DP<3>	B57	B17	GND
NCSI_RXER	A78	A18	MEZZ_SMCLK	KR_TX_DN<3>	B58	B18	GND
GND	A79	A19	MEZZ_SMDATA	GND	B59	B19	KR_RX_DP<4>
NCSI_TXD0	A80	A20	GND	GND	B60	B20	KR_RX_DN<4>
NCSI_TXD1	A81	A21	GND	KR_TX_DP<4>	B61	B21	GND
GND	A82	A22	NCSI_RXD0	KR_TX_DN<4>	B62	B22	GND
GND	A83	A23	NCSI_RXD1	GND	B63	B23	KR_RX_DP<5>
RSVD	A84	A24	GND	GND	B64	B24	KR_RX_DN<5>
RSVD	A85	A25	GND	KR_TX_DP<5>	B65	B25	GND
GND	A86	A26	RSVD	KR_TX_DN<5>	B66	B26	GND

GND	A87	A27	RSVD	GND	B67	B27	KR_RX_DP<6>
KR_TX_DP<8>	A88	A28	GND	GND	B68	B28	KR_RX_DN<6>
KR_TX_DN<8>	A89	A29	GND	KR_TX_DP<6>	B69	B29	GND
GND	A90	A30	KR_RX_DP<8>	KR_TX_DN<6>	B70	B30	GND
GND	A91	A31	KR_RX_DN<8>	GND	B71	B31	KR_RX_DP<7>
KR_TX_DP<9>	A92	A32	GND	GND	B72	B32	KR_RX_DN<7>
KR_TX_DN<9>	A93	A33	GND	KR_TX_DP<7>	B73	B33	GND
GND	A94	A34	KR_RX_DP<9>	KR_TX_DN<7>	B74	B34	GND
GND	A95	A35	KR_RX_DN<9>	GND	B75	B35	RSVD
KR_TX_DP<10>	A96	A36	GND	GND	B76	B36	RSVD
KR_TX_DN<10>	A97	A37	GND	RSVD	B77	B37	GND
GND	A98	A38	KR_RX_DP<10>	RSVD	B78	B38	RSVD
GND	A99	A39	KR_RX_DN<10>	GND	B79	B39	RSVD
KR_TX_DP<11>	A100	A40	GND	MEZZ_PRSNTB2_N	B80	B40	RSVD
KR_TX_DN<11>	A101	A41	GND				
GND	A102	A42	KR_RX_DP<11>				
GND	A103	A43	KR_RX_DN<11>				
KR_TX_DP<12>	A104	A44	GND				
KR_TX_DN<12>	A105	A45	GND				
GND	A106	A46	KR_RX_DP<12>				
GND	A107	A47	KR_RX_DN<12>				
KR_TX_DP<13>	A108	A48	GND				
KR_TX_DN<13>	A109	A49	GND				
GND	A110	A50	KR_RX_DP<13>				
GND	A111	A51	KR_RX_DN<13>				
KR_TX_DP<14>	A112	A52	GND				
KR_TX_DN<14>	A113	A53	GND				
GND	A114	A54	KR_RX_DP<14>				
GND	A115	A55	KR_RX_DN<14>				
KR_TX_DP<15>	A116	A56	GND				
KR_TX_DN<15>	A117	A57	GND				
GND	A118	A58	KR_RX_DP<15>				
GND	A119	A59	KR_RX_DN<15>				
MEZZ_PRSNTA2_N	A120	A60	GND				

For KR Mezz with 4, 8, or 16 KR channels, follow Table 12 to assign the sequence.

Table 12: KR/Repeater numbering sequence

KR/Repeater Numbering Sequence																
# of KR	*Pin 1	Connector A							*Pin 1	Connector B						
2 KR									0	1						
4 KR									0	1	2	3				
8 KR									0	1	2	3	4	5	6	7
16 KR	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7

4.2.3 4x KR Mezzanine card with Connector C

Pin definition of a mezzanine card with up to x4 KR in connector C is in Table 13. The direction of the signals are from the perspective of the baseboard.

Table 13: 4x KR Pin definition in Connector C

Connector C			
Signal	**Pin**	**Pin**	**Signal**
P12V_AUX/P5V_AUX-P12V	C33	C1	MEZZ_SMCLK
P12V_AUX/P5V_AUX-P12V	C34	C2	MEZZ_SMDATA
P12V_AUX/P5V_AUX-P12V	C35	C3	EXT_MDIO_I2C_SEL
RSVD	C36	C4	GND
SDP0	C37	C5	KR_TX_DP<2>
SDP1	C38	C6	KR_TX_DN<2>
GND	C39	C7	GND
KR_TX_DP<0>	C40	C8	LED_P1_0_N
KR_TX_DN<0>	C41	C9	LED_P1_1_N
GND	C42	C10	GND
LED_P0_0_N	C43	C11	KR_TX_DP<3>
LED_P0_1_N	C44	C12	KR_TX_DN<3>
GND	C45	C13	GND
KR_TX_DP<1>	C46	C14	LED_P2_0_N
KR_TX_DN<1>	C47	C15	LED_P2_1_N
GND	C48	C16	GND
SHARED_KR_MDC_0	C49	C17	KR_RX_DP<2>
SHARED_KR_MDIO_0	C50	C18	KR_RX_DN<2>
GND	C51	C19	GND
KR_RX_DP<0>	C52	C20	Module_SCL0
KR_RX_DN<0>	C53	C21	Module_SDA0
GND	C54	C22	GND
LED_P3_0_N	C55	C23	KR_RX_DP<3>
LED_P3_1_N	C56	C24	KR_RX_DN<3>
GND	C57	C25	GND
KR_RX_DP<1>	C58	C26	Module_SCL1
KR_RX_DN<1>	C59	C27	Module_SDA1
GND	C60	C28	GND
Module_SCL2	C61	C29	Module_SCL3
Module_SDA2	C62	C30	Module_SDA3
GND	C63	C31	SDP2
MEZZ_PRSNTC2_N	C64	C32	SDP3

4.3 Mezzanine Card Pin Description

Mezzanine card pin description is shown in Table 14Table 14Table 14; input output direction is in the prospective of baseboard.

Table 14: Mezzanine Card Pin Description

Signals on Connector A	Type	Description
GND	Ground	Ground return; total 51 pins on Connector A
P12V_AUX/P12V	Power	12V Aux/normal power; total 3 pins on Connector A
P5V_AUX	Power	5V Aux power; total 3 pins on Connector A
P3V3_AUX	Power	P3V3 Aux Power; total 2 pins on Connector A
P3V3	Power	P3V3 power; total 8 pins on Connector A

MEZZ_PRSNTA1_N/BASEBOARD_ID_A	Output	Connector A Present Pin; connect to MEZZ_PRSNTA2_N on Mezz with 0 Ohm; Use as baseboard ID during power up
MEZZ_PRSNTA2_N	Input	Connector A Present Pin; connect to MEZZ_PRSNTA1_N on Mezz with 0 Ohm
LAN_3V3STB_ALERT_N	Input	SMBus Alert for OOB management; 3.3V AUX rail
SMB_LAN_3V3STB_CLK	Output	SMBus Clock for OOB management; 3.3V AUX rail; Share with thermal reporting interface; Both 100Kb/s and 400Kb/s shall be supported
SMB_LAN_3V3STB_DAT	Bidirectional	SMBus Data for OOB management; 3.3V AUX rail; Share with thermal reporting interface; Both 100Kb/s and 400Kb/s shall be supported
NCSI_RXER	Input	NC-SI for OOB management; 3.3V AUX rail; Direction is in perspective of baseboard
NCSI_CRSDV	Input	NC-SI for OOB management; 3.3V AUX rail; Direction is in perspective of baseboard
NCSI_RXD[1..0]	Input	NC-SI for OOB management; 3.3V AUX rail; Direction is in perspective of baseboard
NCSI_RCLK	Output	NC-SI for OOB management; 3.3V AUX rail; Direction is in perspective of baseboard
NCSI_TXEN	Output	NC-SI for OOB management; 3.3V AUX rail; Direction is in perspective of baseboard
NCSI_TXD[1..0]	Output	NC-SI for OOB management; 3.3V AUX rail; Direction is in perspective of baseboard
PCIE_WAKE_N	Input	PCIe wake up signal
PERST_N0	Output	PCIe reset signal 0
MEZZ_SMCLK	Output	PCIe SMBus Clock for Mezz slot/EEPROM; 3.3V AUX rail; Share with thermal reporting interface; Both 100Kb/s and 400Kb/s shall be supported
MEZZ_SMDATA	Bidirectional	PCIe SMBus Data for Mezz slot/EEPROM; 3.3V AUX rail; Share with thermal reporting interface; Both 100Kb/s and 400Kb/s shall be supported
CLK_100M_MEZZ[1..0]_DP/N	Output	MB clock output for PCIe devices; total 2 pairs on Connector A; CLK_100M_MEZZ1_DP/N is optional for single host baseboard
MEZZ_TX_DP/N_C<7..0>	Output	PCIe TX; total up to 8 lanes on Connector A; optional with KR signals
MEZZ_RX_DP/N<7..0>	Input	PCIe RX; total up to 8 lanes on Connector A; optional with KR signals
KR_TX_DP/N<15..8>	Output	KR TX; total up to 8 lanes on Connector A; optional with PCIe signals

KR_RX_DP/N<15..8>	Input	KR RX; total up to 8 lanes on Connector A; optional with PCIe signals
RSVD	TBD	Reserved for Future use

Signals on Connector B	Type	Description
GND	Ground	Ground return; total 36 pins on Connector B
P12V_AUX/P12V	Power	12V Aux/Normal power; total 2 pins on Connector B
MEZZ_PRSNTB1_N/ BASEBOARD_ID_B	Output	Connector B Present Pin; connect to MEZZ_PRSNTB2_N on Mezz with 0 Ohm Use as baseboard ID during power up
MEZZ_PRSNTB2_N	Input	Connector B Present Pin; connect to MEZZ_PRSNTB1_N on Mezz with 0 Ohm
PERST_N[3..1]	Output	PCIe reset signal or Node[3..1] PCIe reset signal for baseboard with more than 1 nodes
CLK_100M_MEZZ[3..2]_DP/N	Output	MB clock output for PCIe devices; total 2 pairs on Connector B; optional for single host baseboard
MEZZ_TX_DP/N_C<15..8>	Output	PCIe TX; total up to 8 lanes on Connector B; optional with KR signals
MEZZ_RX_DP/N<15..8>	Input	PCIe RX; total up to 8 lanes on Connector B; optional with KR signals
KR_TX_DP/N<7..0>	Output	KR TX; total up to 8 lanes on Connector B; optional with PCIe signals
KR_RX_DP/N<7..0>	Input	KR RX; total up to 8 lanes on Connector B; optional with PCIe signals
RSVD	TBD	Reserved for Future use

Signals on Connector C	Type	Description
GND	Ground	Ground return
P12V/P12V_AUX/P5V_AUX	Power	Power supply to Mezzanine connector
SDP[3..0]	Input	Software defined pin for port 0~3; OD, pull up at baseboard side SFP+ KR Mezz: MODULE_PRSENT_N[3..0] for Port [3..0] SFP+ modules 10GBaseT KR Mezz: INT_N [3..0] for Port [3..0] 10GBaseT PHY QSFP+ KR Mezz:

		SDP_0 to QSFP+ MODULE_PRSENT_N
KR_TX_DP/N<3..0>	Output	KR TX; total up to 4 lanes on Connector C
KR_RX_DP/N<3..0>	Input	KR RX; total up to 4 lanes on Connector C
LED_P[3..0]_0_N	Output	Port[3..0] LED0 for link speed; OD and active low
LED_P[3..0]_1_N	Output	Port[3..0] LED1 for link activity; OD and active low
SHARED_KR_MDC	Output	MDC for PHY
SHARED_KR_MDIO	Bidirectional	MDIO for PHY
MEZZ_SMCLK	Output	SMBus Clock for Mezzanine slot for PHY/Repeater config/Mezz FRU EEPROM; 3.3V AUX rail; Share with thermal reporting interface; Both 100Kb/s and 400Kb/s shall be supported
MEZZ_SMDATA	Bidirectional	SMBus Data for Mezzanine slot for PHY/Repeater config/Mezz FRU EEPROM; 3.3V AUX rail; Share with thermal reporting interface; Both 100Kb/s and 400Kb/s shall be supported
EXT_MDIO_I2C_SEL	Output	Strapping pin to configure PHY/repeater on KR Mezzanine card to be accessed through MDIO or I2C. High for MDIO and Low for I2C
Module_SCL[3..0]	Output	Dedicate I2C for SFP+ or QSFP+ modules
Module_SDA[3..0]	Bidirectional	Dedicate I2C for SFP+ or QSFP+ modules
MEZZ_PRSNTC2_N	Input	Connector C Present Pin; connect to GND with 0 ohm on Mezzanine card side
RSVD	TBD	Reserved for Future use

4.3.1 MEZZ FRU EEPROM

MEZZ FRU EEPROM is for baseboard to identify different types of Mezzanine card. MEZZ FRU EEPROM is connected to MEZZ_SMCLK/MEZZ_SMDATA (pin A18, A19 or C1, C2) and address is 0xA2 (8bit format). The size of EEPROM is 1Kbits. Mezzanine card vendors may use larger size EEPROM if needed.

Follow IPMI Platform Management FRU Information Storage Definition v1.0 for data format. Use OEM record 0xC0, offset 1 to store Mezzanine ID definition.

There are 2x Bytes defined.
Mezz ID Byte is to define the physical interface on connectors presented to baseboard.
Mezz Capability Byte is to define the bifurcation capability.

Table 15: Mezzanine ID byte definition

Mezz ID Byte (offset 1)	Usage
0x00	8 lanes of PCIe on Connector A
0x01	16 lanes of PCIe on Connector A and Connector B
0x02	X4 KR with Retimer on Connector B
0x03	X4 KR with PHY on Connector B
0x04	X4 KR with Retimer on Connector C
0x05	X4 KR with PHY on Connector C
0x06	X2 KR with Retimer on Connector C
0x07	X2 KR with PHY on Connector C
0x08	X1 KR with Retimer on Connector C
0x09	X1 KR with PHY on Connector C
All others read back	RFU
No FRU device detected	8 lanes of PCIe on Connector A
Mezz Capability Byte(offset 2)	Usage
0x00	Single Host PCIe Mezz
0x01	Multi Host PCIe Mezz capable of 2x hosts, 4x hosts Compatible with Single Host operation
0x02	KR Mezz
0x03	Multi Host PCIe Mezz capable of 2x hosts, 4x hosts, 8x hosts Compatible with Single Host operation
0x04	Multi Host PCIe Mezz capable of 2x hosts, 4x hosts, 8x hosts, and 16x hosts Compatible with Single Host operation
All others read back	RFU
No FRU device detected	Single Host PCIe Mezz

If Baseboard cannot find EEPROM on Mezzanine card, Baseboard will assume the Mezzanine cards is original Mezzanine card which has PCIe interface. This provides backward compatibility for Mezzanine card without ID EEPROM.

4.3.2 Baseboard ID

MEZZ_PRSNTA1_N in connector A and MEZZ_PRSNTB1_N in connector B is connected to ground for this case.

Baseboard ID is an optional feature for special baseboard to identify itself to Mezzanine card. It is only implemented when Mezzanine card needs to have awareness of different baseboard types, and the baseboard Mezzanine card interface is not a single root port PCIe. Baseboard ID only applies connector A and Connector B.

The implementation example of Baseboard ID circuit is shown in Figure 31~~Figure 28~~~~Figure 28~~.

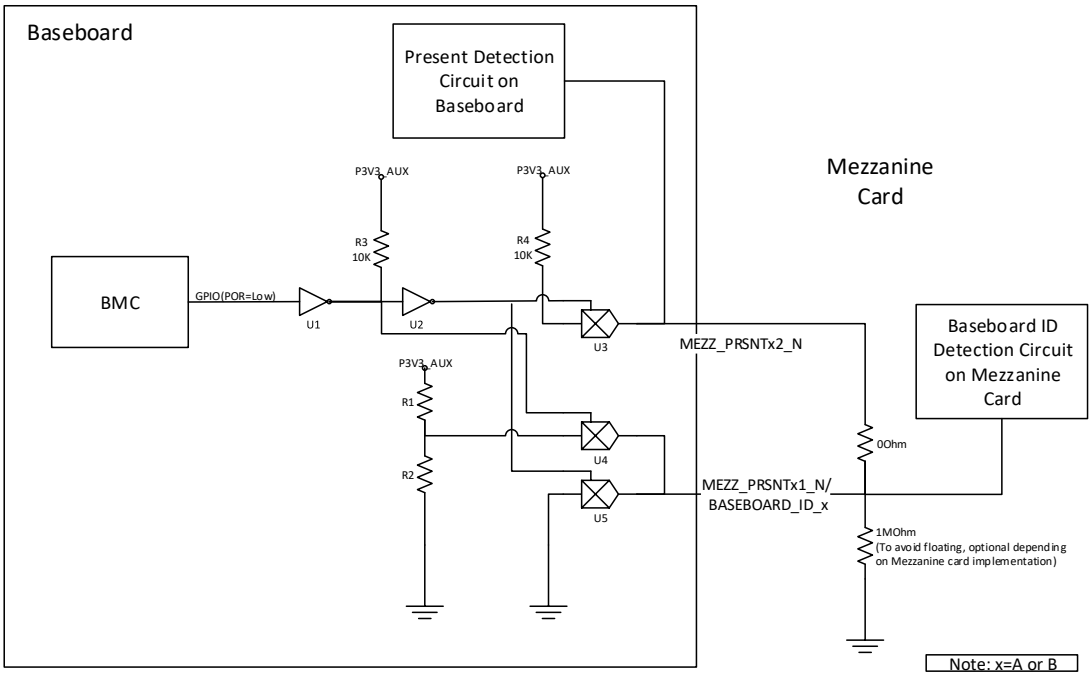

Figure 3128: Baseboard ID circuit

Mezzanine card identifies different of Baseboard based on the resistor pair R1/R2 shown in Table 16.

Table 16: Baseboard ID definiton

ConnA R1	ConnA R2	Baseboard type on Connector A
NC	0 Ω	One x8 PCIe Root Port on baseboard Connector A; No Connector B on Baseboard
10 KΩ	887 Ω	One x16 PCIe Root Ports on Baseboard Connector A and B
10 KΩ	2.10 KΩ	One x8 PCIe Root Port on baseboard Connector A; Connector B presents on Baseboard
10 KΩ	3.83 KΩ	Two x4 PCIe Root Ports on baseboard Connector A
10 KΩ	6.49 KΩ	Four x2 PCIe Root Ports on baseboard Connector A
10 KΩ	11 KΩ	Eight x1 PCIe Root Ports on baseboard Connector A
10 KΩ	20.5 KΩ	RFU
10 KΩ	48.7 KΩ	RFU
10 KΩ	NC	Up to 8x KR on baseboard Connector A

ConnB R1	ConnB R2	Baseboard type on Connector B
NC	NC	No Connector B on baseboard; Mezzanine card samples Baseboard_ID_B as 0V with weak pull low on Mezzanine card side
10 KΩ	887 Ω	One x16 PCIe Root Ports on Baseboard Connector A and B
10 KΩ	2.10 KΩ	One x8 PCIe Root Port on baseboard Connector B
10 KΩ	3.83 KΩ	Two x4 PCIe Root Ports on baseboard Connector B
10 KΩ	6.49 KΩ	Four x2 PCIe Root Ports on baseboard Connector B
10 KΩ	11 KΩ	Eight x1 PCIe Root Ports on baseboard Connector B
10 KΩ	20.5 KΩ	RFU
10 KΩ	48.7 KΩ	RFU
10 KΩ	NC	Up to 8x KR on baseboard Connector B

Mezzanine card has a 4 seconds window to sample Baseboard ID signal, after both P12V_AUX and P3V3_AUX ready. BMC may disable baseboard ID output by GPIO after 4 seconds and change the multipurpose pin for Mezzanine card present purpose.

Mezzanine card implementation shall consider the tolerance of P3V3_AUX, R1, and R2 when doing the sampling. P3V3_AUX has ±5% tolerance and R1, R2 has ±1% tolerance. R1 and R2 are selected to ensure a minimal of 240mV gap between 2 IDs, considering the tolerances above. Input current shall also be considered on Mezzanine card side to ensure correct reading of baseboard ID.

1MOhm pull low is optional at Mezzanine card side to avoid floating of input at Mezzanine card side "Baseboard ID Detection Circuit".

There are 2x typical implementations for Mezzanine card to implement Baseboard ID sampling. Mezzanine card vendors are not limited to these two implementations as long as the Mezzanine card is able to identify correct baseboard ID and initialized itself properly.

- Using comparator to compare the voltage BASEBOARD_A/B_ID pins with reference voltage. It is preferred that the reference voltage is generated from P3V3_AUX and voltage divider. This helps to cancel out the ±5% tolerance on P3V3_AUX DC level.
- Using ADC to identify voltage level on BASEBOARD_A/B_ID pins during 4 seconds window after both P12V_AUX and P3V3_AUX ready. P3V3_AUX is preferred to generate the voltage reference of ADC if it applies.

5 Management Interface

There are two options of management interfaces on PCIe Mezzanine NIC for BMC's out-of-band communication. Both interfaces should be routed from mezzanine card connector to NIC chipset. It is preferred that BMC firmware can choose to hand shake with either interfaces to have out-of-band channel. Only one interface need to be up and running for out-of-band traffic at a given time.

The original OCP Mezzanine 1.0 specification only defines I2C side band interface to work with Facebook OCP Intel® motherboard V2.0. Starting Facebook OCP Intel® motherboard V3.0, the baseboard supports both I2C side band and NC-SI side band. NC-SI side band is the preferred interface due to higher speed and lower image transfer time for FW update from out-of-band.

For new design, PCIe Mezzanine NIC has to implement NC-SI side band interface. It is preferred to implement I2C side band for compatibility with baseboard with I2C side band only.

Management interface shall support both IPv4 and IPv6.

5.1 I2C side band

PCIe Mezzanine NIC implements management interface compatible with Intel's Management Engine (ME) through C600 PCH SMLINK0 port and provides Out of Band (OOB) network access. Vendor should check with Facebook to choose SMBus address for ME OOB access. The hardware and firmware design need to support management capability in both S0 and S5 state.

The same I2C interface should be able to be accessed by BMC (baseboard management controller) on platform that used BMC.

I2C side band interface should support MCTP[3].

5.2 NC-SI side band

RMII based NC-SI (referred as NC-SI in rest of document) management interface can be implemented by PCIe Mezzanine NIC. It is essential to achieve management feature needs higher bandwidth such as upload and update baseboard firmware and BIOS through OOB. Compare to original OCP Mezzanine card Specification, 8x RSVD pins are redefined to NC-SI interface.

The total length of each NC-SI signal and clock from connector pin to BGA pin on mezzanine card should be greater or equal to 1500mil and less or equal to 3500mil. NC-SI clock and signal should be matched within 1000mil on the mezzanine card. NC-SI signal and clock is in 3.3V logic level and in 3.3V AUX power domain.

It is preferred that PCIe Mezzanine NIC is able to be connected by different management controllers and interfaces, such as Management engine, BMC I2C, or BMC NC-SI. It is for having backward and forward compatibility with same hardware and firmware.

Management controller should set priority for its capable connection interfaces in a sequence, and scan through the sequence to hand shake with the 1st available management network device. It is to ensure the Mezzanine card without NC-SI side band can still be compatible with baseboard with NC-SI capability.

Mezzanine card implementation is preferred to add support for latest NC-SI version when applies. 25G/50G/100G mezzanine card implementations enabled after NC-SI Version 1.1.0[4] release shall support this version.

5.3 MAC address of management interface

MAC address of management network interface should be a positive offset based on the MAC address of data network interface. Different vendor may implement different offset number based on port

[3] http://www.dmtf.org/sites/default/files/standards/documents/DSP0236_1.2.1.pdf
http://www.dmtf.org/sites/default/files/standards/documents/DSP0237_1.0.0.pdf
[4] https://www.dmtf.org/sites/default/files/standards/documents/DSP0222_1.1.0.pdf

count, and reserved features. Typical offsets are +1 for single port NIC, +2 for dual port NIC. NIC vendor may use larger offset due to having more than 2 ports, or having more than one MAC of data or storage on each port.

6 PCIe Mezzanine NIC Data network

6.1 Network Booting

Mezzanine NIC shall support network booting in uEFI system environment. Mezzanine NIC shall support both IPv4 and IPv6 network booting.

7 Thermal Reporting Interface

7.1 Overview of Thermal Reporting Interface

A thermal reporting interface is defined on SMB_LAN_3V3STB_CLK/SMB_LAN_3V3STB_DAT (Connector A, pin A75, A76) or MEZZ_SMCLK/ MEZZ_SMDATA (Connector A, pin A18, A19; or Connector C, pin C1, C2). The implementation of this requirement will improve the thermal management of system and allow baseboard management device to access key component temperature on Mezzanine card. Baseboard management device needs to scan SMB_LAN_3V3STB_CLK/SMB_LAN_3V3STB_DAT and MEZZ_SMCLK/ MEZZ_SMDATA to determine the location of the thermal reporting interface.

There are two methods to implement thermal reporting described in this section: Emulated method and remote on-die sensing method. Both methods will be treated by baseboard management controller as a TI/TMP421 thermal sensor with slave address 0x3E in 8 bit format.

For Mezzanine card with Thermal Design Power > 5 Watts, this implementation of this interface is required.

7.1.1 Emulated Thermal Reporting

Mezzanine card should emulate its key temperatures to be accessed from SMBus (Connector A, Pin A18/A19 or pin A75/A76; Or Connector C, C1/C2 for KR Mezz; P3V3_STBY rail). The emulation should follow TMP421 register mapping[5]. Baseboard treats the PCIe card thermal sensor as TMP421. Baseboard BMC controller should use 2x separate reads to obtain the MSB and LSB of temperature data. Data obtained is used for system thermal monitoring and fan speed control.

There are two temperatures for TMP421 register mapping, local and remote channel 1. Remote channel 1 is typically used to represent key controller temperature of the card. Local channel is typically used to represent highest of other key components temperature on the card, such as highest temperature of active cable module.

Address of the emulated TMP421 device is fixed at 0x3E in 8bit format.

An implementation block diagram is shown in Figure 32~~Figure 29~~~~Figure 29~~.

[5] TMP421 specification: http://www.ti.com/lit/ds/sbos398c/sbos398c.pdf

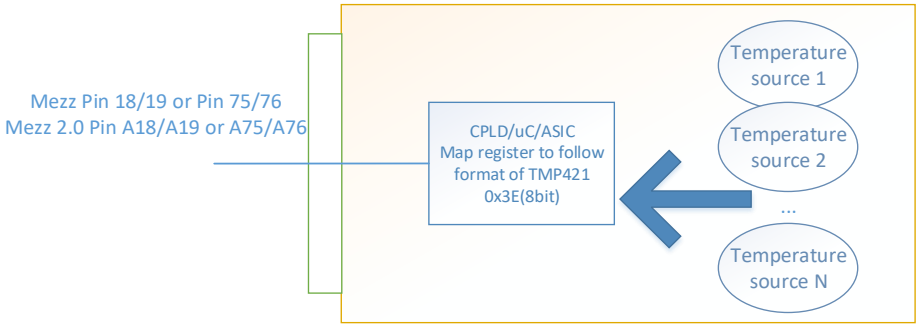

Figure 3229: Block Diagram for Emulated Thermal Reporting

With firmware change of the controller on baseboard managing thermal data and control, a register mapping of TMP422/TMP423 can be used to support one/two more temperatures without hardware change. The slave address of emulated device is always 0x3E, even it emulates TMP422/TMP423.

Vendor ID and device ID is mapped to offset 0xFE and 0xFF in order for board management controller to detect card types.

Power reporting and power capping is mapped to offset 0xF2 and 0xF3 as an optional feature to achieve device power monitoring and power capping level setting.

Table 17:~~Table 17:Table 17:~~ describes the register implementation requirement for emulated method.

Table 17: Implementation Requirement for TMP421 Registers

Offset	Description	Original TMP offset	Implementation requirement for emulated method
0x0	Local Temperature (High Byte)	Y	Represents highest temperature of all other key components Required if any of the other key components or modules are critical for thermal design Otherwise it is an optional offset and return 0x00 if not used
0x1	Remote Temperature 1 (High Byte)	Y	Required; represent temperature of main controller
0x2	Remote Temperature 2 (High Byte)	Y	Optional; represent temperature of key component 1; return 0x00 if not used
0x3	Remote Temperature 3 (High Byte)	Y	Optional; represent temperature of key component 2; return 0x00 if not used
0x8	Status Register	Y	Not required
0x9	Configuration Register 1	Y	Not required; Emulated behavior follows SD=0, Temperature Range=0
0x0A	Configuration Register 2	Y	Required; follow TMP423 datasheet to declare the channel supported; RC=1
0x0B	Conversion Rate Register	Y	Not required; Equivalent emulated conversion rate should be >2 sample/s

0x0F	One-Shot Start	Y	Not required
0x10	Local Temperature (Low Byte)	Y	Optional; return 0x00 if not used
0x11	Remote Temperature 1 (Low Byte)	Y	Optional; return 0x00 if not used
0x12	Remote Temperature 2 (Low Byte)	Y	Optional; return 0x00 if not used
0x13	Remote Temperature 3 (Low Byte)	Y	Optional; return 0x00 if not used
0x21	N Correction 1	Y	Not required
0x22	N Correction 2	Y	Not required
0x23	N Correction 3	Y	Not required
0xF0	Manufacturer ID(High Byte)	N	High byte of PCIe vendor ID, if using emulated temperature sensor method
0xF1	Device ID(High Byte)	N	High byte of PCIe device ID, if using emulated temperature sensor method
0xF2	Power reporting	N	Optional; card power reporting; 1LSB=1W; Read only
0xF3	Power capping	N	Optional; card power capping; 1LSB=1W; Read/Write
0xFC	Software Reset	Y	Not required
0xFE	Manufacturer ID	Y(redefined)	Low byte of PCIe vendor ID, if using emulated temperature sensor method
0xFF	Device ID	Y(redefined)	Low byte of PCIe device ID, if using emulated temperature sensor method

7.1.2 Remote on-die sensing

Alternatively, one TMP421 sensor can be used to do on die temperature sensing for IC with thermal diode interface with TMP421 remote sensing channel; Connection diagram is shown in Figure 33~~Figure 30~~Figure 30.

For NIC needs more than one remote on-die sensing, TMP422/TMP423 can be used and slave address is 0x98(8bit) for this case.

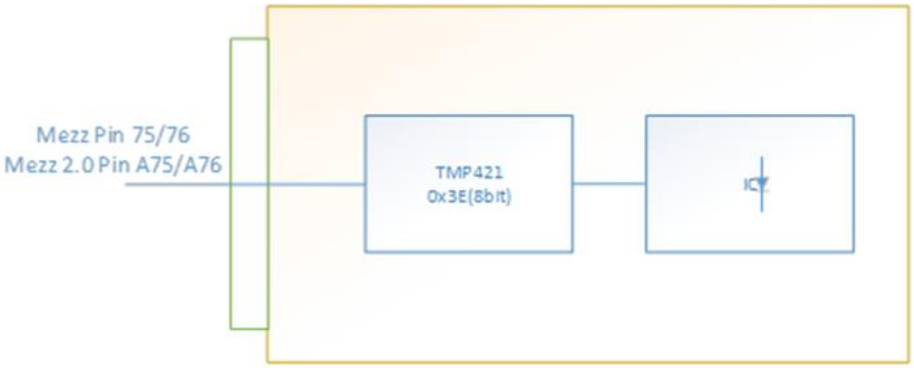

Figure ~~33~~30: Block Diagram for Remote on-die Sensing

8 Environmental

8.1 Environmental Requirements

The specific environment requirement is removed to allow the adoption of OCP Mezzanine NIC in systems with very different thermal requirement and boundary condition.

This Mezzanine card shall meet the same environmental requirements specified in the OCP systems that the Mezzanine card is in. The OCP system that uses OCP Mezzanine card shall define air flow direction, inlet air temperature, air flow (or speed) to the local area where Mezzanine card is at, and simulation boundary.

8.1.1 Thermal Simulation Boundary Example

Placeholder for Thermal Simulation Method. Using Facebook Intel® Motherboard V3.0 as example. Not covered by ~~Rev0.45~~this update.

8.2 Shock & Vibration

This Mezzanine card shall meet the same shock & vibration requirements specified in updated Facebook OCP Intel® Motherboard V2.0 and V3.0 Design Specification.

8.3 Regulation

This Mezzanine card shall meet CE, CB, FCC Class A, WEEE, ROHS requirements.

9 Revision History

Author	Description	Revision	Date
Jia Ning	-Initial draft for community feedback	0.2	5/18/2014
Jia Ning	-Typical correction and clarification	0.21	5/20/2014
Jia Ning	-Add Mezzanine FRU and Baseboard ID -Remove Mezzanine ID resistor network -Change thermal reporting interface from pin 18, 19 to pin 75, 76 - Update pin define table and description	0.31	6/18/2014
Jia Ning	- Correct Pin number from 18/19 to 75/76 in Figure 18 - Correct description for MEZZ_SMCLK and MEZZ_SMDATA in Table 4	0.32	7/9/2014
Jia Ning	- Add option for TMP422/TMP423 to be used for thermal reporting in Section 7.1.2 - Add clarification of air flow direction and air flow information in section 8.1 - Add clarification of 4x QSFP use case in section 3.4 - Add bifurcation rule in section 4.2.1 - Update Phy Mezz table with new port sequence; add repeater option to Phy Mezz - Update FRU EEPROM format in section 4.3.1	0.33	7/16/14

Jia Ning	- Add new Mezz ID per community feedback	0.34	7/19/2014
Jia Ning	- Add section 3.6 for MAC label requirements - Modify thermal reporting interface to be on A18/A19 or A75/A76. - Add clarification for mechanical compatibility in section 3.2.2 - Add CB, WEEE, ROHS into regulation requirement - Change PHY Mezz to KR Mezz - Format clean up	0.40	8/1/2014
Jia Ning	- Table 4: Correct Typo: change from MEZZ_PRSNTA_N to MEZZ_PRSNTA2_N - Table 3: Update Bifurcation rule of PCIe - Table 5: Update Bifurcation rule of KR/Repeater - Table 8: Update Baseboard ID definition to support Dual root ports and Quad root ports - All: update CLK_100M_MEZZ[4..1]_DP/N to CLK_100M_MEZZ[3..0]_DP/N to match PERST_N[3..0] - Table 7: Add capability Byte to Mezz ID definition	0.41	1/17/2015
Jia Ning	- Table 4: Modify KR sequence to match Table 5 - Table 8: Modify baseboard ID definition; separate Connector A and Connector B definition - Section 4.3.2: Modify Baseboard ID rule, and 2x Mezzanine implementation examples	0.42	1/26/2015
Jia Ning	-Table 8: Remove Connector B NC row, since Mezz card is not able to identify it -Figure 18: Add weak Pull Low at Mezzanine card side for Baseboard_ID signal to avoid floating when Baseboard side connector is not populated; Add detection circuit on baseboard side -Figure 11: Add LED location and color for 4x KR Mezz -Table 7: change 0x02 to KR Mezz with 4 lanes -Section 4.1: Change hard requirement of P12V_AUX to optional requirement to allow systems without P12V_AUX to work with some OCP Mezzanine cards	0.43	2/1/2015
Jia Ning	-Table 8: Update table	0.44	2/5/2015
Jia Ning	- Add 25G/50G/100G - Chapter 8: Remove thermal requirements of Mezzanine card. Use system requirements to guide Mezzanine card thermal design - Chapter 8: Add placeholder for thermal simulation method - Add connector C for KR Mezzanine - Add 5mm Stack - Add KR Mezzanine card with Connector C as implementation examples - Add Type 4 stack - Elaborate LED definition - Update Connector C power pin definition, and add matrix for implementation guide power pin definition	0.45	8/30/2015
Jia Ning	- Add acknowledgement chapter	0.46	9/27/2015

	- Add implementation example table		
Jia Ning	- Remove acknowledgement chapter - Section 4.1: Add clarification about thermal limitation in power capability section - Section 5.2: Add note for NC-SI 1.1.0 support is required for new 25G/50G/100G implementation - Section 4.3: Add bit rate for I2C side-band - Section 5.2: clarify some terms around NC-SI over RMII - Section 5.1: clarify I2C side band shall be MCTP capable - Table 14: clarify PCIe clock is optional for single host baseboard - Table 2, section 3.5: Add M1 and M2 for max profile	0.47	10/22/2015
Jia Ning	- Update Figure 13 to reflect 4mm area reduced from 4.5mm - Section 4.3.2 and Figure 28: Add ~~commnets~~comments for 1MOhm resistor being optional - Chapter 5: Move IPv4 and IPv6 requirement to 5 from 5.1 and 5.2 - Update Figure 11 with real picture - Correct typos - Add "_N" for LED pin name to match active low definition - Table 7: Correct P5V to P5V Aux to match with Table 5 - Use "P12V_AUX/P5V_AUX-P12V" as note to note Connector C power pin	0.95	10/31/2015
Jia Ning	- Section 3.4: Add clarification that baseboard need to provide clearance for mezzanine keep out - Section 5.2: Table 14: Add clarification of NC-SI signal and clock logic level being 3.3V - Table 2: Update 3D table - Add section 3.8 for plastic insulation sheet requirement - Table 14: Add notes for direction of NC-SI signals	1.00	12/15/2015
Damien Chong	- Added Type-5 Mezzanine Card definition	1.10	09/04/2019