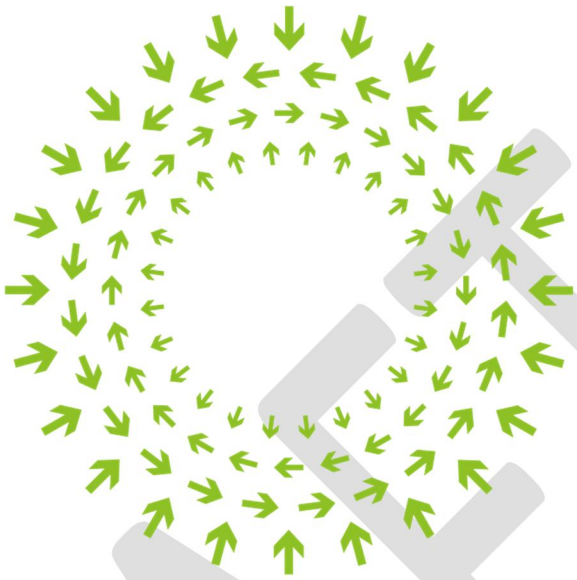

OPEN

Compute Project

Decathlete Server Board Standard

Revision 2.0

DRAFT VERSION – changes highlighted in YELLOW

DRAFT VERSION as presented to SERVER WG November 19, 2014

Revision History

Date	Revision Number	Modifications
April 2012	0.5	First Draft
April 2013	1.0	Initial Release
November 2014	2.0	Tabulation added for Grantley generation products DRAFT VERSION – changes highlighted in YELLOW

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1. License

As of April 25, 2013, the following persons or entities have made this Specification available under the Open Web Foundation Final Specification Agreement (OWFa 1.0), which is available at

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2. Summary

This standard provides board-specific information detailing the features and functionality of a general purpose 2-socket server board for adoption by the Open Compute Project community. The purpose of this document is to define a dual socket server board that is capable of deployment in scale out data centers as well as traditional data centers with 19" rack enclosures. In the creation of the Decathlete specification, considerations are made for 2-socket server boards that were in production at time of specification release that would fulfill these needs.

This document is not intended to be used solely as a basis for a procurement of OCP compatible products. The OCP community may have additional requirements. These incremental requirements can be captured in additional procurement documentation.

3. Compliance to the Standard

Products making the claim of compliance with this specification **SHALL** provide, at a minimum, all features defined as mandatory by the use of the keyword "**SHALL**". Such products may also provide recommended features associated with the keyword "**SHOULD**" and permitted features associated with the keyword "**MAY**".

The specification has been tabulated so that products can be designed to comply to the Revision 1.0 spec and/or the 2.0 spec. The revision 2.0 incorporates new products features and technologies introduced into server products in 2014. Products MAY meet one or both revisions.

Products that comply with one revision only should clearly note "Complies to Decathlete Revision x.0 Specification"

4. Feature Requirements

The Decathlete Server Board is intended to meet the most common usages for 1U and 2U dual socket servers in the scale-able data center. To insure the delivery of products that can be deployed over a period of time, and assure consistency in the services offered to the client of the cloud data server, certain features must be present in each model or generation of servers. These features are listed in the following two (2) tables.

Table 1 Decathlete Server Board Required Features describe features that must be present to be considered compliant to this standard. The table is tabulated for products released to the Revision 1.0 spec and the 2.0 spec.

Table 1 Decathlete Server Board Required Features

Feature	Revision 1.0 Compliant Product	Revision 2.0 Compliant Product
Processor Support	Support up to two processors with a thermal design point (TDP) of up to 135 W. • Minimum of 8 processor cores and 16 threads • 4 memory channels • Support for dynamic overclocking	Support up to two processors using LGA2011-3 (socket type R3) and VRD 12.5 and a thermal design point (TDP) of up to 145W. • Minimum of 8 processor cores and 16 threads • 4 memory channels • Support for dynamic overclocking
Memory Expansion	16 sockets for un-buffered DDR3 and registered DDR3 DIMMS LR DIMM for buffered memory solutions DDR3 standard I/O voltage of 1.5V and DDR3 low voltage of 1.35V • 1.5 V: 1DPC up to 1600, 2DPC up to 1333, 3DPC up to 800. • 1.35 V: 1DPC up to 13, 2DPC up to 1066 1 Gb, 2-Gb, and 4Gb DDR3 DRAM technologies supported for these devices: • UDIMM DDR3 - SR x8 and x16 data widths, DR- x8 data width • RDIMM DDR3 – SR, DR, and QR – x4 and x8 data widths • LRDIMM DDR3 – QR – x4 and x8 data widths with direct map or with rank multiplication	Provide 16 sockets for DDR4 DIMMS Support for RDIMM and LR-DIMM types Support access rates of 1333Mt/s and above Support NVDIMM in 1 or more DIMM slots
Memory RAS	ECC, Patrol & Demand Scrubbing, Sparing, Lockstep mode Channel mirroring within a socket: • CPU1 channel mirror pairs (A,B) and (C,D) • CPU2 channel morror pairs (E,F) and (G,H)	-same as Release 1.0-
Chipset	A chipset that support for Storage Option Select keys	-same as Release 1.0-
External I/O connections	Two RJ-45 Network Interface Connectors supporting 10/100/1000Mb Two USB 2.0 connectors	Two RJ-45 Network Interface Connectors supporting 10GbE/1GbE/100MbE. Two USB connectors fully 2.0 and 3.0 compliant

Feature	Revision 1.0 Compliant Product	Revision 2.0 Compliant Product
Internal I/O connectors /headers	One type-A USB 2.0 connector One SSI-EEB compliant front panel header One DH-10 serial Port B connector	-same as Release 1.0-
I/O Module Options	Support all on-board I/O features in addition to any installed I/O modules or add-in expansion cards.	-same as Release 1.0-
System Fans	Six 10-pin managed system fan headers	Six 10-pin managed system fan headers (1U) Six 6-pin hot swappable,managed fan headers(2U)
Riser Card Support	Two riser card slots with a minimum of 16 PCIe Gen3 lanes per riser Riser card for 1U chassis must support two half-length cards Riser card for 2U chassis must support three PCIe add-in cards with at least one full length	Two riser card slots with a minimum of 24 PCIe Gen3 lanes per riser Riser card for 1U chassis must support two half-length cards Riser card for 2U chassis must support three PCIe add-in cards with at least one full length
Video	Not required	-same as Release 1.0-
Storage	Two single port AHCI SATA connectors capable of supporting up to 6 Gb/sec Two SCU 4-port mini-SAS connectors capable of supporting up to 3 Gb/sec SATA/SAS	Two single port SATA connectors capable of supporting up to 6 Gb/sec Two 4-port mini HD connectors capable of supporting up to 6 Gb/sec SATA
Security	Provide support for a Trusted Platform Module (TPM) security device	Provide support for a Trusted Platform Module TPM1.2 and optionally TPM2.0 security device. A Trusted Platform Module **SHALL** be available for the product.
Server Management	Meets the requirements of the OCP Open Hardware Management Specification for Remote Machine Management V.0.93	Meets the requirements of the OCP Open Hardware Management Specification for Remote Machine Management V.1.01

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Table 2 are optional features that should be present, or features that are acceptable and MAY be present. The table is tabulated for products released to the Revision 1.0 spec and the 2.0 spec. Products MAY meet one or both.

Table 2. Decathlete Server Board Optional Features

Feature	Release 1.0 Product	Release 2.0 Product
Memory Expansion	24 memory sockets	-same as Release 1.0-
Chipset	Storage Option Select keys	-same as Release 1.0-
External I/O connections	DB-15 Video connector RJ-45 serial port A connector Two additional RJ-45 network interface connectors supporting 10/100/1000Mb One or more additional USB 2.0 connectors	DB-15 Video connector RJ-45 serial port A connector Two additional RJ-45 network interface connectors supporting 10Gb/1Gb/100Mb One or more additional USB 2.0 connectors
Internal I/O connectors /headers	One connector to provide support for two USB 2.0 ports on front of system One DH-10 serial Port B connector	-same as Release 1.0-
I/O Module Options	Installed I/O modules shall be supported in addition to standard on-board features and any add-in expansion cards. I/O module options that should be supported: ▪ Quad port 1 GbE module ▪ Dual port 10GBase-T Ethernet module ▪ Dual SFP+ port 10GbE module ▪ Single Port FDR speed InfiniBand module with QSFP connector	-same as Release 1.0-
PCIe Adapter Card Support	Support for *PCI Express* 225W/300W High Power Card Electromechanical Specification 1.0.*	-same as Release 1.0-
Video	Integrated 2D Video Controller 16 MB DDR memory	-same as Release 1.0-
Server Management	Support for KVM-over-IP Support for USB and CDROM virtual media (bootable) Integrated Baseboard Management Controller, IPMI 2.0 compliant Support for DCMI 1.5	-same as Release 1.0-
Misc Features	Status LEDs & Diagnostics LEDs that assist maintenance personnel to identify failed devices or abnormal conditions Indicators that reduce maintenance and repair times	-same as Release 1.0-

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5. Server Board Mechanical Dimensions

A server board that meets the Decathlete Standard **SHALL** complies with one of two layout options:

5.1.1 Asymmetric Layout Option

The asymmetric layout does not define nor follow any specific mechanical requirements. The intent of this layout is to leverage existing OEM and ODM chassis designs. As such, the mechanical features and board outline varies between each supplier and therefore cannot be interchangeable with a chassis. A fully dimensioned layout is not necessary.

The suppliers of a Decathlete server board that chooses this layout **SHALL** make available a complete server system that supports two power supplies located on the right-hand side of the chassis. The approximate location of the CPU sockets, memory, and power supplies are important and provides some consistency in airflow management, cable management, and service documentation.

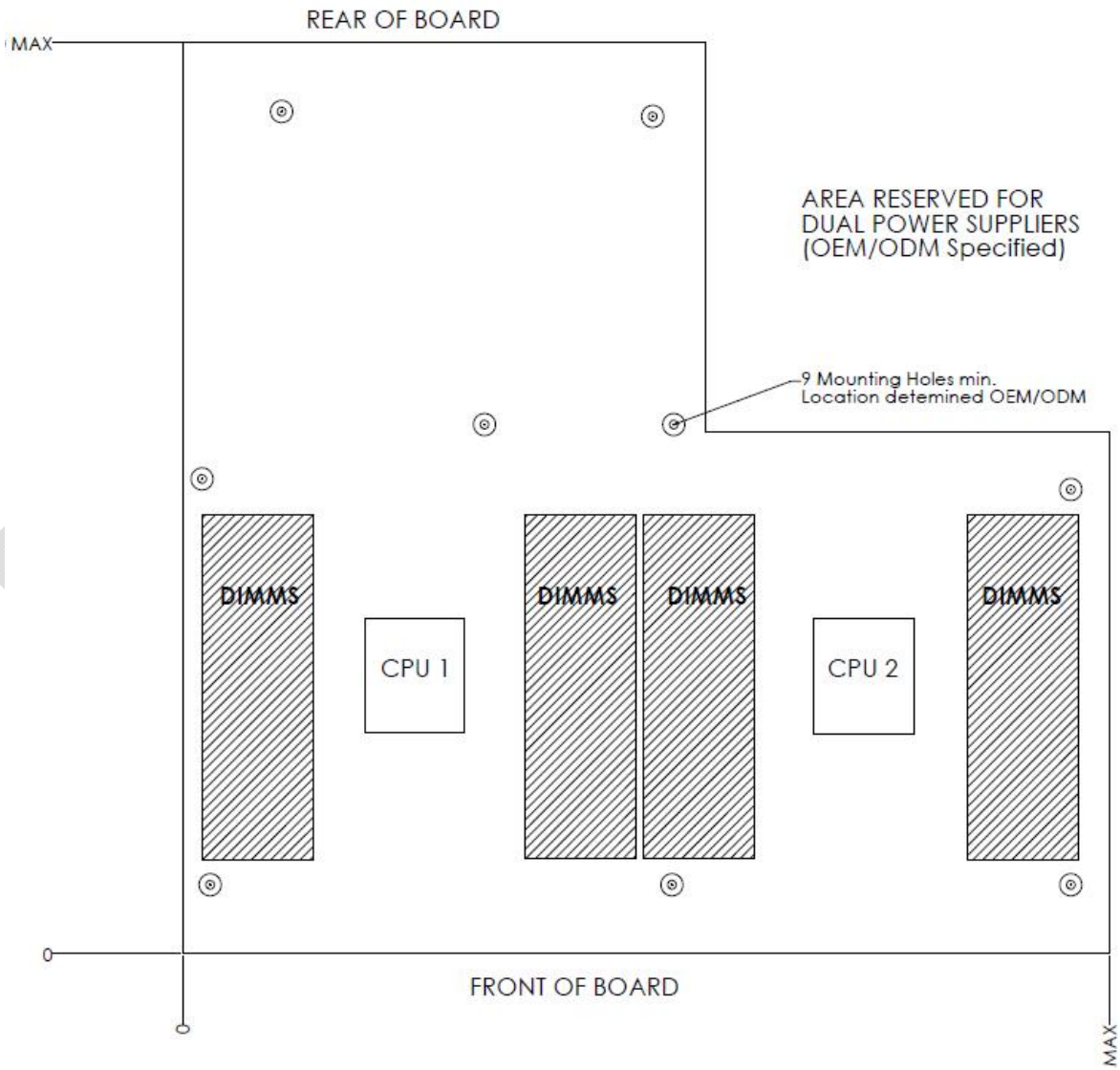


Figure 5-1 Asymmetric Board Layout

5.1.2 Symmetric Layout Option

The symmetric layout defines specific mechanical requirements. The intent of this layout is to allow the server board to be interchangeable with chassis products from more than one supplier. A fully dimensioned layout is necessary.

The symmetric layout SHALL support one power supply located on each side of the chassis (2 total power supplies) and conform to the mechanical layout defined in Figure 5-2.

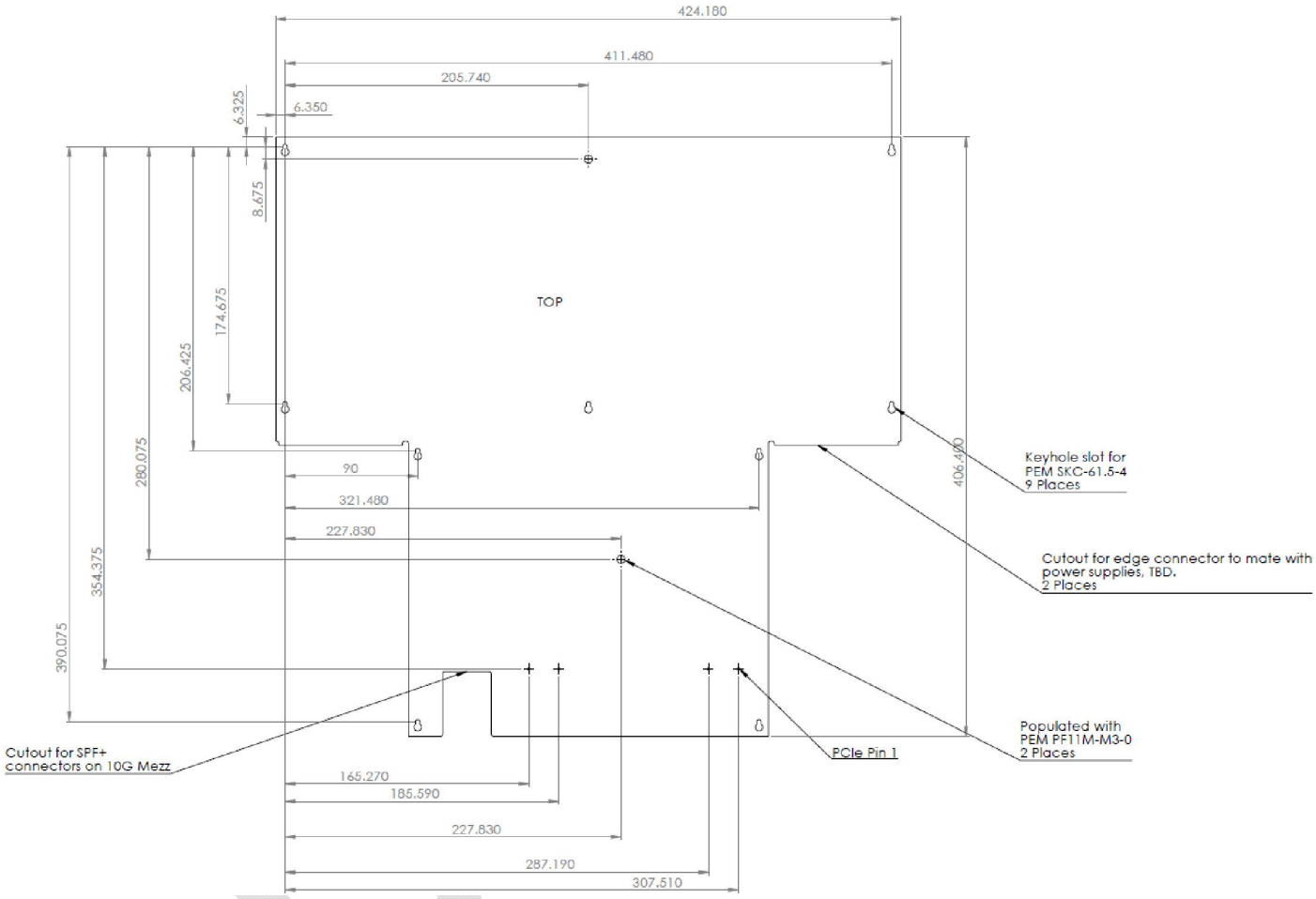


Figure 5-2 Symmetric Board Layout

6. I/O Support

6.1 Network Interface

The server board **SHALL** have one LAN device to support the RJ-45 network interface connectors. The BIOS **SHALL** support PXE boot on the RJ-45 network interface connectors.

Each Ethernet port **SHALL** drive two LEDs located on each network interface connector. The LED at the right of the connector is the link/activity LED and indicates network connection when on, and transmit/receive activity when blinking. The LED at the left of the connector indicates link speed as defined in the following table.

Table 3 External RJ45 NIC Port LED Definition

LED	Color	LED State	NIC State
Left	Green	Off	LAN link not established
		On	LAN link is established
		Blinking	LAN activity is occurring
Right		Off	3rd Fastest data rate
	Green	On	2nd Fastest data rate
	Yellow	On	Fastest data rate

☞ NOTE: Table 2 NIC Port LED Definition is the PREFERRED color and definition. Alternative color and State definitions are acceptable.

6.2 USB

The server board **SHALL** provide two external USB ports and the BIOS **SHALL** support the following USB devices:

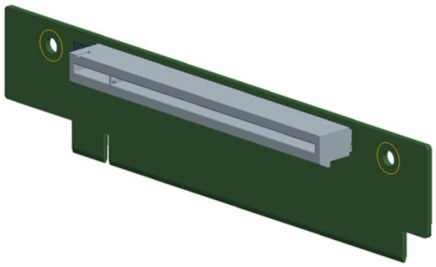
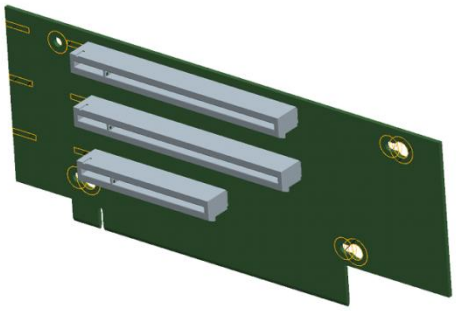
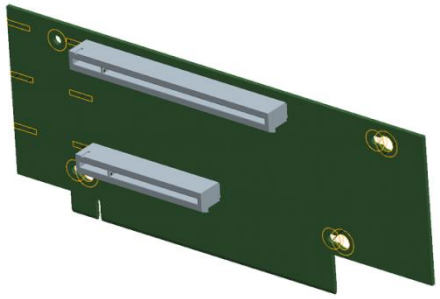
Keyboard and mouse
Bootable USB flash drive
Bootable USB hard disk
Bootable USB optical disk

6.3 SATA

The server board **SHALL** have support up to six SATA ports.

6.4 PCIe and Riser Card Support

The server board **SHALL** provide support for one riser card and **MAY** provide support for two riser cards. The riser card slots can be configured to meet any range of usage models. The following section shows examples of 1U and 2U riser cards:

1U Chassis with 1 add-in card slot	
2U Chassis with 3 add-in card slots.	
2U Chassis with 2 add-in card slots.	

6.5 PCIe Mezzanine Card Support

To broaden the standard on-board feature set, the server board **MAY** provide support for additional I/O Module options.

The **PREFERRED** I/O module **MAY** follow the "Mezzanine Card for Intel V2.0 Motherboard" specification which corresponds to the file name, "Intel_Mezzanine_Card_Design_Specification_v0.5.pdf"

A newer I/O Module specification is also under development at the time of release of V2.0 of this specification.

The new I/O Module is also **PREFERRED** and should follow the "OCP Mezzanine card 2.0 Design Specification" that can be also be found on the www.OpenCompute.org web portal.

The file name of the specification is "Intel_Mezzanine_Card_Design_Specification_v0.5.pdf"

A variety of mezzanine cards are available for Ethernet and storage connectivity. The mezzanine connector pin out and board outline drawing is contained in this specification.

If the common I/O module design is supported the board vendor can utilize the OCP interoperability lab(s) to test the motherboard function with the ecosystem of I/O modules designed to the OCP common I/O module specification. If the vendor chooses to implement a proprietary I/O module design then the motherboard and I/O module interoperability testing is the responsibility of the motherboard vendor.

Support of this module specification is optional and the board vendor may choose to support a different embedded I/O module design.

7. On-board Connectors & Headers

This section identifies the functionality of on-board connectors and headers of the server board that provide an interface to system options/features, on-board platform management, or other user accessible options/features.

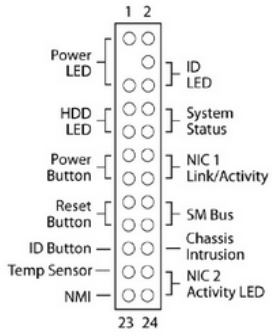
7.1 SSI compatible Front Panel Connector

The server board **MAY** provide a connector for front panel indicators and controls. The functionality and behavior of these buttons and LEDs are not defined by this standard. This connector shall follow the SSI connector definition described below.

Table 4 SSI Front Panel Connector[i]

Description	Pin#		Description
Power LED +	1	2	Front Panel Power
No connect	3	4	ID LED +
Power LED -	5	6	ID LED -
HDD activity LED +	7	8	Status LED Green -
HDD Activity LED -	9	10	Status LED Amber -
Power Button	11	12	NIC 1 Activity LED -
Power Button Ground	13	14	NIC 1 Link LED -
Reset Button	15	16	SMB Sensor DATA
Reset Button Ground	17	18	SMB Sensor Clock
ID Button	19	20	Chassis Intrusion
Front Panel	21	22	NIC 2 Activity LED -
NMI Button	23	24	NIC 2 Link LED -

Figure 7-1 SSI Front Panel Connector



The server board **MAY** provide additional signals via optional pins on the SSI front panel connector.

7.2 Front Panel USB

The server board **SHALL** provide one or more connectors for an external Type-A USB 2.0 connector and **SHALL** follow the connector definition described below.

Table 5 External USB Port Connector

Pin#	Signal Name [i]	Pin#	Signal Name [i]
1	USB_PWR45	2	USB_
3	ICH_P4N_FB	4	ICH_P5N_FB
5	ICH_P4P_FB	6	ICH_P5P_FB
7	GND	8	GND
9	KEY	10	TP_USB45_PIN10

7.3 External Serial Port (external)

The server board **SHALL** provide an external serial connector, either a RJ45 type or a DE9 type connector and **SHALL** follow the connector definition described in Table 6 Serial Header Connector for RJ45or Table 7 Serial Header Connector for DE9.

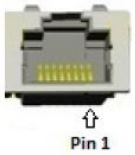


Table 6 Serial Header Connector for RJ45

Pin	Signal Name [i]
1	RTS
2	DTR
3	SOUT
4	GND
5	RI
6	SIN
7	DCD or DSR
8	CTS

Table 7 Serial Header Connector for DE9

Signal Name[i]	Pin#		Signal Name[i]
DCD	1	2	S_IN
S_OUT_N	3	4	DTR
GND	5	6	DSR
RTS	7	8	CTS
GND	9		

7.4 Internal Serial Port

The server board **SHALL** provide a connector for an internal serial interface. This connector **SHALL** follow either of the two connector definitions described below.

Table 8 Serial Port Header Connector

Signal Name[i]	Pin#		Signal Name[i]
DCD	1	2	DSR
S_IN	3	4	RTS
S_OUT_N	5	6	CTS
DTR	7	8	RI
GND	9		key

Table 9 Serial Header Connector

Pin	Signal Name [i]
1	DCD
2	DSR
3	SIN
4	RTS
5	SOUT
6	CTS
7	DTR
8	RI
9	GND

7.5 Single Port AHCI SATA Connector

A server boards that supports single port AHCI SATA connectors capable of supporting up to 6 GB/sec transfer rates **SHALL** follow the connector definition described below.

Table 10 Single Port AHCI SATA Connector[1]

Pin#	Signal Description
9	GND (optional)
8	GND (optional)
7	GND
6	SATA_TXP
5	SATA_TXN
4	GND
3	SATA_RXN
2	SATA_RXP
1	GND

[1] Defined from target point of view. Signal description may vary if defined from host perspective.

7.6 Multiport Mini-SAS/SATA Connectors

The server board that uses multiport mini-SAS/SATA connectors **SHALL** follow this pin out. Each connector **SHALL** support up to four SATA or SAS ports each. The SATA ports **SHALL** be capable of transfer rates of up to 6 Gb/s.

Table 11 Multiport Mini-SAS/SATA Connector

Signal Description	Pin#		Signal Description
GND	A1	B1	GND
SAS0_RX_C_DP	A2	B2	SAS0_TX_C_DP
SAS0_RX_C_DN	A3	B3	SAS0_TX_C_DN
GND	A4	B4	GND
SAS1_RX_C_DP	A5	B5	SAS1_TX_C_DP
SAS1_RX_C_DN	A6	B6	SAS1_TX_C_DN
GND	A7	B7	GND
TP_SAS1_BP_TYPE	A8	B8	SGPIO_SAS1_CLOCK
GND	A9	B9	SGPIO_SAS1_LOAD
SGPIO_SAS1_DATA_OUT	A10	B10	GND
SGPIO_SAS1_DATA_IN	A11	B11	PD_SAS1_CONTROLLER_TYPE
GND	A12	B12	GND
SAS2_RX_C_DP	A13	B13	SAS2_TX_C_DP
SAS2_RX_C_DN	A14	B14	SAS2_TX_C_DN
GND	A15	B15	GND
SAS3_RX_C_DP	A16	B16	SAS3_TX_C_DP
SAS3_RX_C_DN	A17	B17	SAS3_TX_C_DN
GND	A18	B18	GND
GND	G1	G5	GND
GND	G2	G6	GND
GND	G3	G7	GND
GND	G4	G8	GND

8. Power System

The Decathlete server board when used in a server chassis with integrated power supplies **SHALL** consist of 1 or 2 power supplies with the output(s) connected directly to the server board. The power supplies **SHALL** meet the following criteria:

- N+1 capable, hot-swappable
- 80% minimum efficiency measured from 10% to 50% of the rated DC output
- PMbus interface support

8.1 Power Connection for Symmetric Board Outline

When the server board complies with the symmetric layout as described in section 5.1.2, the power supply **SHALL** connector to the server board with a 32 position, double-sided connector. The following vendors and vendor part numbers are examples of the type of connector that **MAY** be used.

- Tyco 1761469 vertical connector
- Tyco 1761468 right-angle connector
- FCI 10046971-100LF Vertical connector
- FCI 10053363-200LF right angle connector

Table 12 Power Connector Definition for Symmetric layout

PCB Top-Side Signal Name	Pin#		PCB Bottom-side Signal Name
+ 12VDC	53-64	1-12	+12VDC
GND	41-52	13-24	GND
PSU_REMOTE_SENSE_P	40	25	TP-TACH
12V_STBY	39	26	PSU_REMOTE_SENSE_N
PS_A	38	27	TP_VIN_GOOD
POK	37	28	CSHARE
Return	36	29	FM_PS_EN_PSU_N
SMB_SCL	35	30	PS_KILL
PSU_PRESENT_N	34	31	RESET_PS
SMB_SDA	33	32	IRQ_PMBUS_ALERT

8.2 Power Connection for Asymmetric Board Outline

The server board connection to the power supply is not defined for the asymmetric layout. The power connection is determined by the OEM or ODM. This is a non-preferred board outline.

8.3 CPU VRM Efficiency

The minimum efficiency for the CPU VRM **SHALL** be 90%.

8.4 Power Connections to the OCP Open Rack

The Decathlete Server Board is not intended for use with the OCP Open Rack, but **MAY** be used with a chassis that is compatible with the OCP Open Rack. When used in the OCP Open Rack, the server enclosure **should** contain a power distribution board (PDB) that provides an electrical interconnector between the 12VDC bus bars in the OCP rack and the Decathlete server board. A cable harness may also be used to provide an interconnect. Regardless of whether a PDB or discrete cable system is used, the Decathlete board and or system **SHALL** contain logic to enable reporting of system input power to the server board.

.Refer to OpenCompute.org for additional specifications or design guides for details on the Open Rack.

9. Platform Management

This section describes the required and optional management features of a Decathlete server board. If any requirement in this section conflicts with the OCP Open Hardware Management Specification for Remote Machine Management V.0.93, the Open Hardware Management Specification for Remote Machine Management V.0.93 is the governing specification.

9.1 Management Controller Firmware Feature Support

This section outlines features that the integrated management controller firmware shall or may support. Support and utilization for some features is dependent on the chassis and other system-level components which may not be installed.

9.1.1 IPMI Features

The management controller **SHALL** support the following IPMI features.

- IPMI Watchdog timer
- chassis device functionality, including power/reset control and BIOS boot flags support
- Field Replaceable Unit (FRU) inventory device functionality
- System Event Log (SEL) device functionality
- Sensor Data Record (SDR) repository device functionality
- Sensor device and sensor scanning/monitoring
- Serial-over-LAN (SOL)

9.1.2 Non IPMI Features

The management controller **SHALL** support the following non-IPMI features.

- In-circuit management firmware update
- Chassis intrusion detection
- Intelligent fan speed control based on thermal sensors. (placement of thermal sensors are the discretion of the vendor)
- Fan redundancy monitoring and support
- Thermal monitoring; including processor, memory, chipset, inlet and outlet temperatures.
- Hot-swap fans
- Power Supply Fan Sensors
- Exit Air Temperature Monitoring
- Platform environment control interface (PECI) thermal management support
- Power supply redundancy monitoring and support
- System status LED and chassis ID LED.
- Power state retention
- Power Supply FW Update

The following features **SHOULD** be supported:

- System Airflow Monitoring
- Ethernet Controller Thermal Monitoring
- power management (e.g. power capping at node level)
- diagnostic beep codes for fault conditions.
- secure lockout of certain front panel functionality
- Integrated KVM
- management of PMBus rev1.2 compliant power supplies
- Power Supply Compatibility

9.2 Advanced Configuration and Power Interface (ACPI)

The server board **SHALL** support for the following ACPI states:

State	Supported	Description
S1	Yes	Sleeping: Context is maintained; equate to processor and chipset clocks being stopped. • The front panel power LED blinks at a rate of 1Hz with a 50% duty cycle • The watchdog timer is stopped • The front panel buttons are unprotected • Fan speed control is determined by available SDRs. Fans may be set to a fixed state, or basic fan management may be applied
S5	Yes	Soft Off • The front panel buttons are not locked • The fans are stopped • The power-up process goes through the normal boot process

Table 13 ACPI Power States

9.3 Power Control Sources

The server board **SHALL** support power control from the following sources. Power control is the ability of an internal or external source to initiate a power-up or power-down activity.

Table 14 Power Control Indicators

Source	External Signal Name or Internal Subsystem	Capabilities
Power button	Front panel power button	Turns power on or off
management controller watchdog timer	Internal management controller timer	Turns power off, or power cycle
Command	Routed through command processor	Turns power on or off, or power cycle
Power state retention	Implemented by means of management controller internal logic	Turns power on when AC power returns
Chipset	Sleep S4/S5 signal (same as POWER_ON)	Turns power on or off
CPU Thermal	CPU Thermtrip	Turns power off
WOL(Wake On LAN)	LAN	Turns power on

9.4 Remote BIOS Update

The Decathlete server board supplier **MAY** provide a BIOS that can be updated remotely under these scenarios:

- Scenario 1: Sample/Audit BIOS settings
  - Return current BIOS settings, or
  - Save/export BIOS settings in a human-readable form that can be restored/imported (as in scenario 2)
- Scenario 2: Update BIOS with pre-configured set of BIOS settings
  - Update/change multiple BIOS settings
  - Reboot
- Scenario 3: BIOS/firmware update with a new revision
  - Load new BIOS/firmware on machine and update, retaining current BIOS settings
  - Reboot

Additionally, the update tools **should** have the following capabilities:

- Update from the operating system over the LAN
- Can complete BIOS update or setup change with a single reboot (no PXE boot, no multiple reboots)
- No user interaction (like prompts)
- BIOS updates and option changes do not take longer than five minutes to complete
- Can be scripted and propagated to multiple machines

9.5 Remote Firmware Update

The Decathlete server board supplier **MAY** provide tool(s) to update the management engine firmware remotely, which does not require any physical input at the system. Remote update means either through out-of-band by the management controller or through logging into the local OS over the network. A remote firmware update may take a maximum of 5 minutes to complete and requires no more than one reset cycle to the system. The OEM/ODM tool **should** support updating the FW and BIOS together or separately, and **should** also provide an option to update only the operational FW region or the entire FW region.

10. Error Handling and Alerts

In general, any correctable and uncorrectable errors should be logged and an error threshold setting should be enabled for both correctable and uncorrectable errors. Once the programmed threshold is reached, an event should be triggered and logged.

The Decathlete server board standard will define a minimal set of error handling and alerts. These features may become a section of this standard, or may be a standalone specification authored by the OCP Hardware Management project.

11. Remote Machine Management

A Revision 1.0 Decathlete server board **SHALL** implement the requirements of the OCP Open Hardware Management Specification for Remote Machine Management (Version 0.93)

A Revision 2.0 Decathlete server board **SHALL** implement the requirements of the OCP Open Hardware Management Specification for Remote Machine Management (Version 1.01)

The latest specification is available at http://opencompute.org/projects/hardware-management/

12. Environmental Requirements

> ☞ NOTE: It is desirable for the product to comply with all requirements in this section. Due to design cycle times and the release of this specification, products designed prior to the release of this specification are not required to comply to be considered compliant.

12.1 General Requirements

The board **SHOULD** meet the following environmental requirements:

- Gaseous Contamination: Severity Level G1 per ANSI/ISA 71.04-1985
- Ambient operating temperature range: 0°C to +45°C
- Operating and storage relative humidity: 10% to 90% (non-condensing)
- Storage temperature range: -40°C to +70°C
- Transportation temperature range: -55°C to +85°C (short-term storage)

12.2 Regulatory Compliance

The server board, when installed into any chassis, **SHOULD** meet the following regulatory compliances:

- FCC Class “A”
- UL Safety

12.3 Vibration and Shock

The motherboard **SHOULD** meet shock and vibration requirements according to the following IEC specifications: IEC78-2-(*) and IEC721-3-(*) Standard & Levels.

Table 9. Vibration and Shock Requirements

	Operating	Non-Operating
Vibration		1g acceleration, 3mm amplitude, 5 to 500 Hz, 10 sweeps at 1 octave / minute for each of the three axes (one sweep is 5 to 500 to 5 Hz)
Shock	2g, half-sine 11mS, 5 shocks for each of the three axes	12g, half-sine 11mS, 10 shocks for each of the three axes

13. Design Standards

The Decathlete server board is expected to conform to design standards, specifications, schematics, PCB stack-up, layout constraints, and thermal and mechanical constraints provided by any of the device manufactures used in the design of the Decathlete server board.

13.1 Connector Labeling

All ports, connectors, and memory slots shall be clearly labeled.

13.2 Documentation

The supplier of the Decathlete server board **SHALL** make available documentation that contains the following information:

- Block Diagram including:
  - PCI to CPU Mapping
  - PCI Speed
  - BMC/Out-of-band Implementation (shared vs. dedicated NICs)
- List of Tools and commands that allow the flashing of firmware
- OOB/BMC OS Integration requirements

14. Prescribed Materials

☞ NOTE: It is desirable for the product to comply with all requirements in this section. Due to design cycle times and the release of this specification, products designed prior to the release of this specification are not required to comply to be considered compliant.

14.1 Disallowed Components

The following components are not used in the design of the motherboard:

- Components disallowed by the European Union's Restriction of Hazardous Substances Directive (RoHS 6)
- Trimmers and/or potentiometers
- Dip switches

14.2 Capacitors and Inductors

The following limitations apply to the use of capacitors:

- Only aluminum organic polymer capacitors made by high quality manufacturers are used; they must be rated 105°C
- All capacitors have a predicted life of at least 50,000 hours at 45°C inlet air temperature, under worst conditions
- Tantalum capacitors using manganese dioxide cathodes are forbidden
- SMT ceramic capacitors with case size > 1206 are forbidden (size 1206 are still allowed when installed far from the PCB edge and with a correct orientation that minimizes risks of cracks)
- Ceramic material for SMT capacitors must be X7R or better material (COG or NP0 type are used in critical portions of the design)
- Only SMT inductors may be used. The use of through-hole inductors is disallowed.

14.3 Component De-rating

For inductors, capacitors, and FETs, a minimum 20% de-rating **SHALL** be used.

15. Reference Documents

- *Advanced Configuration and Power Interface Specification*, Revision 3.0, http://www.acpi.info/.
- *Intelligent Platform Management Bus Communications Protocol Specification*, Version 1.0. 1998. Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Computer Corporation.
- *Intelligent Platform Management Interface Specification*, Version 2.0. 2004. Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Computer Corporation.
- *Platform Support for Serial-over-LAN (SOL), TMode, and Terminal Mode External Architecture Specification*, Version 1.1, 02/01/02, Intel Corporation.
- *Entry-level Electronics-Bay Specification,* Version 3.0, 2001. Intel Corporation, NEC Corporation, Dell Computer Corporation, Data General, a division of EMC, International Business Machines Corporation, Silicon Graphics, Inc., and Compaq Computer Corporation.
- *Trusted Platform Module (TPM) Specifications*. Trusted Computing Group
- PCI Express®225 W/300 W High Power Card Electromechanical Specification Revision 1.0
- *Intel RAID Quick Reference Guide,* Version G46033-003. Intel Corporation

[i] Refer to Server System Infrastructure (SSI) Specification for further details on signals.