# S2B

PCB: DA0S2BMB8D0
PCBA: 31S2BMB0000
FAB: 4
REV: 3.016
DM: MATT YU
DE: PETER / HANK / YULIN
SKU: I350 + AST2300

DATE:MON JUL 15 18:45 2013

COVER PAGE

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# SMLF

U94
DGA^1000014
I0

HSX_EP_EXT

| | | | | | |
|---|---|---|---|---|---|
| 141 | IN | CLK_100M_CPU0_QPI_DP | CL41 | BCLK0_DP | |
| 141 | IN | CLK_100M_CPU0_QPI_DN | CN41 | BCLK0_DN | |
| 141 | IN | CLK_100M_CPU0_PE_DP | BA45 | BCLK1_DP | |
| 141 | IN | CLK_100M_CPU0_PE_DN | AW45 | BCLK1_DN | |
| 40 | IN | PWRGD_CPU0_AB_DRAM_G | CH16 | DRAM_PWR_OK_C01 | |
| 40 | IN | PWRGD_CPU0_CD_DRAM_G | W29 | DRAM_PWR_OK_C23 | |
| 52 51 50 49 48 47 | OUT | M_AB_RESET_N | DC15 | DDR_RESET_C01_N | |
| 58 57 56 55 54 53 | OUT | M_CD_RESET_N | C23 | DDR_RESET_C23_N | |
| 34 41 38 37 | BI | H_CPU0_MEMAB_MEMHOT_G_N | CL33 | MEM_HOT_C01_N | |
| 34 41 38 37 | BI | H_CPU0_MEMCD_MEMHOT_G_N | P36 | MEM_HOT_C23_N | |
| 47 | OUT | M_AB_CPU_VREF | BY16 | DDR01_VREF | |
| | | TP_CPU0_RSVD_28 | CP40 | RSVD_28 | |
| | | TP_CPU0_RSVD_27 | CF40 | RSVD_27 | |
| 53 | OUT | M_CD_CPU_VREF | T40 | DDR23_VREF | |
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| 10 | OUT | SMB_DDR_AB_SCL_G | CK42 | DDR_SCL_C01 | |
| 10 | BI | SMB_DDR_AB_SDA_G | CM42 | DDR_SDA_C01 | |
| 10 | OUT | SMB_DDR_CD_SCL_G | V40 | DDR_SCL_C23 | |
| 10 | BI | SMB_DDR_CD_SDA_G | Y40 | DDR_SDA_C23 | |
| 74 | OUT | SMB_PE_HP_CPU0_SCL_GTL | B46 | PE_HP_SCL | |
| 74 | BI | SMB_PE_HP_CPU0_SDA_GTL | D46 | PE_HP_SDA | |
| 21 44 | IN | XDP_CPU_OBSEN_B_MBP7_G_N | AW43 | BPM_7_N | |
| 21 44 | IN | XDP_CPU_OBSEN_B_MBP6_G_N | BA43 | BPM_6_N | |
| 44 | IN | XDP_CPU0_OBSDATA_A_MBP5_G_N | BD46 | BPM_5_N | |
| 44 | IN | XDP_CPU0_OBSDATA_A_MBP4_G_N | BE45 | BPM_4_N | |
| 44 | IN | XDP_CPU0_OBSDATA_A_MBP3_G_N | BF46 | BPM_3_N | |
| 44 | IN | XDP_CPU0_OBSDATA_A_MBP2_G_N | BE47 | BPM_2_N | |
| 21 | BI | XDP_CPU_MBP1_G_N | BB44 | BPM_1_N | |
| 21 | BI | XDP_CPU_MBP0_G_N | BC43 | BPM_0_N | |
| 46 44 | IN | XDP_CPU0_PREQ_G_N | CW49 | PREQ_N | |
| 46 44 | IN | XDP_CPU0_PRDY_G_N | CU49 | PRDY_N | |
| 45 | IN | XDP_CPU0_TDI_G | CF42 | TDI | |
| 21 45 44 | IN | XDP_CPU_TCK_G | CA45 | TCK | |
| 21 45 44 | IN | XDP_CPU_TMS_G | BY46 | TMS | |
| 21 45 44 | IN | XDP_CPU_TRST_G_N | CV50 | TRST_N | |

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| PWRGOOD | BJ53 | PWRGD_CPU0_G_R | R1293 49.9 1% 1/16W CHIP 0402LF CS04992FB31 | PWRGD_CPU0_G 40 41 44 |
| RESET_N | CR43 | RST_CPU0_G_R_N | R1312 49.9 1% 1/16W CHIP 0402LF | RST_CPU0_G_N 40 41 44 |
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| BMCINIT | AM48 | PU_CPU0_BMCINIT | | 32 |
| TXT_AGENT | AH52 | PU_CPU0_TXT_AGENT | | 32 |
| TXT_PLTEN | AF52 | PD_CPU0_TXT_PLTEN | | 32 |
| BIST_ENABLE | AJ43 | PD_CPU0_BIST_ENABLE | | 32 |
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| SOCKET_ID_1 | CC53 | PU_CPU0_SOCKET_ID_1 | | 32 |
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| RSVD_44 | AY46 | TP_CPU0_RSVD_44 | | |
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| RSVD_42 | BD48 | TP_CPU0_RSVD_42 | | |
| TDO | CG41 | XDP_CPU0_TDO_G | | 45 |

PVCCIO

R1326 100 1% 1/16W CHIP 0402LF TMP_QCS11002FB22
R1328 100 1% 1/16W CHIP 0402LF TMP_QCS11002FB22

PVCCIO

R1333 100 1% 1/16W CHIP 0402LF
R1332 49.9 1% 1/16W CHIP 0402LF

| | | | | | |
|---|---|---|---|---|---|
| 10 | OUT | SVID_ALERT_CPU0_R1_G | R1318 220 1% 1/16W CHIP 0402LF TMP_QCS12202FB14 | SVID_ALERT_CPU0_N | IN 161 167 170 |
| 10 | BI | SVID_DIO_CPU0 | R1317 0 1% 1/16W CHIP 0402LF TMP_QCS00002FB00 | SVID_DIO_CPU0_R1 | BI 161 167 170 |
| 10 | IN | SVID_CLK_CPU0 | R1320 0 1% 1/16W CHIP 0402LF TMP_QCS00002FB00 | SVID_CLK_CPU0_R1 | OUT 161 167 170 |

CPU HASWELL SOCKET0 (1 OF 11)

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SMLF
LGA2011_R3
U94
DGA^1000014
I0

HSX_EP_EXT

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| TP_CPU0_RSVD_75 | AR55 | RSVD_75 | RSVD_81 | BM46 | TP_CPU0_RSVD_81 |
| TP_CPU0_RSVD_74 | AU55 | RSVD_74 | RSVD_80 | BP46 | TP_CPU0_RSVD_80 |
| TP_CPU0_RSVD_73 | H58 | RSVD_73 | RSVD_79 | DA57 | TP_CPU0_RSVD_79 |
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| TP_CPU0_RSVD_71 | D56 | RSVD_71 | RSVD_77 | DD54 | TP_CPU0_RSVD_77 |
| TP_CPU0_RSVD_70 | F56 | RSVD_70 | RSVD_76 | DE55 | TP_CPU0_RSVD_76 |
| TP_CPU0_RSVD_68 | DE53 | RSVD_68 | TEST_1 | DB4 | PD_CPU0_TEST_1 |
| | | | TEST_0 | DB2 | PD_CPU0_TEST_0 |
| TP_CPU0_RSVD_67 | BJ43 | RSVD_67 | TEST_3 | C3 | PD_CPU0_TEST_3 |
| TP_CPU0_RSVD_66 | BH44 | RSVD_66 | TEST_2 | D2 | PD_CPU0_TEST_2 |
| TP_CPU0_RSVD_65 | BJ45 | RSVD_65 | RSVD_82 | CN43 | TP_CPU0_RSVD_82 |
| TP_CPU0_RSVD_64 | BE43 | RSVD_64 | RSVD_83 | CL43 | TP_CPU0_RSVD_83 |
| TP_CPU0_RSVD_63 | BG43 | RSVD_63 | PWR_DEBUG_N | AC41 | CRB_CPU_PWR_DEBUG |
| TP_CPU0_RSVD_62 | BH46 | RSVD_62 | FIVR_FAULT | CY40 | H_CPU0_FIVR_FAULT_G |
| TP_CPU0_RSVD_61 | BF44 | RSVD_61 | RSVD_36 | B54 | TP_CPU0_RSVD_36 |
| TP_CPU0_RSVD_60 | BD44 | RSVD_60 | RSVD_35 | CW51 | TP_CPU0_RSVD_35 |
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| TP_CPU0_RSVD_51 | BY44 | RSVD_51 | RSVD_41 | AL55 | TP_CPU0_RSVD_41 |
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| TP_CPU0_RSVD_16 | R43 | RSVD_16 | | | |
| TP_CPU0_RSVD_15 | V42 | RSVD_15 | | | |
| TP_CPU0_RSVD_14 | W41 | RSVD_14 | | | |

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IN 44 22
OUT 41 34

IN 44 22

| | | | | |
|---|---|---|---|---|
| R1337 | 49.9 | 1% | 1/16W | CHIP | CS04992FB31 0402LF |
| R1340 | 49.9 | 1% | 1/16W | CHIP | CS04992FB31 0402LF |
| R713 | 49.9 | 1% | 1/16W | CHIP | CS04992FB31 0402LF |
| R711 | 49.9 | 1% | 1/16W | CHIP | CS04992FB31 0402LF |

# CPU HASWELL SOCKET0 (2 OF 11)

Quanta

| | | | | |
|---|---|---|---|---|
| DEPARTMENT | CCBU | PROJCET | S2B | DOCUMENT NUMBER | DA0S2BMB8A0 | REV | 1 |
| DESIGNER | NICK | | | | | | |
| REVIEWER | PETER,YULIN,MATT | SIZE | C | DATE | Mon Nov 16 11:51:09 2015 | SHEET | 11 OF 188 |

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I0
DGA^1000014
U94

HSX_EP_EXT

M_A_DQ<63:0>

| | | | |
|---|---|---|---|
| 63 | CK38 | DDR0_DQ_63 | |
| 62 | CM38 | DDR0_DQ_62 | |
| 61 | CK34 | DDR0_DQ_61 | |
| 60 | CM34 | DDR0_DQ_60 | |
| 59 | CJ39 | DDR0_DQ_59 | |
| 58 | CL39 | DDR0_DQ_58 | |
| 57 | CJ35 | DDR0_DQ_57 | |
| 56 | CL35 | DDR0_DQ_56 | |
| 55 | CD38 | DDR0_DQ_55 | |
| 54 | CF38 | DDR0_DQ_54 | |
| 53 | CD34 | DDR0_DQ_53 | |
| 52 | CF34 | DDR0_DQ_52 | |
| 51 | CC39 | DDR0_DQ_51 | |
| 50 | CE39 | DDR0_DQ_50 | |
| 49 | CC35 | DDR0_DQ_49 | |
| 48 | CE35 | DDR0_DQ_48 | |
| 47 | CC31 | DDR0_DQ_47 | |
| 46 | CE31 | DDR0_DQ_46 | |
| 45 | CC27 | DDR0_DQ_45 | |
| 44 | CE27 | DDR0_DQ_44 | |
| 43 | CB32 | DDR0_DQ_43 | |
| 42 | CD32 | DDR0_DQ_42 | |
| 41 | CB28 | DDR0_DQ_41 | |
| 40 | CD28 | DDR0_DQ_40 | |
| 39 | CJ31 | DDR0_DQ_39 | |
| 38 | CL31 | DDR0_DQ_38 | |
| 37 | CJ27 | DDR0_DQ_37 | |
| 36 | CL27 | DDR0_DQ_36 | |
| 35 | CH32 | DDR0_DQ_35 | |
| 34 | CK32 | DDR0_DQ_34 | |
| 33 | CH28 | DDR0_DQ_33 | |
| 32 | CK28 | DDR0_DQ_32 | |
| 31 | CL13 | DDR0_DQ_31 | |
| 30 | CM12 | DDR0_DQ_30 | |
| 29 | CD14 | DDR0_DQ_29 | |
| 28 | CC13 | DDR0_DQ_28 | |
| 27 | CH14 | DDR0_DQ_27 | |
| 26 | CM14 | DDR0_DQ_26 | |
| 25 | CG15 | DDR0_DQ_25 | |
| 24 | CE13 | DDR0_DQ_24 | |
| 23 | CJ9 | DDR0_DQ_23 | |
| 22 | CK8 | DDR0_DQ_22 | |
| 21 | CE11 | DDR0_DQ_21 | |
| 20 | CD10 | DDR0_DQ_20 | |
| 19 | CJ11 | DDR0_DQ_19 | |
| 18 | CK10 | DDR0_DQ_18 | |
| 17 | CF8 | DDR0_DQ_17 | |
| 16 | CE9 | DDR0_DQ_16 | |
| 15 | BY12 | DDR0_DQ_15 | |
| 14 | CA11 | DDR0_DQ_14 | |
| 13 | BU15 | DDR0_DQ_13 | |
| 12 | BT14 | DDR0_DQ_12 | |
| 11 | BY14 | DDR0_DQ_11 | |
| 10 | BW13 | DDR0_DQ_10 | |
| 9 | BU11 | DDR0_DQ_9 | |
| 8 | BT12 | DDR0_DQ_8 | |
| 7 | CB6 | DDR0_DQ_7 | |
| 6 | CA7 | DDR0_DQ_6 | |
| 5 | BU9 | DDR0_DQ_5 | |
| 4 | BT8 | DDR0_DQ_4 | |
| 3 | CB8 | DDR0_DQ_3 | |
| 2 | CA9 | DDR0_DQ_2 | |
| 1 | BT6 | DDR0_DQ_1 | |
| 0 | BU7 | DDR0_DQ_0 | |

M_A_ECC<7..0>

| | | |
|---|---|---|
| 7 | CR11 | DDR0_ECC_7 |
| 6 | CP10 | DDR0_ECC_6 |
| 5 | CN9 | DDR0_ECC_5 |
| 4 | CP8 | DDR0_ECC_4 |
| 3 | CU11 | DDR0_ECC_3 |
| 2 | CW11 | DDR0_ECC_2 |
| 1 | CV8 | DDR0_ECC_1 |
| 0 | CT8 | DDR0_ECC_0 |

M_A_CLK_DP<3..0>

| | | |
|---|---|---|
| 3 | CC19 | DDR0_CLK_DP_3 |
| 2 | CD20 | DDR0_CLK_DP_2 |
| 1 | CD18 | DDR0_CLK_DP_1 |
| 0 | CC21 | DDR0_CLK_DP_0 |

M_A_CLK_DN<3..0>

| | | |
|---|---|---|
| 3 | CE19 | DDR0_CLK_DN_3 |
| 2 | CF20 | DDR0_CLK_DN_2 |
| 1 | CF18 | DDR0_CLK_DN_1 |
| 0 | CE21 | DDR0_CLK_DN_0 |

M_A_BG<1:0>

| | | |
|---|---|---|
| 1 | CN17 | DDR0_BG_1 |
| 0 | CL17 | DDR0_BG_0 |

M_A_BA<1:0>

| | | |
|---|---|---|
| 1 | CH20 | DDR0_BA_1 |
| 0 | CL21 | DDR0_BA_0 |

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M_A_DQS_DP<17:0>

| | | |
|---|---|---|
| DDR0_DQS_DP_17 | CU9 | 17 |
| DDR0_DQS_DP_16 | CM36 | 16 |
| DDR0_DQS_DP_15 | CF36 | 15 |
| DDR0_DQS_DP_14 | CE29 | 14 |
| DDR0_DQS_DP_13 | CL29 | 13 |
| DDR0_DQS_DP_12 | CG13 | 12 |
| DDR0_DQS_DP_11 | CG9 | 11 |
| DDR0_DQS_DP_10 | BU13 | 10 |
| DDR0_DQS_DP_9 | BV8 | 9 |
| DDR0_DQS_DP_8 | CV10 | 8 |
| DDR0_DQS_DP_7 | CJ37 | 7 |
| DDR0_DQS_DP_6 | CC37 | 6 |
| DDR0_DQS_DP_5 | CD30 | 5 |
| DDR0_DQS_DP_4 | CK30 | 4 |
| DDR0_DQS_DP_3 | CK14 | 3 |
| DDR0_DQS_DP_2 | CH10 | 2 |
| DDR0_DQS_DP_1 | BV12 | 1 |
| DDR0_DQS_DP_0 | BY6 | 0 |

M_A_DQS_DN<17:0>

| | | |
|---|---|---|
| DDR0_DQS_DN_17 | CW9 | 17 |
| DDR0_DQS_DN_16 | CK36 | 16 |
| DDR0_DQS_DN_15 | CD36 | 15 |
| DDR0_DQS_DN_14 | CC29 | 14 |
| DDR0_DQS_DN_13 | CJ29 | 13 |
| DDR0_DQS_DN_12 | CF14 | 12 |
| DDR0_DQS_DN_11 | CH8 | 11 |
| DDR0_DQS_DN_10 | BV14 | 10 |
| DDR0_DQS_DN_9 | BW9 | 9 |
| DDR0_DQS_DN_8 | CT10 | 8 |
| DDR0_DQS_DN_7 | CL37 | 7 |
| DDR0_DQS_DN_6 | CE37 | 6 |
| DDR0_DQS_DN_5 | CF30 | 5 |
| DDR0_DQS_DN_4 | CM30 | 4 |
| DDR0_DQS_DN_3 | CJ13 | 3 |
| DDR0_DQS_DN_2 | CG11 | 2 |
| DDR0_DQS_DN_1 | BW11 | 1 |
| DDR0_DQS_DN_0 | BV6 | 0 |

M_A_MA<17:0>

| | | |
|---|---|---|
| DDR0_MA_17 | CD24 | 17 |
| DDR0_MA_16 | CL23 | 16 |
| DDR0_MA_15 | CL25 | 15 |
| DDR0_MA_14 | CJ21 | 14 |
| DDR0_MA_13 | CE23 | 13 |
| DDR0_MA_12 | CR17 | 12 |
| DDR0_MA_11 | CP18 | 11 |
| DDR0_MA_10 | CP24 | 10 |
| DDR0_MA_9 | CK18 | 9 |
| DDR0_MA_8 | CJ19 | 8 |
| DDR0_MA_7 | CH18 | 7 |
| DDR0_MA_6 | CN19 | 6 |
| DDR0_MA_5 | CL19 | 5 |
| DDR0_MA_4 | CP20 | 4 |
| DDR0_MA_3 | CN21 | 3 |
| DDR0_MA_2 | CT22 | 2 |
| DDR0_MA_1 | CR21 | 1 |
| DDR0_MA_0 | CP22 | 0 |

M_A_CKE<5..0>

| | | |
|---|---|---|
| DDR0_CKE_5 | CC15 | 5 |
| DDR0_CKE_4 | CN15 | 4 |
| DDR0_CKE_3 | CC17 | 3 |
| DDR0_CKE_2 | CF16 | 2 |
| DDR0_CKE_1 | CE17 | 1 |
| DDR0_CKE_0 | CJ17 | 0 |

M_A_ODT<5..0>

| | | |
|---|---|---|
| DDR0_ODT_5 | CE25 | 5 |
| DDR0_ODT_4 | CF24 | 4 |
| DDR0_ODT_3 | CC23 | 3 |
| DDR0_ODT_2 | CJ23 | 2 |
| DDR0_ODT_1 | CN25 | 1 |
| DDR0_ODT_0 | CF22 | 0 |

M_A_CS_N<9:0>

| | | |
|---|---|---|
| DDR0_CS9_N | CK26 | 9 |
| DDR0_CS8_N | CK24 | 8 |
| DDR0_CS7_N_CID_4 | CD26 | 7 |
| DDR0_CS6_N_CID_3 | CH26 | 6 |
| DDR0_CS5_N | CH24 | 5 |
| DDR0_CS4_N | CK22 | 4 |
| DDR0_CS3_N_CID_1 | CC25 | 3 |
| DDR0_CS2_N_CID_0 | CF26 | 2 |
| DDR0_CS1_N | CH22 | 1 |
| DDR0_CS0_N | CD22 | 0 |

| | | |
|---|---|---|
| DDR0_CID_2 | CJ25 | M_A_C<2> |
| DDR0_ACT_N | CK16 | M_A_ACT_N |
| DDR0_ALERT_N | CD16 | M_A_ALERT_N |
| DDR0_PAR | CK20 | M_A_PAR |

# CPU HASWELL SOCKET0 (3 OF 11)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | REVIEWER PETER,YULIN,MATT | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | | | SIZE C | DATE Mon Nov 16 11:51:10 2015 | SHEET 12 OF 188 | |

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U94
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HSX_EP_EXT

M_B_DQ<63:0>

| | | | |
|---|---|---|---|
| 63 | DE39 | DDR1_DQ_63 | |
| 62 | DF38 | DDR1_DQ_62 | |
| 61 | DB36 | DDR1_DQ_61 | |
| 60 | DC35 | DDR1_DQ_60 | |
| 59 | DA39 | DDR1_DQ_59 | |
| 58 | DC39 | DDR1_DQ_58 | |
| 57 | DF36 | DDR1_DQ_57 | |
| 56 | DC37 | DDR1_DQ_56 | |
| 55 | CT38 | DDR1_DQ_55 | |
| 54 | CV38 | DDR1_DQ_54 | |
| 53 | CT34 | DDR1_DQ_53 | |
| 52 | CV34 | DDR1_DQ_52 | |
| 51 | CR39 | DDR1_DQ_51 | |
| 50 | CU39 | DDR1_DQ_50 | |
| 49 | CR35 | DDR1_DQ_49 | |
| 48 | CU35 | DDR1_DQ_48 | |
| 47 | DE33 | DDR1_DQ_47 | |
| 46 | DA33 | DDR1_DQ_46 | |
| 45 | CY28 | DDR1_DQ_45 | |
| 44 | DB28 | DDR1_DQ_44 | |
| 43 | DF34 | DDR1_DQ_43 | |
| 42 | DC33 | DDR1_DQ_42 | |
| 41 | DB30 | DDR1_DQ_41 | |
| 40 | DA29 | DDR1_DQ_40 | |
| 39 | CR31 | DDR1_DQ_39 | |
| 38 | CU31 | DDR1_DQ_38 | |
| 37 | CR27 | DDR1_DQ_37 | |
| 36 | CU27 | DDR1_DQ_36 | |
| 35 | CP32 | DDR1_DQ_35 | |
| 34 | CT32 | DDR1_DQ_34 | |
| 33 | CP28 | DDR1_DQ_33 | |
| 32 | CT28 | DDR1_DQ_32 | |
| 31 | DF10 | DDR1_DQ_31 | |
| 30 | DE9 | DDR1_DQ_30 | |
| 29 | CY6 | DDR1_DQ_29 | |
| 28 | DA5 | DDR1_DQ_28 | |
| 27 | DC11 | DDR1_DQ_27 | |
| 26 | DE11 | DDR1_DQ_26 | |
| 25 | DB8 | DDR1_DQ_25 | |
| 24 | DA7 | DDR1_DQ_24 | |
| 23 | CR5 | DDR1_DQ_23 | |
| 22 | CU5 | DDR1_DQ_22 | |
| 21 | CP2 | DDR1_DQ_21 | |
| 20 | CR1 | DDR1_DQ_20 | |
| 19 | CP6 | DDR1_DQ_19 | |
| 18 | CT6 | DDR1_DQ_18 | |
| 17 | CV2 | DDR1_DQ_17 | |
| 16 | CR3 | DDR1_DQ_16 | |
| 15 | CL3 | DDR1_DQ_15 | |
| 14 | CK6 | DDR1_DQ_14 | |
| 13 | CF6 | DDR1_DQ_13 | |
| 12 | CE5 | DDR1_DQ_12 | |
| 11 | CM4 | DDR1_DQ_11 | |
| 10 | CL5 | DDR1_DQ_10 | |
| 9 | CF4 | DDR1_DQ_9 | |
| 8 | CE3 | DDR1_DQ_8 | |
| 7 | BY2 | DDR1_DQ_7 | |
| 6 | CA1 | DDR1_DQ_6 | |
| 5 | BT2 | DDR1_DQ_5 | |
| 4 | BT4 | DDR1_DQ_4 | |
| 3 | CB4 | DDR1_DQ_3 | |
| 2 | CA3 | DDR1_DQ_2 | |
| 1 | BU1 | DDR1_DQ_1 | |
| 0 | BV4 | DDR1_DQ_0 | |

M_B_ECC<7..0>

| | | |
|---|---|---|
| 7 | DE13 | DDR1_ECC_7 |
| 6 | DC13 | DDR1_ECC_6 |
| 5 | CT14 | DDR1_ECC_5 |
| 4 | CR13 | DDR1_ECC_4 |
| 3 | DF14 | DDR1_ECC_3 |
| 2 | DD14 | DDR1_ECC_2 |
| 1 | CV14 | DDR1_ECC_1 |
| 0 | CU13 | DDR1_ECC_0 |

M_B_CLK_DP<3..0>

| | | |
|---|---|---|
| 3 | DE19 | DDR1_CLK_DP_3 |
| 2 | DF20 | DDR1_CLK_DP_2 |
| 1 | DF18 | DDR1_CLK_DP_1 |
| 0 | DE21 | DDR1_CLK_DP_0 |

M_B_CLK_DN<3..0>

| | | |
|---|---|---|
| 3 | DC19 | DDR1_CLK_DN_3 |
| 2 | DD20 | DDR1_CLK_DN_2 |
| 1 | DD18 | DDR1_CLK_DN_1 |
| 0 | DC21 | DDR1_CLK_DN_0 |

M_B_BG<1:0>

| | | |
|---|---|---|
| 1 | CP16 | DDR1_BG_1 |
| 0 | CV16 | DDR1_BG_0 |

M_B_BA<1:0>

| | | |
|---|---|---|
| 1 | CV22 | DDR1_BA_1 |
| 0 | CW23 | DDR1_BA_0 |

M_B_DQS_DP<17:0>

| | | |
|---|---|---|
| DDR1_DQS_DP_17 | CW13 | 17 |
| DDR1_DQS_DP_16 | DD36 | 16 |
| DDR1_DQS_DP_15 | CV36 | 15 |
| DDR1_DQS_DP_14 | DA31 | 14 |
| DDR1_DQS_DP_13 | CU29 | 13 |
| DDR1_DQS_DP_12 | DC7 | 12 |
| DDR1_DQS_DP_11 | CW3 | 11 |
| DDR1_DQS_DP_10 | CH4 | 10 |
| DDR1_DQS_DP_9 | BV2 | 9 |
| DDR1_DQS_DP_8 | DB14 | 8 |
| DDR1_DQS_DP_7 | DB38 | 7 |
| DDR1_DQS_DP_6 | CR37 | 6 |
| DDR1_DQS_DP_5 | DD32 | 5 |
| DDR1_DQS_DP_4 | CT30 | 4 |
| DDR1_DQS_DP_3 | DB10 | 3 |
| DDR1_DQS_DP_2 | CT4 | 2 |
| DDR1_DQS_DP_1 | CJ5 | 1 |
| DDR1_DQS_DP_0 | BY4 | 0 |

M_B_DQS_DN<17:0>

| | | |
|---|---|---|
| DDR1_DQS_DN_17 | CY14 | 17 |
| DDR1_DQS_DN_16 | DE37 | 16 |
| DDR1_DQS_DN_15 | CT36 | 15 |
| DDR1_DQS_DN_14 | CY32 | 14 |
| DDR1_DQS_DN_13 | CR29 | 13 |
| DDR1_DQS_DN_12 | DD8 | 12 |
| DDR1_DQS_DN_11 | CU3 | 11 |
| DDR1_DQS_DN_10 | CG3 | 10 |
| DDR1_DQS_DN_9 | BW1 | 9 |
| DDR1_DQS_DN_8 | DA13 | 8 |
| DDR1_DQS_DN_7 | DA37 | 7 |
| DDR1_DQS_DN_6 | CU37 | 6 |
| DDR1_DQS_DN_5 | DB32 | 5 |
| DDR1_DQS_DN_4 | CV30 | 4 |
| DDR1_DQS_DN_3 | DC9 | 3 |
| DDR1_DQS_DN_2 | CV4 | 2 |
| DDR1_DQS_DN_1 | CH6 | 1 |
| DDR1_DQS_DN_0 | BW3 | 0 |

M_B_MA<17:0>

| | | |
|---|---|---|
| DDR1_MA_17 | CT24 | 17 |
| DDR1_MA_16 | CY24 | 16 |
| DDR1_MA_15 | CV24 | 15 |
| DDR1_MA_14 | CN23 | 14 |
| DDR1_MA_13 | CW25 | 13 |
| DDR1_MA_12 | CW17 | 12 |
| DDR1_MA_11 | CV18 | 11 |
| DDR1_MA_10 | CR23 | 10 |
| DDR1_MA_9 | CY18 | 9 |
| DDR1_MA_8 | DA19 | 8 |
| DDR1_MA_7 | CT18 | 7 |
| DDR1_MA_6 | CW19 | 6 |
| DDR1_MA_5 | CY20 | 5 |
| DDR1_MA_4 | CR19 | 4 |
| DDR1_MA_3 | CW21 | 3 |
| DDR1_MA_2 | CV20 | 2 |
| DDR1_MA_1 | DA21 | 1 |
| DDR1_MA_0 | CY22 | 0 |

M_B_CKE<5..0>

| | | |
|---|---|---|
| DDR1_CKE_5 | DA15 | 5 |
| DDR1_CKE_4 | CY16 | 4 |
| DDR1_CKE_3 | DF16 | 3 |
| DDR1_CKE_2 | DD16 | 2 |
| DDR1_CKE_1 | DC17 | 1 |
| DDR1_CKE_0 | DA17 | 0 |

M_B_ODT<5..0>

| | | |
|---|---|---|
| DDR1_ODT_5 | DD26 | 5 |
| DDR1_ODT_4 | DA25 | 4 |
| DDR1_ODT_3 | DC25 | 3 |
| DDR1_ODT_2 | DC23 | 2 |
| DDR1_ODT_1 | DE25 | 1 |
| DDR1_ODT_0 | DD22 | 0 |

M_B_CS_N<9:0>

| | | |
|---|---|---|
| DDR1_CS9_N | DF26 | 9 |
| DDR1_CS8_N | DF24 | 8 |
| DDR1_CS7_N_CID_4 | CV26 | 7 |
| DDR1_CS6_N_CID_3 | CY26 | 6 |
| DDR1_CS5_N | DD24 | 5 |
| DDR1_CS4_N | DA23 | 4 |
| DDR1_CS3_N_CID_1 | CP26 | 3 |
| DDR1_CS2_N_CID_0 | CT26 | 2 |
| DDR1_CS1_N | DE23 | 1 |
| DDR1_CS0_N | DF22 | 0 |

| | | |
|---|---|---|
| DDR1_CID_2 | CR25 | M_B_C<2> |
| DDR1_ACT_N | CT16 | M_B_ACT_N |
| DDR1_ALERT_N | CR15 | M_B_ALERT_N |
| DDR1_PAR | CT20 | M_B_PAR |

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# CPU HASWELL SOCKET0 (4 OF 11)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:51:12 2015 | SHEET: 13 OF 188 |

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I0

HSX_EP_EXT

| | | | |
|---|---|---|---|
| 55 54 53 BI | M_C_DQ<63:0> | | |
| 63 | AL7 | DDR2_DQ_63 | |
| 62 | AK8 | DDR2_DQ_62 | |
| 61 | AE9 | DDR2_DQ_61 | |
| 60 | AE7 | DDR2_DQ_60 | |
| 59 | AL9 | DDR2_DQ_59 | |
| 58 | AK10 | DDR2_DQ_58 | |
| 57 | AG7 | DDR2_DQ_57 | |
| 56 | AG9 | DDR2_DQ_56 | |
| 55 | AL15 | DDR2_DQ_55 | |
| 54 | AK14 | DDR2_DQ_54 | |
| 53 | AF14 | DDR2_DQ_53 | |
| 52 | AG15 | DDR2_DQ_52 | |
| 51 | AL13 | DDR2_DQ_51 | |
| 50 | AK12 | DDR2_DQ_50 | |
| 49 | AF12 | DDR2_DQ_49 | |
| 48 | AE11 | DDR2_DQ_48 | |
| 47 | Y8 | DDR2_DQ_47 | |
| 46 | AA9 | DDR2_DQ_46 | |
| 45 | U11 | DDR2_DQ_45 | |
| 44 | T10 | DDR2_DQ_44 | |
| 43 | AB8 | DDR2_DQ_43 | |
| 42 | AA11 | DDR2_DQ_42 | |
| 41 | W11 | DDR2_DQ_41 | |
| 40 | U9 | DDR2_DQ_40 | |
| 39 | M6 | DDR2_DQ_39 | |
| 38 | K6 | DDR2_DQ_38 | |
| 37 | L9 | DDR2_DQ_37 | |
| 36 | J9 | DDR2_DQ_36 | |
| 35 | P6 | DDR2_DQ_35 | |
| 34 | R7 | DDR2_DQ_34 | |
| 33 | K8 | DDR2_DQ_33 | |
| 32 | N9 | DDR2_DQ_32 | |
| 31 | T24 | DDR2_DQ_31 | |
| 30 | V24 | DDR2_DQ_30 | |
| 29 | T28 | DDR2_DQ_29 | |
| 28 | V28 | DDR2_DQ_28 | |
| 27 | R23 | DDR2_DQ_27 | |
| 26 | U23 | DDR2_DQ_26 | |
| 25 | R27 | DDR2_DQ_25 | |
| 24 | U27 | DDR2_DQ_24 | |
| 23 | AC31 | DDR2_DQ_23 | |
| 22 | AE31 | DDR2_DQ_22 | |
| 21 | AA35 | DDR2_DQ_21 | |
| 20 | AC35 | DDR2_DQ_20 | |
| 19 | AB30 | DDR2_DQ_19 | |
| 18 | AD30 | DDR2_DQ_18 | |
| 17 | AB34 | DDR2_DQ_17 | |
| 16 | AD34 | DDR2_DQ_16 | |
| 15 | W31 | DDR2_DQ_15 | |
| 14 | T32 | DDR2_DQ_14 | |
| 13 | R35 | DDR2_DQ_13 | |
| 12 | U35 | DDR2_DQ_12 | |
| 11 | T30 | DDR2_DQ_11 | |
| 10 | V30 | DDR2_DQ_10 | |
| 9 | U33 | DDR2_DQ_9 | |
| 8 | V34 | DDR2_DQ_8 | |
| 7 | U37 | DDR2_DQ_7 | |
| 6 | T38 | DDR2_DQ_6 | |
| 5 | AC39 | DDR2_DQ_5 | |
| 4 | AE37 | DDR2_DQ_4 | |
| 3 | Y38 | DDR2_DQ_3 | |
| 2 | R37 | DDR2_DQ_2 | |
| 1 | AA37 | DDR2_DQ_1 | |
| 0 | AD38 | DDR2_DQ_0 | |

| | | | |
|---|---|---|---|
| 55 54 53 BI | M_C_ECC<7..0> | | |
| 7 | AB24 | DDR2_ECC_7 | |
| 6 | AD24 | DDR2_ECC_6 | |
| 5 | AB28 | DDR2_ECC_5 | |
| 4 | AD28 | DDR2_ECC_4 | |
| 3 | AA23 | DDR2_ECC_3 | |
| 2 | AC23 | DDR2_ECC_2 | |
| 1 | AA27 | DDR2_ECC_1 | |
| 0 | AC27 | DDR2_ECC_0 | |
| 55 54 53 OUT | M_C_CLK_DP<3..0> | | |
| 3 | AA19 | DDR2_CLK_DP_3 | |
| 2 | AB18 | DDR2_CLK_DP_2 | |
| 1 | AB20 | DDR2_CLK_DP_1 | |
| 0 | AA17 | DDR2_CLK_DP_0 | |
| 55 54 53 OUT | M_C_CLK_DN<3..0> | | |
| 3 | W19 | DDR2_CLK_DN_3 | |
| 2 | Y18 | DDR2_CLK_DN_2 | |
| 1 | Y20 | DDR2_CLK_DN_1 | |
| 0 | W17 | DDR2_CLK_DN_0 | |
| 55 54 53 OUT | M_C_BG<1:0> | | |
| 1 | AD20 | DDR2_BG_1 | |
| 55 54 53 OUT | M_C_BA<1:0> | | |
| 0 | AA21 | DDR2_BG_0 | |
| 1 | U17 | DDR2_BA_1 | |
| 0 | M14 | DDR2_BA_0 | |

| | | | |
|---|---|---|---|
| | | M_C_DQS_DP<17:0> | 55 54 53 BI |
| DDR2_DQS_DP_17 | AD26 | | 17 |
| DDR2_DQS_DP_16 | AH10 | | 16 |
| DDR2_DQS_DP_15 | AH16 | | 15 |
| DDR2_DQS_DP_14 | V8 | | 14 |
| DDR2_DQS_DP_13 | M8 | | 13 |
| DDR2_DQS_DP_12 | V26 | | 12 |
| DDR2_DQS_DP_11 | AC33 | | 11 |
| DDR2_DQS_DP_10 | T34 | | 10 |
| DDR2_DQS_DP_9 | AB38 | | 9 |
| DDR2_DQS_DP_8 | AC25 | | 8 |
| DDR2_DQS_DP_7 | AJ7 | | 7 |
| DDR2_DQS_DP_6 | AH12 | | 6 |
| DDR2_DQS_DP_5 | AB10 | | 5 |
| DDR2_DQS_DP_4 | N7 | | 4 |
| DDR2_DQS_DP_3 | U25 | | 3 |
| DDR2_DQS_DP_2 | AB32 | | 2 |
| DDR2_DQS_DP_1 | U31 | | 1 |
| DDR2_DQS_DP_0 | V38 | | 0 |
| | | M_C_DQS_DN<17:0> | 55 54 53 BI |
| DDR2_DQS_DN_17 | AB26 | | 17 |
| DDR2_DQS_DN_16 | AJ9 | | 16 |
| DDR2_DQS_DN_15 | AJ15 | | 15 |
| DDR2_DQS_DN_14 | W9 | | 14 |
| DDR2_DQS_DN_13 | L7 | | 13 |
| DDR2_DQS_DN_12 | T26 | | 12 |
| DDR2_DQS_DN_11 | AA33 | | 11 |
| DDR2_DQS_DN_10 | R33 | | 10 |
| DDR2_DQS_DN_9 | AC37 | | 9 |
| DDR2_DQS_DN_8 | AE25 | | 8 |
| DDR2_DQS_DN_7 | AH8 | | 7 |
| DDR2_DQS_DN_6 | AJ13 | | 6 |
| DDR2_DQS_DN_5 | Y10 | | 5 |
| DDR2_DQS_DN_4 | P8 | | 4 |
| DDR2_DQS_DN_3 | W25 | | 3 |
| DDR2_DQS_DN_2 | AD32 | | 2 |
| DDR2_DQS_DN_1 | V32 | | 1 |
| DDR2_DQS_DN_0 | W37 | | 0 |
| | | M_C_MA<17:0> | 55 54 53 OUT |
| DDR2_MA_17 | T14 | | 17 |
| DDR2_MA_16 | P14 | | 16 |
| DDR2_MA_15 | R13 | | 15 |
| DDR2_MA_14 | Y14 | | 14 |
| DDR2_MA_13 | P12 | | 13 |
| DDR2_MA_12 | W21 | | 12 |
| DDR2_MA_11 | T20 | | 11 |
| DDR2_MA_10 | AA15 | | 10 |
| DDR2_MA_9 | P20 | | 9 |
| DDR2_MA_8 | L19 | | 8 |
| DDR2_MA_7 | U19 | | 7 |
| DDR2_MA_6 | M18 | | 6 |
| DDR2_MA_5 | P18 | | 5 |
| DDR2_MA_4 | R19 | | 4 |
| DDR2_MA_3 | L17 | | 3 |
| DDR2_MA_2 | T18 | | 2 |
| DDR2_MA_1 | M16 | | 1 |
| DDR2_MA_0 | L15 | | 0 |
| | | M_C_CKE<5..0> | 55 54 53 OUT |
| DDR2_CKE_5 | AD22 | | 5 |
| DDR2_CKE_4 | AB22 | | 4 |
| DDR2_CKE_3 | Y22 | | 3 |
| DDR2_CKE_2 | T22 | | 2 |
| DDR2_CKE_1 | U21 | | 1 |
| DDR2_CKE_0 | R21 | | 0 |
| | | M_C_ODT<5..0> | 55 54 53 OUT |
| DDR2_ODT_5 | AD14 | | 5 |
| DDR2_ODT_4 | AE17 | | 4 |
| DDR2_ODT_3 | AB14 | | 3 |
| DDR2_ODT_2 | R15 | | 2 |
| DDR2_ODT_1 | W15 | | 1 |
| DDR2_ODT_0 | Y16 | | 0 |
| | | M_C_CS_N<9:0> | 55 54 53 OUT |
| DDR2_CS9_N | T12 | | 9 |
| DDR2_CS8_N | AD18 | | 8 |
| DDR2_CS7_N_CID_4 | AD16 | | 7 |
| DDR2_CS6_N_CID_3 | AC13 | | 6 |
| DDR2_CS5_N | U15 | | 5 |
| DDR2_CS4_N | P16 | | 4 |
| DDR2_CS3_N_CID_1 | AA13 | | 3 |
| DDR2_CS2_N_CID_0 | W13 | | 2 |
| DDR2_CS1_N | T16 | | 1 |
| DDR2_CS0_N | AB16 | | 0 |
| DDR2_CID_2 | U13 | M_C_C<2> | 55 54 53 OUT |
| DDR2_ACT_N | AE21 | M_C_ACT_N | 55 54 53 OUT |
| DDR2_ALERT_N | P22 | M_C_ALERT_N | 55 54 53 IN |
| DDR2_PAR | R17 | M_C_PAR | 55 54 53 OUT |

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# CPU HASWELL SOCKET0 (5 OF 11)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,YULIN,MATT | SIZE C DATE Mon Nov 16 11:51:14 2015 | SHEET 14 OF 188 | |

SMLF
LGA2011_R3
U94
DGA^1000014
I0

HSX_EP_EXT

M_D_DQ<63:0>
BI 58 57 56

| | | |
|---|---|---|
| 63 | AB6 | DDR3_DQ_63 |
| 62 | AC3 | DDR3_DQ_62 |
| 61 | V6 | DDR3_DQ_61 |
| 60 | U5 | DDR3_DQ_60 |
| 59 | AE5 | DDR3_DQ_59 |
| 58 | AC5 | DDR3_DQ_58 |
| 57 | W3 | DDR3_DQ_57 |
| 56 | V4 | DDR3_DQ_56 |
| 55 | AL1 | DDR3_DQ_55 |
| 54 | AJ3 | DDR3_DQ_54 |
| 53 | AE3 | DDR3_DQ_53 |
| 52 | AG5 | DDR3_DQ_52 |
| 51 | AL5 | DDR3_DQ_51 |
| 50 | AL3 | DDR3_DQ_50 |
| 49 | AG1 | DDR3_DQ_49 |
| 48 | AG3 | DDR3_DQ_48 |
| 47 | G7 | DDR3_DQ_47 |
| 46 | D6 | DDR3_DQ_46 |
| 45 | A9 | DDR3_DQ_45 |
| 44 | C9 | DDR3_DQ_44 |
| 43 | F6 | DDR3_DQ_43 |
| 42 | E5 | DDR3_DQ_42 |
| 41 | F8 | DDR3_DQ_41 |
| 40 | E9 | DDR3_DQ_40 |
| 39 | R3 | DDR3_DQ_39 |
| 38 | K2 | DDR3_DQ_38 |
| 37 | N3 | DDR3_DQ_37 |
| 36 | P4 | DDR3_DQ_36 |
| 35 | L1 | DDR3_DQ_35 |
| 34 | J1 | DDR3_DQ_34 |
| 33 | H4 | DDR3_DQ_33 |
| 32 | K4 | DDR3_DQ_32 |
| 31 | B24 | DDR3_DQ_31 |
| 30 | C25 | DDR3_DQ_30 |
| 29 | E29 | DDR3_DQ_29 |
| 28 | G29 | DDR3_DQ_28 |
| 27 | E23 | DDR3_DQ_27 |
| 26 | F24 | DDR3_DQ_26 |
| 25 | E27 | DDR3_DQ_25 |
| 24 | F28 | DDR3_DQ_24 |
| 23 | N31 | DDR3_DQ_23 |
| 22 | L31 | DDR3_DQ_22 |
| 21 | L35 | DDR3_DQ_21 |
| 20 | J35 | DDR3_DQ_20 |
| 19 | M30 | DDR3_DQ_19 |
| 18 | K30 | DDR3_DQ_18 |
| 17 | M34 | DDR3_DQ_17 |
| 16 | K34 | DDR3_DQ_16 |
| 15 | E33 | DDR3_DQ_15 |
| 14 | D32 | DDR3_DQ_14 |
| 13 | E35 | DDR3_DQ_13 |
| 12 | F34 | DDR3_DQ_12 |
| 11 | E31 | DDR3_DQ_11 |
| 10 | G31 | DDR3_DQ_10 |
| 9 | B34 | DDR3_DQ_9 |
| 8 | A35 | DDR3_DQ_8 |
| 7 | K38 | DDR3_DQ_7 |
| 6 | G37 | DDR3_DQ_6 |
| 5 | J39 | DDR3_DQ_5 |
| 4 | C39 | DDR3_DQ_4 |
| 3 | M38 | DDR3_DQ_3 |
| 2 | L37 | DDR3_DQ_2 |
| 1 | B38 | DDR3_DQ_1 |
| 0 | D38 | DDR3_DQ_0 |

M_D_ECC<7..0>
BI 58 57 56

| | | |
|---|---|---|
| 7 | K24 | DDR3_ECC_7 |
| 6 | M24 | DDR3_ECC_6 |
| 5 | M28 | DDR3_ECC_5 |
| 4 | K28 | DDR3_ECC_4 |
| 3 | J23 | DDR3_ECC_3 |
| 2 | L23 | DDR3_ECC_2 |
| 1 | J27 | DDR3_ECC_1 |
| 0 | L27 | DDR3_ECC_0 |

M_D_CLK_DP<3..0>
OUT 58 57 56

| | | |
|---|---|---|
| 3 | A19 | DDR3_CLK_DP_3 |
| 2 | B18 | DDR3_CLK_DP_2 |
| 1 | B20 | DDR3_CLK_DP_1 |
| 0 | A17 | DDR3_CLK_DP_0 |

M_D_CLK_DN<3..0>
OUT 58 57 56

| | | |
|---|---|---|
| 3 | C19 | DDR3_CLK_DN_3 |
| 2 | D18 | DDR3_CLK_DN_2 |
| 1 | D20 | DDR3_CLK_DN_1 |
| 0 | C17 | DDR3_CLK_DN_0 |

M_D_BG<1:0>
OUT 58 57 56

| | | |
|---|---|---|
| 1 | G21 | DDR3_BG_1 |
| 0 | J21 | DDR3_BG_0 |

M_D_BA<1:0>
OUT 58 57 56

| | | |
|---|---|---|
| 1 | K14 | DDR3_BA_1 |
| 0 | G13 | DDR3_BA_0 |

M_D_DQS_DP<17:0>
BI 56 57 58

| | | |
|---|---|---|
| 17 | M26 | DDR3_DQS_DP_17 |
| 16 | Y6 | DDR3_DQS_DP_16 |
| 15 | AH4 | DDR3_DQS_DP_15 |
| 14 | B8 | DDR3_DQS_DP_14 |
| 13 | M4 | DDR3_DQS_DP_13 |
| 12 | F26 | DDR3_DQS_DP_12 |
| 11 | J33 | DDR3_DQS_DP_11 |
| 10 | C35 | DDR3_DQS_DP_10 |
| 9 | F38 | DDR3_DQS_DP_9 |
| 8 | L25 | DDR3_DQS_DP_8 |
| 7 | AB4 | DDR3_DQS_DP_7 |
| 6 | AK2 | DDR3_DQS_DP_6 |
| 5 | E7 | DDR3_DQS_DP_5 |
| 4 | H2 | DDR3_DQS_DP_4 |
| 3 | E25 | DDR3_DQS_DP_3 |
| 2 | M32 | DDR3_DQS_DP_2 |
| 1 | B32 | DDR3_DQS_DP_1 |
| 0 | E37 | DDR3_DQS_DP_0 |

M_D_DQS_DN<17:0>
BI 56 57 58

| | | |
|---|---|---|
| 17 | K26 | DDR3_DQS_DN_17 |
| 16 | W5 | DDR3_DQS_DN_16 |
| 15 | AJ5 | DDR3_DQS_DN_15 |
| 14 | D8 | DDR3_DQS_DN_14 |
| 13 | L3 | DDR3_DQS_DN_13 |
| 12 | D26 | DDR3_DQS_DN_12 |
| 11 | L33 | DDR3_DQS_DN_11 |
| 10 | D34 | DDR3_DQS_DN_10 |
| 9 | H38 | DDR3_DQS_DN_9 |
| 8 | N25 | DDR3_DQS_DN_8 |
| 7 | AA5 | DDR3_DQS_DN_7 |
| 6 | AJ1 | DDR3_DQS_DN_6 |
| 5 | C7 | DDR3_DQS_DN_5 |
| 4 | G3 | DDR3_DQS_DN_4 |
| 3 | G25 | DDR3_DQS_DN_3 |
| 2 | K32 | DDR3_DQS_DN_2 |
| 1 | A33 | DDR3_DQS_DN_1 |
| 0 | C37 | DDR3_DQS_DN_0 |

M_D_MA<17:0>
OUT 56 57 58

| | | |
|---|---|---|
| 17 | L11 | DDR3_MA_17 |
| 16 | J13 | DDR3_MA_16 |
| 15 | F12 | DDR3_MA_15 |
| 14 | K12 | DDR3_MA_14 |
| 13 | M12 | DDR3_MA_13 |
| 12 | M20 | DDR3_MA_12 |
| 11 | K20 | DDR3_MA_11 |
| 10 | L13 | DDR3_MA_10 |
| 9 | F20 | DDR3_MA_9 |
| 8 | G19 | DDR3_MA_8 |
| 7 | J19 | DDR3_MA_7 |
| 6 | F18 | DDR3_MA_6 |
| 5 | K18 | DDR3_MA_5 |
| 4 | J17 | DDR3_MA_4 |
| 3 | G17 | DDR3_MA_3 |
| 2 | F16 | DDR3_MA_2 |
| 1 | K16 | DDR3_MA_1 |
| 0 | G15 | DDR3_MA_0 |

M_D_CKE<5..0>
OUT 56 57 58

| | | |
|---|---|---|
| 5 | K22 | DDR3_CKE_5 |
| 4 | B22 | DDR3_CKE_4 |
| 3 | D22 | DDR3_CKE_3 |
| 2 | A21 | DDR3_CKE_2 |
| 1 | E21 | DDR3_CKE_1 |
| 0 | F22 | DDR3_CKE_0 |

M_D_ODT<5..0>
OUT 56 57 58

| | | |
|---|---|---|
| 5 | E11 | DDR3_ODT_5 |
| 4 | E13 | DDR3_ODT_4 |
| 3 | D12 | DDR3_ODT_3 |
| 2 | D14 | DDR3_ODT_2 |
| 1 | A13 | DDR3_ODT_1 |
| 0 | D16 | DDR3_ODT_0 |

M_D_CS_N<9:0>
OUT 56 57 58

| | | |
|---|---|---|
| 9 | B12 | DDR3_CS9_N |
| 8 | B14 | DDR3_CS8_N |
| 7 | A11 | DDR3_CS7_N_CID_4 |
| 6 | G11 | DDR3_CS6_N_CID_3 |
| 5 | F14 | DDR3_CS5_N |
| 4 | A15 | DDR3_CS4_N |
| 3 | H10 | DDR3_CS3_N_CID_1 |
| 2 | F10 | DDR3_CS2_N_CID_0 |
| 1 | C15 | DDR3_CS1_N |
| 0 | B16 | DDR3_CS0_N |

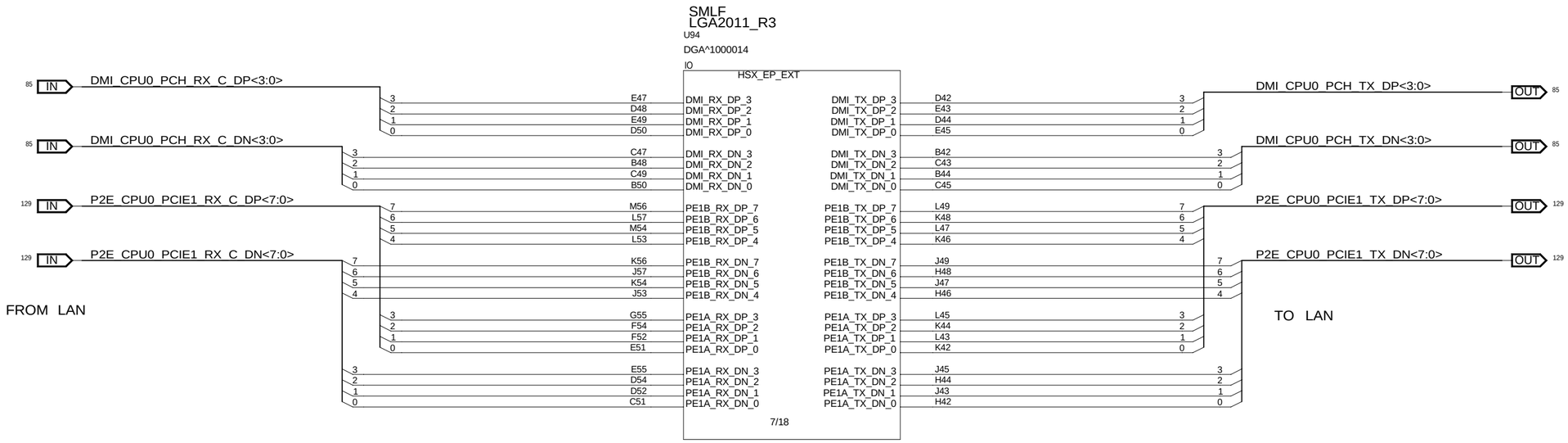
| | | | |
|---|---|---|---|
| DDR3_CID_2 | J11 | M_D_C<2> | OUT 56 57 58 |
| DDR3_ACT_N | L21 | M_D_ACT_N | OUT 56 57 58 |
| DDR3_ALERT_N | M22 | M_D_ALERT_N | IN 56 57 58 |
| DDR3_PAR | J15 | M_D_PAR | OUT 56 57 58 |

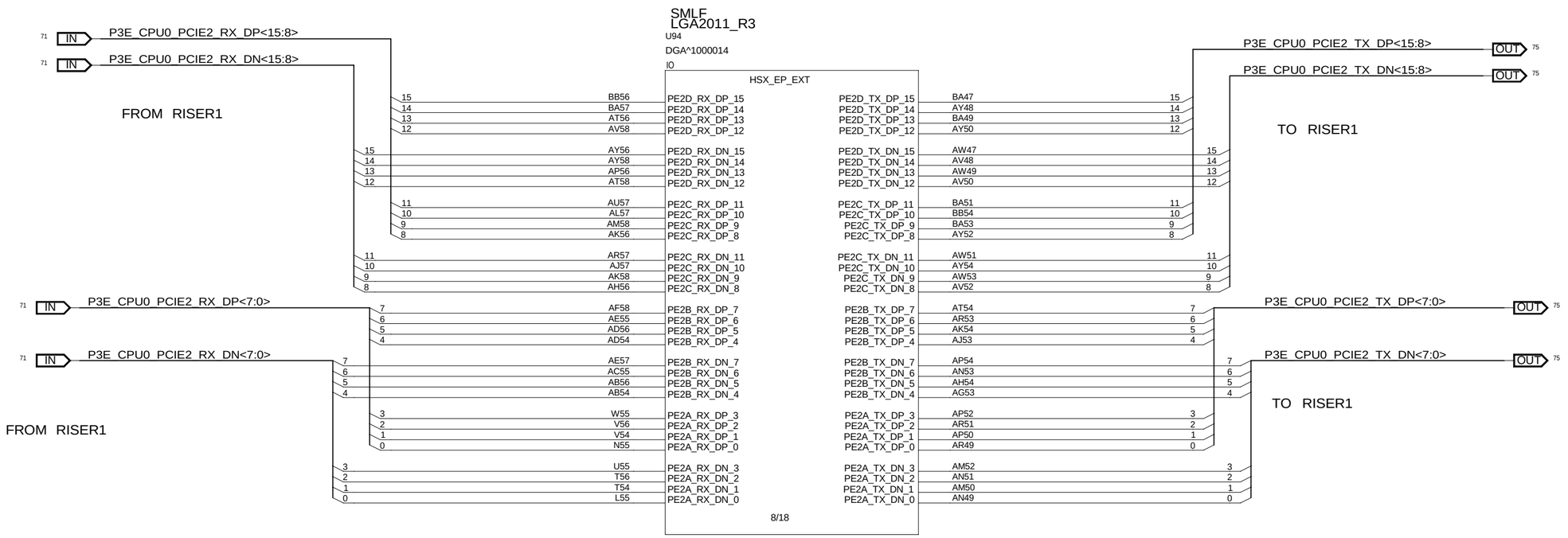
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# CPU HASWELL SOCKET0 (6 OF 11)

Quanta

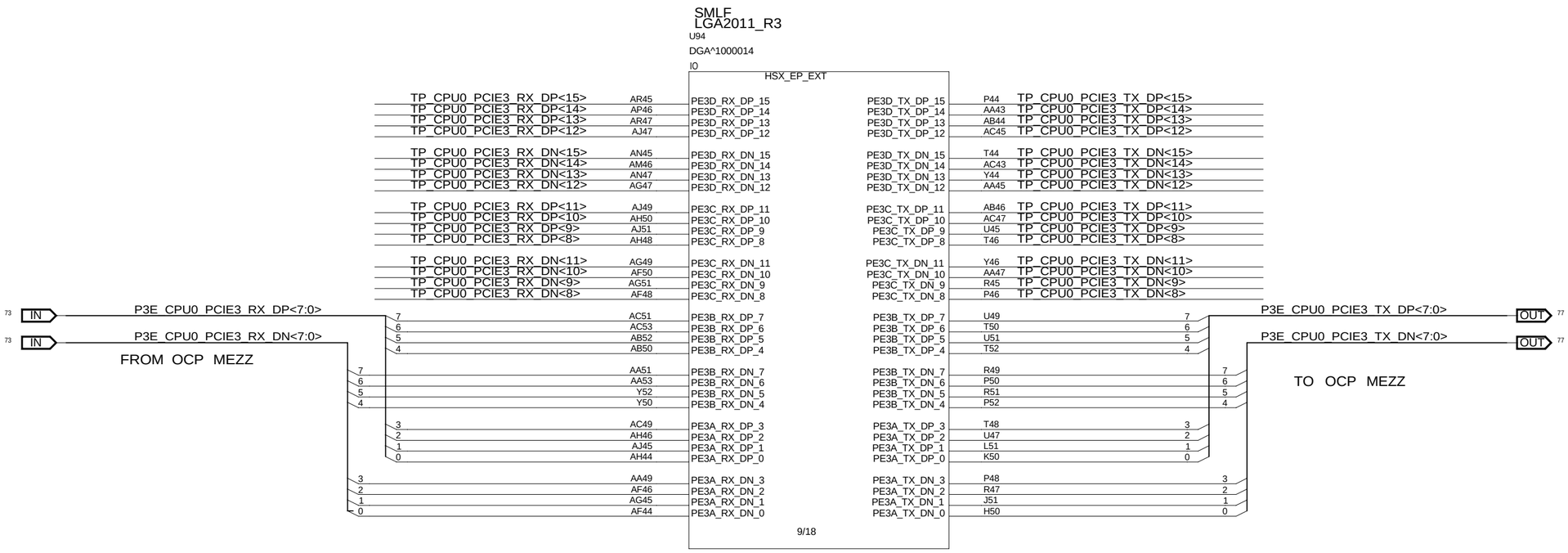
| | | | | | |
|---|---|---|---|---|---|
| DEPARTMENT | CCBU | DESIGNER | NICK | PROJCET | S2B |
| | | REVIEWER | PETER,YULIN,MATT | DOCUMENT NUMBER | DA0S2BMB8A0 |
| | | | | REV | 1 |
| | | | | SIZE C | DATE Mon Nov 16 11:51:16 2015 |
| | | | | SHEET | 15 OF 188 |



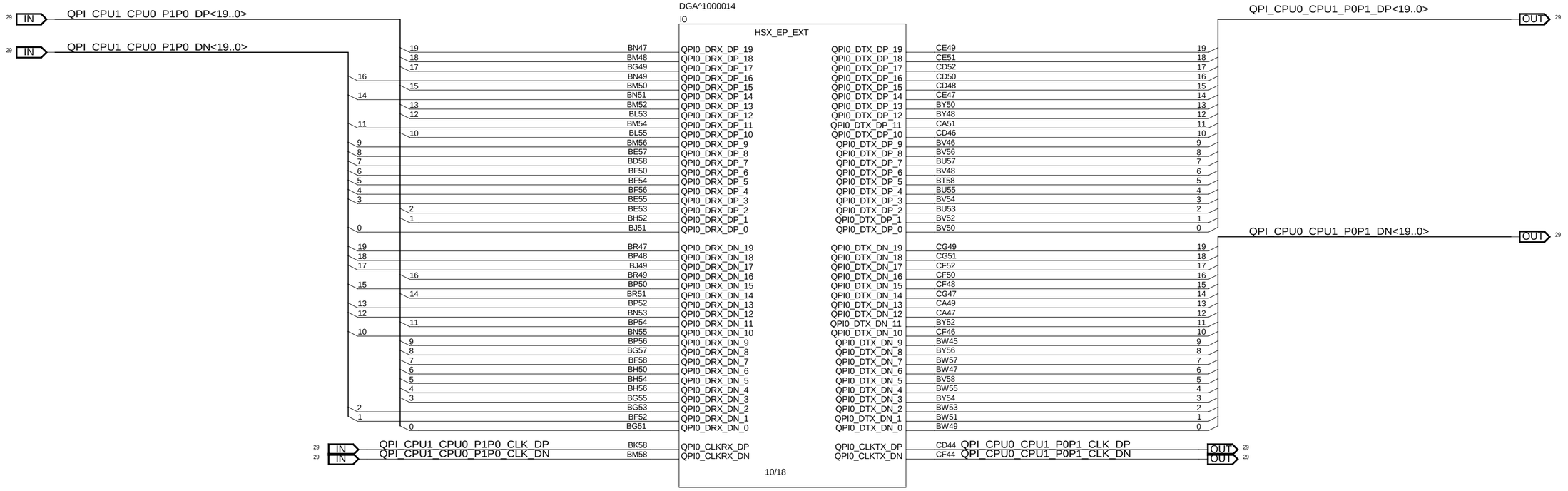

# CPU HASWELL SOCKET0 (7 OF 11)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:51:19 2015 | SHEET: 16 OF 188 |



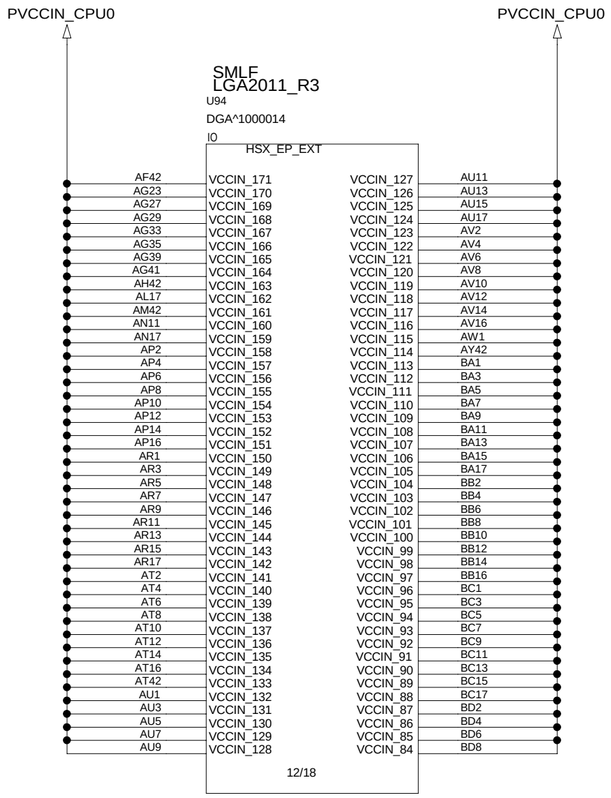

# CPU HASWELL SOCKET0 (8 OF 11)

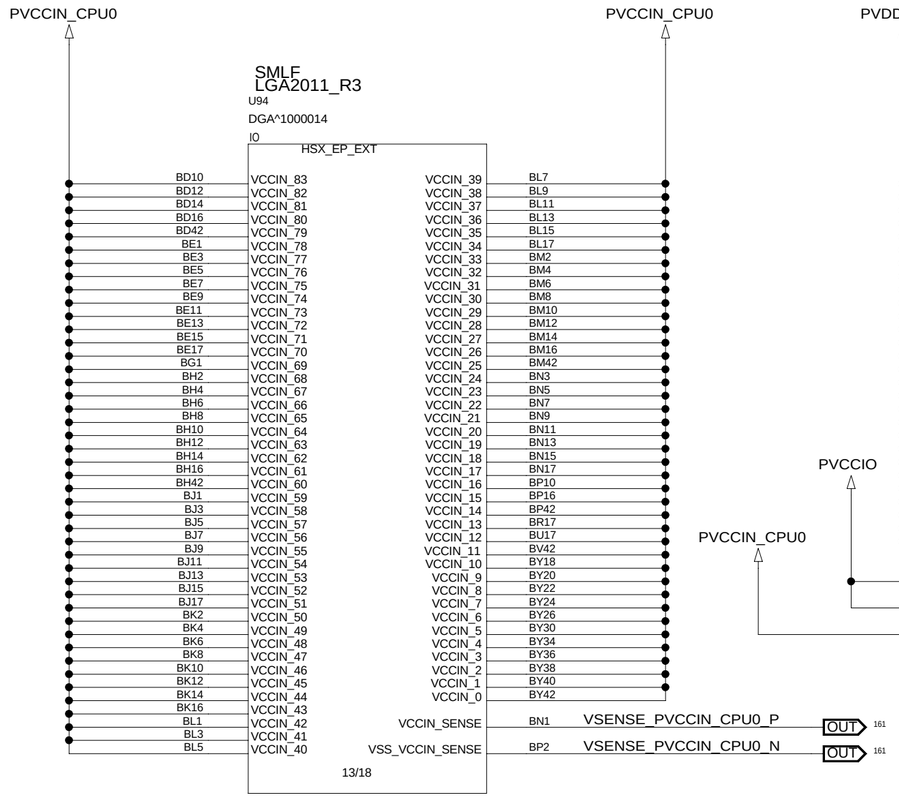
| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:51:20 2015 | SHEET: 17 OF 188 | |

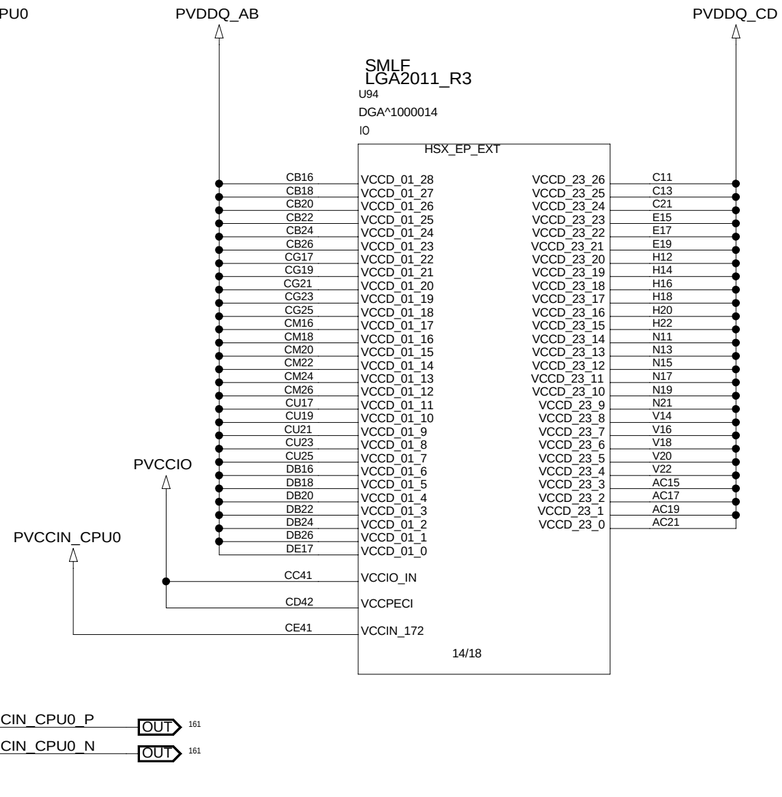



# CPU HASWELL SOCKET0 (9 OF 11)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:51:22 2015 | SHEET: 18 OF 188 |

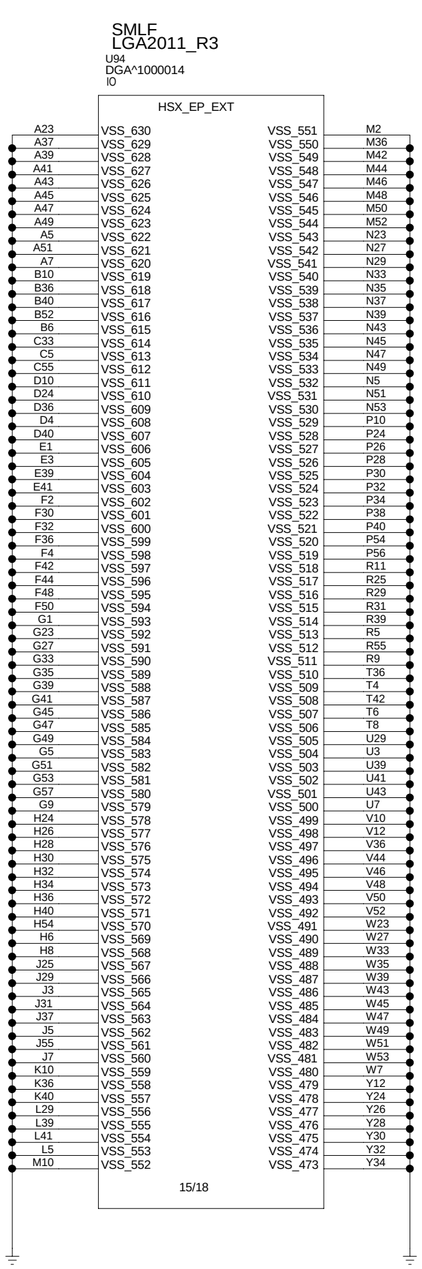


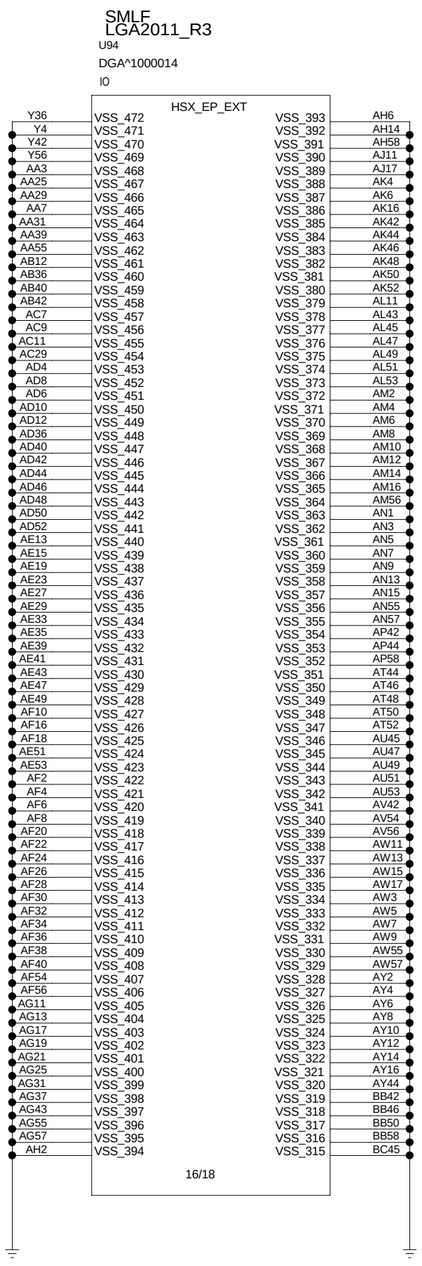



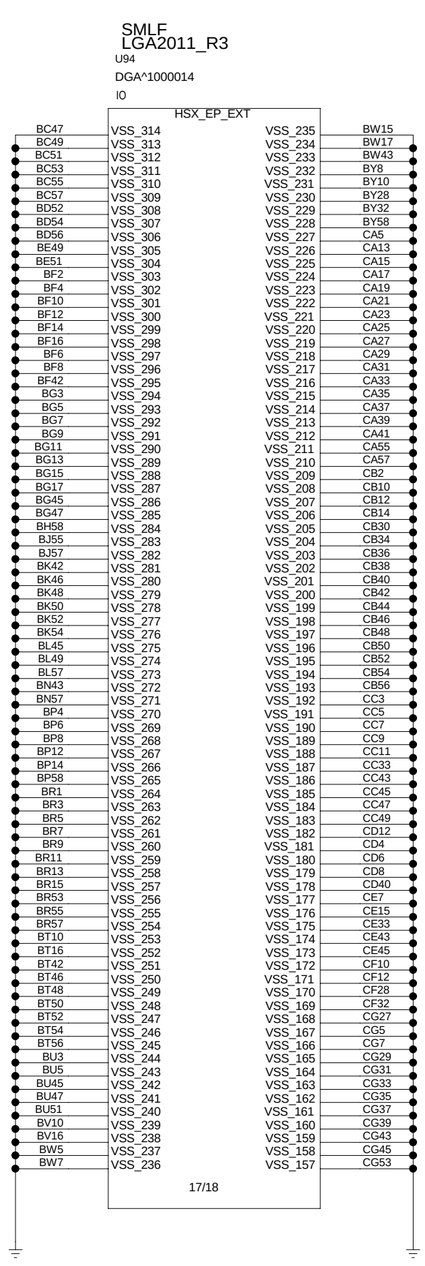



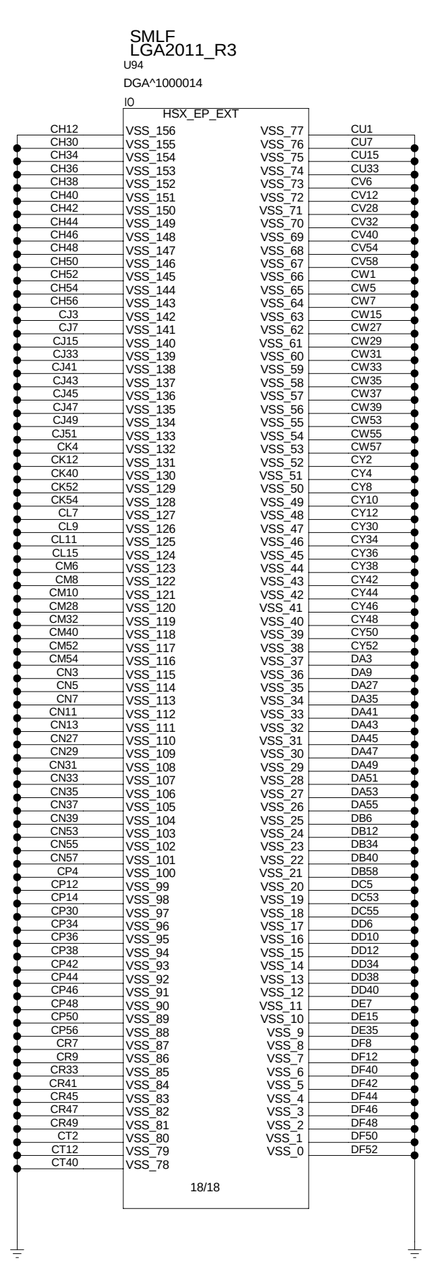

# CPU HASWELL SOCKET0 (10 OF 11)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C DATE: Mon Nov 16 11:51:25 2015 | SHEET: 19 OF 188 | |



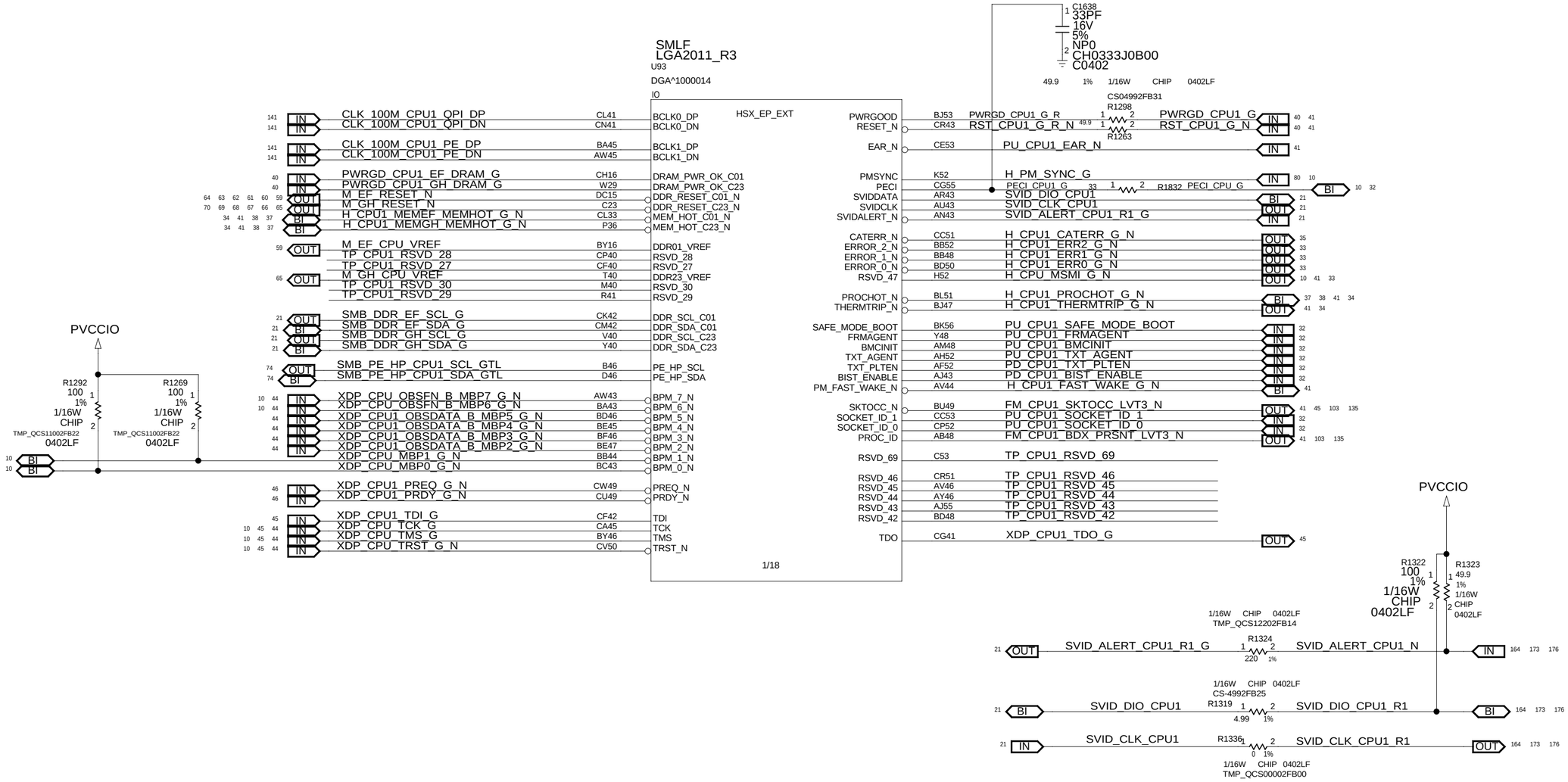



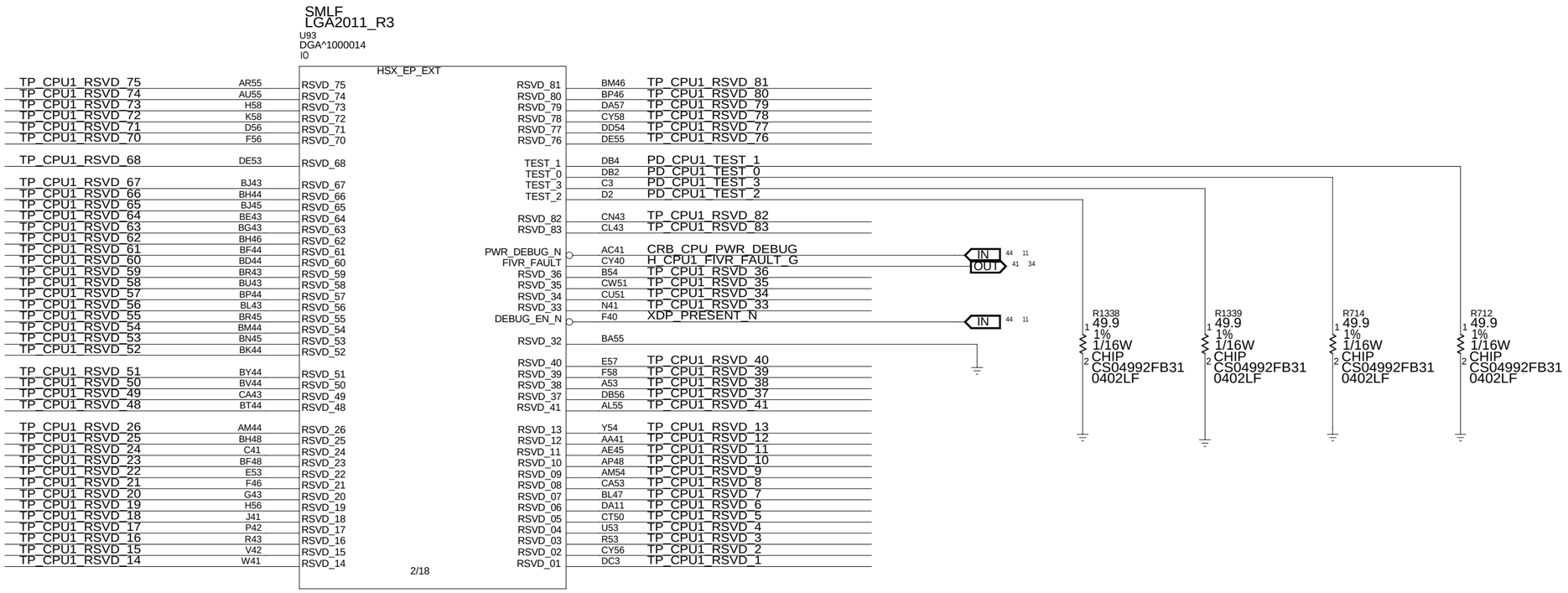

# CPU HASWELL SOCKET0 (11 OF 11)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:51:30 2015 | SHEET: 20 OF 188 |




# CPU HASWELL SOCKET1 (1 OF 11)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C DATE: Mon Nov 16 11:51:31 2015 | SHEET: 21 OF 188 | |




# CPU HASWELL SOCKET1 (2 OF 11)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C DATE: Mon Nov 16 11:51:32 2015 | SHEET: 22 OF 188 | |

SMLF
LGA2011_R3
I0
DGA^1000014
U93

HSX_EP_EXT

M_E_DQ<63:0> (BI)

| | | | |
|---|---|---|---|
| 63 | CK38 | DDR0_DQ_63 | |
| 62 | CM38 | DDR0_DQ_62 | |
| 61 | CK34 | DDR0_DQ_61 | |
| 60 | CM34 | DDR0_DQ_60 | |
| 59 | CJ39 | DDR0_DQ_59 | |
| 58 | CL39 | DDR0_DQ_58 | |
| 57 | CJ35 | DDR0_DQ_57 | |
| 56 | CL35 | DDR0_DQ_56 | |
| 55 | CD38 | DDR0_DQ_55 | |
| 54 | CF38 | DDR0_DQ_54 | |
| 53 | CD34 | DDR0_DQ_53 | |
| 52 | CF34 | DDR0_DQ_52 | |
| 51 | CC39 | DDR0_DQ_51 | |
| 50 | CE39 | DDR0_DQ_50 | |
| 49 | CC35 | DDR0_DQ_49 | |
| 48 | CE35 | DDR0_DQ_48 | |
| 47 | CC31 | DDR0_DQ_47 | |
| 46 | CE31 | DDR0_DQ_46 | |
| 45 | CC27 | DDR0_DQ_45 | |
| 44 | CE27 | DDR0_DQ_44 | |
| 43 | CB32 | DDR0_DQ_43 | |
| 42 | CD32 | DDR0_DQ_42 | |
| 41 | CB28 | DDR0_DQ_41 | |
| 40 | CD28 | DDR0_DQ_40 | |
| 39 | CJ31 | DDR0_DQ_39 | |
| 38 | CL31 | DDR0_DQ_38 | |
| 37 | CJ27 | DDR0_DQ_37 | |
| 36 | CL27 | DDR0_DQ_36 | |
| 35 | CH32 | DDR0_DQ_35 | |
| 34 | CK32 | DDR0_DQ_34 | |
| 33 | CH28 | DDR0_DQ_33 | |
| 32 | CK28 | DDR0_DQ_32 | |
| 31 | CL13 | DDR0_DQ_31 | |
| 30 | CM12 | DDR0_DQ_30 | |
| 29 | CD14 | DDR0_DQ_29 | |
| 28 | CC13 | DDR0_DQ_28 | |
| 27 | CH14 | DDR0_DQ_27 | |
| 26 | CM14 | DDR0_DQ_26 | |
| 25 | CG15 | DDR0_DQ_25 | |
| 24 | CE13 | DDR0_DQ_24 | |
| 23 | CJ9 | DDR0_DQ_23 | |
| 22 | CK8 | DDR0_DQ_22 | |
| 21 | CE11 | DDR0_DQ_21 | |
| 20 | CD10 | DDR0_DQ_20 | |
| 19 | CJ11 | DDR0_DQ_19 | |
| 18 | CK10 | DDR0_DQ_18 | |
| 17 | CF8 | DDR0_DQ_17 | |
| 16 | CE9 | DDR0_DQ_16 | |
| 15 | BY12 | DDR0_DQ_15 | |
| 14 | CA11 | DDR0_DQ_14 | |
| 13 | BU15 | DDR0_DQ_13 | |
| 12 | BT14 | DDR0_DQ_12 | |
| 11 | BY14 | DDR0_DQ_11 | |
| 10 | BW13 | DDR0_DQ_10 | |
| 9 | BU11 | DDR0_DQ_9 | |
| 8 | BT12 | DDR0_DQ_8 | |
| 7 | CB6 | DDR0_DQ_7 | |
| 6 | CA7 | DDR0_DQ_6 | |
| 5 | BU9 | DDR0_DQ_5 | |
| 4 | BT8 | DDR0_DQ_4 | |
| 3 | CB8 | DDR0_DQ_3 | |
| 2 | CA9 | DDR0_DQ_2 | |
| 1 | BT6 | DDR0_DQ_1 | |
| 0 | BU7 | DDR0_DQ_0 | |

M_E_ECC<7..0> (BI)

| | | |
|---|---|---|
| 7 | CR11 | DDR0_ECC_7 |
| 6 | CP10 | DDR0_ECC_6 |
| 5 | CN9 | DDR0_ECC_5 |
| 4 | CP8 | DDR0_ECC_4 |
| 3 | CU11 | DDR0_ECC_3 |
| 2 | CW11 | DDR0_ECC_2 |
| 1 | CV8 | DDR0_ECC_1 |
| 0 | CT8 | DDR0_ECC_0 |

M_E_CLK_DP<3..0> (OUT)

| | | |
|---|---|---|
| 3 | CC19 | DDR0_CLK_DP_3 |
| 2 | CD20 | DDR0_CLK_DP_2 |
| 1 | CD18 | DDR0_CLK_DP_1 |
| 0 | CC21 | DDR0_CLK_DP_0 |

M_E_CLK_DN<3..0> (OUT)

| | | |
|---|---|---|
| 3 | CE19 | DDR0_CLK_DN_3 |
| 2 | CF20 | DDR0_CLK_DN_2 |
| 1 | CF18 | DDR0_CLK_DN_1 |
| 0 | CE21 | DDR0_CLK_DN_0 |

M_E_BG<1:0> (OUT)

| | | |
|---|---|---|
| 1 | CN17 | DDR0_BG_1 |
| 0 | CL17 | DDR0_BG_0 |

M_E_BA<1:0> (OUT)

| | | |
|---|---|---|
| 1 | CH20 | DDR0_BA_1 |
| 0 | CL21 | DDR0_BA_0 |

M_E_DQS_DP<17:0> (BI)

| | | |
|---|---|---|
| DDR0_DQS_DP_17 | CU9 | 17 |
| DDR0_DQS_DP_16 | CM36 | 16 |
| DDR0_DQS_DP_15 | CF36 | 15 |
| DDR0_DQS_DP_14 | CE29 | 14 |
| DDR0_DQS_DP_13 | CL29 | 13 |
| DDR0_DQS_DP_12 | CG13 | 12 |
| DDR0_DQS_DP_11 | CG9 | 11 |
| DDR0_DQS_DP_10 | BU13 | 10 |
| DDR0_DQS_DP_9 | BV8 | 9 |
| DDR0_DQS_DP_8 | CV10 | 8 |
| DDR0_DQS_DP_7 | CJ37 | 7 |
| DDR0_DQS_DP_6 | CC37 | 6 |
| DDR0_DQS_DP_5 | CD30 | 5 |
| DDR0_DQS_DP_4 | CK30 | 4 |
| DDR0_DQS_DP_3 | CK14 | 3 |
| DDR0_DQS_DP_2 | CH10 | 2 |
| DDR0_DQS_DP_1 | BV12 | 1 |
| DDR0_DQS_DP_0 | BY6 | 0 |

M_E_DQS_DN<17:0> (BI)

| | | |
|---|---|---|
| DDR0_DQS_DN_17 | CW9 | 17 |
| DDR0_DQS_DN_16 | CK36 | 16 |
| DDR0_DQS_DN_15 | CD36 | 15 |
| DDR0_DQS_DN_14 | CC29 | 14 |
| DDR0_DQS_DN_13 | CJ29 | 13 |
| DDR0_DQS_DN_12 | CF14 | 12 |
| DDR0_DQS_DN_11 | CH8 | 11 |
| DDR0_DQS_DN_10 | BV14 | 10 |
| DDR0_DQS_DN_9 | BW9 | 9 |
| DDR0_DQS_DN_8 | CT10 | 8 |
| DDR0_DQS_DN_7 | CL37 | 7 |
| DDR0_DQS_DN_6 | CE37 | 6 |
| DDR0_DQS_DN_5 | CF30 | 5 |
| DDR0_DQS_DN_4 | CM30 | 4 |
| DDR0_DQS_DN_3 | CJ13 | 3 |
| DDR0_DQS_DN_2 | CG11 | 2 |
| DDR0_DQS_DN_1 | BW11 | 1 |
| DDR0_DQS_DN_0 | BV6 | 0 |

M_E_MA<17:0> (OUT)

| | | |
|---|---|---|
| DDR0_MA_17 | CD24 | 17 |
| DDR0_MA_16 | CL23 | 16 |
| DDR0_MA_15 | CL25 | 15 |
| DDR0_MA_14 | CJ21 | 14 |
| DDR0_MA_13 | CE23 | 13 |
| DDR0_MA_12 | CR17 | 12 |
| DDR0_MA_11 | CP18 | 11 |
| DDR0_MA_10 | CP24 | 10 |
| DDR0_MA_9 | CK18 | 9 |
| DDR0_MA_8 | CJ19 | 8 |
| DDR0_MA_7 | CH18 | 7 |
| DDR0_MA_6 | CN19 | 6 |
| DDR0_MA_5 | CL19 | 5 |
| DDR0_MA_4 | CP20 | 4 |
| DDR0_MA_3 | CN21 | 3 |
| DDR0_MA_2 | CT22 | 2 |
| DDR0_MA_1 | CR21 | 1 |
| DDR0_MA_0 | CP22 | 0 |

M_E_CKE<5..0> (OUT)

| | | |
|---|---|---|
| DDR0_CKE_5 | CC15 | 5 |
| DDR0_CKE_4 | CN15 | 4 |
| DDR0_CKE_3 | CC17 | 3 |
| DDR0_CKE_2 | CF16 | 2 |
| DDR0_CKE_1 | CE17 | 1 |
| DDR0_CKE_0 | CJ17 | 0 |

M_E_ODT<5..0> (OUT)

| | | |
|---|---|---|
| DDR0_ODT_5 | CE25 | 5 |
| DDR0_ODT_4 | CF24 | 4 |
| DDR0_ODT_3 | CC23 | 3 |
| DDR0_ODT_2 | CJ23 | 2 |
| DDR0_ODT_1 | CN25 | 1 |
| DDR0_ODT_0 | CF22 | 0 |

M_E_CS_N<9:0> (OUT)

| | | |
|---|---|---|
| DDR0_CS9_N | CK26 | 9 |
| DDR0_CS8_N | CK24 | 8 |
| DDR0_CS7_N_CID_4 | CD26 | 7 |
| DDR0_CS6_N_CID_3 | CH26 | 6 |
| DDR0_CS5_N | CH24 | 5 |
| DDR0_CS4_N | CK22 | 4 |
| DDR0_CS3_N_CID_1 | CC25 | 3 |
| DDR0_CS2_N_CID_0 | CF26 | 2 |
| DDR0_CS1_N | CH22 | 1 |
| DDR0_CS0_N | CD22 | 0 |

| | | |
|---|---|---|
| DDR0_CID_2 | CJ25 | M_E_C<2> (OUT) |
| DDR0_ACT_N | CK16 | M_E_ACT_N (OUT) |
| DDR0_ALERT_N | CD16 | M_E_ALERT_N (IN) |
| DDR0_PAR | CK20 | M_E_PAR (OUT) |

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# CPU HASWELL SOCKET1 (3 OF 11)

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|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C DATE: Mon Nov 16 11:51:37 2015 | SHEET: 23 OF 188 | |

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## HSX_EP_EXT

| | | | | | |
|---|---|---|---|---|---|
| 64 63 62 BI | M_F_DQ<63:0> | 63 | DE39 | DDR1_DQ_63 | |
| | | 62 | DF38 | DDR1_DQ_62 | |
| | | 61 | DB36 | DDR1_DQ_61 | |
| | | 60 | DC35 | DDR1_DQ_60 | |
| | | 59 | DA39 | DDR1_DQ_59 | |
| | | 58 | DC39 | DDR1_DQ_58 | |
| | | 57 | DF36 | DDR1_DQ_57 | |
| | | 56 | DC37 | DDR1_DQ_56 | |
| | | 55 | CT38 | DDR1_DQ_55 | |
| | | 54 | CV38 | DDR1_DQ_54 | |
| | | 53 | CT34 | DDR1_DQ_53 | |
| | | 52 | CV34 | DDR1_DQ_52 | |
| | | 51 | CR39 | DDR1_DQ_51 | |
| | | 50 | CU39 | DDR1_DQ_50 | |
| | | 49 | CR35 | DDR1_DQ_49 | |
| | | 48 | CU35 | DDR1_DQ_48 | |
| | | 47 | DE33 | DDR1_DQ_47 | |
| | | 46 | DA33 | DDR1_DQ_46 | |
| | | 45 | CY28 | DDR1_DQ_45 | |
| | | 44 | DB28 | DDR1_DQ_44 | |
| | | 43 | DF34 | DDR1_DQ_43 | |
| | | 42 | DC33 | DDR1_DQ_42 | |
| | | 41 | DB30 | DDR1_DQ_41 | |
| | | 40 | DA29 | DDR1_DQ_40 | |
| | | 39 | CR31 | DDR1_DQ_39 | |
| | | 38 | CU31 | DDR1_DQ_38 | |
| | | 37 | CR27 | DDR1_DQ_37 | |
| | | 36 | CU27 | DDR1_DQ_36 | |
| | | 35 | CP32 | DDR1_DQ_35 | |
| | | 34 | CT32 | DDR1_DQ_34 | |
| | | 33 | CP28 | DDR1_DQ_33 | |
| | | 32 | CT28 | DDR1_DQ_32 | |
| | | 31 | DF10 | DDR1_DQ_31 | |
| | | 30 | DE9 | DDR1_DQ_30 | |
| | | 29 | CY6 | DDR1_DQ_29 | |
| | | 28 | DA5 | DDR1_DQ_28 | |
| | | 27 | DC11 | DDR1_DQ_27 | |
| | | 26 | DE11 | DDR1_DQ_26 | |
| | | 25 | DB8 | DDR1_DQ_25 | |
| | | 24 | DA7 | DDR1_DQ_24 | |
| | | 23 | CR5 | DDR1_DQ_23 | |
| | | 22 | CU5 | DDR1_DQ_22 | |
| | | 21 | CP2 | DDR1_DQ_21 | |
| | | 20 | CR1 | DDR1_DQ_20 | |
| | | 19 | CP6 | DDR1_DQ_19 | |
| | | 18 | CT6 | DDR1_DQ_18 | |
| | | 17 | CV2 | DDR1_DQ_17 | |
| | | 16 | CR3 | DDR1_DQ_16 | |
| | | 15 | CL3 | DDR1_DQ_15 | |
| | | 14 | CK6 | DDR1_DQ_14 | |
| | | 13 | CF6 | DDR1_DQ_13 | |
| | | 12 | CE5 | DDR1_DQ_12 | |
| | | 11 | CM4 | DDR1_DQ_11 | |
| | | 10 | CL5 | DDR1_DQ_10 | |
| | | 9 | CF4 | DDR1_DQ_9 | |
| | | 8 | CE3 | DDR1_DQ_8 | |
| | | 7 | BY2 | DDR1_DQ_7 | |
| | | 6 | CA1 | DDR1_DQ_6 | |
| | | 5 | BT2 | DDR1_DQ_5 | |
| | | 4 | BT4 | DDR1_DQ_4 | |
| | | 3 | CB4 | DDR1_DQ_3 | |
| | | 2 | CA3 | DDR1_DQ_2 | |
| | | 1 | BU1 | DDR1_DQ_1 | |
| | | 0 | BV4 | DDR1_DQ_0 | |
| 64 63 62 BI | M_F_ECC<7..0> | 7 | DE13 | DDR1_ECC_7 | |
| | | 6 | DC13 | DDR1_ECC_6 | |
| | | 5 | CT14 | DDR1_ECC_5 | |
| | | 4 | CR13 | DDR1_ECC_4 | |
| | | 3 | DF14 | DDR1_ECC_3 | |
| | | 2 | DD14 | DDR1_ECC_2 | |
| | | 1 | CV14 | DDR1_ECC_1 | |
| | | 0 | CU13 | DDR1_ECC_0 | |
| 64 63 62 OUT | M_F_CLK_DP<3..0> | 3 | DE19 | DDR1_CLK_DP_3 | |
| | | 2 | DF20 | DDR1_CLK_DP_2 | |
| | | 1 | DF18 | DDR1_CLK_DP_1 | |
| | | 0 | DE21 | DDR1_CLK_DP_0 | |
| 64 63 62 OUT | M_F_CLK_DN<3..0> | 3 | DC19 | DDR1_CLK_DN_3 | |
| | | 2 | DD20 | DDR1_CLK_DN_2 | |
| | | 1 | DD18 | DDR1_CLK_DN_1 | |
| | | 0 | DC21 | DDR1_CLK_DN_0 | |
| 64 63 62 OUT | M_F_BG<1:0> | 1 | CP16 | DDR1_BG_1 | |
| | | 0 | CV16 | DDR1_BG_0 | |
| 64 63 62 OUT | M_F_BA<1:0> | 1 | CV22 | DDR1_BA_1 | |
| | | 0 | CW23 | DDR1_BA_0 | |

| | | | | | |
|---|---|---|---|---|---|
| | | | | DDR1_DQS_DP_17 | CW13 |
| | | | | DDR1_DQS_DP_16 | DD36 |
| | | | | DDR1_DQS_DP_15 | CV36 |
| | | | | DDR1_DQS_DP_14 | DA31 |
| | | | | DDR1_DQS_DP_13 | CU29 |
| | | | | DDR1_DQS_DP_12 | DC7 |
| | | | | DDR1_DQS_DP_11 | CW3 |
| | | | | DDR1_DQS_DP_10 | CH4 |
| | | | | DDR1_DQS_DP_9 | BV2 |
| | | | | DDR1_DQS_DP_8 | DB14 |
| | | | | DDR1_DQS_DP_7 | DB38 |
| | | | | DDR1_DQS_DP_6 | CR37 |
| | | | | DDR1_DQS_DP_5 | DD32 |
| | | | | DDR1_DQS_DP_4 | CT30 |
| | | | | DDR1_DQS_DP_3 | DB10 |
| | | | | DDR1_DQS_DP_2 | CT4 |
| | | | | DDR1_DQS_DP_1 | CJ5 |
| | | | | DDR1_DQS_DP_0 | BY4 |
| | | | | DDR1_DQS_DN_17 | CY14 |
| | | | | DDR1_DQS_DN_16 | DE37 |
| | | | | DDR1_DQS_DN_15 | CT36 |
| | | | | DDR1_DQS_DN_14 | CY32 |
| | | | | DDR1_DQS_DN_13 | CR29 |
| | | | | DDR1_DQS_DN_12 | DD8 |
| | | | | DDR1_DQS_DN_11 | CU3 |
| | | | | DDR1_DQS_DN_10 | CG3 |
| | | | | DDR1_DQS_DN_9 | BW1 |
| | | | | DDR1_DQS_DN_8 | DA13 |
| | | | | DDR1_DQS_DN_7 | DA37 |
| | | | | DDR1_DQS_DN_6 | CU37 |
| | | | | DDR1_DQS_DN_5 | DB32 |
| | | | | DDR1_DQS_DN_4 | CV30 |
| | | | | DDR1_DQS_DN_3 | DC9 |
| | | | | DDR1_DQS_DN_2 | CV4 |
| | | | | DDR1_DQS_DN_1 | CH6 |
| | | | | DDR1_DQS_DN_0 | BW3 |
| | | | | DDR1_MA_17 | CT24 |
| | | | | DDR1_MA_16 | CY24 |
| | | | | DDR1_MA_15 | CV24 |
| | | | | DDR1_MA_14 | CN23 |
| | | | | DDR1_MA_13 | CW25 |
| | | | | DDR1_MA_12 | CW17 |
| | | | | DDR1_MA_11 | CV18 |
| | | | | DDR1_MA_10 | CR23 |
| | | | | DDR1_MA_9 | CY18 |
| | | | | DDR1_MA_8 | DA19 |
| | | | | DDR1_MA_7 | CT18 |
| | | | | DDR1_MA_6 | CW19 |
| | | | | DDR1_MA_5 | CY20 |
| | | | | DDR1_MA_4 | CR19 |
| | | | | DDR1_MA_3 | CW21 |
| | | | | DDR1_MA_2 | CV20 |
| | | | | DDR1_MA_1 | DA21 |
| | | | | DDR1_MA_0 | CY22 |
| | | | | DDR1_CKE_5 | DA15 |
| | | | | DDR1_CKE_4 | CY16 |
| | | | | DDR1_CKE_3 | DF16 |
| | | | | DDR1_CKE_2 | DD16 |
| | | | | DDR1_CKE_1 | DC17 |
| | | | | DDR1_CKE_0 | DA17 |
| | | | | DDR1_ODT_5 | DD26 |
| | | | | DDR1_ODT_4 | DA25 |
| | | | | DDR1_ODT_3 | DC25 |
| | | | | DDR1_ODT_2 | DC23 |
| | | | | DDR1_ODT_1 | DE25 |
| | | | | DDR1_ODT_0 | DD22 |
| | | | | DDR1_CS9_N | DF26 |
| | | | | DDR1_CS8_N | DF24 |
| | | | | DDR1_CS7_N_CID_4 | CV26 |
| | | | | DDR1_CS6_N_CID_3 | CY26 |
| | | | | DDR1_CS5_N | DD24 |
| | | | | DDR1_CS4_N | DA23 |
| | | | | DDR1_CS3_N_CID_1 | CP26 |
| | | | | DDR1_CS2_N_CID_0 | CT26 |
| | | | | DDR1_CS1_N | DE23 |
| | | | | DDR1_CS0_N | DF22 |
| | | | | DDR1_CID_2 | CR25 |
| | | | | DDR1_ACT_N | CT16 |
| | | | | DDR1_ALERT_N | CR15 |
| | | | | DDR1_PAR | CT20 |

| | | | |
|---|---|---|---|
| M_F_DQS_DP<17:0> | 17 | CW13 | DDR1_DQS_DP_17 |
| | 16 | DD36 | DDR1_DQS_DP_16 |
| | 15 | CV36 | DDR1_DQS_DP_15 |
| | 14 | DA31 | DDR1_DQS_DP_14 |
| | 13 | CU29 | DDR1_DQS_DP_13 |
| | 12 | DC7 | DDR1_DQS_DP_12 |
| | 11 | CW3 | DDR1_DQS_DP_11 |
| | 10 | CH4 | DDR1_DQS_DP_10 |
| | 9 | BV2 | DDR1_DQS_DP_9 |
| | 8 | DB14 | DDR1_DQS_DP_8 |
| | 7 | DB38 | DDR1_DQS_DP_7 |
| | 6 | CR37 | DDR1_DQS_DP_6 |
| | 5 | DD32 | DDR1_DQS_DP_5 |
| | 4 | CT30 | DDR1_DQS_DP_4 |
| | 3 | DB10 | DDR1_DQS_DP_3 |
| | 2 | CT4 | DDR1_DQS_DP_2 |
| | 1 | CJ5 | DDR1_DQS_DP_1 |
| | 0 | BY4 | DDR1_DQS_DP_0 |
| M_F_DQS_DN<17:0> | 17 | CY14 | DDR1_DQS_DN_17 |
| | 16 | DE37 | DDR1_DQS_DN_16 |
| | 15 | CT36 | DDR1_DQS_DN_15 |
| | 14 | CY32 | DDR1_DQS_DN_14 |
| | 13 | CR29 | DDR1_DQS_DN_13 |
| | 12 | DD8 | DDR1_DQS_DN_12 |
| | 11 | CU3 | DDR1_DQS_DN_11 |
| | 10 | CG3 | DDR1_DQS_DN_10 |
| | 9 | BW1 | DDR1_DQS_DN_9 |
| | 8 | DA13 | DDR1_DQS_DN_8 |
| | 7 | DA37 | DDR1_DQS_DN_7 |
| | 6 | CU37 | DDR1_DQS_DN_6 |
| | 5 | DB32 | DDR1_DQS_DN_5 |
| | 4 | CV30 | DDR1_DQS_DN_4 |
| | 3 | DC9 | DDR1_DQS_DN_3 |
| | 2 | CV4 | DDR1_DQS_DN_2 |
| | 1 | CH6 | DDR1_DQS_DN_1 |
| | 0 | BW3 | DDR1_DQS_DN_0 |
| M_F_MA<17:0> | 17 | CT24 | DDR1_MA_17 |
| | 16 | CY24 | DDR1_MA_16 |
| | 15 | CV24 | DDR1_MA_15 |
| | 14 | CN23 | DDR1_MA_14 |
| | 13 | CW25 | DDR1_MA_13 |
| | 12 | CW17 | DDR1_MA_12 |
| | 11 | CV18 | DDR1_MA_11 |
| | 10 | CR23 | DDR1_MA_10 |
| | 9 | CY18 | DDR1_MA_9 |
| | 8 | DA19 | DDR1_MA_8 |
| | 7 | CT18 | DDR1_MA_7 |
| | 6 | CW19 | DDR1_MA_6 |
| | 5 | CY20 | DDR1_MA_5 |
| | 4 | CR19 | DDR1_MA_4 |
| | 3 | CW21 | DDR1_MA_3 |
| | 2 | CV20 | DDR1_MA_2 |
| | 1 | DA21 | DDR1_MA_1 |
| | 0 | CY22 | DDR1_MA_0 |
| M_F_CKE<5..0> | 5 | DA15 | DDR1_CKE_5 |
| | 4 | CY16 | DDR1_CKE_4 |
| | 3 | DF16 | DDR1_CKE_3 |
| | 2 | DD16 | DDR1_CKE_2 |
| | 1 | DC17 | DDR1_CKE_1 |
| | 0 | DA17 | DDR1_CKE_0 |
| M_F_ODT<5..0> | 5 | DD26 | DDR1_ODT_5 |
| | 4 | DA25 | DDR1_ODT_4 |
| | 3 | DC25 | DDR1_ODT_3 |
| | 2 | DC23 | DDR1_ODT_2 |
| | 1 | DE25 | DDR1_ODT_1 |
| | 0 | DD22 | DDR1_ODT_0 |
| M_F_CS_N<9:0> | 9 | DF26 | DDR1_CS9_N |
| | 8 | DF24 | DDR1_CS8_N |
| | 7 | CV26 | DDR1_CS7_N_CID_4 |
| | 6 | CY26 | DDR1_CS6_N_CID_3 |
| | 5 | DD24 | DDR1_CS5_N |
| | 4 | DA23 | DDR1_CS4_N |
| | 3 | CP26 | DDR1_CS3_N_CID_1 |
| | 2 | CT26 | DDR1_CS2_N_CID_0 |
| | 1 | DE23 | DDR1_CS1_N |
| | 0 | DF22 | DDR1_CS0_N |
| M_F_C<2> | | CR25 | DDR1_CID_2 |
| M_F_ACT_N | | CT16 | DDR1_ACT_N |
| M_F_ALERT_N | | CR15 | DDR1_ALERT_N |
| M_F_PAR | | CT20 | DDR1_PAR |

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# CPU HASWELL SOCKET1 (4 OF 11)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT | CCBU | PROJCET | S2B | DOCUMENT NUMBER DA0S2BMB8A0 REV 1 |
| | DESIGNER | NICK | | | |
| | REVIEWER | PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:51:39 2015 | SHEET 24 OF 188 |

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DGA^1000014

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HSX_EP_EXT

M_G_DQ<63:0> BI 67 66 65

| | | |
|---|---|---|
| 63 | AL7 | DDR2_DQ_63 |
| 62 | AK8 | DDR2_DQ_62 |
| 61 | AE9 | DDR2_DQ_61 |
| 60 | AE7 | DDR2_DQ_60 |
| 59 | AL9 | DDR2_DQ_59 |
| 58 | AK10 | DDR2_DQ_58 |
| 57 | AG7 | DDR2_DQ_57 |
| 56 | AG9 | DDR2_DQ_56 |
| 55 | AL15 | DDR2_DQ_55 |
| 54 | AK14 | DDR2_DQ_54 |
| 53 | AF14 | DDR2_DQ_53 |
| 52 | AG15 | DDR2_DQ_52 |
| 51 | AL13 | DDR2_DQ_51 |
| 50 | AK12 | DDR2_DQ_50 |
| 49 | AF12 | DDR2_DQ_49 |
| 48 | AE11 | DDR2_DQ_48 |
| 47 | Y8 | DDR2_DQ_47 |
| 46 | AA9 | DDR2_DQ_46 |
| 45 | U11 | DDR2_DQ_45 |
| 44 | T10 | DDR2_DQ_44 |
| 43 | AB8 | DDR2_DQ_43 |
| 42 | AA11 | DDR2_DQ_42 |
| 41 | W11 | DDR2_DQ_41 |
| 40 | U9 | DDR2_DQ_40 |
| 39 | M6 | DDR2_DQ_39 |
| 38 | K6 | DDR2_DQ_38 |
| 37 | L9 | DDR2_DQ_37 |
| 36 | J9 | DDR2_DQ_36 |
| 35 | P6 | DDR2_DQ_35 |
| 34 | R7 | DDR2_DQ_34 |
| 33 | K8 | DDR2_DQ_33 |
| 32 | N9 | DDR2_DQ_32 |
| 31 | T24 | DDR2_DQ_31 |
| 30 | V24 | DDR2_DQ_30 |
| 29 | T28 | DDR2_DQ_29 |
| 28 | V28 | DDR2_DQ_28 |
| 27 | R23 | DDR2_DQ_27 |
| 26 | U23 | DDR2_DQ_26 |
| 25 | R27 | DDR2_DQ_25 |
| 24 | U27 | DDR2_DQ_24 |
| 23 | AC31 | DDR2_DQ_23 |
| 22 | AE31 | DDR2_DQ_22 |
| 21 | AA35 | DDR2_DQ_21 |
| 20 | AC35 | DDR2_DQ_20 |
| 19 | AB30 | DDR2_DQ_19 |
| 18 | AD30 | DDR2_DQ_18 |
| 17 | AB34 | DDR2_DQ_17 |
| 16 | AD34 | DDR2_DQ_16 |
| 15 | W31 | DDR2_DQ_15 |
| 14 | T32 | DDR2_DQ_14 |
| 13 | R35 | DDR2_DQ_13 |
| 12 | U35 | DDR2_DQ_12 |
| 11 | T30 | DDR2_DQ_11 |
| 10 | V30 | DDR2_DQ_10 |
| 9 | U33 | DDR2_DQ_9 |
| 8 | V34 | DDR2_DQ_8 |
| 7 | U37 | DDR2_DQ_7 |
| 6 | T38 | DDR2_DQ_6 |
| 5 | AC39 | DDR2_DQ_5 |
| 4 | AE37 | DDR2_DQ_4 |
| 3 | Y38 | DDR2_DQ_3 |
| 2 | R37 | DDR2_DQ_2 |
| 1 | AA37 | DDR2_DQ_1 |
| 0 | AD38 | DDR2_DQ_0 |

M_G_ECC<7..0> BI 67 66 65

| | | |
|---|---|---|
| 7 | AB24 | DDR2_ECC_7 |
| 6 | AD24 | DDR2_ECC_6 |
| 5 | AB28 | DDR2_ECC_5 |
| 4 | AD28 | DDR2_ECC_4 |
| 3 | AA23 | DDR2_ECC_3 |
| 2 | AC23 | DDR2_ECC_2 |
| 1 | AA27 | DDR2_ECC_1 |
| 0 | AC27 | DDR2_ECC_0 |

M_G_CLK_DP<3..0> OUT 67 66 65

| | | |
|---|---|---|
| 3 | AA19 | DDR2_CLK_DP_3 |
| 2 | AB18 | DDR2_CLK_DP_2 |
| 1 | AB20 | DDR2_CLK_DP_1 |
| 0 | AA17 | DDR2_CLK_DP_0 |

M_G_CLK_DN<3..0> OUT 67 66 65

| | | |
|---|---|---|
| 3 | W19 | DDR2_CLK_DN_3 |
| 2 | Y18 | DDR2_CLK_DN_2 |
| 1 | Y20 | DDR2_CLK_DN_1 |
| 0 | W17 | DDR2_CLK_DN_0 |

M_G_BG<1:0> OUT 67 66 65

| | | |
|---|---|---|
| 1 | AD20 | DDR2_BG_1 |
| 0 | AA21 | DDR2_BG_0 |

M_G_BA<1:0> OUT 67 66 65

| | | |
|---|---|---|
| 1 | U17 | DDR2_BA_1 |
| 0 | M14 | DDR2_BA_0 |

M_G_DQS_DP<17:0> BI 65 66 67

| | | |
|---|---|---|
| DDR2_DQS_DP_17 | AD26 | 17 |
| DDR2_DQS_DP_16 | AH10 | 16 |
| DDR2_DQS_DP_15 | AH16 | 15 |
| DDR2_DQS_DP_14 | V8 | 14 |
| DDR2_DQS_DP_13 | M8 | 13 |
| DDR2_DQS_DP_12 | V26 | 12 |
| DDR2_DQS_DP_11 | AC33 | 11 |
| DDR2_DQS_DP_10 | T34 | 10 |
| DDR2_DQS_DP_9 | AB38 | 9 |
| DDR2_DQS_DP_8 | AC25 | 8 |
| DDR2_DQS_DP_7 | AJ7 | 7 |
| DDR2_DQS_DP_6 | AH12 | 6 |
| DDR2_DQS_DP_5 | AB10 | 5 |
| DDR2_DQS_DP_4 | N7 | 4 |
| DDR2_DQS_DP_3 | U25 | 3 |
| DDR2_DQS_DP_2 | AB32 | 2 |
| DDR2_DQS_DP_1 | U31 | 1 |
| DDR2_DQS_DP_0 | V38 | 0 |

M_G_DQS_DN<17:0> BI 65 66 67

| | | |
|---|---|---|
| DDR2_DQS_DN_17 | AB26 | 17 |
| DDR2_DQS_DN_16 | AJ9 | 16 |
| DDR2_DQS_DN_15 | AJ15 | 15 |
| DDR2_DQS_DN_14 | W9 | 14 |
| DDR2_DQS_DN_13 | L7 | 13 |
| DDR2_DQS_DN_12 | T26 | 12 |
| DDR2_DQS_DN_11 | AA33 | 11 |
| DDR2_DQS_DN_10 | R33 | 10 |
| DDR2_DQS_DN_9 | AC37 | 9 |
| DDR2_DQS_DN_8 | AE25 | 8 |
| DDR2_DQS_DN_7 | AH8 | 7 |
| DDR2_DQS_DN_6 | AJ13 | 6 |
| DDR2_DQS_DN_5 | Y10 | 5 |
| DDR2_DQS_DN_4 | P8 | 4 |
| DDR2_DQS_DN_3 | W25 | 3 |
| DDR2_DQS_DN_2 | AD32 | 2 |
| DDR2_DQS_DN_1 | V32 | 1 |
| DDR2_DQS_DN_0 | W37 | 0 |

M_G_MA<17:0> OUT 65 66 67

| | | |
|---|---|---|
| DDR2_MA_17 | T14 | 17 |
| DDR2_MA_16 | P14 | 16 |
| DDR2_MA_15 | R13 | 15 |
| DDR2_MA_14 | Y14 | 14 |
| DDR2_MA_13 | P12 | 13 |
| DDR2_MA_12 | W21 | 12 |
| DDR2_MA_11 | T20 | 11 |
| DDR2_MA_10 | AA15 | 10 |
| DDR2_MA_9 | P20 | 9 |
| DDR2_MA_8 | L19 | 8 |
| DDR2_MA_7 | U19 | 7 |
| DDR2_MA_6 | M18 | 6 |
| DDR2_MA_5 | P18 | 5 |
| DDR2_MA_4 | R19 | 4 |
| DDR2_MA_3 | L17 | 3 |
| DDR2_MA_2 | T18 | 2 |
| DDR2_MA_1 | M16 | 1 |
| DDR2_MA_0 | L15 | 0 |

M_G_CKE<5..0> OUT 65 66 67

| | | |
|---|---|---|
| DDR2_CKE_5 | AD22 | 5 |
| DDR2_CKE_4 | AB22 | 4 |
| DDR2_CKE_3 | Y22 | 3 |
| DDR2_CKE_2 | T22 | 2 |
| DDR2_CKE_1 | U21 | 1 |
| DDR2_CKE_0 | R21 | 0 |

M_G_ODT<5..0> OUT 65 66 67

| | | |
|---|---|---|
| DDR2_ODT_5 | AD14 | 5 |
| DDR2_ODT_4 | AE17 | 4 |
| DDR2_ODT_3 | AB14 | 3 |
| DDR2_ODT_2 | R15 | 2 |
| DDR2_ODT_1 | W15 | 1 |
| DDR2_ODT_0 | Y16 | 0 |

M_G_CS_N<9:0> OUT 65 66 67

| | | |
|---|---|---|
| DDR2_CS9_N | T12 | 9 |
| DDR2_CS8_N | AD18 | 8 |
| DDR2_CS7_N_CID_4 | AD16 | 7 |
| DDR2_CS6_N_CID_3 | AC13 | 6 |
| DDR2_CS5_N | U15 | 5 |
| DDR2_CS4_N | P16 | 4 |
| DDR2_CS3_N_CID_1 | AA13 | 3 |
| DDR2_CS2_N_CID_0 | W13 | 2 |
| DDR2_CS1_N | T16 | 1 |
| DDR2_CS0_N | AB16 | 0 |

| | | | |
|---|---|---|---|
| DDR2_CID_2 | U13 | M_G_C<2> | OUT 65 66 67 |
| DDR2_ACT_N | AE21 | M_G_ACT_N | OUT 65 66 67 |
| DDR2_ALERT_N | P22 | M_G_ALERT_N | IN 65 66 67 |
| DDR2_PAR | R17 | M_G_PAR | OUT 65 66 67 |

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# CPU HASWELL SOCKET1 (5 OF 11)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:51:41 2015 | SHEET 25 OF 188 |

SMLF
LGA2011_R3
U93
DGA^1000014
I0

HSX_EP_EXT

| | | | | | |
|---|---|---|---|---|---|
| 63 | AB6 | DDR3_DQ_63 | DDR3_DQS_DP_17 | M26 | 17 |
| 62 | AC3 | DDR3_DQ_62 | DDR3_DQS_DP_16 | Y6 | 16 |
| 61 | V6 | DDR3_DQ_61 | DDR3_DQS_DP_15 | AH4 | 15 |
| 60 | U5 | DDR3_DQ_60 | DDR3_DQS_DP_14 | B8 | 14 |
| 59 | AE5 | DDR3_DQ_59 | DDR3_DQS_DP_13 | M4 | 13 |
| 58 | AC5 | DDR3_DQ_58 | DDR3_DQS_DP_12 | F26 | 12 |
| 57 | W3 | DDR3_DQ_57 | DDR3_DQS_DP_11 | J33 | 11 |
| 56 | V4 | DDR3_DQ_56 | DDR3_DQS_DP_10 | C35 | 10 |
| 55 | AL1 | DDR3_DQ_55 | DDR3_DQS_DP_9 | F38 | 9 |
| 54 | AJ3 | DDR3_DQ_54 | DDR3_DQS_DP_8 | L25 | 8 |
| 53 | AE3 | DDR3_DQ_53 | DDR3_DQS_DP_7 | AB4 | 7 |
| 52 | AG5 | DDR3_DQ_52 | DDR3_DQS_DP_6 | AK2 | 6 |
| 51 | AL5 | DDR3_DQ_51 | DDR3_DQS_DP_5 | E7 | 5 |
| 50 | AL3 | DDR3_DQ_50 | DDR3_DQS_DP_4 | H2 | 4 |
| 49 | AG1 | DDR3_DQ_49 | DDR3_DQS_DP_3 | E25 | 3 |
| 48 | AG3 | DDR3_DQ_48 | DDR3_DQS_DP_2 | M32 | 2 |
| 47 | G7 | DDR3_DQ_47 | DDR3_DQS_DP_1 | B32 | 1 |
| 46 | D6 | DDR3_DQ_46 | DDR3_DQS_DP_0 | E37 | 0 |
| 45 | A9 | DDR3_DQ_45 | | | |
| 44 | C9 | DDR3_DQ_44 | DDR3_DQS_DN_17 | K26 | 17 |
| 43 | F6 | DDR3_DQ_43 | DDR3_DQS_DN_16 | W5 | 16 |
| 42 | E5 | DDR3_DQ_42 | DDR3_DQS_DN_15 | AJ5 | 15 |
| 41 | F8 | DDR3_DQ_41 | DDR3_DQS_DN_14 | D8 | 14 |
| 40 | E9 | DDR3_DQ_40 | DDR3_DQS_DN_13 | L3 | 13 |
| 39 | R3 | DDR3_DQ_39 | DDR3_DQS_DN_12 | D26 | 12 |
| 38 | K2 | DDR3_DQ_38 | DDR3_DQS_DN_11 | L33 | 11 |
| 37 | N3 | DDR3_DQ_37 | DDR3_DQS_DN_10 | D34 | 10 |
| 36 | P4 | DDR3_DQ_36 | DDR3_DQS_DN_9 | H38 | 9 |
| 35 | L1 | DDR3_DQ_35 | DDR3_DQS_DN_8 | N25 | 8 |
| 34 | J1 | DDR3_DQ_34 | DDR3_DQS_DN_7 | AA5 | 7 |
| 33 | H4 | DDR3_DQ_33 | DDR3_DQS_DN_6 | AJ1 | 6 |
| 32 | K4 | DDR3_DQ_32 | DDR3_DQS_DN_5 | C7 | 5 |
| 31 | B24 | DDR3_DQ_31 | DDR3_DQS_DN_4 | G3 | 4 |
| 30 | C25 | DDR3_DQ_30 | DDR3_DQS_DN_3 | G25 | 3 |
| 29 | E29 | DDR3_DQ_29 | DDR3_DQS_DN_2 | K32 | 2 |
| 28 | G29 | DDR3_DQ_28 | DDR3_DQS_DN_1 | A33 | 1 |
| 27 | E23 | DDR3_DQ_27 | DDR3_DQS_DN_0 | C37 | 0 |
| 26 | F24 | DDR3_DQ_26 | | | |
| 25 | E27 | DDR3_DQ_25 | DDR3_MA_17 | L11 | 17 |
| 24 | F28 | DDR3_DQ_24 | DDR3_MA_16 | J13 | 16 |
| 23 | N31 | DDR3_DQ_23 | DDR3_MA_15 | F12 | 15 |
| 22 | L31 | DDR3_DQ_22 | DDR3_MA_14 | K12 | 14 |
| 21 | L35 | DDR3_DQ_21 | DDR3_MA_13 | M12 | 13 |
| 20 | J35 | DDR3_DQ_20 | DDR3_MA_12 | M20 | 12 |
| 19 | M30 | DDR3_DQ_19 | DDR3_MA_11 | K20 | 11 |
| 18 | K30 | DDR3_DQ_18 | DDR3_MA_10 | L13 | 10 |
| 17 | M34 | DDR3_DQ_17 | DDR3_MA_9 | F20 | 9 |
| 16 | K34 | DDR3_DQ_16 | DDR3_MA_8 | G19 | 8 |
| 15 | E33 | DDR3_DQ_15 | DDR3_MA_7 | J19 | 7 |
| 14 | D32 | DDR3_DQ_14 | DDR3_MA_6 | F18 | 6 |
| 13 | E35 | DDR3_DQ_13 | DDR3_MA_5 | K18 | 5 |
| 12 | F34 | DDR3_DQ_12 | DDR3_MA_4 | J17 | 4 |
| 11 | E31 | DDR3_DQ_11 | DDR3_MA_3 | G17 | 3 |
| 10 | G31 | DDR3_DQ_10 | DDR3_MA_2 | F16 | 2 |
| 9 | B34 | DDR3_DQ_9 | DDR3_MA_1 | K16 | 1 |
| 8 | A35 | DDR3_DQ_8 | DDR3_MA_0 | G15 | 0 |
| 7 | K38 | DDR3_DQ_7 | | | |
| 6 | G37 | DDR3_DQ_6 | DDR3_CKE_5 | K22 | 5 |
| 5 | J39 | DDR3_DQ_5 | DDR3_CKE_4 | B22 | 4 |
| 4 | C39 | DDR3_DQ_4 | DDR3_CKE_3 | D22 | 3 |
| 3 | M38 | DDR3_DQ_3 | DDR3_CKE_2 | A21 | 2 |
| 2 | L37 | DDR3_DQ_2 | DDR3_CKE_1 | E21 | 1 |
| 1 | B38 | DDR3_DQ_1 | DDR3_CKE_0 | F22 | 0 |
| 0 | D38 | DDR3_DQ_0 | | | |
| | | | DDR3_ODT_5 | E11 | 5 |
| 7 | K24 | DDR3_ECC_7 | DDR3_ODT_4 | E13 | 4 |
| 6 | M24 | DDR3_ECC_6 | DDR3_ODT_3 | D12 | 3 |
| 5 | M28 | DDR3_ECC_5 | DDR3_ODT_2 | D14 | 2 |
| 4 | K28 | DDR3_ECC_4 | DDR3_ODT_1 | A13 | 1 |
| 3 | J23 | DDR3_ECC_3 | DDR3_ODT_0 | D16 | 0 |
| 2 | L23 | DDR3_ECC_2 | | | |
| 1 | J27 | DDR3_ECC_1 | DDR3_CS9_N | B12 | 9 |
| 0 | L27 | DDR3_ECC_0 | DDR3_CS8_N | B14 | 8 |
| | | | DDR3_CS7_N_CID_4 | A11 | 7 |
| 3 | A19 | DDR3_CLK_DP_3 | DDR3_CS6_N_CID_3 | G11 | 6 |
| 2 | B18 | DDR3_CLK_DP_2 | DDR3_CS5_N | F14 | 5 |
| 1 | B20 | DDR3_CLK_DP_1 | DDR3_CS4_N | A15 | 4 |
| 0 | A17 | DDR3_CLK_DP_0 | DDR3_CS3_N_CID_1 | H10 | 3 |
| 3 | C19 | DDR3_CLK_DN_3 | DDR3_CS2_N_CID_0 | F10 | 2 |
| 2 | D18 | DDR3_CLK_DN_2 | DDR3_CS1_N | C15 | 1 |
| 1 | D20 | DDR3_CLK_DN_1 | DDR3_CS0_N | B16 | 0 |
| 0 | C17 | DDR3_CLK_DN_0 | | | |
| | | | DDR3_CID_2 | J11 | M_H_C<2> |
| 1 | G21 | DDR3_BG_1 | | | |
| 0 | J21 | DDR3_BG_0 | DDR3_ACT_N | L21 | M_H_ACT_N |
| 1 | K14 | DDR3_BA_1 | DDR3_ALERT_N | M22 | M_H_ALERT_N |
| 0 | G13 | DDR3_BA_0 | DDR3_PAR | J15 | M_H_PAR |

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70 69 68 BI M_H_DQ<63:0>

M_H_DQS_DP<17:0> BI 68 69 70

M_H_DQS_DN<17:0> BI 68 69 70

M_H_MA<17:0> OUT 68 69 70

M_H_CKE<5..0> OUT 68 69 70

M_H_ODT<5..0> OUT 68 69 70

M_H_CS_N<9:0> OUT 68 69 70

70 69 68 BI M_H_ECC<7..0>

70 69 68 OUT M_H_CLK_DP<3..0>

70 69 68 OUT M_H_CLK_DN<3..0>

70 69 68 OUT M_H_BG<1:0>

70 69 68 OUT M_H_BA<1:0>

M_H_C<2> OUT 68 69 70

M_H_ACT_N OUT 68 69 70

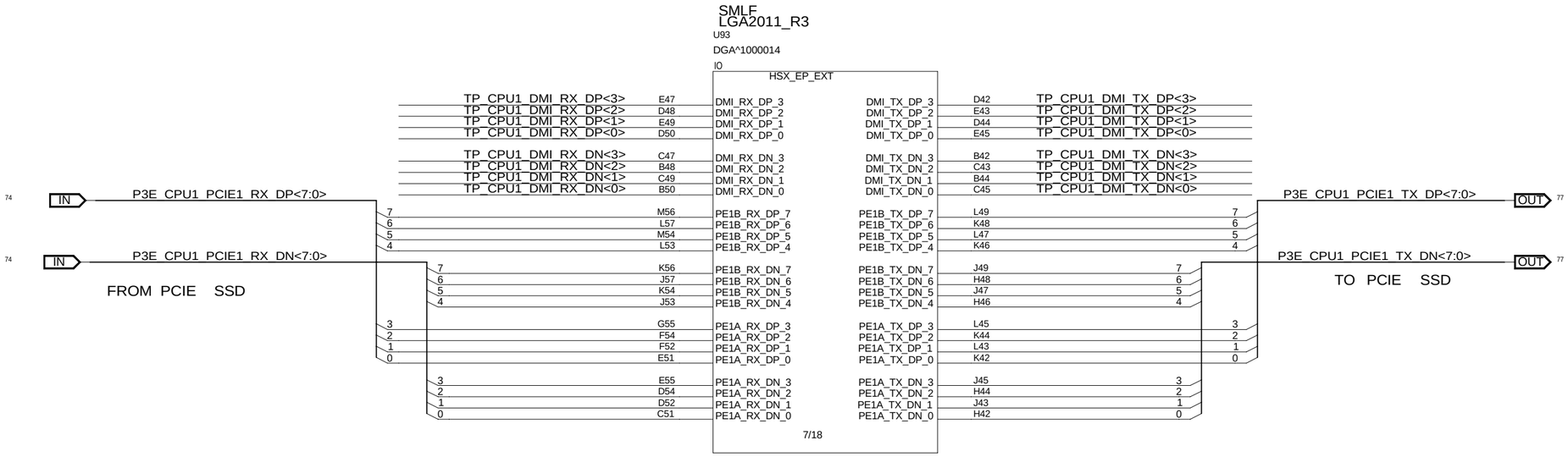
M_H_ALERT_N IN 68 69 70

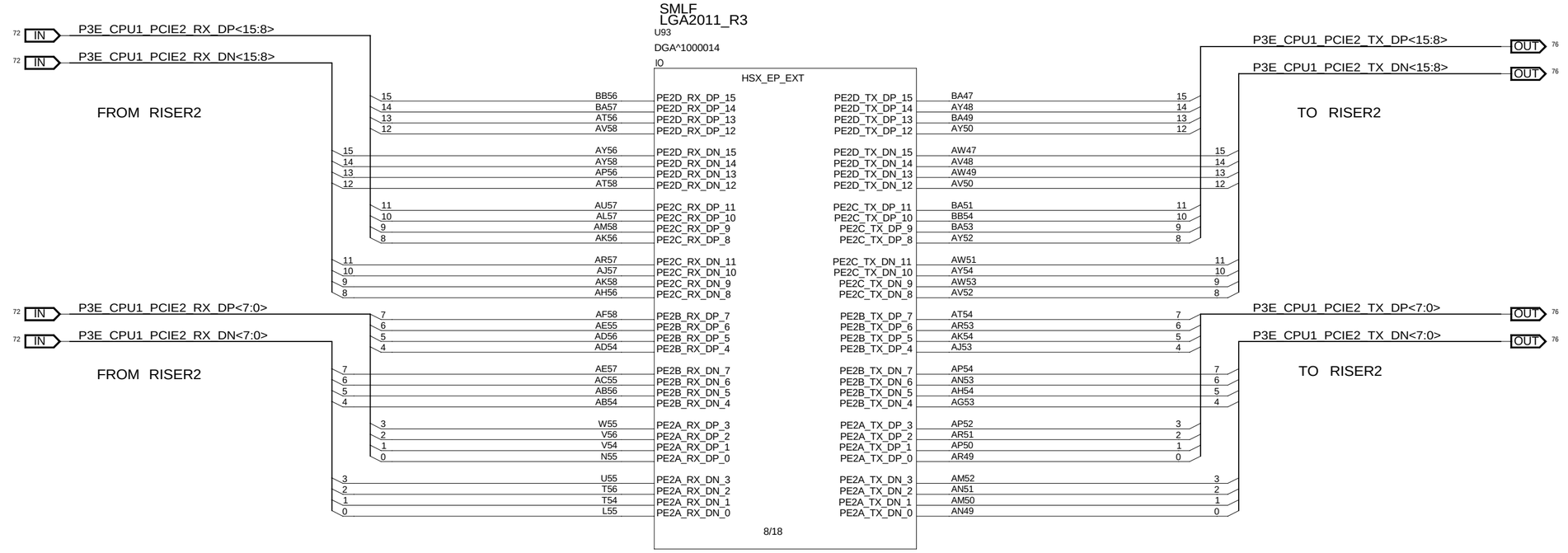
M_H_PAR OUT 68 69 70

# CPU HASWELL SOCKET1 (6 OF 11)

Quanta

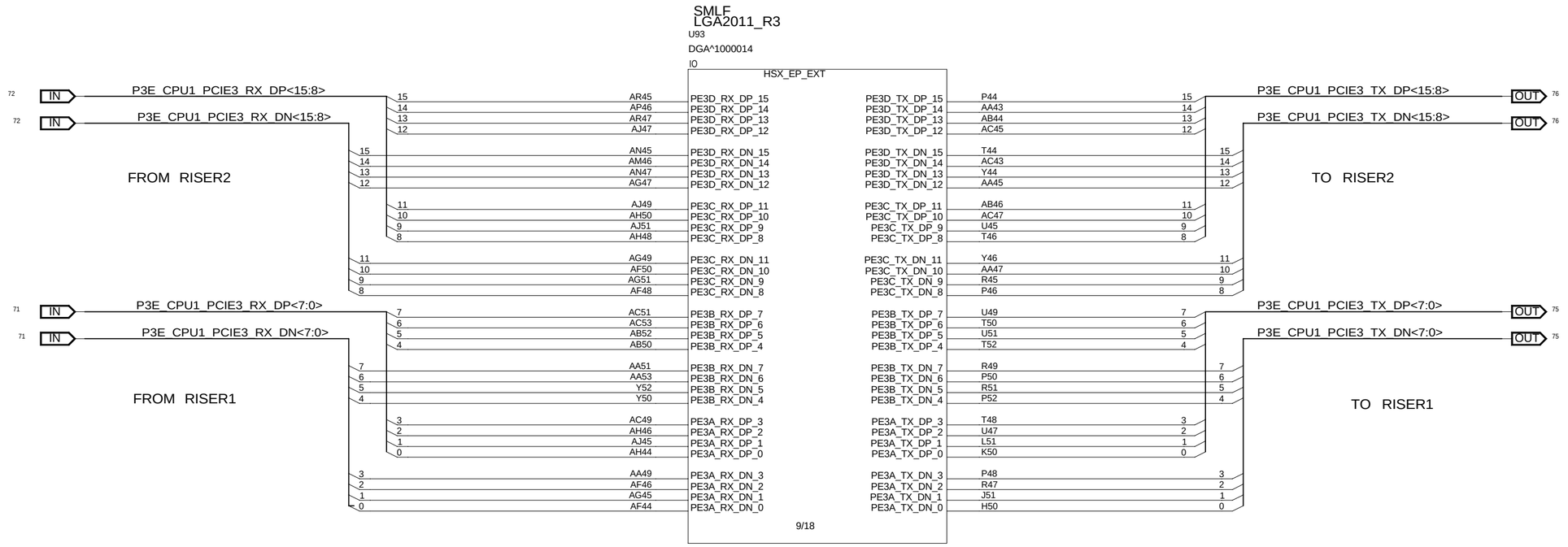
| | | | |
|---|---|---|---|
| DEPARTMENT | DESIGNER | PROJCET | DOCUMENT NUMBER / REV |
| CCBU | NICK | S2B | DA0S2BMB8A0 / 1 |
| | REVIEWER PETER,YULIN,MATT | SIZE C DATE Mon Nov 16 11:51:43 2015 | SHEET 26 OF 188 |



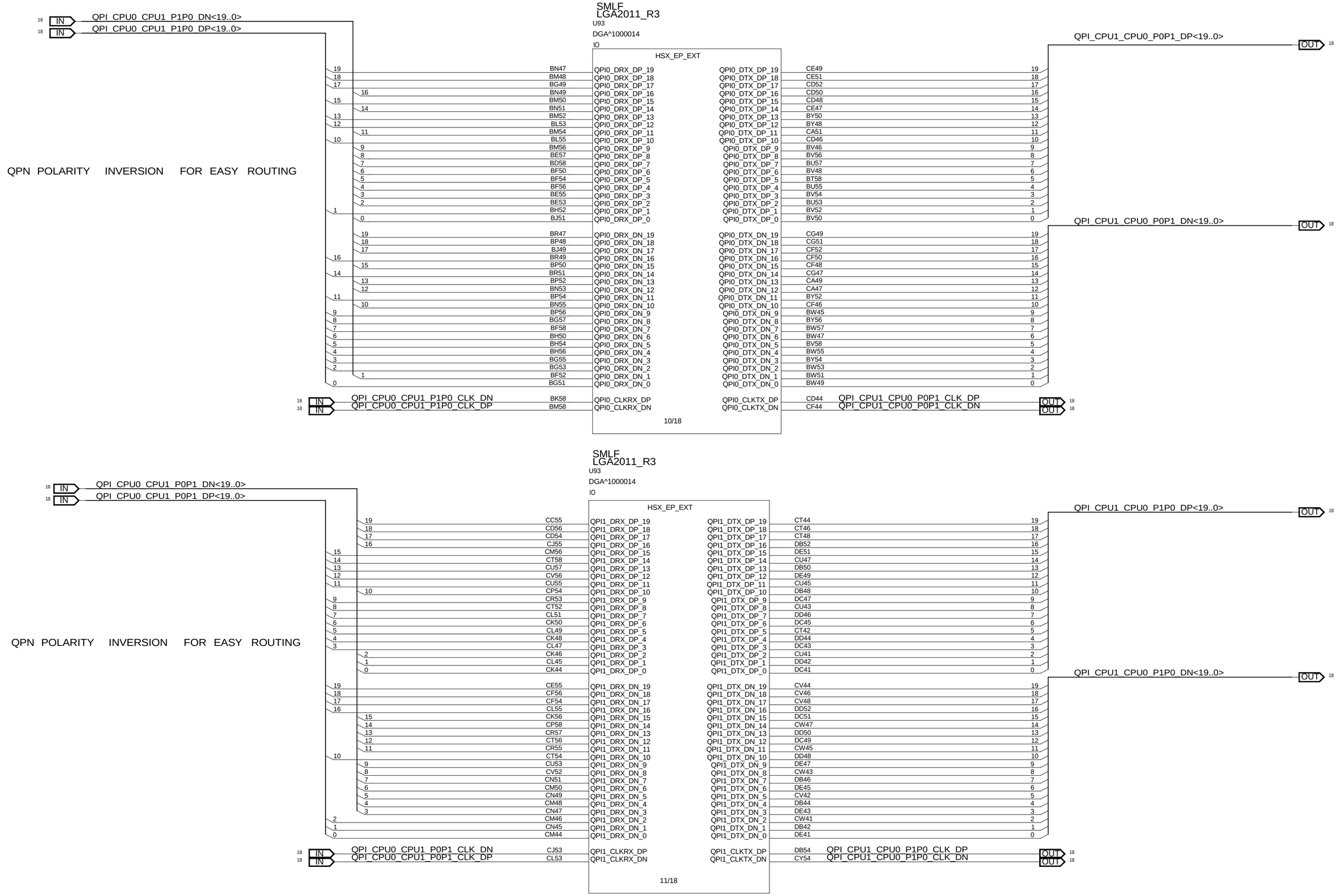

# CPU HASWELL SOCKET1 (7 OF 11)

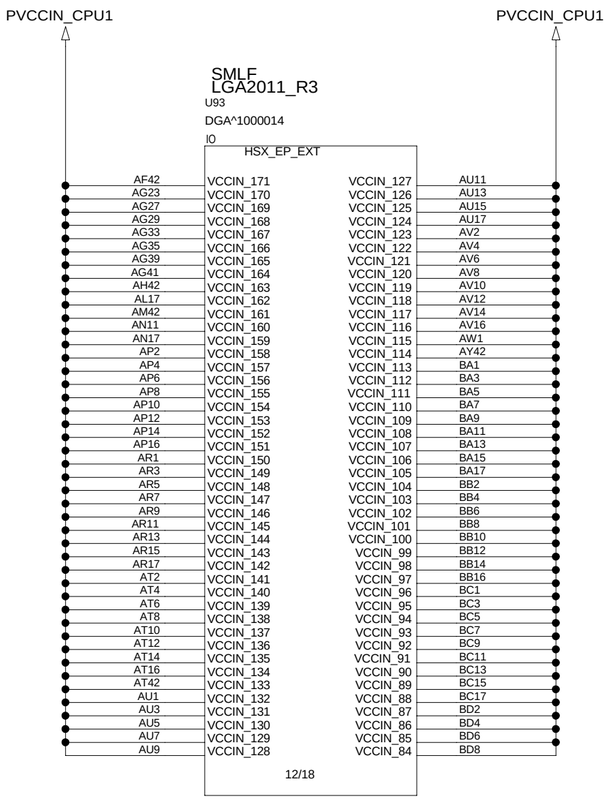
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | | |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:51:45 2015 | SHEET: 27 OF 188 | | |

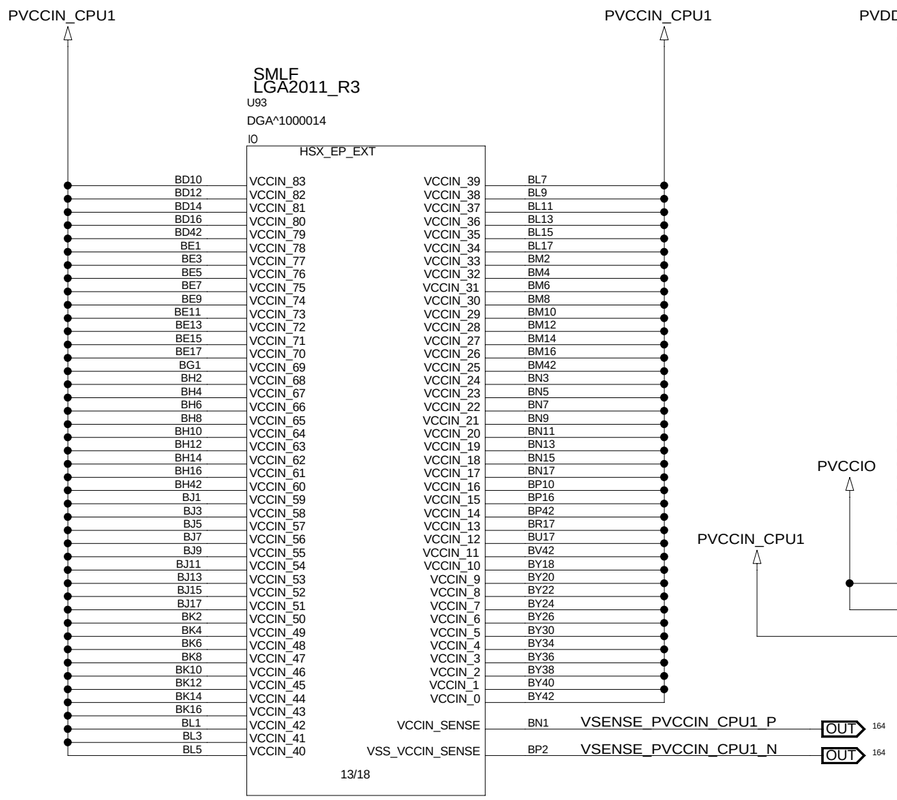


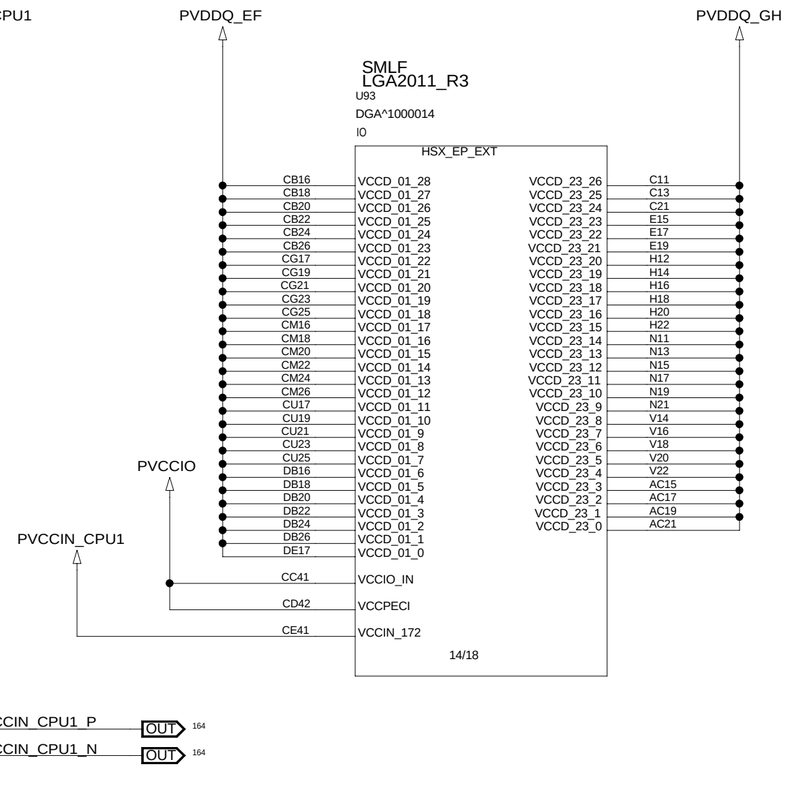

# CPU HASWELL SOCKET1 (8 OF 11)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | | |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:51:46 2015 | SHEET 28 OF 188 | | |


QPI_CPU0_CPU1_P1P0_DN<19..0>
QPI_CPU0_CPU1_P1P0_DP<19..0>
QPN POLARITY INVERSION FOR EASY ROUTING
SMLF
LGA2011_R3
U93
DGA^1000014
IO
HSX_EP_EXT
QPI0_DRX_DP_19 BN47
QPI0_DRX_DP_18 BM48
QPI0_DRX_DP_17 BG49
QPI0_DRX_DP_16 BN49
QPI0_DRX_DP_15 BM50
QPI0_DRX_DP_14 BN51
QPI0_DRX_DP_13 BM52
QPI0_DRX_DP_12 BL53
QPI0_DRX_DP_11 BM54
QPI0_DRX_DP_10 BL55
QPI0_DRX_DP_9 BM56
QPI0_DRX_DP_8 BE57
QPI0_DRX_DP_7 BD58
QPI0_DRX_DP_6 BF50
QPI0_DRX_DP_5 BF54
QPI0_DRX_DP_4 BF56
QPI0_DRX_DP_3 BE55
QPI0_DRX_DP_2 BE53
QPI0_DRX_DP_1 BH52
QPI0_DRX_DP_0 BJ51
QPI0_DRX_DN_19 BR47
QPI0_DRX_DN_18 BP48
QPI0_DRX_DN_17 BJ49
QPI0_DRX_DN_16 BR49
QPI0_DRX_DN_15 BP50
QPI0_DRX_DN_14 BR51
QPI0_DRX_DN_13 BP52
QPI0_DRX_DN_12 BN53
QPI0_DRX_DN_11 BP54
QPI0_DRX_DN_10 BN55
QPI0_DRX_DN_9 BP56
QPI0_DRX_DN_8 BG57
QPI0_DRX_DN_7 BF58
QPI0_DRX_DN_6 BH50
QPI0_DRX_DN_5 BH54
QPI0_DRX_DN_4 BH56
QPI0_DRX_DN_3 BG55
QPI0_DRX_DN_2 BG53
QPI0_DRX_DN_1 BF52
QPI0_DRX_DN_0 BG51
QPI0_CLKRX_DP BK58
QPI0_CLKRX_DN BM58
QPI_CPU0_CPU1_P1P0_CLK_DN
QPI_CPU0_CPU1_P1P0_CLK_DP
QPI0_DTX_DP_19 CE49
QPI0_DTX_DP_18 CE51
QPI0_DTX_DP_17 CD62
QPI0_DTX_DP_16 CD50
QPI0_DTX_DP_15 CD48
QPI0_DTX_DP_14 CE47
QPI0_DTX_DP_13 BY50
QPI0_DTX_DP_12 BY48
QPI0_DTX_DP_11 CA51
QPI0_DTX_DP_10 CD46
QPI0_DTX_DP_9 BV46
QPI0_DTX_DP_8 BV56
QPI0_DTX_DP_7 BU57
QPI0_DTX_DP_6 BV48
QPI0_DTX_DP_5 BT58
QPI0_DTX_DP_4 BU55
QPI0_DTX_DP_3 BV54
QPI0_DTX_DP_2 BU53
QPI0_DTX_DP_1 BV52
QPI0_DTX_DP_0 BV50
QPI0_DTX_DN_19 CG49
QPI0_DTX_DN_18 CG51
QPI0_DTX_DN_17 CF52
QPI0_DTX_DN_16 CF50
QPI0_DTX_DN_15 CF48
QPI0_DTX_DN_14 CG47
QPI0_DTX_DN_13 CA49
QPI0_DTX_DN_12 CA47
QPI0_DTX_DN_11 BY52
QPI0_DTX_DN_10 CF46
QPI0_DTX_DN_9 BW45
QPI0_DTX_DN_8 BY56
QPI0_DTX_DN_7 BW57
QPI0_DTX_DN_6 BW47
QPI0_DTX_DN_5 BV58
QPI0_DTX_DN_4 BW55
QPI0_DTX_DN_3 BY54
QPI0_DTX_DN_2 BW53
QPI0_DTX_DN_1 BW51
QPI0_DTX_DN_0 BW49
QPI0_CLKTX_DP CD44
QPI0_CLKTX_DN CF44
QPI_CPU1_CPU0_P0P1_CLK_DP
QPI_CPU1_CPU0_P0P1_CLK_DN
10/18
QPI_CPU1_CPU0_P0P1_DP<19..0>
QPI_CPU1_CPU0_P0P1_DN<19..0>
QPI_CPU0_CPU1_P0P1_DN<19..0>
QPI_CPU0_CPU1_P0P1_DP<19..0>
QPN POLARITY INVERSION FOR EASY ROUTING
SMLF
LGA2011_R3
U93
DGA^1000014
IO
HSX_EP_EXT
QPI1_DRX_DP_19 CC55
QPI1_DRX_DP_18 CD56
QPI1_DRX_DP_17 CD54
QPI1_DRX_DP_16 CJ55
QPI1_DRX_DP_15 CM56
QPI1_DRX_DP_14 CT58
QPI1_DRX_DP_13 CU57
QPI1_DRX_DP_12 CV56
QPI1_DRX_DP_11 CU55
QPI1_DRX_DP_10 CP54
QPI1_DRX_DP_9 CR53
QPI1_DRX_DP_8 CT52
QPI1_DRX_DP_7 CL51
QPI1_DRX_DP_6 CK50
QPI1_DRX_DP_5 CL49
QPI1_DRX_DP_4 CK48
QPI1_DRX_DP_3 CL47
QPI1_DRX_DP_2 CK46
QPI1_DRX_DP_1 CL45
QPI1_DRX_DP_0 CK44
QPI1_DRX_DN_19 CE55
QPI1_DRX_DN_18 CF56
QPI1_DRX_DN_17 CF54
QPI1_DRX_DN_16 CL55
QPI1_DRX_DN_15 CK56
QPI1_DRX_DN_14 CP58
QPI1_DRX_DN_13 CR57
QPI1_DRX_DN_12 CT56
QPI1_DRX_DN_11 CR55
QPI1_DRX_DN_10 CT54
QPI1_DRX_DN_9 CU53
QPI1_DRX_DN_8 CV52
QPI1_DRX_DN_7 CN51
QPI1_DRX_DN_6 CM50
QPI1_DRX_DN_5 CN49
QPI1_DRX_DN_4 CM48
QPI1_DRX_DN_3 CN47
QPI1_DRX_DN_2 CM46
QPI1_DRX_DN_1 CN45
QPI1_DRX_DN_0 CM44
QPI1_CLKRX_DP CJ53
QPI1_CLKRX_DN CL53
QPI_CPU0_CPU1_P0P1_CLK_DN
QPI_CPU0_CPU1_P0P1_CLK_DP
QPI1_DTX_DP_19 CT44
QPI1_DTX_DP_18 CT46
QPI1_DTX_DP_17 CT48
QPI1_DTX_DP_16 DB52
QPI1_DTX_DP_15 DE51
QPI1_DTX_DP_14 CU47
QPI1_DTX_DP_13 DB50
QPI1_DTX_DP_12 DE49
QPI1_DTX_DP_11 CU45
QPI1_DTX_DP_10 DB48
QPI1_DTX_DP_9 DC47
QPI1_DTX_DP_8 CU43
QPI1_DTX_DP_7 DD46
QPI1_DTX_DP_6 DC45
QPI1_DTX_DP_5 CT42
QPI1_DTX_DP_4 DD44
QPI1_DTX_DP_3 DC43
QPI1_DTX_DP_2 CU41
QPI1_DTX_DP_1 DD42
QPI1_DTX_DP_0 DC41
QPI1_DTX_DN_19 CV44
QPI1_DTX_DN_18 CV46
QPI1_DTX_DN_17 CV48
QPI1_DTX_DN_16 DD52
QPI1_DTX_DN_15 DC51
QPI1_DTX_DN_14 CW47
QPI1_DTX_DN_13 DD50
QPI1_DTX_DN_12 DC49
QPI1_DTX_DN_11 CW45
QPI1_DTX_DN_10 DD48
QPI1_DTX_DN_9 DE47
QPI1_DTX_DN_8 CW43
QPI1_DTX_DN_7 DB46
QPI1_DTX_DN_6 DE45
QPI1_DTX_DN_5 CV42
QPI1_DTX_DN_4 DB44
QPI1_DTX_DN_3 DE43
QPI1_DTX_DN_2 CW41
QPI1_DTX_DN_1 DB42
QPI1_DTX_DN_0 DE41
QPI1_CLKTX_DP DB54
QPI1_CLKTX_DN CY54
QPI_CPU1_CPU0_P1P0_CLK_DP
QPI_CPU1_CPU0_P1P0_CLK_DN
11/18
QPI_CPU1_CPU0_P1P0_DP<19..0>
QPI_CPU1_CPU0_P1P0_DN<19..0>
CPU HASWELL SOCKET1 (9 OF 11)
Quanta
DEPARTMENT CCBU
DESIGNER NICK
REVIEWER PETER,YULIN,MATT
PROJCET S2B
DOCUMENT NUMBER DA0S2BMB8A0
REV 1
SIZE C
DATE Mon Nov 16 11:51:47 2015
SHEET 29 OF 188

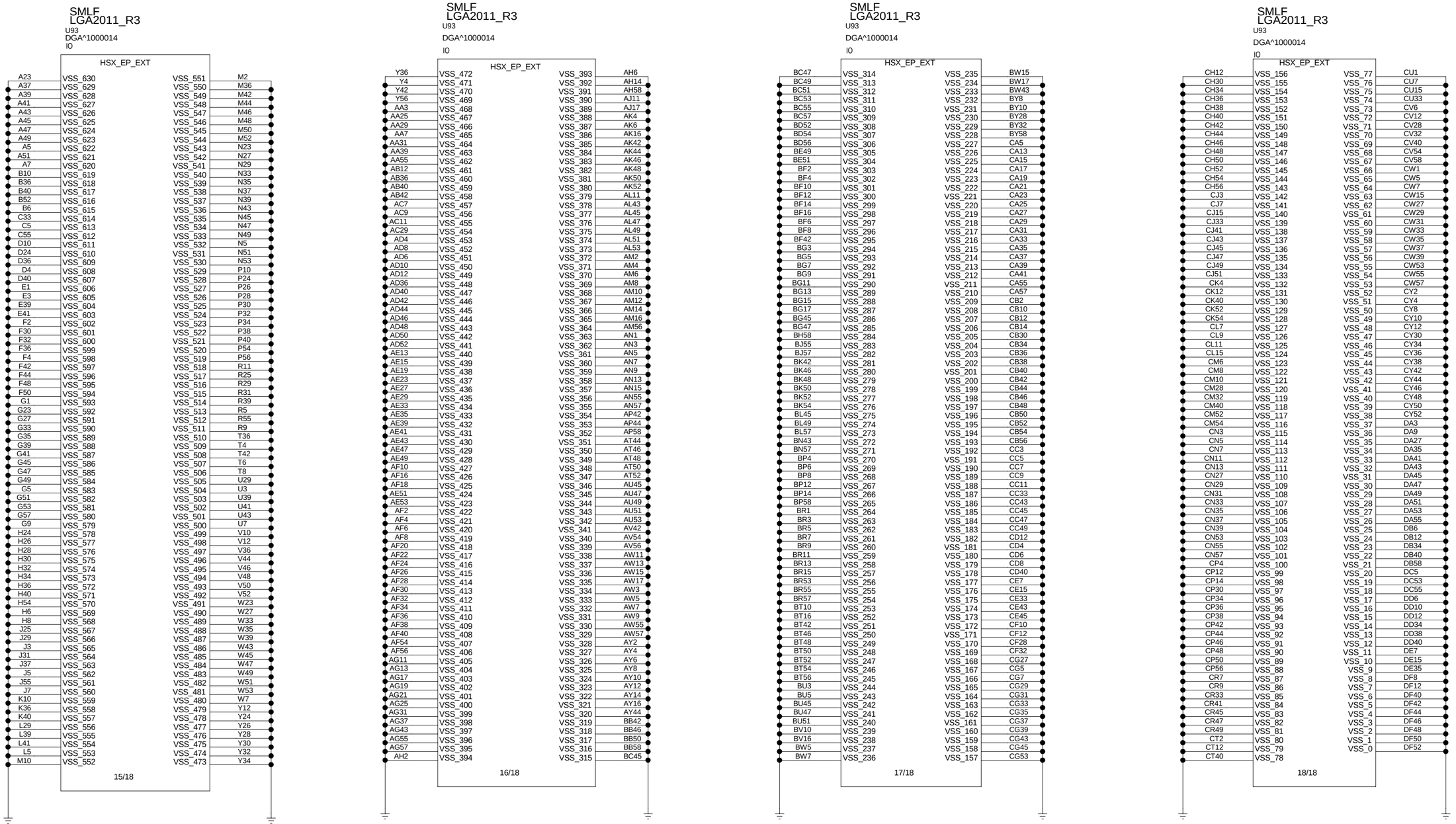



# CPU HASWELL SOCKET1 (10 OF 11)

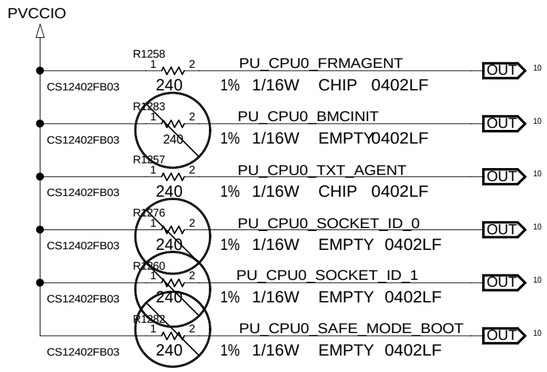
| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:51:49 2015 | SHEET 30 OF 188 | |

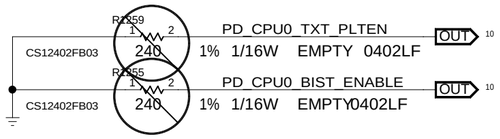



# CPU HASWELL SOCKET1 (11 OF 11)

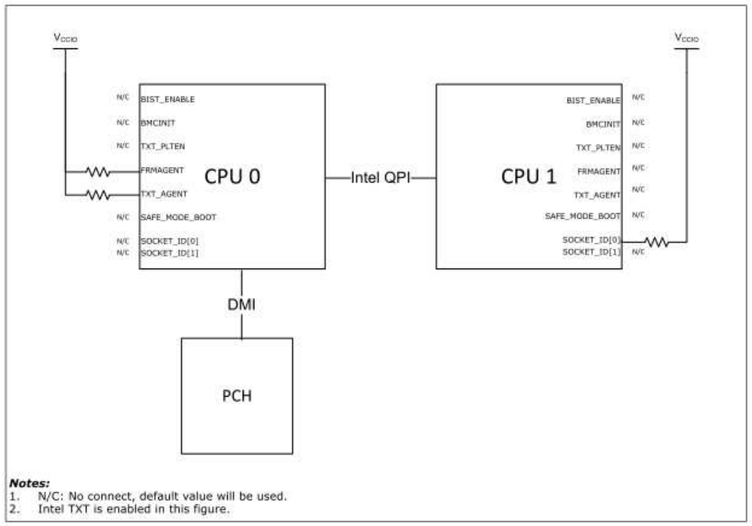
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:51:50 2015 | SHEET: 31 OF 188 |

# CPU0 STRAPS




BIST:(INTERNAL PU)
DISABLE BIST FOR A STEPPING CPU
ENABLE BIST FOR B STEPPING (OR LATER) CPU



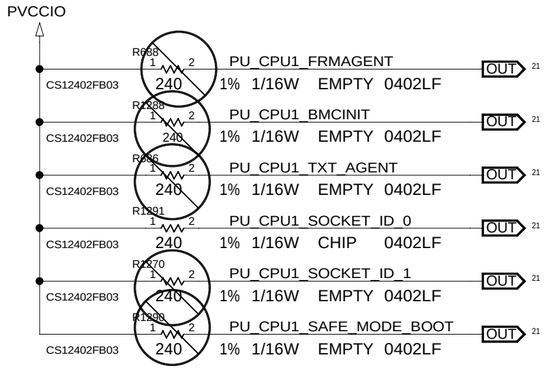

***Notes:***
1. N/C: No connect, default value will be used.
2. Intel TXT is enabled in this figure.

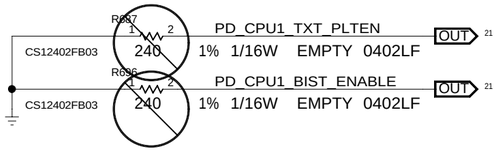
## Table 5-34. Intel TXT Strap Signal Configuration

| Signal Name | Intel TXT Default Setting | CPU0 | CPU1 | CPU2 | CPU3 |
|---|---|---|---|---|---|
| **Intel TXT Enabled** | | | | | |
| TXT_AGENT | Disabled | Pull-up | No Connect | No Connect | No Connect |
| TXT_PLTEN | Enabled | No Connect | No Connect | No Connect | No Connect |
| **Intel TXT Disabled** | | | | | |
| TXT_AGENT | Disabled | No Connect | No Connect | No Connect | No Connect |
| TXT_PLTEN | Enabled | Pull-down | Pull-down | Pull-down | Pull-down |
| ***Notes:*** A pull-up on board to $V_{CCIO}$ is via a 240 ohm resistor ±5% or a pull-down on board to VSS is via 240 ohm resistor ±5%. | | | | | |

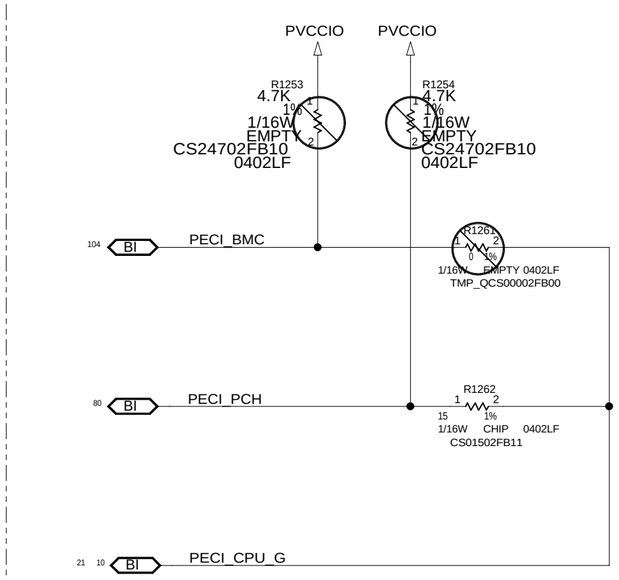
# CPU1 STRAPS

EMPTY PU OF CPU1_FRMAGENT IS SUGGEST BY TME
AND IT NEED TO BE CHECKED AGAIN WITH LATER RELEASE OF DOCUMENTATION.



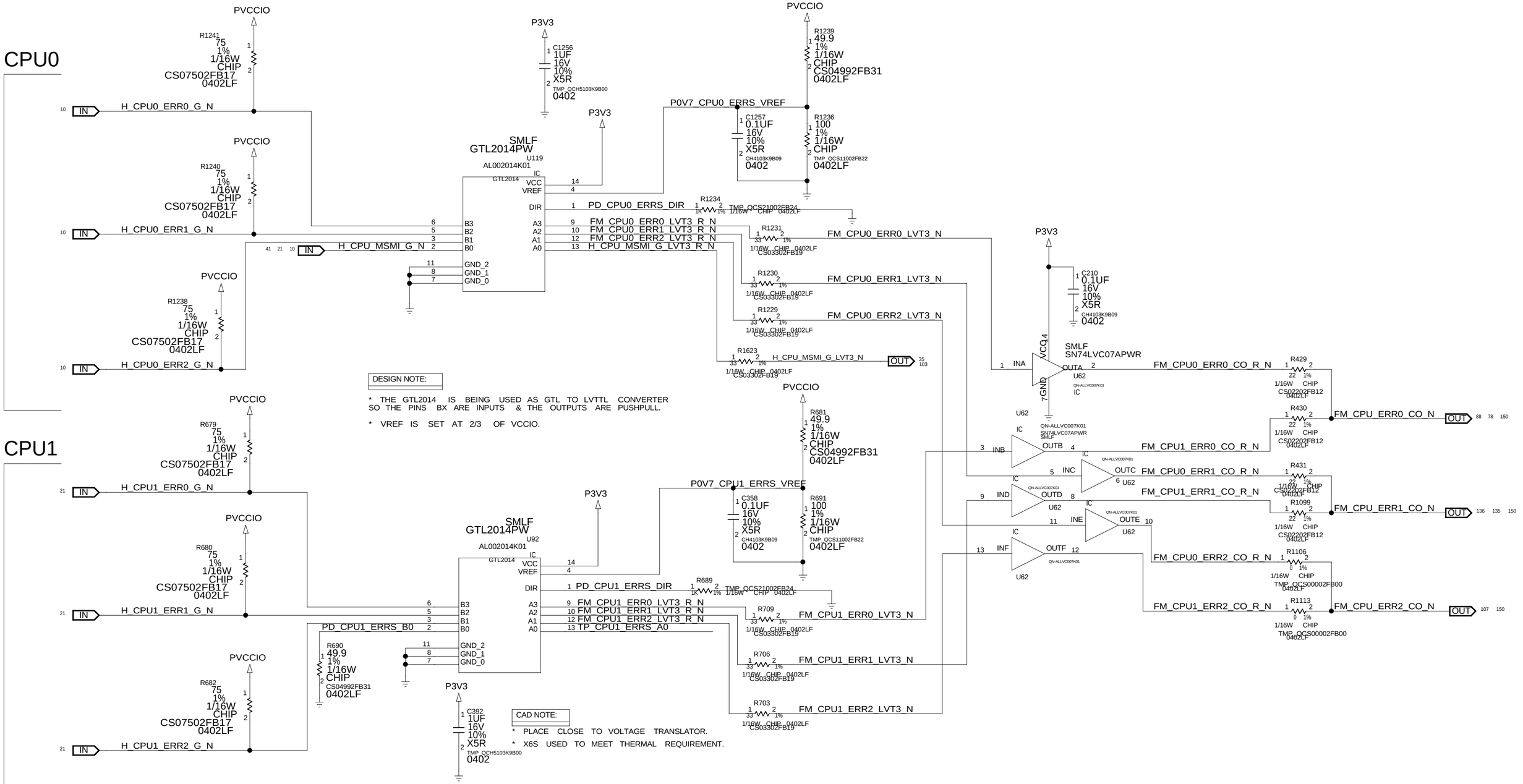




BIST:(INTERNAL PU)
DISABLE BIST FOR A STEPPING CPU
ENABLE BIST FOR B STEPPING (OR LATER) CPU



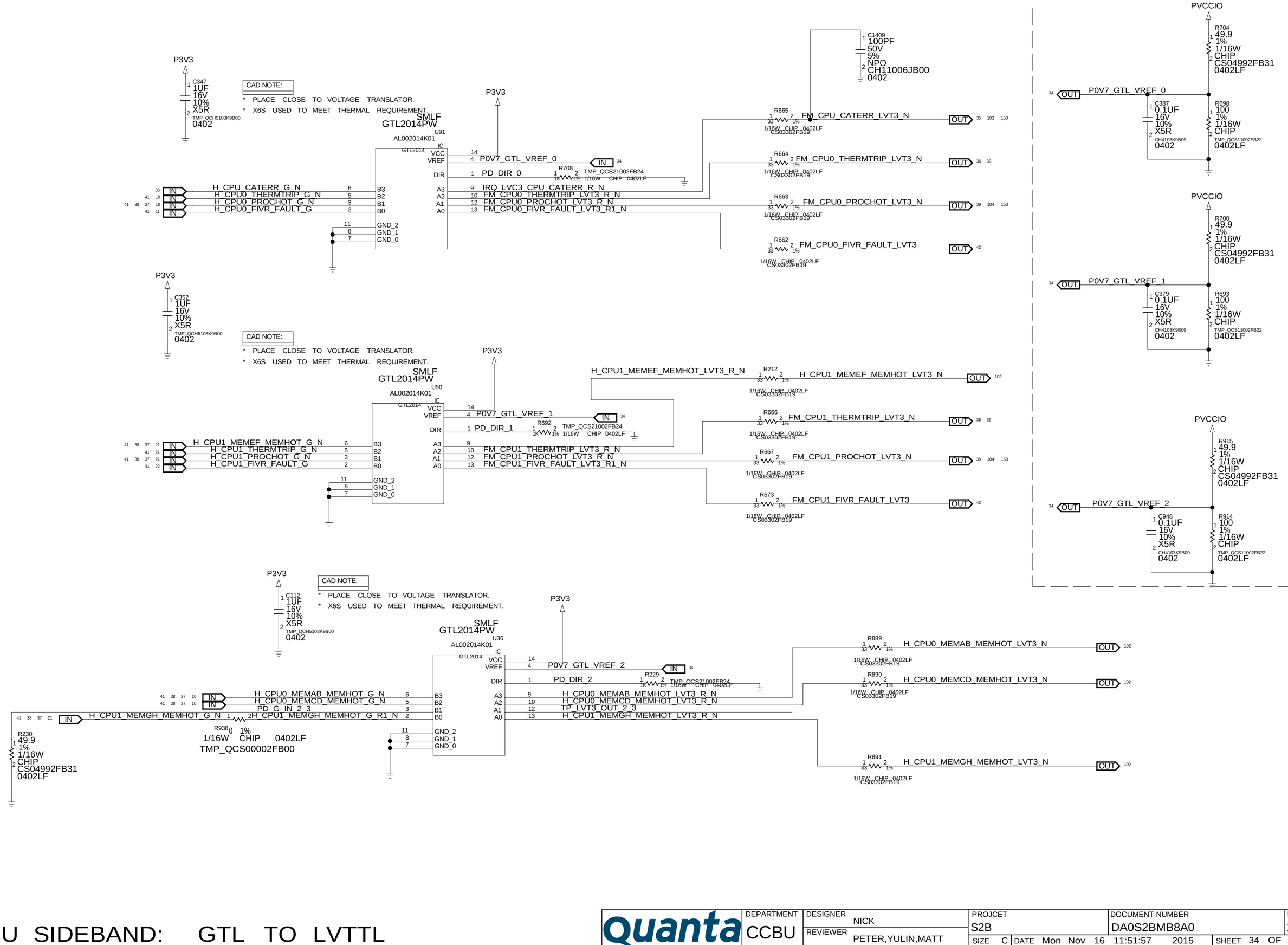

# CPU SIDEBAND: H/W STRAPS AND PECI

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:51:54 2015 | SHEET 32 OF 188 |




CPU SIDEBAND: ERROR CICUITS

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:51:55 2015 | SHEET 33 OF 188 |

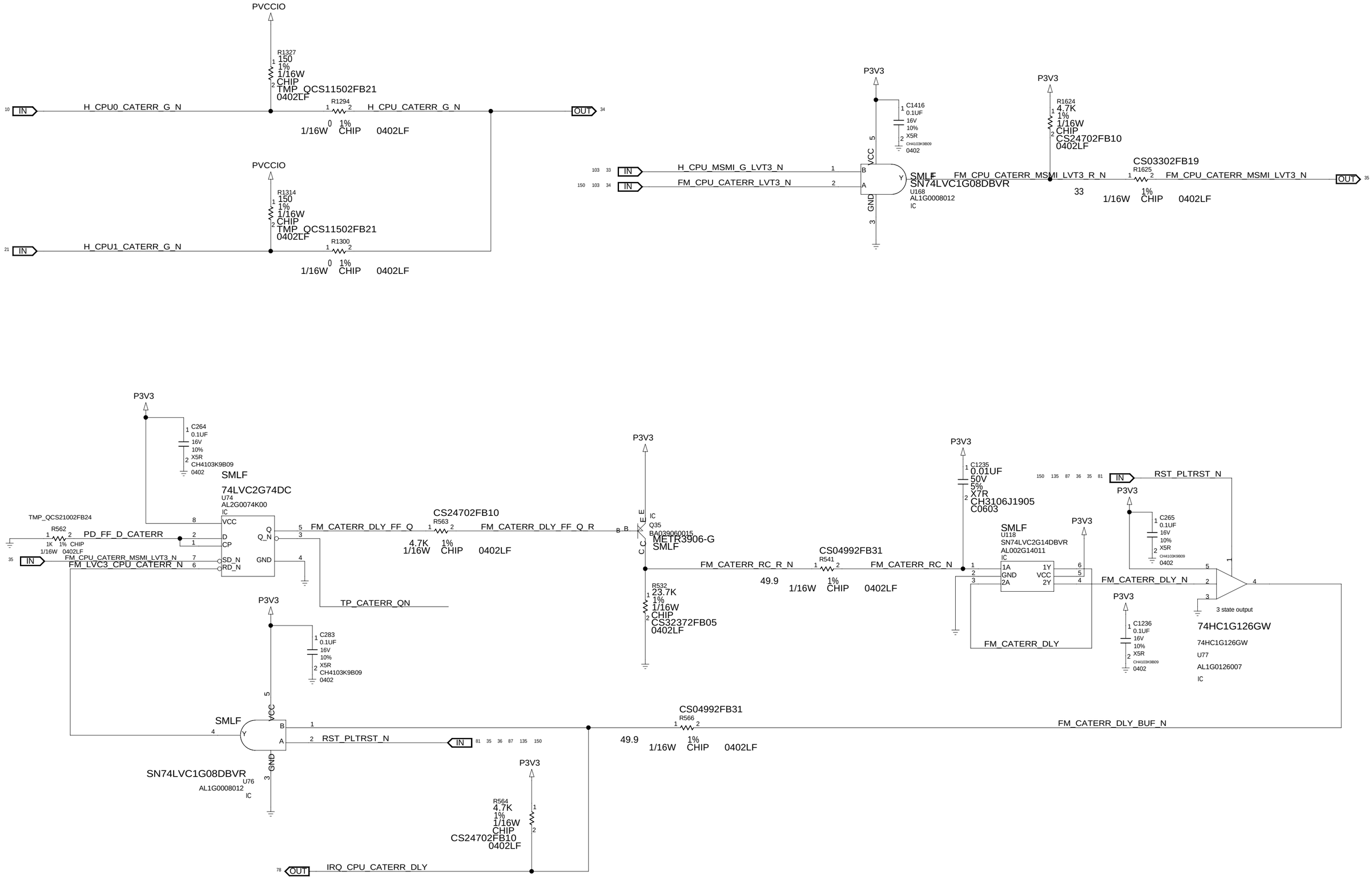



# CPU SIDEBAND: GTL TO LVTTL

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:51:57 2015 | SHEET: 34 OF 188 | |

NOTE:

PU IS 147 OHM IN CRB




# CPU SIDEBAND: CATERR

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:51:59 2015 | SHEET: 35 OF 188 | |

FROM VOLTAGE TRANSLATOR GTL TO LVT3

39 34 IN FM_CPU0_THERMTRIP_LVT3_N

40 135 IN PWRGD_CPU0_LVC3

87 36 150 35 135 81 IN RST_PLTRST_N

P3V3_AUX

C269 0.1UF 16V 10% X5R CH4103K9B09 0402

CS03302FB19

R1826 EMPTY 33

R1823 33

P3V3_AUX

C286 0.1UF 16V 10% X5R CH4103K9B09 0402

C287 1UF 16V 10% X5R TMP_QCH5103K9B00 0402

TP_BUF_01

PD_THERMTRIP_PORST

SMLF U80 TMP_QAL1G0017003 IC VCC NC A GND Y

FM_CPU_THERMTRIP_PORST

R578 49.9K 1% 1/16W CHIP TMP_QCS34992FB10 0402LF

P3V3_AUX

C284 0.1UF 16V 10% X5R CH4103K9B09 0402

C285 1UF 16V 10% X5R TMP_QCH5103K9B00 0402

TP_BUF_02

PD_PWRGD_PORST

SMLF U79 TMP_QAL1G0017003

FM_CPU0_PWRGD_PORST

R576 15K 1% 1/16W CHIP TMP_QCS31502FB24 0402LF

RST_CPU0_LVC3_R2_N

RST_CPU1_LVC3_R2_N

SMLF 74LVC32APW U78 ALLVC032K14 IC

VCC GND

1A 1B 1Y

2A 2B 2Y

3A 3B 3Y

4A 4B 4Y

FM_CPU0_THERMTRIP_LVC3_R_N

FM_CPU1_THERMTRIP_LVC3_R_N

R1733 56 1% 1/16W CHIP 0402LF

R1734 56 1% 1/16W CHIP 0402LF

OUT 42

P3V3_AUX

C1013 0.1UF 16V 10% X5R CH4103K9B09 0402

FM_CPU0_THERMTRIP_LVC3_N

D Q GND VCC LE OE# IC AL7SZ373006 U112 NC7SZ373P6X SMLF

FM_CPU0_THERMTRIP_LATCH_LVC3_N

OUT 104 150

PD_CPU0_THERMTRIP_LATCH_OE

R997 0 1% 1/16W CHIP TMP_QCS00002FB00 0402LF

FM_LVC3_CPU0_PWRGD_R

R575 56 1% 1/16W CHIP 0402LF TMP_QCS05602FB15

FM_LVC3_CPU0_PWRGD

OUT 42

FM_LVC3_CPU1_PWRGD_R

R1220 56 1% 1/16W CHIP 0402LF TMP_QCS05602FB15

FM_LVC3_CPU1_PWRGD

OUT 42

P3V3_AUX

C1234 0.1UF 16V 10% X5R CH4103K9B09 0402

FM_CPU1_THERMTRIP_LVC3_N

D Q GND VCC LE OE# IC AL7SZ373006 U117 NC7SZ373P6X SMLF

FM_CPU1_THERMTRIP_LATCH_LVC3_N

OUT 104 150

PD_CPU1_THERMTRIP_LATCH_OE

R1219 0 1% 1/16W CHIP TMP_QCS00002FB00 0402LF

OUT 42

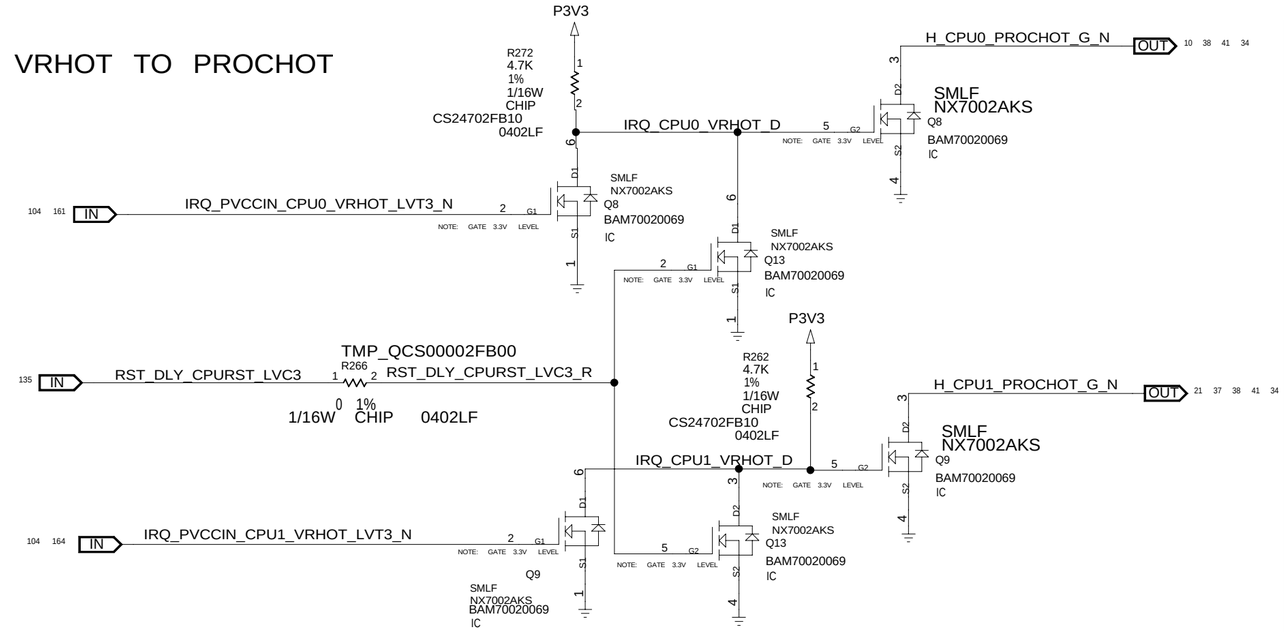
FROM VOLTAGE TRANSLATOR GTL TO LVT3

39 34 IN FM_CPU1_THERMTRIP_LVT3_N

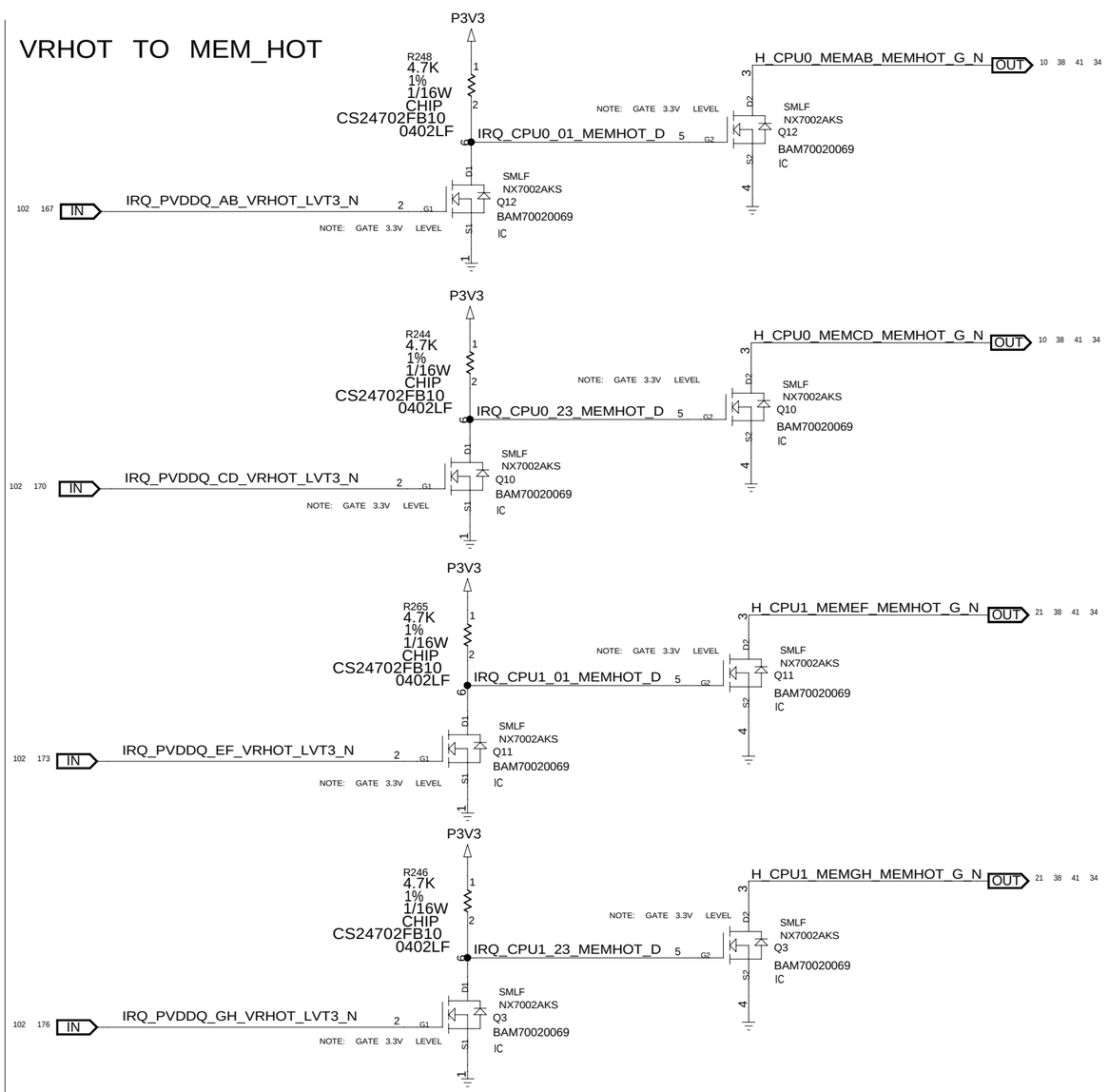
# CPU SIDEBAND: THERMALTRIP

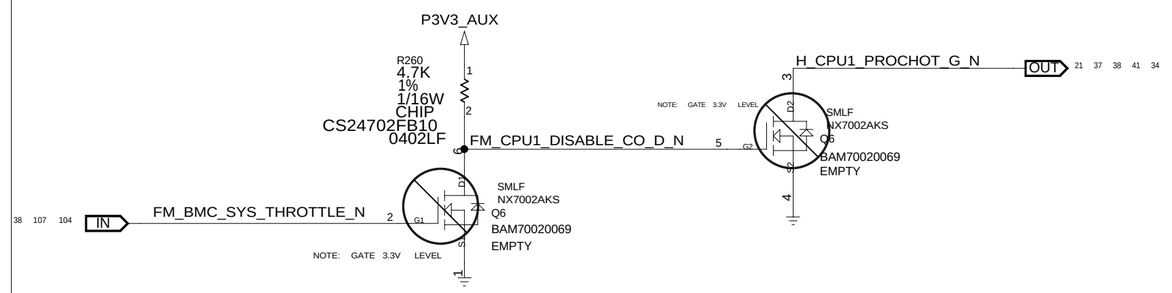
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | | |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:52:00 2015 | SHEET 36 OF 188 | | |

## VRHOT TO PROCHOT



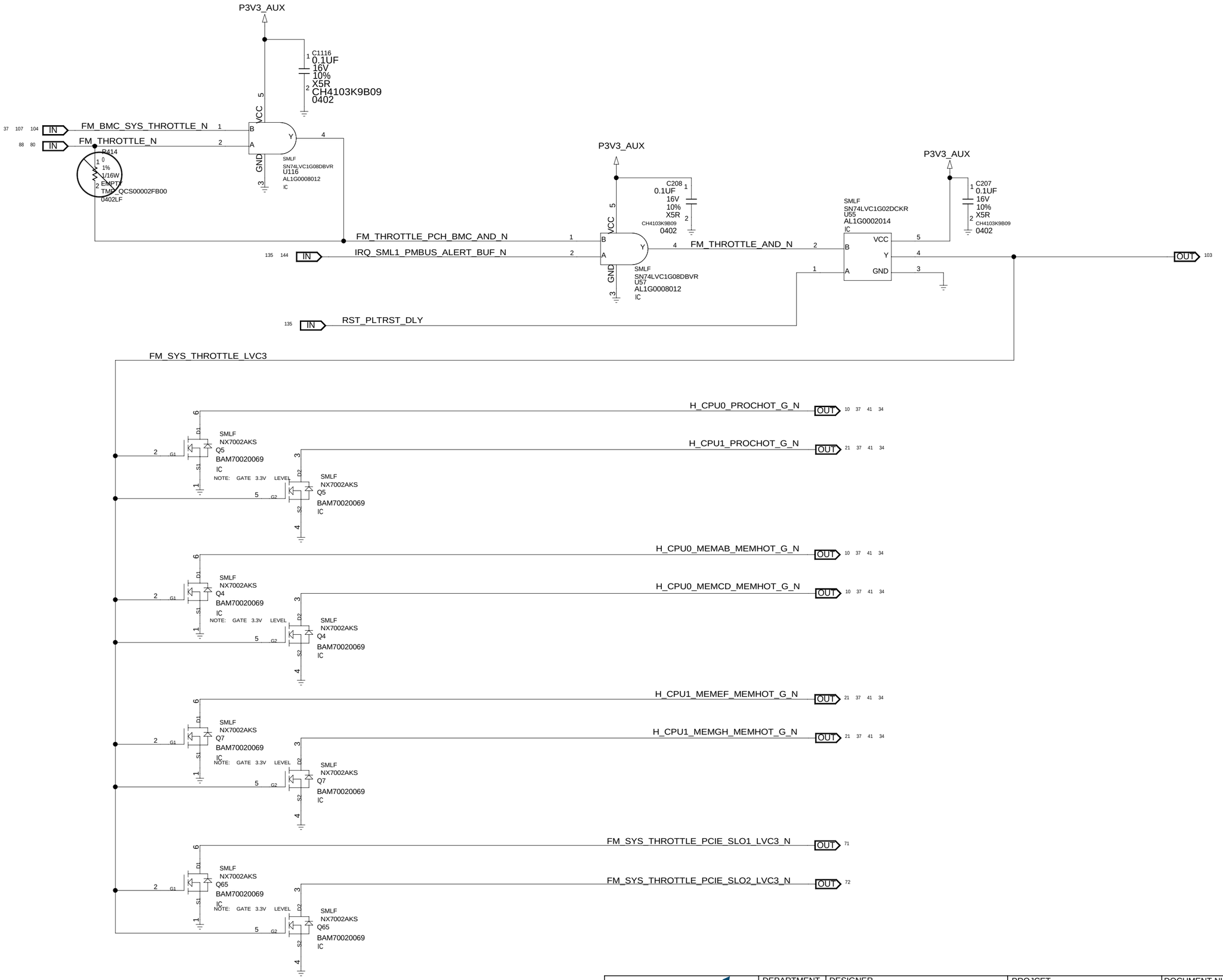

## VRHOT TO MEM_HOT



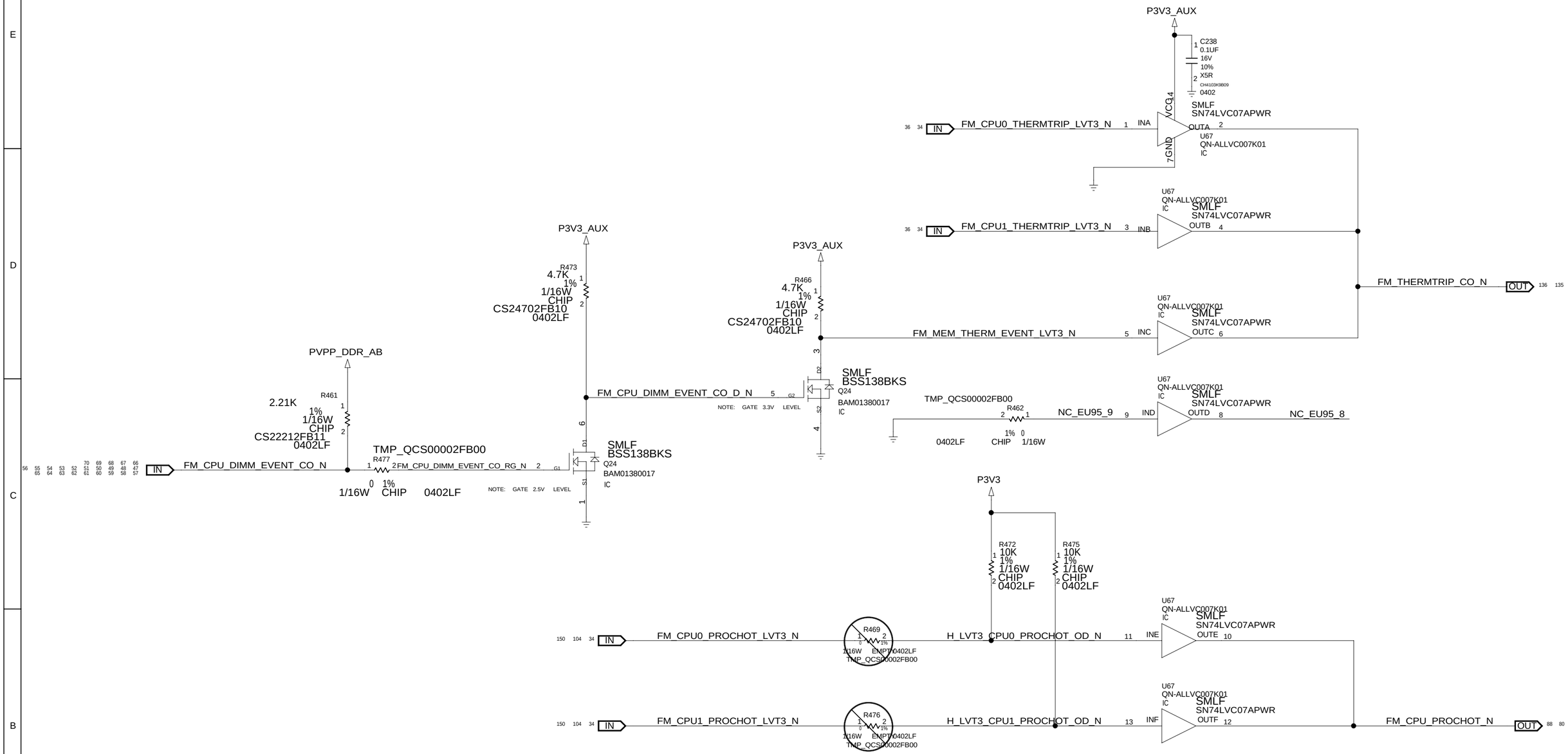

# CPU SIDEBAND: PROCHOT & MEMHOT

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:01 2015 | SHEET: 37 OF 188 |



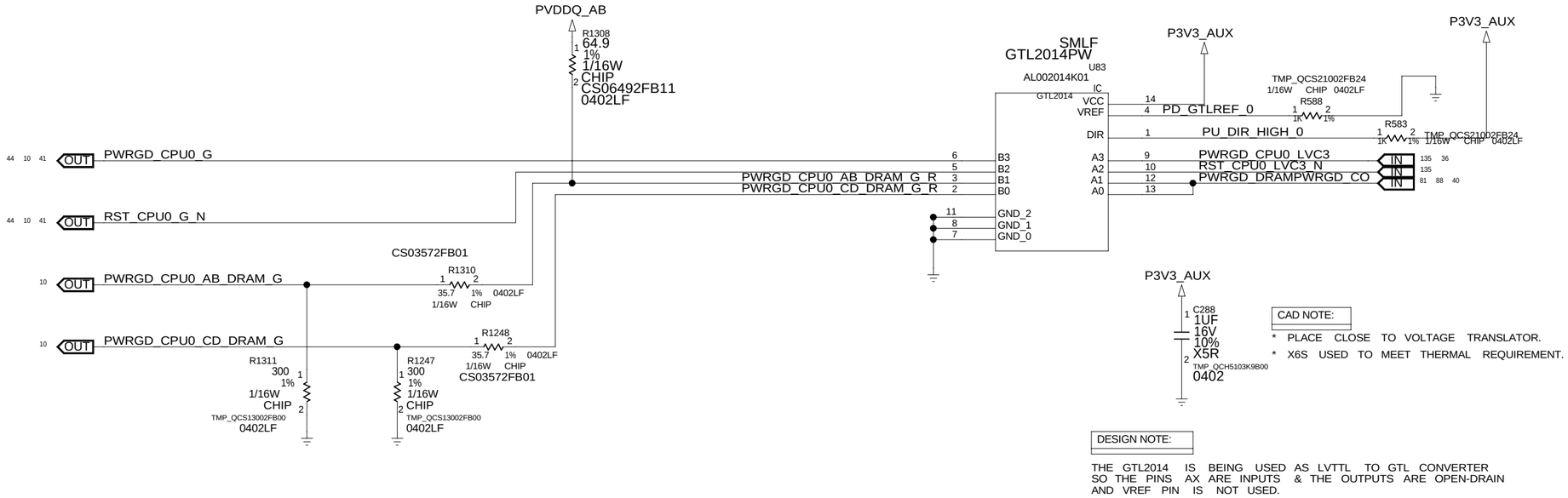

# CPU SIDEBAND:THROTTLE

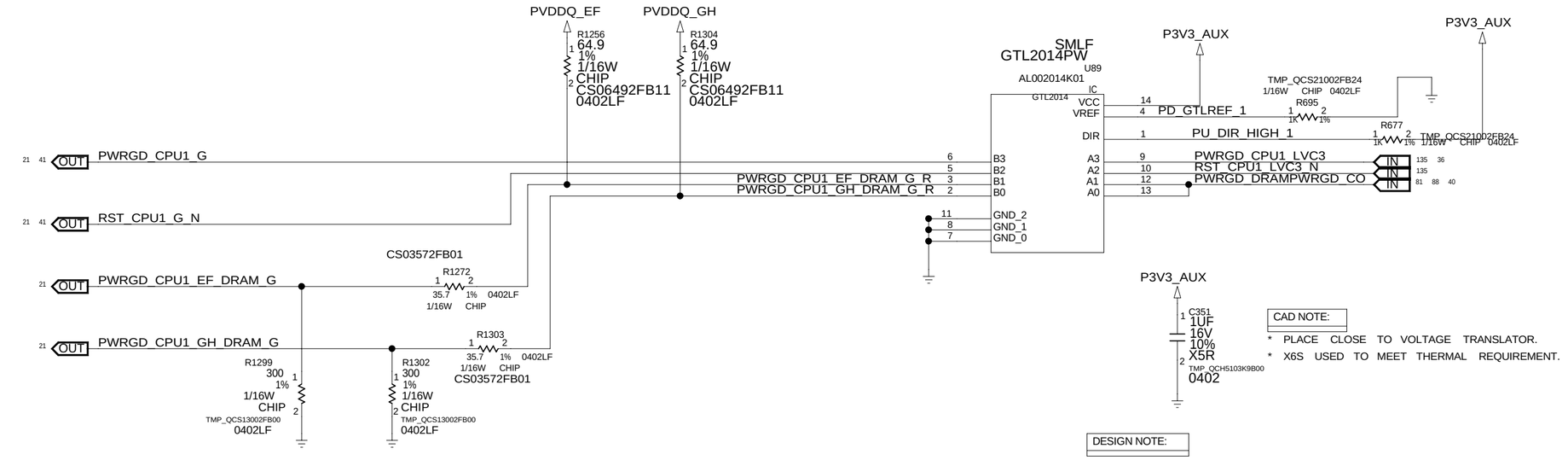
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:02 2015 | SHEET: 38 OF 188 |




# CPU SIDEBAND: DIMM EVENT

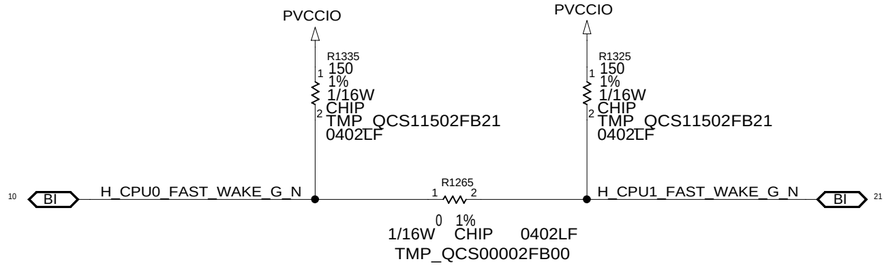
| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:03 2015 | SHEET: 39 OF 188 | |




# CPU SIDEBAND: RESETS & PWRGOOD

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:04 2015 | SHEET: 40 OF 188 |



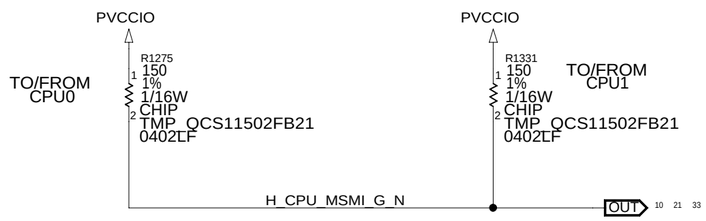

# PM_FAST_WAKE_N




# CPU PWRGOOD



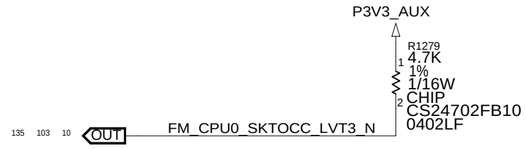

# CPU RESET_N

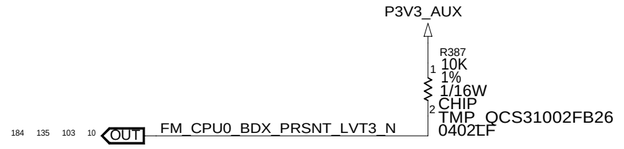


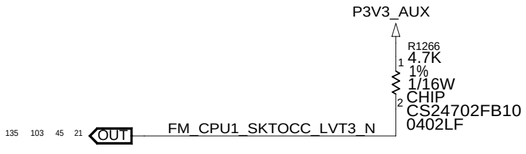


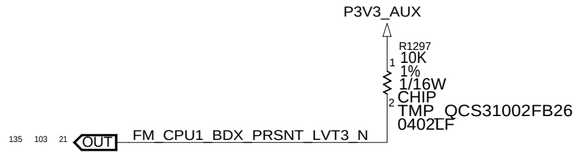


# FIVR

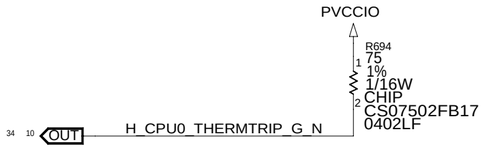


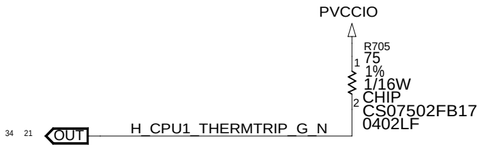



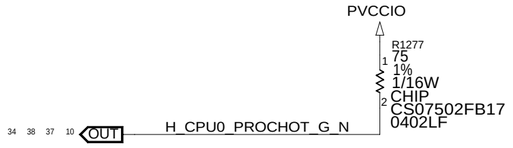



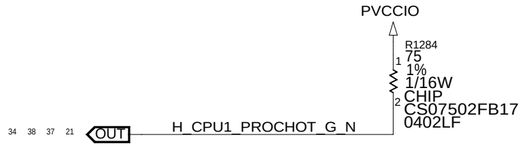

# PROC_ID AND SKTOCC_N



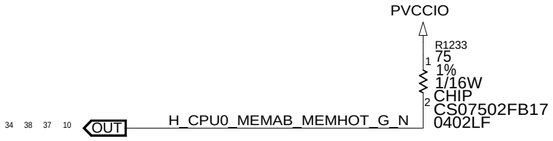



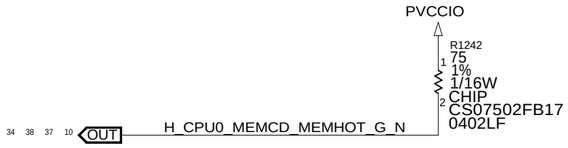

# PU OF THERMTRIP

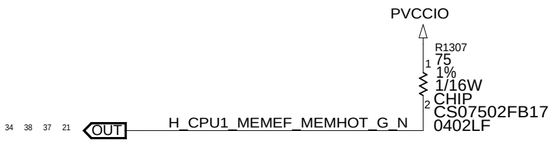


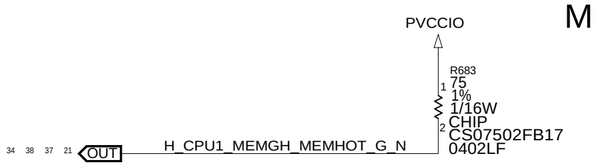




# PU OF PROCHOT

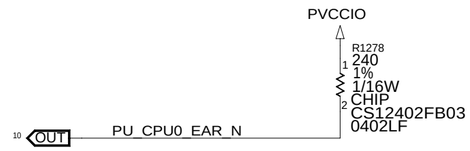


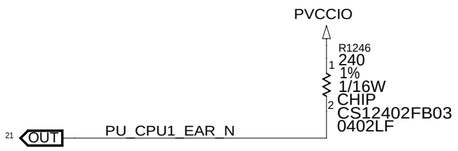




# PU OF MEM HOT

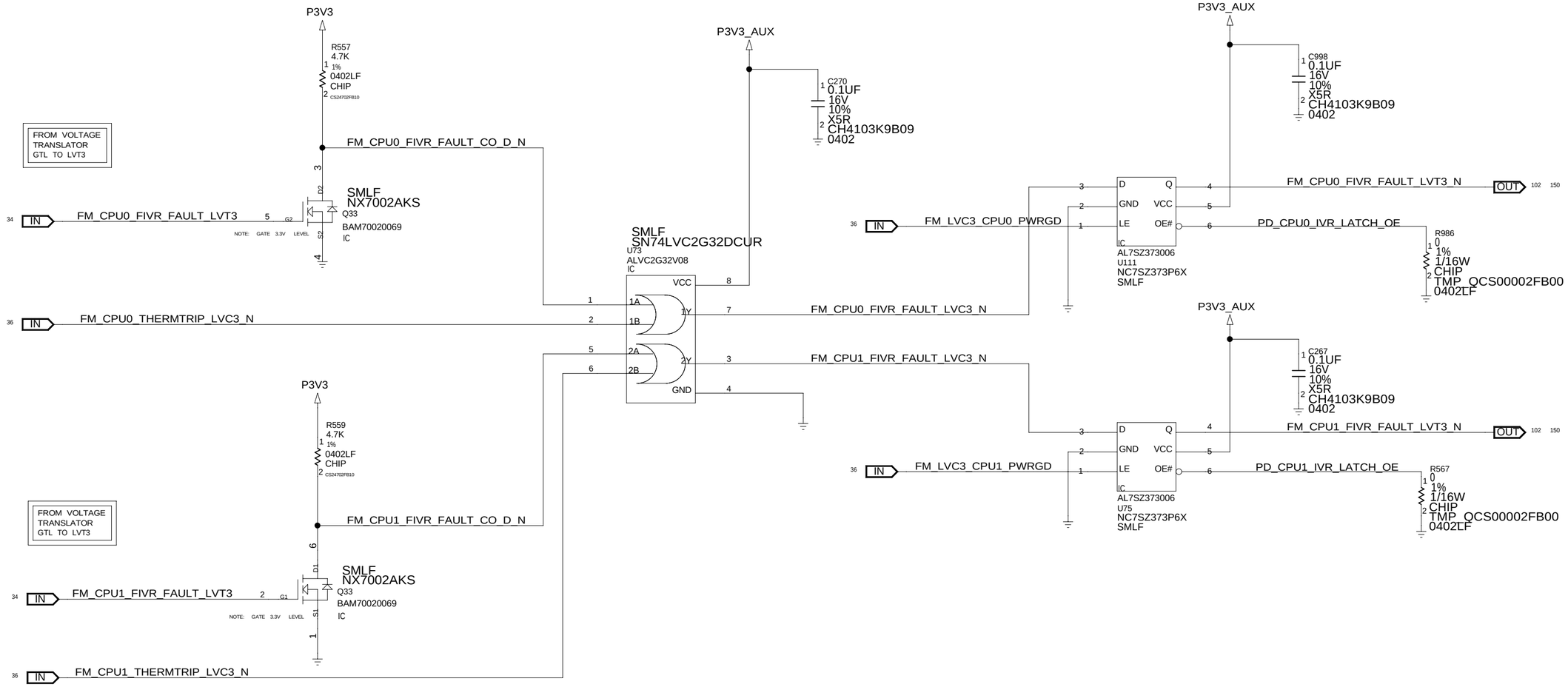



# CPU EAR

# CPU SIDEBAND: PUS AND PDS

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C DATE: Mon Nov 16 11:52:05 2015 | SHEET: 41 OF 188 | |




# CPU SIDEBAND: FIVR FAULT

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:52:07 2015 | SHEET 42 OF 188 |

PVCCIN_CPU0

C464 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C480 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C438 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C426 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C505 47UF 4V 20% X6S CH647KMEA00 0805

PVCCIN_CPU0

C465 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C500 47UF 4V 20% X6S CH647KMEA00 0805
C502 47UF 4V 20% X6S CH647KMEA00 0805
C408 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C467 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVCCIN_CPU0

C499 47UF 4V 20% X6S CH647KMEA00 0805
C418 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C439 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C552 47UF 4V 20% X6S CH647KMEA00 0805
C481 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVCCIN_CPU0

C506 47UF 4V 20% X6S CH647KMEA00 0805
C494 47UF 4V 20% X6S CH647KMEA00 0805
C429 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C445 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C423 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVCCIN_CPU0

C427 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C512 47UF 4V 20% X6S CH647KMEA00 0805
C530 47UF 4V 20% X6S CH647KMEA00 0805
C419 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

## SOCKET 0 CAVITY CAPS, PLACE ON TOP SIDE

PVCCIN_CPU0

C1291 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1267 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1273 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1261 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1303 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVCCIN_CPU0

C1308 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1314 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1284 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1278 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1302 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVCCIN_CPU0

C1309 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1279 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1285 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1315 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1297 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVCCIN_CPU0

C1260 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1272 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1296 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1266 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1290 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVCCIN_CPU0

C1294 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1300 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1312 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1264 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1318 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVCCIN_CPU0

C1276 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1288 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1282 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1270 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1306 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

## SOCKET 0 CAVITY CAPS, PLACE ON BOTTOM SIDE

PVCCIN_CPU1

C436 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C425 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1319 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C462 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C497 47UF 4V 20% X6S CH647KMEA00 0805

PVCCIN_CPU1

C498 47UF 4V 20% X6S CH647KMEA00 0805
C528 47UF 4V 20% X6S CH647KMEA00 0805
C550 47UF 4V 20% X6S CH647KMEA00 0805
C479 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C478 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVCCIN_CPU1

C444 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C424 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C417 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1313 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1316 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVCCIN_CPU1

C503 47UF 4V 20% X6S CH647KMEA00 0805
C493 47UF 4V 20% X6S CH647KMEA00 0805
C504 47UF 4V 20% X6S CH647KMEA00 0805
C501 47UF 4V 20% X6S CH647KMEA00 0805
C510 47UF 4V 20% X6S CH647KMEA00 0805

PVCCIN_CPU1

C1277 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C422 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C407 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C463 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

## SOCKET 1 CAVITY CAPS, PLACE ON TOP SIDE

PVCCIN_CPU1

C1317 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1283 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1289 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1263 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1274 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVCCIN_CPU1

C1280 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1286 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1310 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1311 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1299 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVCCIN_CPU1

C1262 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C466 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1265 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1295 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1301 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVCCIN_CPU1

C1307 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1268 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1304 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1292 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1298 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVCCIN_CPU1

C1305 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1287 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1293 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1271 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C428 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVCCIN_CPU1

C1269 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1281 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C1275 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C437 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C416 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

## SOCKET 1 CAVITY CAPS, PLACE ON BOTTOM SIDE

PVDDQ_AB

C508 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C514 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C536 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVDDQ_CD

C511 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C529 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C551 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

PVDDQ_EF

C535 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C513 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C507 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

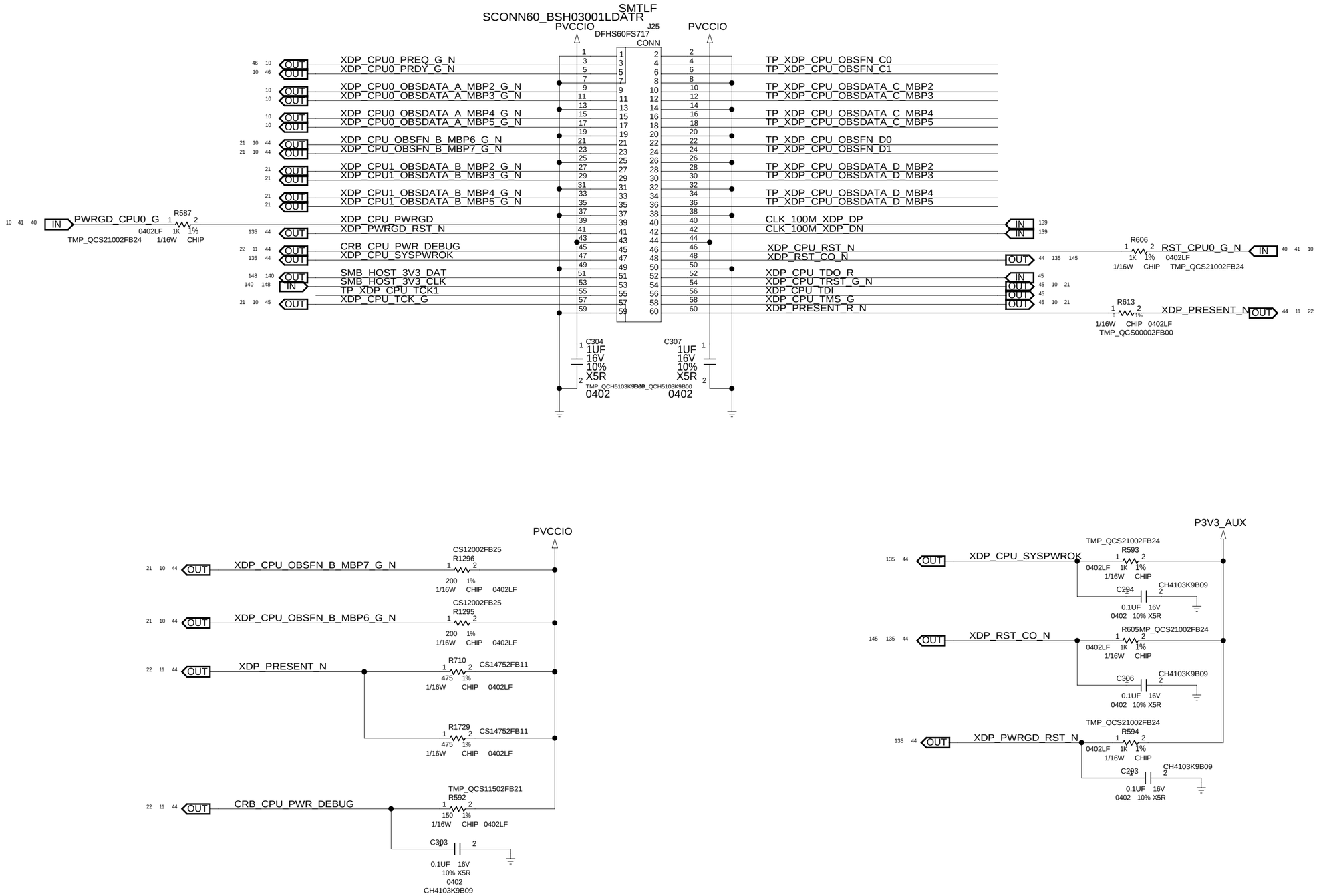
PVDDQ_GH

C549 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C509 22UF 4V 20% X6S TMP_QCH622KMEA01 0805
C527 22UF 4V 20% X6S TMP_QCH622KMEA01 0805

# CPU DECOUPLING CAPS

| | | | | |
|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C DATE: Mon Nov 16 11:52:08 2015 | SHEET 43 OF 188 |

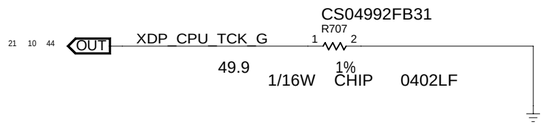
REV 1



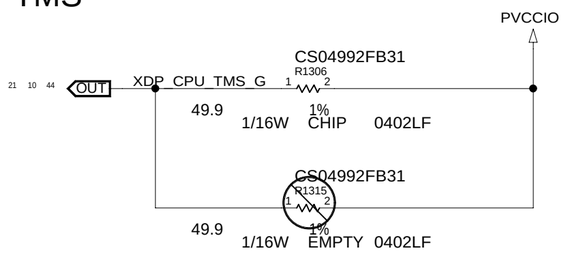

# CPU XDP

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:10 2015 | SHEET: 44 OF 188 | |

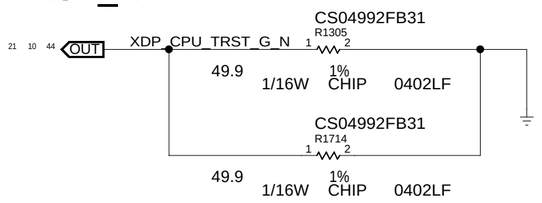
## TCK



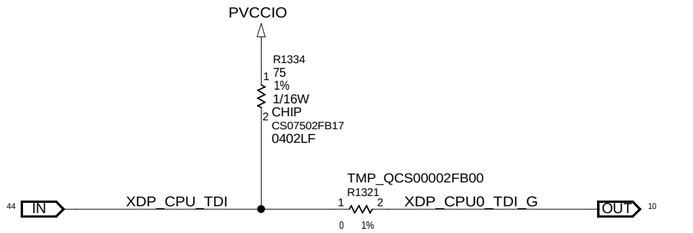

## TMS

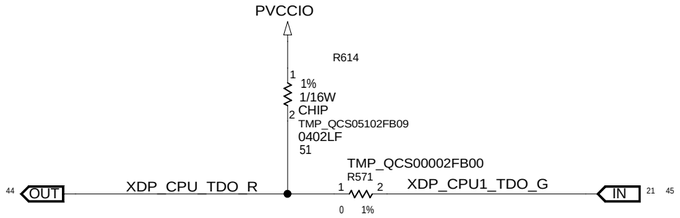


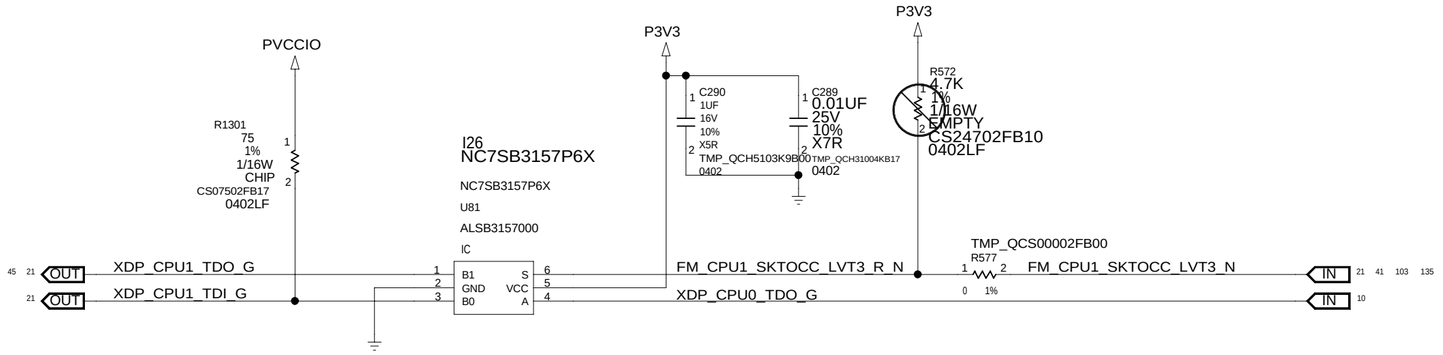

## TRST_N

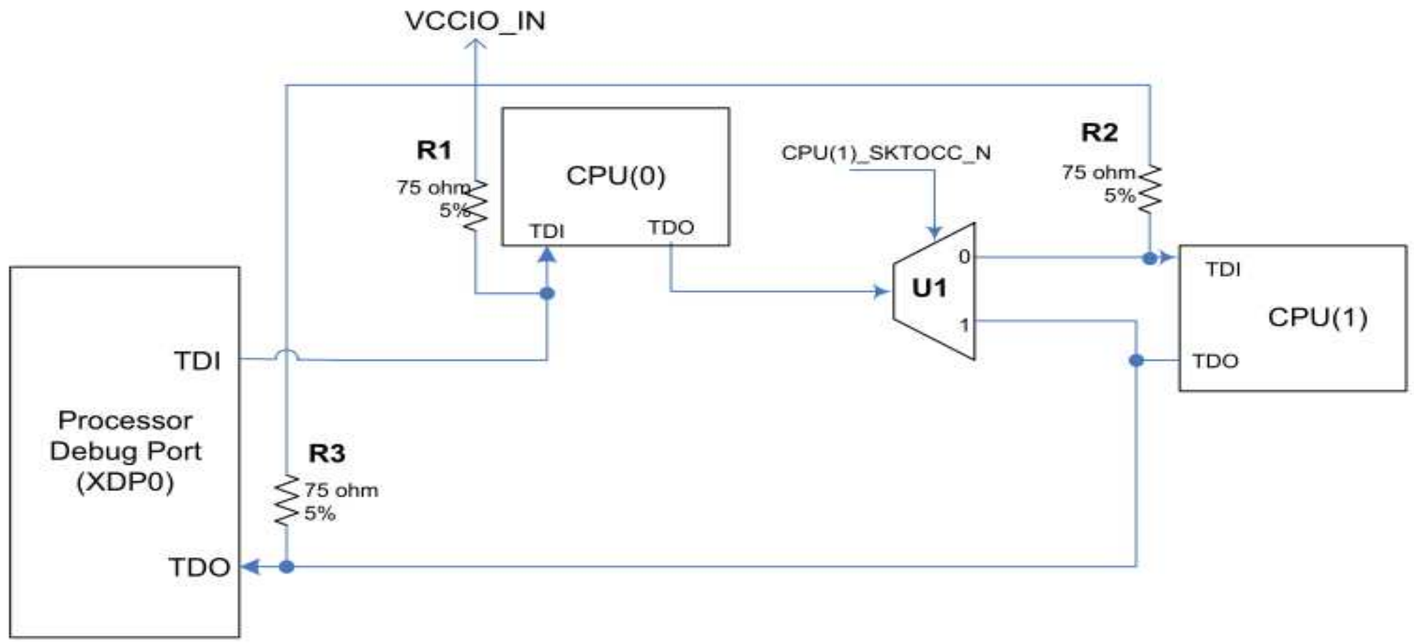



## TDI -- TDO



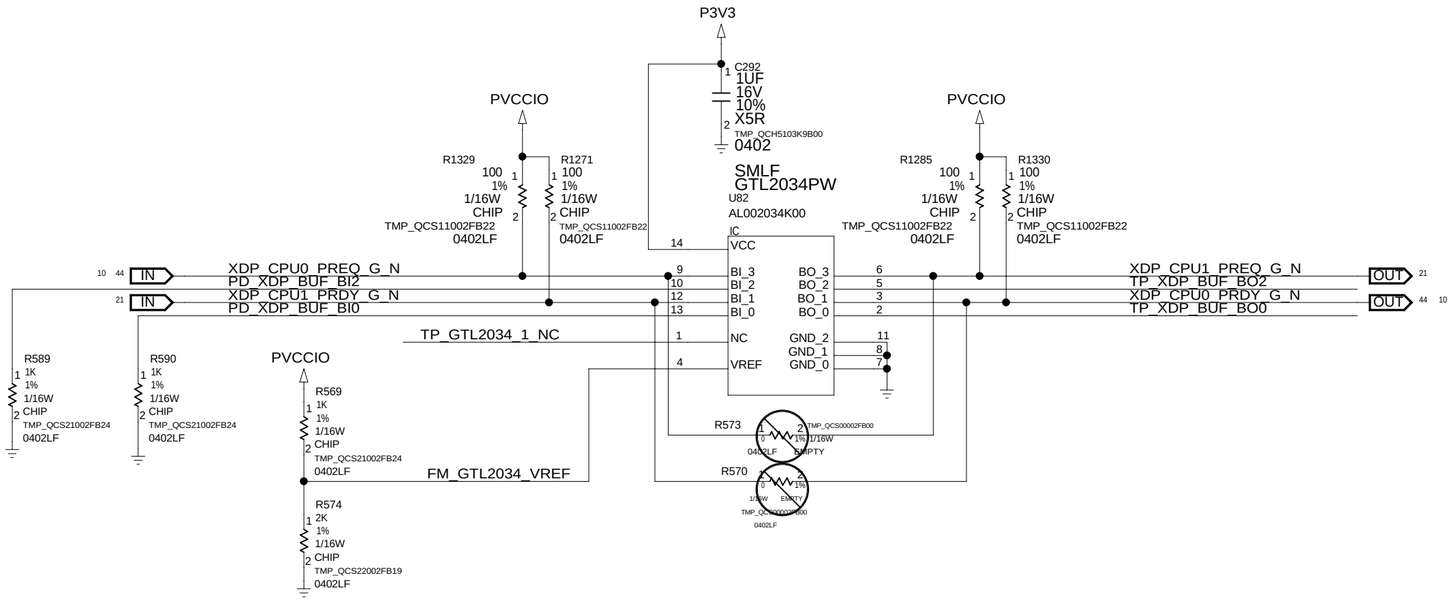



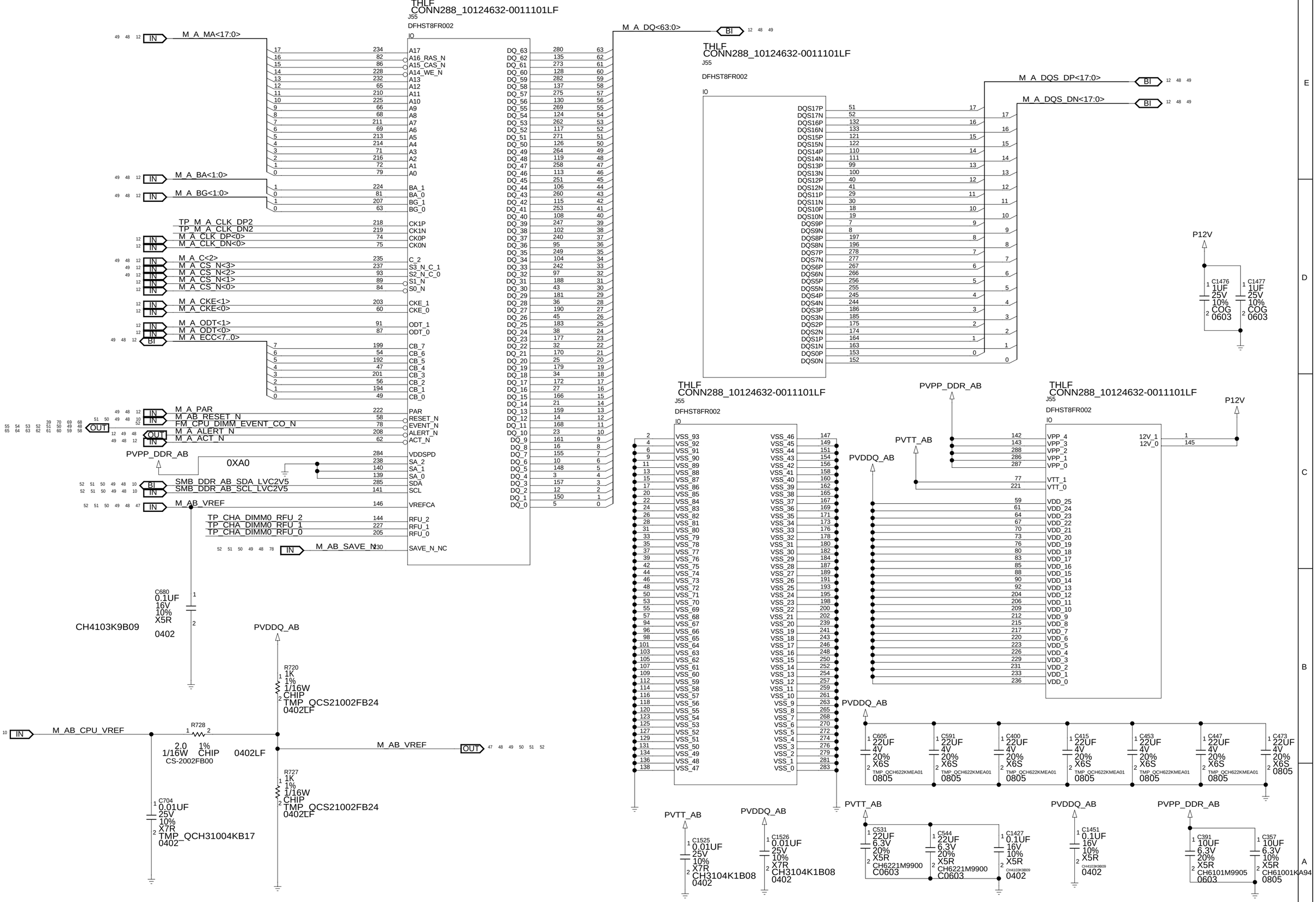

CPU JTAG 1 OF 2

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:52:11 2015 | SHEET 45 OF 188 |



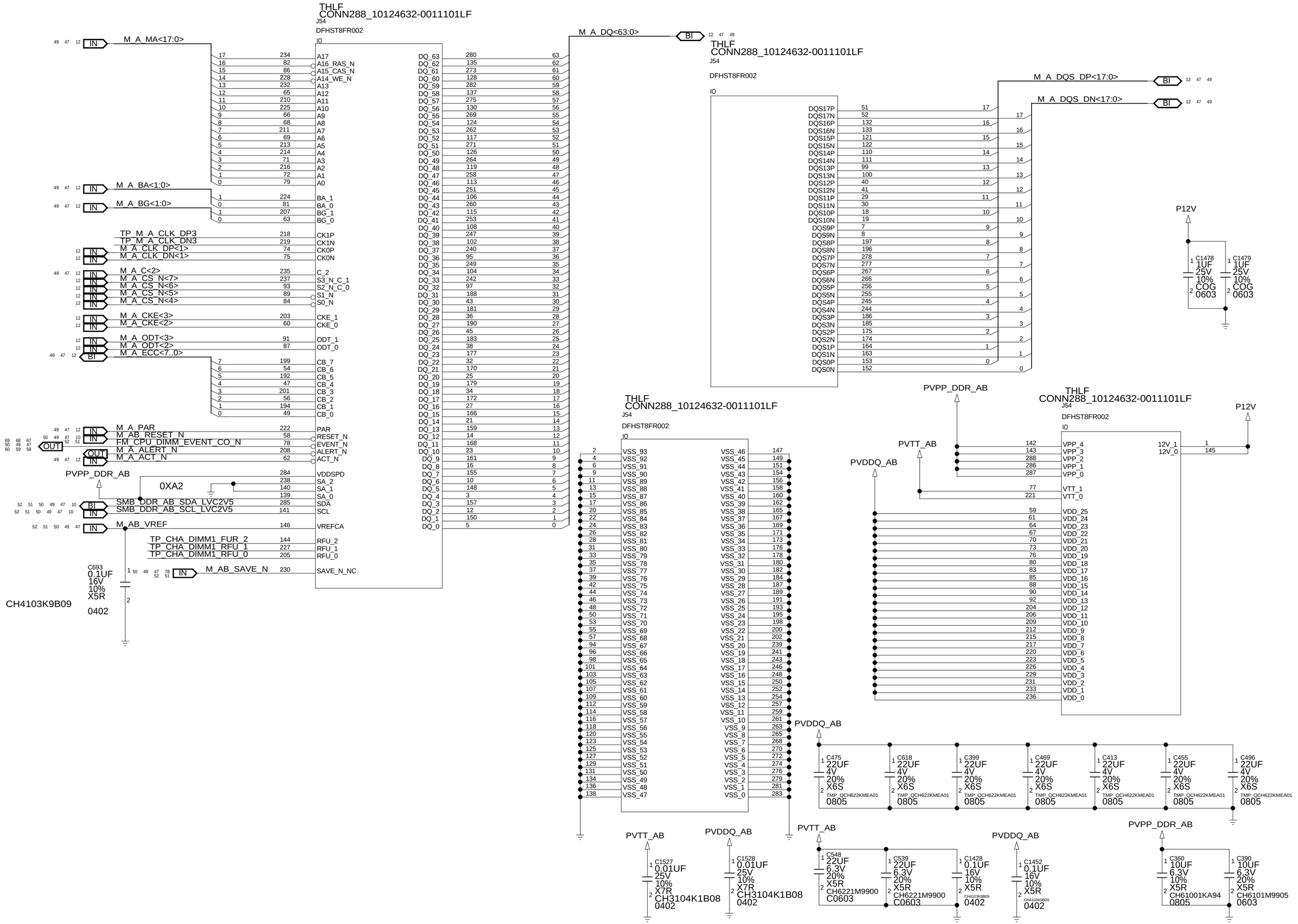

# CPU JTAG 2 OF 2

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:52:12 2015 | SHEET 46 OF 188 | |



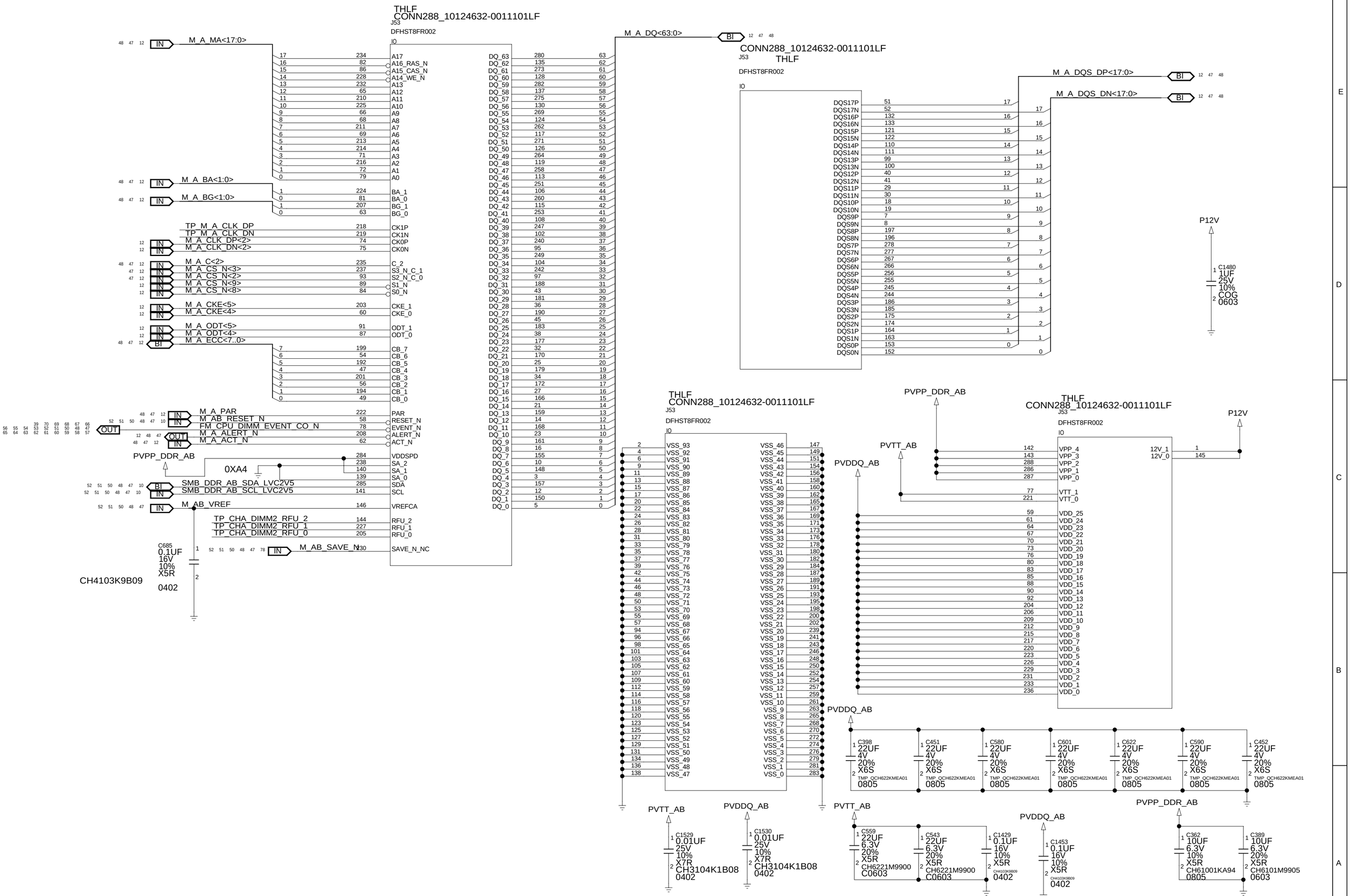

# DDR4 CHANNEL A DIMM1 (BLUE)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:14 2015 | SHEET: 47 OF 188 |



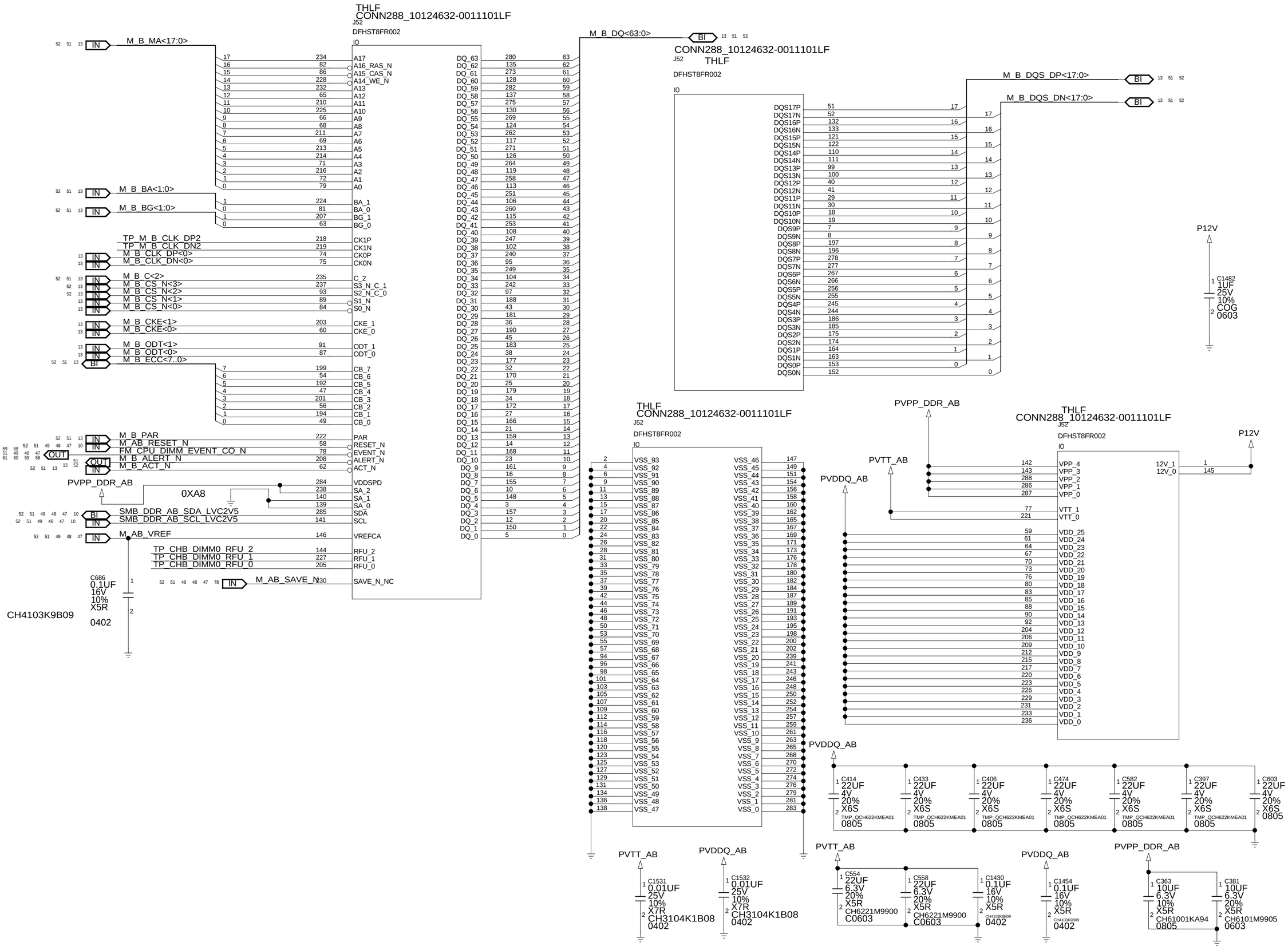

# DDR4 CHANNEL A DIMM2 (BLACK)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:18 2015 | SHEET: 48 OF 188 |




# DDR4 CHANNEL A DIMM3 (BLACK)

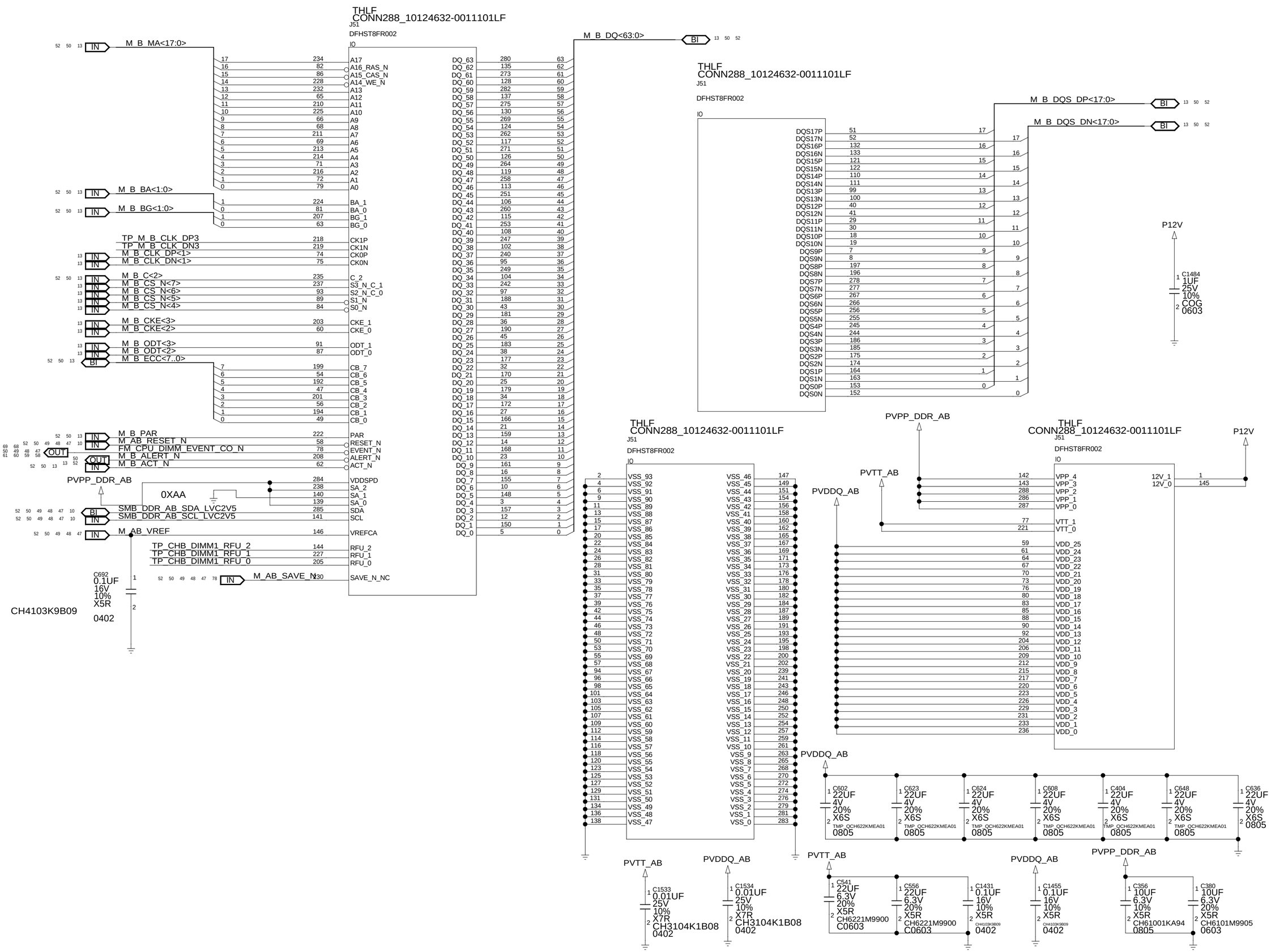
| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:22 2015 | SHEET: 49 OF 188 | |




# DDR4 CHANNEL B DIMM1 (BLUE)

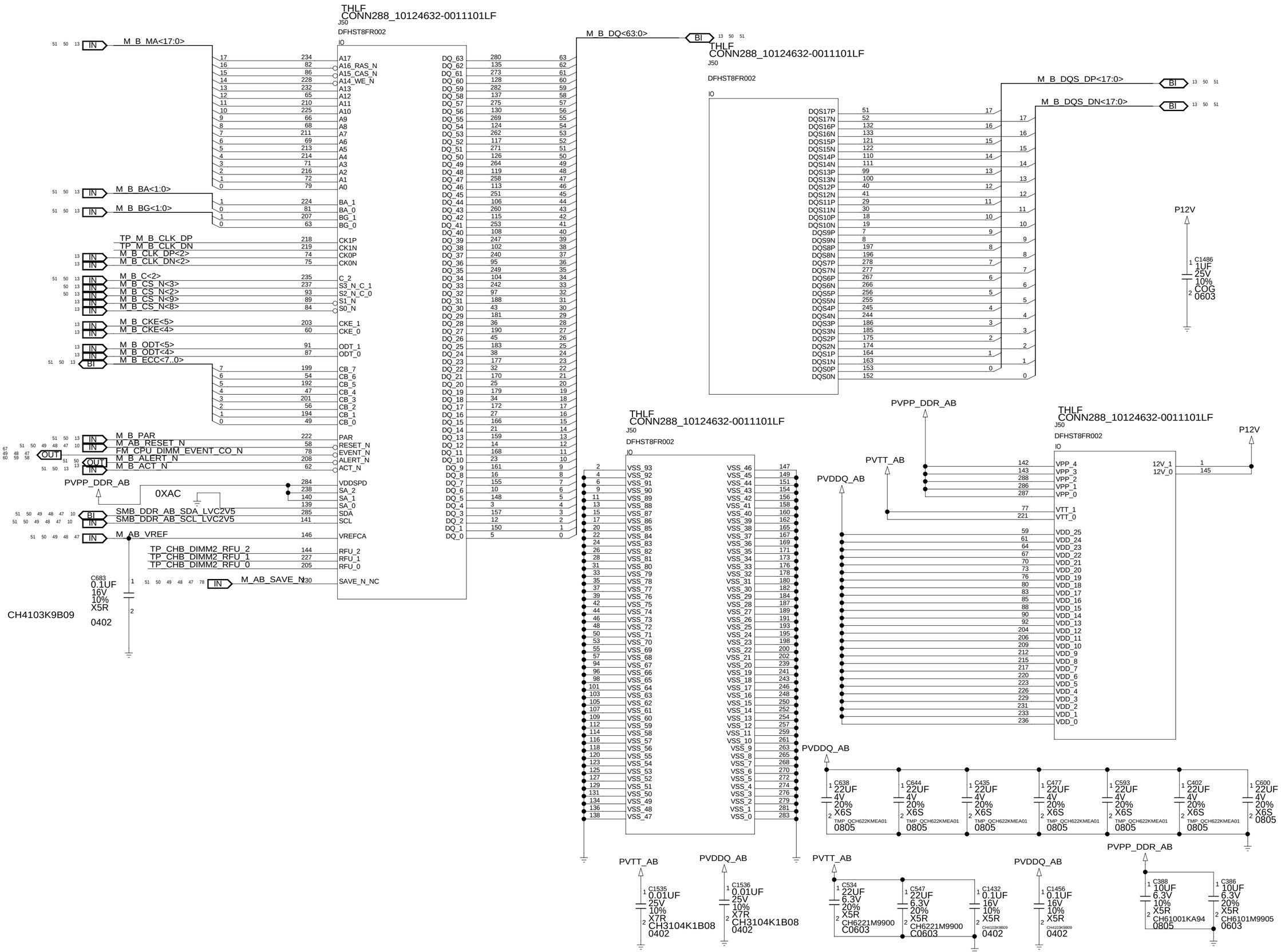
| | | | | |
|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C DATE: Mon Nov 16 11:52:24 2015 | SHEET 50 OF 188 |

REV: 1



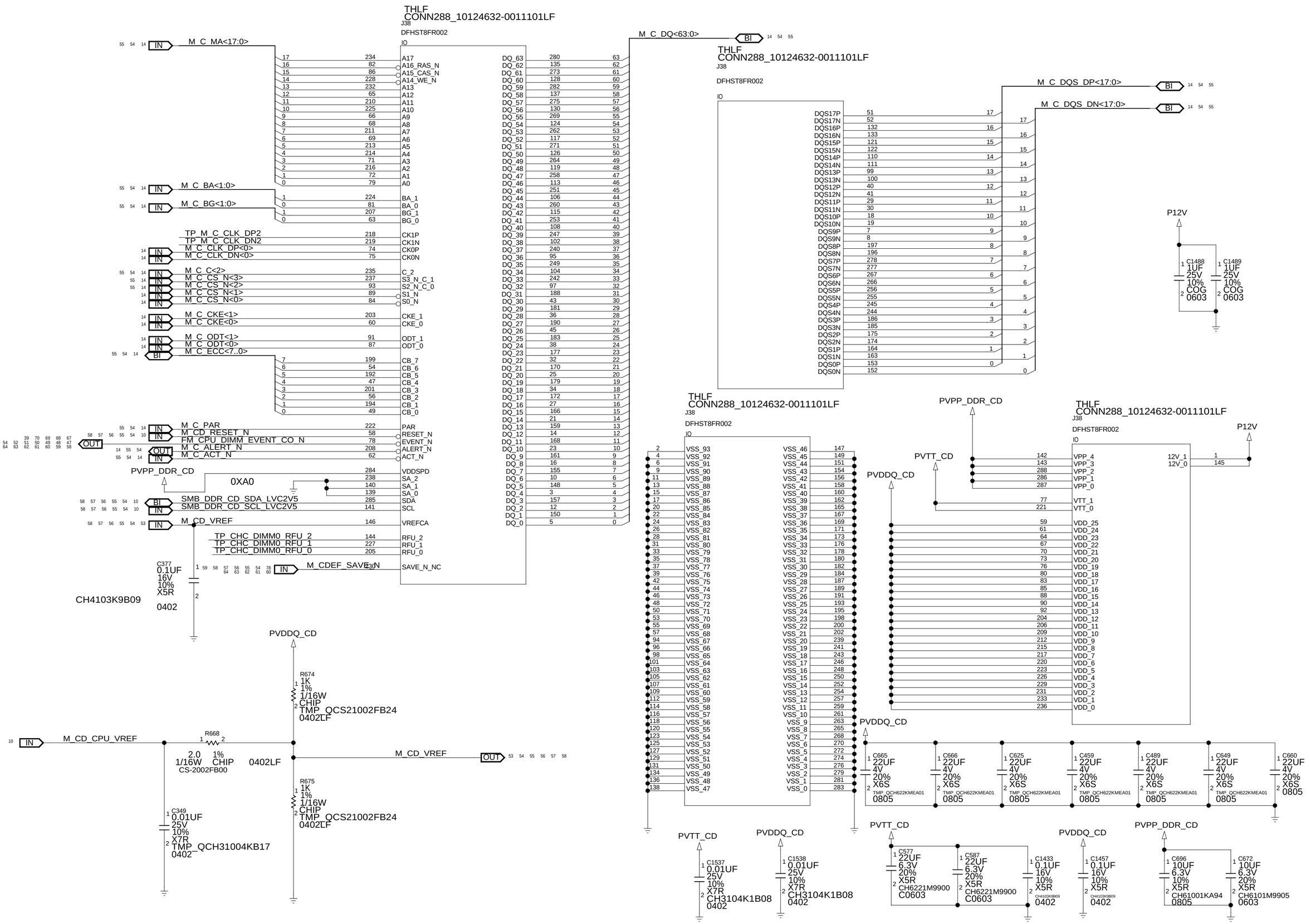

# DDR4 CHANNEL B DIMM2 (BLACK)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:26 2015 | SHEET: 51 OF 188 |



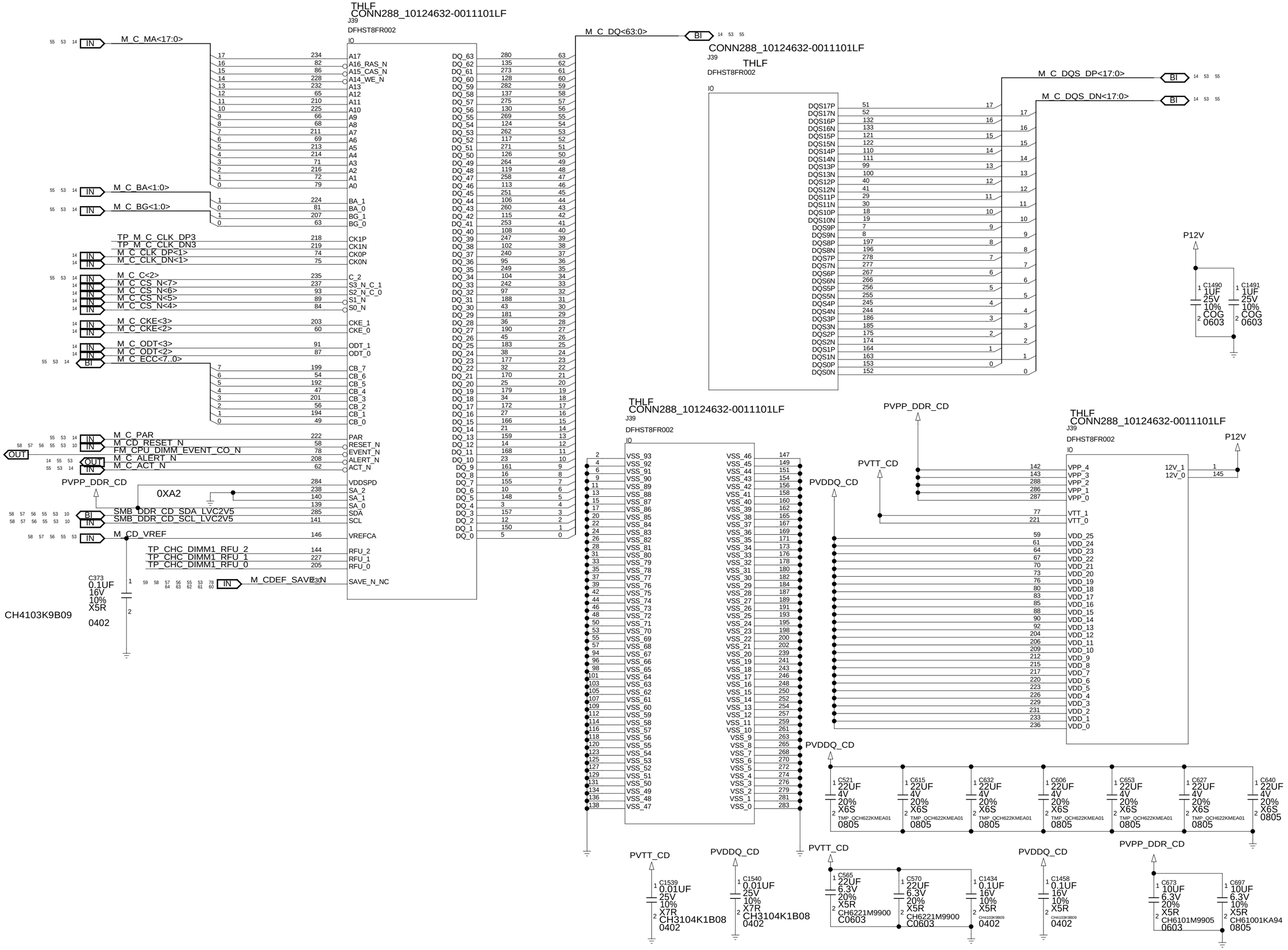

# DDR4 CHANNEL B DIMM3 (BLACK)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:29 2015 | SHEET: 52 OF 188 |



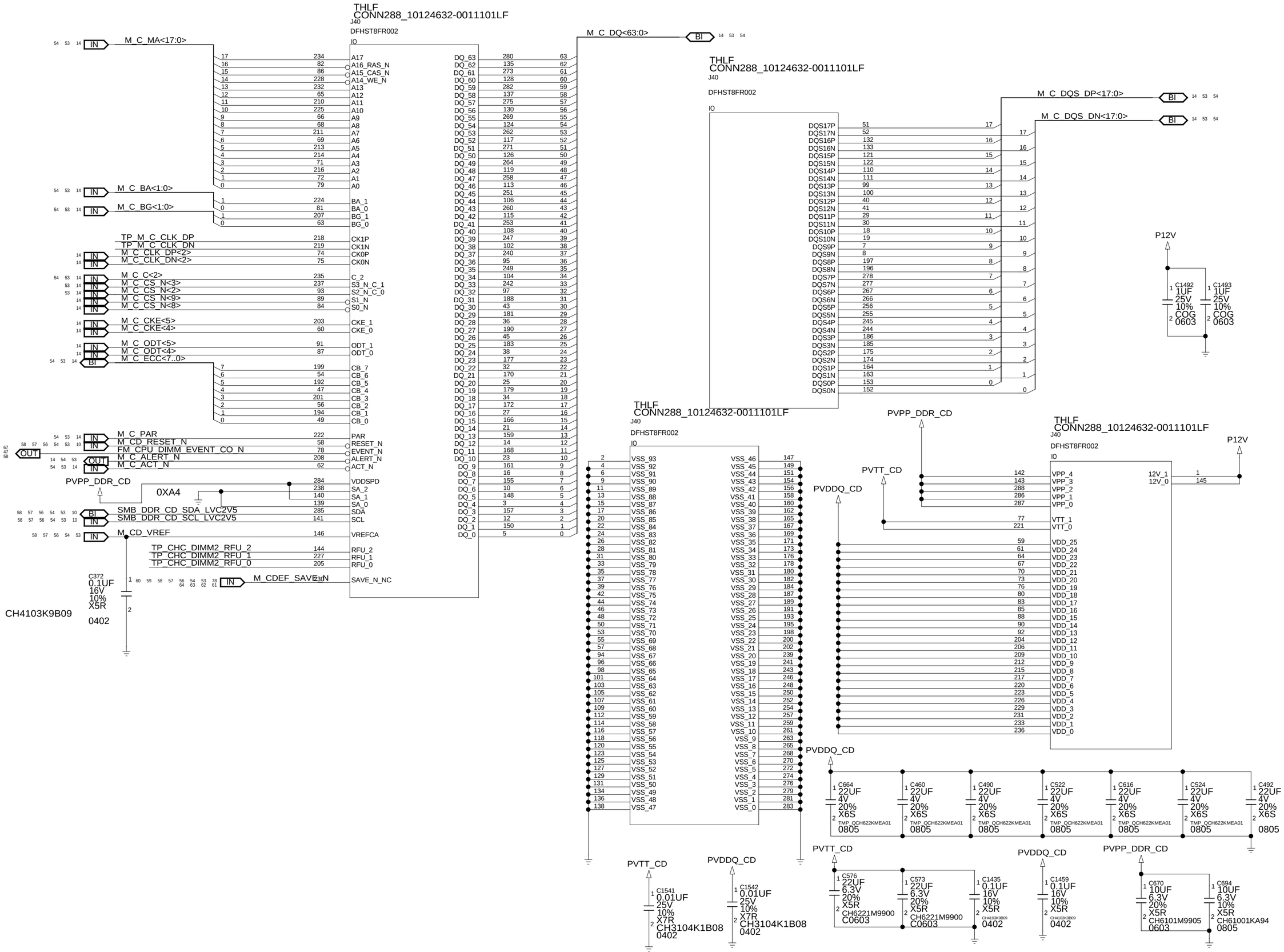

# DDR4 CHANNEL C DIMM1 (BLUE)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:31 2015 | SHEET: 53 OF 188 |



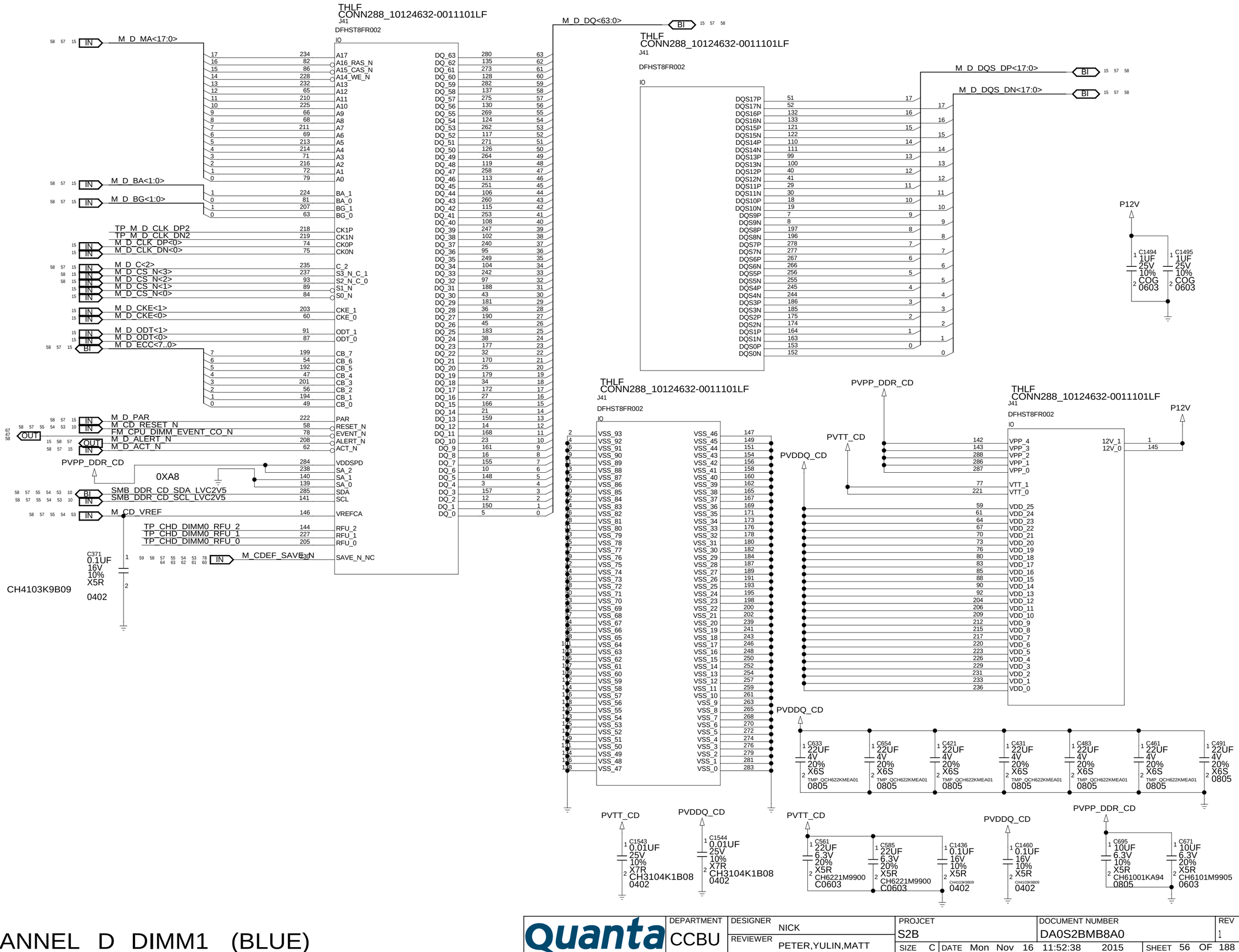

# DDR4 CHANNEL C DIMM2 (BLACK)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:33 2015 | SHEET: 54 OF 188 |



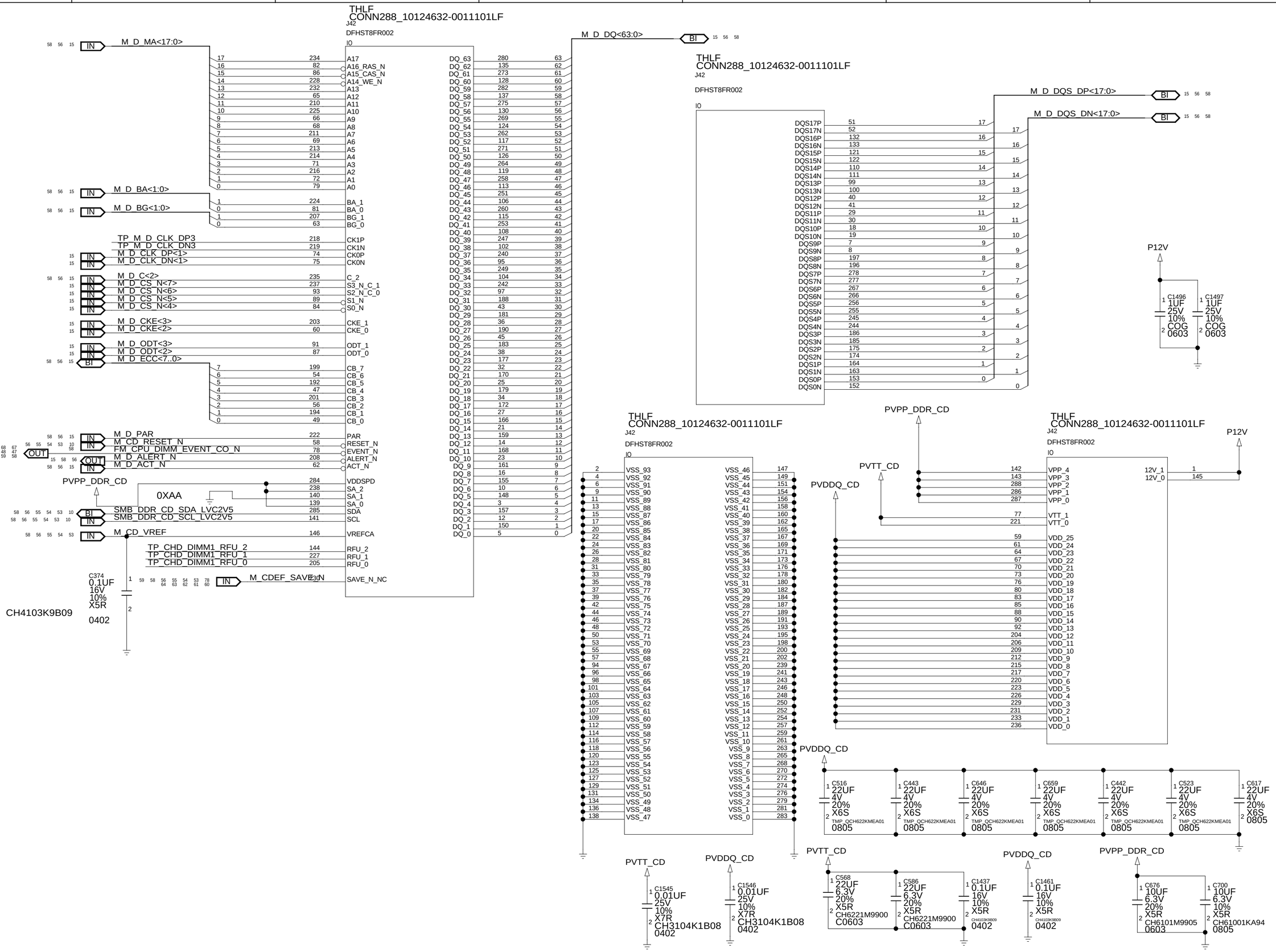

# DDR4 CHANNEL C DIMM3 (BLACK)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:35 2015 | SHEET: 55 OF 188 |



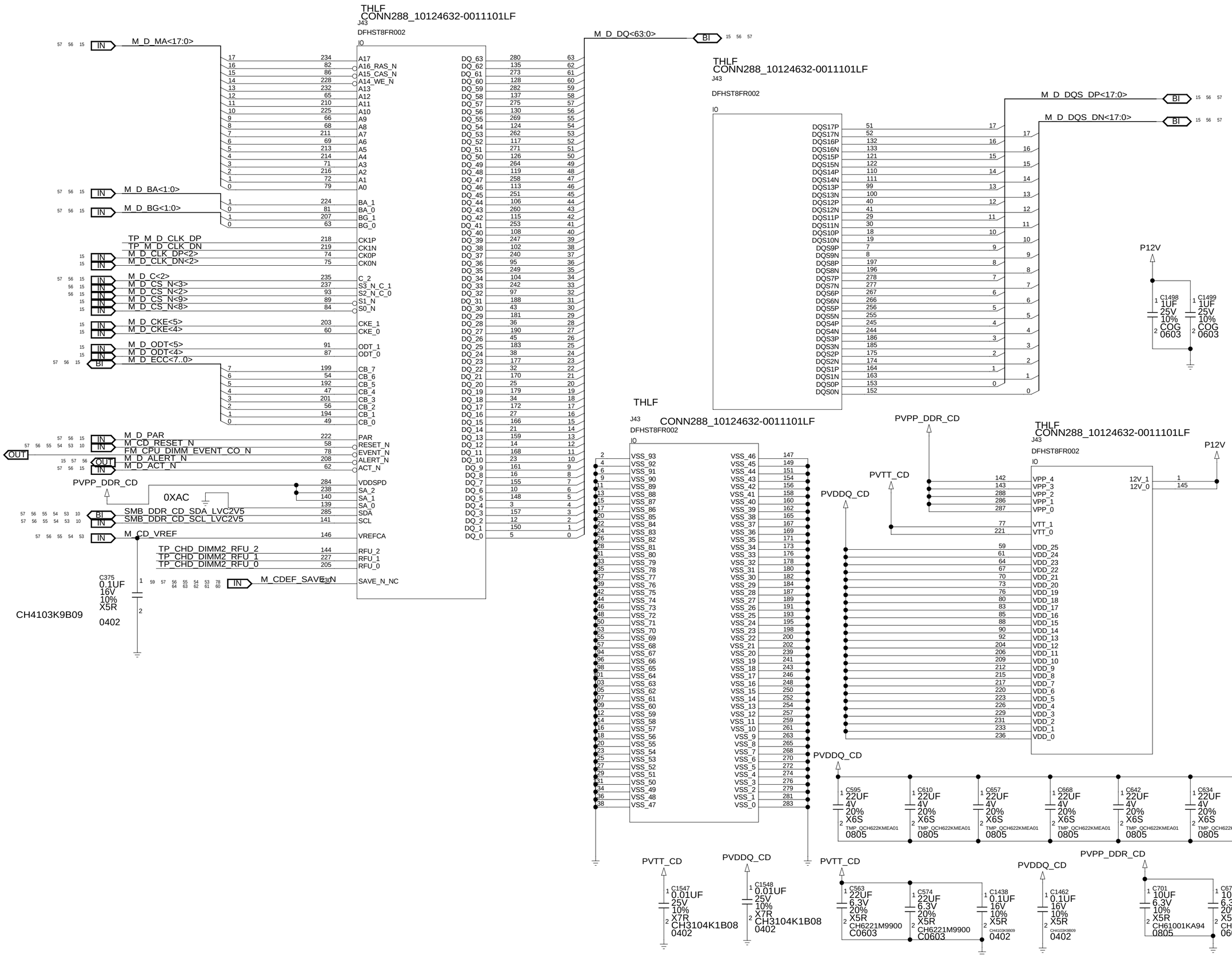

# DDR4 CHANNEL D DIMM1 (BLUE)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:38 2015 | SHEET: 56 OF 188 |




# DDR4 CHANNEL D DIMM2 (BLACK)

| | | | |
|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B |
| | | REVIEWER: PETER,YULIN,MATT | DOCUMENT NUMBER: DA0S2BMB8A0 |
| | | SIZE: C | DATE: Mon Nov 16 11:52:40 2015 |
| | | | SHEET: 57 OF 188 |
| | | | REV: 1 |




# DDR4 CHANNEL D DIMM3 (BLACK)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:42 2015 | SHEET: 58 OF 188 |

THLF
CONN288_10124632-0011101LF
J49
DFHST8FR002
IO

M_E_MA<17:0>
M_E_BA<1:0>
M_E_BG<1:0>
TP_M_E_CLK_DP2
TP_M_E_CLK_DN2
M_E_CLK_DP<0>
M_E_CLK_DN<0>
M_E_C<2>
M_E_CS_N<3>
M_E_CS_N<2>
M_E_CS_N<1>
M_E_CS_N<0>
M_E_CKE<1>
M_E_CKE<0>
M_E_ODT<1>
M_E_ODT<0>
M_E_ECC<7..0>
M_E_PAR
M_EF_RESET_N
FM_CPU_DIMM_EVENT_CO_N
M_E_ALERT_N
M_E_ACT_N
PVPP_DDR_EF
0XA0
SMB_DDR_EF_SDA_LVC2V5
SMB_DDR_EF_SCL_LVC2V5
M_EF_VREF
TP_CHE_DIMM0_RFU_2
TP_CHE_DIMM0_RFU_1
TP_CHE_DIMM0_RFU_0
M_CDEF_SAVE_N

| | | | |
|---|---|---|---|
| A17 | 234 | 17 | |
| A16_RAS_N | 82 | 16 | |
| A15_CAS_N | 86 | 15 | |
| A14_WE_N | 228 | 14 | |
| A13 | 232 | 13 | |
| A12 | 65 | 12 | |
| A11 | 210 | 11 | |
| A10 | 225 | 10 | |
| A9 | 66 | 9 | |
| A8 | 68 | 8 | |
| A7 | 211 | 7 | |
| A6 | 69 | 6 | |
| A5 | 213 | 5 | |
| A4 | 214 | 4 | |
| A3 | 71 | 3 | |
| A2 | 216 | 2 | |
| A1 | 72 | 1 | |
| A0 | 79 | 0 | |
| BA_1 | 224 | 1 | |
| BA_0 | 81 | 0 | |
| BG_1 | 207 | 1 | |
| BG_0 | 63 | 0 | |
| CK1P | 218 | | |
| CK1N | 219 | | |
| CK0P | 74 | | |
| CK0N | 75 | | |
| C_2 | 235 | | |
| S3_N_C_1 | 237 | | |
| S2_N_C_0 | 93 | | |
| S1_N | 89 | | |
| S0_N | 84 | | |
| CKE_1 | 203 | | |
| CKE_0 | 60 | | |
| ODT_1 | 91 | | |
| ODT_0 | 87 | | |
| CB_7 | 199 | 7 | |
| CB_6 | 54 | 6 | |
| CB_5 | 192 | 5 | |
| CB_4 | 47 | 4 | |
| CB_3 | 201 | 3 | |
| CB_2 | 56 | 2 | |
| CB_1 | 194 | 1 | |
| CB_0 | 49 | 0 | |
| PAR | 222 | | |
| RESET_N | 58 | | |
| EVENT_N | 78 | | |
| ALERT_N | 208 | | |
| ACT_N | 62 | | |
| VDDSPD | 284 | | |
| SA_2 | 238 | | |
| SA_1 | 140 | | |
| SA_0 | 139 | | |
| SDA | 285 | | |
| SCL | 141 | | |
| VREFCA | 146 | | |
| RFU_2 | 144 | | |
| RFU_1 | 227 | | |
| RFU_0 | 205 | | |
| SAVE_N_NC | 230 | | |

| | | | |
|---|---|---|---|
| DQ_63 | 280 | 63 | |
| DQ_62 | 135 | 62 | |
| DQ_61 | 273 | 61 | |
| DQ_60 | 128 | 60 | |
| DQ_59 | 282 | 59 | |
| DQ_58 | 137 | 58 | |
| DQ_57 | 275 | 57 | |
| DQ_56 | 130 | 56 | |
| DQ_55 | 269 | 55 | |
| DQ_54 | 124 | 54 | |
| DQ_53 | 262 | 53 | |
| DQ_52 | 117 | 52 | |
| DQ_51 | 271 | 51 | |
| DQ_50 | 126 | 50 | |
| DQ_49 | 264 | 49 | |
| DQ_48 | 119 | 48 | |
| DQ_47 | 258 | 47 | |
| DQ_46 | 113 | 46 | |
| DQ_45 | 251 | 45 | |
| DQ_44 | 106 | 44 | |
| DQ_43 | 260 | 43 | |
| DQ_42 | 115 | 42 | |
| DQ_41 | 253 | 41 | |
| DQ_40 | 108 | 40 | |
| DQ_39 | 247 | 39 | |
| DQ_38 | 102 | 38 | |
| DQ_37 | 240 | 37 | |
| DQ_36 | 95 | 36 | |
| DQ_35 | 249 | 35 | |
| DQ_34 | 104 | 34 | |
| DQ_33 | 242 | 33 | |
| DQ_32 | 97 | 32 | |
| DQ_31 | 188 | 31 | |
| DQ_30 | 43 | 30 | |
| DQ_29 | 181 | 29 | |
| DQ_28 | 36 | 28 | |
| DQ_27 | 190 | 27 | |
| DQ_26 | 45 | 26 | |
| DQ_25 | 183 | 25 | |
| DQ_24 | 38 | 24 | |
| DQ_23 | 177 | 23 | |
| DQ_22 | 32 | 22 | |
| DQ_21 | 170 | 21 | |
| DQ_20 | 25 | 20 | |
| DQ_19 | 179 | 19 | |
| DQ_18 | 34 | 18 | |
| DQ_17 | 172 | 17 | |
| DQ_16 | 27 | 16 | |
| DQ_15 | 166 | 15 | |
| DQ_14 | 21 | 14 | |
| DQ_13 | 159 | 13 | |
| DQ_12 | 14 | 12 | |
| DQ_11 | 168 | 11 | |
| DQ_10 | 23 | 10 | |
| DQ_9 | 161 | 9 | |
| DQ_8 | 16 | 8 | |
| DQ_7 | 155 | 7 | |
| DQ_6 | 10 | 6 | |
| DQ_5 | 148 | 5 | |
| DQ_4 | 3 | 4 | |
| DQ_3 | 157 | 3 | |
| DQ_2 | 12 | 2 | |
| DQ_1 | 150 | 1 | |
| DQ_0 | 5 | 0 | |

C687 0.1UF 16V 10% X5R 0402
CH4103K9B09

PVDDQ_EF
R719 1K 1% 1/16W CHIP TMP_QCS21002FB24 0402LF
R726 2.0 1% 1/16W CHIP CS-2002FB00 0402LF
R725 1K 1% 1/16W CHIP TMP_QCS21002FB24 0402LF
M_EF_CPU_VREF
M_EF_VREF
C681 0.01UF 25V 10% X7R TMP_QCH31004KB17 0402

M_E_DQ<63:0>

THLF
CONN288_10124632-0011101LF
J49
DFHST8FR002
IO

M_E_DQS_DP<17:0>
M_E_DQS_DN<17:0>

| | | | |
|---|---|---|---|
| DQS17P | 51 | 17 | |
| DQS17N | 52 | 17 | |
| DQS16P | 132 | 16 | |
| DQS16N | 133 | 16 | |
| DQS15P | 121 | 15 | |
| DQS15N | 122 | 15 | |
| DQS14P | 110 | 14 | |
| DQS14N | 111 | 14 | |
| DQS13P | 99 | 13 | |
| DQS13N | 100 | 13 | |
| DQS12P | 40 | 12 | |
| DQS12N | 41 | 12 | |
| DQS11P | 29 | 11 | |
| DQS11N | 30 | 11 | |
| DQS10P | 18 | 10 | |
| DQS10N | 19 | 10 | |
| DQS9P | 7 | 9 | |
| DQS9N | 8 | 9 | |
| DQS8P | 197 | 8 | |
| DQS8N | 196 | 8 | |
| DQS7P | 278 | 7 | |
| DQS7N | 277 | 7 | |
| DQS6P | 267 | 6 | |
| DQS6N | 266 | 6 | |
| DQS5P | 256 | 5 | |
| DQS5N | 255 | 5 | |
| DQS4P | 245 | 4 | |
| DQS4N | 244 | 4 | |
| DQS3P | 186 | 3 | |
| DQS3N | 185 | 3 | |
| DQS2P | 175 | 2 | |
| DQS2N | 174 | 2 | |
| DQS1P | 164 | 1 | |
| DQS1N | 163 | 1 | |
| DQS0P | 153 | 0 | |
| DQS0N | 152 | 0 | |

P12V
C1500 1UF 25V 10% COG 0603
C1501 1UF 25V 10% COG 0603

THLF
CONN288_10124632-0011101LF
J49
DFHST8FR002
IO

| | | | |
|---|---|---|---|
| VSS_93 | 2 | VSS_46 | 147 |
| VSS_92 | 4 | VSS_45 | 149 |
| VSS_91 | 6 | VSS_44 | 151 |
| VSS_90 | 9 | VSS_43 | 154 |
| VSS_89 | 11 | VSS_42 | 156 |
| VSS_88 | 13 | VSS_41 | 158 |
| VSS_87 | 15 | VSS_40 | 160 |
| VSS_86 | 17 | VSS_39 | 162 |
| VSS_85 | 20 | VSS_38 | 165 |
| VSS_84 | 22 | VSS_37 | 167 |
| VSS_83 | 24 | VSS_36 | 169 |
| VSS_82 | 26 | VSS_35 | 171 |
| VSS_81 | 28 | VSS_34 | 173 |
| VSS_80 | 31 | VSS_33 | 176 |
| VSS_79 | 33 | VSS_32 | 178 |
| VSS_78 | 35 | VSS_31 | 180 |
| VSS_77 | 37 | VSS_30 | 182 |
| VSS_76 | 39 | VSS_29 | 184 |
| VSS_75 | 42 | VSS_28 | 187 |
| VSS_74 | 44 | VSS_27 | 189 |
| VSS_73 | 46 | VSS_26 | 191 |
| VSS_72 | 48 | VSS_25 | 193 |
| VSS_71 | 50 | VSS_24 | 195 |
| VSS_70 | 53 | VSS_23 | 198 |
| VSS_69 | 55 | VSS_22 | 200 |
| VSS_68 | 57 | VSS_21 | 202 |
| VSS_67 | 64 | VSS_20 | 239 |
| VSS_66 | 66 | VSS_19 | 241 |
| VSS_65 | 68 | VSS_18 | 243 |
| VSS_64 | 101 | VSS_17 | 246 |
| VSS_63 | 103 | VSS_16 | 248 |
| VSS_62 | 105 | VSS_15 | 250 |
| VSS_61 | 107 | VSS_14 | 252 |
| VSS_60 | 109 | VSS_13 | 254 |
| VSS_59 | 112 | VSS_12 | 257 |
| VSS_58 | 114 | VSS_11 | 259 |
| VSS_57 | 116 | VSS_10 | 261 |
| VSS_56 | 118 | VSS_9 | 263 |
| VSS_55 | 120 | VSS_8 | 265 |
| VSS_54 | 123 | VSS_7 | 268 |
| VSS_53 | 125 | VSS_6 | 270 |
| VSS_52 | 127 | VSS_5 | 272 |
| VSS_51 | 129 | VSS_4 | 274 |
| VSS_50 | 131 | VSS_3 | 276 |
| VSS_49 | 134 | VSS_2 | 279 |
| VSS_48 | 136 | VSS_1 | 281 |
| VSS_47 | 138 | VSS_0 | 283 |

PVTT_EF
C1549 0.01UF 25V 10% X7R CH3104K1B08 0402
PVDDQ_EF
C1550 0.01UF 25V 10% X7R CH3104K1B08 0402

PVPP_DDR_EF
PVTT_EF
PVDDQ_EF

THLF
CONN288_10124632-0011101LF
J49
DFHST8FR002
IO

| | | | |
|---|---|---|---|
| VPP_4 | 142 | 12V_1 | 1 |
| VPP_3 | 143 | 12V_0 | 145 |
| VPP_2 | 288 | | |
| VPP_1 | 286 | | |
| VPP_0 | 287 | | |
| VTT_1 | 77 | | |
| VTT_0 | 221 | | |
| VDD_25 | 59 | | |
| VDD_24 | 61 | | |
| VDD_23 | 64 | | |
| VDD_22 | 67 | | |
| VDD_21 | 70 | | |
| VDD_20 | 73 | | |
| VDD_19 | 76 | | |
| VDD_18 | 80 | | |
| VDD_17 | 83 | | |
| VDD_16 | 85 | | |
| VDD_15 | 88 | | |
| VDD_14 | 90 | | |
| VDD_13 | 92 | | |
| VDD_12 | 204 | | |
| VDD_11 | 206 | | |
| VDD_10 | 209 | | |
| VDD_9 | 212 | | |
| VDD_8 | 215 | | |
| VDD_7 | 217 | | |
| VDD_6 | 220 | | |
| VDD_5 | 223 | | |
| VDD_4 | 226 | | |
| VDD_3 | 229 | | |
| VDD_2 | 231 | | |
| VDD_1 | 233 | | |
| VDD_0 | 236 | | |

PVDDQ_EF
C604 22UF 4V 20% X6S 0805
C450 22UF 4V 20% X6S 0805
C446 22UF 4V 20% X6S 0805
C468 22UF 4V 20% X6S 0805
C619 22UF 4V 20% X6S 0805
C434 22UF 4V 20% X6S 0805
C403 22UF 4V 20% X6S 0805
TMP_QCH622KMEA01

PVTT_EF
C525 22UF 6.3V 20% X5R C0603
CH6221M9900
C537 22UF 6.3V 20% X5R C0603
CH6221M9900
C1439 0.1UF 16V 10% X5R 0402
CH4103K9B09

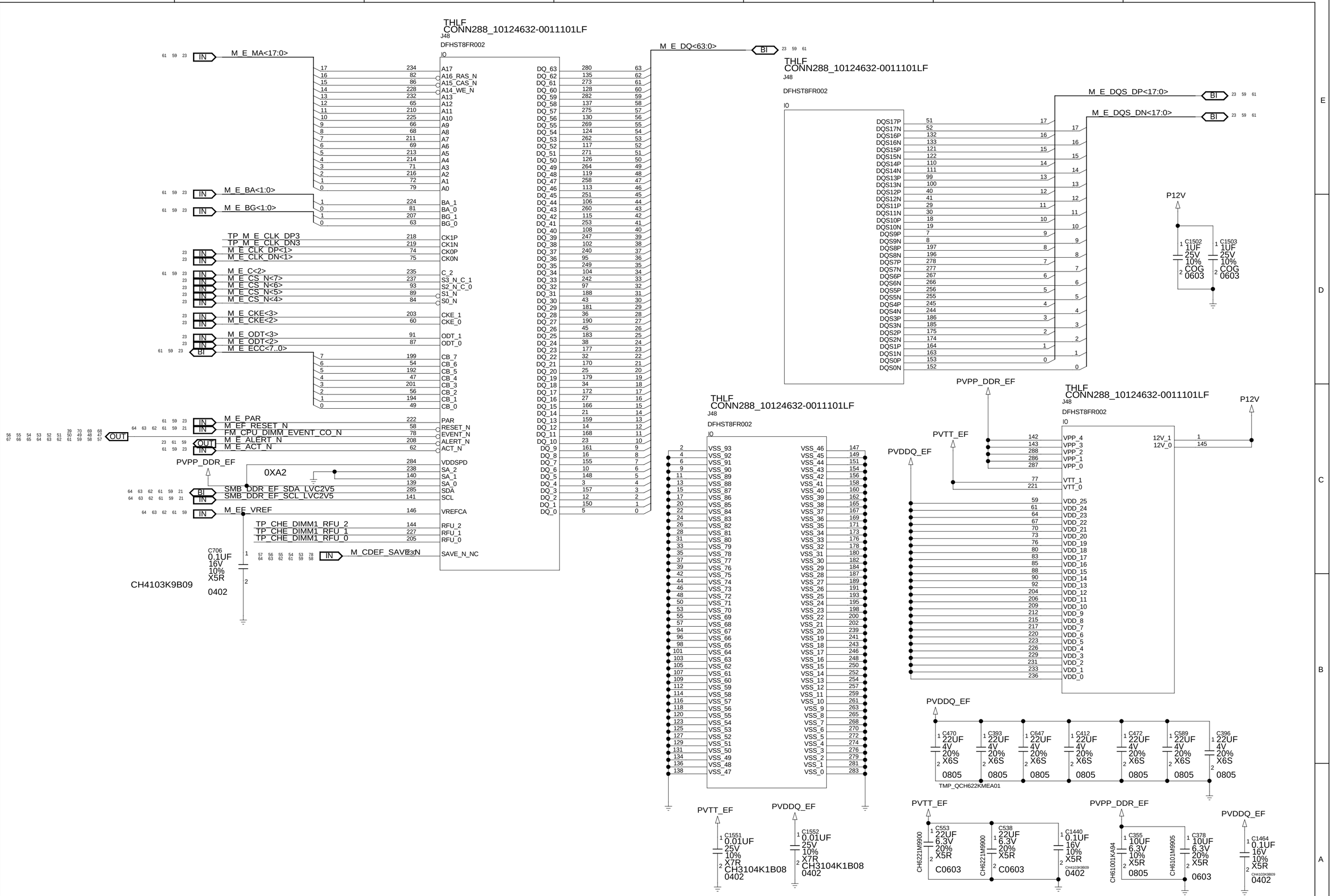
PVPP_DDR_EF
C353 10UF 6.3V 10% X5R 0805
CH61001KA94
C376 10UF 6.3V 20% X5R 0603
CH6101M9905

PVDDQ_EF
C1463 0.1UF 16V 10% X5R 0402
CH4103K9B09

# DDR4 CHANNEL E DIMM1 (BLUE)

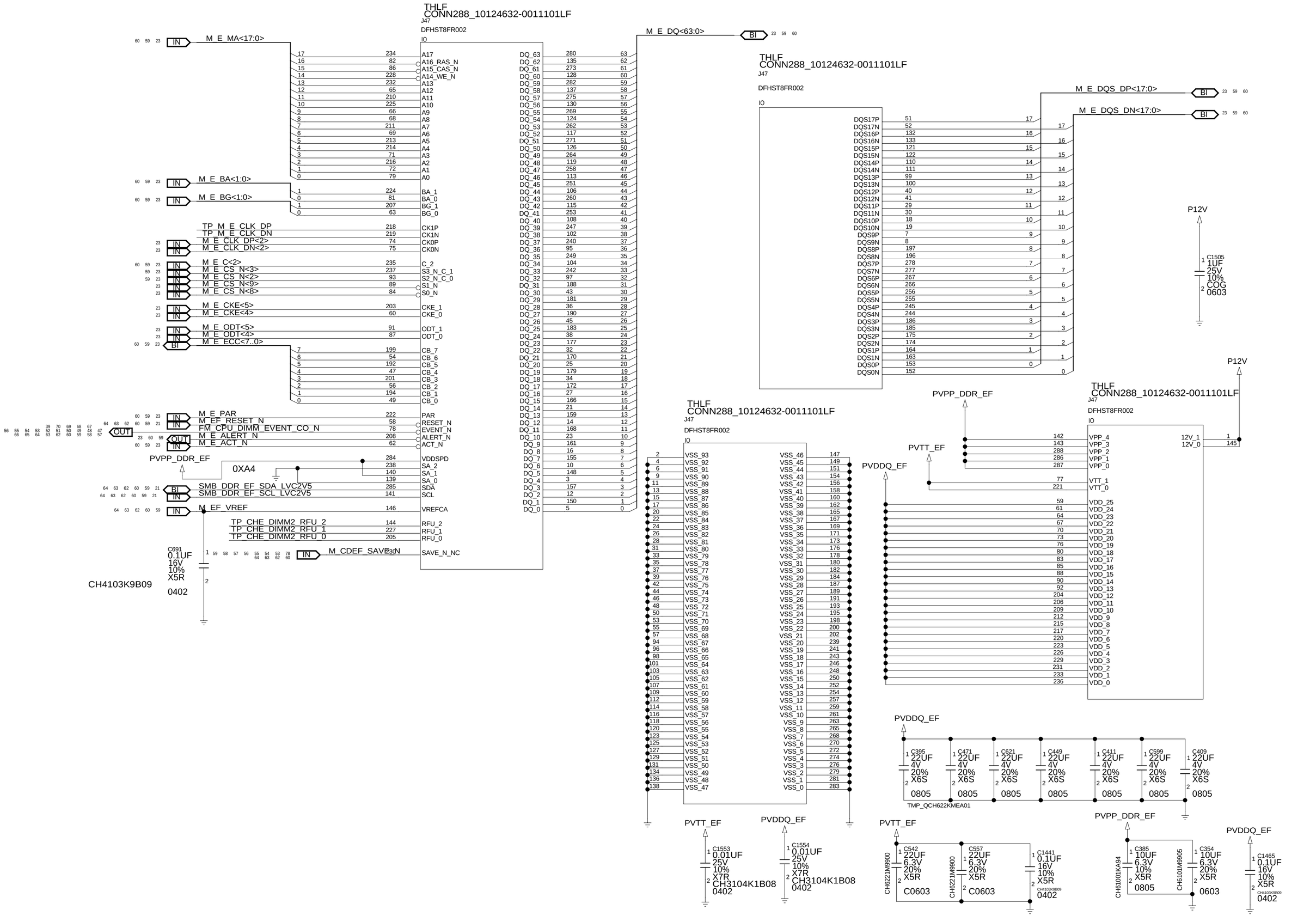
Quanta

| | | | | | |
|---|---|---|---|---|---|
| DEPARTMENT | CCBU | DESIGNER | NICK | PROJCET | S2B |
| | | REVIEWER | PETER,YULIN,MATT | DOCUMENT NUMBER | DA0S2BMB8A0 |
| | | | | REV | 1 |
| | | | | SIZE C | DATE Mon Nov 16 11:52:45 2015 |
| | | | | SHEET | 59 OF 188 |



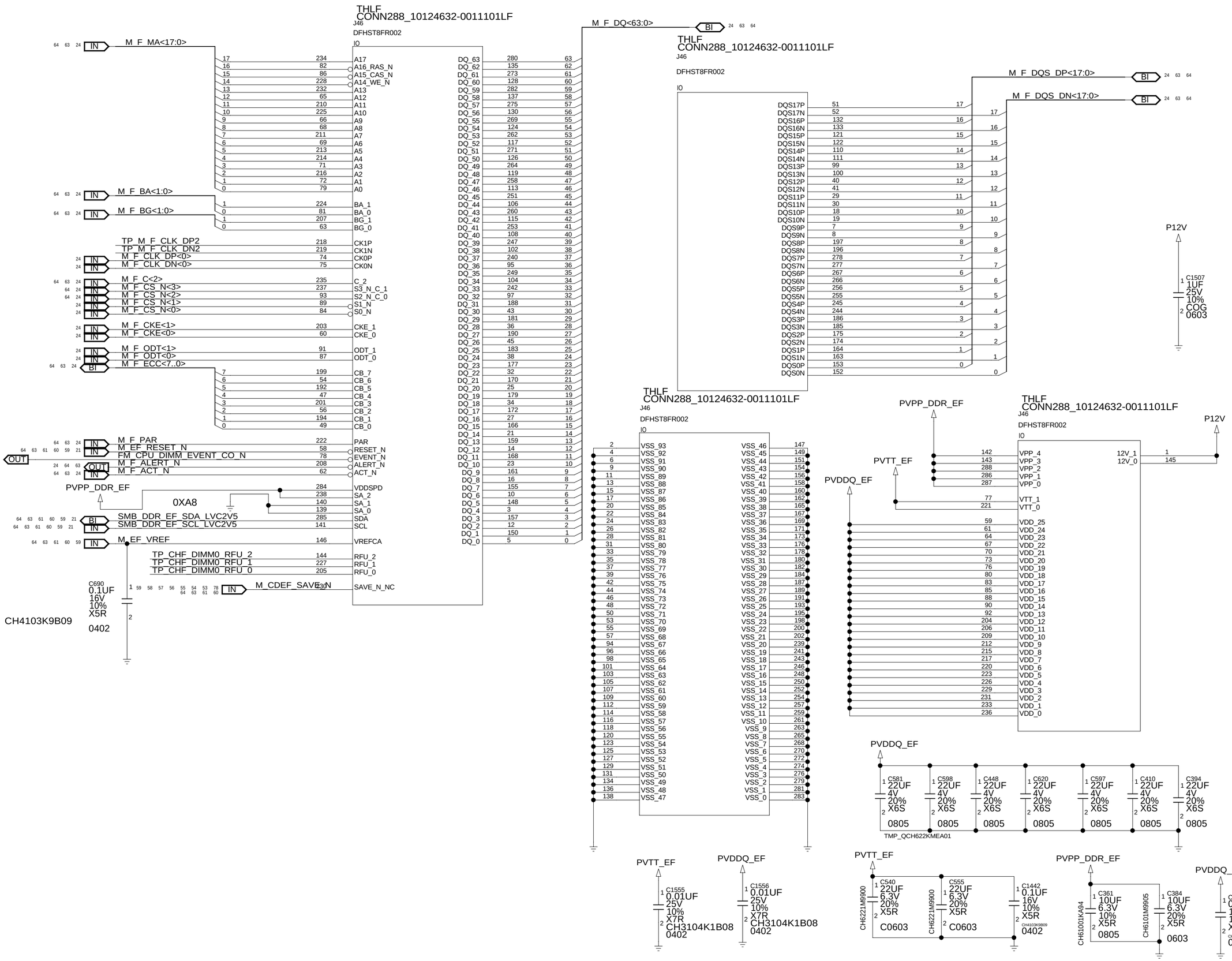

# DDR4 CHANNEL E DIMM2 (BLACK)

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:47 2015 | SHEET: 60 OF 188 |



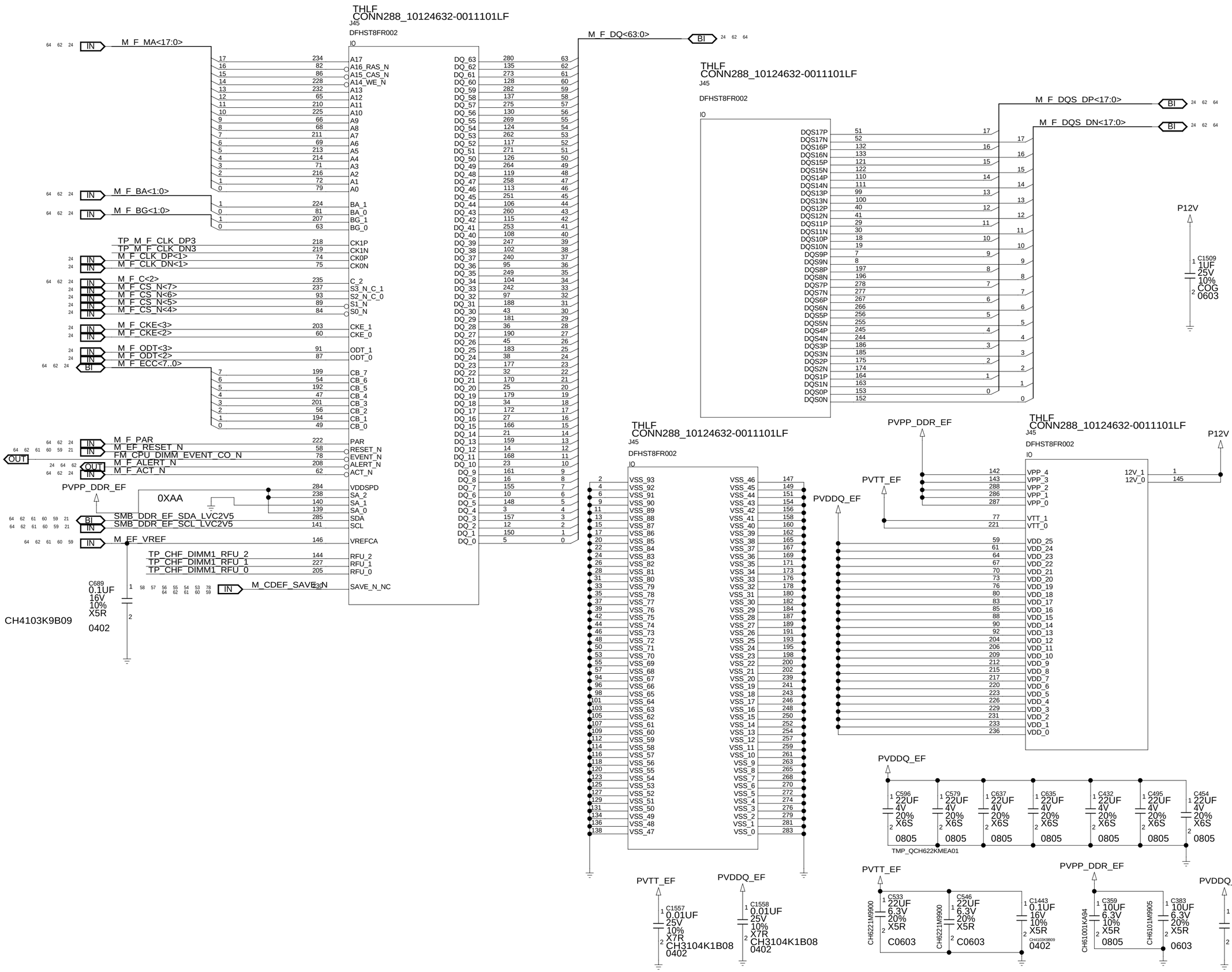

# DDR4 CHANNEL E DIMM3 (BLACK)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:49 2015 | SHEET: 61 OF 188 |



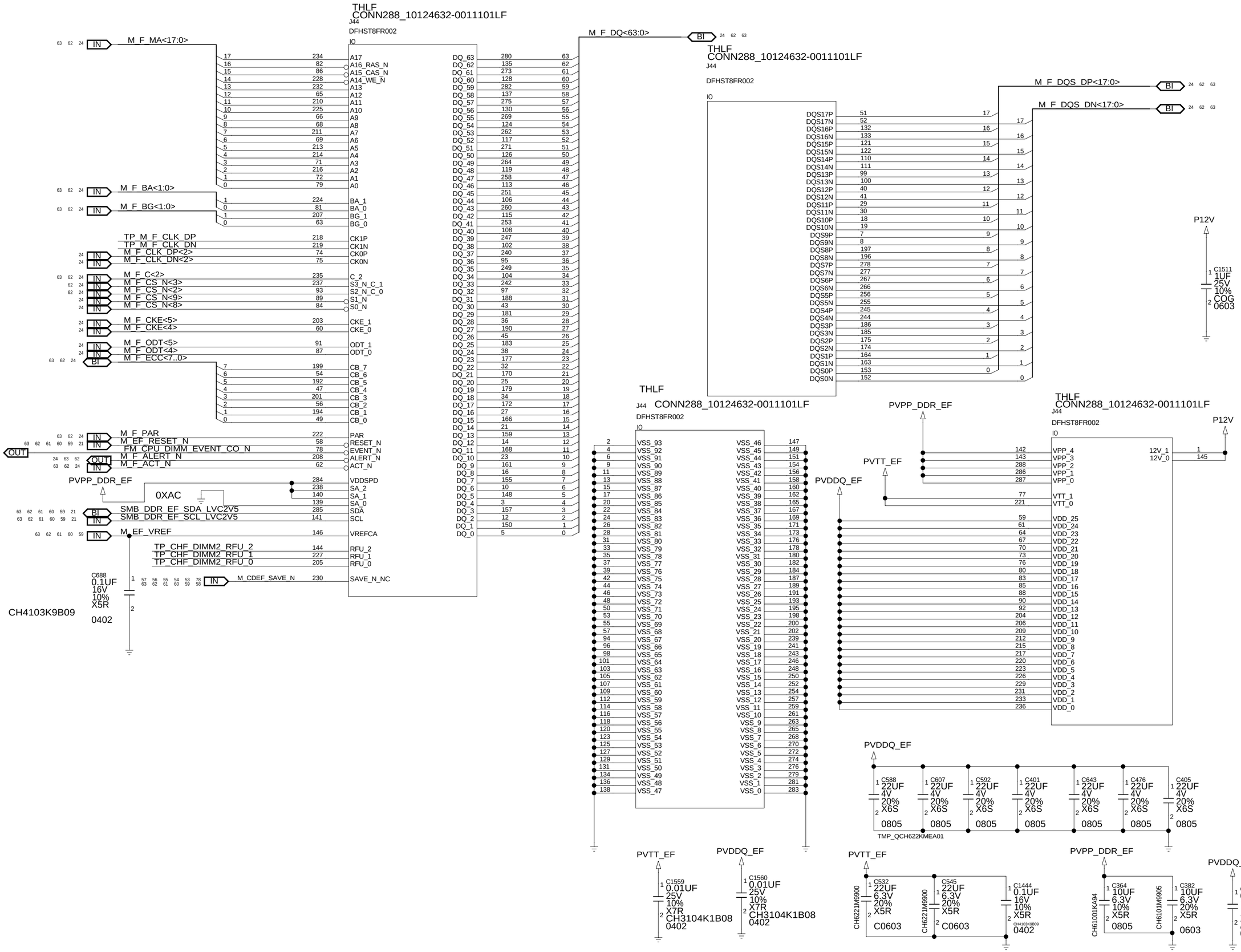

# DDR4 CHANNEL F DIMM1 (BLUE)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:52 2015 | SHEET: 62 OF 188 |



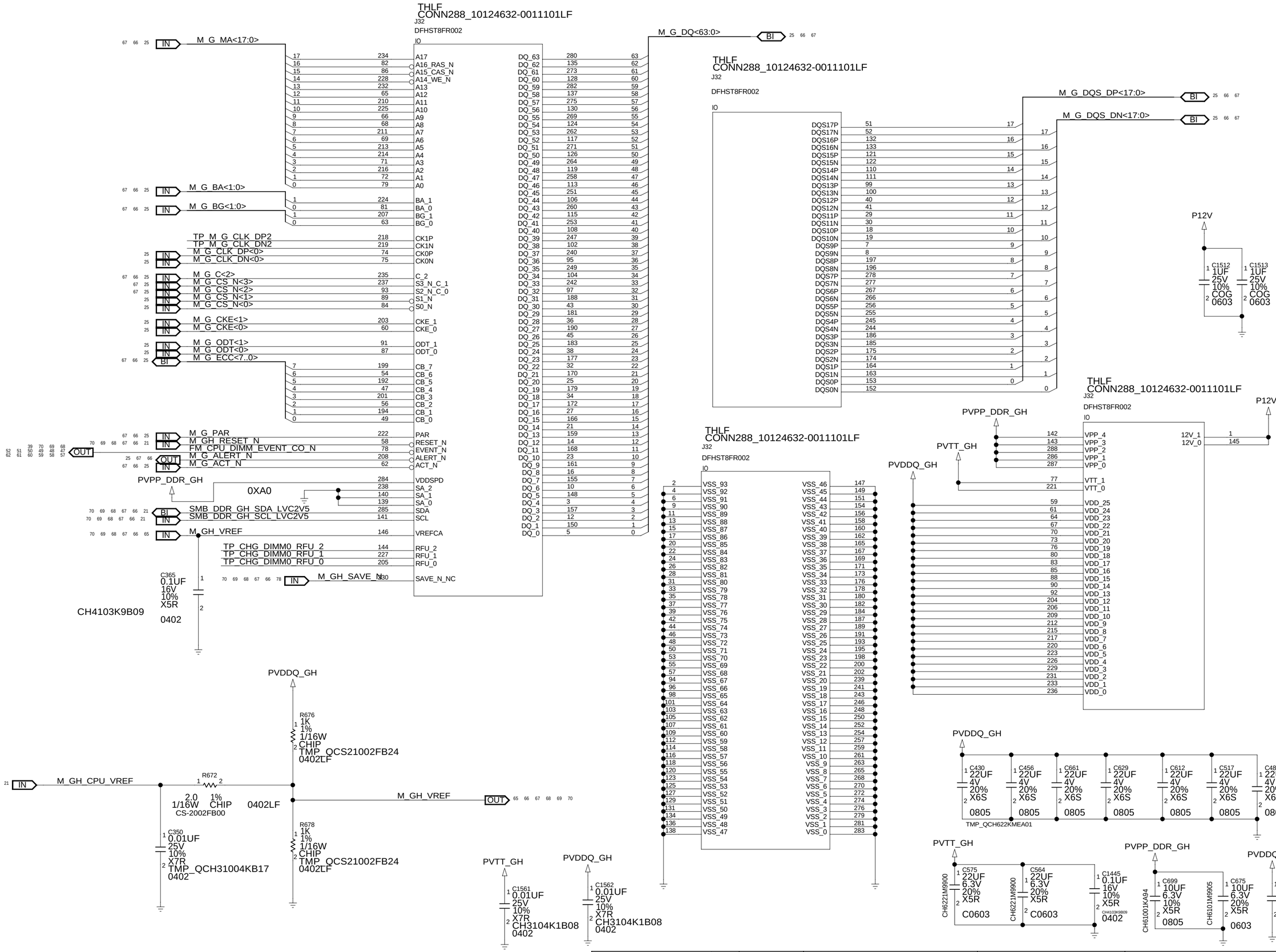

# DDR4 CHANNEL F DIMM2 (BLACK)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:55 2015 | SHEET: 63 OF 188 |



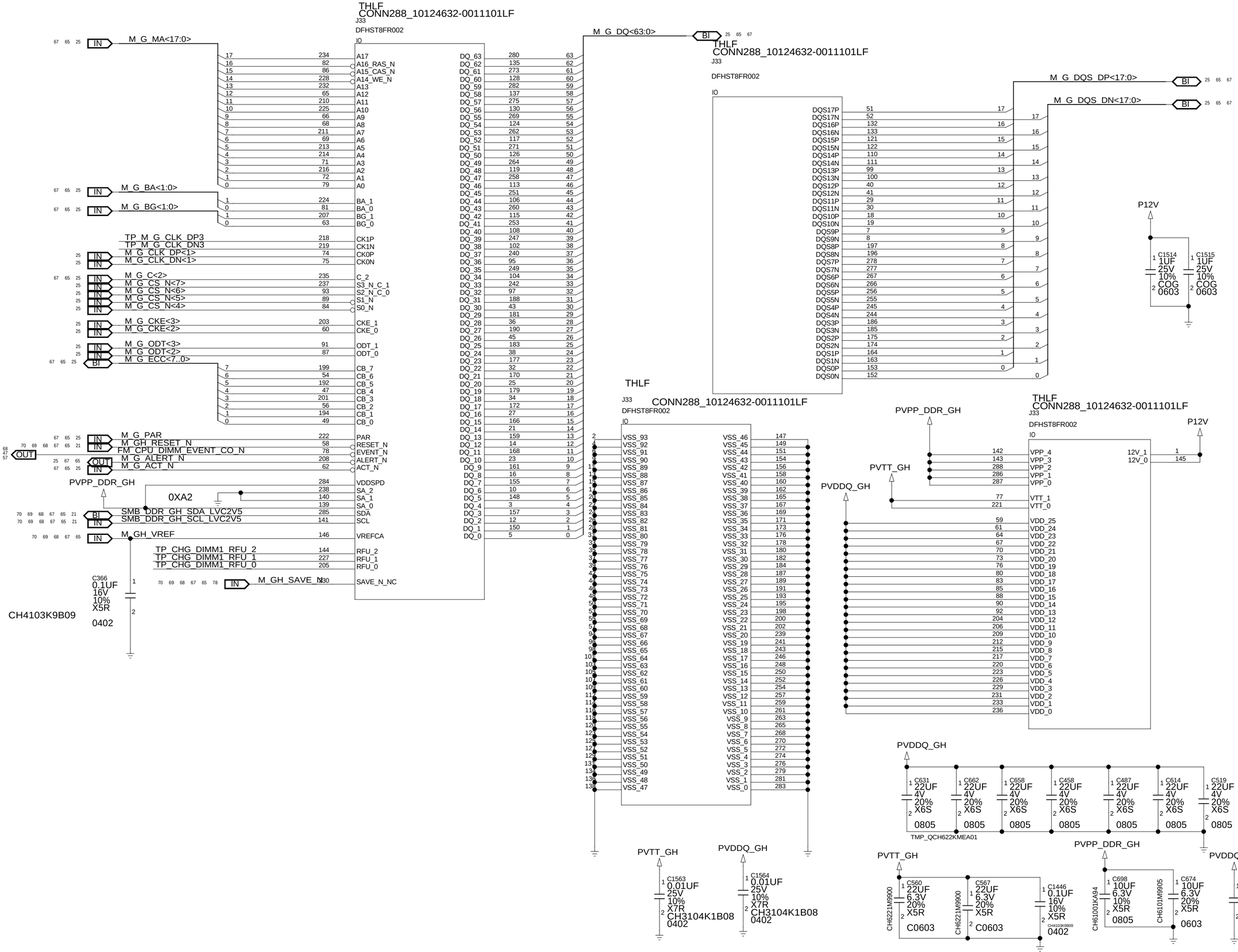

# DDR4 CHANNEL F DIMM3 (BLACK)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:52:58 2015 | SHEET: 64 OF 188 |



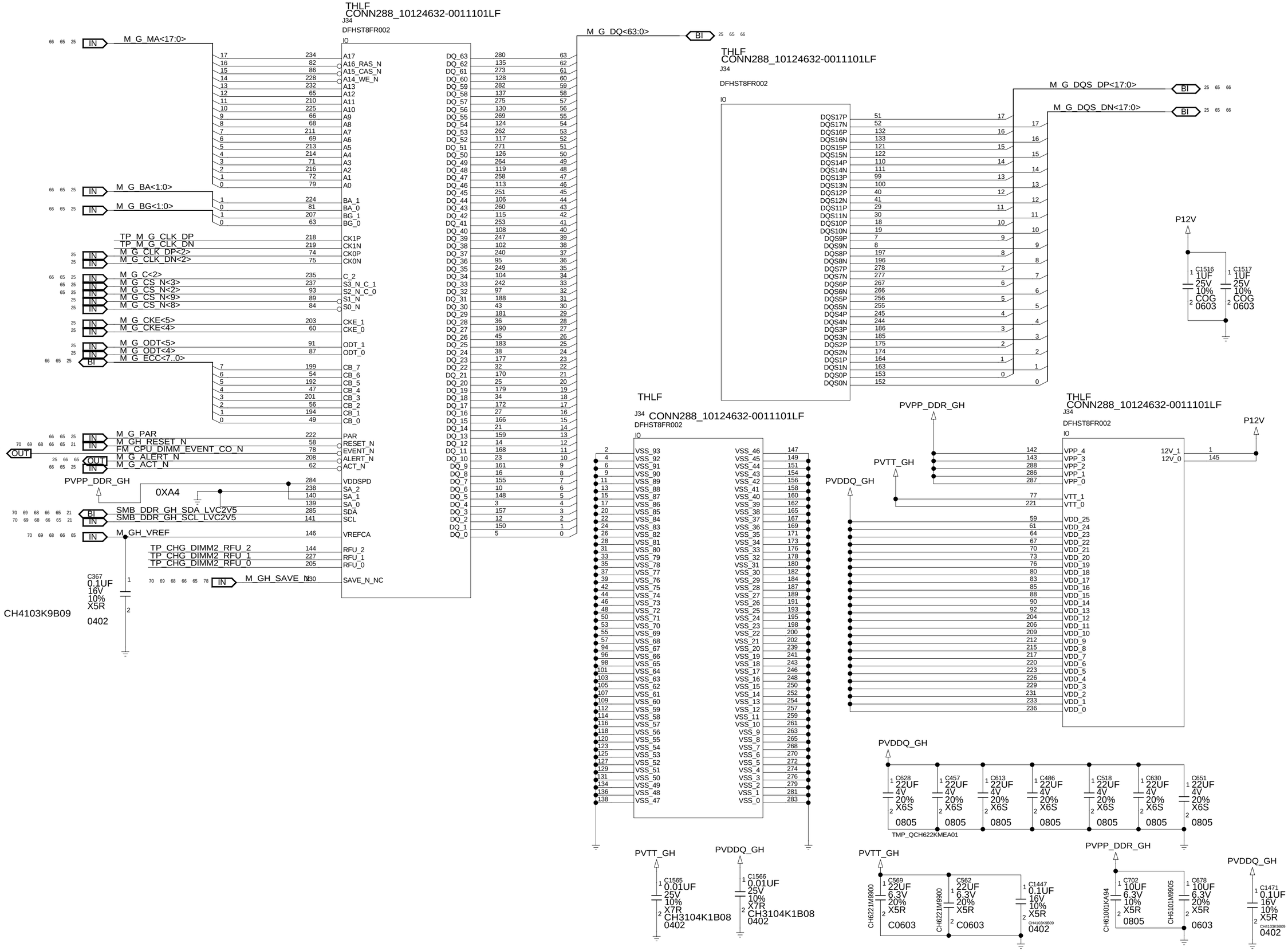

# DDR4 CHANNEL G DIMM1 (BLUE)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:53:00 2015 | SHEET: 65 OF 188 |



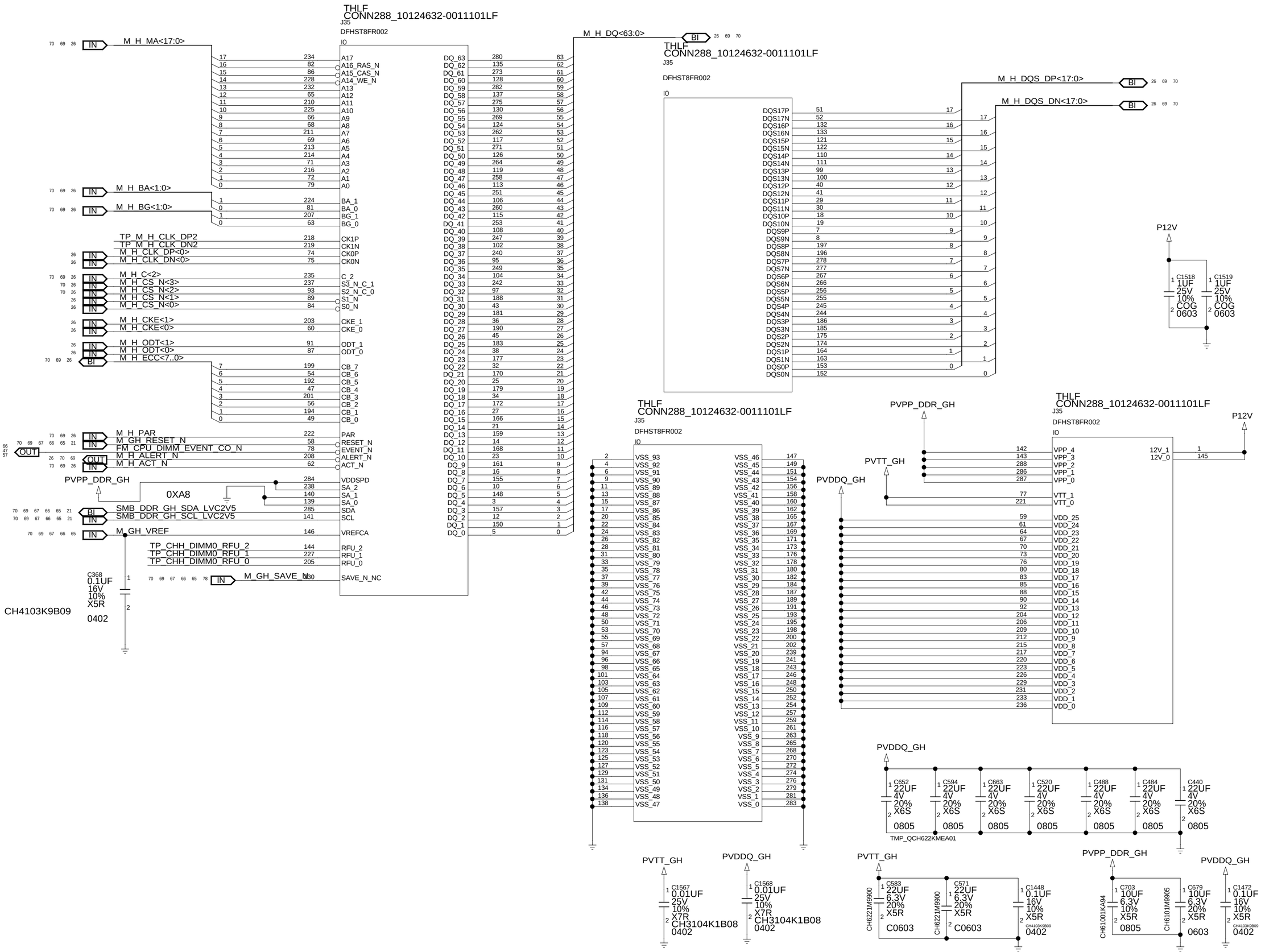

# DDR4 CHANNEL G DIMM2 (BLACK)

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:53:02 2015 | SHEET: 66 OF 188 |




# DDR4 CHANNEL G DIMM3 (BLACK)

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:53:05 2015 | SHEET: 67 OF 188 |




# DDR4 CHANNEL H DIMM1 (BLUE)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:53:07 2015 | SHEET: 68 OF 188 |

THLF
CONN288_10124632-0011101LF
J36
DFHST8FR002
IO

M_H_MA<17:0>
M_H_BA<1:0>
M_H_BG<1:0>
TP_M_H_CLK_DP3
TP_M_H_CLK_DN3
M_H_CLK_DP<1>
M_H_CLK_DN<1>
M_H_C<2>
M_H_CS_N<7>
M_H_CS_N<6>
M_H_CS_N<5>
M_H_CS_N<4>
M_H_CKE<3>
M_H_CKE<2>
M_H_ODT<3>
M_H_ODT<2>
M_H_ECC<7..0>
M_H_PAR
M_GH_RESET_N
FM_CPU_DIMM_EVENT_CO_N
M_H_ALERT_N
M_H_ACT_N
PVPP_DDR_GH
0XAA
SMB_DDR_GH_SDA_LVC2V5
SMB_DDR_GH_SCL_LVC2V5
M_GH_VREF
TP_CHH_DIMM1_RUF_2
TP_CHH_DIMM1_RFU_1
TP_CHH_DIMM1_RFU_0
M_GH_SAVE_N
C369 0.1UF 16V 10% X5R 0402
CH4103K9B09

M_H_DQ<63:0>

THLF
CONN288_10124632-0011101LF
J36
DFHST8FR002
IO

M_H_DQS_DP<17:0>
M_H_DQS_DN<17:0>

P12V
C1520 1UF 25V 10% COG 0603
C1521 1UF 25V 10% COG 0603

THLF
CONN288_10124632-0011101LF
J36
DFHST8FR002
IO

PVPP_DDR_GH
PVTT_GH
PVDDQ_GH
P12V

THLF
CONN288_10124632-0011101LF
J36
DFHST8FR002
IO

PVDDQ_GH
C515 22UF 4V 20% X6S 0805
C639 22UF 4V 20% X6S 0805
C482 22UF 4V 20% X6S 0805
C609 22UF 4V 20% X6S 0805
C420 22UF 4V 20% X6S 0805
C656 22UF 4V 20% X6S 0805
C611 22UF 4V 20% X6S 0805
TMP_QCH622KMEA01

PVTT_GH
C1569 0.01UF 25V 10% X7R CH3104K1B08 0402
PVDDQ_GH
C1570 0.01UF 25V 10% X7R CH3104K1B08 0402

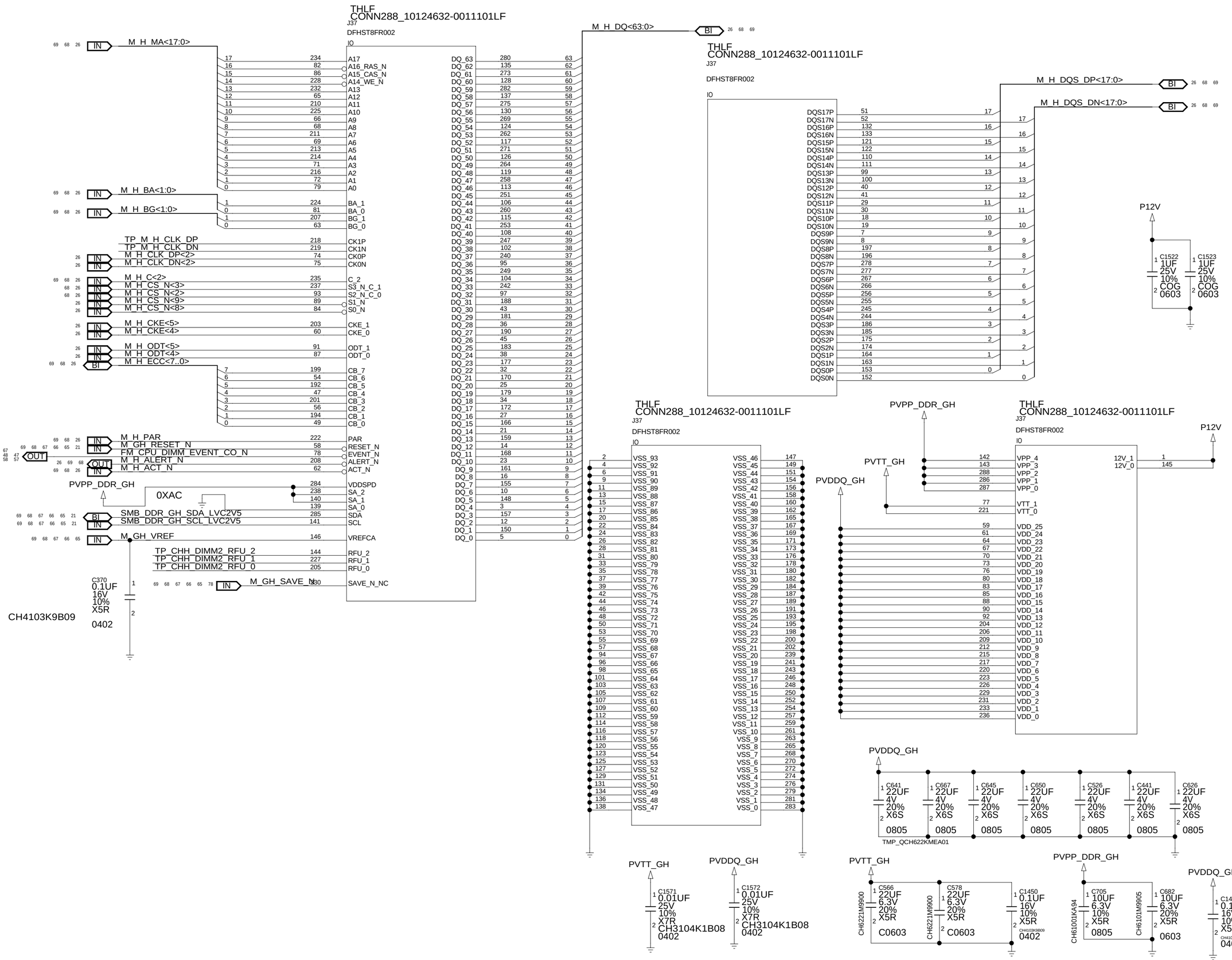
PVTT_GH
C584 22UF 6.3V 20% X5R C0603
CH6221M9900
C572 22UF 6.3V 20% X5R C0603
CH6221M9900
C1449 0.1UF 16V 10% X5R 0402
CH4103K9B09

PVPP_DDR_GH
C707 10UF 6.3V 10% X5R 0805
CH61001KA94
C684 10UF 6.3V 20% X5R 0603
CH61101M9905

PVDDQ_GH
C1473 0.1UF 16V 10% X5R 0402
CH4103K9B09

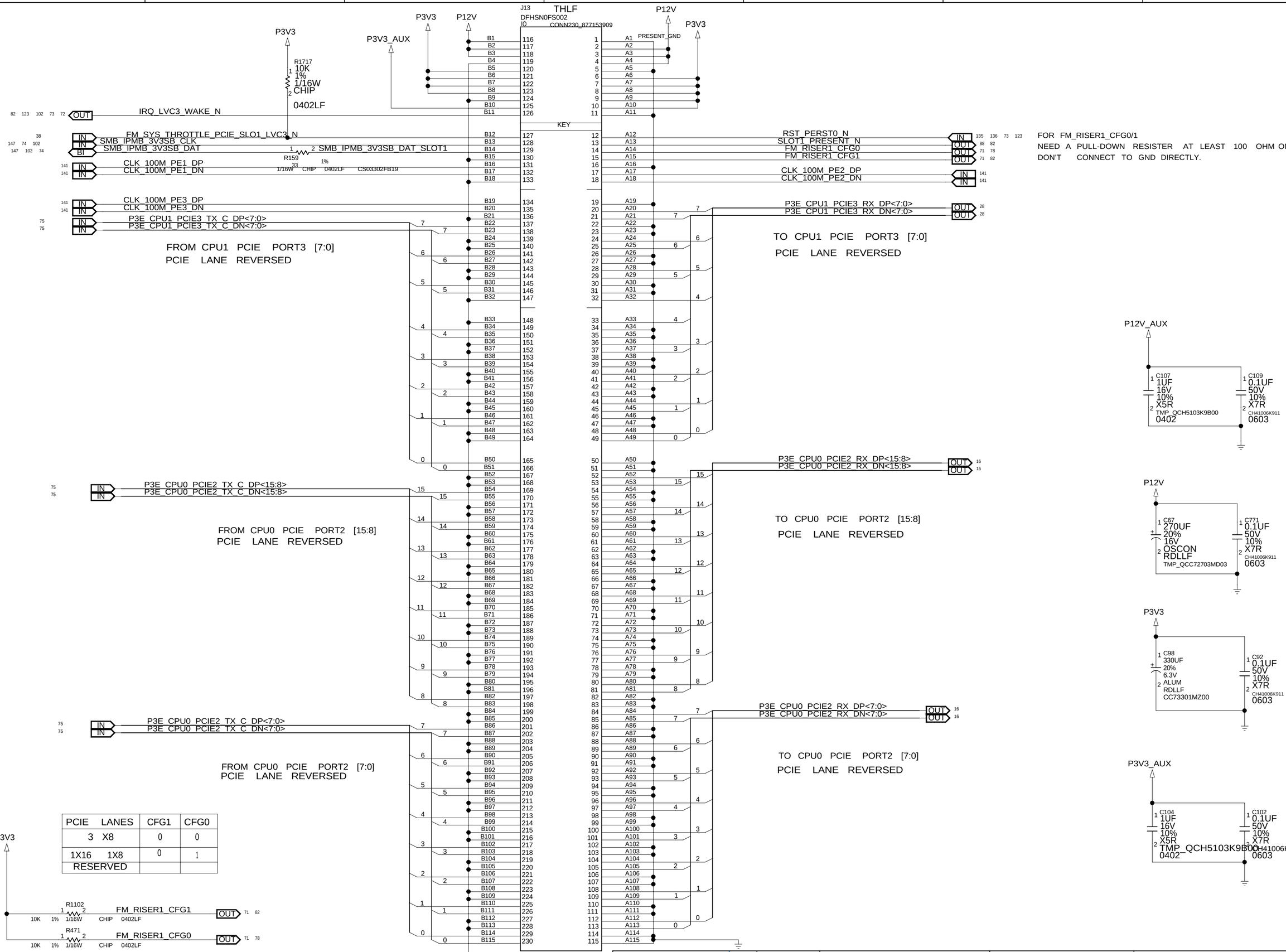
# DDR4 CHANNEL H DIMM2 (BLACK)

| | | | |
|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B |
| | | REVIEWER: PETER,YULIN,MATT | DOCUMENT NUMBER: DA0S2BMB8A0 |
| | | SIZE: C | DATE: Mon Nov 16 11:53:09 2015 |
| | | | SHEET: 69 OF 188 |
| | | | REV: 1 |




# DDR4 CHANNEL H DIMM3 (BLACK)

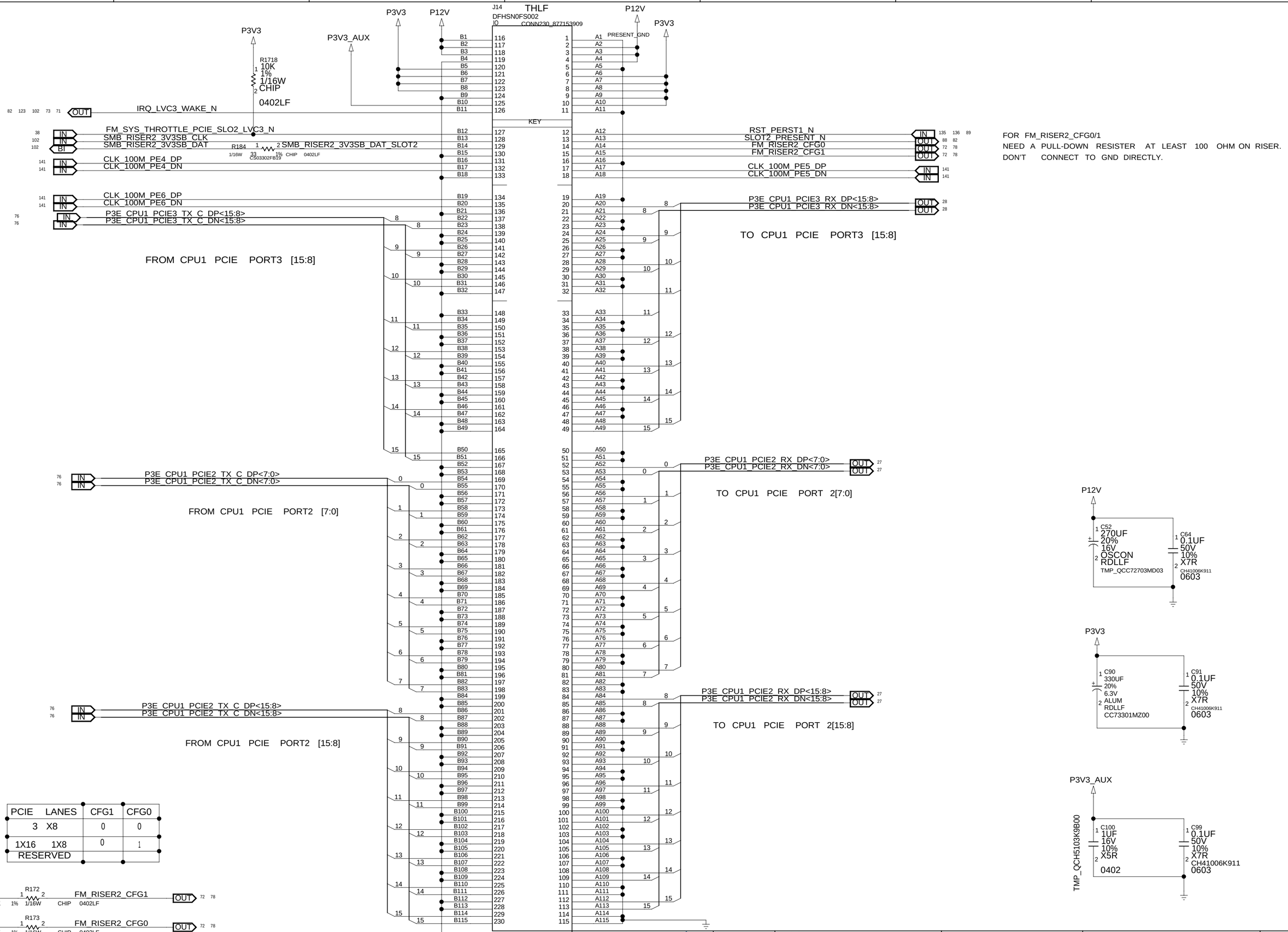
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:53:11 2015 | SHEET 70 OF 188 |




| PCIE LANES | CFG1 | CFG0 |
|---|---|---|
| 3 X8 | 0 | 0 |
| 1X16 1X8 | 0 | 1 |
| RESERVED | | |

# PCIE RISER SLOT 1

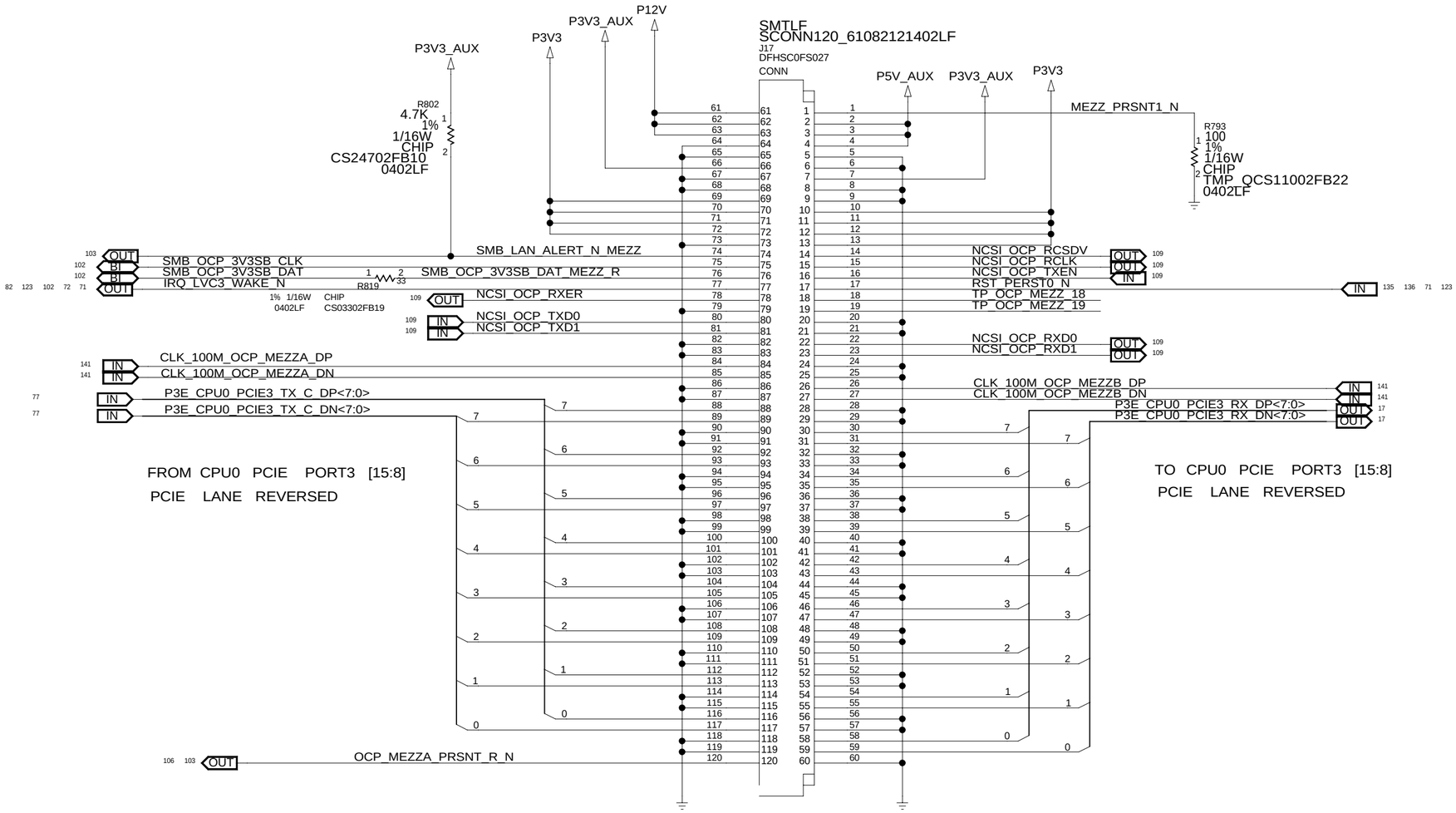
| | | | |
|---|---|---|---|
| DEPARTMENT | DESIGNER | PROJCET | DOCUMENT NUMBER / REV |
| CCBU | NICK | S2B | DA0S2BMB8A0 / 1 |
| | REVIEWER: PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:53:17 2015 |
| | | | SHEET 71 OF 188 |




# PCIE RISER SLOT 2

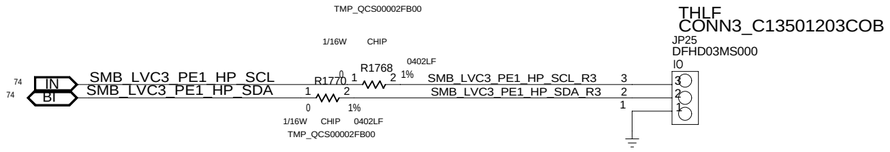
| | | | | | |
|---|---|---|---|---|---|
| DEPARTMENT | DESIGNER | PROJCET | DOCUMENT NUMBER | REV |
| CCBU | NICK | S2B | DA0S2BMB8A0 | 1 |
| | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:53:19 2015 | SHEET 72 OF 188 |

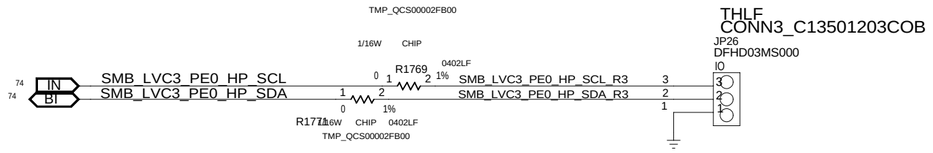
# OCP MEZZ

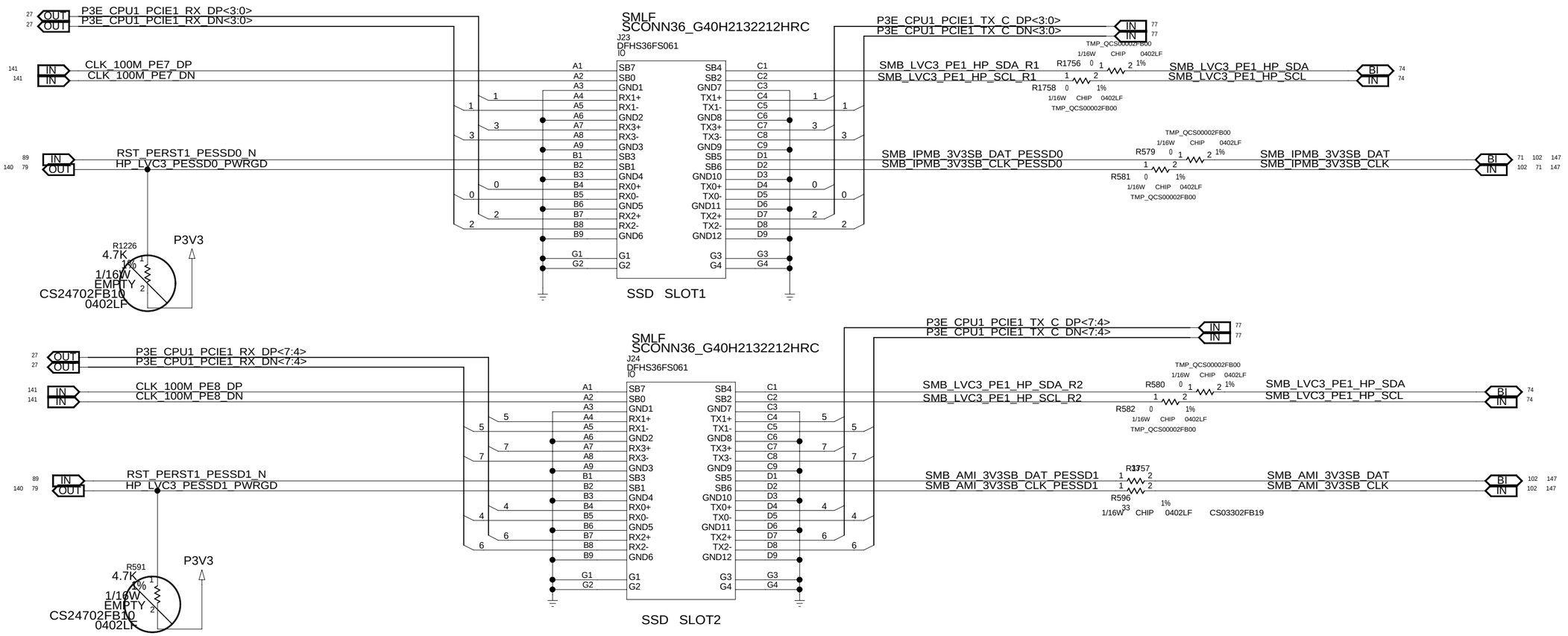



# PCIE OCP MEZZ

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:53:20 2015 | SHEET: 73 OF 188 |



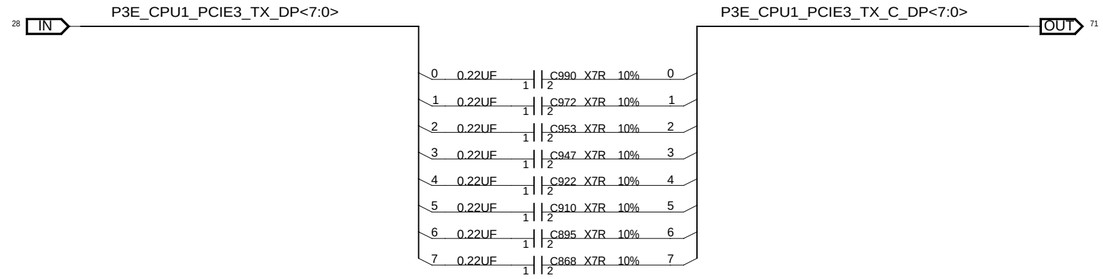



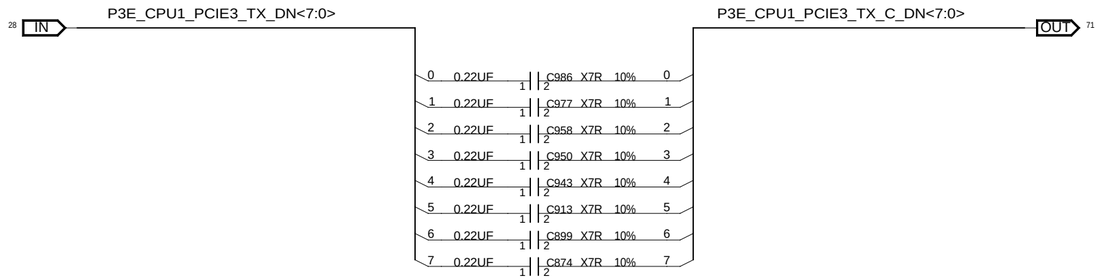




# PCIE SSD

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:53:22 2015 | SHEET: 74 OF 188 |

# RISER SLOT1





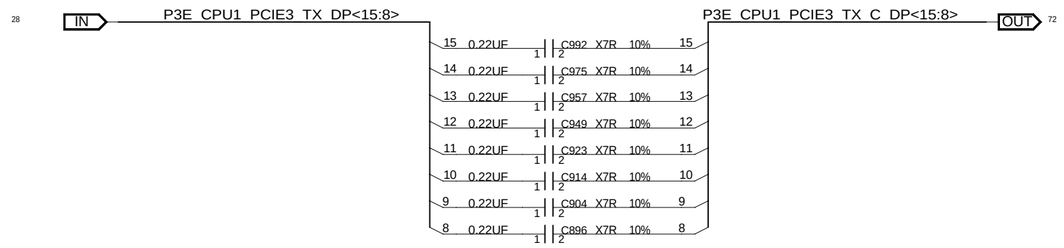


# PCIE AC COUPLE CAPS - RISER 1

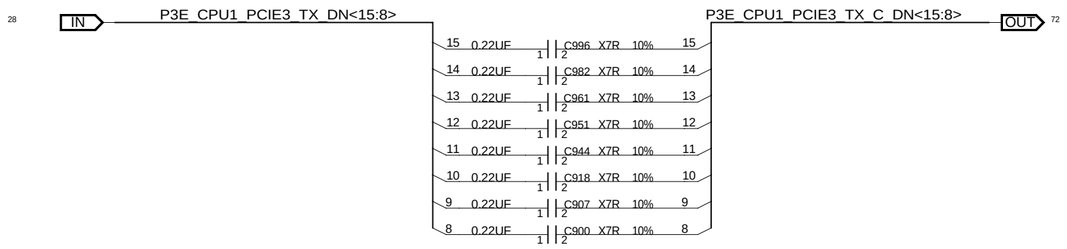
Quanta

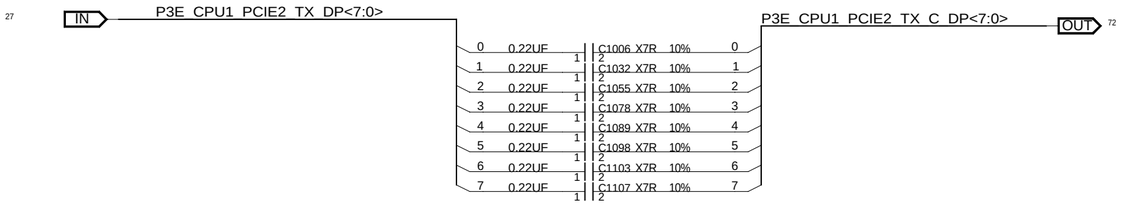
| DEPARTMENT | DESIGNER | PROJCET | DOCUMENT NUMBER | REV |
|---|---|---|---|---|
| CCBU | NICK | S2B | DA0S2BMB8A0 | 1 |
| | REVIEWER: PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:53:23 2015 | SHEET 75 OF 188 |

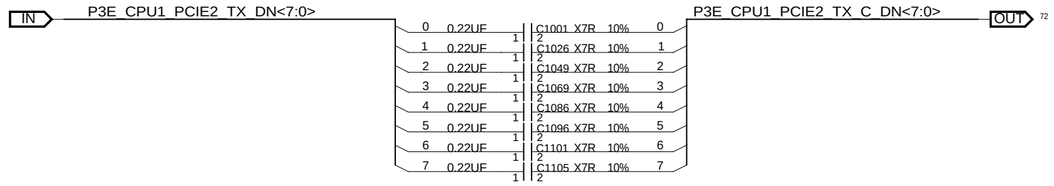
# RISER SLOT2

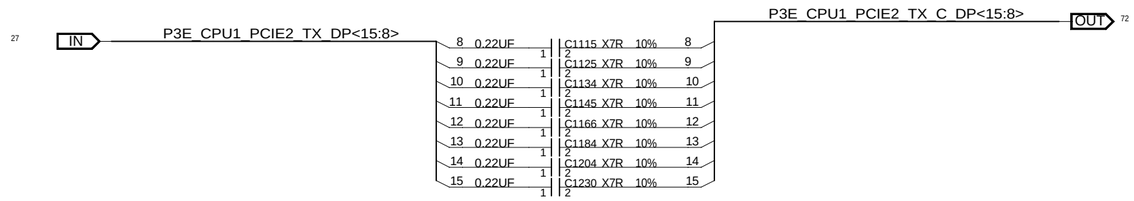


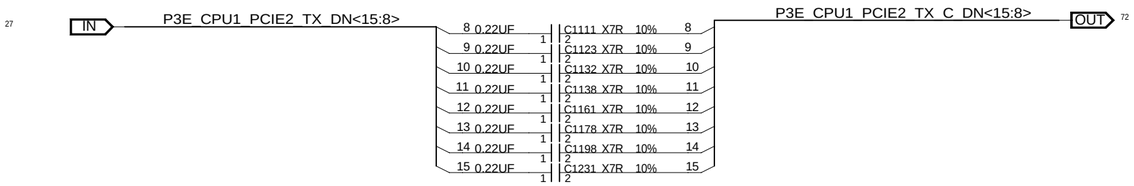

PLEASE CLOSE TO CPU SIDE



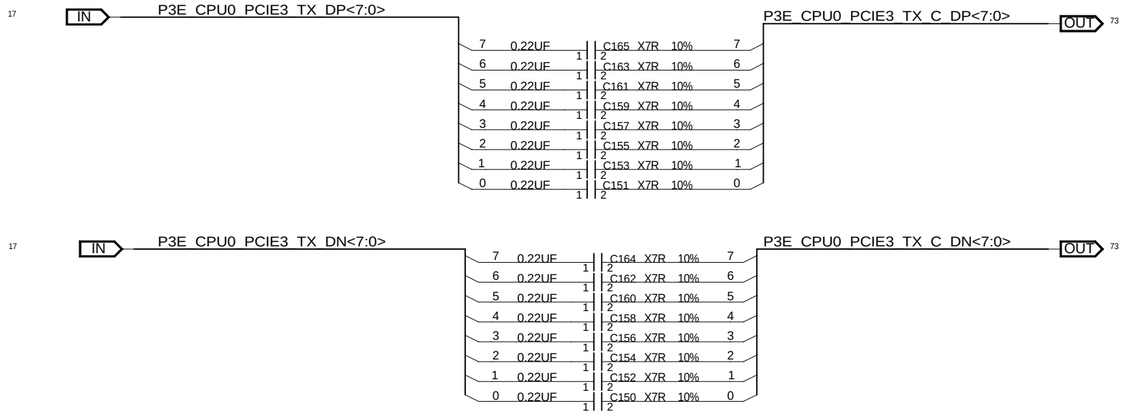



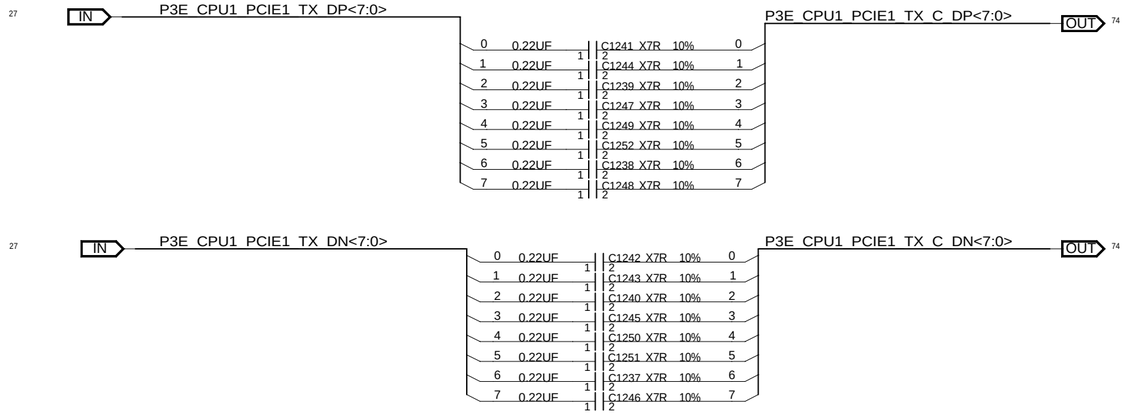

PCIE AC COUPLE CAPS - RISER2

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:53:25 2015 | SHEET 76 OF 188 |

# OCP MEZZ

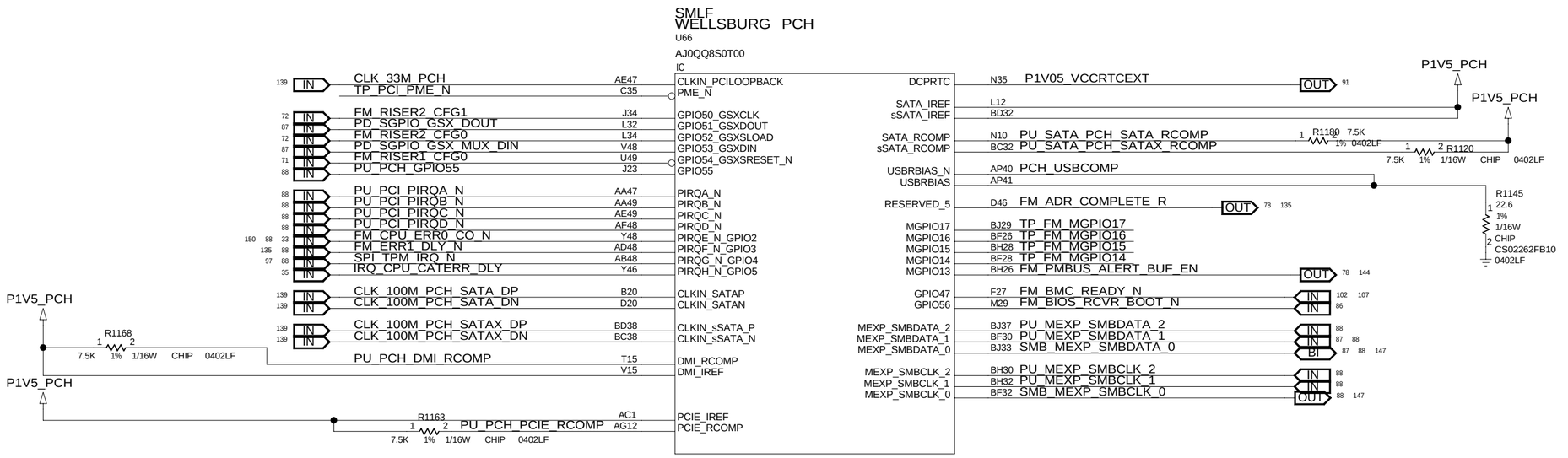


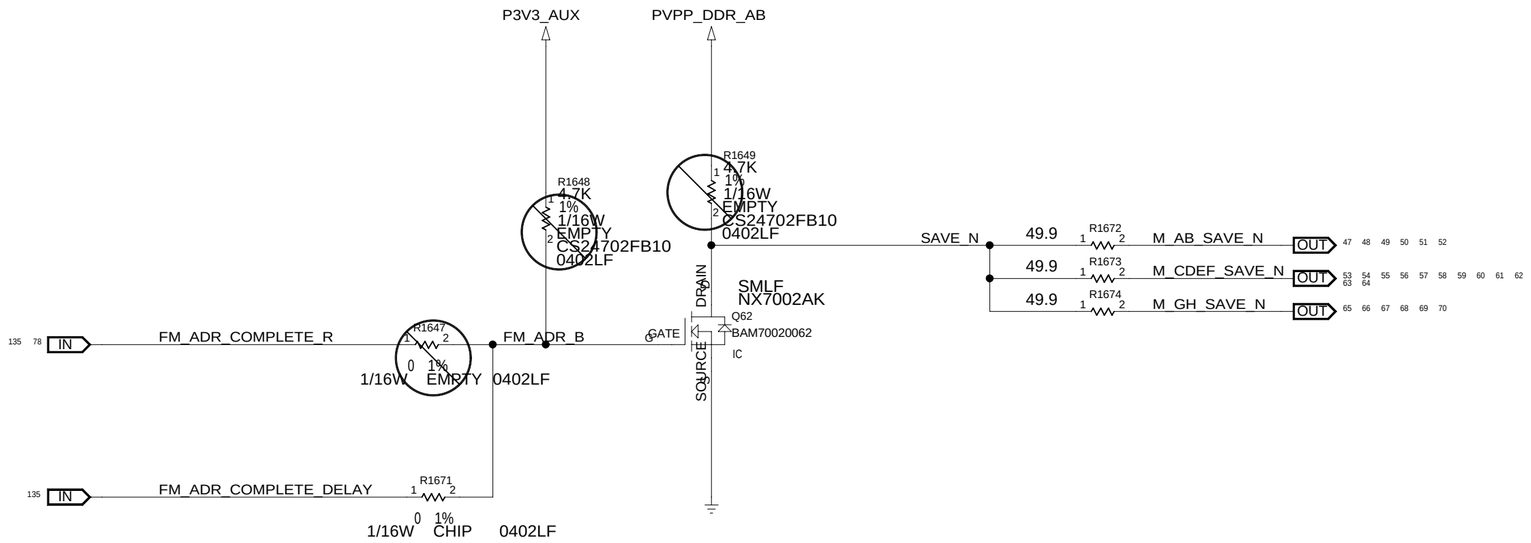

# PCIE SSD




# PCIE AC COUPLE CAPS - MEZZ&SSD

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:53:27 2015 | SHEET 77 OF 188 |






| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER PETER | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | | |
| | | REVIEWER PETER,RUNNER,MATT | SIZE C | DATE Mon Nov 16 11:53:29 2015 | SHEET 78 OF 188 | | |

U66
AJ0QQ8S0T00
IC

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 85 IN | DMI_CPU0_PCH_TX_C_DP<3> | L6 | DMI_RXP_3 | DMI_TXP_3 | F4 | DMI_CPU0_PCH_RX_DP<3> | OUT 85 |
| 85 IN | DMI_CPU0_PCH_TX_C_DN<3> | J6 | DMI_RXN_3 | DMI_TXN_3 | E2 | DMI_CPU0_PCH_RX_DN<3> | OUT 85 |
| 85 IN | DMI_CPU0_PCH_TX_C_DP<2> | N6 | DMI_RXP_2 | DMI_TXP_2 | H4 | DMI_CPU0_PCH_RX_DP<2> | OUT 85 |
| 85 IN | DMI_CPU0_PCH_TX_C_DN<2> | N7 | DMI_RXN_2 | DMI_TXN_2 | H2 | DMI_CPU0_PCH_RX_DN<2> | OUT 85 |
| 85 IN | DMI_CPU0_PCH_TX_C_DP<1> | T9 | DMI_RXP_1 | DMI_TXP_1 | K4 | DMI_CPU0_PCH_RX_DP<1> | OUT 85 |
| 85 IN | DMI_CPU0_PCH_TX_C_DN<1> | T7 | DMI_RXN_1 | DMI_TXN_1 | K2 | DMI_CPU0_PCH_RX_DN<1> | OUT 85 |
| 85 IN | DMI_CPU0_PCH_TX_C_DP<0> | T14 | DMI_RXP_0 | DMI_TXP_0 | M4 | DMI_CPU0_PCH_RX_DP<0> | OUT 85 |
| 85 IN | DMI_CPU0_PCH_TX_C_DN<0> | T12 | DMI_RXN_0 | DMI_TXN_0 | M2 | DMI_CPU0_PCH_RX_DN<0> | OUT 85 |
| R1164 10K 1% 1/16W CHIP 0402LF | TP_PCH_RSVD_3 | V10 | RESERVED_3 | CLKOUT_DMIP_0 | BD4 | TP_CLK_100M_PCH_CLKREF_R_DP | |
| R1165 10K 1% 1/16W CHIP 0402LF | TP_PCH_RSVD_2 | V12 | RESERVED_2 | CLKOUT_DMIN_0 | BE2 | TP_CLK_100M_PCH_CLKREF_R_DN | |
| | TP_PCH_PERP_8 | AU12 | PERP_8 | PETP_8 | AV4 | TP_PCH_PETP_8 | |
| | TP_PCH_PERN_8 | AU10 | PERN_8 | PETN_8 | AV2 | TP_PCH_PETN_8 | |
| | TP_PCH_PERP_7 | AU7 | PERP_7 | PETP_7 | AT2 | TP_PCH_PETP_7 | |
| | TP_PCH_PERN_7 | AU6 | PERN_7 | PETN_7 | AT4 | TP_PCH_PETN_7 | |
| | TP_PCH_PERP_6 | AP7 | PERP_6 | PETP_6 | AP2 | TP_PCH_PETP_6 | |
| | TP_PCH_PERN_6 | AP9 | PERN_6 | PETN_6 | AP4 | TP_PCH_PETN_6 | |
| | TP_PCH_PERP_5 | AP12 | PERP_5 | PETP_5 | AM2 | TP_PCH_PETP_5 | |
| | TP_PCH_PERN_5 | AP14 | PERN_5 | PETN_5 | AM4 | TP_PCH_PETN_5 | |
| | TP_PCH_PERP_4 | AM6 | PERP_4 | PETP_4 | AK2 | TP_PCH_PETP_4 | |
| | TP_PCH_PERN_4 | AM7 | PERN_4 | PETN_4 | AK4 | TP_PCH_PETN_4 | |
| | TP_PCH_PERP_3 | AM10 | PERP_3 | PETP_3 | AH2 | TP_PCH_PETP_3 | |
| | TP_PCH_PERN_3 | AM12 | PERN_3 | PETN_3 | AH4 | TP_PCH_PETN_3 | |
| | TP_PCH_USB3_03_RXP | AG15 | PERP_2_USB3RP_4 | PETP_2_USB3TP_4 | AF2 | TP_PCH_USB3_03_TXP | |
| | TP_PCH_USB3_03_RXN | AG14 | PERN_2_USB3RN_4 | PETN_2_USB3TN_4 | AF4 | TP_PCH_USB3_03_TXN | |
| 102 IN | PE_PCH_IBMC_RX_C_DP | AG7 | PERP_1_USB3RP_3 | PETP_1_USB3TP_3 | AD4 | PE_PCH_IBMC_TX_DP | |
| 102 IN | PE_PCH_IBMC_RX_C_DN | AG6 | PERN_1_USB3RN_3 | PETN_1_USB3TN_3 | AD2 | PE_PCH_IBMC_TX_DN | |
| | TP_PCH_USB3_05_RXP | AC9 | USB3RP_6 | USB3TP_6 | AB4 | TP_PCH_USB3_05_TXP | |
| | TP_PCH_USB3_05_RXN | AC7 | USB3RN_6 | USB3TN_6 | AB2 | TP_PCH_USB3_05_TXN | |
| | TP_PCH_USB3_04_RXP | AC12 | USB3RP_5 | USB3TN_5 | Y4 | TP_PCH_USB3_04_TXP | |
| | TP_PCH_USB3_04_RXN | AC14 | USB3RN_5 | USB3TN_5 | Y2 | TP_PCH_USB3_04_TXN | |
| 95 IN | USB3_01_RXP | AA15 | USB3RP_2 | USB3TP_2 | V4 | USB3_01_TXP | |
| 95 IN | USB3_01_RXN | AA14 | USB3RN_2 | USB3TN_2 | V2 | USB3_01_TXN | OUT 95 |
| 95 IN | USB3_00_RXP | AA6 | USB3RP_1 | USB3TP_1 | T4 | USB3_00_TXP | OUT 95 |
| 95 IN | USB3_00_RXN | AA7 | USB3RN_1 | USB3TN_1 | T2 | USB3_00_TXN | OUT 95 |
| 79 IN | PESSD_PRESENT_PCH_N | J44 | OC7_N_GPIO14 | USB2P_13 | AC38 | TP_USB2_13_DP | |
| 97 88 IN | FM_TPM_PRSNT_N | L43 | OC6_N_GPIO10 | USB2N_13 | AC36 | TP_USB2_13_DN | |
| 145 102 88 OUT | FP_PWR_LED_N R1188 0 1% 0402LF FP_PWR_LED_R1_N | G43 | OC5_N_GPIO9 | USB2P_12 | AC43 | TP_USB2_12_DP | |
| 94 IN | FM_USB_OC4_FP_R_N | G44 | OC4_N_GPIO43 | USB2N_12 | AC44 | TP_USB2_12_DN | |
| 107 103 IN | ROMA<0> R364 0 1% 0402LF FM_BMC_DISABLE | B42 | OC3_N_GPIO42 | USB2P_11 | AC41 | USB2_11_DP | |
| 88 IN | PU_USB_OC2_R_N | A37 | OC2_N_GPIO41 | USB2N_11 | AC40 | USB2_11_DN | BI 94 |
| 95 IN | FM_USB_OC1_BP_R_N | B38 | OC1_N_GPIO40 | USB2P_10 | AG35 | USB2_10_DP | BI 94 |
| 88 IN | PU_USB_OC0_R_N | J43 | OC0_N_GPIO59 | USB2N_10 | AG36 | USB2_10_DN | BI 94 |
| | | | | USB2P_9 | AG41 | USB2_PCH_P9_DP | BI 106 |
| | | | | USB2N_9 | AG40 | USB2_PCH_P9_DN | BI 106 |
| | | | | USB2P_8 | AG44 | USB_PCH_P8_DP | BI 106 |
| | | | | USB2N_8 | AG43 | USB_PCH_P8_DN | BI 106 |
| | | | | USB2P_7 | AM43 | TP_USB2_07_DP | |
| | | | | USB2N_7 | AM44 | TP_USB2_07_DN | |
| | | | | USB2P_6 | AJ43 | TP_USB2_06_DP | |
| | | | | USB2N_6 | AJ44 | TP_USB2_06_DN | |
| | | | | USB2P_5 | AJ41 | TP_USB2_05_DP | |
| | | | | USB2N_5 | AJ40 | TP_USB2_05_DN | |
| | | | | USB2P_4 | AM40 | TP_USB2_04_DP | |
| | | | | USB2N_4 | AM41 | TP_USB2_04_DN | |
| | | | | USB2P_3 | AP43 | TP_USB2_03_DP | |
| | | | | USB2N_3 | AP44 | TP_USB2_03_DN | |
| | | | | USB2P_2 | AJ35 | USB2_02_DP | BI 96 |
| | | | | USB2N_2 | AJ36 | USB2_02_DN | BI 96 |
| | | | | USB2P_1 | AY46 | USB2_01_DP | BI 96 |
| | | | | USB2N_1 | AY48 | USB2_01_DN | BI 96 |
| | | | | USB2P_0 | AV46 | TP_USB2_00_DP | |
| | | | | USB2N_0 | AV48 | TP_USB2_00_DN | |
| | | | CLKIN_DOT96P | | AM36 | CLK_96M_PCH_DP | IN 139 |
| | | | CLKIN_DOT96N | | AM35 | CLK_96M_PCH_DN | IN 139 |

CH4103K9B09
X5R 16V
10% 0.1UF C223 0402
1 2 PE_PCH_IBMC_TX_C_DP OUT 102
1 2 PE_PCH_IBMC_TX_C_DN OUT 102
10% 0.1UF C224 0402
X5R 16V
CH4103K9B09

FOR REAR USB3

P10,P11 FOR FRONT USB
P8,P9 FOR BMC

P1,P2 FOR REAR USB

88 IN

140 74 IN HP_LVC3_PESSD1_PWRGD R1818 0 1% 0402LF

140 74 IN HP_LVC3_PESSD0_PWRGD R1819 0 1% 0402LF

PESSD_PRESENT_N

SMLF
SN74LVC2G07DCKR
U188
AL002G07006
IC

| | | | |
|---|---|---|---|
| 1 | 1A | 1Y | 6 |
| 2 | GND | VCC | 5 |
| 3 | 2A | 2Y | 4 |

PESSD_PRESENT_PCH_R_N
PESSD_PRESENT_BMC_R_N

P3V3_AUX
C1639 0.1UF 16V 10% X5R CH4103K9B09 0402

P3V3_AUX
R1838 10K 5% 1/16W CHIP TMP_OCS31002JB28 0402LF

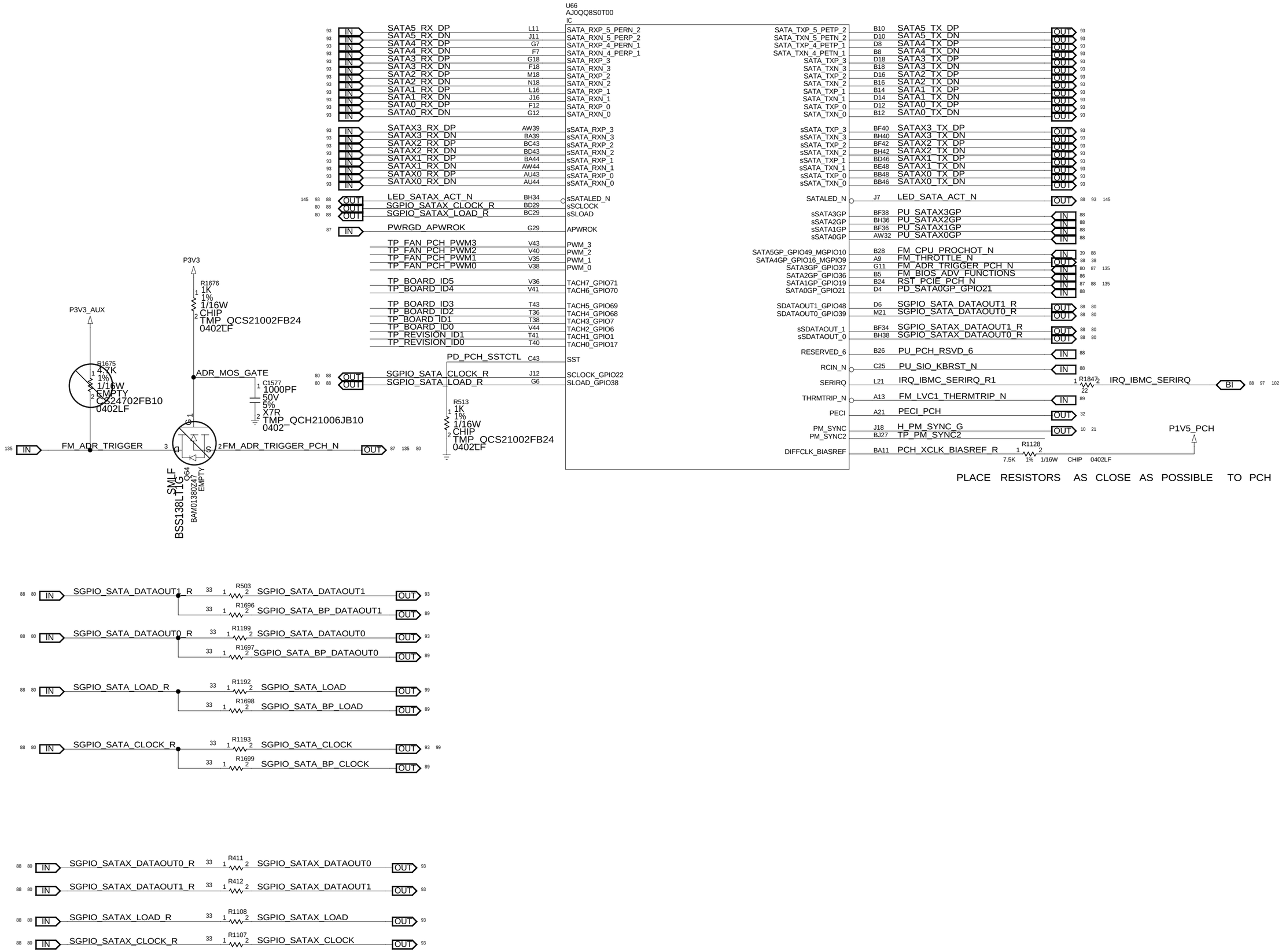
R1836 33
R1837 33

P3V3_AUX
R1839 10K 5% 1/16W CHIP TMP_OCS31002JB28 0402LF

PESSD_PRESENT_PCH_N OUT 79
PESSD_PRESENT_BMC_N OUT 102

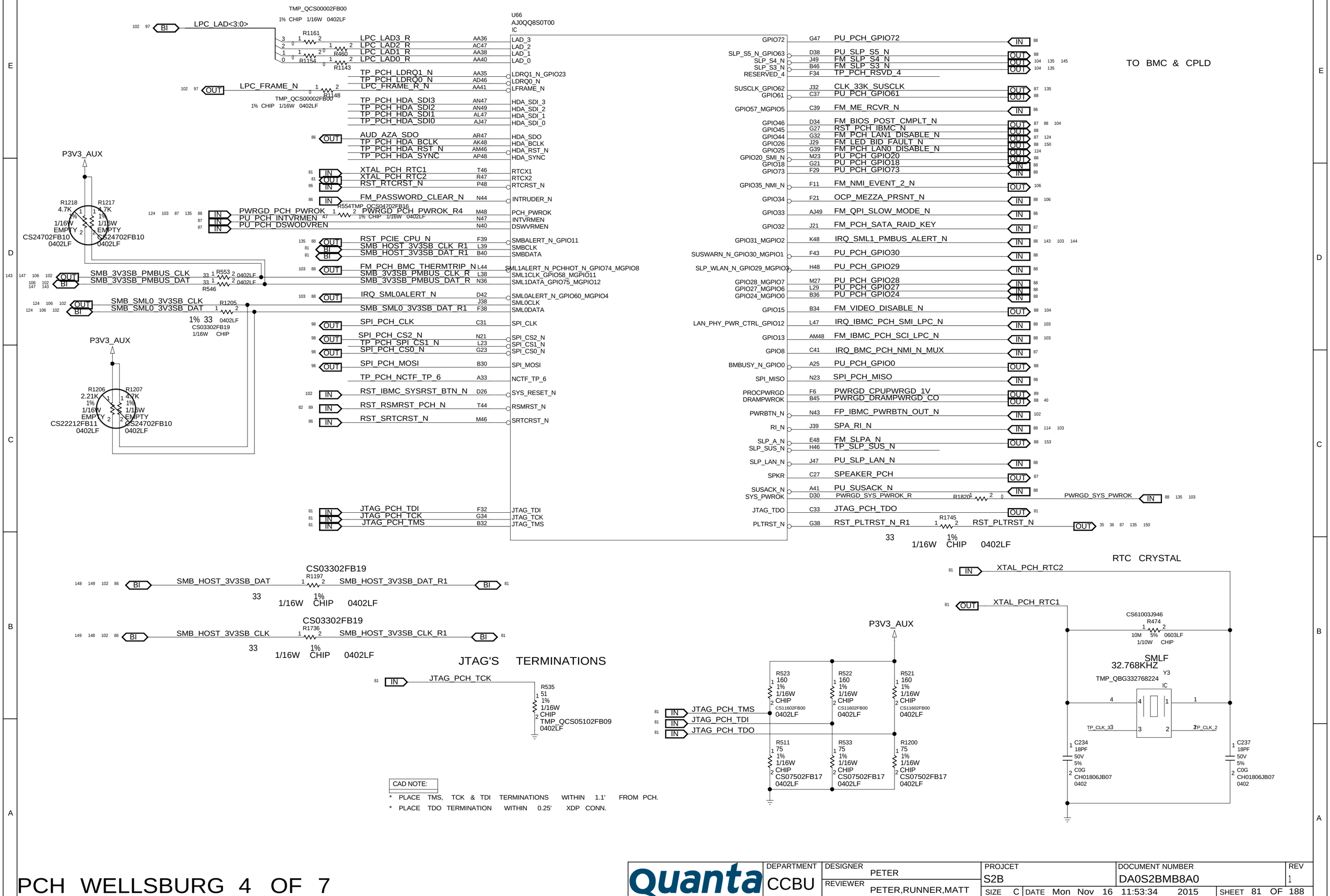
# PCH WELLSBURG 2 OF 7

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER PETER | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,RUNNER,MATT | SIZE C | DATE Mon Nov 16 11:53:30 2015 | SHEET 79 OF 188 |




# PCH WELLSBURG 3 OF 7

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER PETER | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER PETER,RUNNER,MATT | SIZE C | DATE Mon Nov 16 11:53:32 2015 | SHEET 80 OF 188 | |




PCH WELLSBURG 4 OF 7

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: PETER | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,RUNNER,MATT | SIZE: C DATE: Mon Nov 16 11:53:34 2015 | | SHEET: 81 OF 188 |

10K PULLDOWN RESISTORS FOR ISCLK

82 OUT CLK_14M_PCH

R958 10K 1% 1/16W CHIP TMP_QCS31002FB26 0402LF

U66
AJ0QQ8S0T00
IC

141 IN CLK_100M_DB1900_PCH_CPY_DP P4
141 IN CLK_100M_DB1900_PCH_CPY_DN P2
CLKIN_CPYP
CLKIN_CPYN

139 OUT CLK_100M_PCH_DB1900_R_DP AY2
139 OUT CLK_100M_PCH_DB1900_R_DN AY4
CLKOUT_DMIP_1
CLKOUT_DMIN_1

139 OUT CLK_100M_PCH_XDP_DP BD16
139 OUT CLK_100M_PCH_XDP_DN BC16
CLKOUT_ITPXDPP
CLKOUT_ITPXDPN

123 102 73 72 71 IN IRQ_LVC3_WAKE_N F44
WAKE_N

XTAL_PCH_25M_IN BA12
XTAL25_IN

CS51002FB11

R427 1M 1% 1/16W CHIP 0402LF

XTAL_PCH_25M_OUT AW12
XTAL25_OUT

SMLF 25MHZ
Y2
BG625000081
IC

C211 27PF 50V 5% NPO CH02706JB06 0402

C212 27PF 50V 5% NPO CH02706JB06 0402

CLKOUT_PCI_4 BF24 TP_CLKOUT_PCI_4
CLKOUT_PCI_3 BH24 TP_CLKOUT_PCI_3
CLKOUT_PCI_2 BF22 CLK_33M_PCH_BMC_LPC_R OUT 139
CLKOUT_PCI_1 BJ21 TP_CLKOUT_PCI_1
CLKOUT_PCI_0 BH22 CLK_33M_PCH_TPM OUT 139

CLKOUTFLEX3_GPIO67 BC23 SLOT1_PRESENT_N IN 71 88
CLKOUTFLEX2_GPIO66 BJ17 SLOT2_PRESENT_N IN 72 88
CLKOUTFLEX1_GPIO65 BD23 SLOT3_PRESENT_N IN 88
CLKOUTFLEX0_GPIO64 AW23 FM_RISER1_CFG1 IN 71

CLKOUTPCIEP_7 BD11 TP_CLKOUT_SRC_P7
CLKOUTPCIEN_7 BC11 TP_CLKOUT_SRC_N7
CLKOUTPCIEP_6 BB4 TP_CLKOUT_SRC_P6
CLKOUTPCIEN_6 BB2 TP_CLKOUT_SRC_N6
CLKOUTPCIEP_5 BH5 TP_CLKOUT_SRC_P5
CLKOUTPCIEN_5 BF6 TP_CLKOUT_SRC_N5
CLKOUTPCIEP_4 BH8 TP_CLKOUT_SRC_P4
CLKOUTPCIEN_4 BF8 TP_CLKOUT_SRC_N4
CLKOUTPCIEP_3 BH14 TP_CLKOUT_SRC_P3
CLKOUTPCIEN_3 BF14 TP_CLKOUT_SRC_N3
CLKOUTPCIEP_2 BH16 TP_CLKOUT_SRC_P2
CLKOUTPCIEN_2 BF16 TP_CLKOUT_SRC_N2
CLKOUTPCIEP_1 BH10 TP_CLKOUT_SRC_P1
CLKOUTPCIEN_1 BF10 TP_CLKOUT_SRC_N1
CLKOUTPCIEP_0 BC21 TP_CLKOUT_SRC_P0
CLKOUTPCIEN_0 BD21 TP_CLKOUT_SRC_N0

CLKOUT_GPB_PCIE_P0 BH12 TP_CLKOUT_PEG_AP
CLKOUT_GPB_PCIE_N0 BF12 TP_CLKOUT_PEG_AN

CLKOUT_GPB_PCIE_P1 BA18 TP_CLKOUT_PEG_BP
CLKOUT_GPB_PCIE_N1 BC18 TP_CLKOUT_PEG_BN

CLKOUT_GPB_PCIE_P2 BH20 TP_CLKOUT_PEG_CP
CLKOUT_GPB_PCIE_N2 BF20 TP_CLKOUT_PEG_CN

U66
AJ0QQ8S0T00
IC

98 OUT FM_BIOS_SPI_IO2 L27
98 OUT FM_BIOS_SPI_IO3 C29
SPI_IO2
SPI_IO3

82 IN CLK_14M_PCH BA23
REFCLK14IN

R1126 8.2K 1% 1/16W CHIP 0402LF
P1V5_PCH
PD_TD_IREF BC6
TD_IREF

AW11
ICLK_IREF

TP_RST_PLTRST_CPU_1V05_N A17
PLTRST_PROC_N

NC_DUT_DETECT_3 BH46 NC_PCH_DETECT_3
NC_DUT_DETECT_2 BF2 NC_PCH_DETECT_2
NC_DUT_DETECT_1 B4 NC_PCH_DETECT_1

DPWROK N41 PWRGD_DSW_P3V3_DPWROK

CGC_DUT_DETECT_N D48 FM_PCH_PRSNT_CO_N

0402LF TMP_QCS00002FB00
R508 1/16W 0 1% CHIP
RST_RSMRST_PCH_N IN 89 81
FM_PCH_PRSNT_CO_N OUT 135

P3V3_AUX
R1189 10K 1% 1/16W CHIP TMP_QCS31002FB26 0402LF

U66
AJ0QQ8S0T00
IC

R1100 1K 1% 1/16W EMPTY 0402LF

PD_PGDMON AH46

TP_PCH_NCTF_TP_1 V6
TP_PCH_NCTF_TP_0 V7
NCTF_TP_1
NCTF_TP_0

TP_PCH_NCTF_TP_4 AG10
TP_PCH_NCTF_TP_3 AG9
NCTF_TP_4
NCTF_TP_3

TP_PCH_NCTF_TP_11 BA7
TP_PCH_NCTF_TP_12 AW7
NCTF_TP_11
NCTF_TP_12

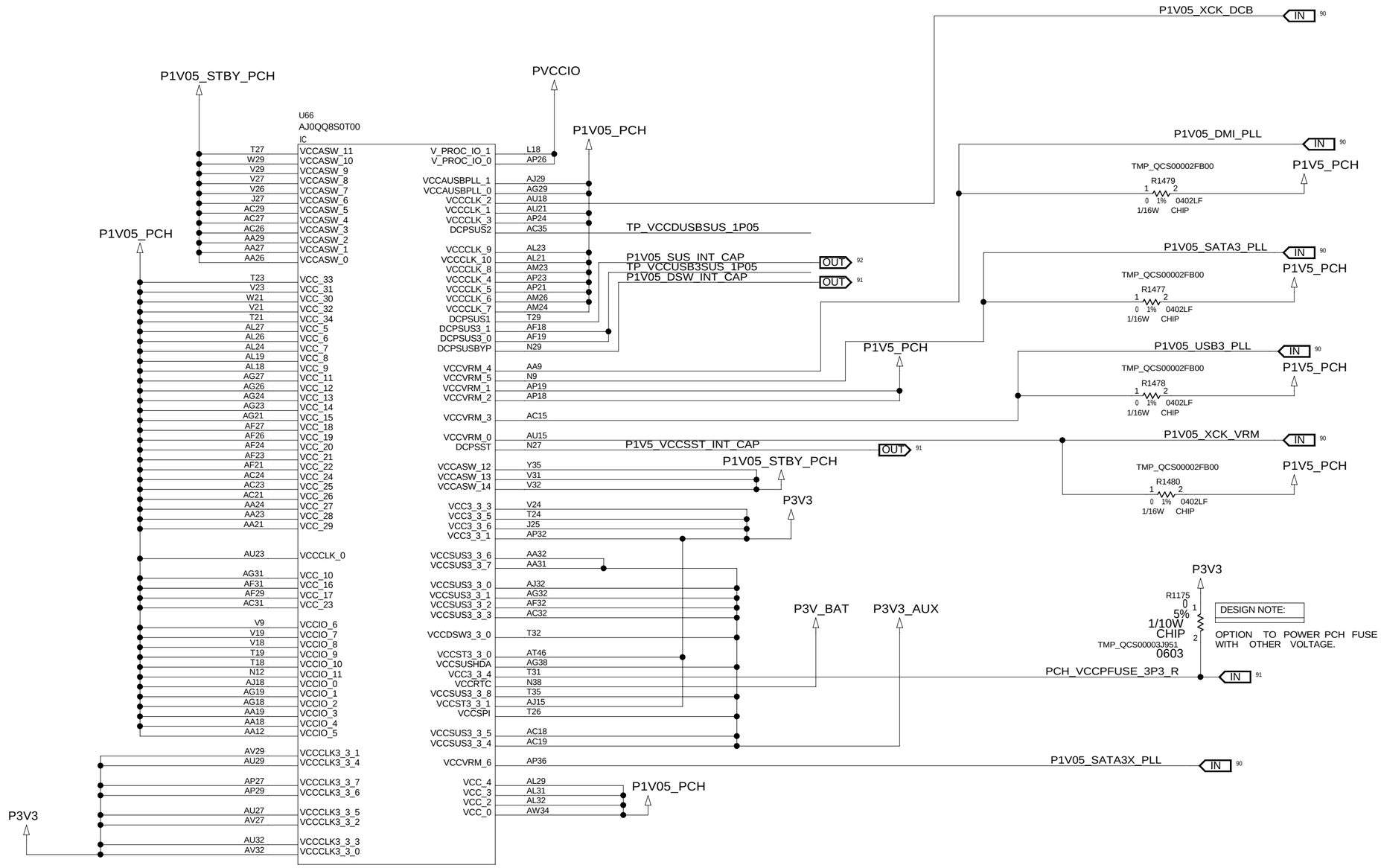
TP_PCH_RSVD_1 AW6
TP_PCH_RSVD_0 BA6
RESERVED_1
RESERVED_0

NCTF_TP_16 BD7 TP_PCH_NCTF_TP_16
NCTF_TP_15 BC7 TP_PCH_NCTF_TP_15
NCTF_TP_8 N14 TP_PCH_NCTF_TP_8
NCTF_TP_7 N15 TP_PCH_NCTF_TP_7
NCTF_TP_10 BC34 TP_PCH_NCTF_TP_10
NCTF_TP_9 BA34 TP_PCH_NCTF_TP_9
NCTF_TP_14 BH45 TP_PCH_NCTF_TP_14
NCTF_TP_13 BJ45 TP_PCH_NCTF_TP_13
NCTF_TP_2 N49 TP_PCH_NCTF_TP_2

# PCH WELLSBURG 5 OF 7

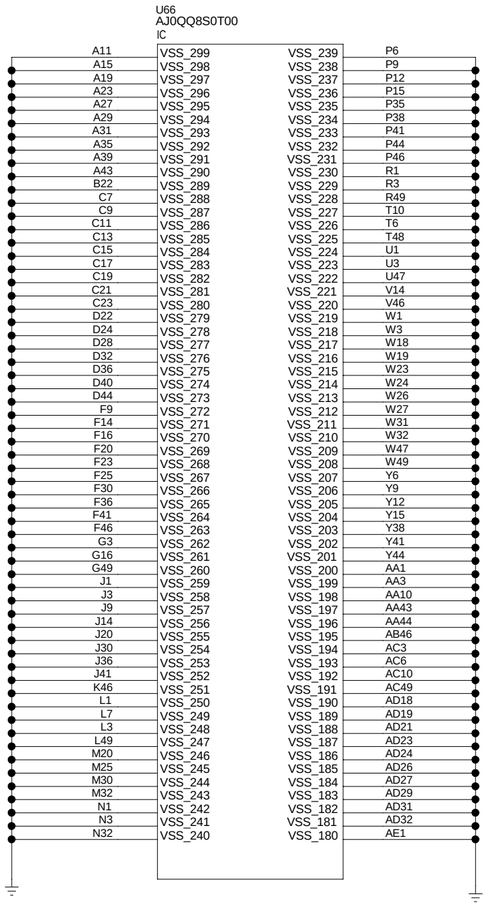
| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER PETER | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER PETER,RUNNER,MATT | SIZE C | DATE Mon Nov 16 11:53:36 2015 | SHEET 82 OF 188 | |

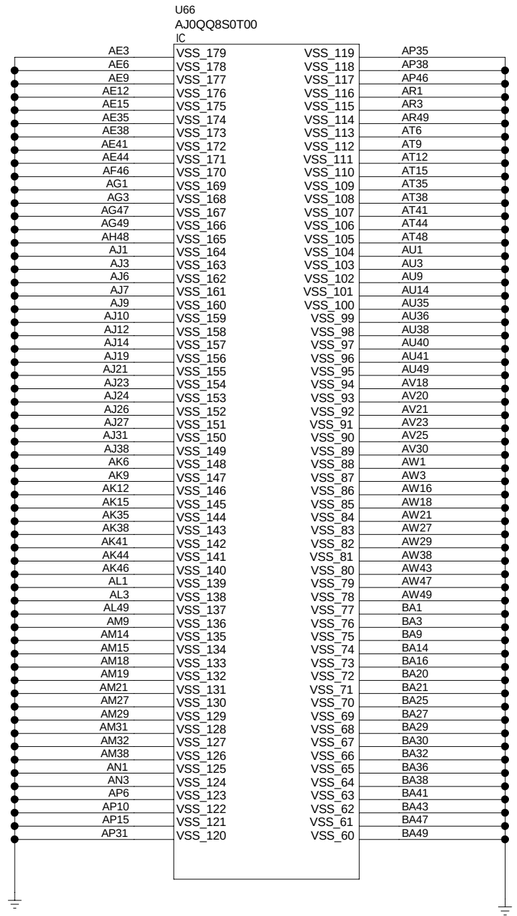
| | NOT FILTERED:(P1V5_PCH) | FILTERED:(P1V05) |
|---|---|---|
| STUFF | R1479,R1477,R1478,R1480,R1475 | L15,L33,L14,R1156,L31 |
| UNSTUFF | L15,L33,L14,R1156,L31 | R1479,R1477,R1478,R1480,R1475 |

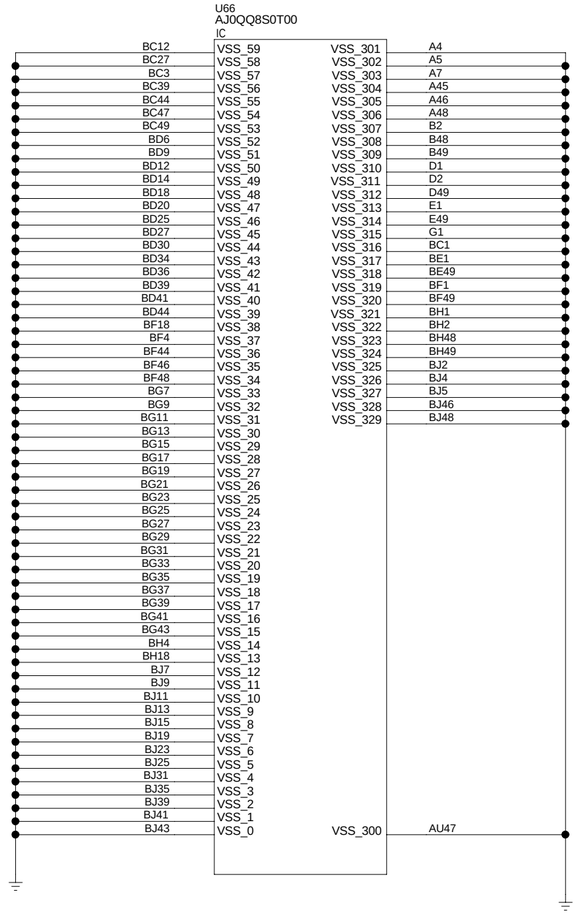



PCH WELLSBURG 6 OF 7

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: PETER | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,RUNNER,MATT | SIZE: C | DATE: Mon Nov 16 11:53:37 2015 | SHEET: 83 OF 188 |

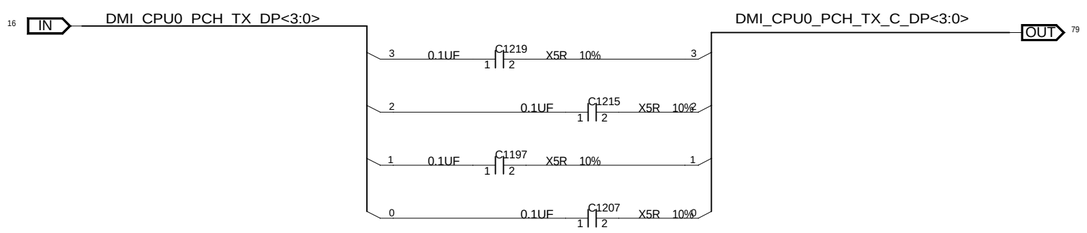


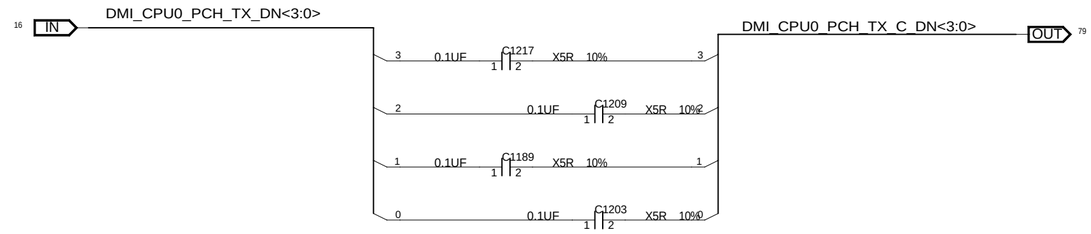




PCH WELLSBURG 7 OF 7

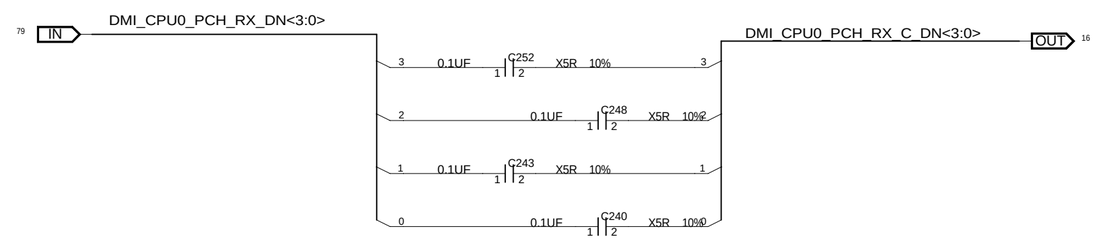
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER PETER | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,RUNNER,MATT | SIZE C | DATE Mon Nov 16 11:53:38 2015 | SHEET 84 OF 188 |







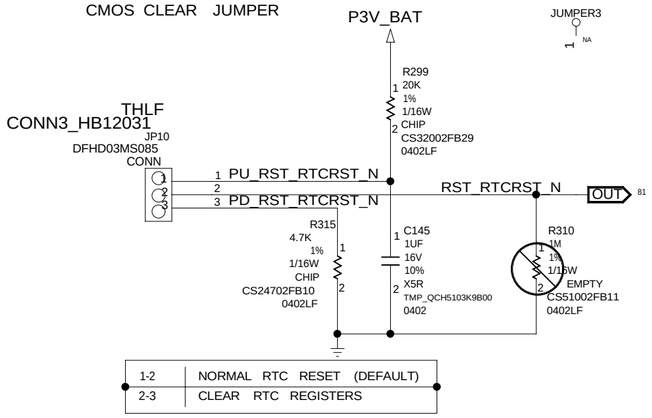



PCH WELLSBURG AC COUPLING

Quanta

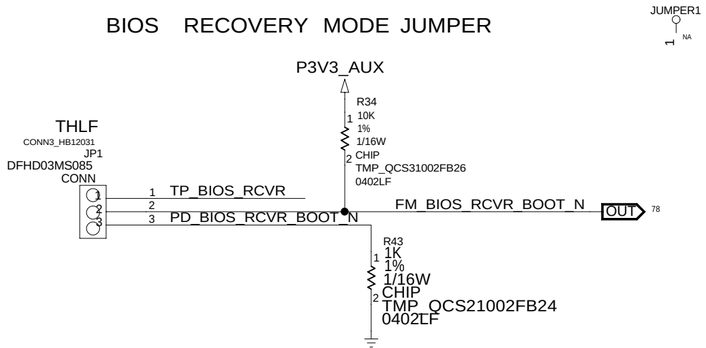
| | | | | |
|---|---|---|---|---|
| DEPARTMENT | DESIGNER | PROJCET | DOCUMENT NUMBER | REV |
| CCBU | PETER | S2B | DA0S2BMB8A0 | 1 |
| | REVIEWER PETER,RUNNER,MATT | SIZE C | DATE Mon Nov 16 11:53:39 2015 | SHEET 85 OF 188 |

## CMOS CLEAR JUMPER



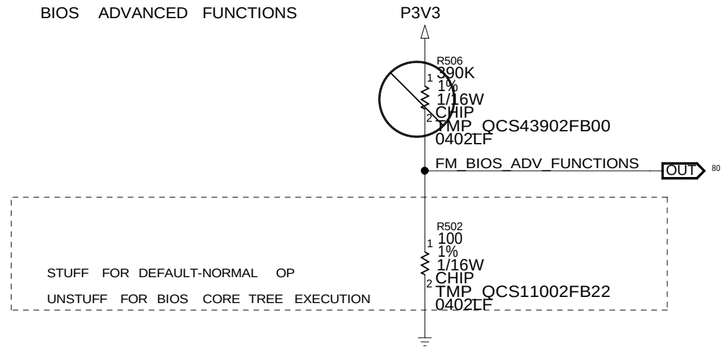

| | |
|---|---|
| 1-2 | NORMAL RTC RESET (DEFAULT) |
| 2-3 | CLEAR RTC REGISTERS |

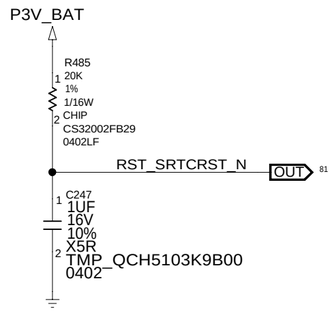
## BIOS RECOVERY MODE JUMPER



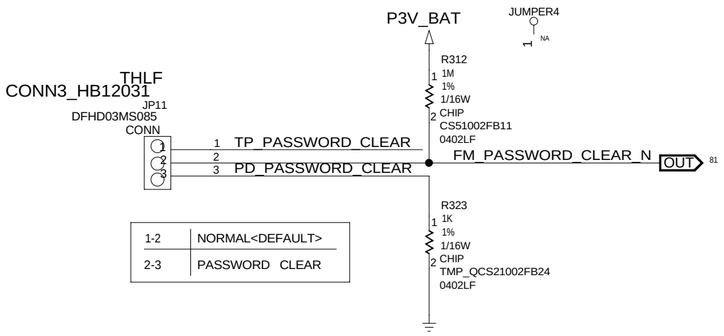

| | | |
|---|---|---|
| 1-2 | (DEFAULT) | NORMAL OPERATION |
| 2-3 | | RECOVER BIOS |

## BIOS ADVANCED FUNCTIONS



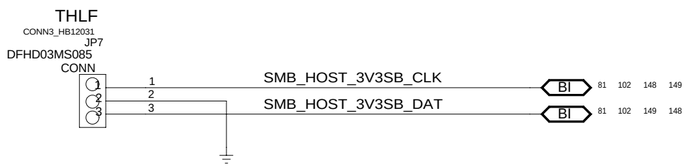




## PASSWORD CLEAR JUMPER

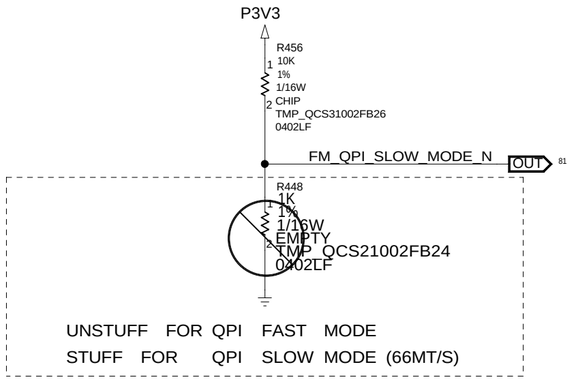



| | |
|---|---|
| 1-2 | NORMAL<DEFAULT> |
| 2-3 | PASSWORD CLEAR |

## ME <--> BMC DEBUG HEADER




## QPI SLOW MODE SELECT

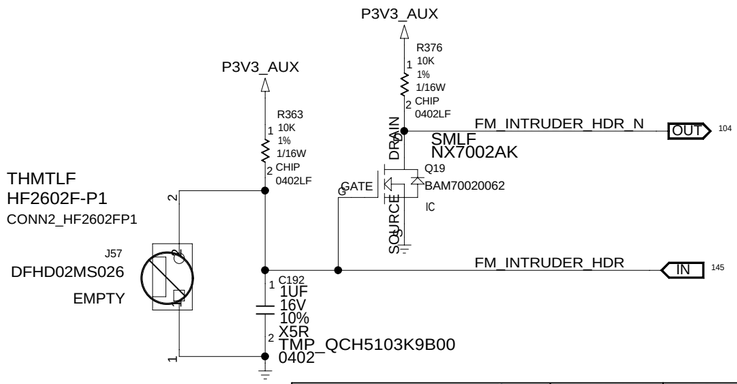



UNSTUFF FOR QPI FAST MODE
STUFF FOR QPI SLOW MODE (66MT/S)

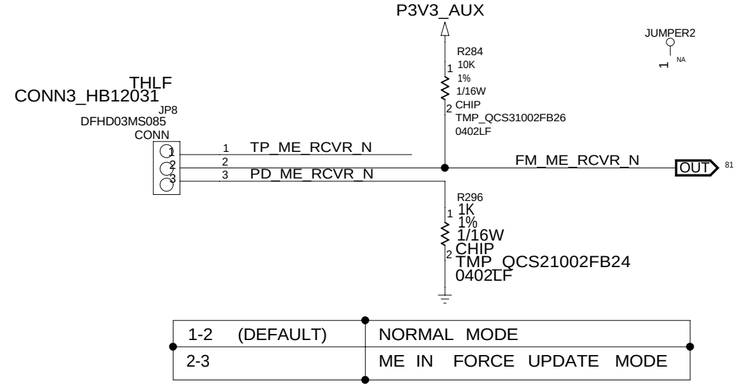
DMI TX TERMINATION
WHEN DC-COUPLED MODE:
0: DMI TX IS TERMINATED TO VSS
1: DMI TX IS TERMINATED TO VCC

INTERNAL PULL DOWN (9K-50K)
WHEN OPERATING IN AC-COUPLED MODE,
THIS STRAP HAS NO EFFECT ON THE TX TERMINATION

## INTRUDER DETECT

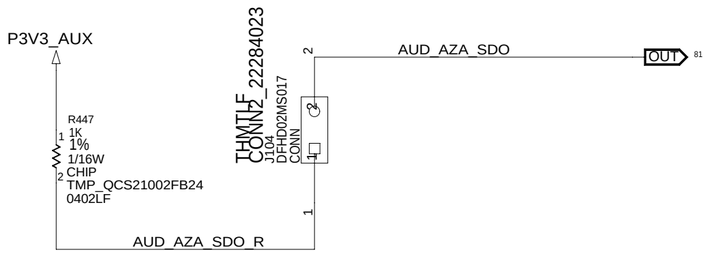



## ME FIRMWARE UPDATE




| | | |
|---|---|---|
| 1-2 | (DEFAULT) | NORMAL MODE |
| 2-3 | | ME IN FORCE UPDATE MODE |

## MFG MODE




# PCH WELLSBURG HEADER

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: PETER | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,RUNNER,MATT | SIZE: C | DATE: Mon Nov 16 11:53:40 2015 | SHEET: 86 OF 188 |

# WELLSBURG PIN STRAP SETTINGS

P3V3

CS23012FB16

R525 3.01K 1% 1/16W CHIP 0402LF

SPEAKER_PCH → OUT 81

REBOOT DISABLE WHEN HIGH

P3V3

R507 1K 1% 1/16W CHIP 0402LF

FM_ADR_TRIGGER_PCH_N → OUT 80 135

DESIGN NOTE:
TLS CONFIDENTIALITY ENABLE
ENABLED WHEN SAMPLED HIGH
DISABLED WHEN SAMPLED LOW
INTERNAL PULL DOWN (15K-40K)

P3V_BAT

TMP_QCS43902FB00

R478 390K 1% 1/16W CHIP 0402LF

PU_PCH_INTVRMEN → OUT 81

DESIGN NOTE:
INTERNAL VRM ENABLE:
THIS SIGNAL IS USED TO ENABLE OR DISABLE THE INTEGRATED 1.05 VOLTAGE REGULATORS FOR THE SUSPEND WELL ON THE WELLSBURG
P/U: ENABLED VR (DEFAULT)
P/D: DISABLES VR
P/D OPTION NOT BEING PROVIDED

CAD NOTE:
PLACE RES AS CLOSE AS POSSIBLE TO PCH

R1215 1K 1% 1/16W EMPTY 0402LF

CLK_33K_SUSCLK → OUT 81 135

DESIGN NOTE:

PLL ON-DIE VOLTAGE REGULATOR ENABLE
ENABLED WHEN SAMPLED HIGH
DISABLED WHEN SAMPLED LOW
WEAK INTERNAL PULL-UP (15K - 40K)

P3V_BAT

TMP_QCS43902FB00

R1183 390K 1% 1/16W CHIP 0402LF

PU_PCH_DSWODVREN → OUT 81

R1179 1K 1% 1/16W EMPTY 0402LF

DESIGN NOTE:
DSWODVREN: DEEP SLEEP WELL ON-DIE VOLTAGE REGULATOR ENABLE-
P/U: DSW ODVR IS ENABLED (DEFAULT)
P/D: DSW ODVR IS DISABLED

TMP_QCS21002FB24

R470 1K 1% 1/16W CHIP 0402LF

PD_SGPIO_GSX_MUX_DIN → OUT 78

DMI AC MODE WHEN STRIPPED LOW (DEFAULT)
DMI DC MODE WHEN STRIPPED HIGH

R405 100 1% 1/16W EMPTY 0402LF

PU_MEXP_SMBDATA_1 → OUT 88 78

LT KEY DOWNGRADE
P/U : LT DEBUG MODE IS DISABLED WHEN PULLED HIGH (DEFAULT).
P/D : LT DEBUG MODE IS ENABLED WHEN PULLED LOW.
THIS PIN IS SHARED WITH MEXP_BMDATA1. IF THIS FEATURE NEEDS TO BE ENABLED.

R520 1K 1% 1/16W EMPTY 0402LF

FM_BIOS_POST_CMPLT_N → OUT 81 88 104

JTAG CLK FILTER BYPASS.
P/U: JTAG CLK FILTER IS NOT BYPASSED
P/D: JTAG CLK FILTER IS BYPASSED

R1194 1K 1% 1/16W EMPTY 0402LF

FM_PCH_LAN1_DISABLE_N → OUT 81 124

RING OSCILLATOR BYPASS.
P/U: RING OSCILLATOR BYPASS IS DISABLED (DEFAULT)
P/D: RING OSCILLATOR BYPASS IS ENABLED.

R542 1K 1% 1/16W EMPTY 0402LF

PD_SGPIO_GSX_DOUT → OUT 78

R552 1K 1% 1/16W EMPTY 0402LF

RST_PCIE_PCH_N → OUT 88 80 135

R399 100 1% 1/16W EMPTY 0402LF

SMB_MEXP_SMBDATA_0 → OUT 78 88 147

ADR TIMER HOLD OFF
P/U : ADR TIMER HOLD OFF IS DISABLED WHEN PULLED HIGH (DEFAULT).
P/D : ADR TIMER HOLD OFF IS ENABLED WHEN PULLED LOW.

SW RAID OPTION ROM SELECTION

P3V3

THMTLF CONN2_22284023
JP18 DFHD02MS017 CONN

R599 2.21K 1% 1/16W CHIP CS22212FB11 0402LF

FM_PCH_SATA_RAID_KEY_R

R600 33 1% 0402LF CS03302FB19

FM_PCH_SATA_RAID_KEY → OUT 81

BOOT BIOS STRAPS (BBS)

| GNT[1]_GSXDOUT BBS[1] | SATA1GP_GP19 BBS[0] | |
|---|---|---|
| 0 | 0 | LPC |
| 0 | 1 | NAND |
| 1 | 0 | PCI |
| 1 | 1 | SPI |

P3V3_AUX

NC7SB3157P6X
I183
NC7SB3157P6X
U69
ALSB3157000
IC

C245 0.1UF 16V 10% X5R CH4103K9B09 0402

R492 1K 1% 1/16W EMPTY 0402LF

IRQ_BMC_PCH_NMI_N → B1
PD_INTEGRATED_CLK_DIS → B0
GND
S → RST_PLTRST_N → IN 81 35 36 135 150
VCC
A → IRQ_BMC_PCH_NMI_N_MUX → OUT 81

INTEGRATED CLOCK CHIP DISABLE.
ENABLED WHEN SAMPLED LOW.
INTERNAL PULL-UP (15K-40K).

PWRGD_P1V05_PCH_STBY_DLY → IN 135 88

R547 0 1% 1/16W CHIP TMP_QCS00002FB00 0402LF

PWRGD_APWROK → OUT 80

R534 0 1% 1/16W EMPTY TMP_QCS00002FB00 0402LF

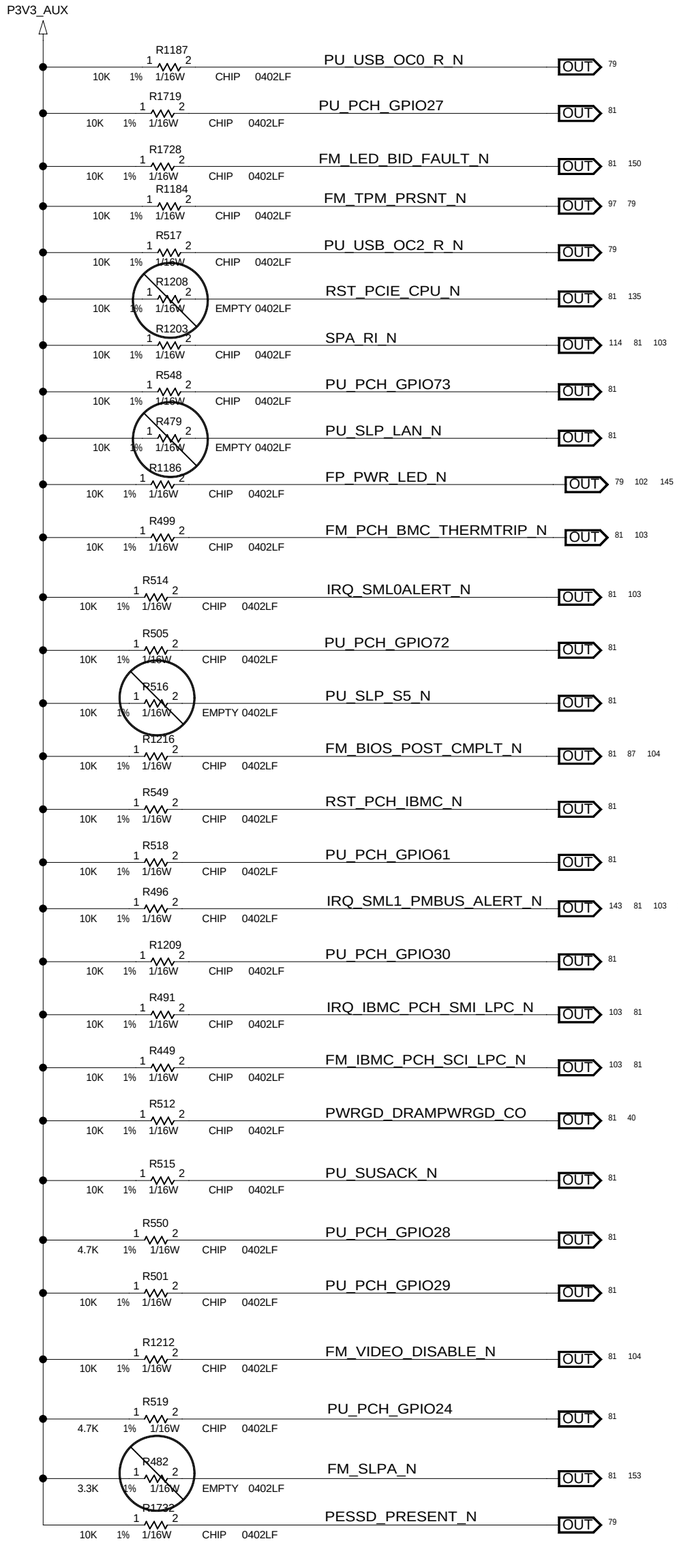
PWRGD_PCH_PWROK → IN 124 103 81 135 88

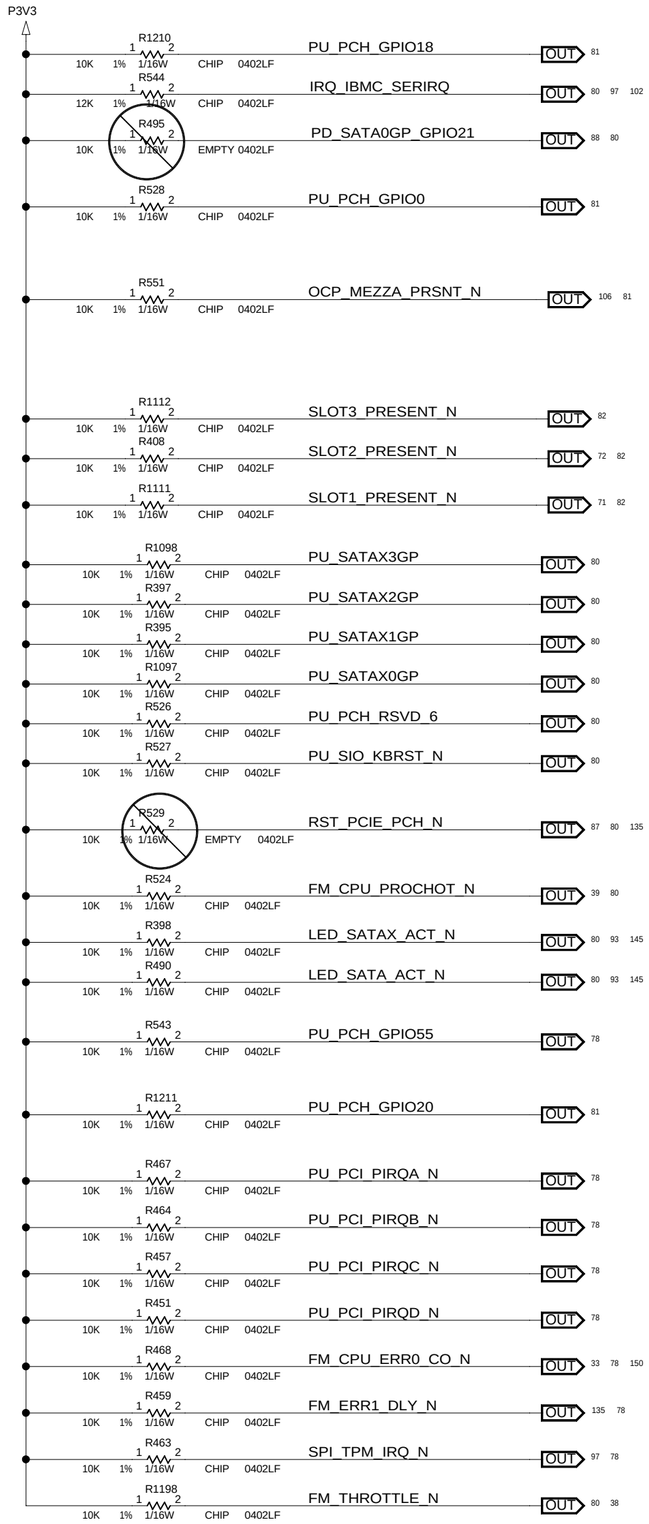
CONNECT PWRGD_APWROK TO PWRGD_P1V05_PCH_STBY_DLY FOR NORMAL OPERATION.

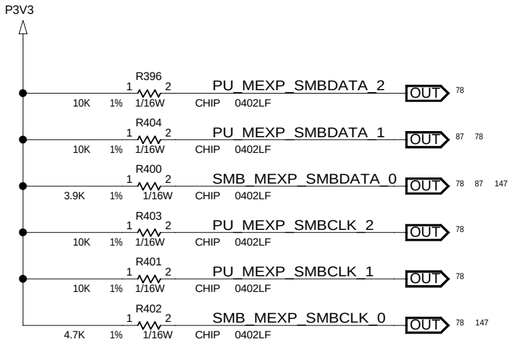
# PCH WELLSBURG STRAPPING

| | | | | |
|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: PETER | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 REV: 1 |
| | | REVIEWER: PETER,RUNNER,MATT | SIZE: C DATE: Mon Nov 16 11:53:42 2015 | SHEET 87 OF 188 |

# WBG PULL UPS




CAD NOTE: PLACE SGPIO PULL UPS WITHIN 2" FROM WBG




FOLLOW INTEL TME DIRECTION FOR KEEP PU 3.3K FOR SLP_A# SAME AS CRB

# PCH WELLSBURG PU AND PD

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER PETER | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,RUNNER,MATT | SIZE C | DATE Mon Nov 16 11:53:43 2015 | SHEET 88 OF 188 |

# RTC POWER-WELL ISOLATION

I40

ADM809SARTZ-REEL7

ADM809SARTZ-REEL7

U70

P3V3_AUX

AL0008090R3

IC

GND

VCC

RESET*

C255 0.1UF 16V 10% X5R CH4103K9B09 0402

R1191 100K 1% 1/16W CHIP 0402LF

P3V3_AUX

R1201 4.7K 1% 1/16W CHIP 0402LF

C1233 0.01UF 25V 10% X7R TMP_QCH31004KB17 0402

RST_RSMRST_R_N

CS12002FB25

R1190

200 1% 1/16W CHIP 0402LF

RST_RSMRST_N

OUT 104 111 135

C1229 100PF 50V 5% NPO CH11006JB00 0402

METR3906-G SMLF BA039060015 Q31 IC

RST_RSMRST_PCH_N

OUT 81 82

R510 10K 1% 1/16W CHIP 0402LF

SMLF BAV99S U71 BC000099069 IC

RST_RSMRST_BAV99_1

RST_RSMRST_BAV99_2

TP_BAV99_5

TP_BAV99_6

RST_RSMRST_BAV99_3

R1204 2.21K 1% 1/16W CHIP CS22212FB11 0402LF

PVCCIO

R531 200 1% 1/16W CHIP CS12002FB25 0402LF

FM_LVC1_THERMTRIP_N

OUT 80

SMLF METR3904-G Q32 BA039040020 IC

THERMTRIP DELAY ON CPLD:
MIN 500US, MAX 1MS

135 IN FM_LVC3_THERMTRIP_DLY

CS21502FB14 R539 1.5K 1% 1/16W CHIP 0402LF

FM_LVC3_THERMTRIP_DLY_R

P3V3_AUX

R530 4.7K 1% 1/16W CHIP CS24702FB10 0402LF

P3V3_AUX

R1202 2K 1% 1/16W CHIP TMP_QCS22002FB19 0402LF

PWRGD_CPUPWRGD

OUT 135

PWRGD_CPUPWRGD_NPN

SMLF MBT3904DW1T1G Q30 IC BA039040080

CS21502FB14

81 IN PWRGD_CPUPWRGD_1V

R1196 1% 1.5K 0402LF CHIP 1/16W

PWRGD_CPUPWRGD_R

SMLF MBT3904DW1T1G Q30 IC

---

P3V3

C1584 0.1UF 16V 10% X5R 0402

R1700 10K 1% 1/16W CHIP 0402LF

R1702 10K 1% 1/16W CHIP 0402LF

72 136 135 IN RST_PERST1_N

80 IN SGPIO_SATA_BP_DATAOUT1 INA

U178 QN-ALLVC007K01 IC SMLF SN74LVC07APWR

SGPIO_SATA_BP_BUF_DATAOUT1

CS03302FB19 R1704 33 1% 1/16W CHIP 0402LF

SGPIO_SATA_BP_BUF_DATAOUT1_R

80 IN SGPIO_SATA_BP_DATAOUT0 INB

SGPIO_SATA_BP_BUF_DATAOUT0

CS03302FB19 R1705 33 1% 1/16W CHIP 0402LF

SGPIO_SATA_BP_BUF_DATAOUT0_R

R1701 10K 1% 1/16W CHIP 0402LF

R1703 10K 1% 1/16W CHIP 0402LF

80 IN SGPIO_SATA_BP_LOAD INC

SGPIO_SATA_BP_BUF_LOAD

CS03302FB19 R1706 33 1% 1/16W CHIP 0402LF

SGPIO_SATA_BP_BUF_LOAD_R

80 IN SGPIO_SATA_BP_CLOCK IND

SGPIO_SATA_BP_BUF_CLOCK

CS03302FB19 R1707 33 1% 1/16W CHIP 0402LF

SGPIO_SATA_BP_BUF_CLOCK_R

THLF CONN5_HF5505EP1 J101 DFHD05MS030 IO

11 INE

SGPIO_SATA_BP_BUF_DATAOUT1_R

SGPIO_SATA_BP_BUF_DATAOUT0_R

SGPIO_SATA_BP_BUF_LOAD_R

SGPIO_SATA_BP_BUF_CLOCK_R

13 INF

P3V3

R1766 10K 1% 1/16W CHIP 0402LF

R1767 10K 1% 1/16W CHIP 0402LF

U178 QN-ALLVC007K01 IC SMLF SN74LVC07APWR

RST_PERST1_PESSD0_R_N

CS02202FB12 R1855 22 1% 1/16W CHIP 0402LF

RST_PERST1_PESSD0_N

OUT 74

RST_PERST1_PESSD1_R_N

CS02202FB12 R1856 22 1% 1/16W CHIP 0402LF

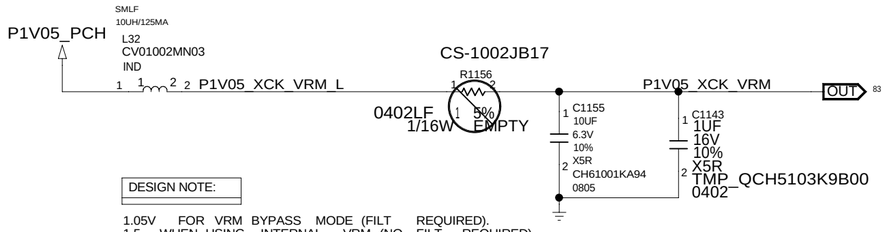
RST_PERST1_PESSD1_N

OUT 74

# PCH WELLSBURG MISC/SGPIO

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER PETER | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | | |
| | | REVIEWER PETER,RUNNER,MATT | SIZE C | DATE Mon Nov 16 11:53:45 2015 | SHEET 89 OF 188 | | |

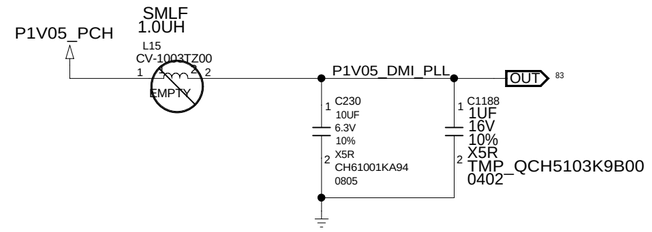
# P1V05_XCK_VRM - CLOCK INTEGRATION




DESIGN NOTE:

1.05V FOR VRM BYPASS MODE (FILT REQUIRED).
1.5 WHEN USING INTERNAL VRM (NO FILT REQUIRED).
THIS POWER IS SUPPLIED WITH CORE WELL.

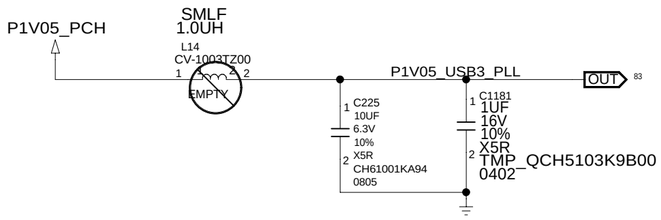
# DMI PLL FILTER
# 1.05V PCIE/DMI SECTION




CAD NOTE:

PLACE CAP BOARDCAP
STYLE NEAR TO PIN.

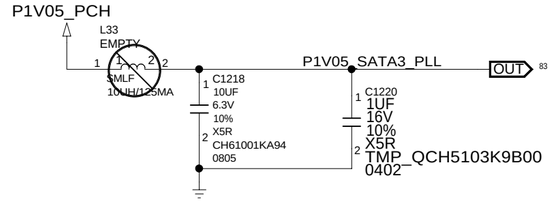
# USB3 PLL FILTER




DESIGN NOTE:

1.05V FOR VRM BYPASS MODE (FILT REQUIRED).
1.5 WHEN USING INTERNAL VRM (NO FILT REQUIRED).
THIS POWER IS SUPPLIED WITH CORE WELL.

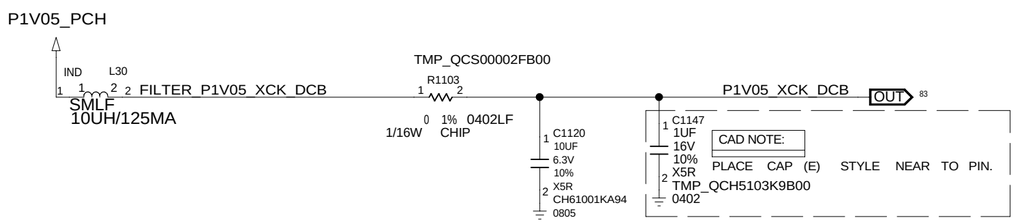
# SATA PLL FILTER




DESIGN NOTE:

1.05V FOR VRM BYPASS MODE (FILT REQUIRED).
1.5 WHEN USING INTERNAL VRM (NO FILT REQUIRED).
THIS POWER IS SUPPLIED WITH CORE WELL.

# P1V05_XCK_DCB - CLOCK INTEGRATION



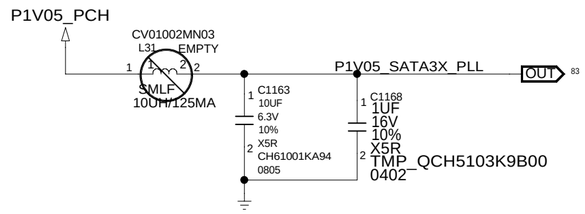

CAD NOTE:

PLACE CAP (E) STYLE NEAR TO PIN.

DESIGN NOTE:

FC RW10: REMOVE THE INDUCTOR
REPLACE WITH RES A93552-002
EMPTY CAP 10UF
ALLOWS FOR BYPASS OPTION WITH DISCRETE CAP.

# SATAX PLL FILTER




DESIGN NOTE:

1.05V FOR VRM BYPASS MODE (FILT REQUIRED).
1.5 WHEN USING INTERNAL VRM (NO FILT REQUIRED).
THIS POWER IS SUPPLIED WITH CORE WELL.

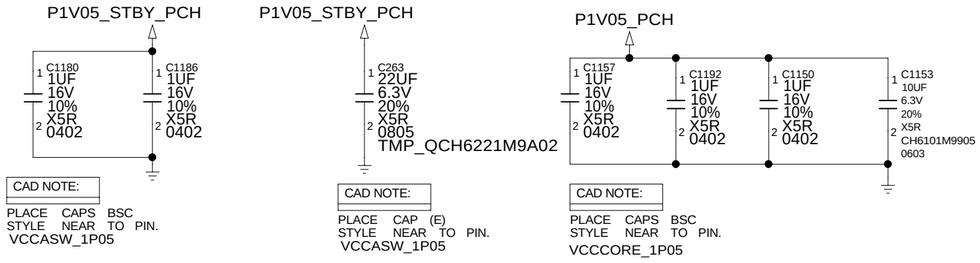
CAD NOTE:

PUT L & C AS CLOSE AS POSSIBLE WITH THE 10MIL TRACE MAX LENGTH OF 240MIL
A MINIMUM TRACE WIDTH OF 35MIL IS REQUIRED TO INTERCONNECT THE RESISTANCES

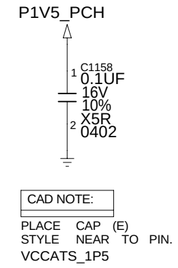
# PCH WELLSBURG FILTERING

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: PETER | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: PETER,RUNNER,MATT | SIZE: C | DATE: Mon Nov 16 11:53:47 2015 | SHEET: 90 OF 188 | |

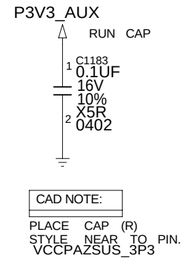
## 1.05V CORE/ASW/SUS FOR CORE SECTION



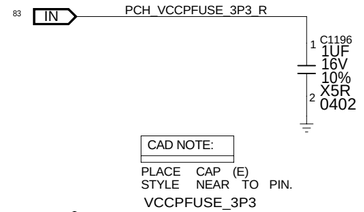

## 1.5V TSENSE



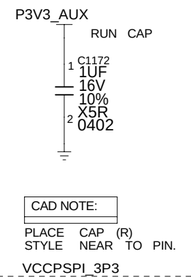

## 3.3V SUS AZA SECTION



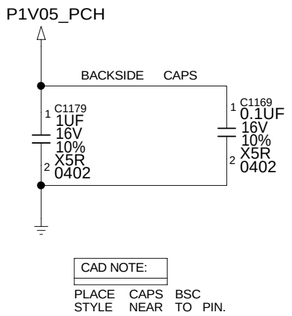

## 3.3V FUSE SECTION



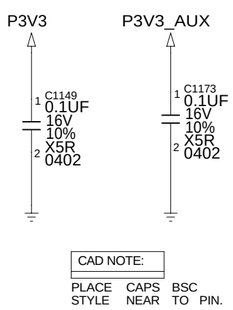

## 3.3V SPI SECTION



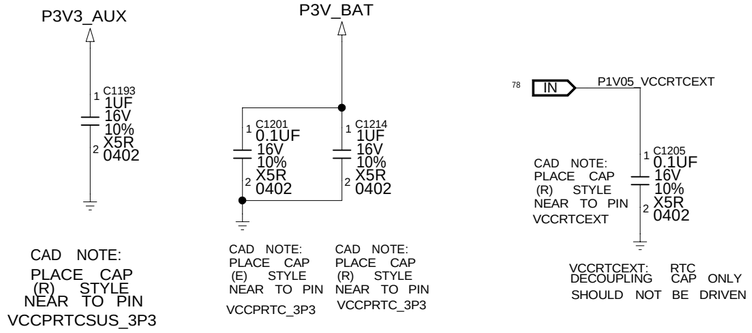

## 1.05V CORE USB2 SECTION



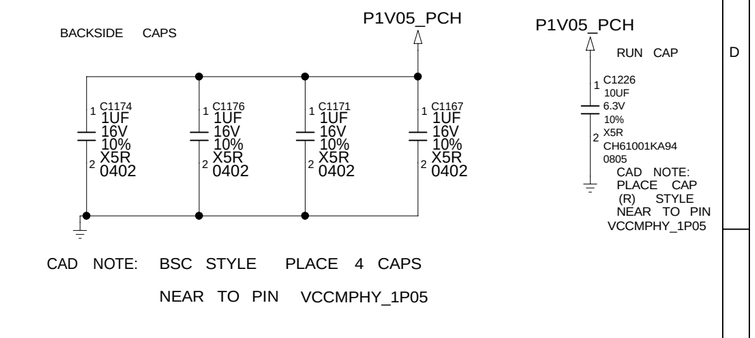

## 3.3 CORE/SUS USB2 SECTION




## 3.3V DSW/RTC FOR RTC SECTION



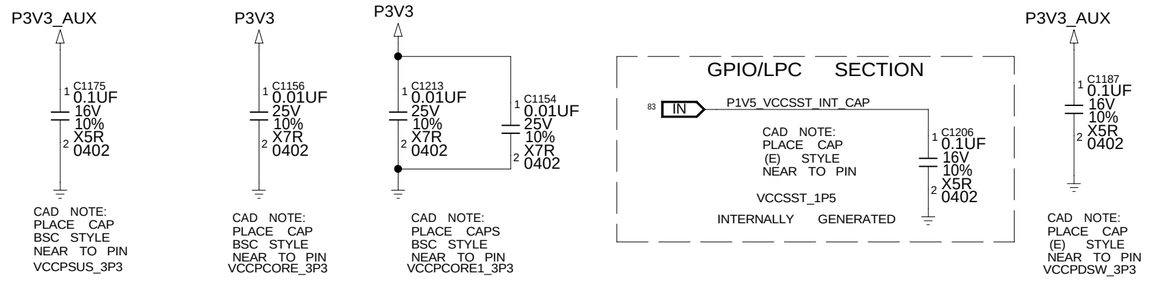

## 1.05V PCIE/DMI/SATA SECTION

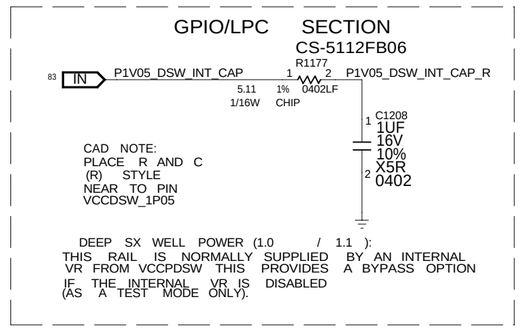



## 3.3V CORE THERMAL SENSOR

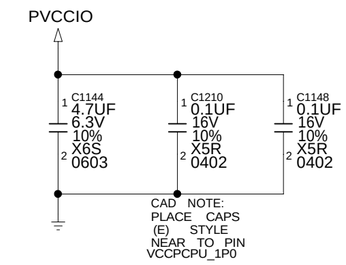



## 3.3V SUS/DSW/CORE FOR GPIO/LPC SECTION




## VCCIO2PCH FOR CPU SECTION




CAD NOTE:

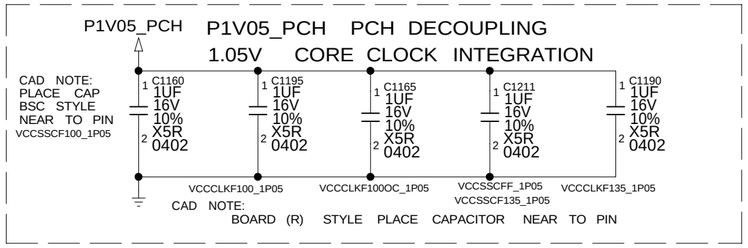
BSC: BACK SIDE COMPONENT

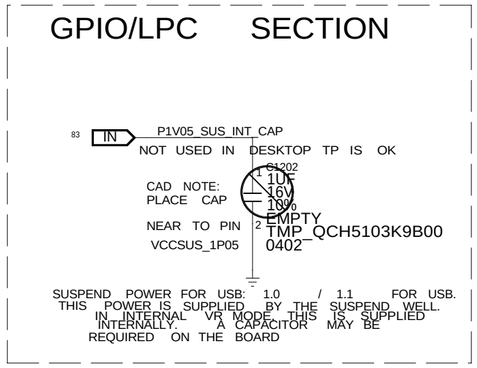
E: EDGE

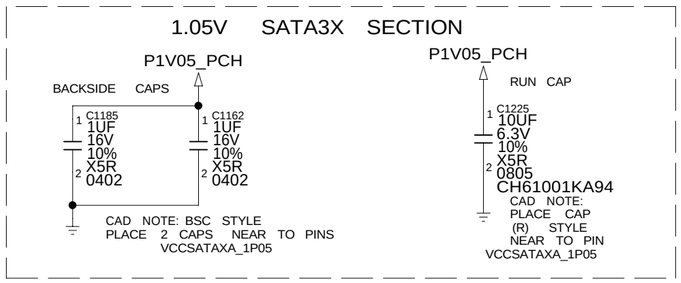
R: RUN

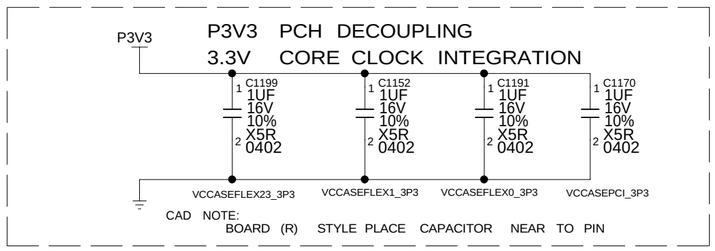
# PCH WELLSBURG DECOUPLING 1 OF 2

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: PETER | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,RUNNER,MATT | SIZE: C | DATE: Mon Nov 16 11:53:48 2015 | SHEET: 91 OF 188 |



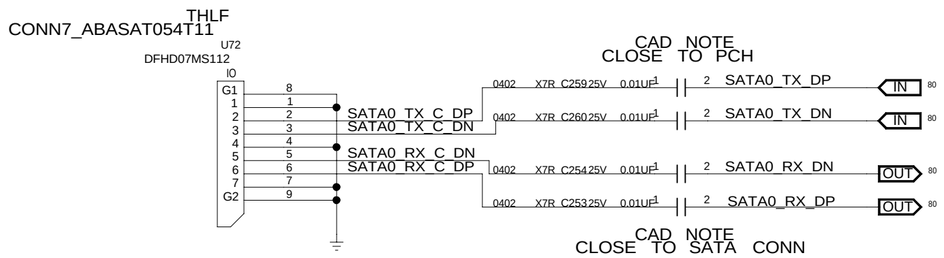



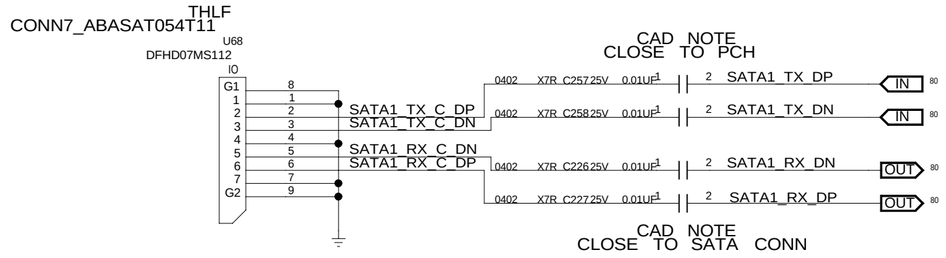



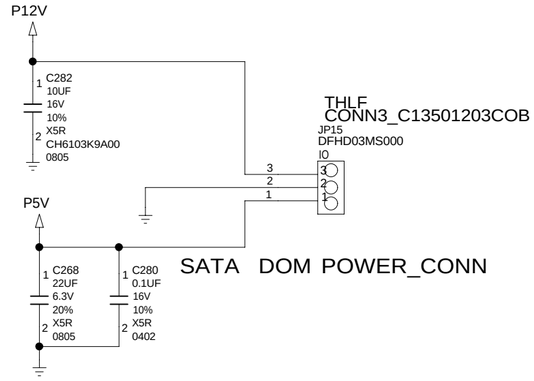



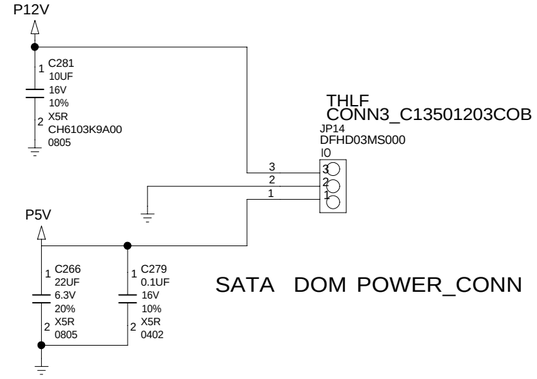

# PCH WELLSBURG DECOUPLING 2 OF 2

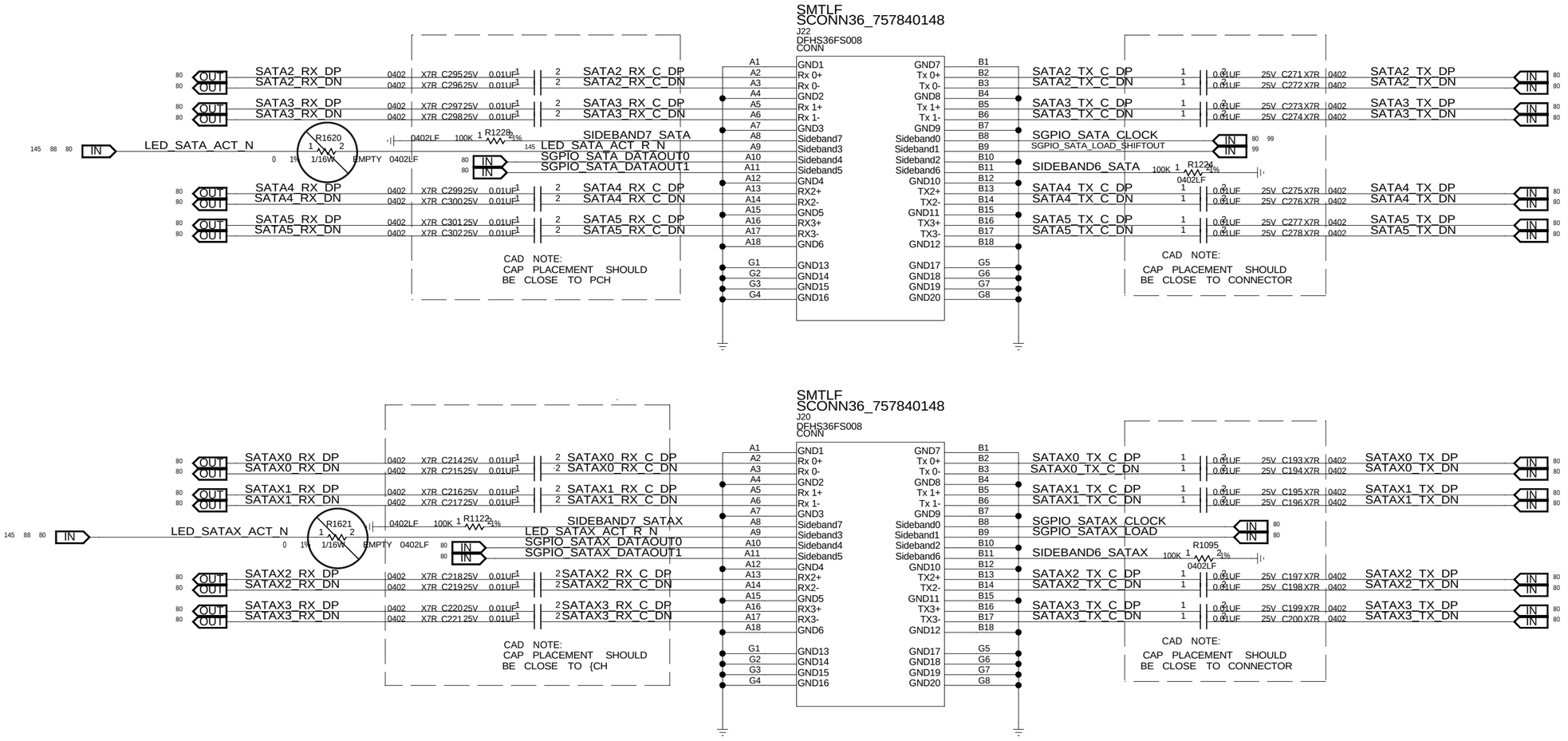
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: PETER | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,RUNNER,MATT | SIZE: C | DATE: Mon Nov 16 11:53:52 2015 | SHEET: 92 OF 188 |



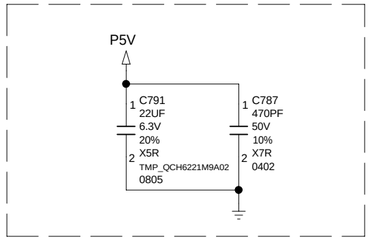





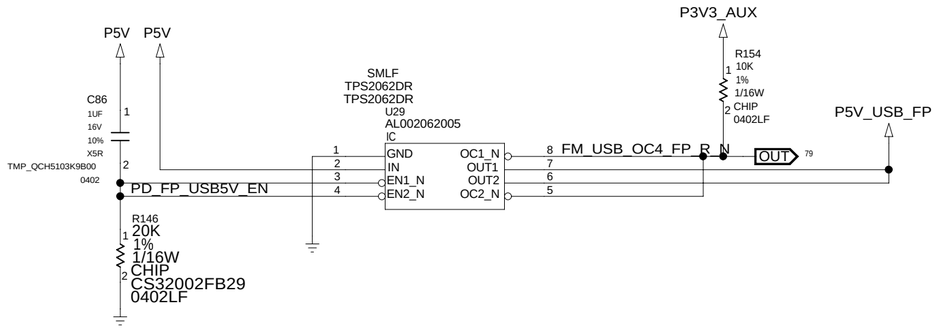


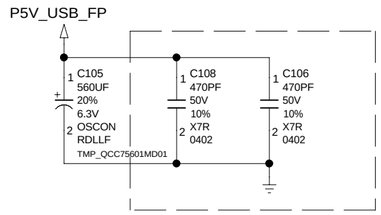
# PCH SATA

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:53:53 2015 | SHEET: 93 OF 188 | |

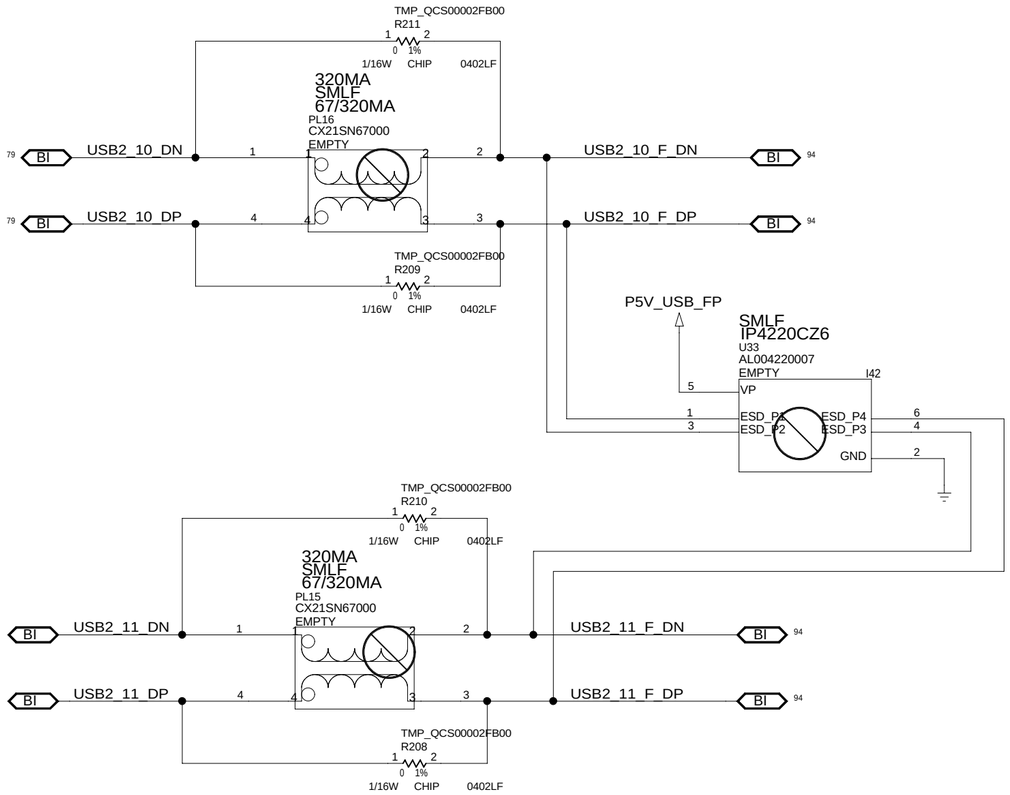



CAD NOTE: PLACE AS CLOSE AS POSSIBLE TO TPS2062

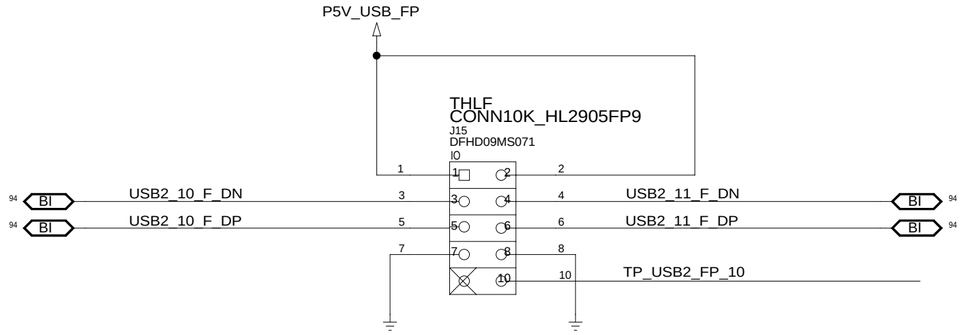



CAD NOTE: PLACE AS CLOSE AS POSSIBLE TO USB CONNECTOR

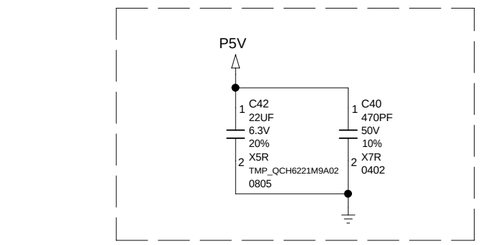



FRONT PANEL USB PORTS

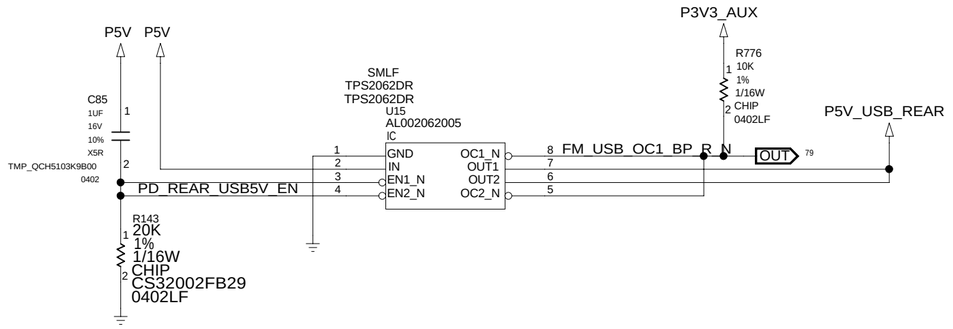


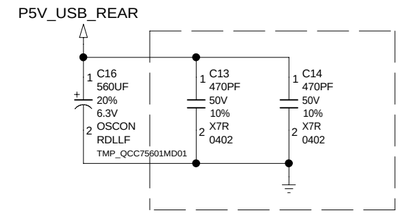

# PCH FRONT USB PORT (2 PORTS)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:53:58 2015 | SHEET: 94 OF 188 |

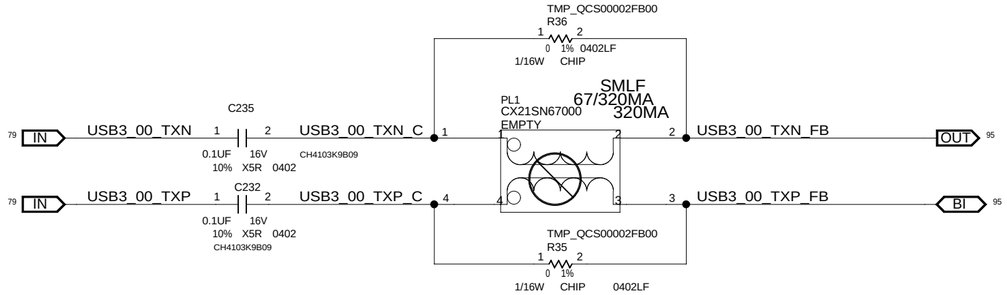


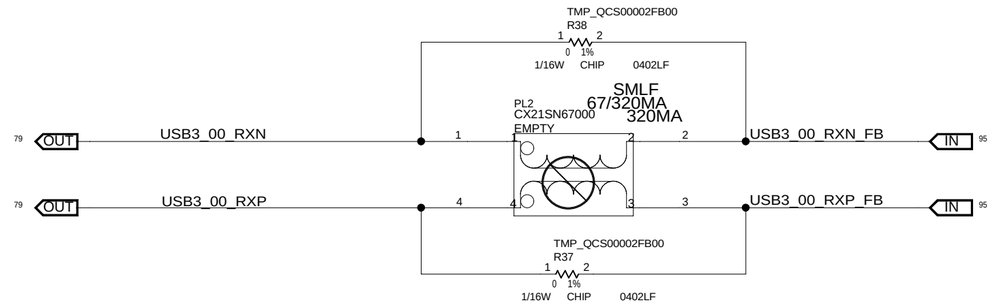

CAD NOTE: PLACE AS CLOSE AS POSSIBLE TO TPS2062

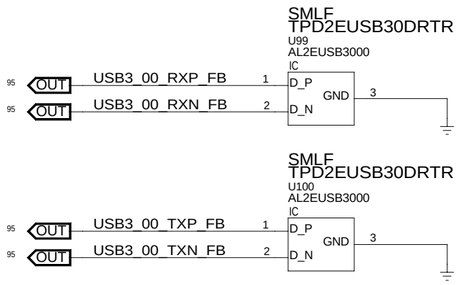


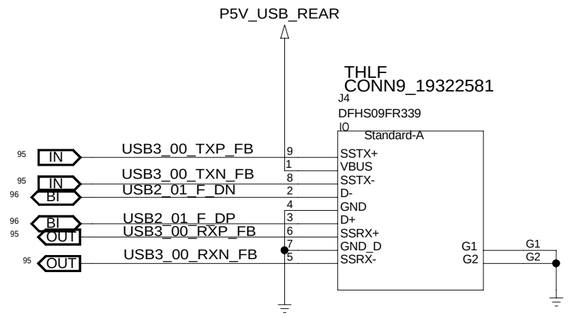



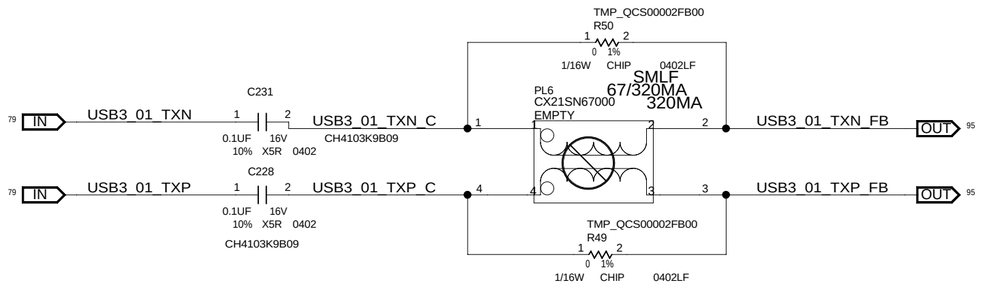

CAD NOTE: PLACE AS CLOSE AS POSSIBLE TO USB CONNECTOR

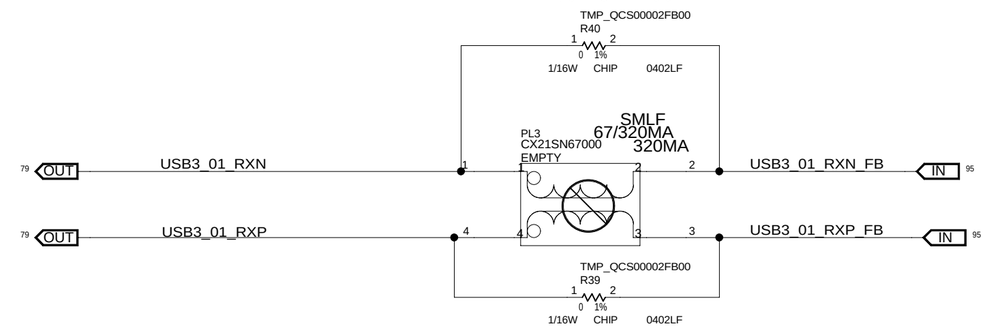


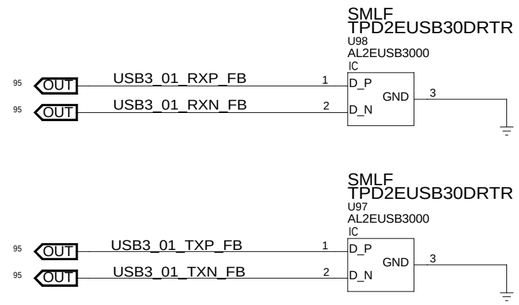



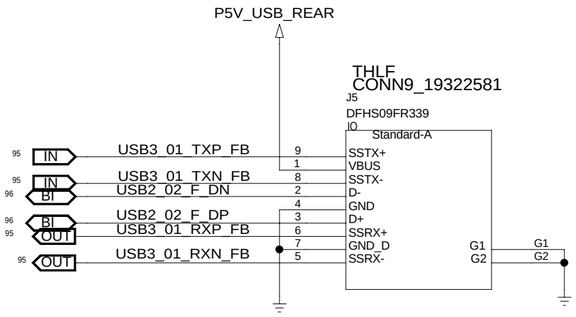



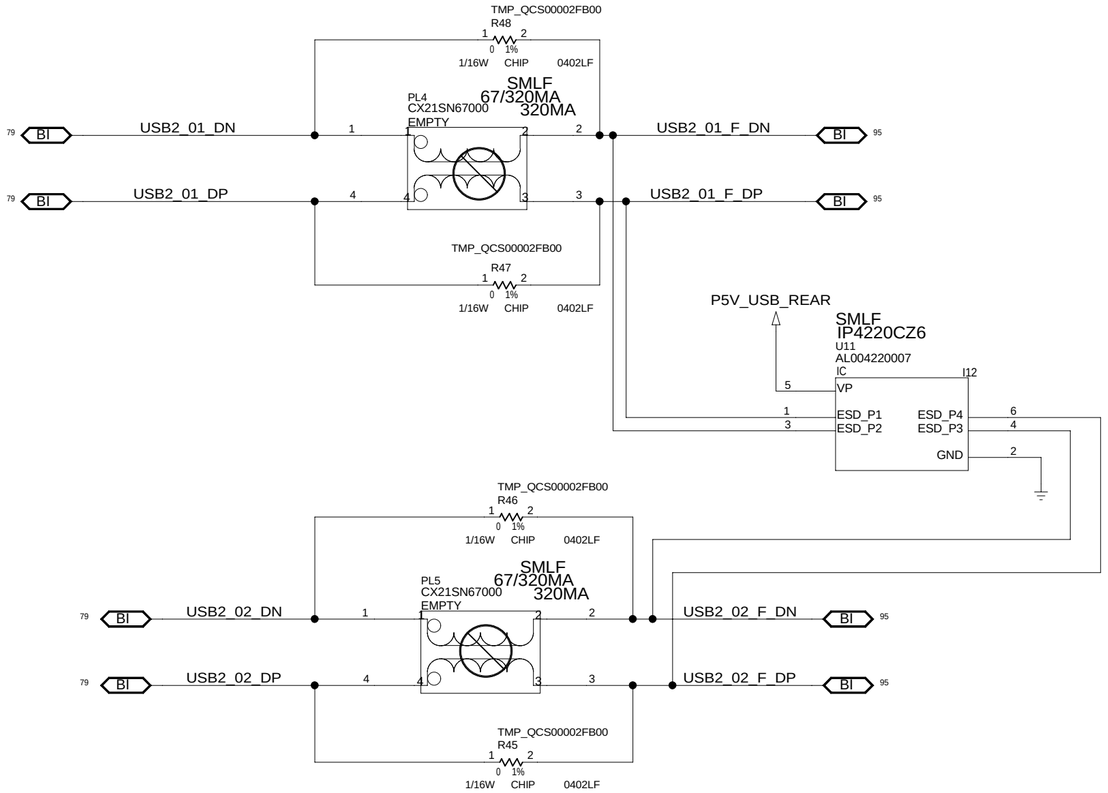



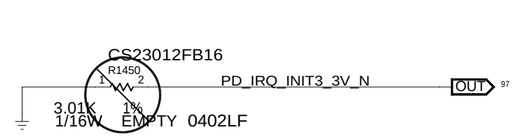

# PCH REAR USB PORTS 1 OF 2

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C DATE: Mon Nov 16 11:53:59 2015 | SHEET: 95 OF 188 | |

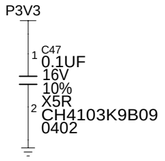



# PCH REAR USB PORTS 2 OF 2

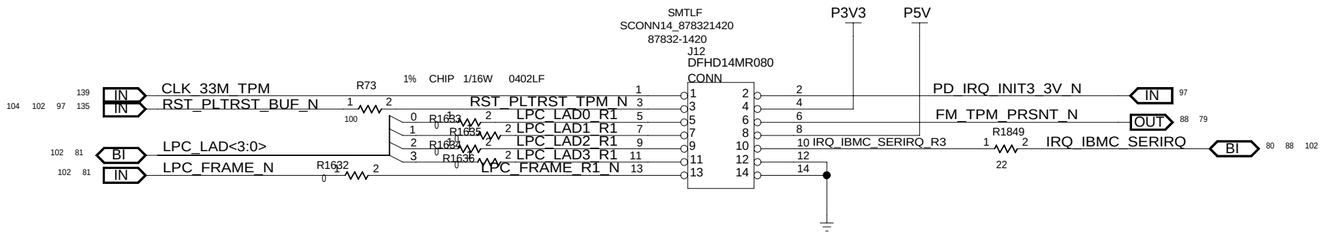
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:54:00 2015 | SHEET: 96 OF 188 |

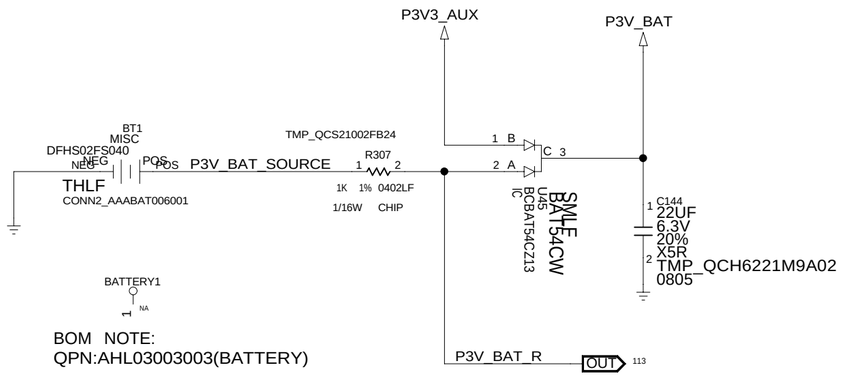



TPM PRESENT FUNCTION

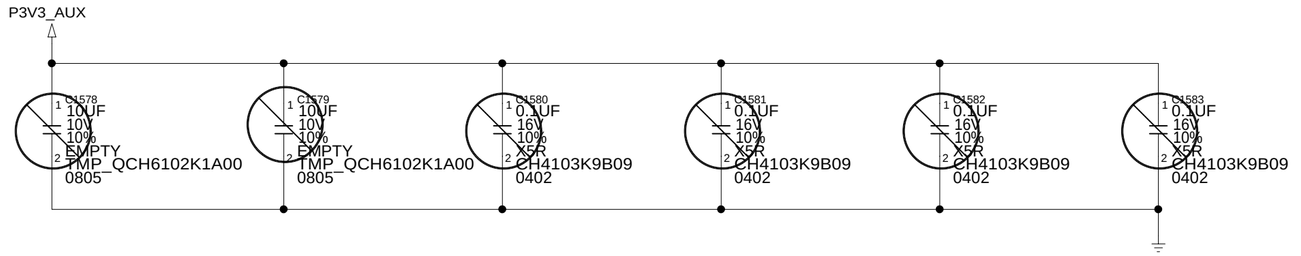


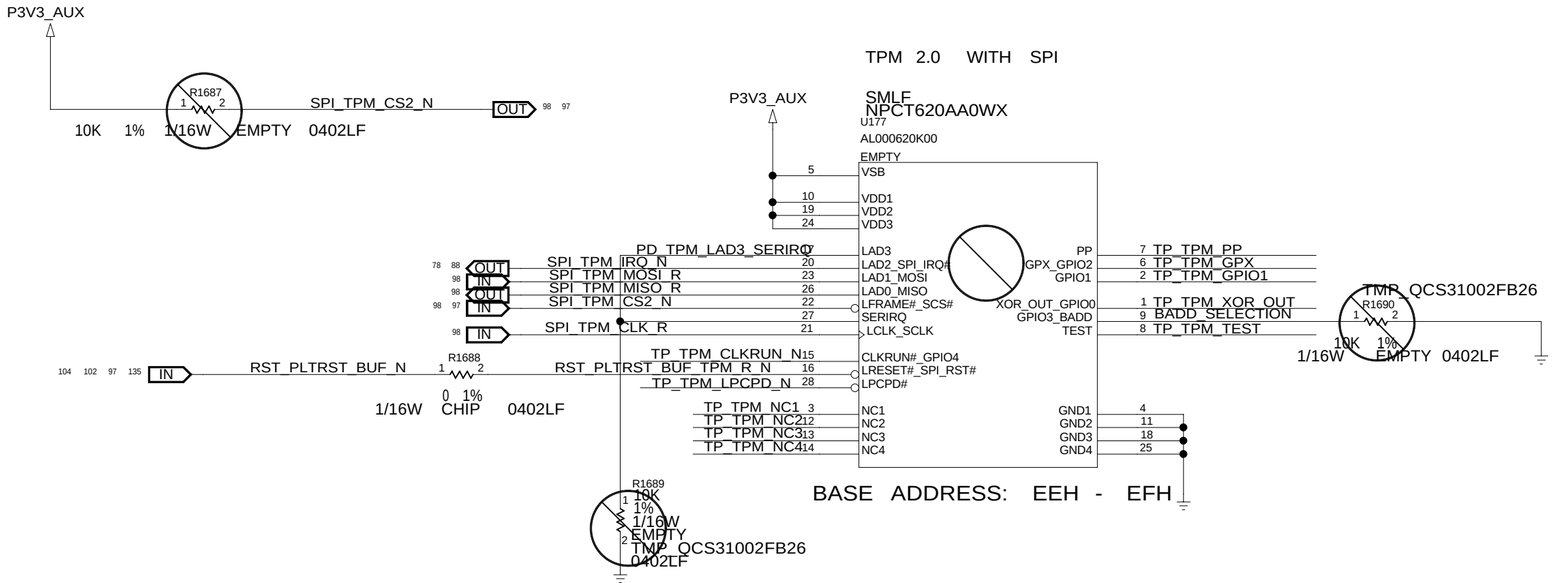

TPM 1.2 WITH LPC




BOM NOTE:
QPN:AHL03003003(BATTERY)



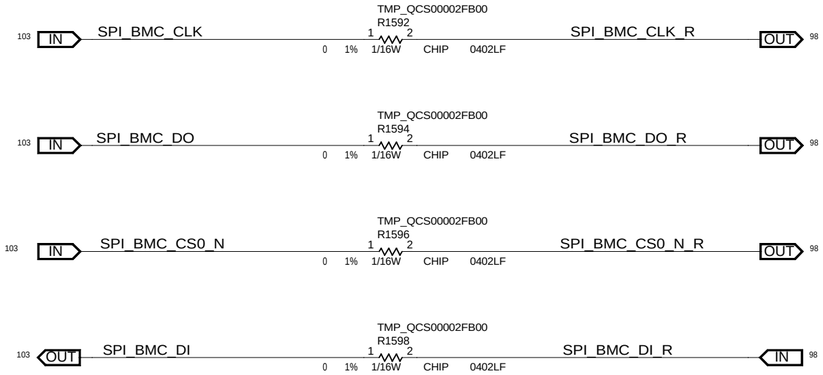




BASE ADDRESS: EEH - EFH

# PCH TPM / BATTERY

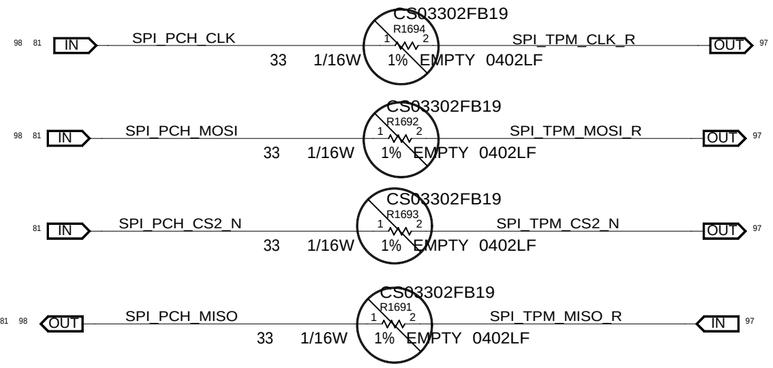
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:54:02 2015 | SHEET 97 OF 188 |

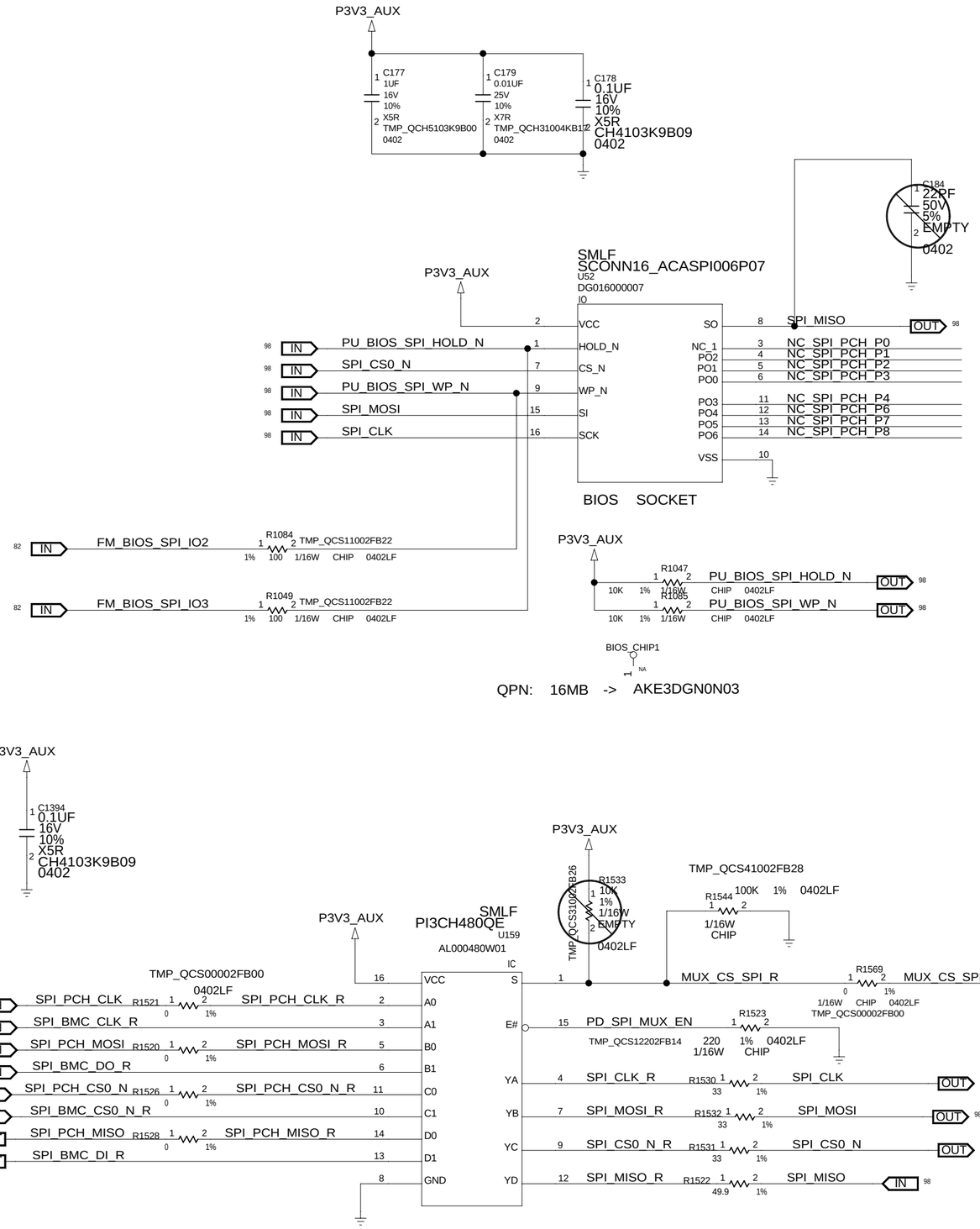
FROM BMC




FROM PCH

TO TPM 2.0



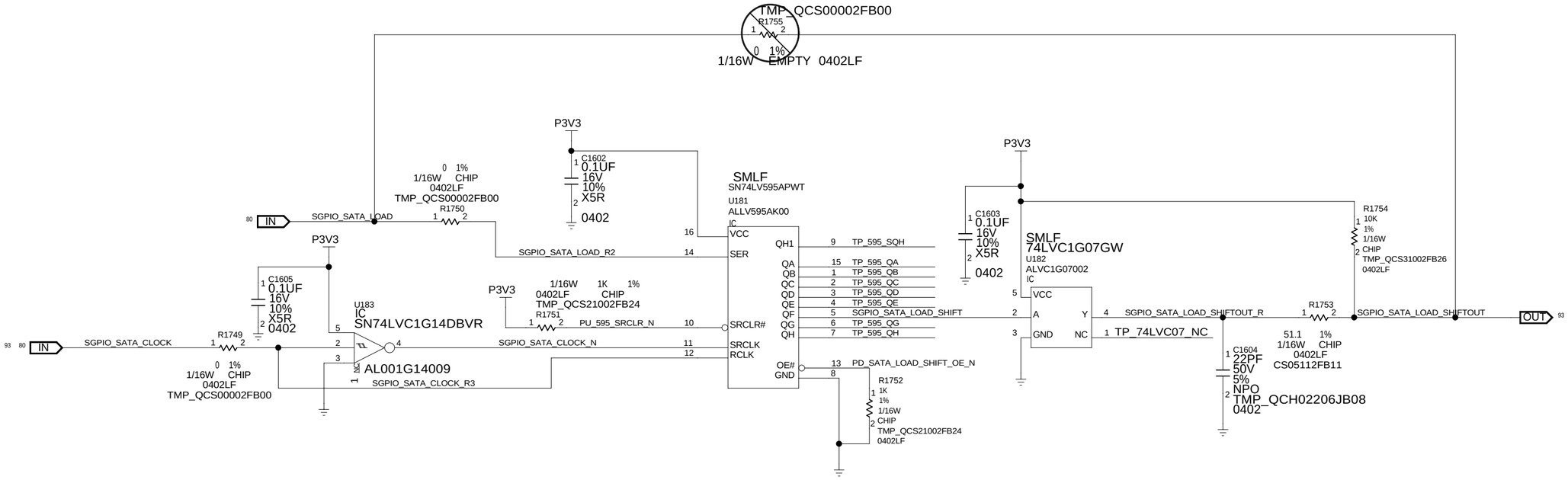







PCH BIOS

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | | REV 1 |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:54:03 2015 | SHEET 98 OF 188 | |




# PCH SATA SGPIO LOAD SHIFT

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:54:04 2015 | SHEET: 99 OF 188 | |

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| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NAME | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER NAME | SIZE C | DATE Thu Jul 04 19:34:13 2013 | SHEET 100 OF 188 | |

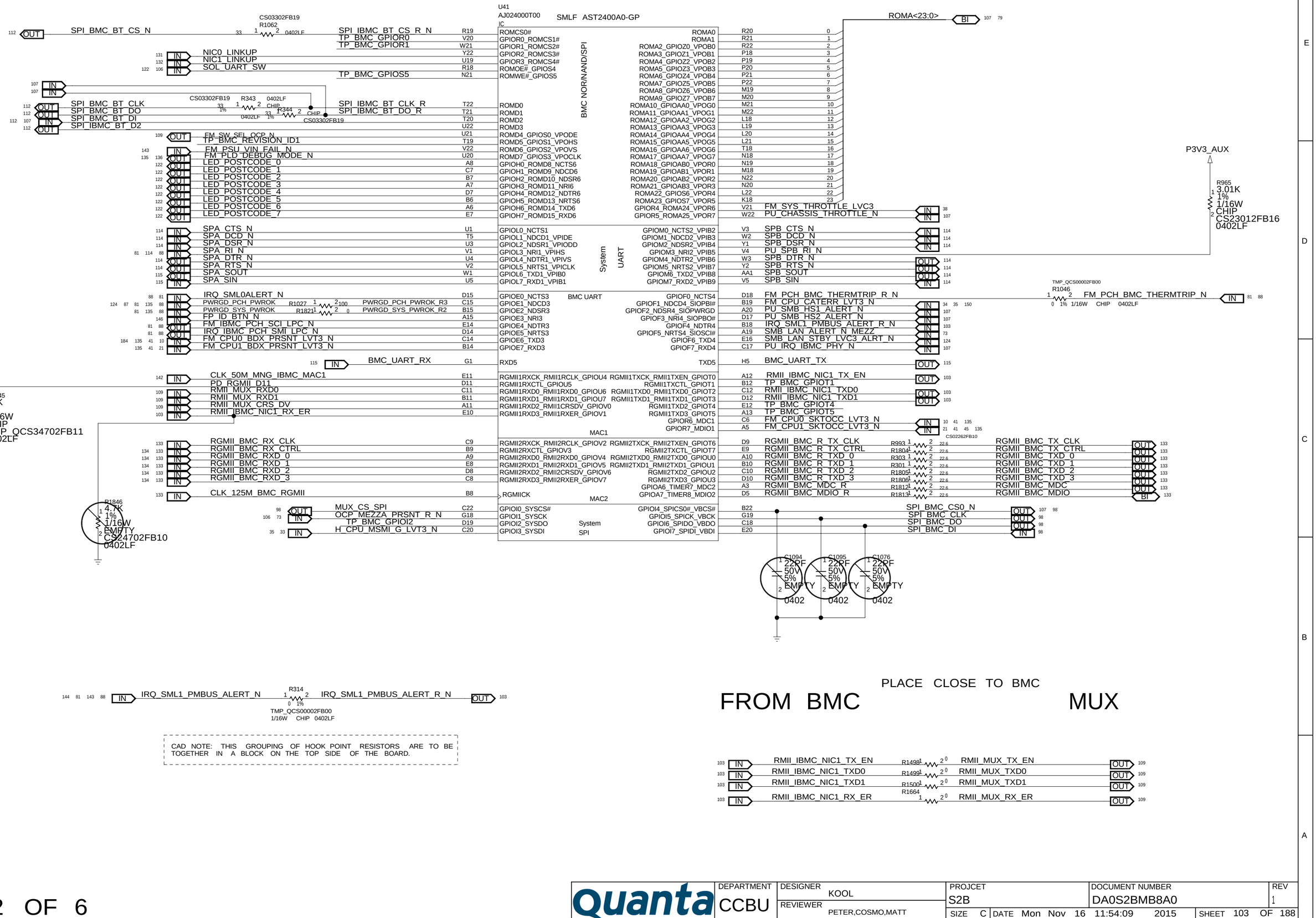
BLANK

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NAME | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER NAME | SIZE C | DATE Thu Jul 04 19:33:38 2013 | SHEET 101 OF 188 |

P0V75_AUX_VTTREF
P1V538_AUX
R9M1 1K 1% CHIP 0402LF
C9M3 0.01UF 25V 10% X7R 0402
R8M1 1K 1% CHIP 0402LF
C9M1 1UF 16V 10% X5R 0402
C9M2 0.01UF 25V 10% X7R 0402
TRACE WIDTH >=15MIL
P3V3_AUX
R357 4.7K 1% 1/16W CHIP 0402LF CS24702FB10
TMP_QCS00002FB00
R348 0 1% EMPTY 0402LF
IRQ_LVC3_WAKE_N
DE NOTE: PREVENT FLOATING WHEN SYSTEM POWER IS OFF
TMP_QCS41002FB28
R1068 100K CHIP 1% 0402LF
R1077 0 1% 1/16W 0402LF
RST_PLTRST_BUF_N
PE_BMC_WAKE_N
CHIP 0 1% 1/16W 0402LF
CLK_100M_BMC_PE_DP
CLK_100M_BMC_PE_DN
PE_PCH_IBMC_TX_C_DP
PE_PCH_IBMC_TX_C_DN
V_M_IBMC_DDR3_DQ<15:0>
SMLF AST2400A0-GP
U41 A1024000T00 IC
PERST# PEWAKE# PEREFCLKP PEREFCLKN PERXP PERXN
PCI-Express
PETXP PETXN PEREXT
PE_PCH_IBMC_RX_DP
PE_PCH_IBMC_RX_DN
BMC_PEREXT
CAD NOTE: CLOSE TO BMC
C173 10% 0.1UF 16V X5R 0402
C174 0.1UF 10% 16V X5R 0402
CH4103K9B09
MDQ0 MDQ1 MDQ2 MDQ3 MDQ4 MDQ5 MDQ6 MDQ7 MDQ8 MDQ9 MDQ10 MDQ11 MDQ12 MDQ13 MDQ14 MDQ15
MDQS0 MDQS0# MDQS1 MDQS1#
V_M_IBMC_DDR3_DQS0_P
V_M_IBMC_DDR3_DQS1_P
V_M_IBMC_DDR3_DQS0_N
V_M_IBMC_DDR3_DQS1_N
DE NOTE: PREVENT FLOATING WHEN SYSTEM POWER DOWN
MVREF
DE NOTE: NC OR TIE TO GND, OR KEEPING AS AST2300 SERIES
MIOZ
DDR2/DDR3
MCK MCK# MCKE MODT MCS# MRAS# MCAS# MWE# MBA0 MBA1 MBA2
V_M_IBMC_DDR3_CLK_P
V_M_IBMC_DDR3_CLK_N
V_M_IBMC_DDR3_CKE
V_M_IBMC_DDR3_ODT
V_M_IBMC_DDR3_CS_N
V_M_IBMC_DDR3_RAS_N
V_M_IBMC_DDR3_CAS_N
V_M_IBMC_DDR3_WE_N
V_M_IBMC_DDR3_BA0
V_M_IBMC_DDR3_BA1
V_M_IBMC_DDR3_BA2
MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8 MA9 MA10 MA11 MA12 MA13 MA14
MDM0 MDM1
V_M_IBMC_DDR3_MA<14:0>
V_M_IBMC_DDR3_DM0
V_M_IBMC_DDR3_DM1
CAD NOTE: CLOSE TO MVREF
C1027 0.01UF 25V 10% X7R 0402
C1036 0.1UF 16V 10% X5R 0402
C1042 0.1UF 16V 10% X5R 0402
CH4103K9B09
CLK_33M_BMC_LPC
LPC_FRAME_N
IRQ_IBMC_SERIRQ
R1848 22
R1637 0 LPC_FRAME_R3_N
IRQ_IBMC_SERIRQ_R2
LCLK LFRAME# LSIRQ#
LPC
LAD0 LAD1 LAD2 LAD3
LPC_LAD0_R3 LPC_LAD1_R3 LPC_LAD2_R3 LPC_LAD3_R3
R1640 R1638 R1641 R1639 0
LPC_LAD<3:0>
CONNECT PCH,TPM
DE NOTE: ASPEED CONFIRM WE CAN USE 33M
100K CHIP R324 0 TMP_QCS41002FB28 0402LF 1%
R1041 R309 R1035 4.7K 1% CHIP 0402LF CS24702FB10
IRQ_PVDDQ_AB_VRHOT_LVT3_N
IRQ_PVDDQ_CD_VRHOT_LVT3_N
H_CPU0_MEMAB_MEMHOT_LVT3_N
H_CPU0_MEMCD_MEMHOT_LVT3_N
IRQ_PVDDQ_EF_VRHOT_LVT3_N
IRQ_PVDDQ_GH_VRHOT_LVT3_N
H_CPU1_MEMEF_MEMHOT_LVT3_N
H_CPU1_MEMGH_MEMHOT_LVT3_N
IRQ_BMC_PCH_NMI_N
R331 0 TMP_QCS00002FB00
FP_NMI_BTN_N
IRQ_BMC_PCH_NMI_STBY_R_N
FP_PWR_BTN_N
FP_IBMC_PWRBTN_OUT_N
FP_RST_BTN_N
RST_IBMC_SYSRST_BTN_OUT_N
PESSD_PRESENT_BMC_N
TP_BMC_GPIOD7
GPIOQ0_SD1CLK_SCL10 GPIOC1_SD1CMD_SDA10 GPIOC2_SD1DAT0_SCL11 GPIOC3_SD1DAT1_SDA11 GPIOC4_SD1DAT2_SCL12 GPIOC5_SD1DAT3_SDA12 GPIOC6_SD1CD#_SCL13 GPIOC7_SD1WP#_SDA13
GPIOD0_SD2CLK GPIOD1_SD2CMD GPIOD2_SD2DAT0 GPIOD3_SD2DAT1 GPIOD4_SD2DAT2 GPIOD5_SD2DAT3 GPIOD6_SD2CD# GPIOD7_SD2WP#
SD/SDIO
GPIOQ4_SCL14 GPIOQ5_SDA14 GPIOQ6 GPIOQ7
GPIO
I2C
SCL1 SDA1 SCL2 SDA2 GPIOQ0_SCL3 GPIOQ1_SDA3 GPIOQ2_SCL4 GPIOQ3_SDA4 GPIOK0_SCL5 GPIOK1_SDA5 GPIOK2_SCL6 GPIOK3_SDA6 GPIOK4_SCL7 GPIOK5_SDA7 GPIOK6_SCL8 GPIOK7_SDA8 GPIOA4_TIMER5_SCL9 GPIOA5_TIMER6_SDA9 GPIOB0_SALT1 GPIOB1_SALT2 GPIOB2_SALT3 GPIOB3_SALT4
SMB_AMI_3V3SB_CLK_R SMB_AMI_3V3SB_DAT_R SMB_RISER2_3V3SB_CLK_R SMB_RISER2_3V3SB_DAT_R SMB_OCP_3V3SB_CLK_R SMB_OCP_3V3SB_DAT_R SMB_HOST_3V3SB_CLK_R SMB_HOST_3V3SB_DAT_R SMB_SML0_3V3SB_CLK_R SMB_SML0_3V3SB_DAT_R SMB_LAN_3V3SB_CLK_R SMB_LAN_3V3SB_DAT_R SMB_SENSOR_3V3SB_CLK_R SMB_SENSOR_3V3SB_DAT_R SMB_SML1_3V3SB_CLK_R SMB_SML1_3V3SB_DAT_R SMB_IPMB_3V3SB_CLK_R SMB_IPMB_3V3SB_DAT_R
FP_ID_LED_N FP_LED_STATUS_GREEN_N FP_LED_STATUS_AMBER_N
P3V3_AUX
CS24702FB10 R1057 4.7K CHIP 1% 0402LF
CS24702FB10 R1078 4.7K 1% 0402LF CHIP
FP_RST_BTN_N RST_IBMC_SYSRST_BTN_OUT_N
FP_PWR_BTN_N FP_IBMC_PWRBTN_OUT_N
FP_PWR_LED_N FP_PWR_LED_R2_N
R1042 R928 EMPTY 0402LF
FM_BMC_READY_N
FP_PWR_LED_R2_N
FM_CPU0_FIVR_FAULT_LVT3_N
FM_CPU1_FIVR_FAULT_LVT3_N
R927 33 R223
FM_CPU0_FIVR_FAULT_LVT3_R2_N
FM_CPU1_FIVR_FAULT_LVT3_R2_N
P3V3
R311 1K 1% 1/16W 0402LF
R308 4.7K 1% 1/16W CHIP 0402LF CS24702FB10
R313 1% 1.5K 0402LF
RST_IBMC_SYSRST_BTN_N
RST_IBMC_SYSRST_BTN_R
RST_IBMC_SYSRST_BTN_OUT_R_N
MBT3904DW1T1G Q16
BA039040080 IC SMLF
SMB_AMI_3V3SB_CLK SMB_AMI_3V3SB_DAT SMB_RISER2_3V3SB_CLK SMB_RISER2_3V3SB_DAT SMB_OCP_3V3SB_CLK SMB_OCP_3V3SB_DAT SMB_HOST_3V3SB_CLK SMB_HOST_3V3SB_DAT SMB_SML0_3V3SB_CLK SMB_SML0_3V3SB_DAT SMB_3V3SB_VR12_CLK SMB_3V3SB_VR12_DAT SMB_SENSOR_3V3SB_CLK SMB_SENSOR_3V3SB_DAT SMB_3V3SB_PMBUS_CLK SMB_3V3SB_PMBUS_DAT SMB_IPMB_3V3SB_CLK SMB_IPMB_3V3SB_DAT
R339 R353 R361 R360 R943 R960 R916 R933 R936 R934 R233 R232 R196 R202 R940 R234 R649 R654 33 CS03302FB19

BMC 1 OF 6

| DEPARTMENT | DESIGNER | PROJCET | DOCUMENT NUMBER | REV |
|---|---|---|---|---|
| CCBU | KOOL | S2B | DA0S2BMB8A0 | 1 |
| | REVIEWER PETER,COSMO,MATT | SIZE C | DATE Mon Nov 16 11:54:05 2015 | SHEET 102 OF 188 |




BMC 2 OF 6

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: KOOL | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,COSMO,MATT | SIZE: C | DATE: Mon Nov 16 11:54:09 2015 | SHEET: 103 OF 188 |

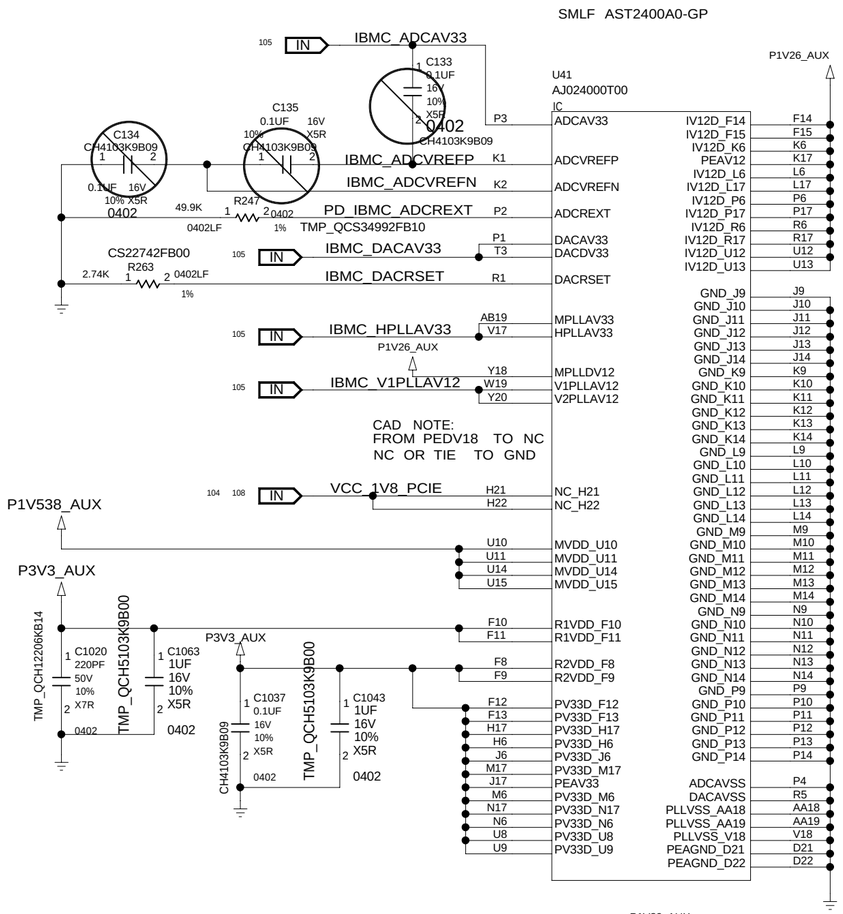
P3V3_AUX
P3V3_AUX
C175 0.1UF 16V 10% X5R 0402 CM4103K9B09
R355 10K 1% 1/16W CHIP 0402LF TMP_QCS31002FB26
SMLF 24MHZ OSC5 BF624000002 OSC
VDD OUT OE GND
PU_24M_BMC_CLK_EN
CLK_24M_BMC_CLKIN_R
TMP_QCS00002FB00
R335 0 1% 1/16W CHIP 0402LF
CLK_24M_BMC_CLKIN
SMLF AST2400A0-GP
U41
AJ024000T00
IC
KEEP SRST# LOW AFTER POWER-ON AND POWER STABLE FOR A PERIOD OF TIME (MINIMUM 1MS). IT WILL RESET THE SOC AND DRAM PART FUNCTION
RST_RSMRST_N
TMP_QCS31002FB26
R979 10K 1% CHIP 0402LF
PD_BMC_E4
CLKIN SRST# ENTEST
MISC
AB22 W20 E4
FAN_TACH0 FAN_TACH1 FAN_TACH2 FAN_TACH3 FAN_TACH4 FAN_TACH5 FAN_TACH6 FAN_TACH7
TP_BMC_GPIOP0 TP_BMC_GPIOP1 TP_BMC_GPIOP2 TP_BMC_GPIOP3
IRQ_PVCCIN_CPU0_VRHOT_LVT3_N IRQ_PVCCIN_CPU1_VRHOT_LVT3_N FM_CPU0_PROCHOT_LVT3_N FM_CPU1_PROCHOT_LVT3_N
GPIOO0_TACH0_VPIG8 GPIOO1_TACH1_VPIG9 GPIOO2_TACH2_VPIR0 GPIOO3_TACH3_VPIR1 GPIOO4_TACH4_VPIR2 GPIOO5_TACH5_VPIR3 GPIOO6_TACH6_VPIR4 GPIOO7_TACH7_VPIR5 GPIOP0_TACH8_VPIR6 GPIOP1_TACH9_VPIR7 GPIOP2_TACH10_VPIR8 GPIOP3_TACH11_VPIR9 GPIOP4_TACH12 GPIOP5_TACH13 GPIOP6_TACH14_BMCINT GPIOP7_TACH15_FLACK
FAN
V6 Y5 AA4 AB3 W6 AA5 AB4 V7 Y6 AB5 W7 AA6 AB6 Y7 AA7 AB7
P3V3_AUX
R950 47K 1% 0402LF CHIP
R226 47K 1% 0402LF EMPTY
R224 47K 1% 0402LF CHIP
R225 47K 1% 0402LF CHIP
R228 10K 1% CHIP 0402LF
TMP_QCS34702FB11
TMP_QCS31002FB26
P3V3_SCALED P5V_SCALED P12V_SCALED P1V05_STBY_PCH_SENSOR P1V8_AUX_SENSOR P3V3_AUX_SCALED P5V_AUX_SCALED P3V_BAT_SCALED
ADC0_GPIW0 ADC1_GPIW1 ADC2_GPIW2 ADC3_GPIW3 ADC4_GPIW4 ADC5_GPIW5 ADC6_GPIW6 ADC7_GPIW7 ADC8_GPIX0 ADC9_GPIX1 ADC10_GPIX2 ADC11_GPIX3 ADC12_GPIX4 ADC13_GPIX5 ADC14_GPIX6 ADC15_GPIX7
ADC
L5 L4 L3 L2 L1 M5 M4 M3 M2 M1 N5 N4 N3 N2 N1 P5
PU_JTAG_IBMC_NTRST JTAG_IBMC_PLD_TDI JTAG_IBMC_PLD_TMS JTAG_IBMC_PLD_TCK PD_BMC_RTCK JTAG_IBMC_PLD_TDO
NTRST TDI_BDM TMS TCK RTCK TDO
JTAG
E1 F1 G2 F2 G4 G3
R967 10K 1% 0402LF CHIP TMP_QCS31002FB26
C130 1UF 16V 10% X5R 0402 TMP_QCH5103K9B00
FM_VIDEO_DISABLE_N FM_BMC_DEBUG_SW_N FM_BIOS_POST_CMPLT_N FM_BMC_SYS_THROTTLE_N
BATTERY_DETECT FM_INTRUDER_HDR_R_N FM_BMC_NMI_N TP_NCSI_RISER_PRNT_N
GPIOA0_MAC1LINK GPIOA1_MAC2LINK GPIOA2_TIMER3 GPIOA3_TIMER4 GPIOG4_WDTRST1_OSCCLK GPIOG5_WDTRST2_USBCKI GPIOG6_FLBUSY# GPIOG7_FLWP#
GPIO
D6 B5 A4 E6 B13 Y21 AA22 U18
FM_INTRUDER_HDR_N
R1067 0 1% 1/16W CHIP 0402LF TMP_QCS00002FB00
GPIOB4_LPCRST# GPIOB5_LPCPD#_LPCSMI# GPIOB6_LPCPME# GPIOB7_EXTRST#_SPICS1# GPIOY0_SIOS3# GPIOY1_SIOS5# GPIOY2_SIOPWREQ# GPIOY3_SIOONCTRL#
SGPIO
E19 H19 H20 E18 C21 F20 G20 K20
RST_PLTRST_BUF_N FM_CPU0_THERMTRIP_LATCH_LVC3_N FM_CPU1_THERMTRIP_LATCH_LVC3_N TP_SPEAKER_IBMC VCC_1V8_PCIEA VCC_1V8_PCIE FM_BMC_ONCTL_N PU_BMC_GPIOY3
R1695 0
R419 0 EMPTY
DACB DACG DACR
VGA
R4 R3 R2
V_IBMC_GFX_BLU V_IBMC_GFX_GRN V_IBMC_GFX_RED
VGAHS_GPIOJ4 VGAVS_GPIOJ5 DDCCLK_GPIOJ6 DDCDAT_GPIOJ7
T4 U2 T2 T1
V_IBMC_GFX_HSYN_R V_IBMC_GFX_VSYN_R V_IBMC_DDC_SCL V_IBMC_DDC_SDA
TMP_QCS11502FB21
R955 150 1% 0402LF CHIP
R959 150 1% 0402LF CHIP
R961 150 1% 0402LF CHIP
R249 33 1% 0402LF CHIP
R256 33 1% 0402LF CHIP
CS03302FB19
V_IBMC_GFX_HSYN V_IBMC_GFX_VSYN
CAD NOTE: PLACE RESISTORS CLOSE TO IBMC USE THE SAME GND COPPER
CAD NOTE: PLACE RESISTORS CLOSE TO IBMC WITHIN 1 INCH
GPION0_PWM0_VPIG0 GPION1_PWM1_VPIG1 GPION2_PWM2_VPIG2 GPION3_PWM3_VPIG3 GPION4_PWM4_VPIG4 GPION5_PWM5_VPIG5 GPION6_PWM6_VPIG6 GPION7_PWM7_VPIG7
W4 Y3 AA2 AB1 W5 Y4 AA3 AB2
FAN_PWM_OUT_SYS0 FAN_PWM_OUT_SYS1 FAN_PWM_OUT_SYS2 FAN_PWM_OUT_SYS3 TP_BMC_GPION4 TP_BMC_GPION5 TP_BMC_GPION6 TP_BMC_GPION7
USB
USB2AV33 USB2VRES USB2AVSS USB2_DP/USB2_HDP USB2_DN/USB2_HDN USB11_HDP USB11_HDN USB11_DP/USB11_HDP2 USB11_DN/USB11_HDN2
W18 AA20 Y19 AB21 AB20 J1 J2 K4 K3
IBMC_USB2AV33 IBMC_USB2VRES USB2_PCH_P9_R_DP USB2_PCH_P9_R_DN PD_USB_BMC_P1_DP PD_USB_BMC_P1_DN USB_PCH_P8_R_DP USB_PCH_P8_R_DN
R1056 8.25K 1% 0402LF
R1618 0 CHIP 0402LF
R1619 0 CHIP 0402LF
PECI
PECIVDD PECI
V19 AA21
PECI_BMC_R
R338 33 1% CHIP 0402LF
CS03302FB19
PECI_BMC
GPIOJ0_SGPMCK GPIOJ1_SGPMLD GPIOJ2_SGPMO GPIOJ3_SGPMI GPIOG0_SGPSCK GPIOG1_SGPSLD GPIOG2_SGPSI0 GPIOG3_SGPSI1
J5 J4 K5 J3 A14 E13 D13 C13
SGPIO_IBMC_CLK_R SGPIO_IBMC_LD_R_N TP_SGPIO_IBMC_DOUT_R SGPIO_IBMC_DIN_R PSU0_PRESENT_R_N PSU1_PRESENT_R_N FM_SLP_S3_N FM_SLP_S4_N
R251 15 1% 0402LF CHIP
R946 15 1% 0402LF CHIP
R956 33 1% 0402LF CHIP
SGPIO_IBMC_CLK SGPIO_IBMC_LD_N SGPIO_IBMC_DIN
P3V3_AUX
220 OHM@100MHZ
U50
220/1500MA
C170 4.7UF 6.3V 10% X6S 0603
C172 100PF 50V NPO 0402
C171 0.1UF 16V X5R 0402
C1079 1UF X5R 16V 10% 0402 TMP_QCH5103K9B00
PVCCIO
DE NOTE: MUST PULL LOW FOR IDLE STATE
R1065 10K 1% CHIP 0402LF TMP_QCS31002FB26
R1031 100K 1% 1/16W EMPTY 0402LF TMP_QCS41002FB28
DE NOTE: IN AST2300 PINC21,F20,G20 IS 1.8V POWER
DE NOTE: IN AST2300 PIN K20 IS ENTEST2

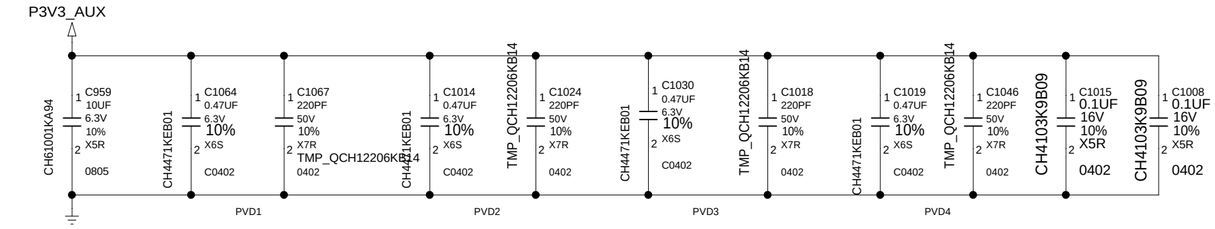
BYPASS BMC PS_ON_N

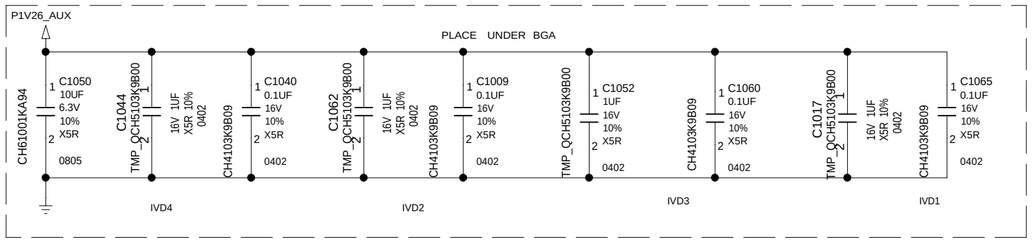
P3V3_AUX
R656 4.7K 1% 1/16W CHIP 0402LF CS24702FB10
FM_BMC_ONCTL_R_N
R416 0 1% 0402LF
FM_BMC_ONCTL_N
CS32002FB29
FM_SLP_S3_N
R369 20K 1% 1/16W CHIP 0402LF
FM_SLP_S3_R_N
C23 MBT3904DW1T6G Q20 IC BA039040080 SMLF

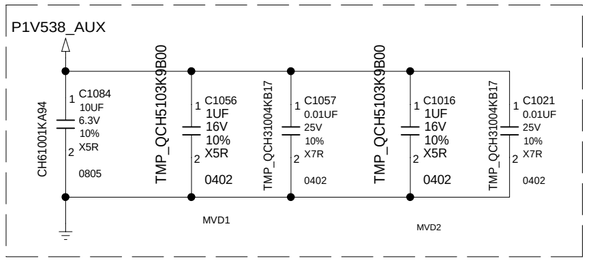
BMC 3 OF 6

| DEPARTMENT | DESIGNER | PROJCET | DOCUMENT NUMBER | REV |
|---|---|---|---|---|
| CCBU | KOOL | S2B | DA0S2BMB8A0 | 1 |
| | REVIEWER PETER,COSMO,MATT | SIZE C DATE Mon Nov 16 11:54:11 2015 | SHEET 104 OF 188 | |

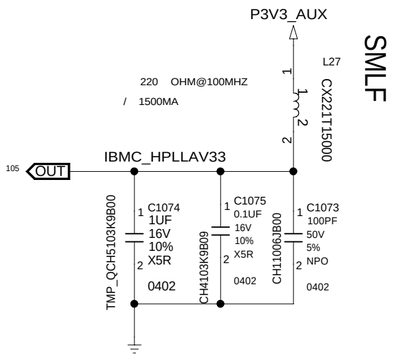


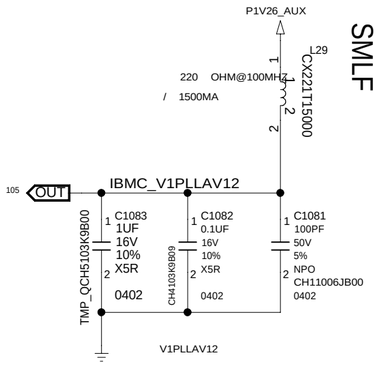



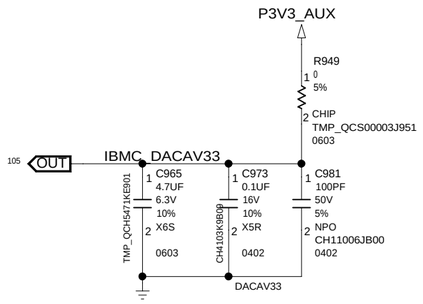



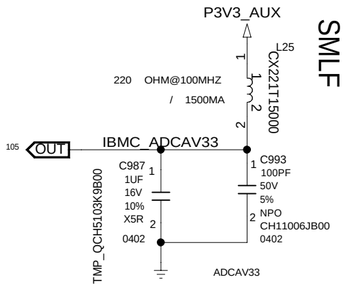




PLACE UNDER BGA AT LEAST 5 POWER VIAS(18 MIL)



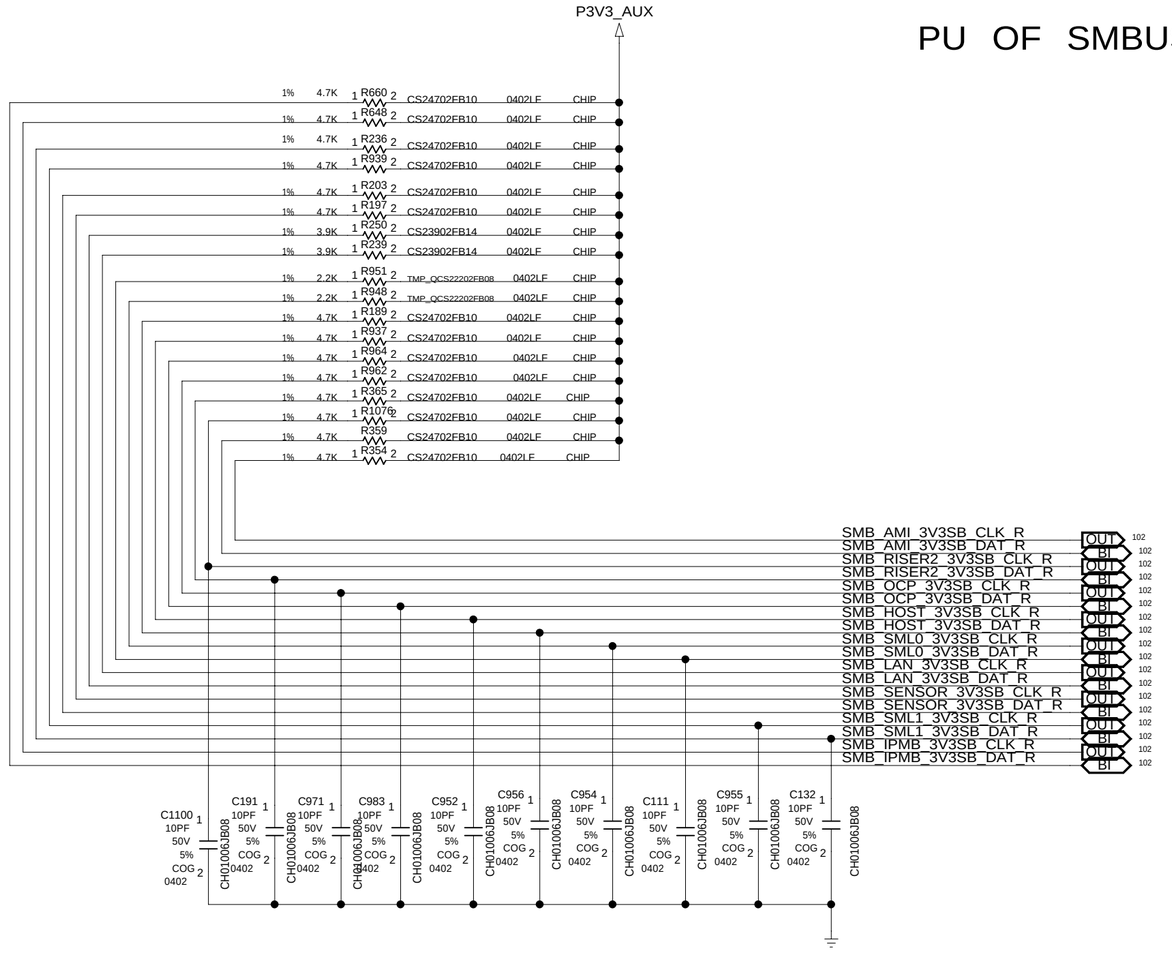




BMC 4 OF 6

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER KOOL | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER PETER,COSMO,MATT | SIZE C | DATE Mon Nov 16 11:54:13 2015 | SHEET 105 OF 188 | |

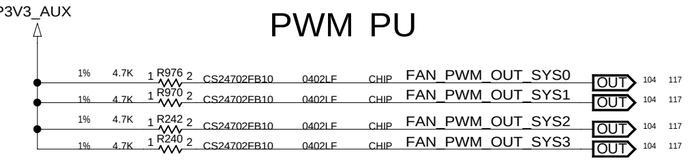
# PU OF SMBUS



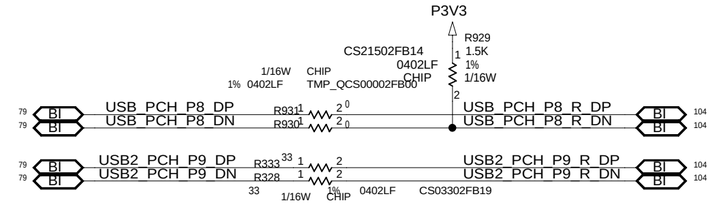

CAD NOTES:

PLACE 10PF CLOSE TO BMC

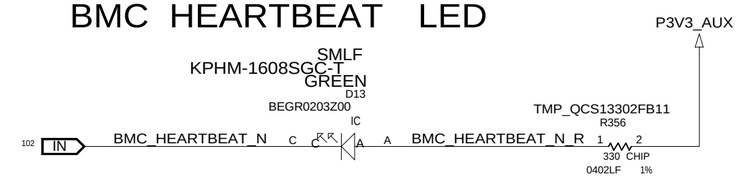
# PWM PU



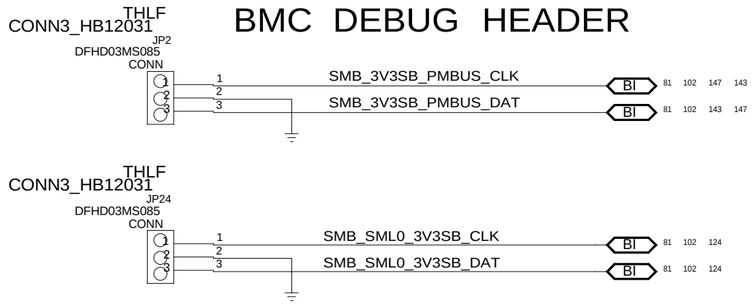

# USB TERMINATION



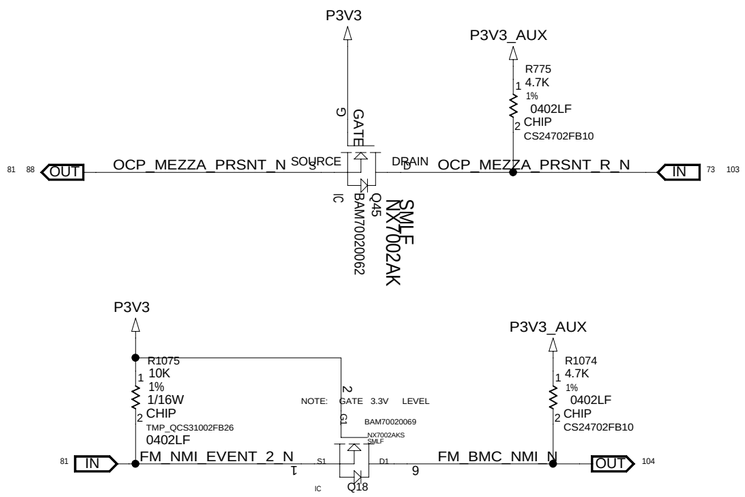

# BMC HEARTBEAT LED



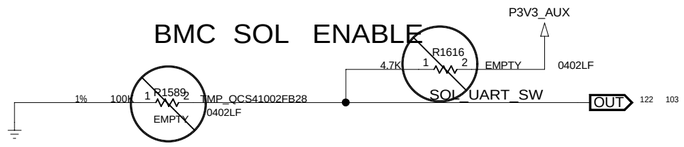

# BMC DEBUG HEADER




# GPIO ISOLATION




# BMC SOL ENABLE




# BMC 5 OF 6

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER KOOL | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | | |
| | | REVIEWER PETER,COSMO,MATT | SIZE C | DATE Mon Nov 16 11:54:15 2015 | SHEET 106 OF 188 | | |

ROMA[1:0] : ARM CPU BOOT CODE SELECTION
00 : BOOT FROM NOR FLASH MEMORY
01 : BOOT FROM NAND FLASH MEMORY
*10 : BOOT FROM SPI FLASH MEMORY
11 : DISABLE ARM CPU OPERATION

ROMA[3:2] : VGA MEMORY SIZE SELECTION
*00 : SELECT 8 MB VGA MEMORY
01 : SELECT 16 MB VGA MEMORY
10 : SELECT 32 MB VGA MEMORY
11 : SELECT 64 MB VGA MEMORY

ROMA4 : BOOT FLASH MEMORY EXTENDED OPTION
NOR TYPE FLASH : DATA BUS WIDTH SELECTION
0 : SELECT 8 BITS INTERFACE
1 : SELECT 16 BITS INTERFACE
SPI TYPE FLASH : BOOT ADDRESS MODE SELECTION
*0 : BOOT WITH 24 BITS ADDRESS MODE
1 : BOOT WITH 32 BITS ADDRESS MODE

ROMA5 : ENABLE VGA BIOS ROM
*0 : NO VGA BIOS ROM (FOR ON-BOARD APPLICATIONS)
1 : ENABLE VGA BIOS ROM (FOR ADD-ON CARD APPLICATIONS)

ROMA6 : DEFINE MAC#1 INTERFACE
*0 : RMII/NCSI
1 : RGMII

ROMA7 : DEFINE MAC#2 INTERFACE
*0 : RMII/NCSI
1 : RGMII

ROMA[9:8] : H-PLL DEFAULT CLOCK FREQUENCY SELECTION
00 : SELECT 384 MHZ
*01 : SELECT 360 MHZ
10 : SELECT 336 MHZ
11 : SELECT 204 MHZ

ROMA[11:10] : CPU/AHB CLOCK FREQUENCY RATIO SELECTION
00 : SELECT CPU:AHB = 1:1
*01 : SELECT CPU:AHB = 2:1
10 : SELECT CPU:AHB = 4:1
11 : SELECT CPU:AHB = 3:1

ROMA[13:12] : SPI MODE SELECTION
*00 : DISABLE SPI INTERFACE
01 : ENABLE SPI MASTER
10 : ENABLE SPI MASTER AND SPI SLAVE TO AHB BRIDGE
11 : ENABLE SPI BYPASS

ROMA14 : ENABLE LPC DEDICATED RESET PIN FUNCTION
0 : LPC RESET IS SHARED WITH PCI RESET PIN
*1 : LPC RESET IS LOCATED AT PIN NUMBER E19, SHARED WITH GPIOB4.

ROMA15 : VGA CLASS CODE SELECTION
0 : SELECT THE CLASS CODE FOR VIDEO DEVICE
*1 : SELECT THE CLASS CODE FOR VGA DEVICE

ROMA16 : SUPERIO CONFIGURATION ADDRESS SELECTION
*0 : DECODE 0X2E
1 : DECODE 0X4E

ROMA17 : ENABLE BMC 2ND BOOT WATCHDOG TIMER
*0 : DISABLE
1 : ENABLE BMC 2ND BOOT WATCHDOG TIMER START COUNTING AT POWER UP.

ROMA23,ROMA18 : CLOCK SOURCE SELECTION
*00 : CLKIN=24 MHZ
01 : CLKIN=48 MHZ
10 : CLKIN=25 MHZ, USBCKI=24 MHZ
11 : CLKIN=25 MHZ, USBCKI=48 MHZ

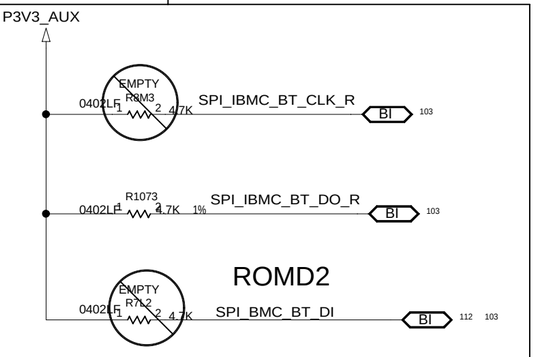
ROMA19 : DISABLE ACPI CONTROLLER
0 : ENABLE
*1 : DISABLE

ROMA20 : DISABLE LPC TO DECODE SUPERIO 0X2E/0X4E ADDRESS
*0 : ENABLE ADRESS DECODING
1 : DISABLE ADDRESS DECODING

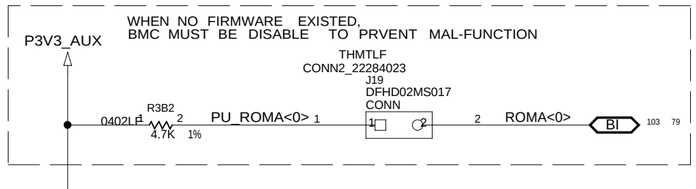
ROMA21 : ENABLE GPIOD PASS-THROUGH MODE
0 : DISABLE
*1 : ENABLE PASS-THROUGH AT POWER ON

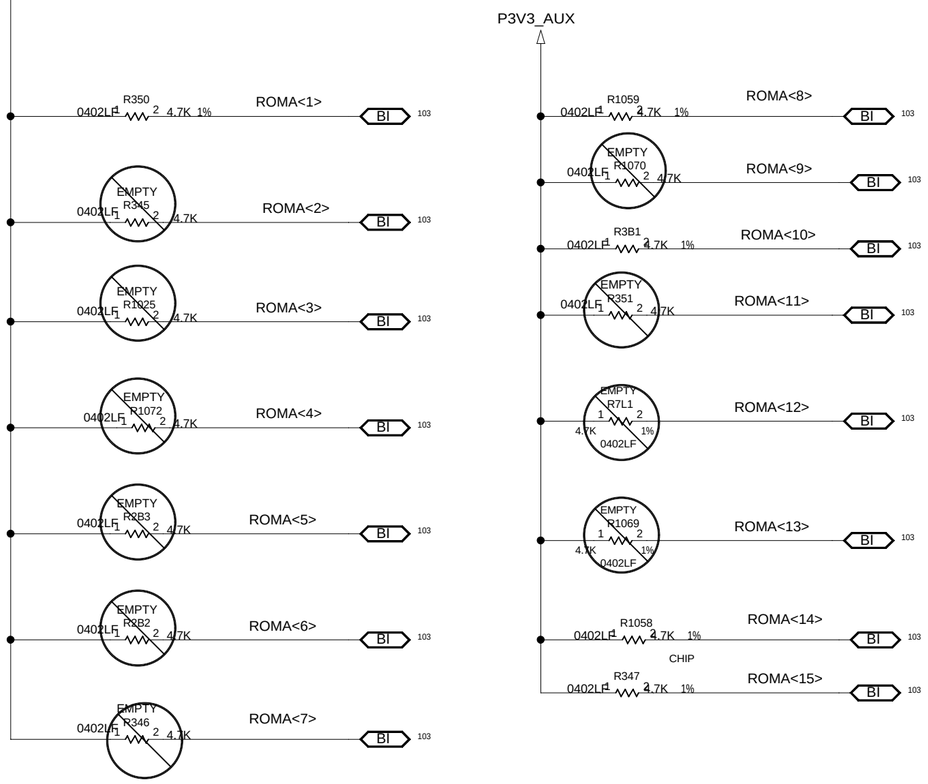
ROMA22 : ENABLE GPIOE PASS-THROUGH MODE
*0 : DISABLE
1 : ENABLE PASS-THROUGH AT POWER ON

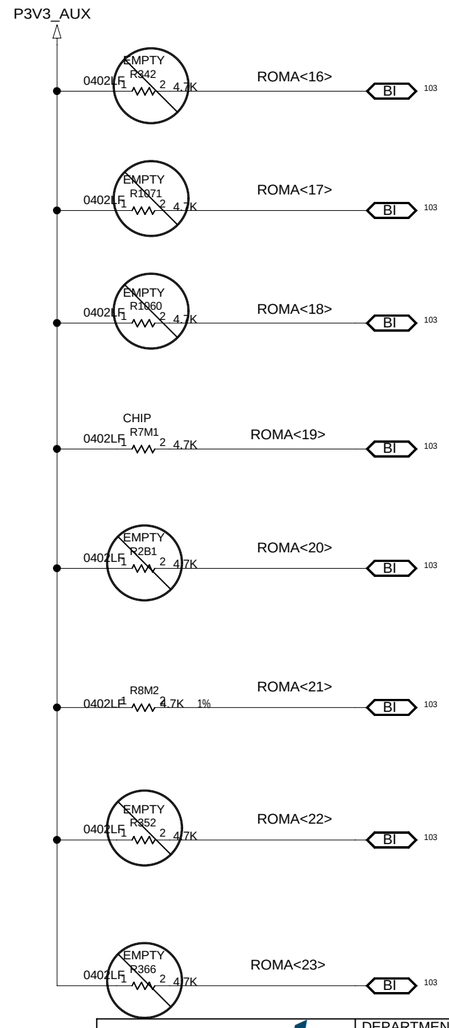
ROMD[2:0] : DRAM CONFIGURATION SETTING
000 : DDR3 SDRAM WITH CL=5, CWL=5
*010 : DDR3 SDRAM WITH CL=6, CWL=5
100 : DDR3 SDRAM WITH CL=7, CWL=6
110 : DDR3 SDRAM WITH CL=8, CWL=6
001 : DDR2 SDRAM WITH CL=4
011 : DDR2 SDRAM WITH CL=5
101 : DDR2 SDRAM WITH CL=6
111 : DDR2 SDRAM WITH CL=7

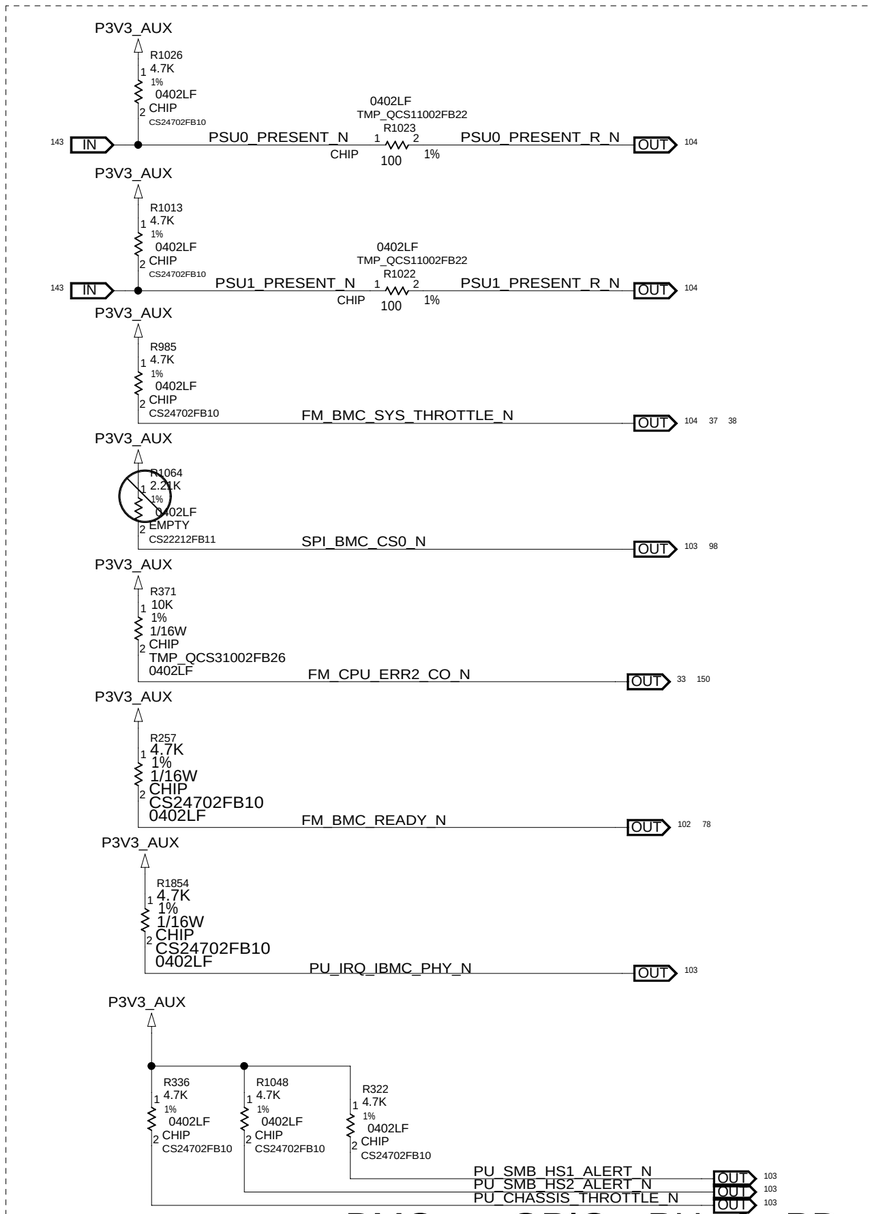



ROMD[7:3] : SOFTWARE DEFINED
THERE BITS RE NOT DEFINED BY CHIP, THEY CAN BE USED AS FIRMWARE DEFINED SETTING, OR SYSTEM DEFINED SETTING.




BMC - GPIO PU & PD

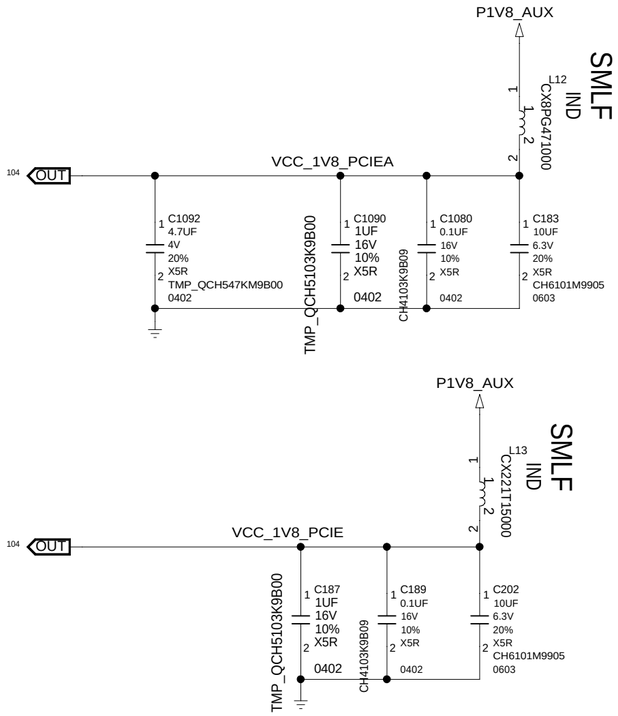
BMC - HW STRAPPING

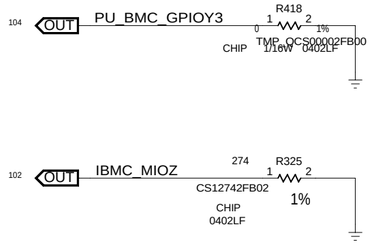
BMC 6 OF 6

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER KOOL | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,COSMO,MATT | SIZE C | DATE Mon Nov 16 11:54:16 2015 | SHEET 107 OF 188 |

UN-STUFF FOR AST2400

STUFF FOR AST2300



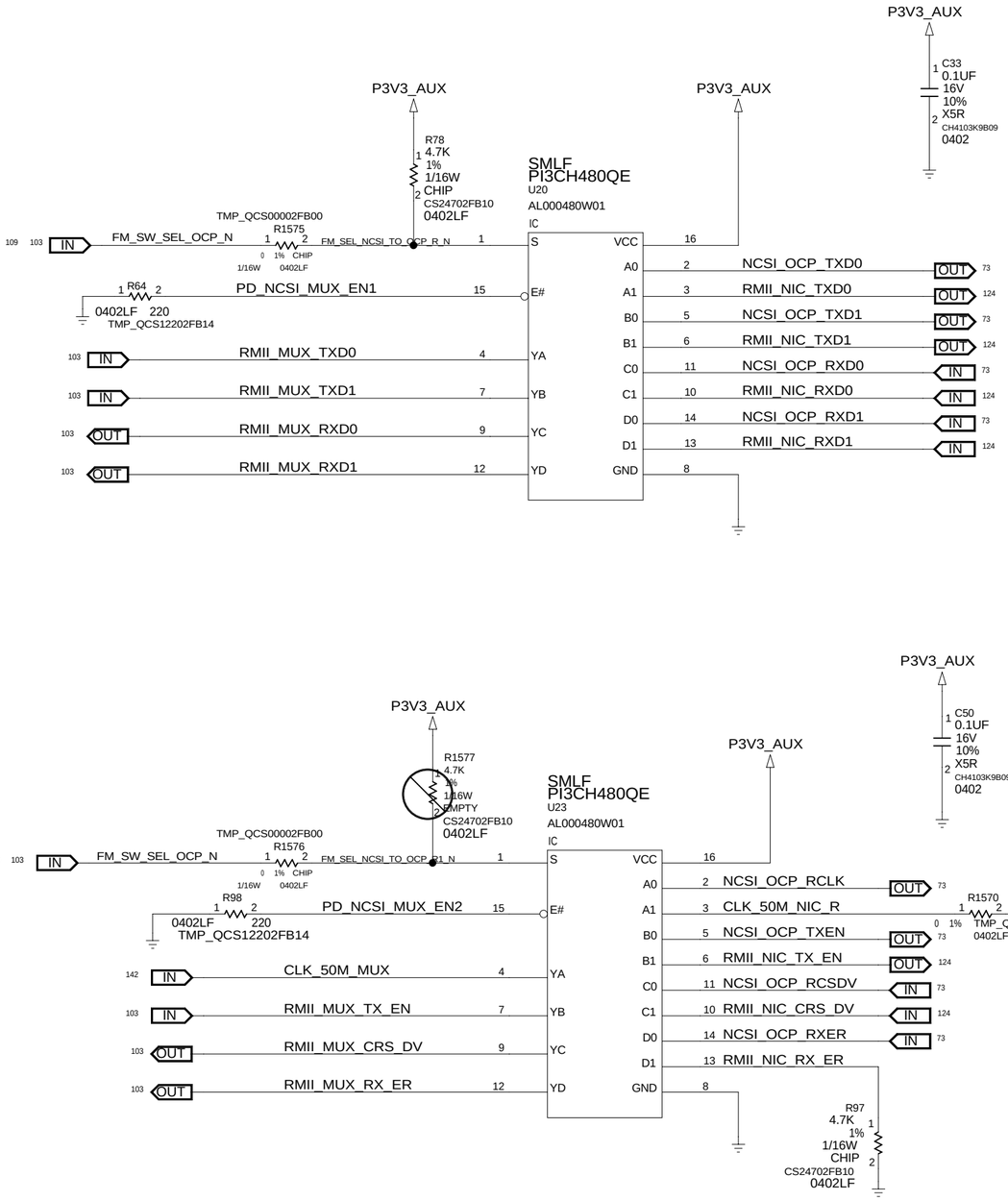

190 OHM FOR AST2400

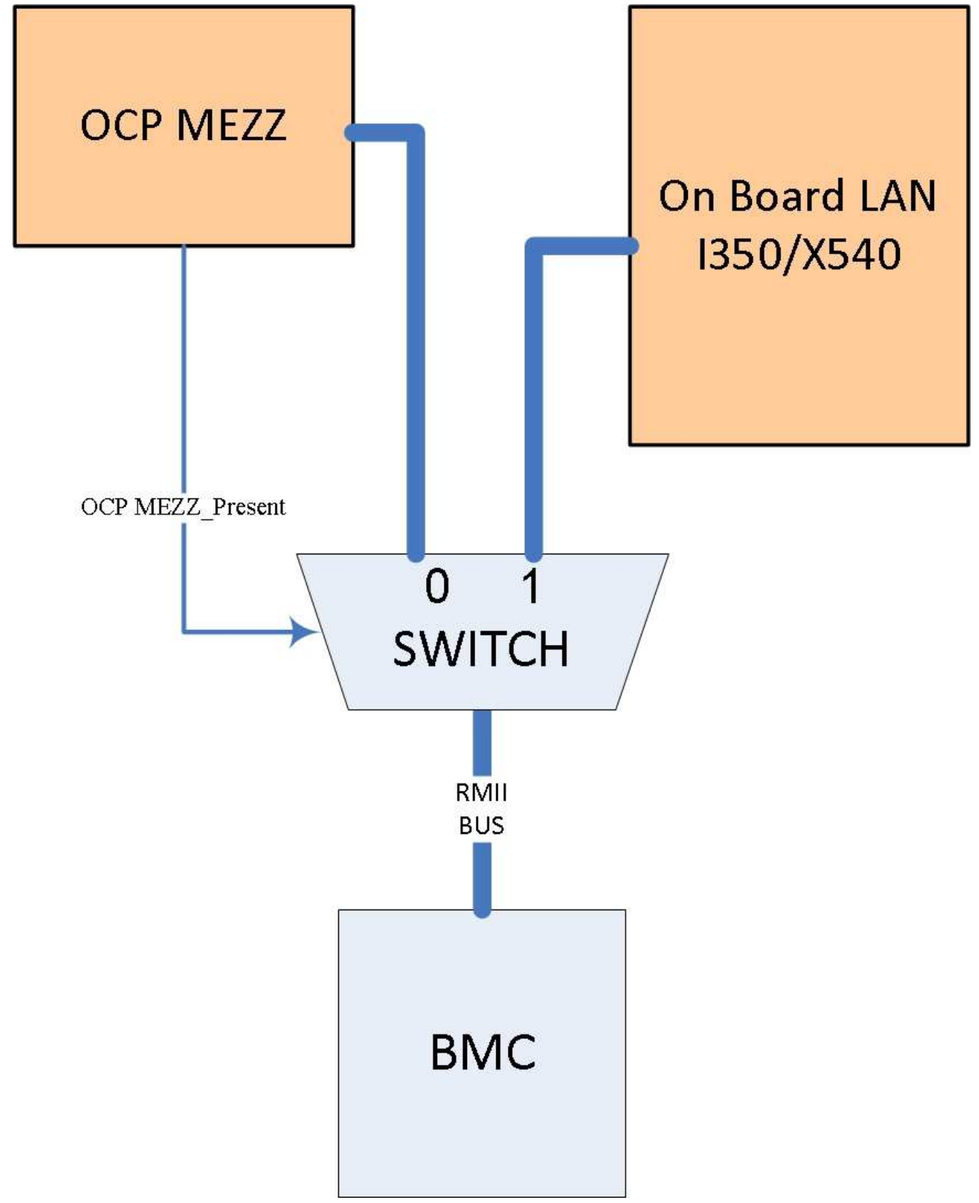
10K OHM FOR AST2300




BMC CO-LAY OPTION

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NAME | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: NAME | SIZE: C | DATE: Mon Nov 16 11:54:18 2015 | SHEET: 108 OF 188 |



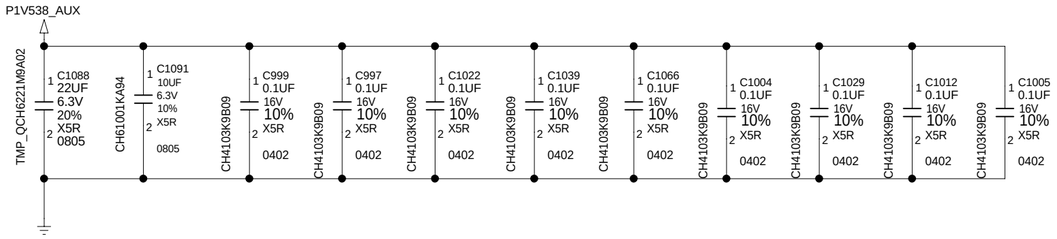



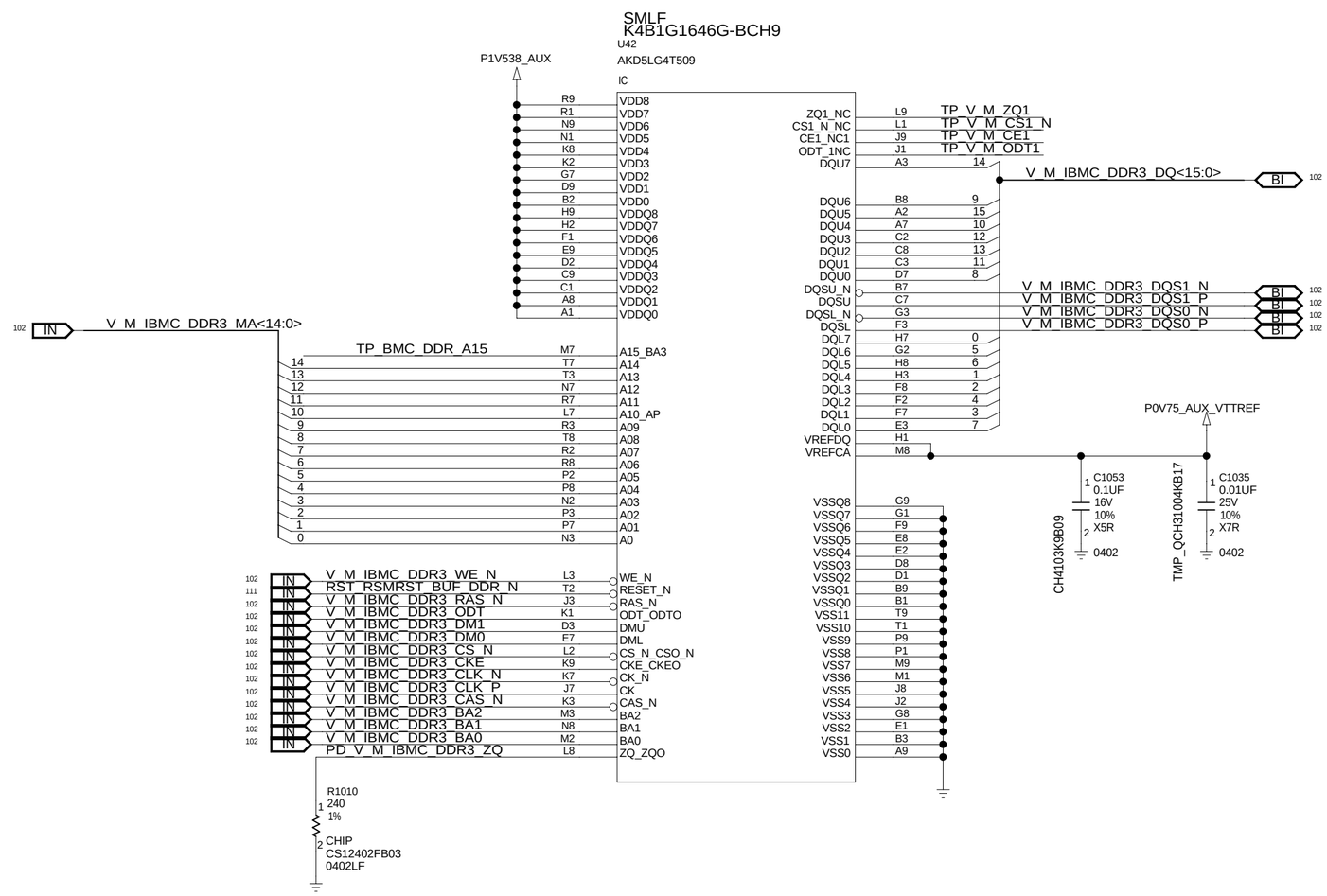

# BMC NCSI MUX

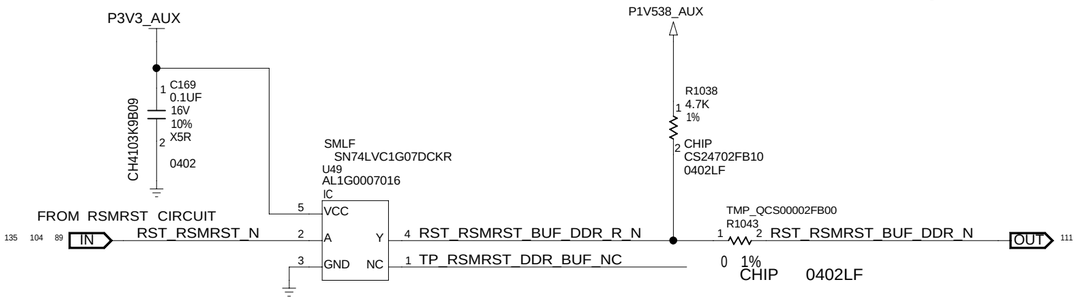
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER KOOL | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,COSMO,MATT | SIZE C DATE Mon Nov 16 11:54:19 2015 | SHEET 109 OF 188 | |

BLANK

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NAME | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER NAME | SIZE C | DATE Wed Jul 24 08:30:14 2013 | SHEET 110 OF 188 | |

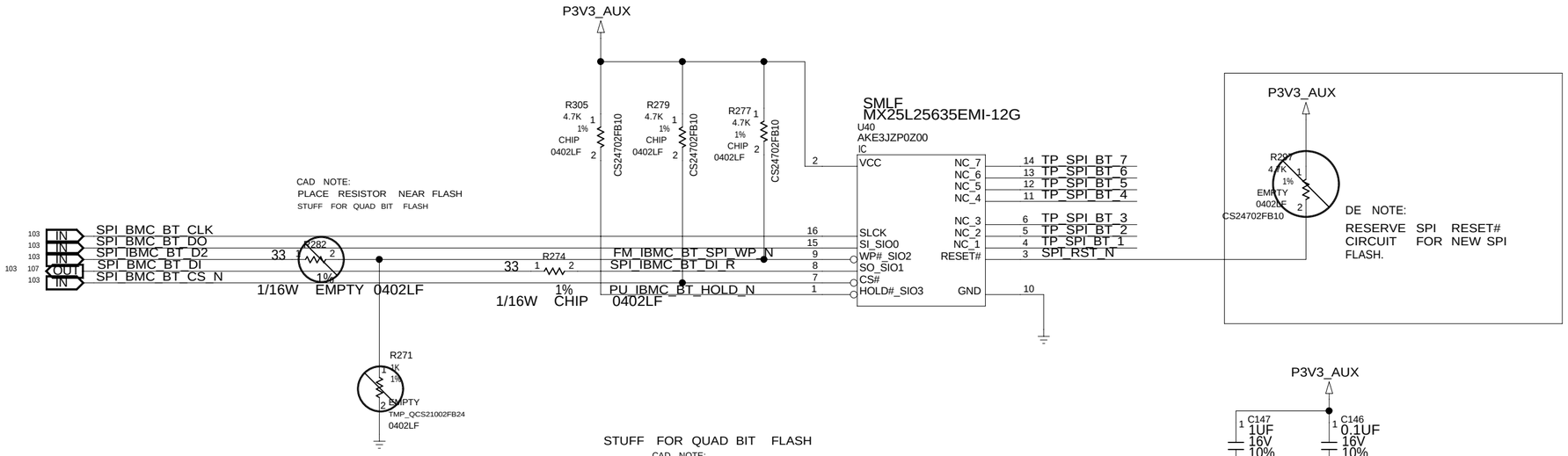



# BMC DDRIII SDRAM

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER KOOL | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | | |
| | | REVIEWER PETER,COSMO,MATT | SIZE C | DATE Mon Nov 16 11:54:20 2015 | SHEET 111 OF 188 | | |




STUFF FOR QUAD BIT FLASH

CAD NOTE:
THIS PART WILL BE IN SOCKET
USE ALT SYMBOL ASSOCIATED WITH PART FOOTPRINT
BOM NOTE: SOCKET IS D91187-001

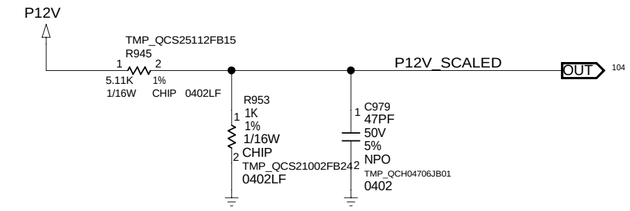
BOM NOTE
PULL-DOWN WRITE PROTECT
FOR FLASH PROTECTION
PULL-UP (DEFAULT)

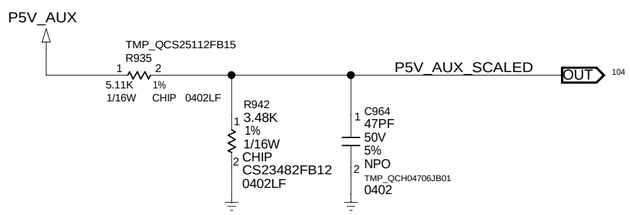
BOM NOTES:
AST2400 (FLASH SIZE=256MBIT/32MBYTE)
SOIC16 :
AKE3JZP0Z00 (MX25L25635EMI-12G) : SOIC16 300MIL
BMC_FLASH

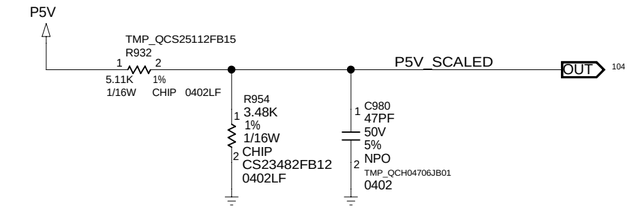
BMC_FLASH1
NA

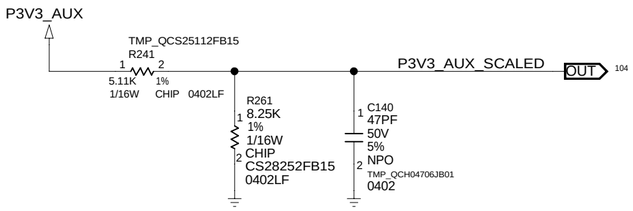
# BMC SPI FLASH

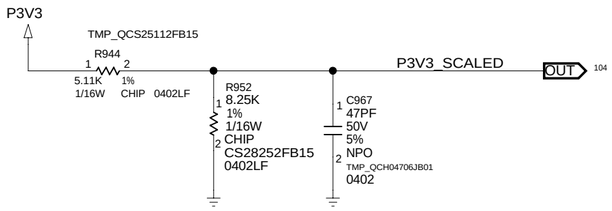
| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER KOOL | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER PETER,COSMO,MATT | SIZE C | DATE Mon Nov 16 11:54:21 2015 | SHEET 112 OF 188 | |

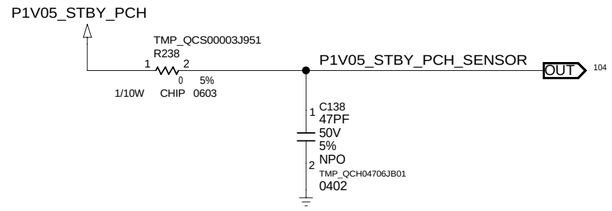


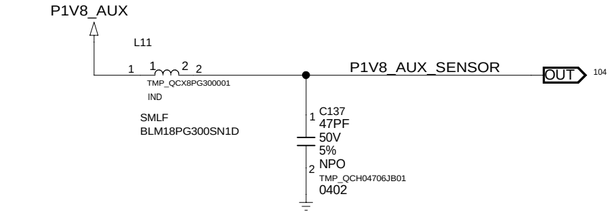



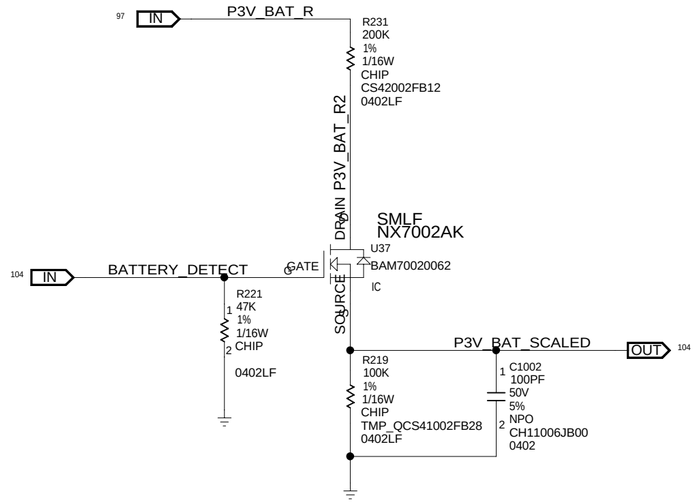



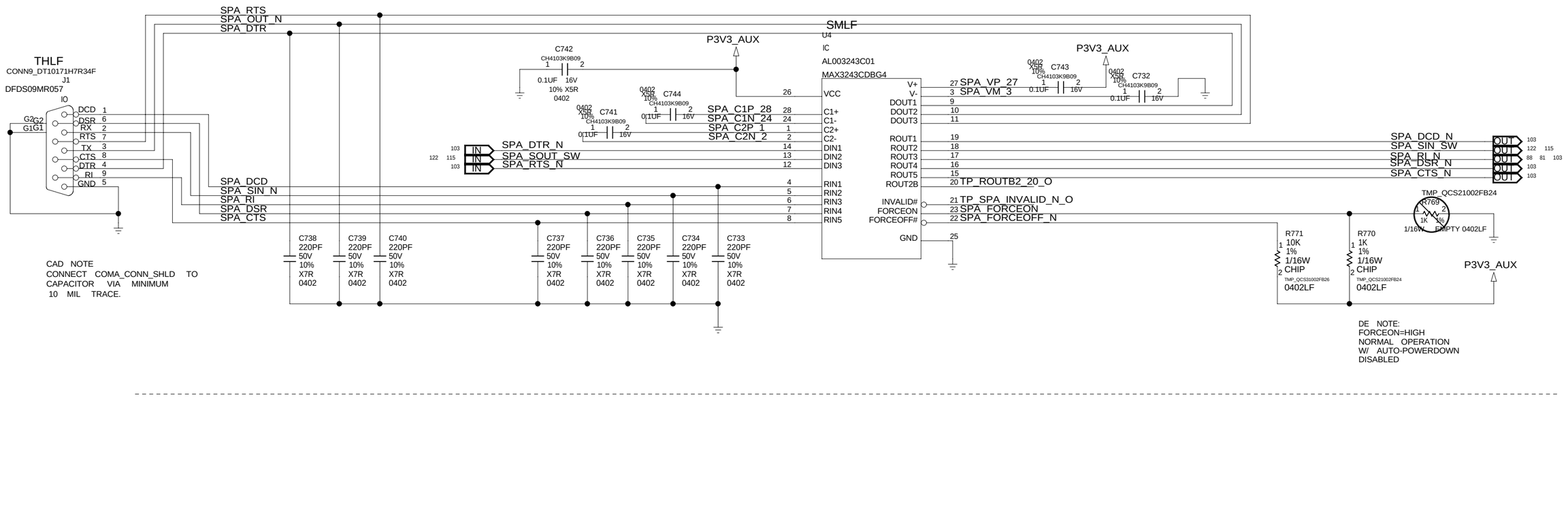




CAD NOTE:
ROUTE ALL ADC NETS AT 6 MILS WIDE

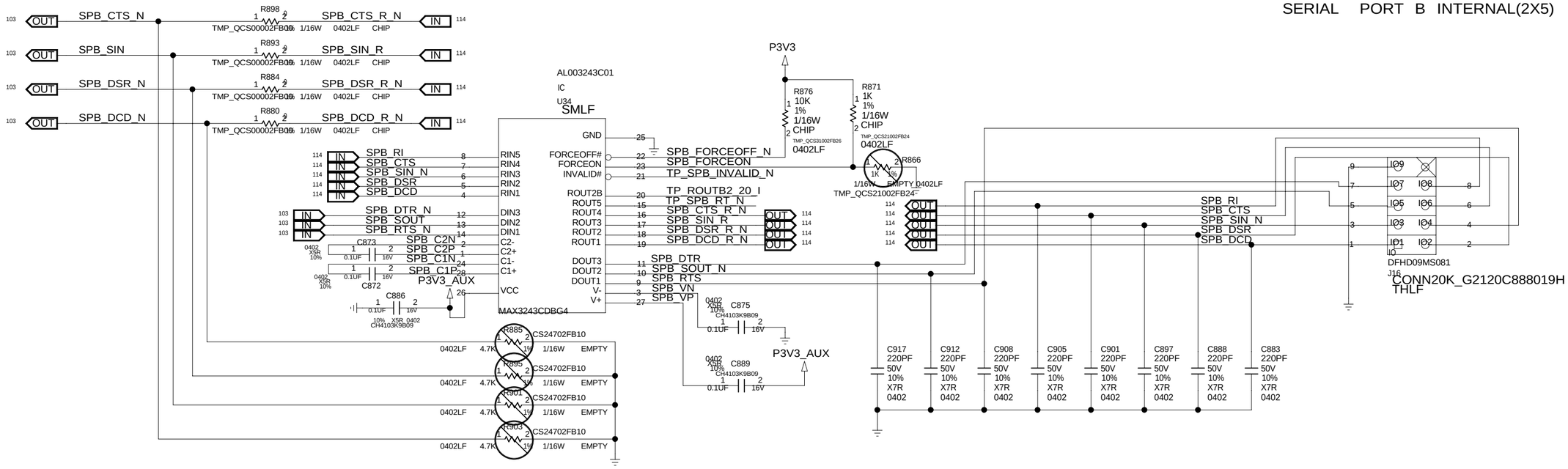
# BMC VOLTAGE SENSOR

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER KOOL | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | | |
| | | REVIEWER PETER,COSMO,MATT | SIZE C | DATE Mon Nov 16 11:54:22 2015 | SHEET 113 OF 188 | | |

# SERIAL PORT A EXTERNAL (DB9)

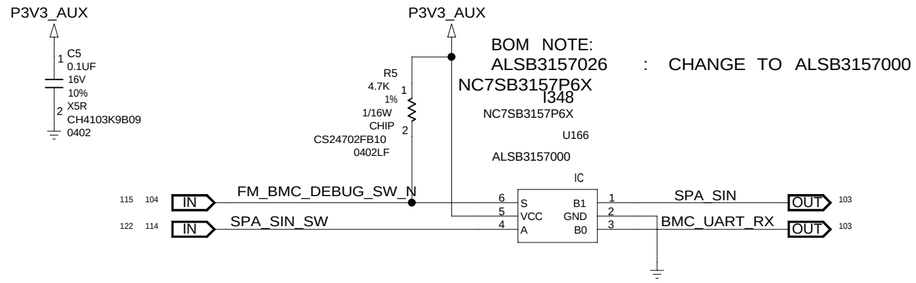


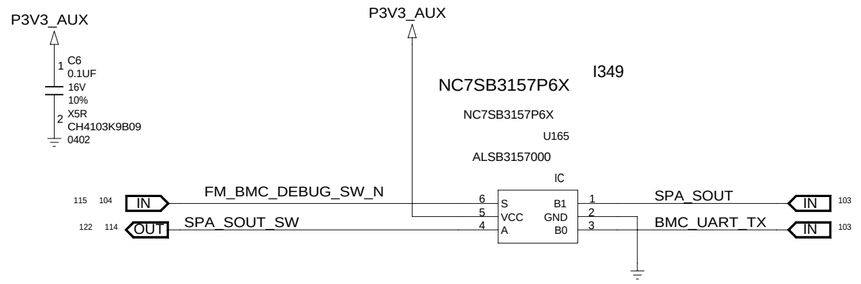

# SERIAL PORT B INTERNAL(2X5)

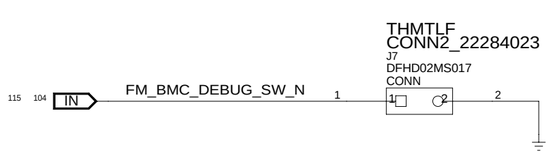



BMC SERIAL PORT A AND B

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:54:24 2015 | SHEET 114 OF 188 | |



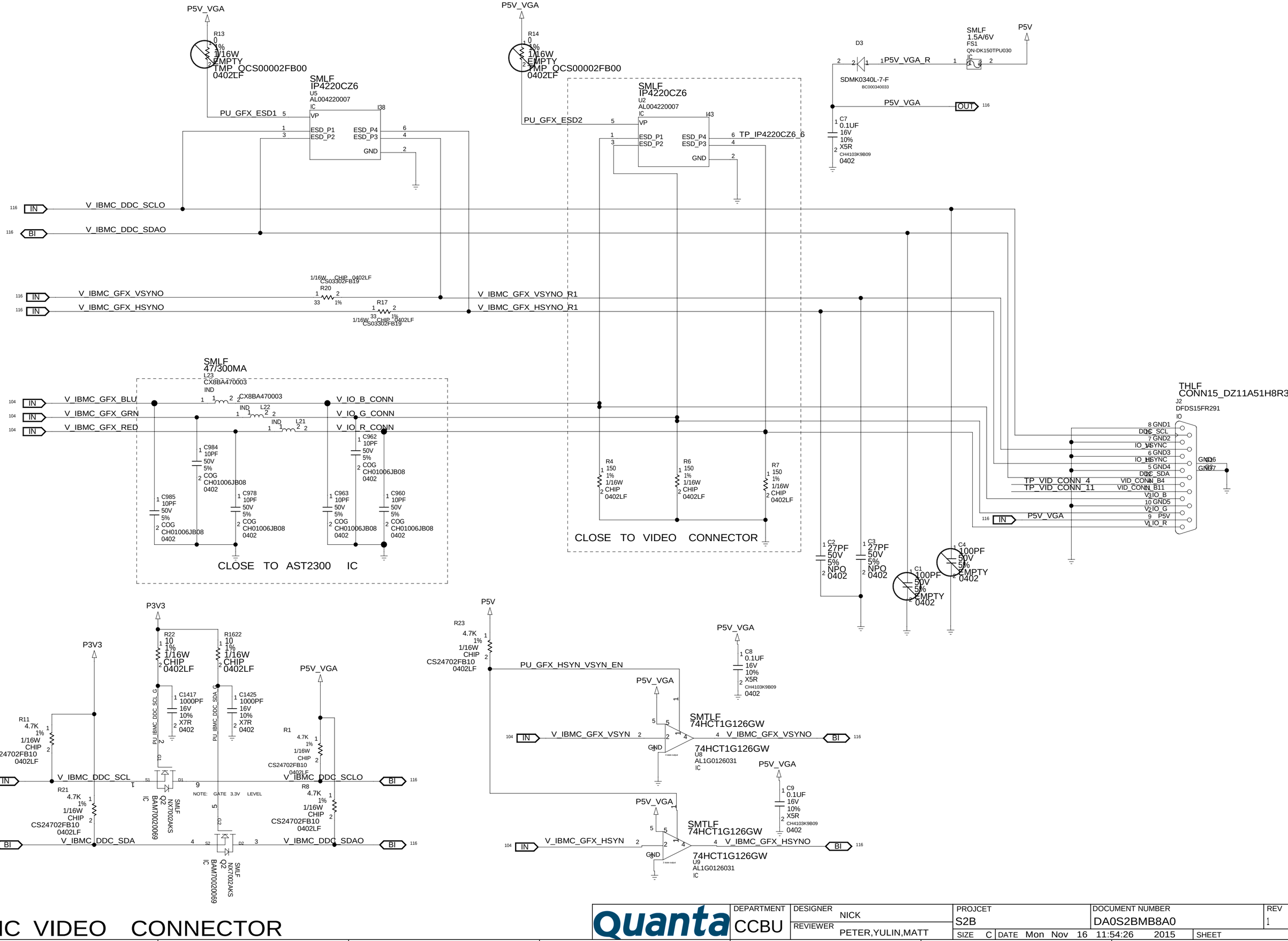




| | COM-BMC_DEBUG | COM-SYSTEM | COM |
|---|---|---|---|
| BMC_DEBUG_SW_N | L(1-2) | H(DEFULT | DE-POP JUMPER) |

# MUX:COM-BMC_DEBUG / COM-SYSTEM

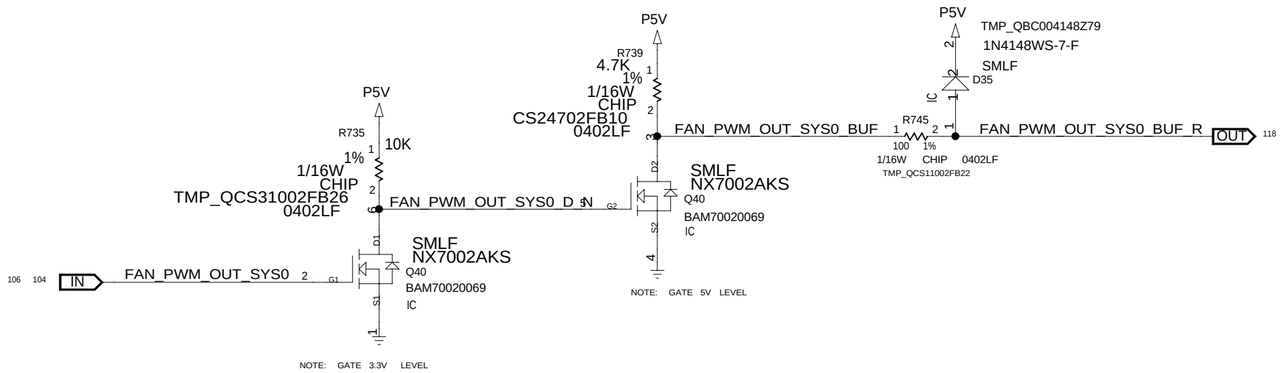
BMC SERIAL PORT MUX

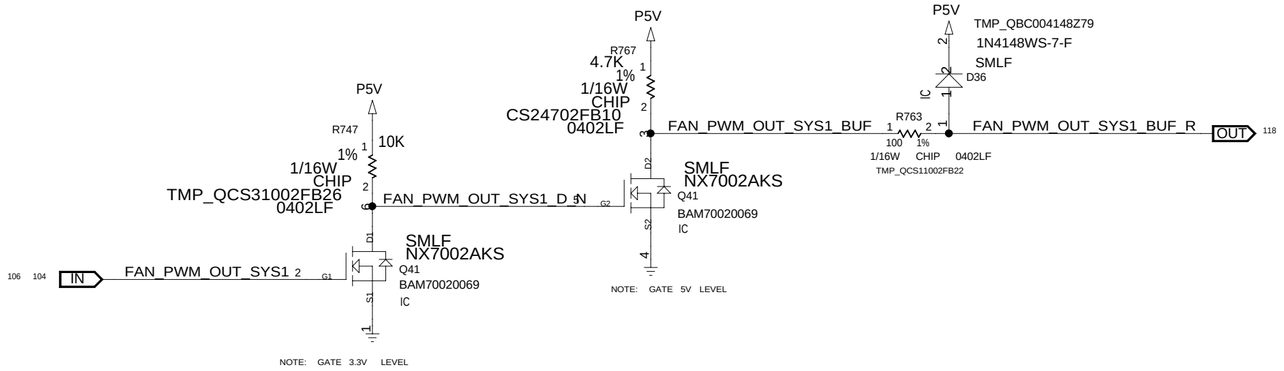
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C DATE: Mon Nov 16 11:54:25 2015 | SHEET: 115 OF 188 | |

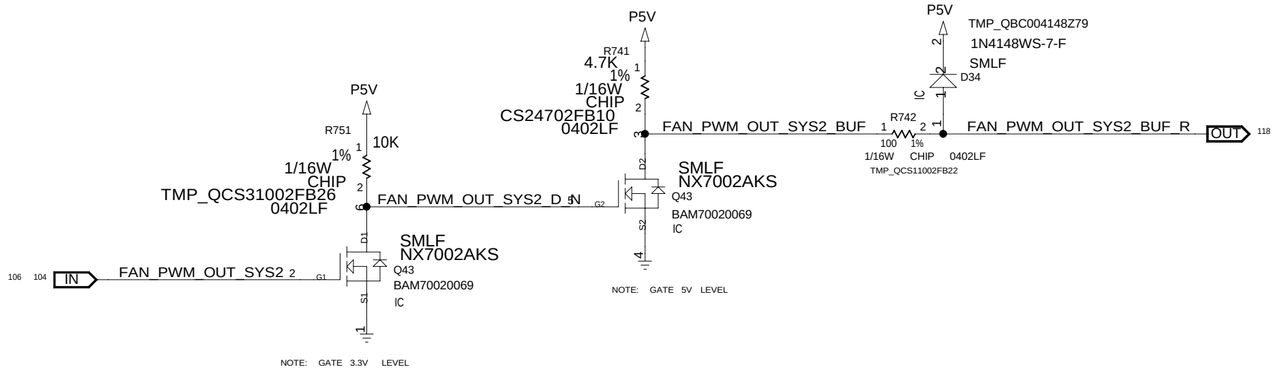


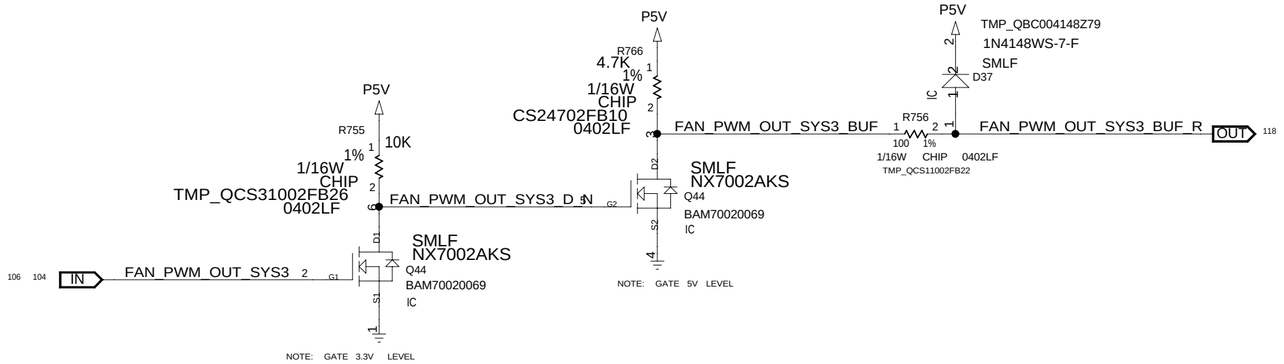

# BMC VIDEO CONNECTOR

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:54:26 2015 | SHEET 116 OF 188 |



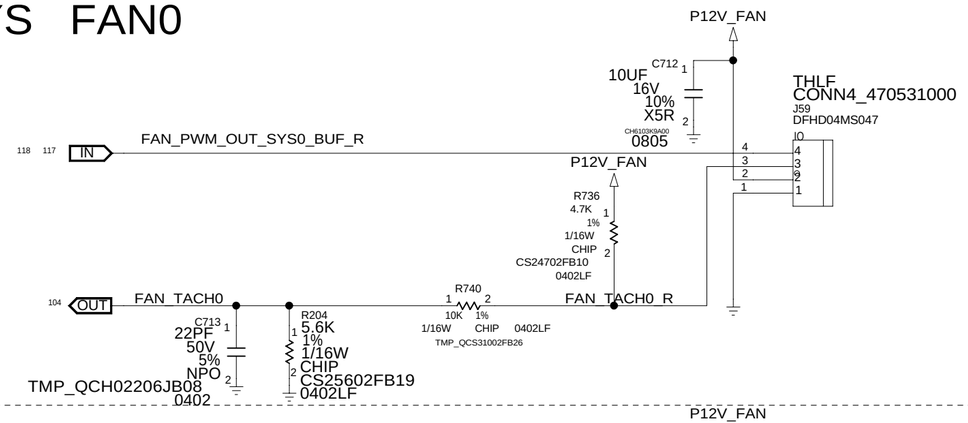



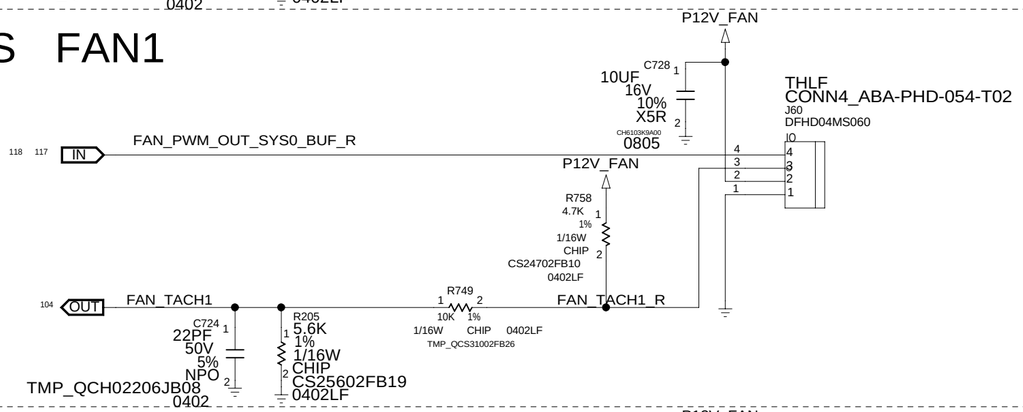

# BMC SYSTEM FAN PWM

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: NICK,PETER,MATT | SIZE: C | DATE: Mon Nov 16 11:54:28 2015 | SHEET: 117 OF 188 |

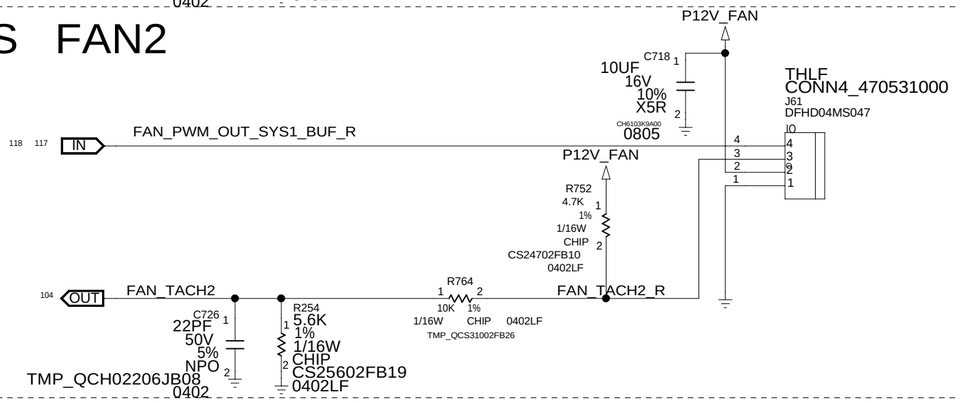
## SYS FAN0



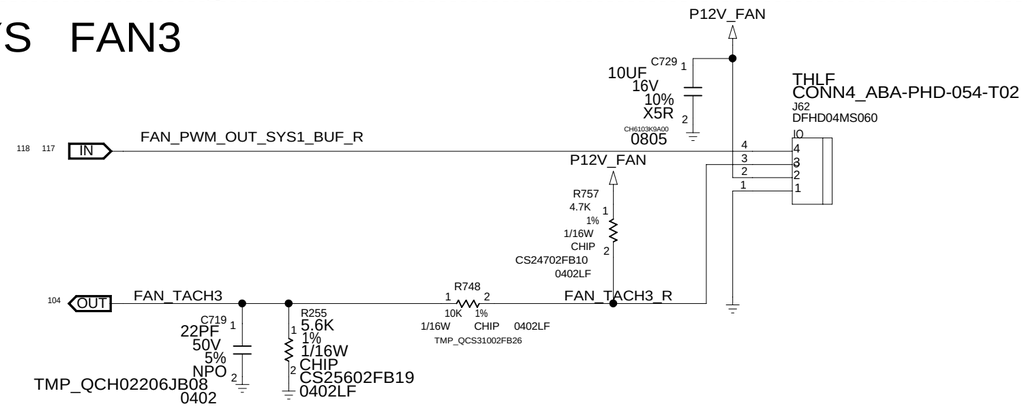

## SYS FAN1



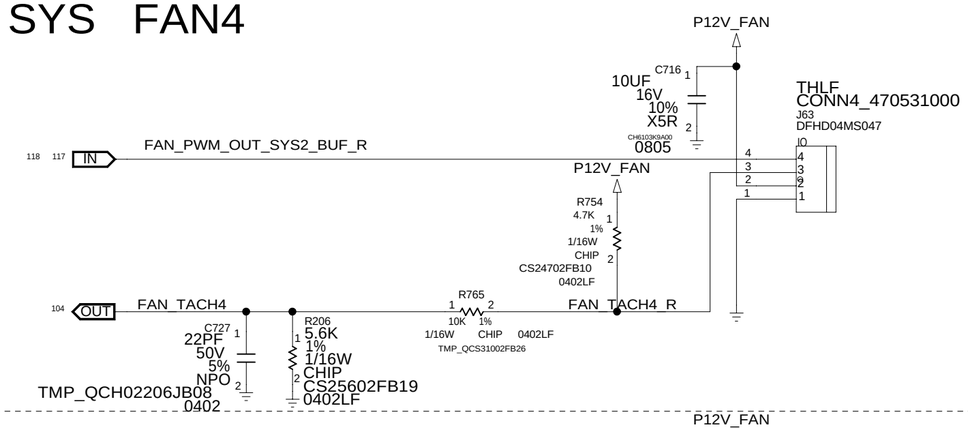

## SYS FAN2



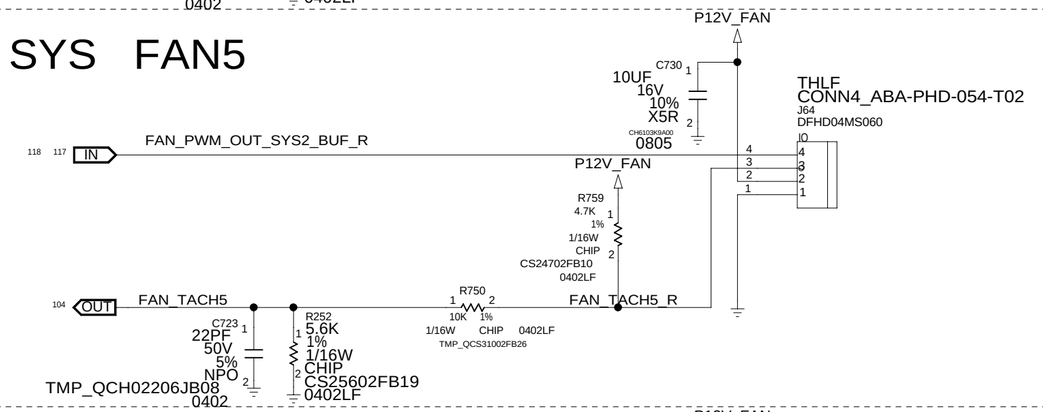

## SYS FAN3



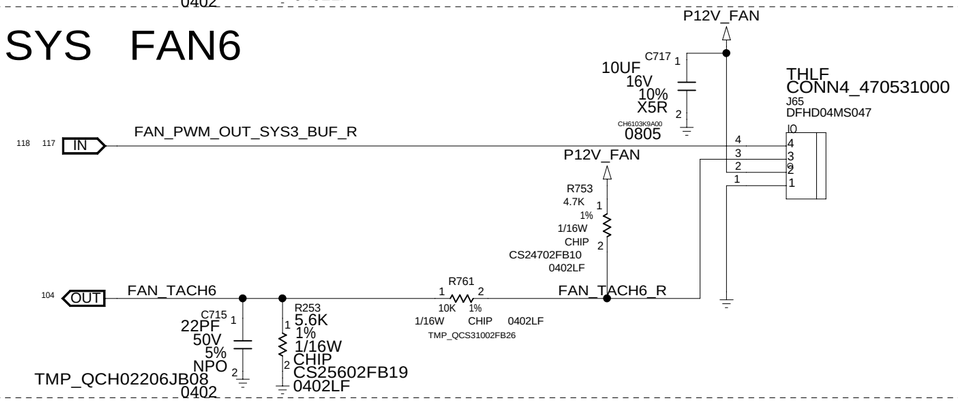

## SYS FAN4



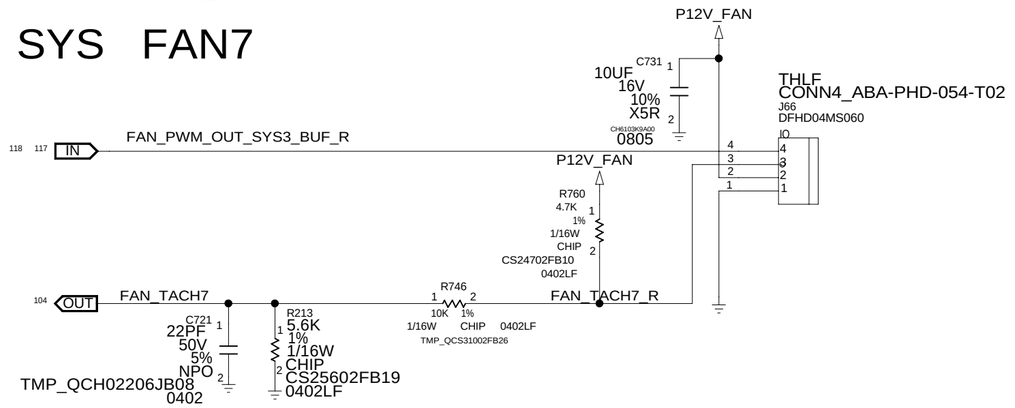

## SYS FAN5




## SYS FAN6

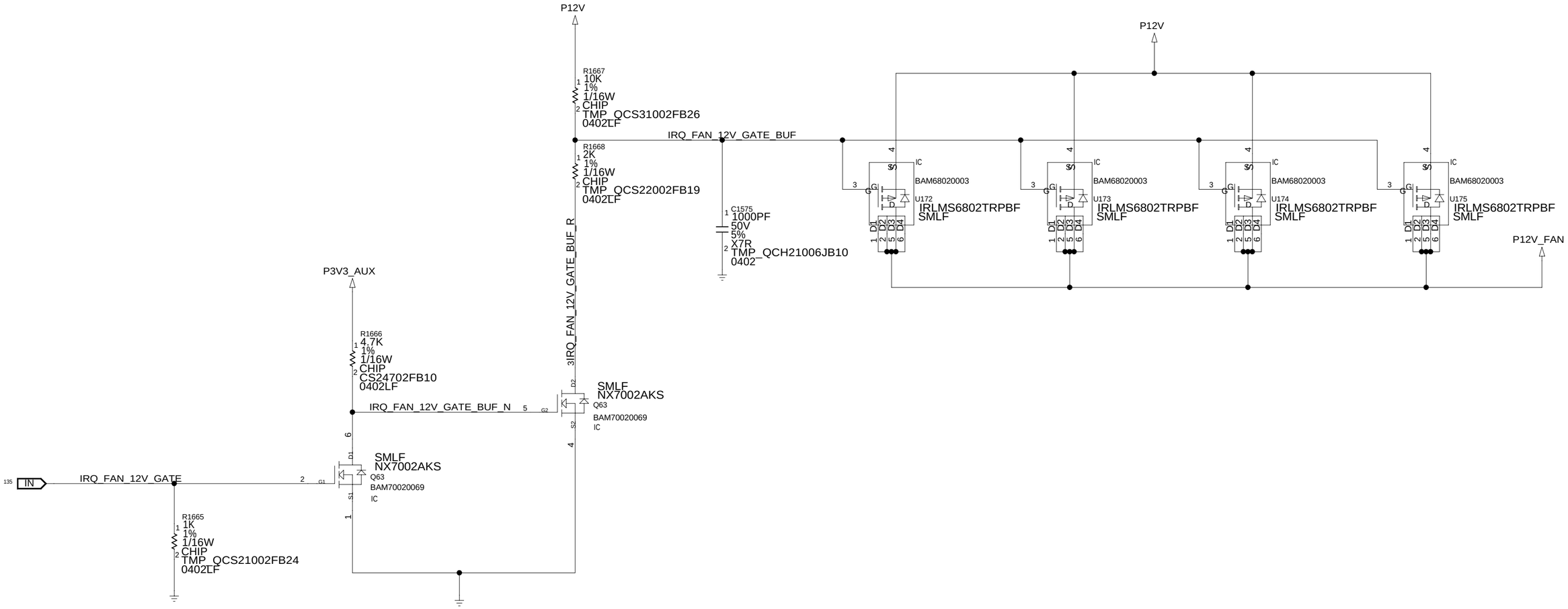



## SYS FAN7




# BMC SYSTEM FAN CONNECTORS (1 OF 2)

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: NICK,PETER,MATT | SIZE: C | DATE: Mon Nov 16 11:54:30 2015 | SHEET: 118 OF 188 |




# BMC SYSTEM FAN CONNECTORS (2 OF 2)

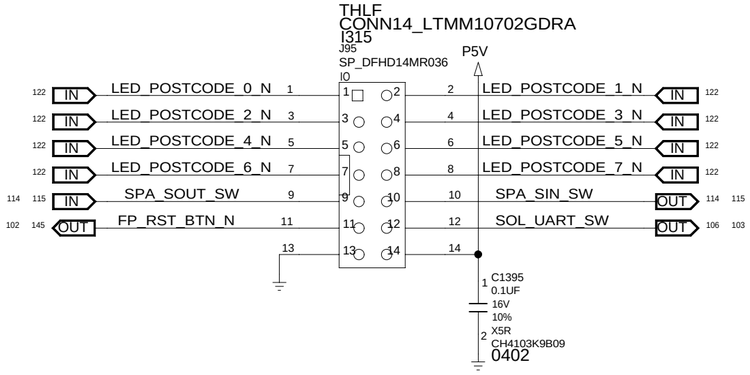
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:54:28 2015 | SHEET: 119 OF 188 |

BLANK

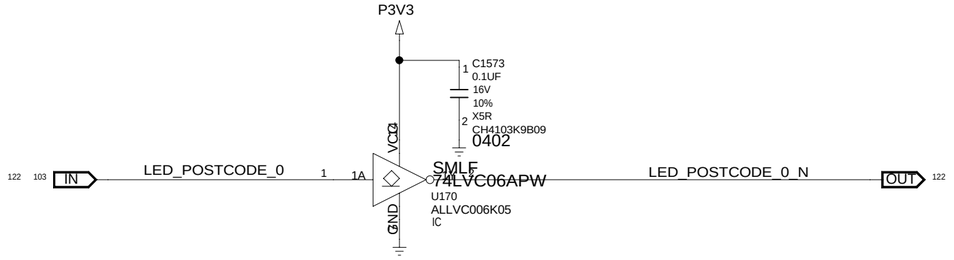
| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Fri Jul 05 09:07:10 2013 | SHEET 120 OF 188 | |

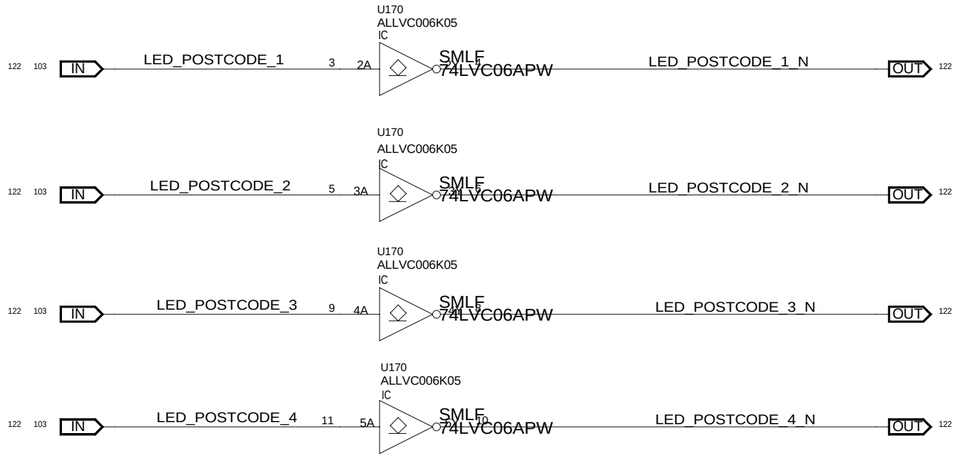
BLANK

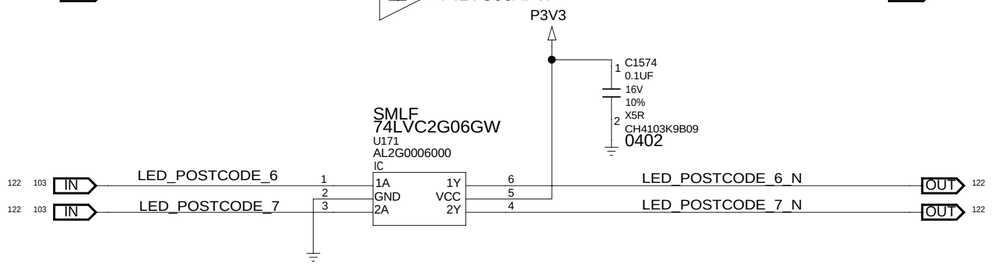
| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Fri Jul 05 09:06:22 2013 | SHEET 121 OF 188 | |

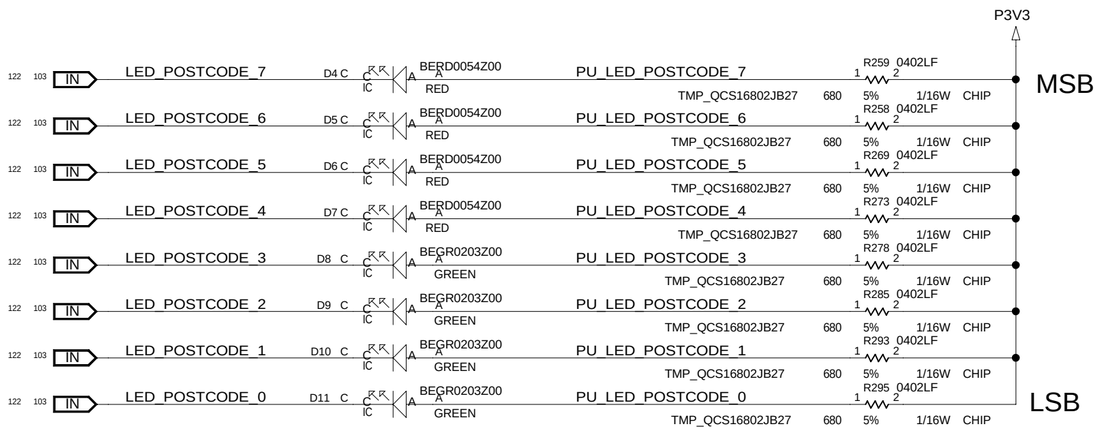


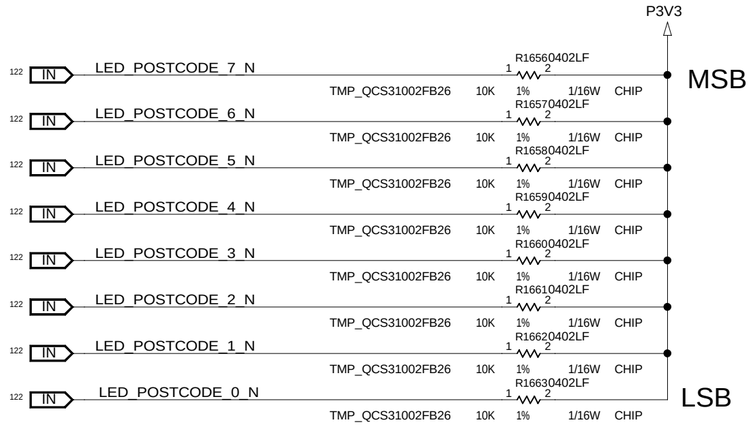

# SIO 80 PORT




BMC PORT80

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:54:31 2015 | SHEET: 122 OF 188 |

BOM NOTE
I350 PN: AJSLJ3Y0T00
X540 PN: AJSLJEJ0T00

U31
AJ0BHPC0T00
IC
Twinville
X540
BGA
TWINVILLE_X540

131 BI NIC_A_MDI_DP<4..0>
131 BI NIC_A_MDI_DN<4..0>
4 A11 MDI0_4P / B11 MDI0_4N
3 A9 MDI0_3P / B9 MDI0_3N
2 A7 MDI0_2P / B7 MDI0_2N
1 A5 MDI0_1P / B5 MDI0_1N
0 A3 MDI0_0P / B3 MDI0_0N

132 BI NIC_B_MDI_DP<4..0>
132 BI NIC_B_MDI_DN<4..0>
4 A14 MDI1_4P / B14 MDI1_4N
3 A16 MDI1_3P / B16 MDI1_3N
2 A18 MDI1_2P / B18 MDI1_2N
1 A20 MDI1_1P / B20 MDI1_1N
0 A22 MDI1_0P / B22 MDI1_0N

129 IN P2E_CPU0_PCIE1_TX_C_DP<7:0>
129 IN P2E_CPU0_PCIE1_TX_C_DN<7:0>
7 AB23 PER_7P / AB24 PER_7N
6 AD19 PER_6P / AC19 PER_6N
5 AD18 PER_5P / AC18 PER_5N
4 AD13 PER_4P / AC13 PER_4N
3 AD12 PER_3P / AC12 PER_3N
2 AD7 PER_2P / AC7 PER_2N
1 AD6 PER_1P / AC6 PER_1N
0 AB2 PER_0P / AB1 PER_0N

141 IN CLK_100M_LAN_DP
141 IN CLK_100M_LAN_DN
Y2 PE_CLKP / Y1 PE_CLKN

NIC_PE_RBIAS_1 V2 PE_RBIAS1
NIC_PE_RBIAS_0 V1 PE_RBIAS0

73 71 136 135 IN RST_PERST0_N W2 PE_RST_N

LED0_3 K4 NIC0_LED03_1G_LVT2
LED0_2 J4 NIC0_LED02_ACT_LVT2_N
LED0_1 J3 NIC0_LED01_10G_LVT2
LED0_0 H4 NIC0_LED00_LINKUP_LVT2_N
OUT 131 / OUT 146 / OUT 131 / OUT 146

SDP0_3 R3 TP_SDP0_3
SDP0_2 T4 TP_SDP0_2
SDP0_1 P3 TP_SDP0_1
SDP0_0 R4 TP_SDP0_0

LED1_3 K22 NIC1_LED13_1G_LVT2
LED1_2 K21 NIC1_LED12_ACT_LVT2_N
LED1_1 J22 NIC1_LED11_10G_LVT2
LED1_0 J21 NIC1_LED10_LINKUP_LVT2_N
OUT 132 / OUT 146 / OUT 132 / OUT 146

SDP1_3 U22 TP_SDP1_3
SDP1_2 U21 TP_SDP1_2
SDP1_1 T22 TP_SDP1_1
SDP1_0 T21 TP_SDP1_0

PHY1_RVSL V23 NIC_PHY1_RVSL
PHY0_RVSL T3 NIC_PHY0_RVSL
IN 123 / IN 123

PET_7P AC22 / PET_7N AD22 — 7
PET_6P AC21 / PET_6N AD21 — 6
PET_5P AC16 / PET_5N AD16 — 5
PET_4P AC15 / PET_4N AD15 — 4
PET_3P AC10 / PET_3N AD10 — 3
PET_2P AC9 / PET_2N AD9 — 2
PET_1P AC4 / PET_1N AD4 — 1
PET_0P AC3 / PET_0N AD3 — 0

P2E_CPU0_PCIE1_RX_DP<7:0> OUT 129
P2E_CPU0_PCIE1_RX_DN<7:0> OUT 129

PE_WAKE_N W1 — IRQ_LVC3_WAKE_N — OUT 71 72 73 102 82

P3V3_AUX
TMP_QCS31002FB26
R187 10K

P2V1_SGVL_P2V5_X540_P3V3_I350

R181 10K 1% 1/16W EMPTY TMP_QCS31002FB26 0402LF
R176 10K 1% 1/16W EMPTY TMP_QCS31002FB26 0402LF
123 OUT NIC_PHY1_RVSL
123 OUT NIC_PHY0_RVSL
R188 3.3K 1% 1/16W EMPTY TMP_QCS23302FB12 0402LF
R170 3.3K 1% 1/16W EMPTY TMP_QCS23302FB12 0402LF

POPULATE THIS RESISTOR
IF I350 IS BEING USED
UNPOPULATE IF
TWINVILLE IS BEING USED

R185 1.5K 1% 1/16W CHIP 0402LF CS21502FB14

R182 3.01K 1% 1/16W EMPTY CS23012FB16 0402LF
R179 3.01K 1% 1/16W EMPTY CS23012FB16 0402LF

POPULATE THESE RESISTORS
IF TWINVILLE IS BEING USED
UNPOPULATE
IF I350 IS BEING USED

CAD NOTE:
PLACE CLOSE TO SILICON. TOTAL
PE_RBIAS0 PE_RBAIS1
TRACE LENGTH SHOULD BE
LESS THAN 1 INCH.

UNPOPULATE FOR SAGEVILLE
R185, R182, R179

FOX X540 PHY MDI LANE SWAPSL CONFIGURATION
DEFAULT CONFIGURATION - 0,1,2,3 <-> A,B,C,D
CONNECT PHY0_RVSL SIGNAL TO GND VIA 3.3KOHM PULL DOWN
CONNECT PHY1_RVSL SIGNAL TO GND VIA 3.3KOHM PULL DOWN

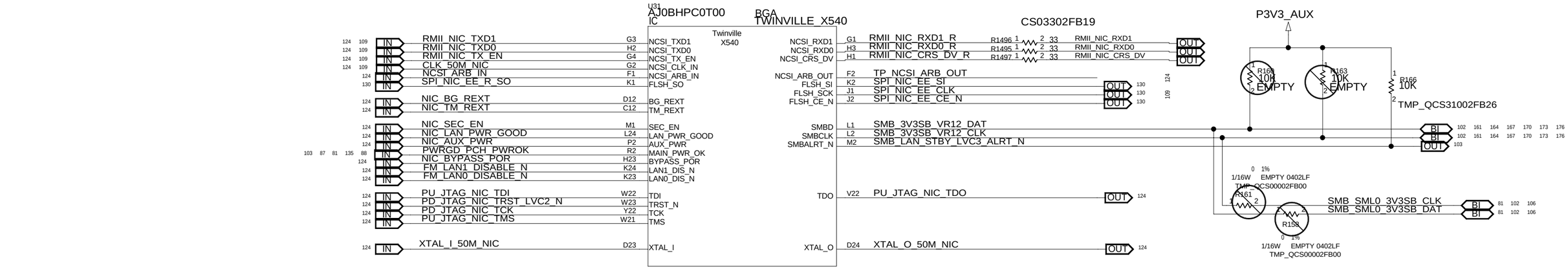
MDI SWAPS CONFIGURATION - 3,2,1,0 <-> A,B,C,D
CONNECT PHY0_RVSL SIGNAL TO 2.5V VIA 10KOHM PULL UP
CONNECT PHY1_RVSL SIGNAL TO 2.5V VIA 10KOHM PULL UP

FOX I350-BT2 PHY MDI LANE SWAPSL CONFIGURATION
USE EEPROM SETTING
DEFAULT CONFIGURATION - 0,1,2,3 <-> A,B,C,D
MDI SWAPS CONFIGURATION - 3,2,1,0 <-> A,B,C,D

# FOR I350

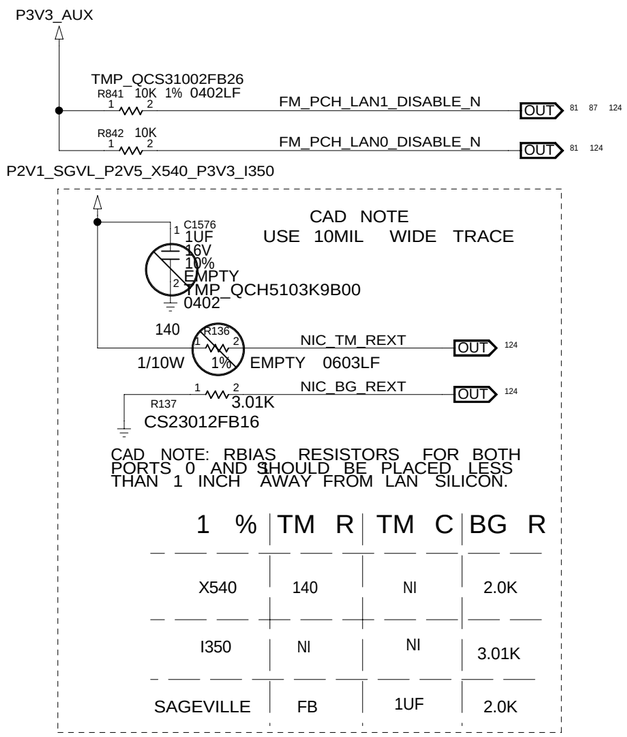
POWERVILLE 1 OF 6

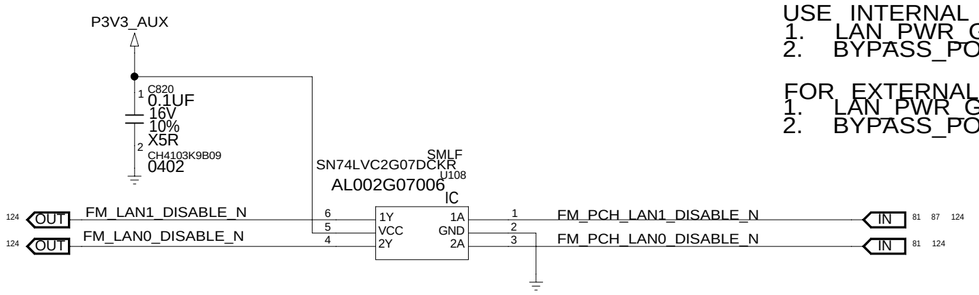
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER JOSEPH | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER NICK,PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:54:33 2015 | SHEET 123 OF 188 |

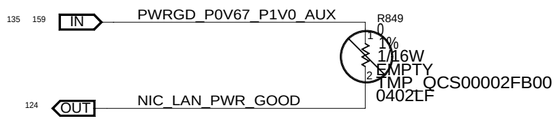


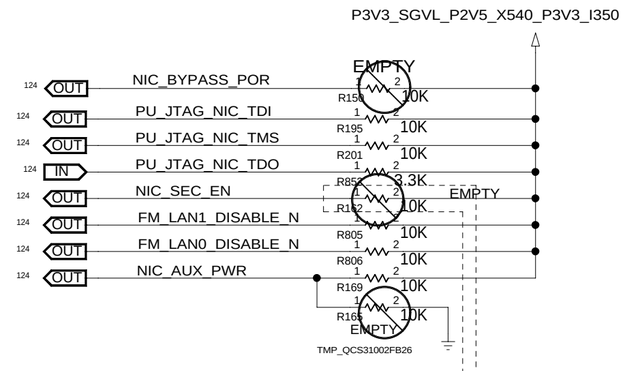

USE INTERNAL POR AS DEFAULT
1. LAN PWR GOOD SIGNAL TO BE CONNECTED TO PULL UP
2. BYPASS_POR SIGNAL TO BE CONNECTED TO PULL DOWN

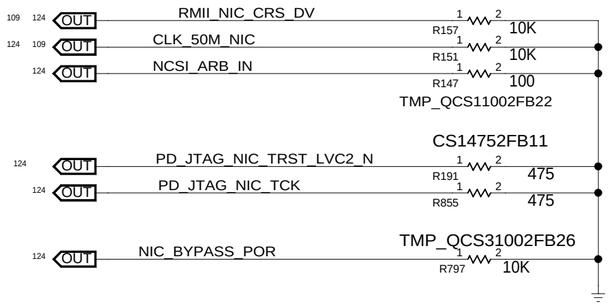
FOR EXTERNAL POWER ON RESET USE:
1. LAN PWR GOOD SIGNAL
2. BYPASS_POR SIGNAL TO BE CONNECTED TO PULL UP

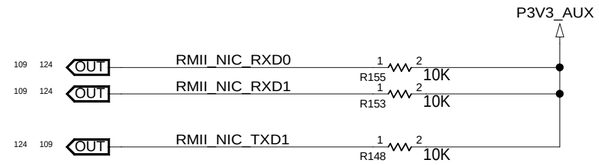


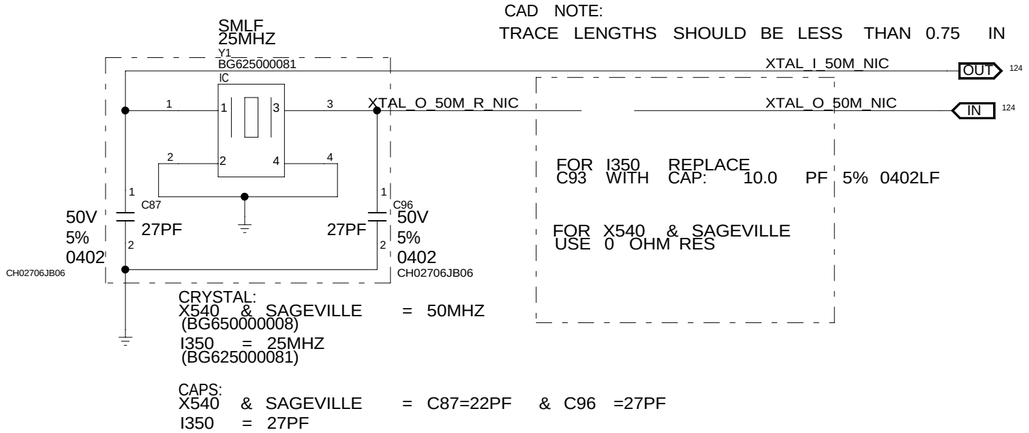



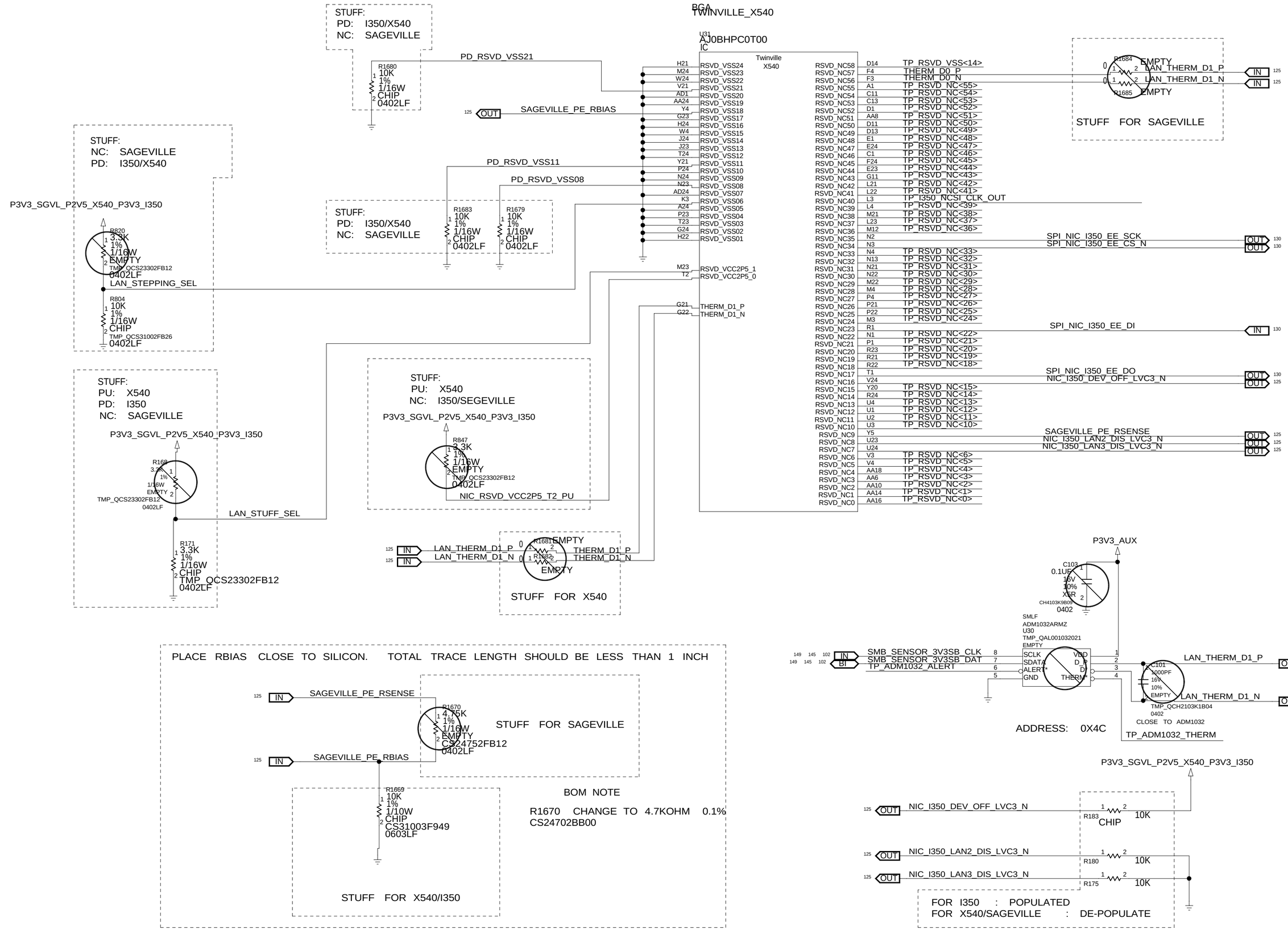






| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER JOSEPH | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | | |
| | | REVIEWER NICK,PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:54:35 2015 | SHEET 124 OF 188 | | |




POWERVILLE 3 OF 6

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER JOSEPH | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | | REV 1 |
| | | REVIEWER NICK,PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:54:36 2015 | SHEET 125 | OF 188 |

BGA
TWINVILLE_X540

P0V85_SGVL_P0V8_X540_P1V0_I350

P0V85_SGVL_P0V67_X540_P1V0_I350

U31
AJ0BHPC0T00
IC

Twinville
X540

| | | | |
|---|---|---|---|
| G13 | VCC_0P8_42 | VCC_0P65_40 | G5 |
| G15 | VCC_0P8_41 | VCC_0P65_39 | G7 |
| G17 | VCC_0P8_40 | VCC_0P65_38 | G9 |
| G19 | VCC_0P8_39 | VCC_0P65_37 | H10 |
| H14 | VCC_0P8_38 | VCC_0P65_36 | H12 |
| H16 | VCC_0P8_37 | VCC_0P65_35 | H6 |
| H18 | VCC_0P8_36 | VCC_0P65_34 | H8 |
| H20 | VCC_0P8_35 | VCC_0P65_33 | J11 |
| J13 | VCC_0P8_34 | VCC_0P65_32 | J5 |
| J15 | VCC_0P8_33 | VCC_0P65_31 | J7 |
| J17 | VCC_0P8_32 | VCC_0P65_30 | J9 |
| J19 | VCC_0P8_31 | VCC_0P65_29 | K10 |
| K14 | VCC_0P8_30 | VCC_0P65_28 | K12 |
| K16 | VCC_0P8_29 | VCC_0P65_27 | K6 |
| K18 | VCC_0P8_28 | VCC_0P65_26 | K8 |
| K20 | VCC_0P8_27 | VCC_0P65_25 | L11 |
| L13 | VCC_0P8_26 | VCC_0P65_24 | L7 |
| L15 | VCC_0P8_25 | VCC_0P65_23 | L9 |
| L17 | VCC_0P8_24 | VCC_0P65_22 | M10 |
| L19 | VCC_0P8_23 | VCC_0P65_21 | M8 |
| M14 | VCC_0P8_22 | VCC_0P65_20 | N11 |
| M16 | VCC_0P8_21 | VCC_0P65_19 | N7 |
| M18 | VCC_0P8_20 | VCC_0P65_18 | N9 |
| N15 | VCC_0P8_19 | VCC_0P65_17 | P10 |
| N17 | VCC_0P8_18 | VCC_0P65_16 | P12 |
| P14 | VCC_0P8_17 | VCC_0P65_15 | P8 |
| P16 | VCC_0P8_16 | VCC_0P65_14 | R11 |
| P18 | VCC_0P8_15 | VCC_0P65_13 | R7 |
| R13 | VCC_0P8_14 | VCC_0P65_12 | R9 |
| R15 | VCC_0P8_13 | VCC_0P65_11 | T10 |
| R17 | VCC_0P8_12 | VCC_0P65_10 | T12 |
| T14 | VCC_0P8_11 | VCC_0P65_09 | T8 |
| T16 | VCC_0P8_10 | VCC_0P65_08 | U11 |
| T18 | VCC_0P8_09 | VCC_0P65_07 | U7 |
| U13 | VCC_0P8_08 | VCC_0P65_06 | U9 |
| U15 | VCC_0P8_07 | VCC_0P65_05 | V10 |
| U17 | VCC_0P8_06 | VCC_0P65_04 | V12 |
| V14 | VCC_0P8_05 | VCC_0P65_03 | V8 |
| V16 | VCC_0P8_04 | VCC_0P65_02 | W11 |
| V18 | VCC_0P8_03 | VCC_0P65_01 | W7 |
| W13 | VCC_0P8_02 | VCC_0P65_00 | W9 |
| W15 | VCC_0P8_01 | | |
| W17 | VCC_0P8_00 | | |

P0V85_SGVL_P0V8_X540_P1V0_I350

C789 22UF 6.3V 20% X5R 0805
C95 22UF 6.3V 20% X5R 0805
C97 22UF 6.3V 20% X5R 0805
C89 22UF 6.3V 20% X5R 0805
C845 22UF 6.3V 20% X5R 0805
C783 22UF 6.3V 20% X5R 0805
C810 22UF 6.3V 20% X5R 0805
C821 22UF 6.3V 20% X5R 0805
C828 22UF 6.3V 20% X5R 0805
TMP_QCH6221M9A02

C827 1UF 16V 10% X5R 0402
C808 1UF 16V 10% X5R 0402
C811 1UF 16V 10% X5R 0402
C871 1UF 16V 10% X5R 0402
C817 1UF 16V 10% X5R 0402
C822 1UF 16V 10% X5R 0402
C832 1UF 16V 10% X5R 0402
C838 1UF 16V 10% X5R 0402
C851 1UF 16V 10% X5R 0402

C831 1UF 16V 10% X5R 0402
C856 1UF 16V 10% X5R 0402
C824 1UF 16V 10% X5R 0402
C839 1UF 16V 10% X5R 0402
C826 1UF 16V 10% X5R 0402
C830 1UF 16V 10% X5R 0402
C865 1UF 16V 10% X5R 0402
C862 1UF 16V 10% X5R 0402
C860 1UF 16V 10% X5R 0402

P0V85_SGVL_P0V67_X540_P1V0_I350

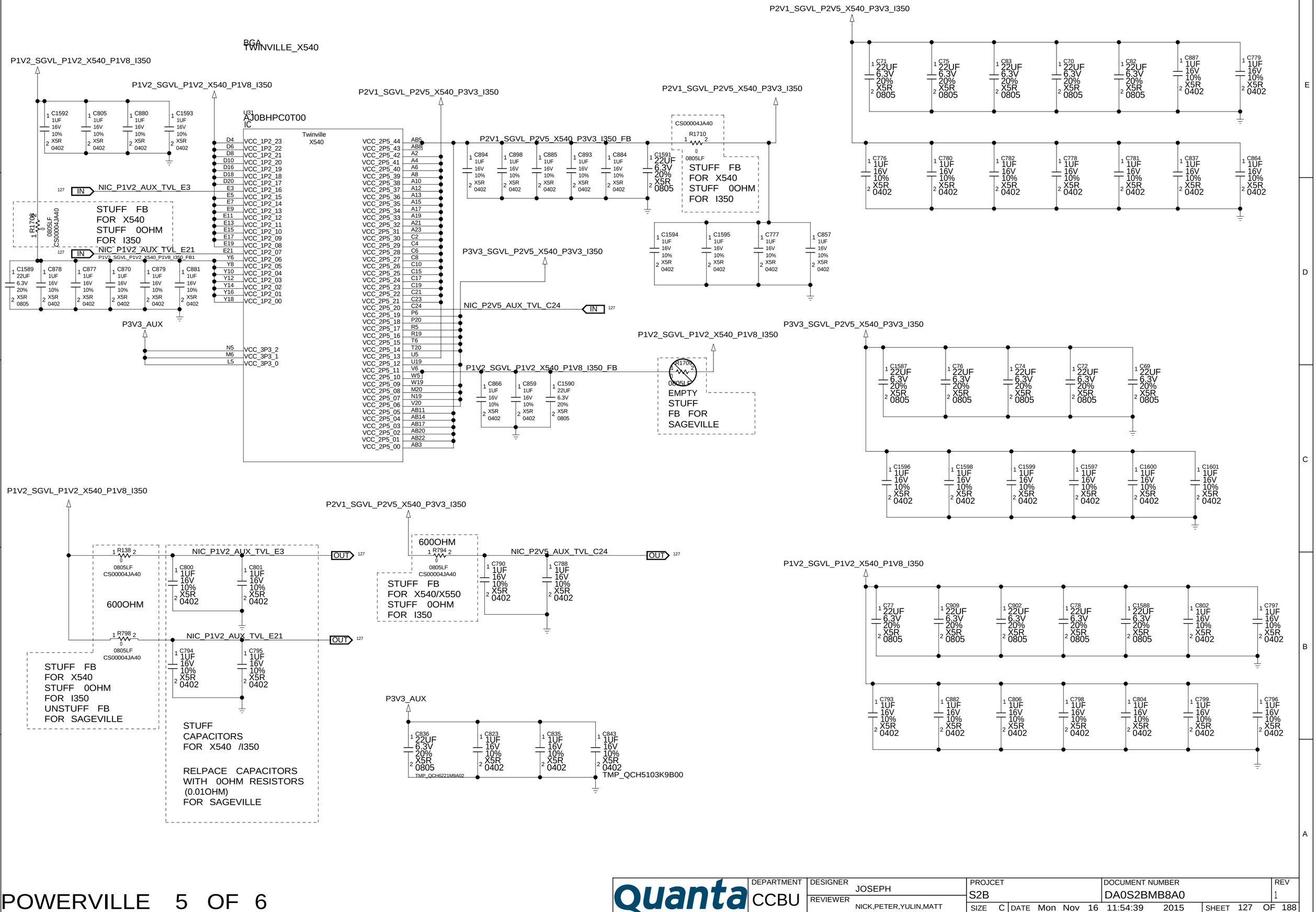
C88 22UF 6.3V 20% X5R 0805
C769 22UF 6.3V 20% X5R 0805
C767 22UF 6.3V 20% X5R 0805
C768 22UF 6.3V 20% X5R 0805
C772 22UF 6.3V 20% X5R 0805
C94 22UF 6.3V 20% X5R 0805
C84 22UF 6.3V 20% X5R 0805
C63 22UF 6.3V 20% X5R 0805
C68 22UF 6.3V 20% X5R 0805
TMP_QCH6221M9A02

C840 1UF 16V 10% X5R 0402
C858 1UF 16V 10% X5R 0402
C818 1UF 16V 10% X5R 0402
C833 1UF 16V 10% X5R 0402
C869 1UF 16V 10% X5R 0402
C863 1UF 16V 10% X5R 0402
C844 1UF 16V 10% X5R 0402
C854 1UF 16V 10% X5R 0402
C816 1UF 16V 10% X5R 0402

C842 1UF 16V 10% X5R 0402
C848 1UF 16V 10% X5R 0402
C814 1UF 16V 10% X5R 0402
C841 1UF 16V 10% X5R 0402
C819 1UF 16V 10% X5R 0402
C809 1UF 16V 10% X5R 0402
C861 1UF 16V 10% X5R 0402
C812 1UF 16V 10% X5R 0402
C834 1UF 16V 10% X5R 0402

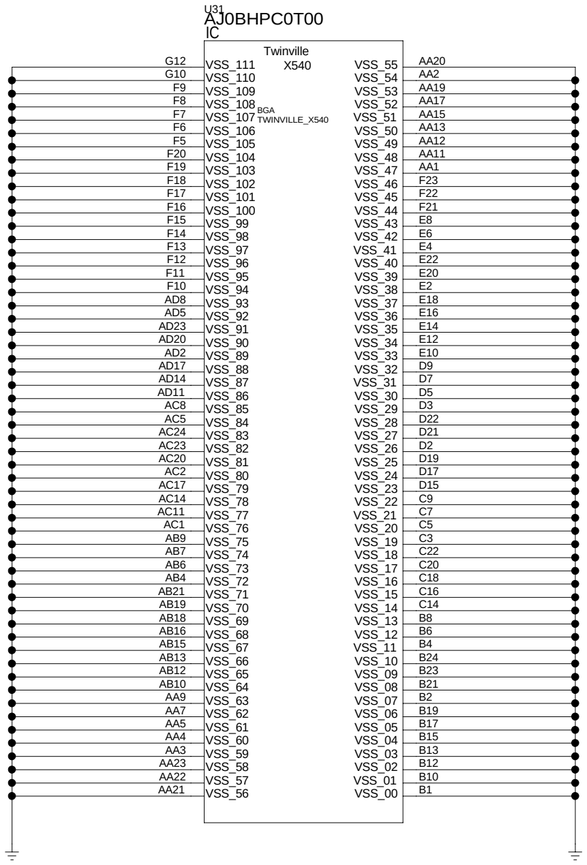
POWERVILLE 4 OF 6

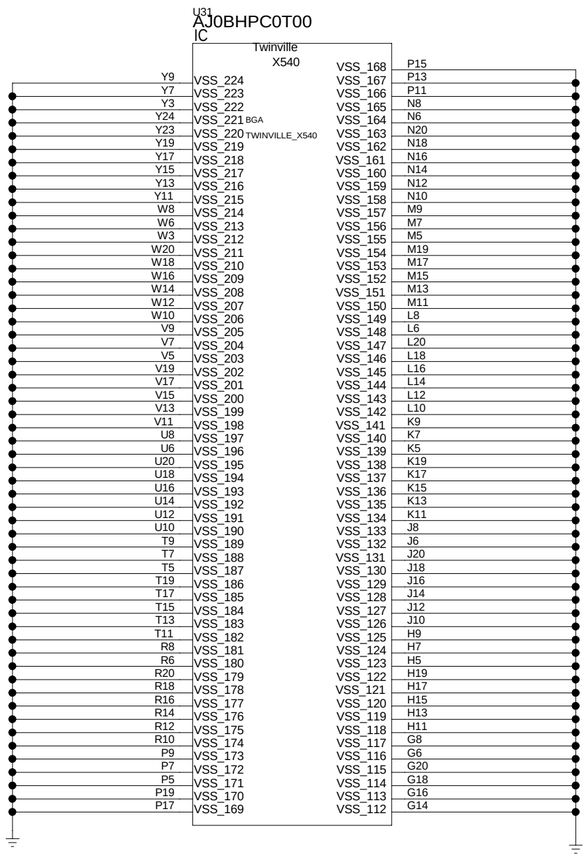
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: JOSEPH | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: NICK,PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:54:38 2015 | SHEET: 126 OF 188 |




POWERVILLE 5 OF 6

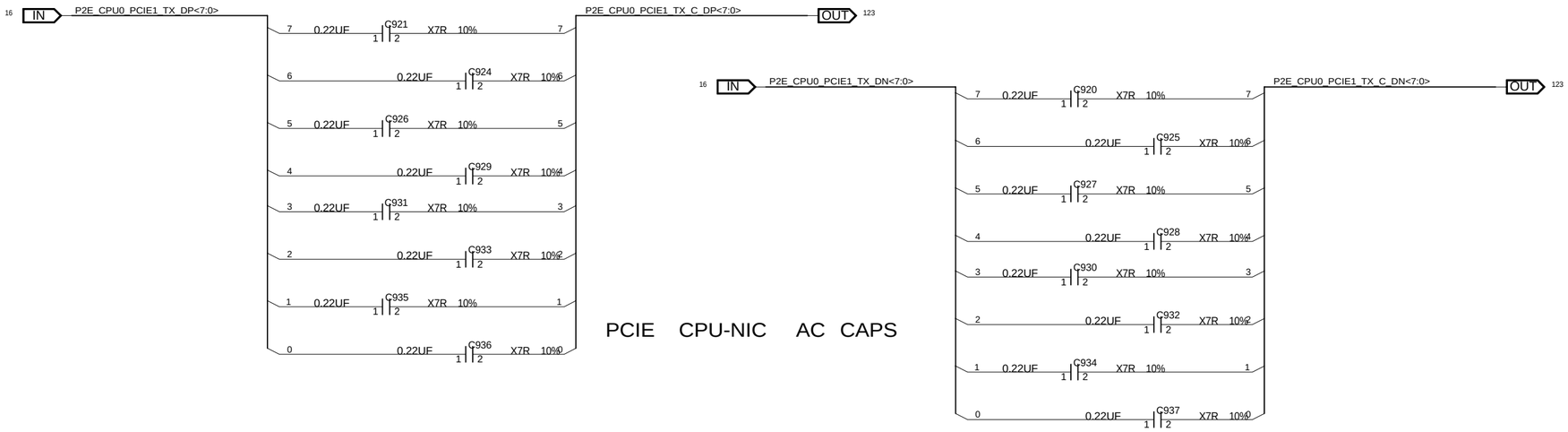
| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER JOSEPH | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER NICK,PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:54:39 2015 | SHEET 127 OF 188 | |



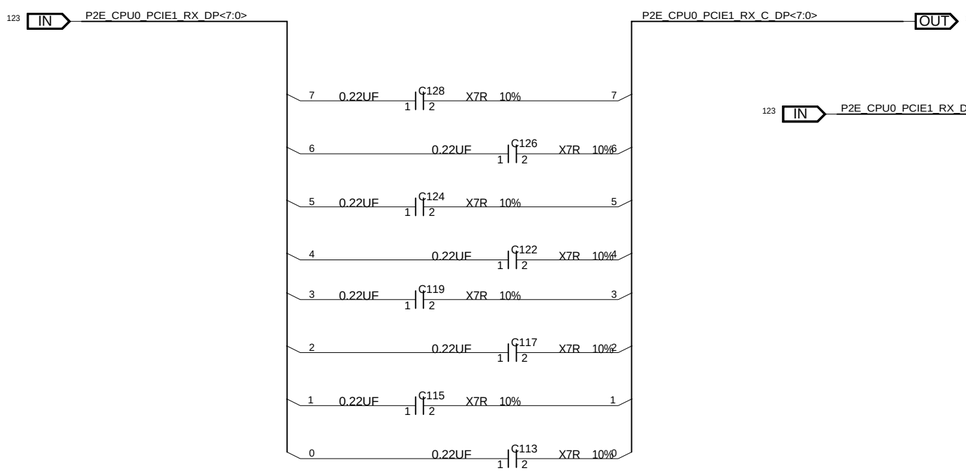

POWERVILLE 6 OF 6

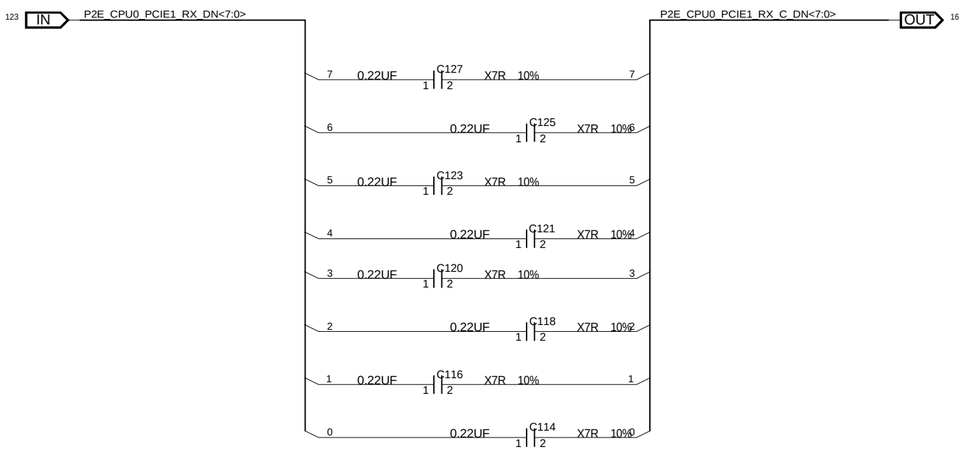
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER JOSEPH | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER NICK,PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:54:42 2015 | SHEET 128 OF 188 |




PCIE CPU-NIC AC CAPS



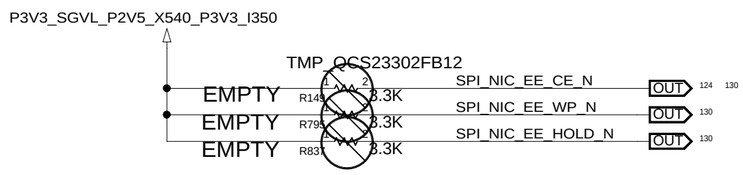



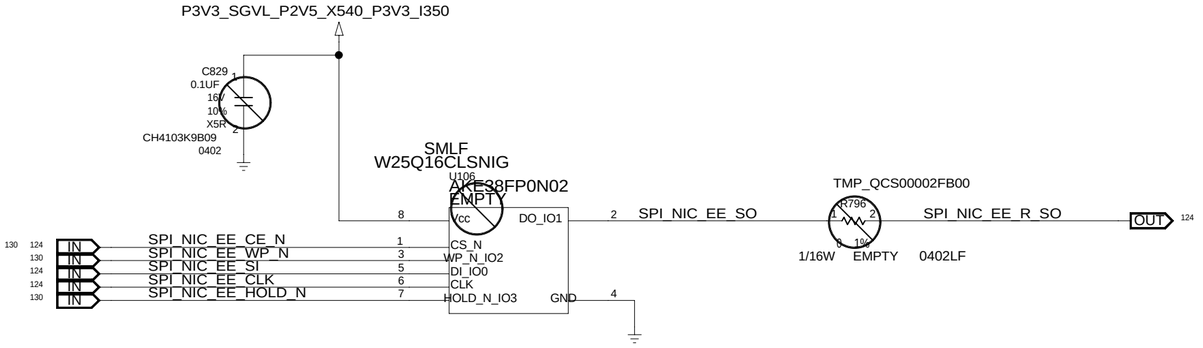

PLACE AC CAP CLOSE TO LAN CHIP

# POWERVILLE AC COUPLING CAPS

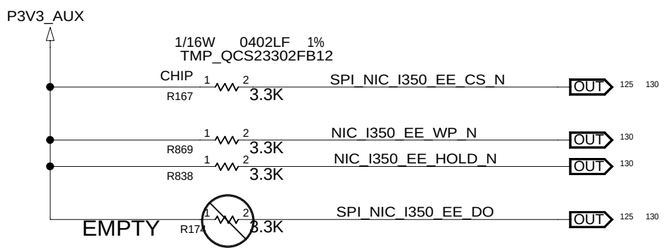
| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:54:43 2015 | SHEET 129 OF 188 | |

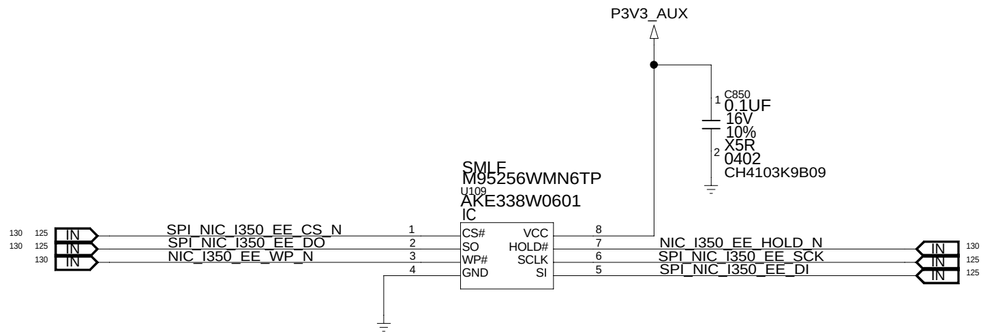
# TWINVILLE FLASH



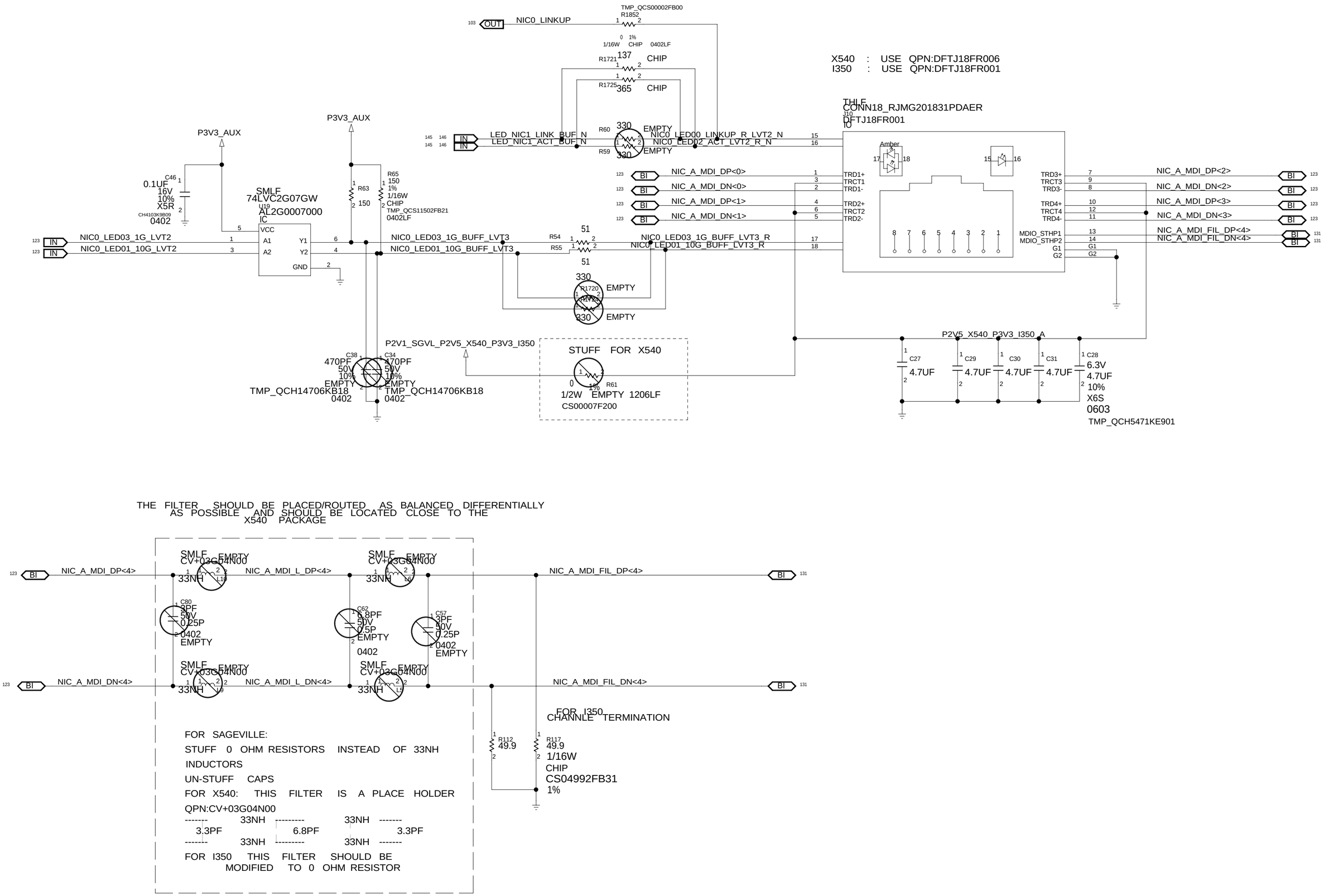

# I350 EEPROM




# POWERVILLE FLASH ROM

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER JOSEPH | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER NICK,PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:54:45 2015 | SHEET 130 OF 188 | |

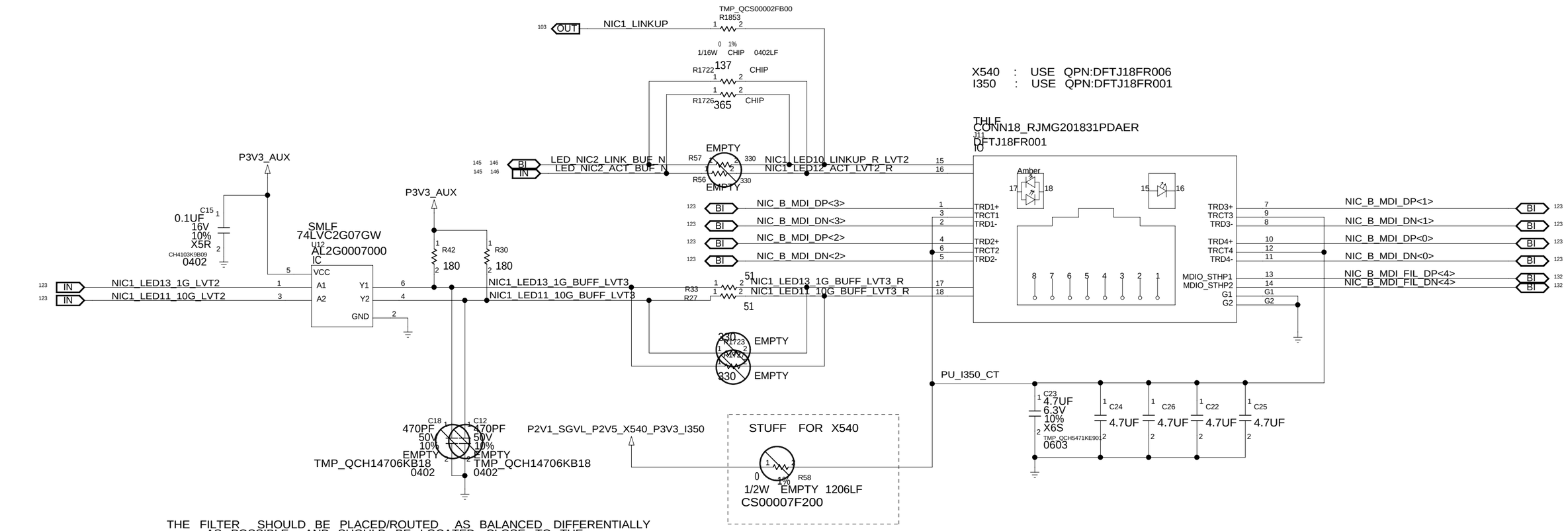






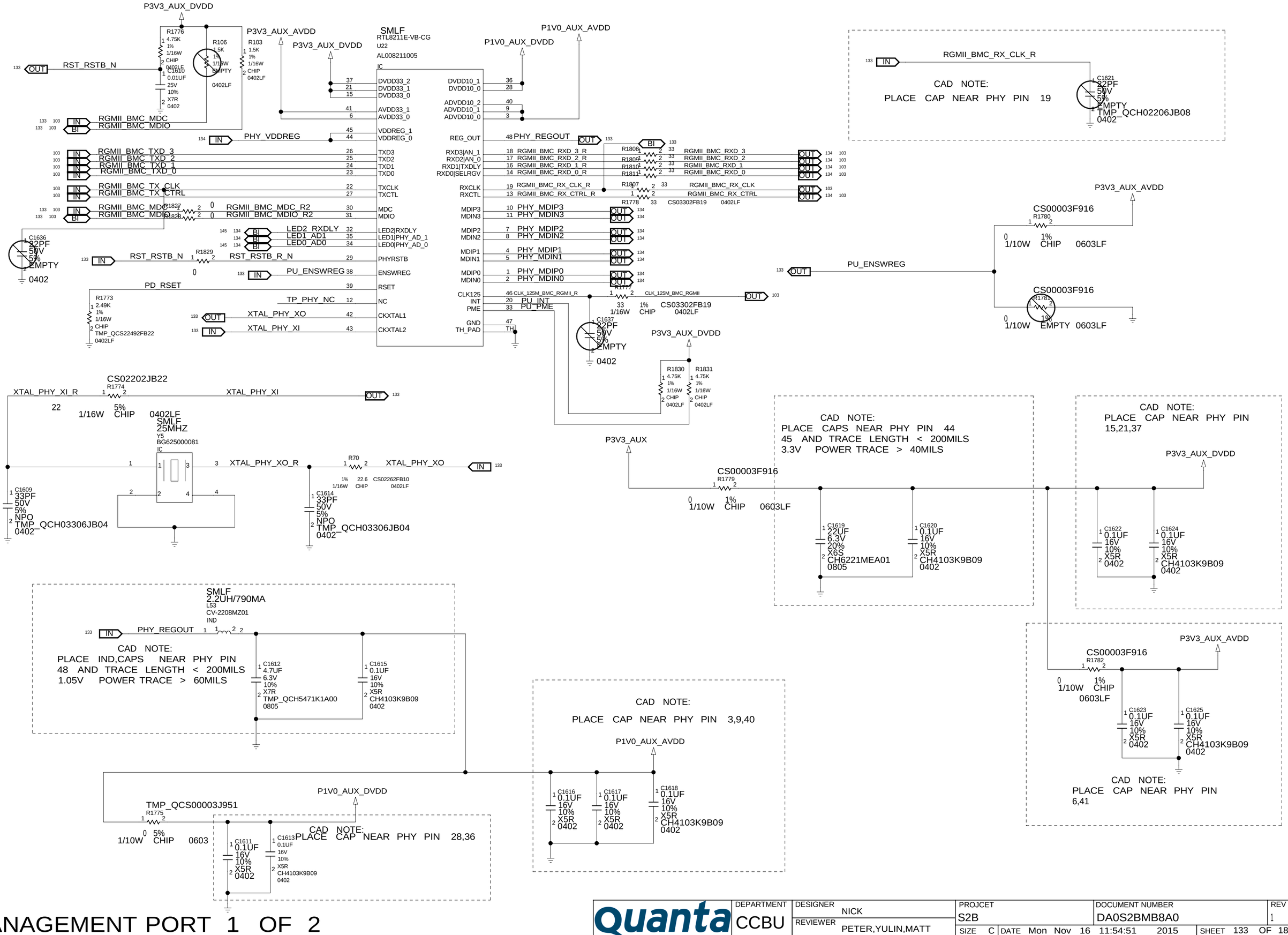
POWERVILLE PORT 0

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER JOSEPH | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER NICK,PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:54:46 2015 | SHEET 131 OF 188 | |



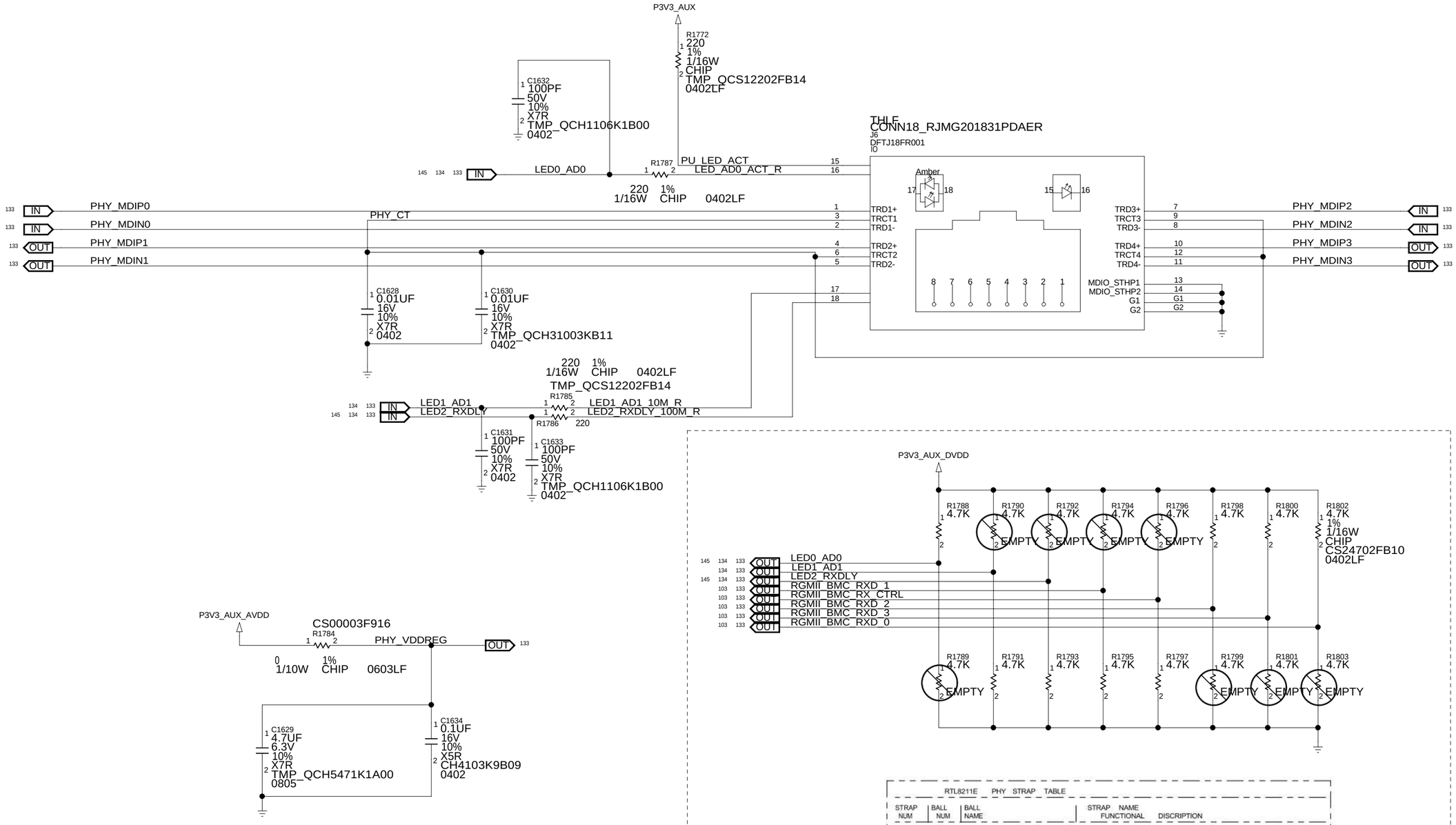

POWERVILLE PORT 1

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER JOSEPH | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | | |
| | | REVIEWER NICK,PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:54:47 2015 | SHEET 132 OF 188 | | |




# MANAGEMENT PORT 1 OF 2

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:54:51 2015 | SHEET: 133 OF 188 | |




RTL8211E PHY STRAP TABLE

| STRAP NUM | BALL NUM | BALL NAME | STRAP NAME FUNCTIONAL DISCRIPTION |
|---|---|---|---|
| | 35 | LED0/PHY_AD_0 (DEFUALT = 1) | AD0,AD1,AD2 ARE PHY ADDRESS<br>RTL8211D : 01 (AD1-AD0)<br>RTL8211E : 001 (AD2-AD0) |
| | 34 | LED1/PHY_AD_1 (DEFUALT = 0) | |
| | 13 | RXCTL_AD2 (DEFUALT = 0) | PHY_AD2 ONLY FOR RTL8211E |
| | 32 | LED2/RXDLY (DEFUALT = 0) | WITHOUT RX DELAY |
| | 16 | RXD1/TXDLY (DEFUALT = 0) | WITHOUT TX DELAY |
| | 17 | RXD2/AN_0 (DEFUALT = 1) | AN_0/AN_1 ARE HI FOR ALL CAPABILITY |
| | 18 | RXD3/AN_1 (DEFUALT = 1) | |
| | 14 | RXD0/SELRGV (DEFUALT = 1) | HI FOR 3V3 RGMII (RTL8211D/8211E)<br>HI FOR 1V5/1V8 RGMII (RTL8211E-VL ONLY)<br>LO FOR 2V5 RGMII (RTL8211D/8211E) |

# MANAGEMENT PORT 2 OF 2

| | | | |
|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B |
| | | REVIEWER: PETER,YULIN,MATT | DOCUMENT NUMBER: DA0S2BMB8A0 |
| | | SIZE: C | DATE: Mon Nov 16 11:54:54 2015 |
| | | | SHEET: 134 OF 188 |
| | | | REV: 1 |

CPLD NOTE

CURRENTLY, CPLD DON'T SUPPORT ADR FUNCTION

CAD NOTE:

ROUTE ALL THE SIGNALS WITH NETNAMES THAT STARTS WITH RST_.. OR IRQ_
500MIL AWAY FROM THE CRB EDGE OF THE BOARD

SMLF_SMDC9
LCMXO256C-3MN100C_SMDC9

U63
AJ0256C0U00
IC

P3V3_AUX

TMP_QCS24022FB13 R1083 4.02K 1% 1/16W EMPTY 0402LF

C1109 100PF 50V 5% EMPTY CH11006JB00 0402

TMP_QCS00002FB00

PWRGD_CPUPWRGD
PWRGD_PCH_PWROK → R1087 0 1% CHIP 1/16W 0402LF → PWRGD_PCH_PWROK_R2
PWRGD_CPU1_BDX_PRSNT_LVT3_N
PWRGD_P1V05_PCH → R1081 0 1% CHIP 1/16W 0402LF
RST_CPU1_LVC3_N → R1088 2K 1% 1/16W 0402LF → RST_CPU1_LVC3_R_N
PWRGD_CPU1_LVC3 → R1086 75 1% CHIP 1/16W 0402LF → PWRGD_CPU1_LVC3_R
PWRGD_PS
RST_CPU0_LVC3_N → R1090 75 1% CHIP 1/16W 0402LF → RST_CPU0_LVC3_R_N
PWRGD_SYS_PWROK → R1822 0 → PWRGD_SYS_PWROK_R1
FM_PLD_RESET_N
FM_CPU1_SKTOCC_LVT3_N
FM_PLD_TSALL
PVCCIN_CPU1_EN_R
FM_CPU0_BDX_PRSNT_LVT3_N
FM_CPU_ERR1_CO_N
FM_THERMTRIP_CO_N
FM_PLD_BUG_MODE_N
PWRGD_P1V5_PCH
FM_CPU0_SKTOCC_LVT3_N
PWRGD_P1V05_PCH_STBY_DLY
PWRGD_P1V05_STBY_PCH

C1112 0.1UF 16V 10% X5R 0402
R385 4.02K 1% 1/16W EMPTY 0402LF

2K 1% R384 1/16W 0402LF

XDP_RST_CO_N
XDP_PWRGD_RST_N
FP_PWR_BTN_N
FM_XDP_HOOK1_SEL
RST_PLTRST_N → R1746 0 → RST_PLTRST_N_R2
PWRGD_P5V
FM_PERST_SRC_LVT3
FM_VPP_MEM_ABCD_EN_R
PWRGD_PVPP_PVDDQ_AB
PWRGD_PVPP_PVDDQ_CD
RST_RSMRST_N
FM_LVC3_THERMTRIP_DLY
FM_ADR_TRIGGER
PU_PLD_SLEEP_N
JTAG_PLD_TCK
JTAG_PLD_TMS
JTAG_PLD_TDI

R1131 2K 1% 1/16W EMPTY 0402LF

R1114 4.7K 1% 1/16W 0402LF

CANT BE CONECTED

| | | | |
|---|---|---|---|
| P1 | VCCIO1_P1 | B1 | PL2A |
| G1 | VCCIO1_G1 | C1 | PL2B |
| P10 | VCCIO1_P10 | D2 | PL3A |
| H14 | VCCIO0_H14 | D1 | PL3B |
| A14 | VCCIO0_A14 | C2 | PL3C |
| B5 | VCCIO0_B5 | E1 | PL3D |
| | | E2 | PL4A |
| | | F1 | PL4B |
| | | F2 | PL5A |
| | | G2 | PL5B |
| | | H2 | PL5C |
| | | J1 | PL5D_GSRN |
| | | J2 | PL6A |
| | | K1 | PL6B_TSALL |
| | | K2 | PL7A |
| | | L1 | PL7B |
| | | L2 | PL7C |
| | | M1 | PL7D |
| | | M2 | PL8A |
| | | N1 | PL8B |
| | | M3 | PL9A |
| | | P3 | PL9B |
| | | P4 | PB2A |
| | | N3 | PB2B |
| | | N5 | PB2C |
| | | N6 | PB2D |
| | | N7 | PB3A_PCLK1_1 |
| | | P8 | PB3B |
| | | N8 | PB3C_PCLK1_0 |
| | | P9 | PB3D |
| | | P11 | PB4A |
| | | N11 | PB4B |
| | | P12 | PB4C |
| | | N12 | PB4D |
| | | P13 | PB5A |
| | | P14 | PB5C |
| | | N13 | PB5D |
| | | M12 | SLEEPN |
| | | N4 | TCK |
| | | P2 | TMS |
| | | P6 | TDI |
| | | B9 | GND_B9 |
| | | N9 | GND_N9 |

P3V3_AUX

| | | | |
|---|---|---|---|
| VCCAUX | B7 | | |
| VCC_B6 | B6 | | |
| VCC_P7 | P7 | | |
| PR9A | M14 | RST_PCIE_CPU_N | |
| PR9B | N14 | IRQ_FAN_12V_GATE | |
| PR8A | L14 | PU_240VA_OC | |
| PR8B | L13 | FM_PLD_DEBUG1 | |
| PR7A | J14 | FM_VPP_MEM_EFGH_EN_R | |
| PR7B | K13 | RST_PCIE_PCH_R_N → R11410 1 2 → RST_PCIE_PCH_N | |
| PR7C | K14 | RST_PERST0_R_N → R1137 49.9 → RST_PERST0_N | |
| PR7D | M13 | TP_RST_PCIE_PCH_DEV_N | |
| PR6A | H13 | PWRGD_PVPP_PVDDQ_GH | |
| PR6B | J13 | SGPIO_PLD_DOUT | |
| PR5A | E14 | PWRGD_PVPP_PVDDQ_EF | |
| PR5B | F13 | RST_PLTRST_BUF_N | |
| PR5C | F14 | RST_PERST1_R_N → R1135 100 → RST_PERST1_N | |
| PR5D | G13 | TP_FM_PLD_DEBUG4 | |
| PR4A | D14 | XDP_CPU_SYSPWROK | |
| PR4B | E13 | IRQ_SML1_PMBUS_ALERT_BUF_N | |
| PR3A | B14 | FM_ADR_COMPLETE_DELAY | |
| PR3B | C13 | | |
| PR3C | C14 | RST_DLY_CPURST_LVC3 | |
| PR3D | D13 | SGPIO_PLD_LD_N → R410 0 → SGPIO_IBMC_LD_N | |
| PR2A | A13 | PWRGD_PVCCIN_CPU0 | |
| PR2B | C12 | PWRGD_P0V67_P1V0_AUX | |
| PT5A | A11 | SGPIO_PLD_CLK → R435 0 → SGPIO_IBMC_CLK | |
| PT5B | B11 | FM_AUX_SW_EN | |
| PT5C | A12 | RST_PLTRST_DLY | |
| PCLK0_0_PT4A | B8 | FM_PCH_PRSNT_CO_N | |
| PCLK0_1_PT4B | A8 | FM_VCC_MAIN_EN | |
| PT4C | A9 | TP_FM_PLD_DEBUG2 | |
| PT4D | B10 | FM_ERR1_DLY_N | |
| PT4E | A10 | PWRGD_PVCCIN_CPU1 | |
| PT4F | B12 | PWRGD_P3V3 | |
| PT3A | B4 | FM_SLP_S3_N | |
| PT3B | A5 | TP_FM_PLD_DEBUG3 | |
| PT3C | A6 | FM_BMC_ONCTL_N | |
| PT3D | A7 | CLK_33K_SUSCLK_PLD_R | |
| PT2A | B2 | FM_ADR_COMPLETE_R | |
| PT2B | A1 | FM_SLP_S4_N | |
| PT2C | C3 | PWRGD_CPU0_LVC3_R → R413 0 → PWRGD_CPU0_LVC3 | |
| PT2D | A2 | FM_PS_EN | |
| PT2E | B3 | FM_PLD_CLK_EN | |
| PT2F | A3 | TP_FM_PLD_DEBUG5 | |
| TDO | P5 | JTAG_PLD_TDO | |
| GNDIO1_N10 | N10 | | |
| GNDIO1_N2 | N2 | | |
| GNDIO1_H1 | H1 | | |
| GNDIO0_A4 | A4 | | |
| GNDIO0_B13 | B13 | | |
| GNDIO0_G14 | G14 | | |

R1140 2K 1% 1/16W EMPTY 0402LF

C1151 1000PF 16V 10% X7R 0402

C1139 1000PF 16V 10% X7R 0402

SGPIO_PLD_DOUT → R454 0 1% 1/16W CHIP 0402LF TMP_QCS00002FB00 → SGPIO_IBMC_DIN

I240 CS03302FB19

CLK_33K_SUSCLK → R1195 33 1% 1/16W CHIP 0402LF → CLK_33K_SUSCLK_PLD_R

CAD NOTE: PLACE TERMINATION RESISTOR WITHIN 1" FROM PLD

DESIGN NOTE:

* IO PINS C13 & N3 WERE GROUNDED TO IMPROVE CPLD BREAKOUT.
* IO PINS N13 &B2 ARE UNCONNECTED TO IMPROVE CPLD BREAKOUT.

P3V3_AUX

C1129 0.1UF 16V 10% X5R 0402
C1119 0.1UF 16V 10% X5R 0402
C1127 0.1UF 16V 10% X5R 0402
C1122 0.1UF 16V 10% X5R 0402
C1126 10UF 16V 10% X5R 0805 CH6103K9A00
C1136 0.1UF 16V 10% X5R 0402
C1130 0.1UF 16V 10% X5R 0402
C1135 0.1UF 16V 10% X5R 0402
C1121 0.01UF 25V 10% X7R 0402
C1140 0.1UF 16V 10% X5R 0402
C1141 0.01UF 25V 10% X7R 0402 TMP_QCH31004KB17

CH4103K9B09

P3V3

R1678 4.7K 1% 1/16W EMPTY CS24702FB10 0402LF

FM_ADR_TRIGGER_PCH_N

SMLF NX7002AK U176 BAM70020062 IC

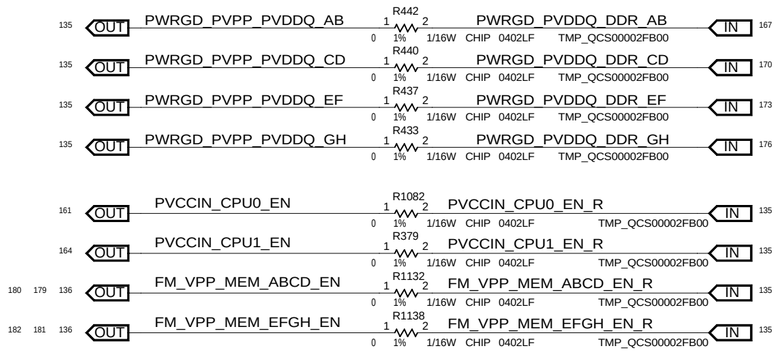
FM_ADR_TRIGGER

R1677 10K 5% 1/16W CHIP TMP_QCS31002JB28 0402LF

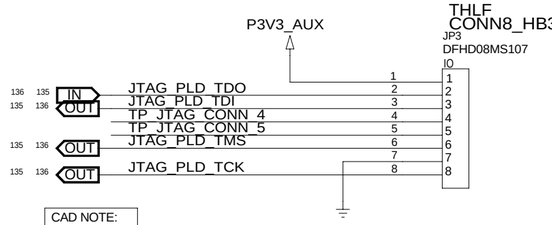


Quanta

| DEPARTMENT | DESIGNER | PROJCET | DOCUMENT NUMBER | REV |
|---|---|---|---|---|
| CCBU | MINGLI | S2B | DA0S2BMB8A0 | 1 |
| | REVIEWER: NICK,PETER,YULIN,MATT | SIZE C DATE Mon Nov 16 11:54:56 2015 | SHEET 135 OF 188 | |

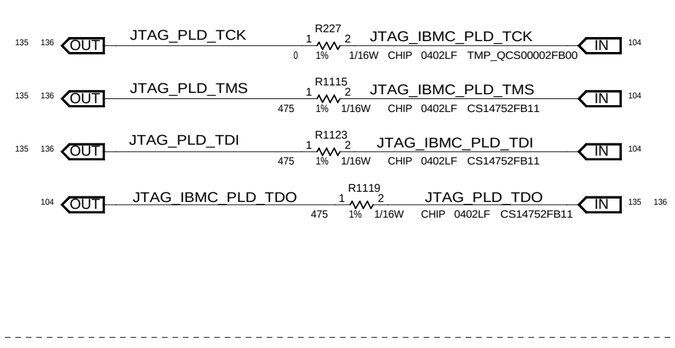


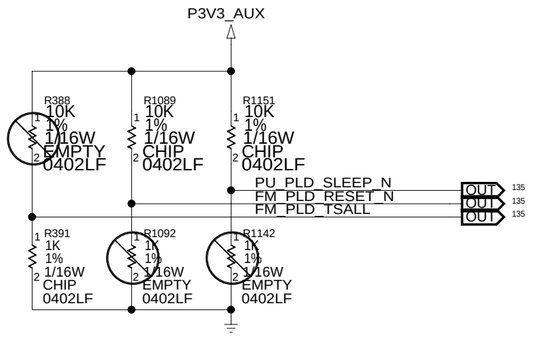

# LATTICE IN SYSTEM PROGRAMMING HEADER.

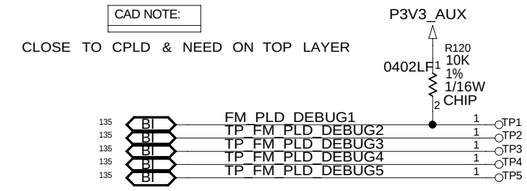


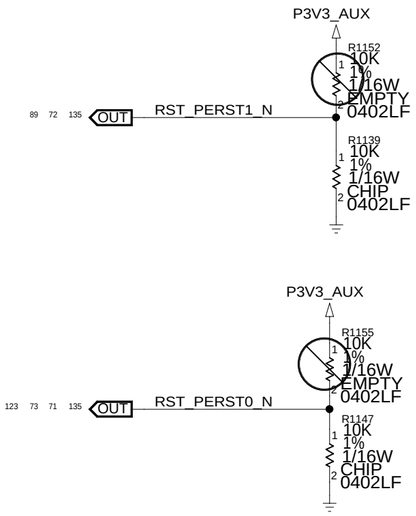

CAD NOTE:

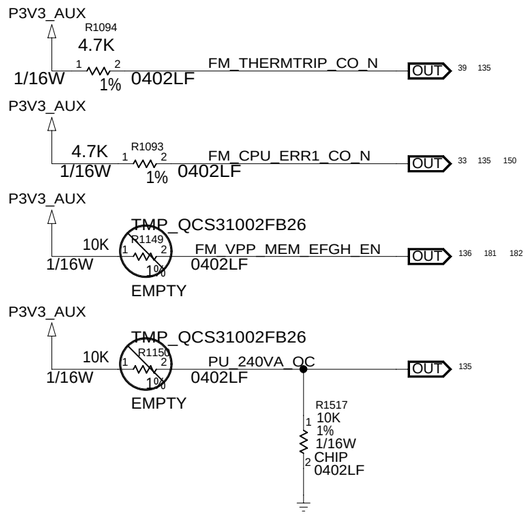
PLACE DECOUPLING CAPACITORS NEAR POWER PIN ON PLD PROGRAMMING HEADER

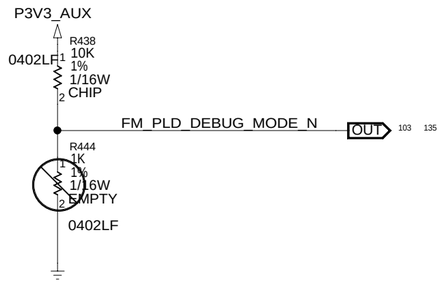


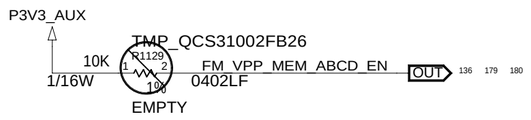



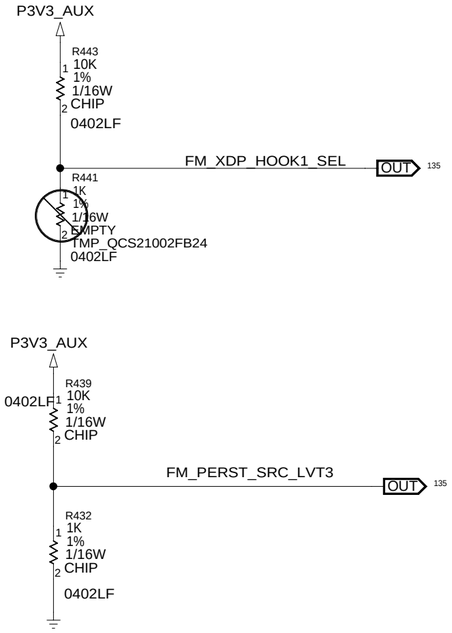




CPLD 2 OF 2

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER MINGLI | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER NICK,PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:54:57 2015 | SHEET 136 OF 188 |

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|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER MINGLI | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER NICK,PETER,YULIN,MATT | SIZE C | DATE Thu Feb 07 10:16:29 2013 | SHEET 137 OF 188 | |

BLANK

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Jul 01 19:20:40 2013 | SHEET 138 OF 188 | |





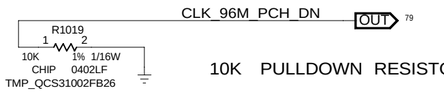




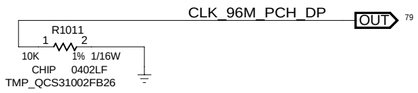


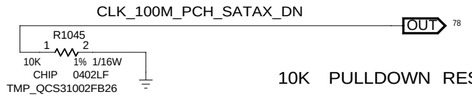


CAD NOTE:PLACE RS/RP RESISTOR CLOSE TO CLK SOURCE WITHIN 0.5 INCHES

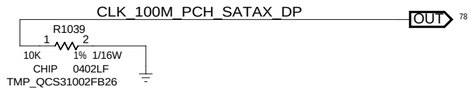


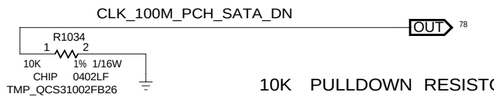

10K PULLDOWN RESISTORS FOR ISCLK



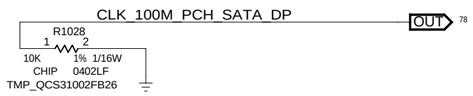



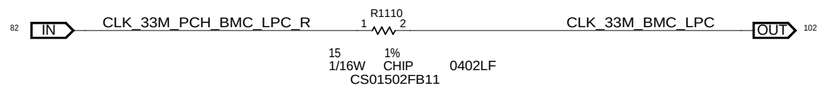

10K PULLDOWN RESISTORS FOR ISCLK




10K PULLDOWN RESISTORS FOR ISCLK



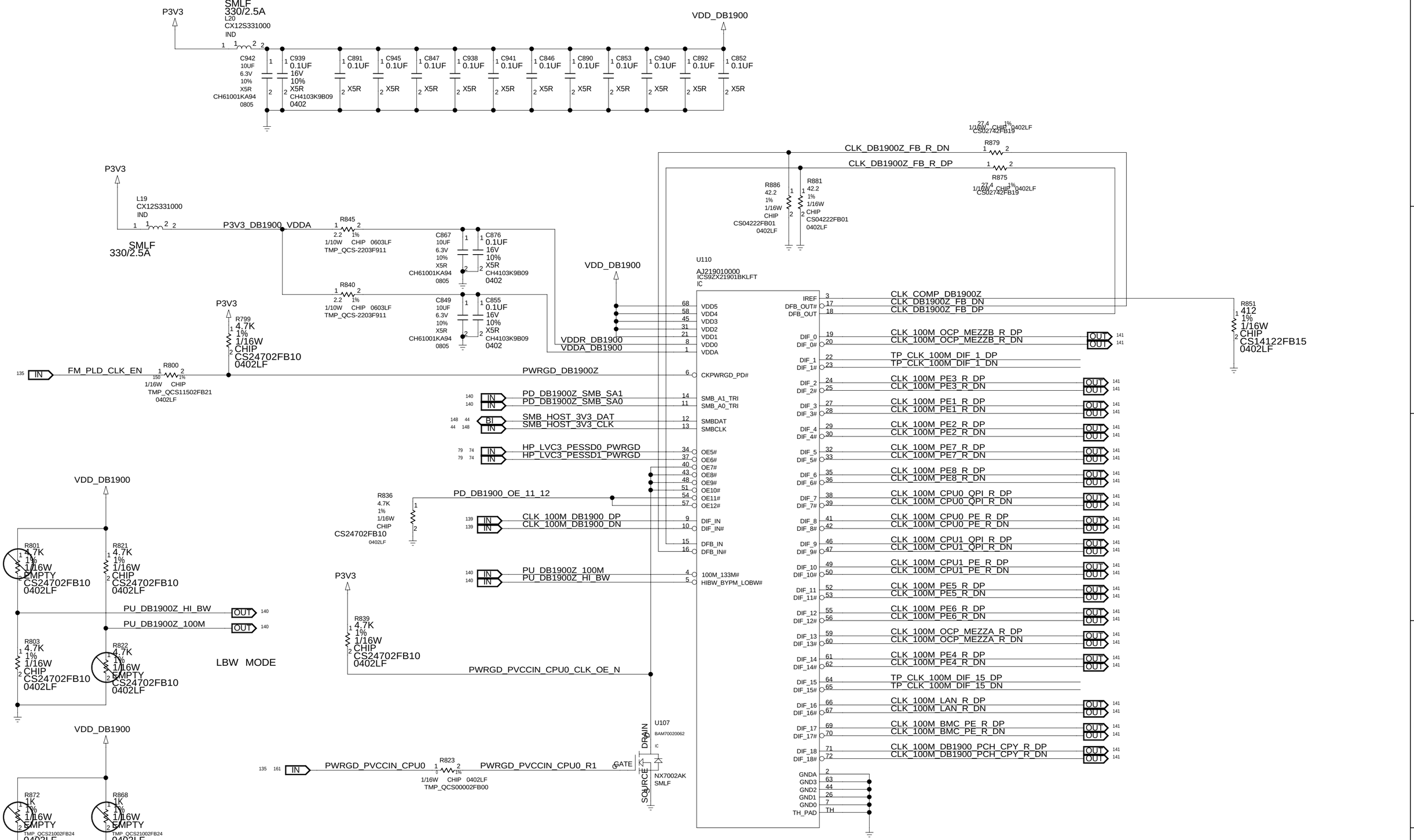







# CK420BQ TERMINATION

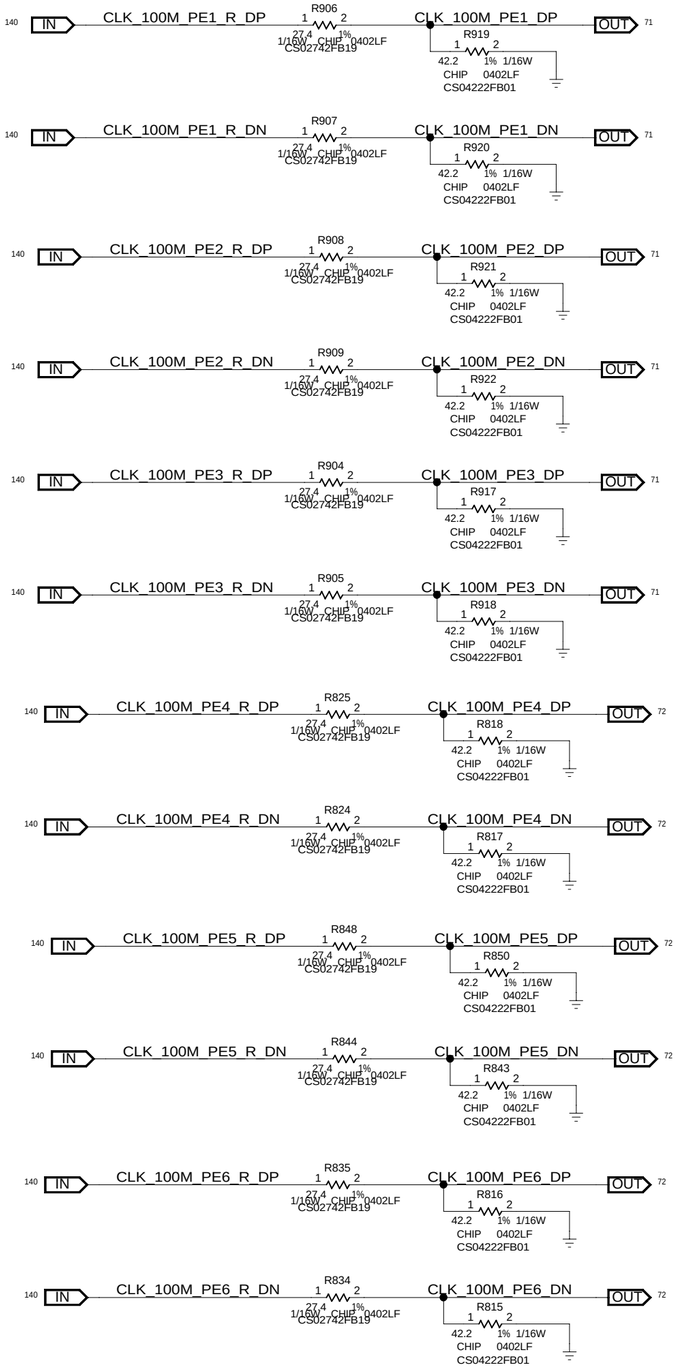
| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:54:59 2015 | SHEET: 139 OF 188 | |



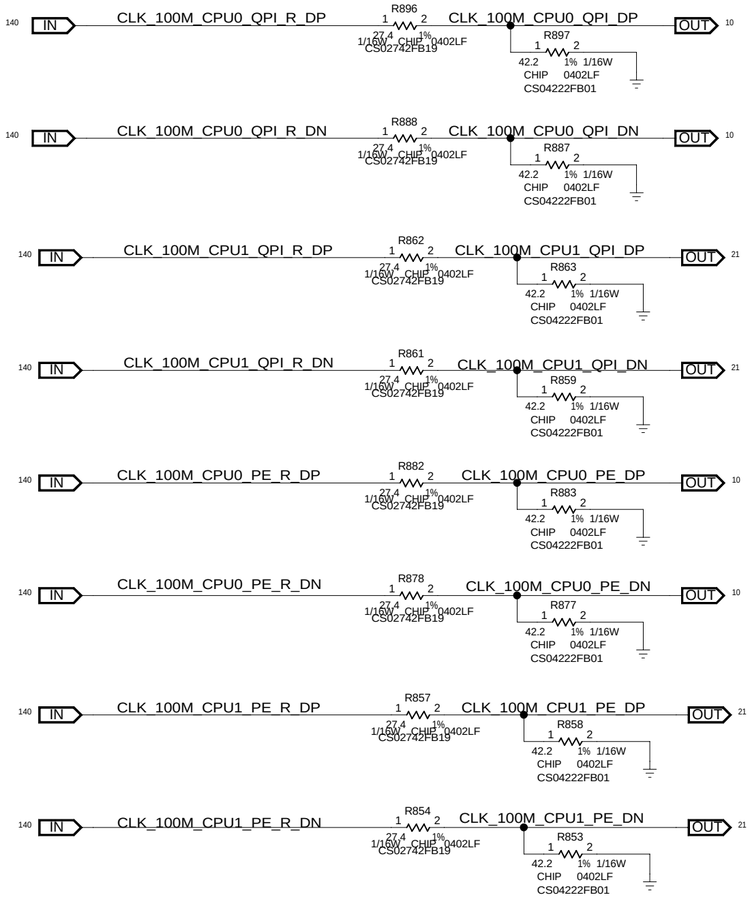

# DB1900Z CLOCK BUFFER

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:55:00 2015 | SHEET: 140 OF 188 |

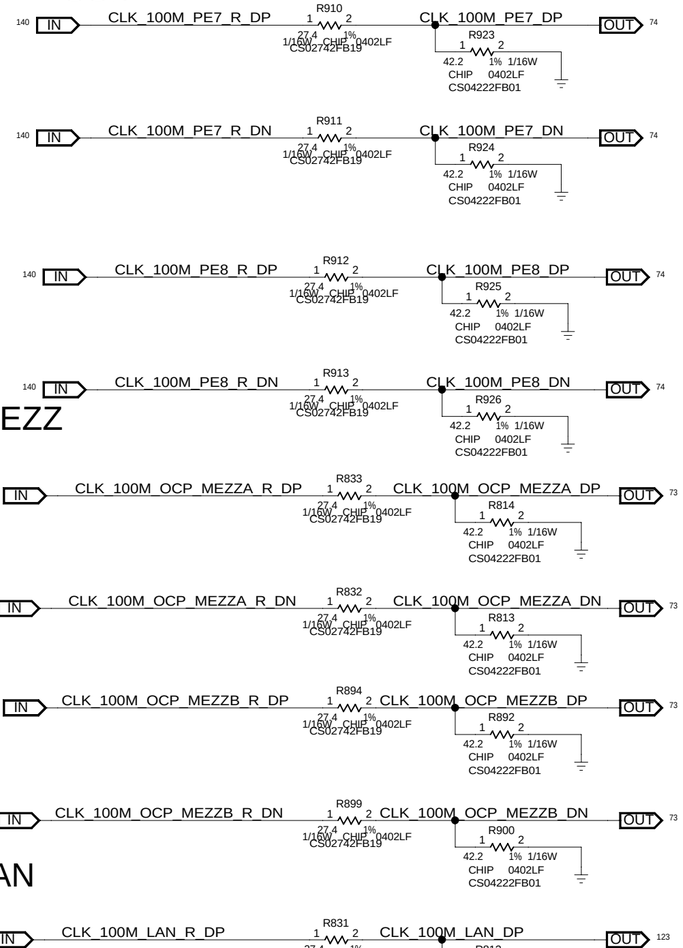
## RISER




## CPU



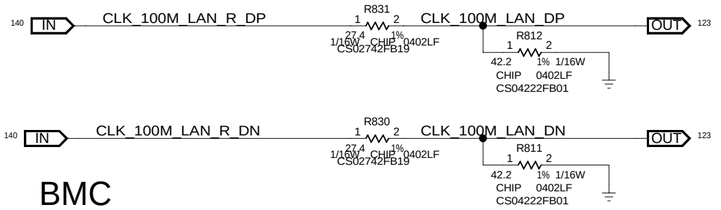

## PCIE SSD



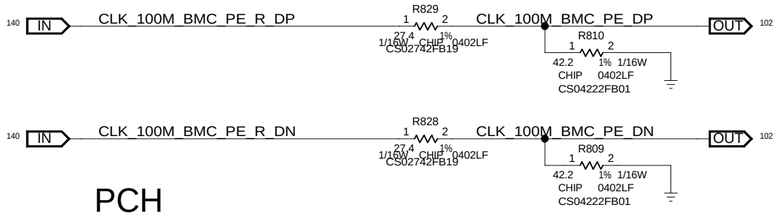

## MEZZ



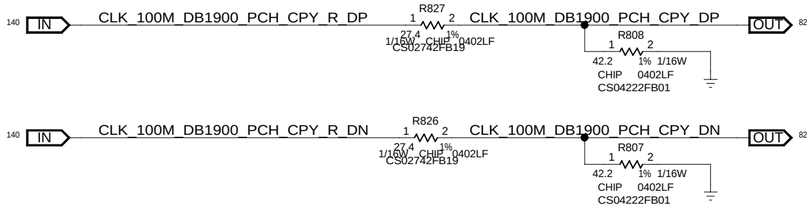

## LAN




## BMC



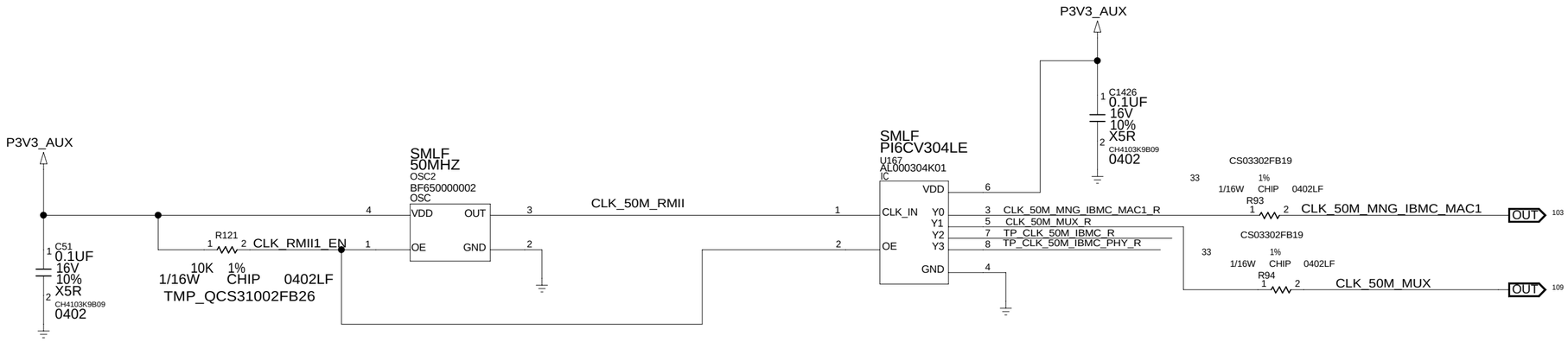

## PCH




CAD NOTE:PLACE RS/RP RESISTOR CLOSE TO CLK SOURCE WITHIN 0.5 INCHES

# DB1900Z CLOCK TERMINATION

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:55:02 2015 | SHEET: 141 OF 188 |




RMII 50MHZ CLOCK

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:55:04 2015 | SHEET 142 OF 188 | |

# PSU1 ADDRESS: B2

# PSU0 ADDRESS: B0

# PSU AC LOSS OR CIRCUIT

# POWER SUPPLY CONNECTOR

SMTLF
SCONN64_C2101610104Y
JP17
DFHS64FR007
CONN

| | | | |
|---|---|---|---|
| 64 | +12V24 | +12V1 | 1 |
| 63 | +12V23 | +12V2 | 2 |
| 62 | +12V22 | +12V3 | 3 |
| 61 | +12V21 | +12V4 | 4 |
| 60 | +12V20 | +12V5 | 5 |
| 59 | +12V19 | +12V6 | 6 |
| 58 | +12V18 | +12V7 | 7 |
| 57 | +12V17 | +12V8 | 8 |
| 56 | +12V16 | +12V9 | 9 |
| 55 | +12V15 | +12V10 | 10 |
| 54 | +12V14 | +12V11 | 11 |
| 53 | +12V13 | +12V12 | 12 |
| 52 | SGND23 | SGND0 | 13 |
| 51 | SGND22 | SGND1 | 14 |
| 50 | SGND21 | SGND2 | 15 |
| 49 | SGND20 | SGND3 | 16 |
| 48 | SGND19 | SGND4 | 17 |
| 47 | SGND18 | SGND5 | 18 |
| 46 | SGND17 | SGND6 | 19 |
| 45 | SGND16 | SGND7 | 20 |
| 44 | SGND15 | SGND8 | 21 |
| 43 | SGND14 | SGND9 | 22 |
| 42 | SGND13 | SGND10 | 23 |
| 41 | SGND12 | SGND11 | 24 |
| 40 | SENSE_P | TACH | 25 |
| 39 | P12V_SB | SENSE* | 26 |
| 38 | PS_A0 | VINGOOD | 27 |
| 37 | PSOK | CSHARE | 28 |
| 36 | RETURN | PSON# | 29 |
| 35 | SCL | PS_KILL | 30 |
| 34 | PRESENT# | RESET | 31 |
| 33 | SDA | ALERT | 32 |

PD_PSU_REMOTE_SENSE_N OUT 143
SM EMPTY SHORT6 R603 SHORT

P12V
P5V_AUX
R621 8.25K 1% 1/16W CHIP CS28252FB15 0402LF
SM EMPTY SHORT6 R616 SHORT
P12V_STBY

PU_PSU1_REMOTE_SENSE_P
PU_PSU1_A0
PWRGD_PSU1 OUT 144
SMB_3V3SB_PMBUS_CLK_R1 IN 143 107 143
PSU1_PRESENT_N OUT
SMB_3V3SB_PMBUS_DAT_R1 BI

PSU1_ISHARE
PD_PSU_REMOTE_SENSE_N
FM_PSU1_VIN_FAIL_N
FM_CSHARE
FM_PS_EN_PSU_N
PD_PSU_KILL_1
PD_RST_PS_1
IRQ_SML1_PMBUS_ALERT_R2_N

R1843 0 PSU_ISHARE BI 143 143
TMP_QCS11002FB22 1/16W CHIP 0402LF
R610 100 1% R608 100 1% 1/16W CHIP TMP_QCS11002FB22 0402LF OUT 143

CS03302FB19
SMB_3V3SB_PMBUS_CLK IN 143 147 106 102 81
R620 33 1% 1/16W CHIP 0402LF
SMB_3V3SB_PMBUS_CLK_R1 OUT 143

CS03302FB19
SMB_3V3SB_PMBUS_DAT BI 147 143 106 102 81
R618 33 1% 1/16W CHIP 0402LF
SMB_3V3SB_PMBUS_DAT_R1 BI 143

P12V
C212 4.7UF 25V 20% EMPTY CH5474M1200 C1206
C329 4.7UF 25V 20% EMPTY CH5474M1200 C1206
C1254 10UF 16V 10% X5R CH6103K9A00 0805
C337 10UF 16V 10% X5R CH6103K9A00 0805
C1253 10UF 16V 10% X5R CH6103K9A00 0805

P12V
C240 4.7UF 25V 20% EMPTY CH5474M1200 C1206
C213 4.7UF 25V 20% EMPTY CH5474M1200 C1206
C336 10UF 16V 10% X5R CH6103K9A00 0805
C1255 10UF 16V 10% X5R CH6103K9A00 0805

P12V
P12V_BLEEDER_RES
TMP_QCS18206FA00 R1614 820 1% 1/4W CHIP 0805LF
TMP_QCS18206FA00 R1615 820 1% 1/4W CHIP 0805LF
SMLF NX7002AKS Q37 BAM70020069 IC
IN 143 144 FM_PS_EN_PSU_N 5 G2 D2 S2 3 4

P3V3_AUX
R1849 4.75K EMPTY
R1841 4.75K 1% 1/16W EMPTY CS24752FB12 0402LF
FM_PSU1_VIN_FAIL_N IN 143
FM_PSU0_VIN_FAIL_N IN 143
R1833 33 FM_PSU1_VIN_FAIL_R_N
R1834 33 FM_PSU0_VIN_FAIL_R_N
R1850 100K
R1851 100K 5% 1/16W CHIP CS41002JB20 0402LF

P3V3_AUX
C1640 0.1UF 16V 10% X5R CH4103K9B09 0402
VCC GND
A B Y
4 FM_PSU_VIN_FAIL_R_N
SMLF SN74LVC1G32DBVR U189 AL001G32015 IC

P3V3_AUX
R1842 4.75K
R1835 33 FM_PSU_VIN_FAIL_N OUT 103

1/16W CHIP 0402LF TMP_QCS00002FB00
IRQ_SML1_PMBUS_ALERT_R2_N IN 143
IRQ_SML1_PMBUS_ALERT_R1_N IN 143
R611 IRQ_SML1_PMBUS_ALERT_N OUT 88 81 103 144
R607 0 1%
0 1% 1/16W CHIP 0402LF TMP_QCS00002FB00

C308 47UF 50V 5% EMPTY TMP_QCH04706JB01 0402
C309 47UF 50V 5% EMPTY TMP_QCH04706JB01 0402

P12V
C328 180UF 20% 16V ALUM RDLLF CC71803MZ03
C315 10UF 16V 10% X5R CH6103K9A00 0805
C326 10UF 16V 10% X5R CH6103K9A00 0805
C318 10UF 16V 10% X5R CH6103K9A00 0805
C322 4.7UF 25V 20% EMPTY CH5474M1200 C1206
C321 4.7UF 25V 20% EMPTY CH5474M1200 C1206

P12V
C319 4.7UF 25V 20% EMPTY CH5474M1200 C1206
C320 4.7UF 25V 20% EMPTY CH5474M1200 C1206
C316 10UF 16V 10% X5R CH6103K9A00 0805
C317 10UF 16V 10% X5R CH6103K9A00 0805

SMTLF
SCONN64_C2101610104Y
JP16
DFHS64FR007
CONN

| | | | |
|---|---|---|---|
| 64 | +12V24 | +12V1 | 1 |
| 63 | +12V23 | +12V2 | 2 |
| 62 | +12V22 | +12V3 | 3 |
| 61 | +12V21 | +12V4 | 4 |
| 60 | +12V20 | +12V5 | 5 |
| 59 | +12V19 | +12V6 | 6 |
| 58 | +12V18 | +12V7 | 7 |
| 57 | +12V17 | +12V8 | 8 |
| 56 | +12V16 | +12V9 | 9 |
| 55 | +12V15 | +12V10 | 10 |
| 54 | +12V14 | +12V11 | 11 |
| 53 | +12V13 | +12V12 | 12 |
| 52 | SGND23 | SGND0 | 13 |
| 51 | SGND22 | SGND1 | 14 |
| 50 | SGND21 | SGND2 | 15 |
| 49 | SGND20 | SGND3 | 16 |
| 48 | SGND19 | SGND4 | 17 |
| 47 | SGND18 | SGND5 | 18 |
| 46 | SGND17 | SGND6 | 19 |
| 45 | SGND16 | SGND7 | 20 |
| 44 | SGND15 | SGND8 | 21 |
| 43 | SGND14 | SGND9 | 22 |
| 42 | SGND13 | SGND10 | 23 |
| 41 | SGND12 | SGND11 | 24 |
| 40 | SENSE_P | TACH | 25 |
| 39 | P12V_SB | SENSE* | 26 |
| 38 | PS_A0 | VINGOOD | 27 |
| 37 | PSOK | CSHARE | 28 |
| 36 | RETURN | PSON# | 29 |
| 35 | SCL | PS_KILL | 30 |
| 34 | PRESENT# | RESET | 31 |
| 33 | SDA | ALERT | 32 |

P12V
P12V_STBY
SM EMPTY SHORT6 R612 SHORT

PU_PSU0_REMOTE_SENSE_P
PD_PSU0_A0
PWRGD_PSU0 OUT 144
SMB_3V3SB_PMBUS_CLK_R2 IN 143 107 143
PSU0_PRESENT_N OUT
SMB_3V3SB_PMBUS_DAT_R2 BI

PSU0_ISHARE
PD_PSU_REMOTE_SENSE_N
FM_PSU0_VIN_FAIL_N
FM_CSHARE
FM_PS_EN_PSU_N
PD_RST_PS_0
IRQ_SML1_PMBUS_ALERT_R1_N

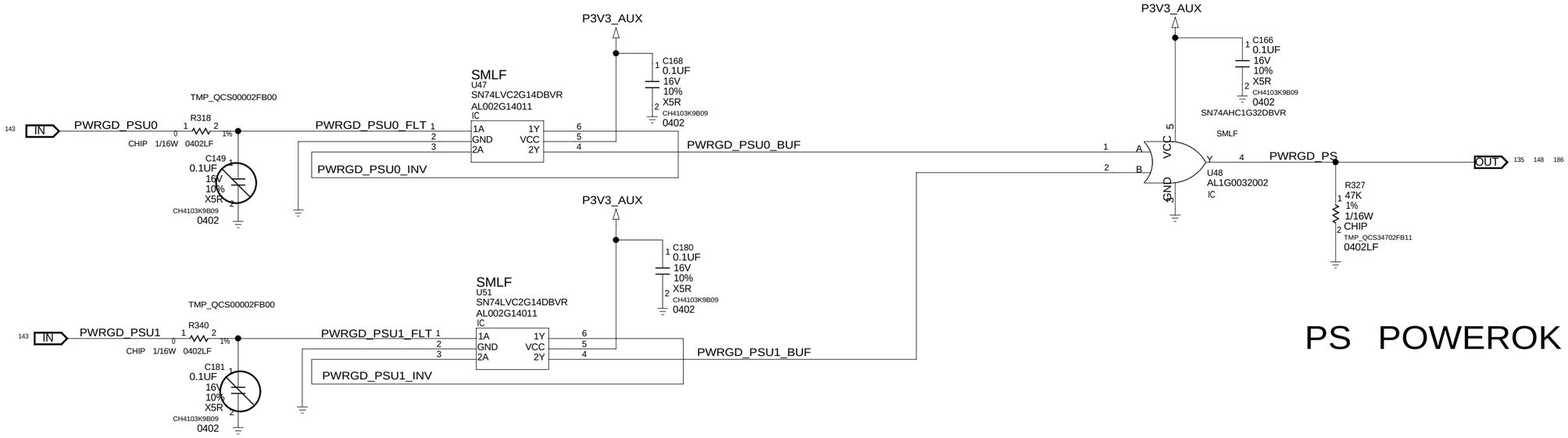
R1844 0 PSU_ISHARE BI 143 143
TMP_QCS11002FB22 1/16W CHIP 0402LF
R609 100 1% R617 100 1% 1/16W CHIP 0402LF TMP_QCS11002FB22 OUT 143
PD_PSU_KILL_0 IN 143

R604 100 1% 1/16W CHIP TMP_QCS11002FB22 0402LF

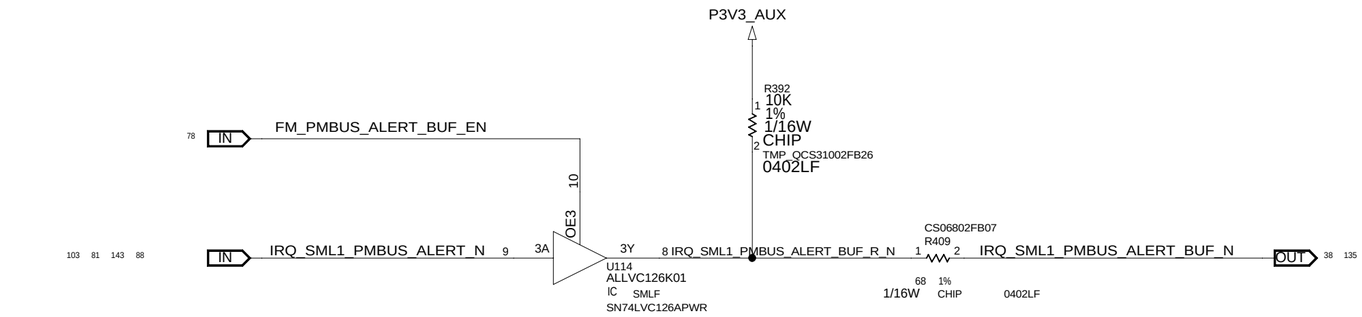
CS03302FB19
SMB_3V3SB_PMBUS_CLK IN 143 147 106 102 81
R623 33 1% 1/16W CHIP 0402LF
SMB_3V3SB_PMBUS_CLK_R2 OUT 143

CS03302FB19
SMB_3V3SB_PMBUS_DAT BI 147 143 106 102 81
R622 33 1% 1/16W CHIP 0402LF
SMB_3V3SB_PMBUS_DAT_R2 BI 143

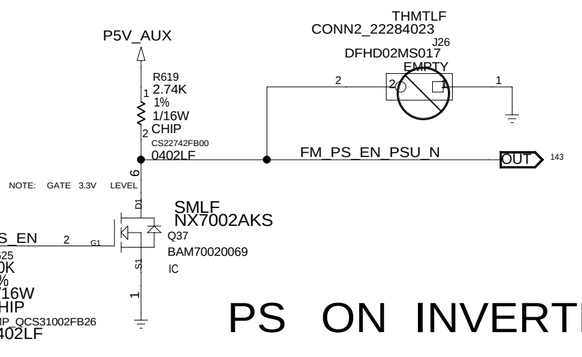
| | | | |
|---|---|---|---|
| DEPARTMENT | CCBU | DESIGNER | NICK |
| REVIEWER | PETER,YULIN,MATT | PROJCET | S2B |
| DOCUMENT NUMBER | DA0S2BMB8A0 | REV | 1 |
| SIZE | C | DATE | Mon Nov 16 11:55:05 2015 |
| SHEET | 143 OF 188 | | |



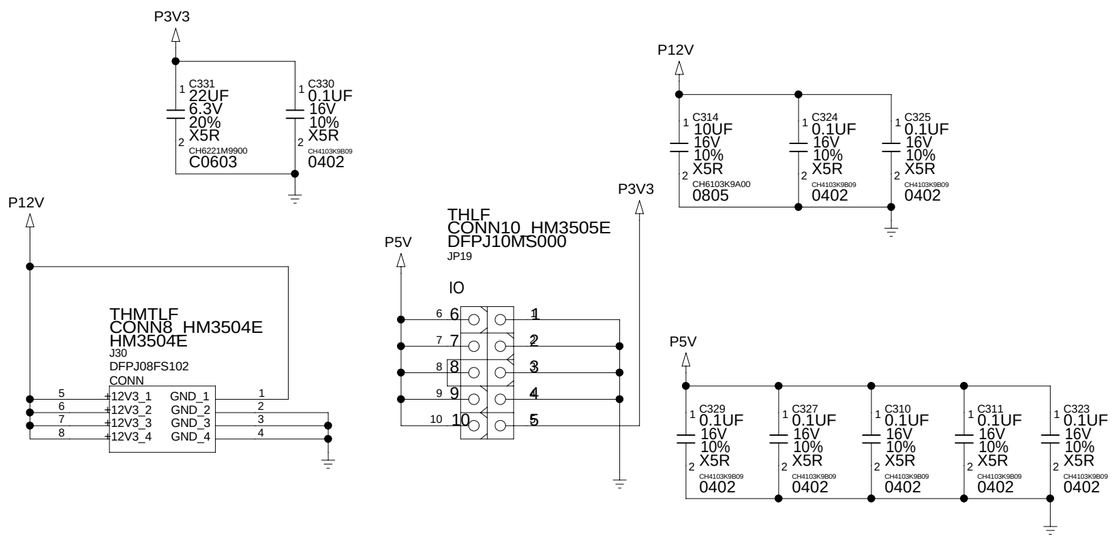

# PS POWEROK OR CIRCUIT



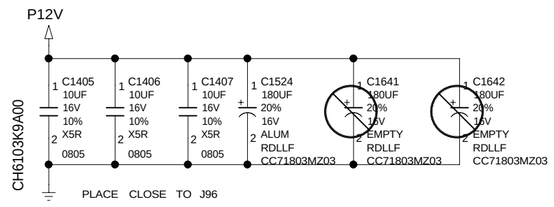

# PMBUS ALRET BUFFER



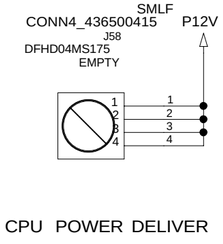

# PS ON INVERTER



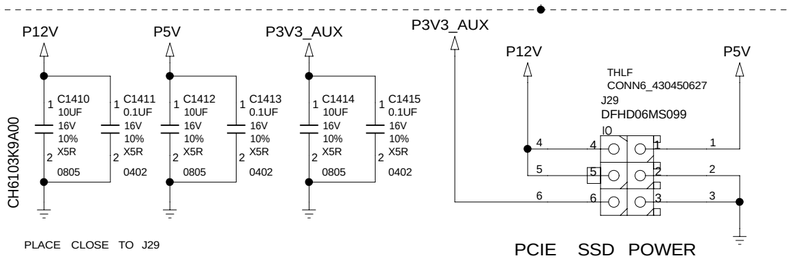

# BACKPLANE POWER CONNECTOR




# GPGPU CONNECTOR




# CPU POWER DELIVER

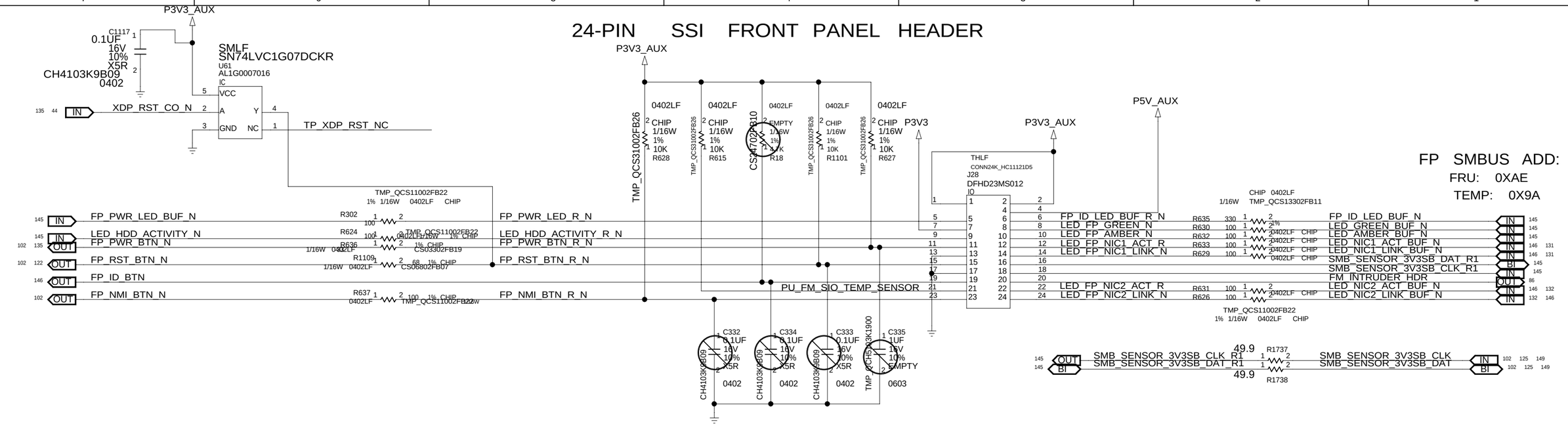



# PCIE SSD POWER

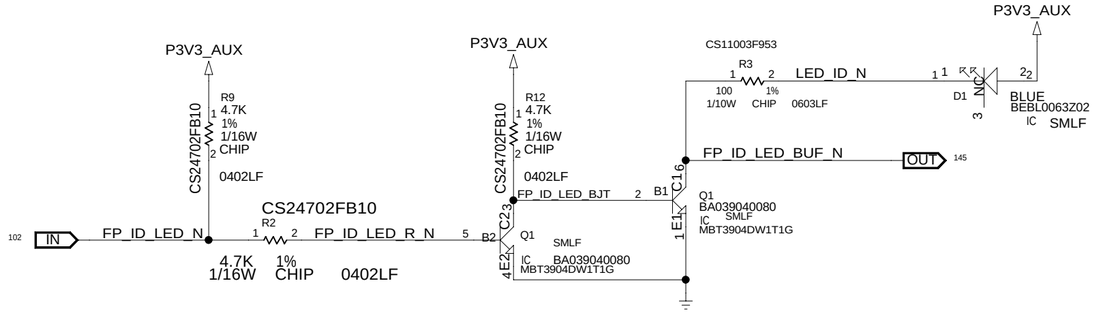
# POWER SUPPLY MISC

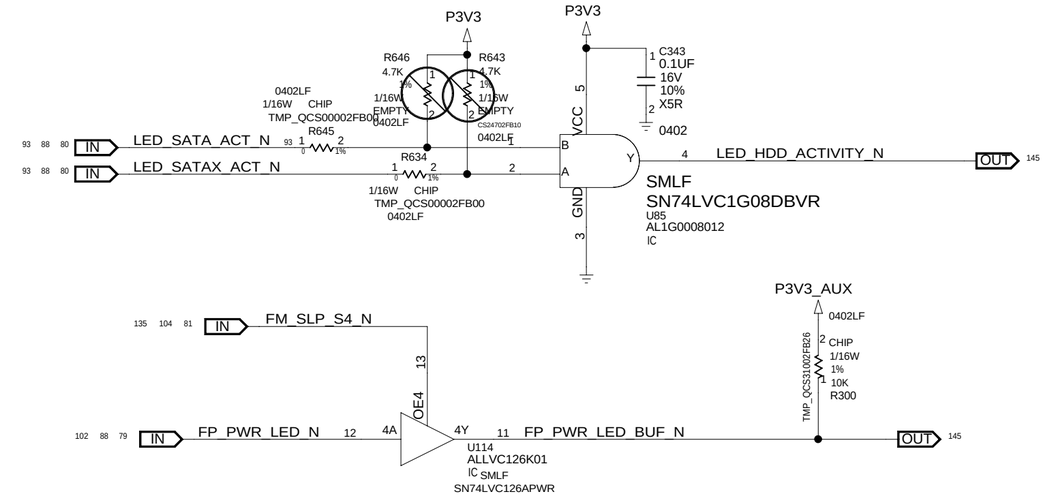
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:55:09 2015 | SHEET 144 OF 188 |

# 24-PIN SSI FRONT PANEL HEADER




BOM NOTE
R3 CHANGE TO CS32323F917 (23.2K)

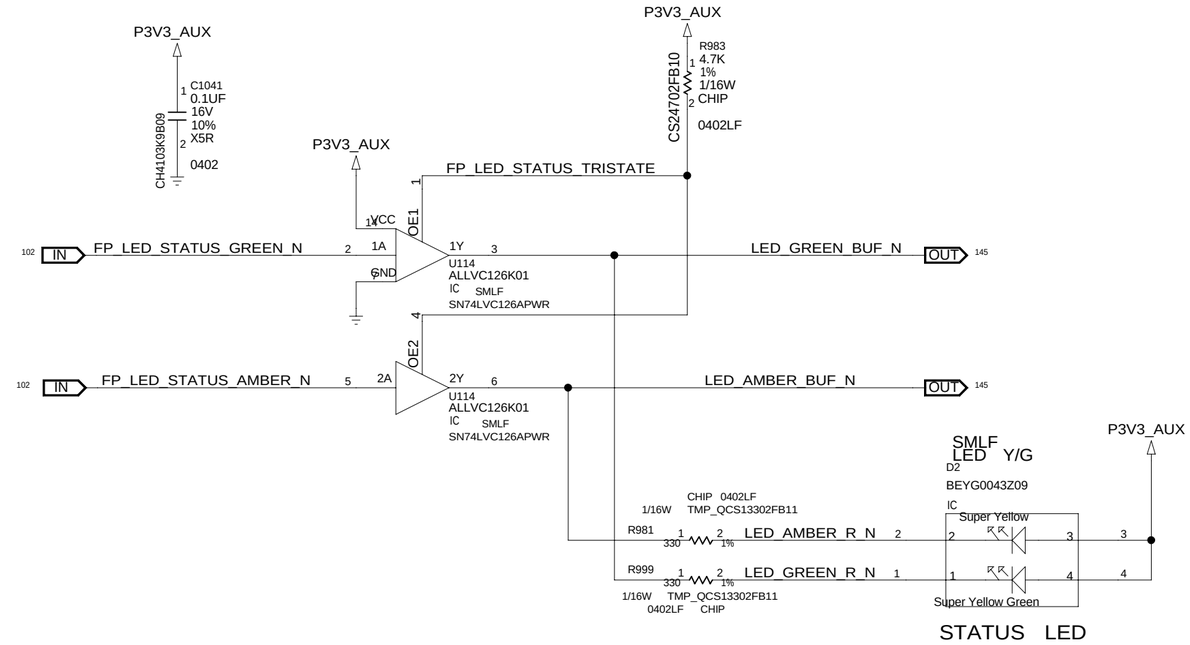




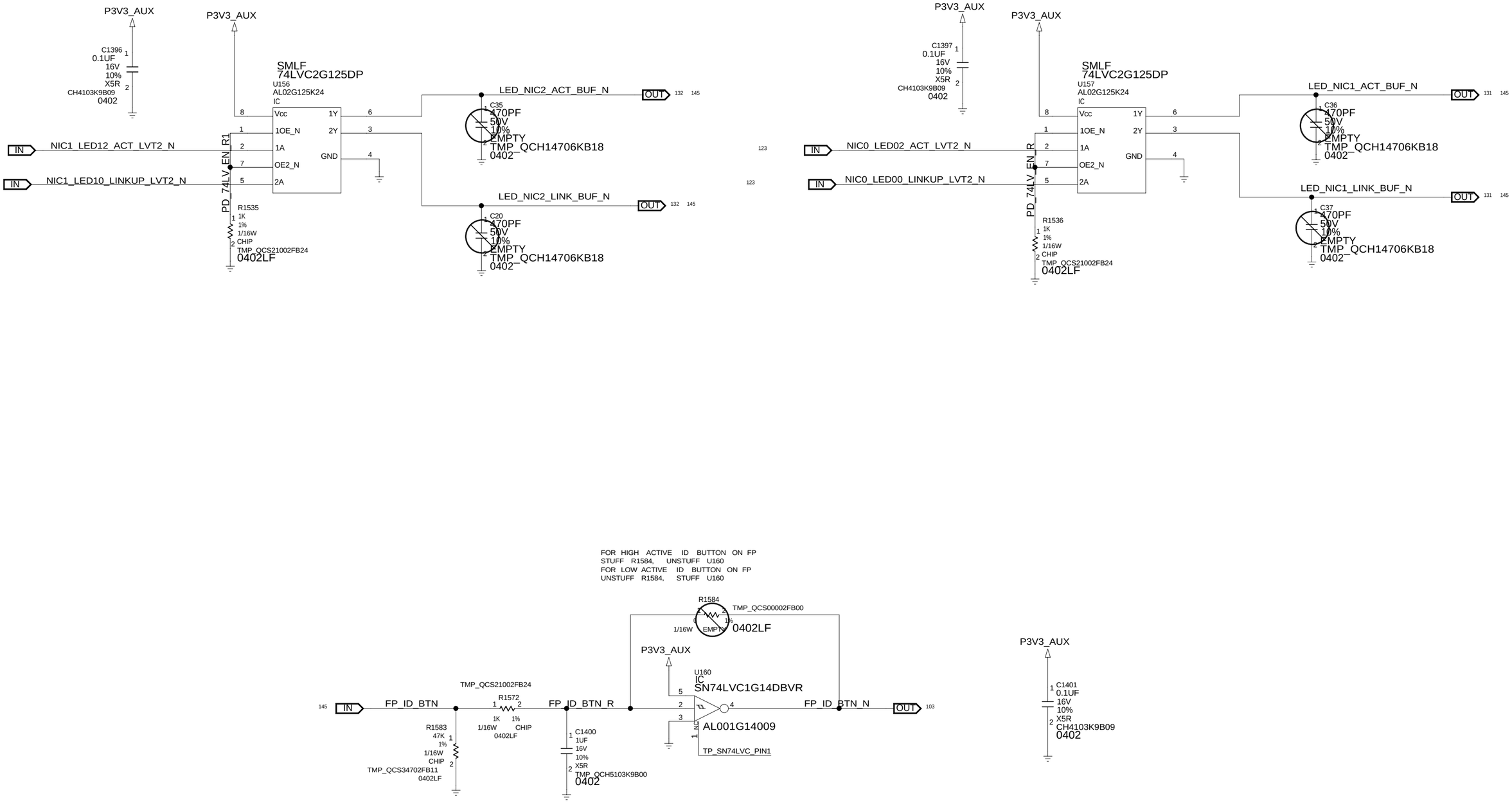


# STATUS & LAN LINK/ACT LEDS BUF




# FRONT CONTROL PANEL

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:55:10 2015 | SHEET 145 OF 188 |

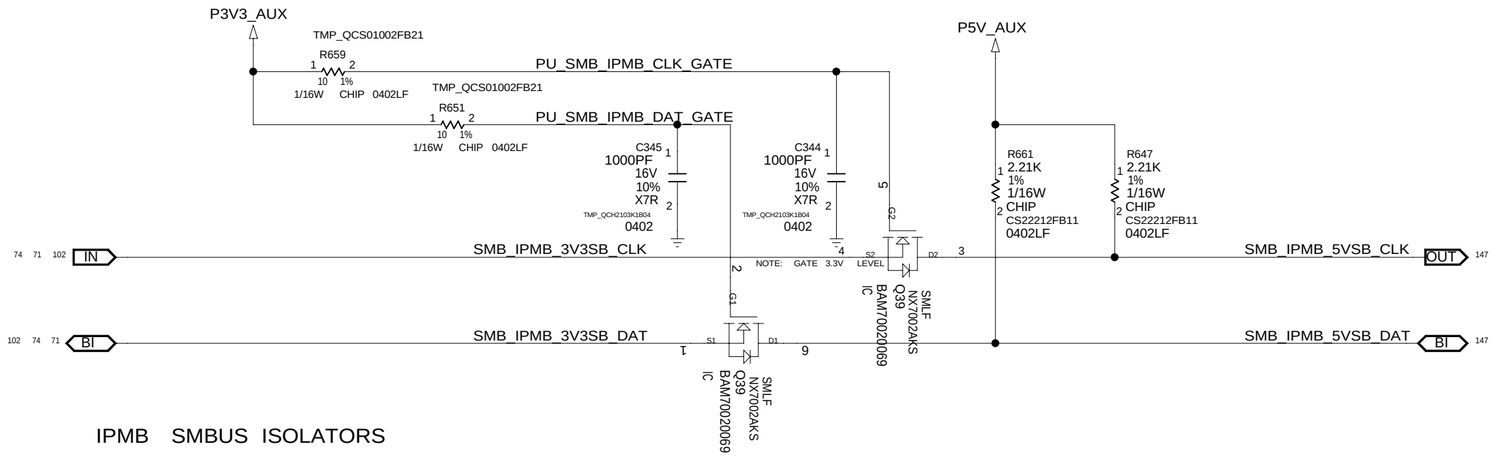


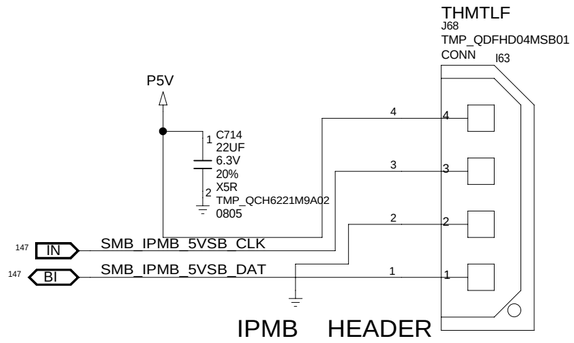

FOR HIGH ACTIVE ID BUTTON ON FP
STUFF R1584, UNSTUFF U160
FOR LOW ACTIVE ID BUTTON ON FP
UNSTUFF R1584, STUFF U160

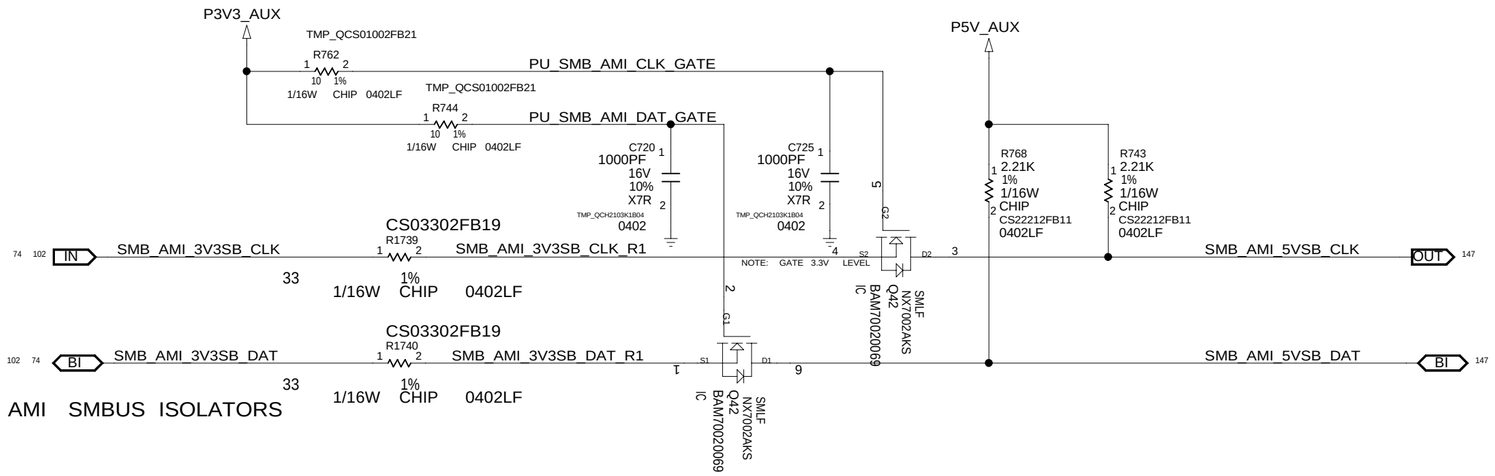


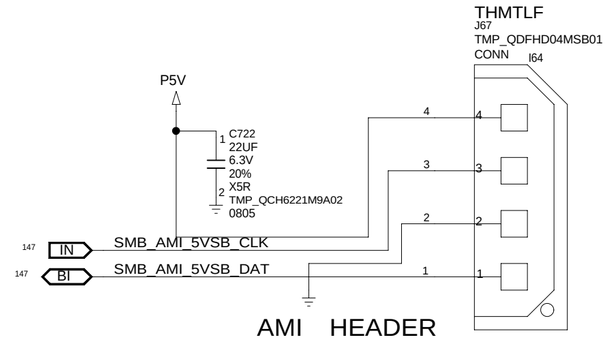

# FRONT_PANEL_RESET_PWR_ID_BTN_BUFFER

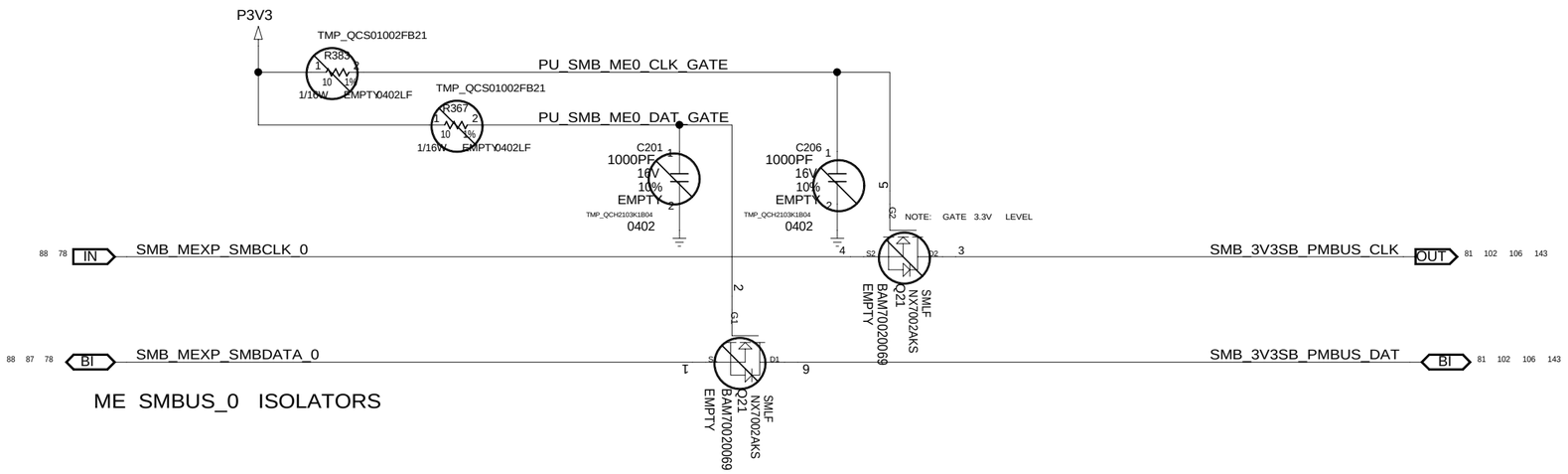
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | | |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Mon Nov 16 11:55:12 2015 | SHEET 146 OF 188 | | |



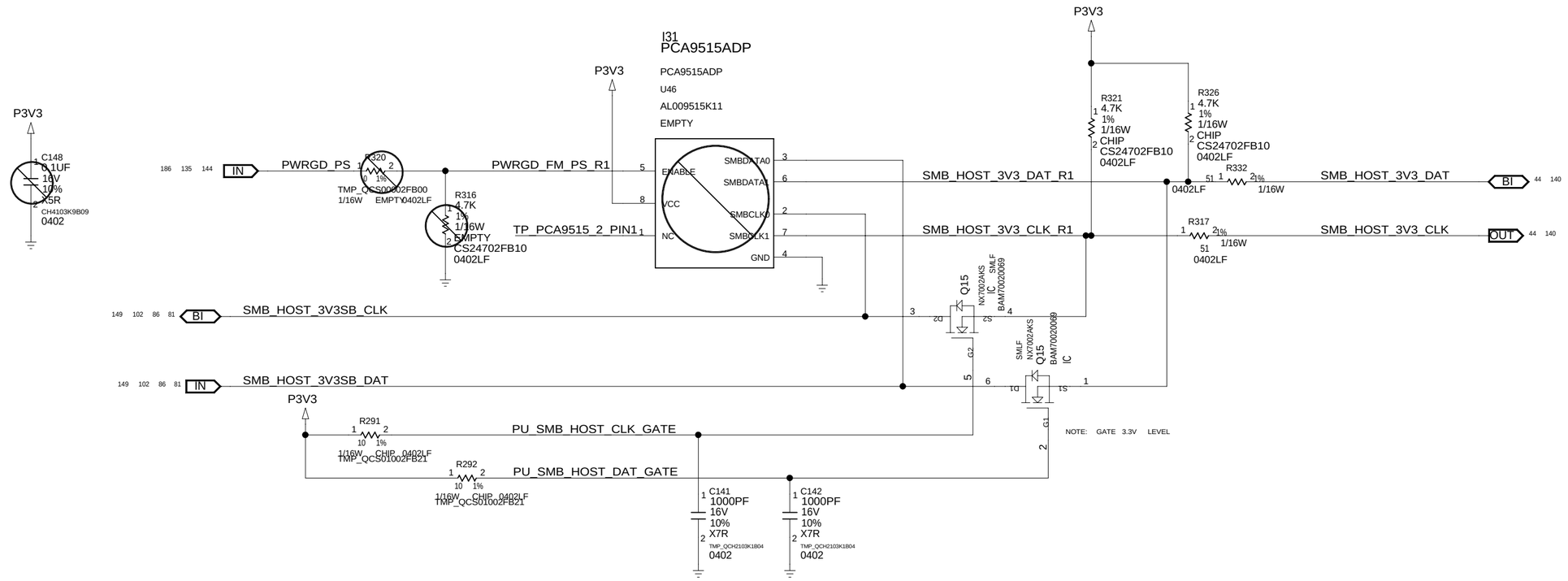




# SMBUS ISOLATION 1 OF 2

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:55:13 2015 | SHEET: 147 OF 188 |

HOST SMBUS REPEATER/ISOLATORS

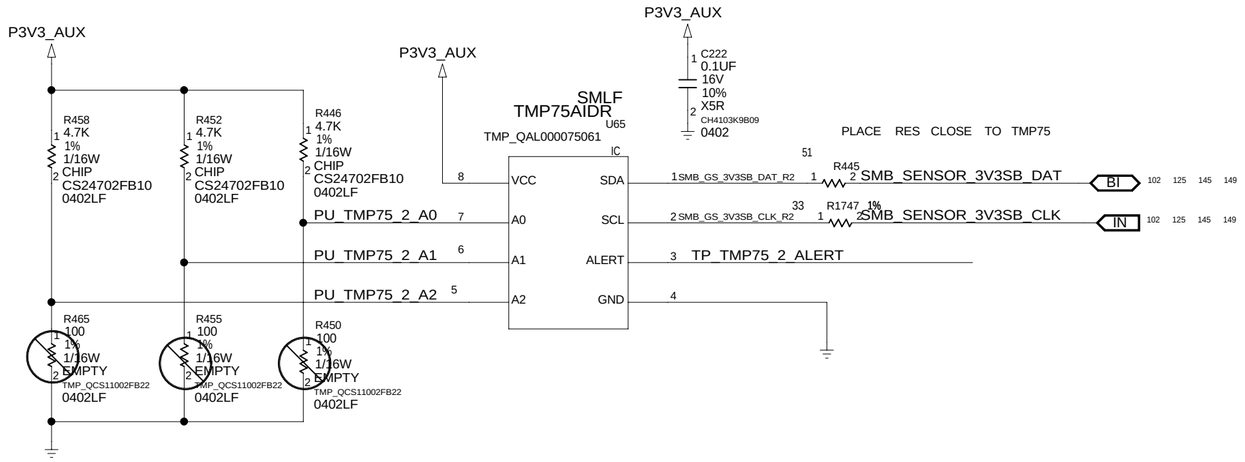



# SMBUS ISOLATION 2 OF 2

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:55:14 2015 | SHEET: 148 OF 188 | |

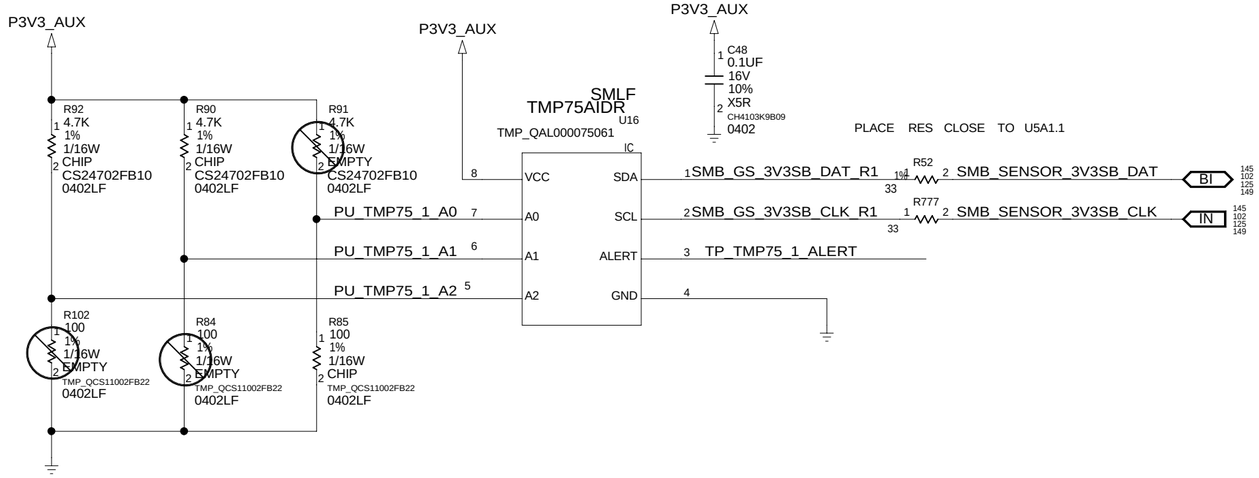
## SMBUS ADDRESS: 0X9E

CAD NOTE:
THIS SENSOR NEED TO BE PLACED IN MILLDE OF THE BOARD



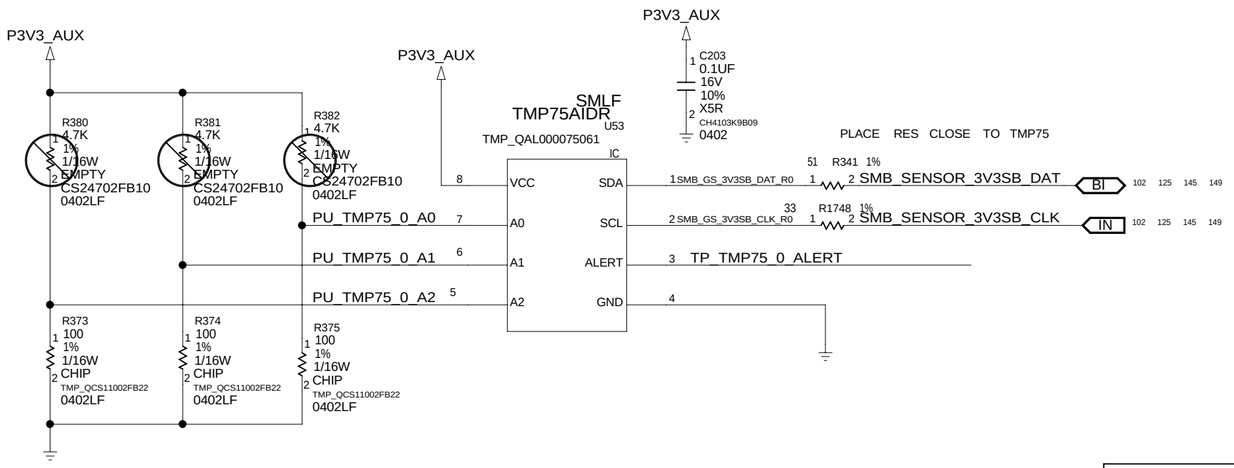

## SMBUS ADDRESS: 0X9C

CAD NOTE:
THIS SENSOR NEED TO BE PLACED IN THE NORTH-WEST SIDE

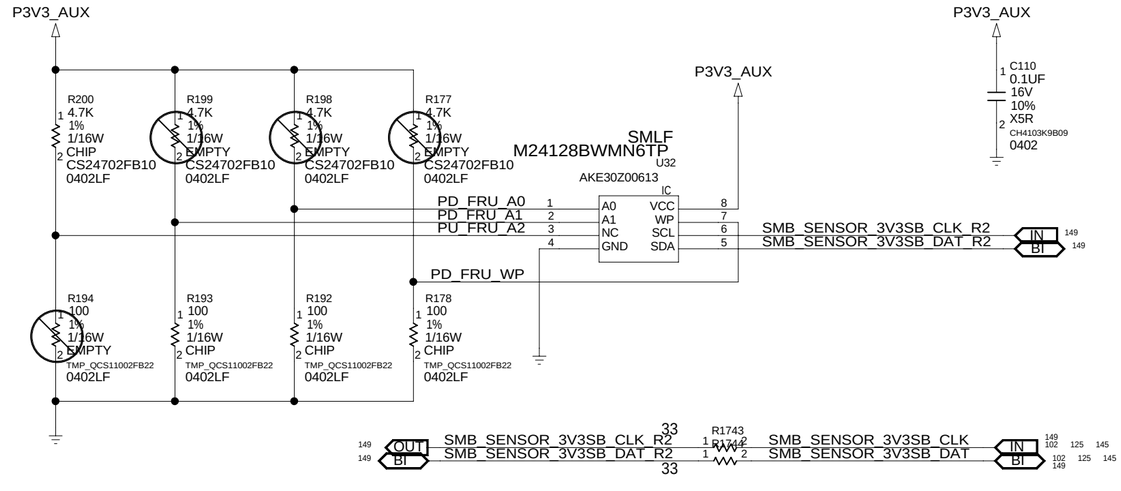



## SMBUS ADDRESS: 0X90

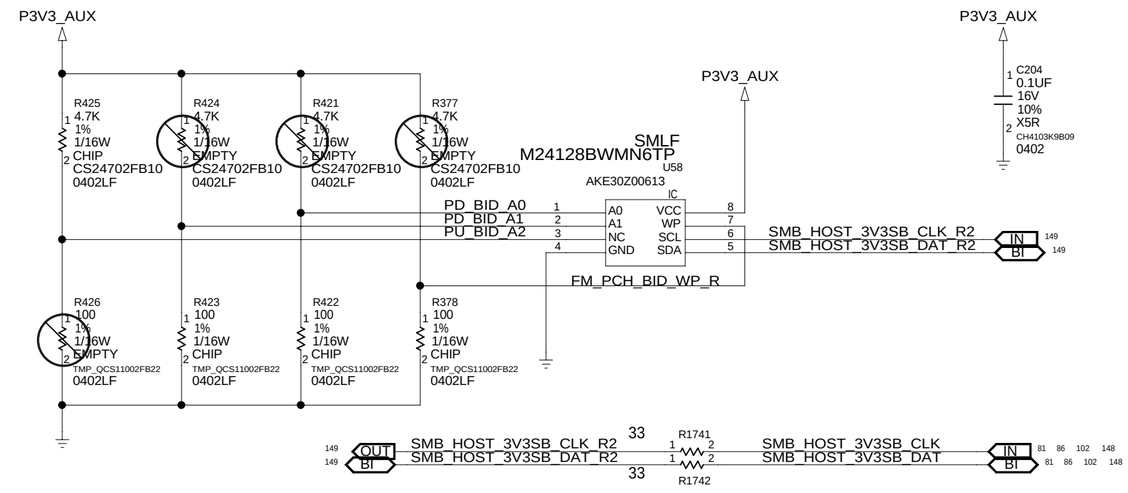
CAD NOTE:
THIS SENSOR NEED TO BE PLACED CLOST TO OCP MEZZ




## BASEBOARD FRU EEPROM
## SMBUS ADDRESS: 0XA8

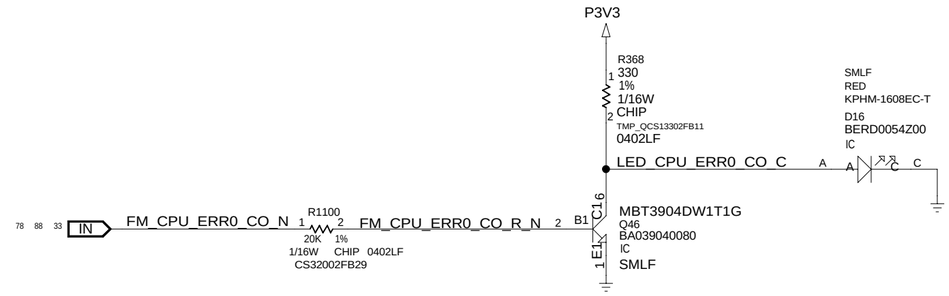


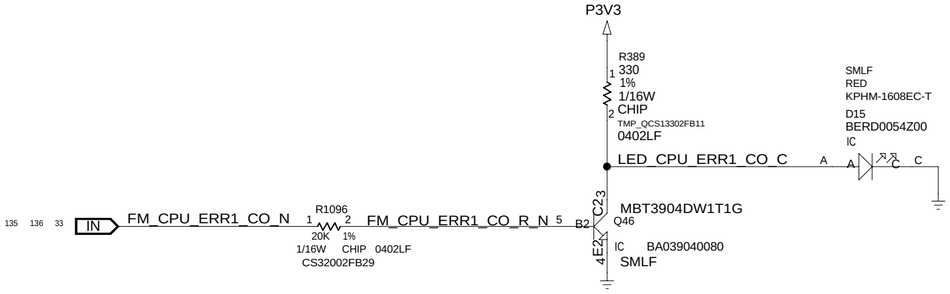

## BOARD ID EEPROM
## SMBUS ADDRESS: 0XA8

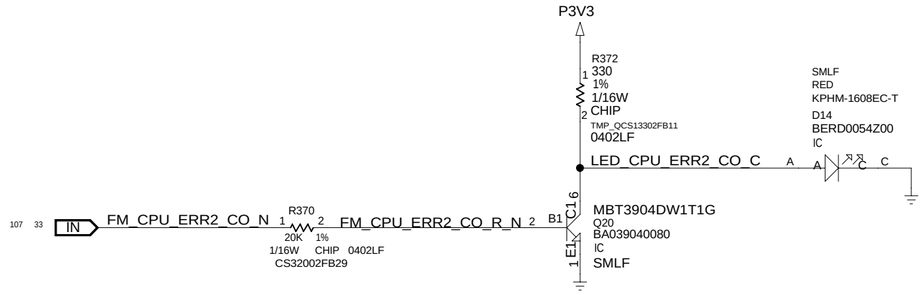



# SMBUS FRU AND TEMP SENSOR

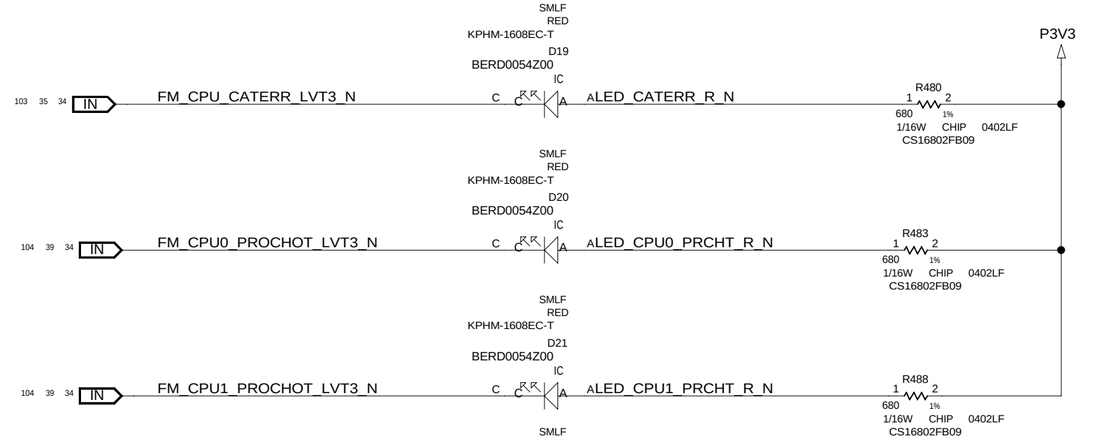
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C | DATE: Mon Nov 16 11:55:15 2015 | SHEET: 149 OF 188 |

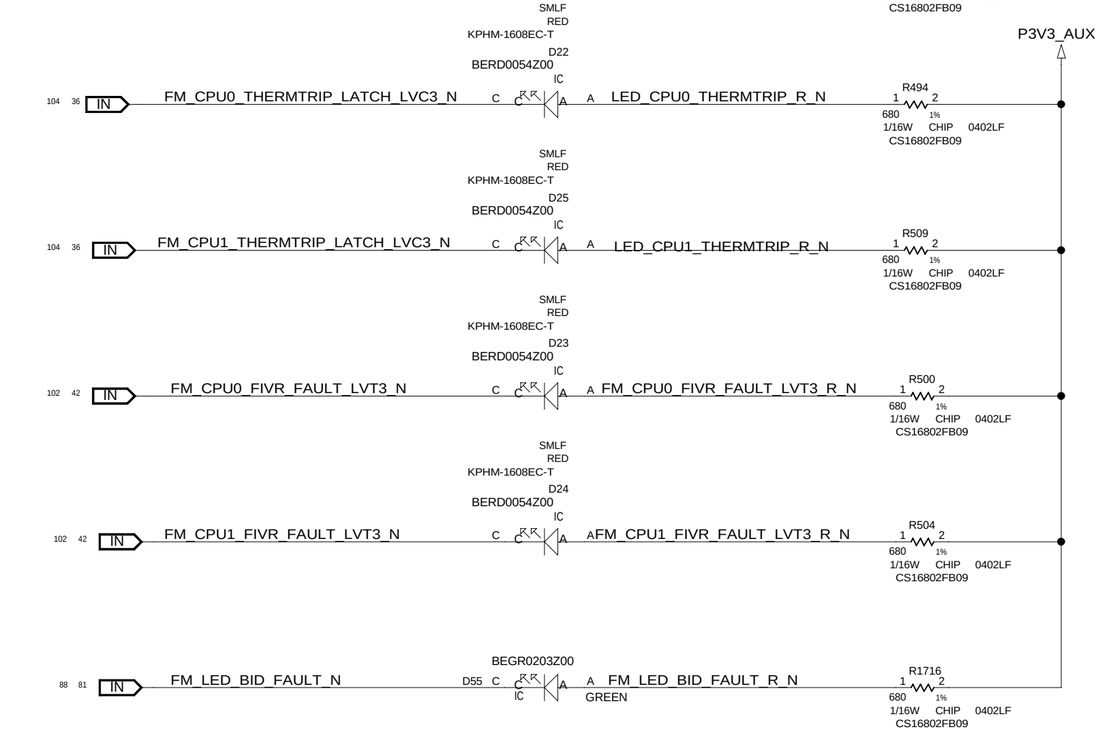


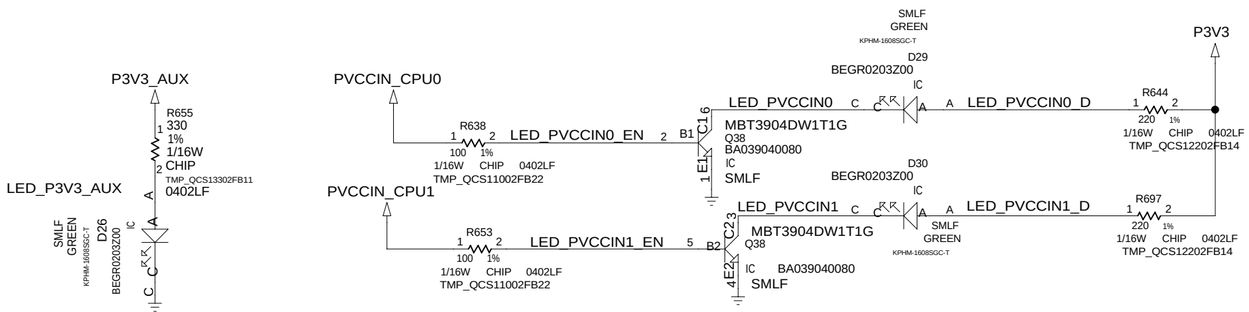



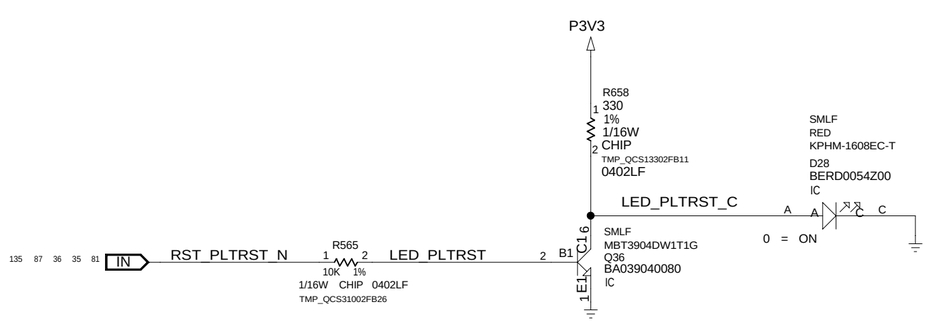

ERROR 0/1/2 LED




SYSTEM POWER LEDS




RESET LEDS

STATUS LED

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: NICK | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: PETER,YULIN,MATT | SIZE: C DATE: Mon Nov 16 11:55:17 2015 | SHEET: 150 OF 188 | |

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|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER PETER,YULIN,MATT | SIZE C | DATE Thu Feb 21 15:18:56 2013 | SHEET 151 OF 188 | |

# DESIGN SPECIFICATION

OUTPUT VOLTAGE = 5.0V+/-5%
OUTPUT RIPPLE & NOISE < 50MV
TRANSIENT TOLERANCE = 500MV
TDC = 10A
MAX CURRENT = 20A
OVER-CURRENT PROTECTION(MAX RATING * 1.2) = 24A
CURRENT STEP = 5A
SLEW RATE = 2.5A/US
WORK FREQUENCY = 300KHZ
EFFICIENCY > 90% @TDC

# DESIGN SPECIFICATION

OUTPUT VOLTAGE = 3.3V+/-5%
OUTPUT RIPPLE & NOISE < 50MV
TRANSIENT TOLERANCE = 330MV
TDC = 12A
MAX CURRENT = 30A
OVER-CURRENT PROTECTION(MAX RATING * 1.2) = 36A
CURRENT STEP = 6A
SLEW RATE = 2.5A/US
WORK FREQUENCY = 355KHZ
EFFICIENCY > 90% @TDC

P12V_AUX
PL21 0.1UH SMLF SMD 4*4*6 CV+10G0MZ01 IND
SW_P5V_AUX_P3V3_AUX_FLT
PC40 270UF 20% 16V OSCON RDLLF ESR = 10M TMP_QCC72703MD03 8*9
PC42 10UF 25V 20% X6S TMP_QCH61004M2E8 1206
PC43 10UF 25V 20% X6S TMP_QCH61004M2E8 1206
PC46 10UF 25V 20% X6S TMP_QCH61004M2E8 1206
PC50 10UF 25V 20% X6S TMP_QCH61004M2E8 1206
PC51 10UF 25V 20% X6S TMP_QCH61004M2E8 1206
PC44 10UF 25V 20% X6S TMP_QCH61004M2E8 1206
PC48 270UF 20% 16V OSCON RDLLF ESR = 10M TMP_QCC72703MD03 8*9
P12V_AUX
PC369 0.1UF 16V 10% X5R CH4103K9B09 0402
PQ3 CSD86360Q5D SMLF BAM86360000 IC
PU32 SMLF TPS51225RUKR AL051225000 IC
PQ2 CSD86360Q5D SMLF BAM86360000 IC
ISAT = 40A DCR = 0.5M SMD 13*13*10 SMLF 1.2UH/43A PL20 CV-12^0KZ00 IND
ISAT = 50A DCR = 0.5M SMD 13*13*10 SMLF 1.0UH/50A PL19 CV-10^0KZ00 IND
P5V_AUX
P3V3_AUX
SW_P5V_AUX_PH
SW_P3V3_AUX_PH
PC45 560UF 20% 6.3V OSCON RDLLF ESR = 7M TMP_QCC75601MD01 6.3*9
PC47 0.1UF 16V 10% X5R CH4103K9B09 0402
PR136 15K 1% 1/16W CHIP TMP_QCS31502FB24 0402LF
PR133 9.76K 1% 1/16W CHIP CS29762FB00 0402LF
PR137 6.49K 1% 1/16W CHIP TMP_QCS26492FB23 0402LF
PR134 10K 1% 1/16W CHIP TMP_QCS31002FB26 0402LF
PC36 560UF 20% 6.3V OSCON RDLLF ESR = 7M TMP_QCC75601MD01 6.3*9
PC39 0.1UF 16V 10% X5R CH4103K9B09 0402
SW_P5V_AUX_UG
SW_P5V_AUX_LG
P5V_AUX_BT
SW_P5V_AUX_SW
SW_P3V3_AUX_UG
SW_P3V3_AUX_LG
P3V3_AUX_BT
SW_P3V3_AUX_SW
PC371 0.1UF 10% 16V X5R 0402 CH4103K9B09
PC370 0.1UF 10% 16V X5R 0402 CH4103K9B09
RDS = 1.8M/4.5V MAX
RDS = 1.8M/4.5V MAX
VIN DRVH1 DRVL1 VBST1 SW1 VO1 VFB1 EN1 EN2 CS1 VREG5
DRVH2 DRVL2 VBST2 SW2 VFB2 VCLK PGOOD CS2 VREG3 GND
P5V_AUX_FB
P5V_AUX_VR_EN1
P3V3_AUX_VR_EN2
P5V_AUX_CS
P5V_AUX_VREG
P3V3_AUX_FB
TP_P3V3AUX_VCLK
PWRGD_P5V_AUX_P3V3_AUX
P3V3_AUX_CS
P3V3_AUX_VREG
152 IN P3V3_AUX_VREG
PR128 68.1K 1% 1/16W CHIP 0402LF
PR126 100K 1% 1/16W CHIP 0402LF
PR125 10K 1% 1/16W CHIP TMP_QCS31002FB26 0402LF
OUT 154 160
OUT 152
PC49 560UF 20% 6.3V OSCON RDLLF TMP_QCC75601MD01
PR127 154K 1% 1/16W CHIP CS41542FB16 0402LF
PR131 100K 1% 1/16W CHIP 0402LF
PC1404 0.01UF 16V 10% EMPTY TMP_QCH31003KB11 0402
PR129 30.1K 1% 1/16W CHIP CS33012FB18 0402LF
PC368 1UF 16V 10% X5R TMP_QCH5103K9B00 0402
PC372 1UF 16V 10% X5R TMP_QCH5103K9B00 0402
PR132 46.4K 1% 1/16W CHIP CS34642FB16 0402LF
PC41 560UF 20% 6.3V OSCON RDLLF TMP_QCC75601MD01

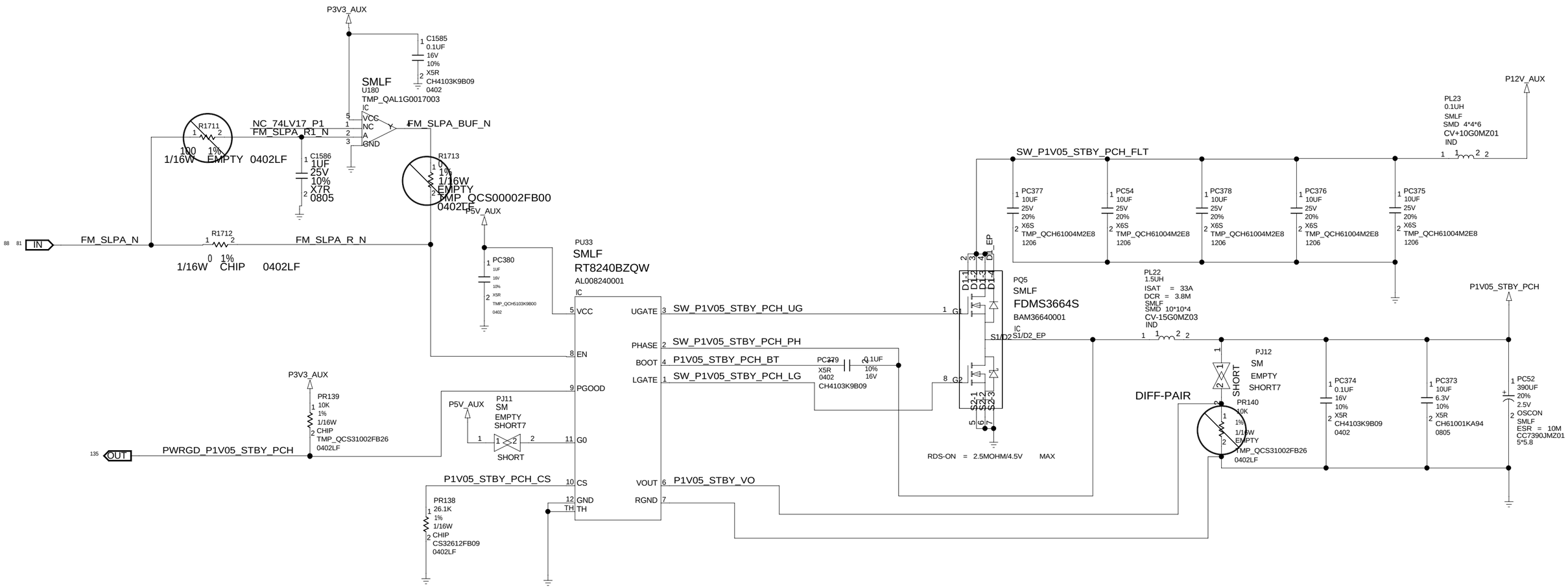
# P5V_AUX & P3V3_AUX

Quanta

| DEPARTMENT | DESIGNER | PROJCET | DOCUMENT NUMBER | REV |
|---|---|---|---|---|
| CCBU | BEN CHIANG | S2B | DA0S2BMB8A0 | 1 |
| | REVIEWER NICK,PETER,MATT,KUOCHAN | SIZE C | DATE Mon Nov 16 11:55:18 2015 | SHEET 152 OF 188 |

# DESIGN SPECIFICATION

OUTPUT VOLTAGE = 1.05+/-5%
OUTPUT RIPPLE & NOISE < 21MV
TRANSIENT TOLERANCE = 105MV
TDC = 6.8A
MAX CURRENT = 8A
OVER-CURRENT PROTECTION(MAX RATING * 1.2) = 10.4A
CURRENT STEP = 5A
SLEW RATE = 1A/US
WORK FREQUENCY = 400KHZ
EFFICIENCY > 90% @TDC




P1V05_STBY_PCH

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: BEN CHIANG | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: NICK,PETER,MATT,KUOCHAN | SIZE: C | DATE: Mon Nov 16 11:55:21 2015 | SHEET: 153 OF 188 | |

# DESIGN SPECIFICATION

OUTPUT VOLTAGE = 1.8+/-5%
OUTPUT RIPPLE & NOISE < 36MV
TRANSIENT TOLERANCE = 180MV
TDC = 1A
MAX CURRENT = 2A
OVER-CURRENT PROTECTION(MAX RATING * 1.4) = 2.8A
CURRENT STEP = 0.2A
SLEW RATE = 1A/US
WORK FREQUENCY = 300KHZ
EFFICIENCY > 90% @TDC

P12V_AUX
SMLF
0.1UH
PL17
CV+10G0MZ01
IND
SMD 4*4*6

PC363 10UF 25V 20% X6S TMP_QCH61004M2E8 1206
PC24 10UF 25V 20% X6S TMP_QCH61004M2E8 1206
PC362 10UF 25V 20% EMPTY TMP_QCH61004M2E8 1206
PC23 0.1UF 16V 10% X5R CH4103K9B09 0402

SW_P1V8_AUX_FLT

P3V3_AUX
PR123 10K 1% 1/16W CHIP TMP_QCS31002FB26 0402LF

SMLF
HPA02167RVER
PU5
AL002167000
IC

VIN_1 15
VIN_2 16
VIN_3 17
VIN_4 18
PGOOD 2 → PWRGD_P1V8_AUX → OUT 155
MODE 21
VBST 4
SW_1 5
SW_2 6
SW_3 7
SW_4 8
SW_5 9
EN 3 ← IN 160 152 PWRGD_P5V_AUX_P3V3_AUX
VDD 19
VREG 20 → P1V8_AUX_VREG
RF 1 → P1V8_AUX_RF
NC 26 → TP_P1V8AUX_53513_26
TRIP 25 → P1V8_AUX_TRIP
VO 24
FB 23 ← P1V8_AUX_FB
GND_1 27
GND_2 28
AGND 22
PGND_1 10
PGND_2 11
PGND_3 12
PGND_4 13
PGND_5 14
GND-PAD TH

P1V8_AUX_BT
PC364 0.1UF X5R 0402 10% 16V CH4103K9B09
SW_P1V8_AUX_PH
PL18 2.2UH ISAT = 18A DCR = 6M SMLF SMD 10*10*4 CV-22C0MZ02 IND

P1V8_AUX
PC367 0.1UF 16V 10% X5R CH4103K9B09 0402
PC366 10UF 6.3V 10% X5R CH61001KA94 0805
PC365 10UF 6.3V 10% X5R CH61001KA94 0805
PC35 390UF 20% 2.5V OSCON SMLF CC7390JMZ01
ESR = 10M 5*5.8

P5V_AUX
PC22 1UF 16V 10% X5R TMP_QCH5103K9B00 0402
PC21 1UF 16V 10% X5R TMP_QCH5103K9B00 0402

PR121 255K 1% 1/16W CHIP CS42552FB05 0402LF
PR122 27K 1% 1/16W CHIP CS32702FB16 0402LF
PR18 24.9K 1% 1/16W CHIP CS32492FB16 0402LF

RA
PR17 20K 1% 1/16W 0402LF CHIP CS32002FB29
PR16 10K 1% 1/16W CHIP TMP_QCS31002FB26 0402LF
RB

VO=0.6(1+RA/RB) = 1.8V

P1V8_AUX

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER BEN CHIANG | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER NICK,PETER,MATT,KUOCHAN | SIZE C | DATE Mon Nov 16 11:55:23 2015 | SHEET 154 OF 188 |

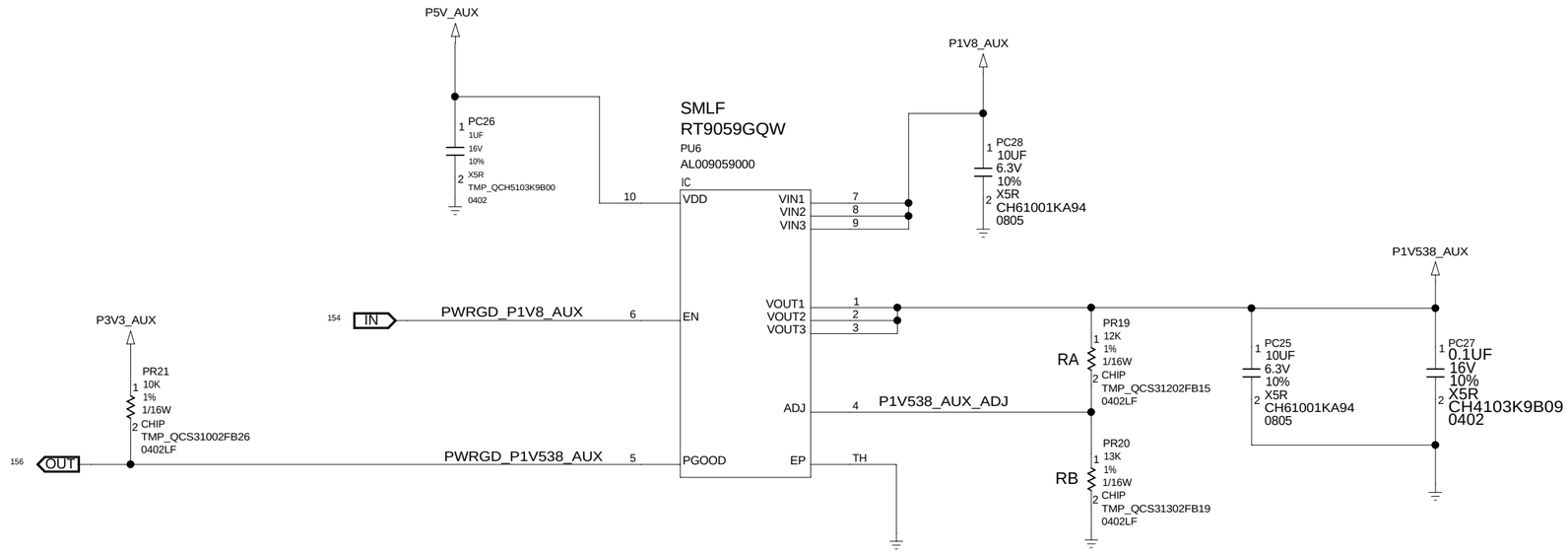
OUTPUT VOLTAGE = 1.538V+/-5%

OUTPUT RIPPLE & NOISE < 30MV

TRANSIENT TOLERANCE = 153.8MV

MAX CURRENT = 1.9A

PD = (1.8V - 1.538V) * 1.9A =0.4978W




VNOM=0.8(1+RA/RB)=1.538

P1V538_AUX

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: BEN CHIANG | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: NICK,PETER,MATT,KUOCHAN | SIZE: C DATE: Mon Nov 16 11:55:24 2015 | SHEET: 155 OF 188 | |

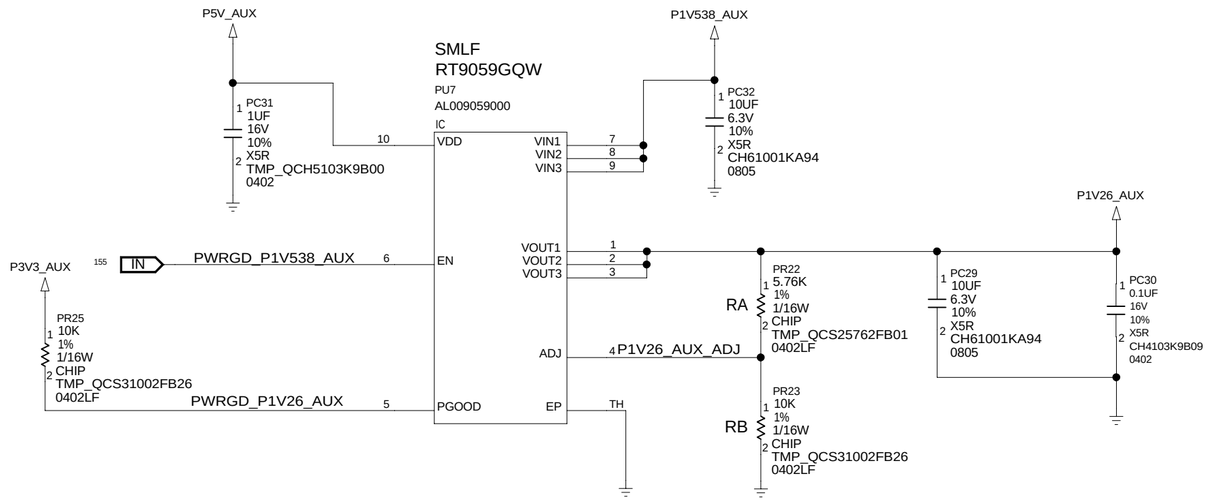
OUTPUT VOLTAGE = 1.26V+/-5%

OUTPUT RIPPLE & NOISE < 30MV

TRANSIENT TOLERANCE = 126MV

MAX CURRENT = 1.1A

PD = (1.538V - 1.26V) * 1.1A = 0.3058W




VNOM=0.8(1+RA/RB)=1.26

P1V26_AUX

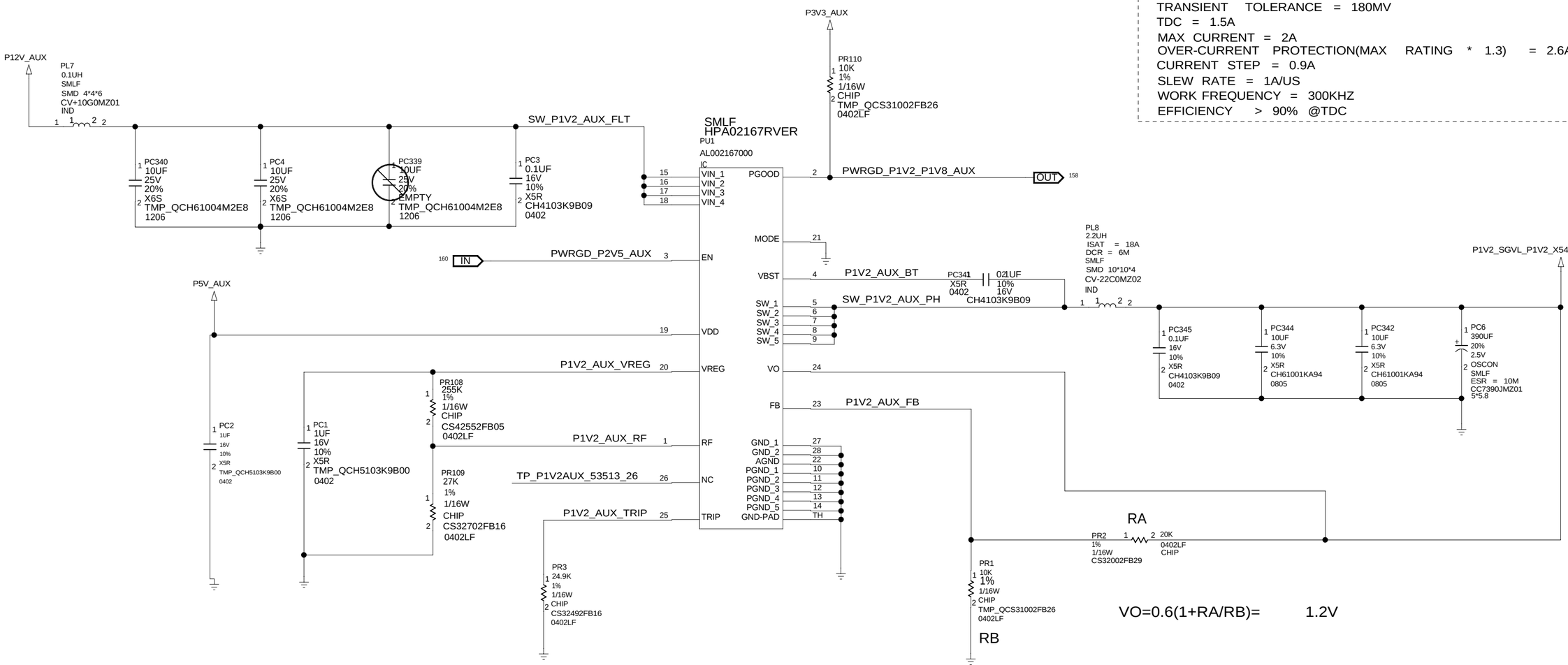
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: BEN CHIANG | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: NICK,PETER,MATT,KUOCHAN | SIZE: C | DATE: Mon Nov 16 11:55:25 2015 | SHEET: 156 OF 188 |

## X540 DESIGN SPECIFICATION

OUTPUT VOLTAGE = 1.2+/-2% DC +-3% AC
OUTPUT RIPPLE & NOISE < 24MV
TRANSIENT TOLERANCE = 180MV
TDC = 1.5A
MAX CURRENT = 2A
OVER-CURRENT PROTECTION(MAX RATING * 1.3) = 2.6A
CURRENT STEP = 0.9A
SLEW RATE = 1A/US
WORK FREQUENCY = 300KHZ
EFFICIENCY > 90% @TDC

## I350 DESIGN SPECIFICATION

OUTPUT VOLTAGE = 1.8+/-2% DC +-3% AC
OUTPUT RIPPLE & NOISE < 36MV
TRANSIENT TOLERANCE = 180MV
TDC = 1.5A
MAX CURRENT = 2A
OVER-CURRENT PROTECTION(MAX RATING * 1.3) = 2.6A
CURRENT STEP = 0.9A
SLEW RATE = 1A/US
WORK FREQUENCY = 300KHZ
EFFICIENCY > 90% @TDC




| | RA | VOUT |
|---|---|---|
| X540 | 10K | 1.2V |
| I350 | 20K | 1.8V |

P1V2_X540_P1V8_I350

| | | | | |
|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER BEN CHIANG<br>REVIEWER NICK,PETER,MATT,KUOCHAN | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 REV 1 |
| | | | SIZE C | DATE Mon Nov 16 11:55:28 2015 |
| | | | | SHEET 157 OF 188 |

## X540 DESIGN SPECIFICATION

OUTPUT VOLTAGE = 0.8+/-2% DC +-3% AC
OUTPUT RIPPLE & NOISE < 16MV
TRANSIENT TOLERANCE = 80MV
TDC = 4.5A
MAX CURRENT = 10A
OVER-CURRENT PROTECTION(MAX RATING * 1.3) = 12A
CURRENT STEP = 4A
SLEW RATE = 1A/US
WORK FREQUENCY = 300KHZ
EFFICIENCY > 90% @TDC

## I350 DESIGN SPECIFICATION

OUTPUT VOLTAGE = 1+/-2% DC +-3% AC
OUTPUT RIPPLE & NOISE < 20MV
TRANSIENT TOLERANCE = 100MV
TDC = 4.5A
MAX CURRENT = 8A
OVER-CURRENT PROTECTION(MAX RATING * 1.3) = 10.4A
CURRENT STEP = 4A
SLEW RATE = 1A/US
WORK FREQUENCY = 300KHZ
EFFICIENCY > 90% @TDC

P12V_AUX
PL14 0.1UH SMLF SMD_4*4*6 CV+10G0MZ01 IND
PC355 10UF 25V 20% X6S TMP_QCH61004M2E8 1206
PC360 10UF 25V 20% X6S TMP_QCH61004M2E8 1206
PC17 10UF 25V 20% X6S TMP_QCH61004M2E8 1206
PC16 0.1UF 16V 10% X5R CH4103K9B09 0402
SW_P0V8_AUX_FLT

P3V3_AUX
PR114 10K 1% 1/16W CHIP TMP_QCS31002FB26 0402LF

SMLF HPA02167RVER PU3 AL002167000 IC
VIN_1 VIN_2 VIN_3 VIN_4 PGOOD
PWRGD_P0V8_P1V0_AUX → OUT 159

157 IN PWRGD_P1V2_P1V8_AUX → EN
MODE
VBST
P0V8_AUX_BT
PC351 0.1UF 10% 16V X5R 0402
SW_1 SW_2 SW_3 SW_4 SW_5
SW_P0V8_AUX_PH
CH4103K9B09
VDD
VREG
P0V8_AUX_VREG
VO
FB
P0V8_AUX_FB
RF
P0V8_AUX_RF
NC
TP_P0V8AUX_53513_26
TRIP
P0V8_AUX_TRIP
GND_1 GND_2 AGND PGND_1 PGND_2 PGND_3 PGND_4 PGND_5 GND-PAD TH

PL11 1.5UH ISAT = 33A DCR = 3.8M SMLF SMD_10*10*4 CV-15G0MZ03 IND
P0V85_SGVL_P0V8_X540_P1V0_I350
PC12 390UF 20% 2.5V OSCON SMLF ESR = 10M CC7390JMZ01 5*5.8
PC352 10UF 6.3V 10% X5R CH61001KA94 0805
PC354 10UF 6.3V 10% X5R CH61001KA94 0805
PC353 0.1UF 16V 10% X5R CH4103K9B09 0402

P5V_AUX
PC13 1UF 16V 10% X5R TMP_QCH5103K9B00 0402
PC11 1UF 16V 10% X5R TMP_QCH5103K9B00 0402
PR118 255K 1% 1/16W CHIP CS42552FB05 0402LF
PR116 27K 1% 1/16W CHIP CS32702FB16 0402LF
PR7 42.2K 1% 1/16W CHIP TMP_QCS34222FB00 0402LF

RA
PR6 6.65K 1% 1/16W 0402LF CHIP TMP_QCS26652FB06
PR9 10K 1% 1/16W CHIP TMP_QCS31002FB26 0402LF
RB

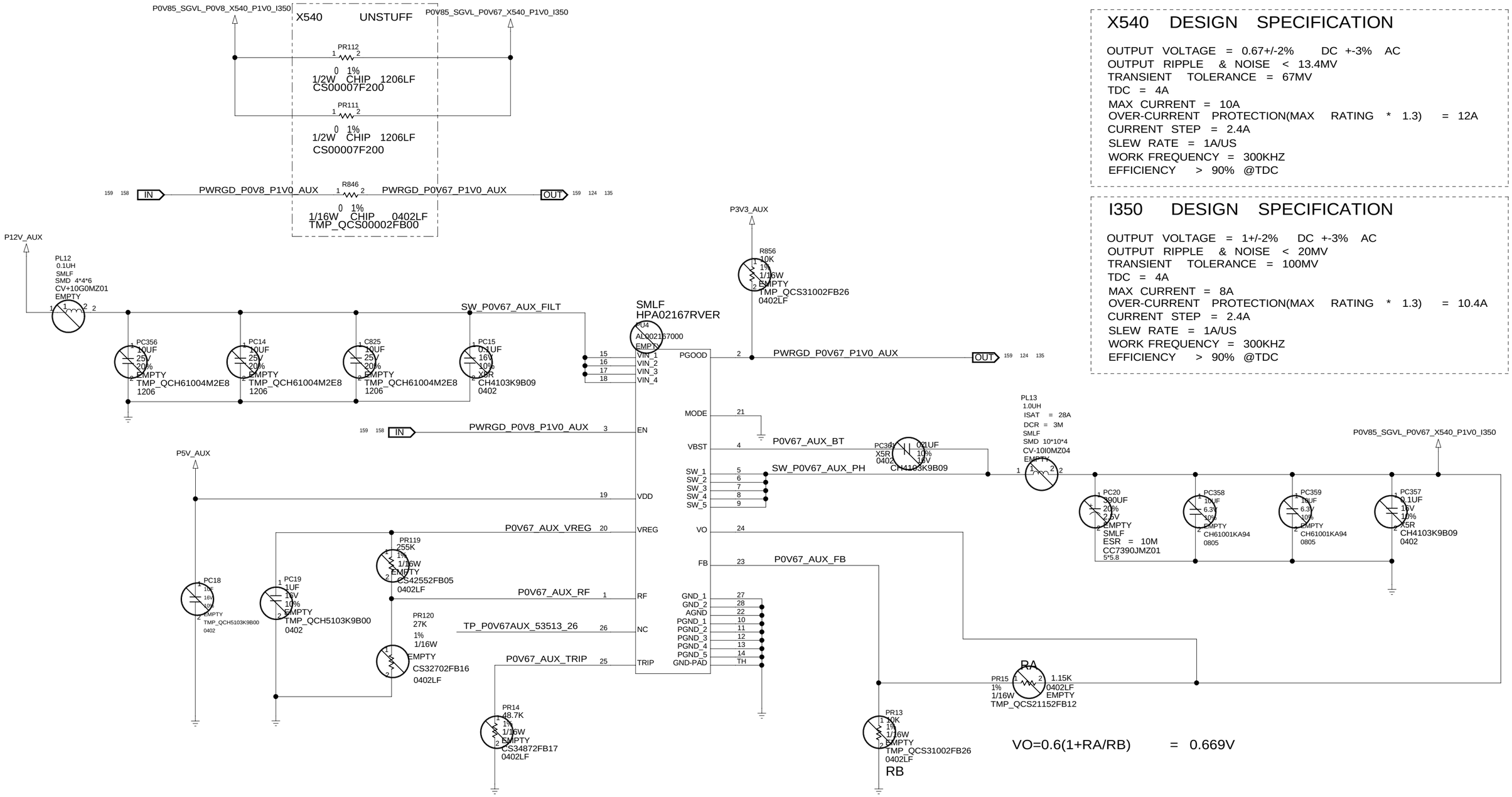
VO=0.6(1+RA/RB) = 0.804V

| | RA | VOUT |
|---|---|---|
| X540 | 3.4K | 0.804V |
| I350 | 6.65K | 0.999V |
| SAGEVILLE | 4.22K | 0.853V |

# P0V8_X540_P1V0_I350

| | | | | |
|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: BEN CHIANG | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 |
| | | REVIEWER: NICK,PETER,MATT,KUOCHAN | SIZE: C DATE: Mon Nov 16 11:55:29 2015 | SHEET: 158 OF 188 |

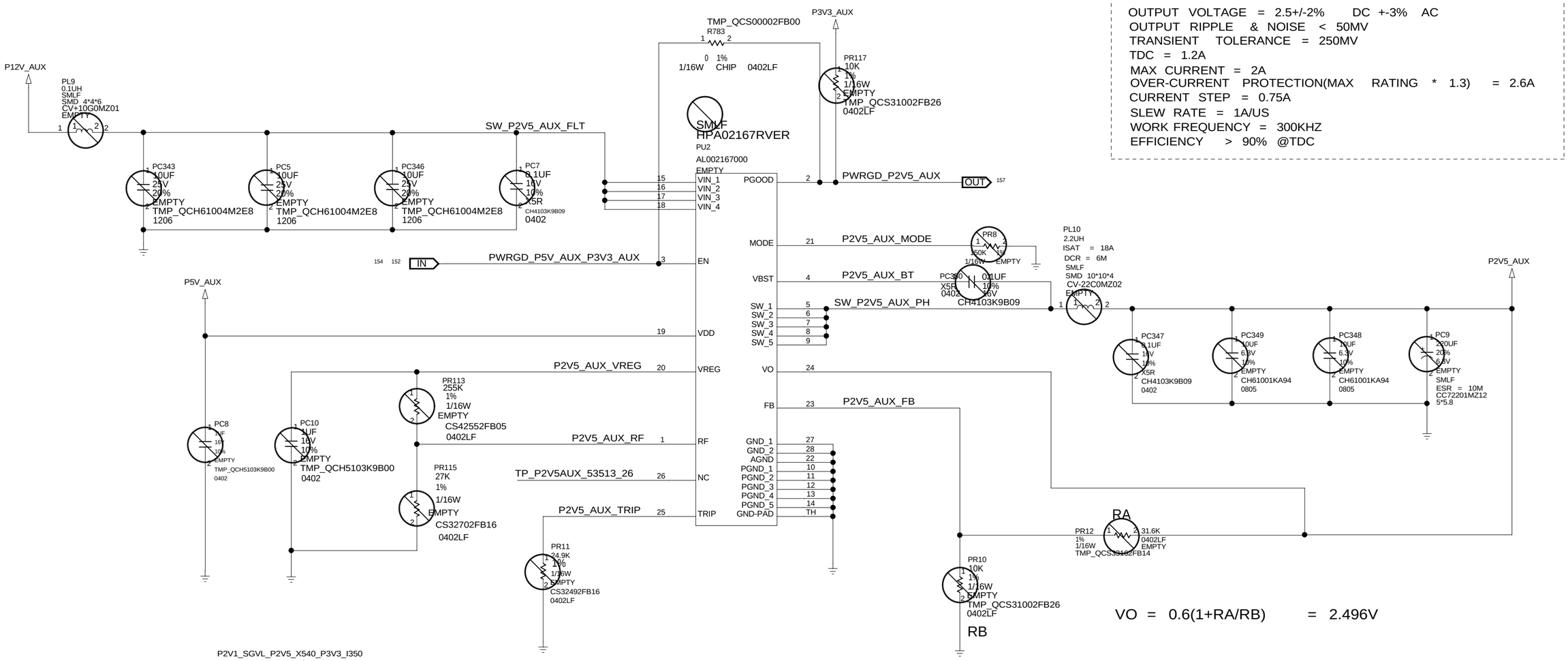
REV: 1




| | RA | VOUT |
|---|---|---|
| X540 | 1.15K | 0.669V |
| SAGEVILLE | 4.22K | 0.853V |
| I350 | EMPTY 0.67V VR | |

P0V67_X540_P1V0_I350

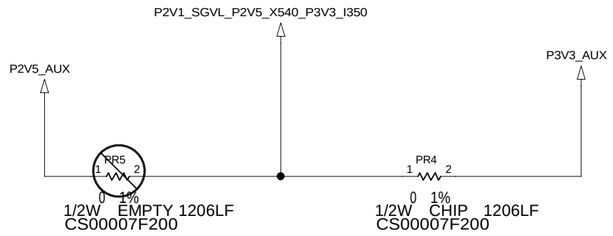
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: BEN CHIANG | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: NICK,PETER,MATT,KUOCHAN | SIZE: C DATE: Mon Nov 16 11:55:30 2015 | SHEET: 159 OF 188 | |

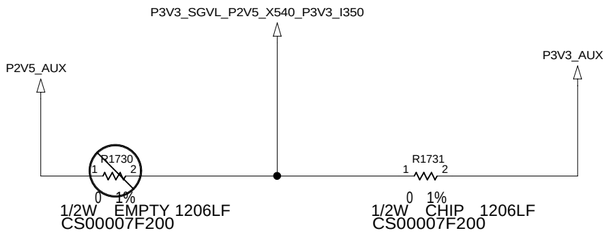



## DESIGN SPECIFICATION

OUTPUT VOLTAGE = 2.5+/-2% DC +-3% AC
OUTPUT RIPPLE & NOISE < 50MV
TRANSIENT TOLERANCE = 250MV
TDC = 1.2A
MAX CURRENT = 2A
OVER-CURRENT PROTECTION(MAX RATING * 1.3) = 2.6A
CURRENT STEP = 0.75A
SLEW RATE = 1A/US
WORK FREQUENCY = 300KHZ
EFFICIENCY > 90% @TDC

VO = 0.6(1+RA/RB) = 2.496V

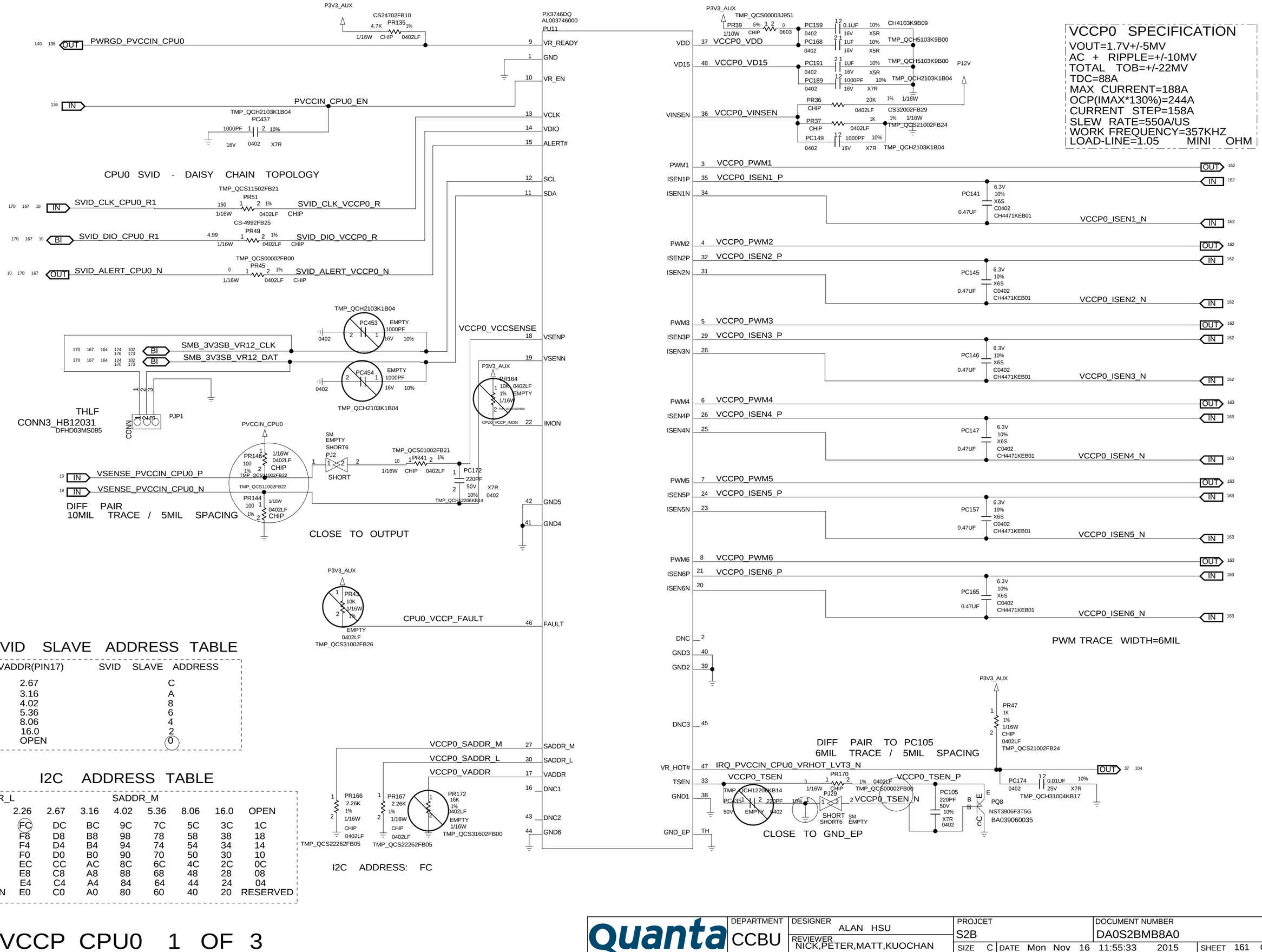



| | RA | VOUT |
|---|---|---|
| X540 | 31.6K | 2.496V |
| I350 | 45.3K | 3.318V |
| SAGEVILLE | 24.9K | 2.098V |

P2V5_AUX

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER BEN CHIANG | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER NICK,PETER,MATT,KUOCHAN | SIZE C | DATE Mon Nov 16 11:55:31 2015 | SHEET 160 OF 188 |

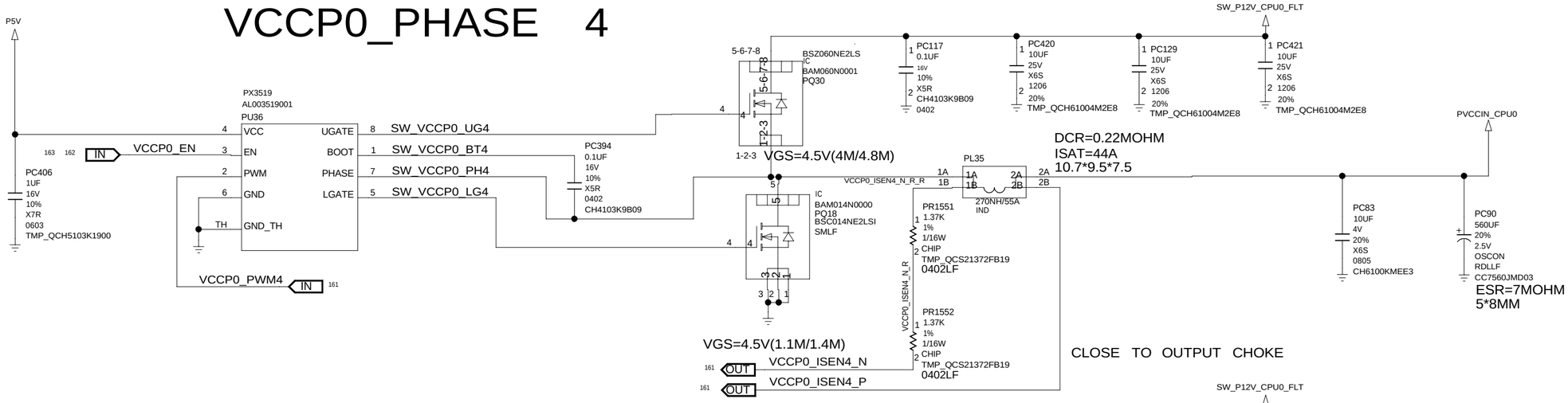



PV_VCCP_CPU0 1 OF 3

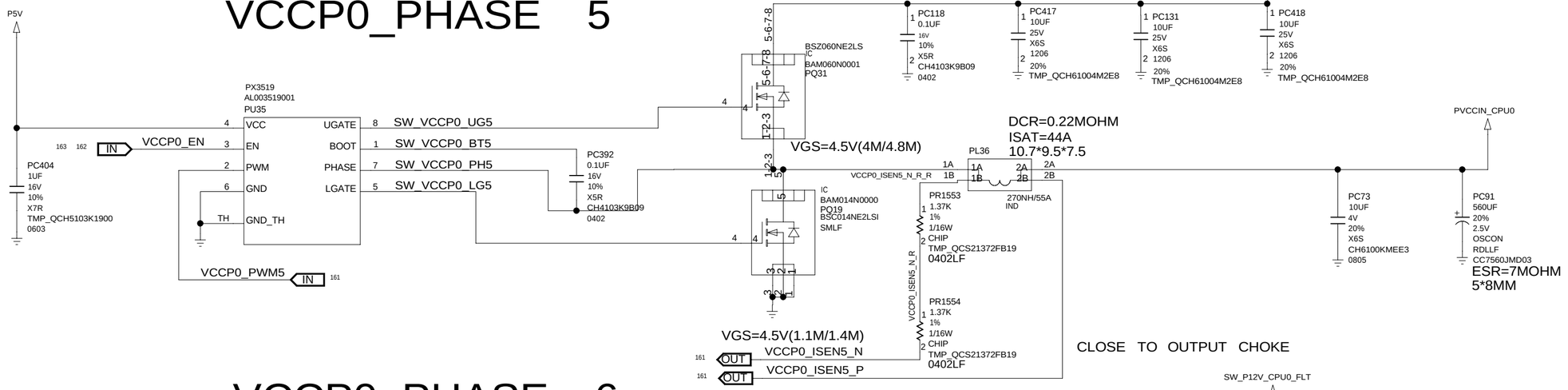
| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER ALAN HSU | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER NICK,PETER,MATT,KUOCHAN | SIZE C | DATE Mon Nov 16 11:55:33 2015 | SHEET 161 OF 188 | |

VCCP0_PHASE 1
P5V
PR148
2.26K
1%
1/16W
CHIP
0402LF
TMP_QCS22262FB05
PX3519
AL003519001
PU39
VCC
EN
PWM
GND
TH
GND_TH
UGATE
BOOT
PHASE
LGATE
SW_VCCP0_UG1
SW_VCCP0_BT1
SW_VCCP0_PH1
SW_VCCP0_LG1
VCCP0_EN
VCCP0_PWM1
OUT
IN
PC402
1UF
16V
10%
X7R
0603
TMP_QCH5103K1900
PC387
0.1UF
16V
10%
X5R
0402
CH4103K9B09
PR162
4.02K
1%
1/16W
CHIP
0402LF
TMP_QCS24022FB13
PC399
0.1UF
16V
10%
X5R
0402
CH4103K9B09
PQ27
BSZ060NE2LS
IC
BAM060N0001
PQ10
BSC014NE2LSI
SMLF
BAM014N0000
VGS=4.5V(4M/4.8M)
VGS=4.5V(1.1M/1.4M)
PC120
0.1UF
16V
10%
X5R
0402
CH4103K9B09
PC128
10UF
25V
20%
X6S
1206
TMP_QCH61004M2E8
PC415
10UF
25V
X6S
1206
20%
PC132
10UF
25V
X6S
1206
20%
PC163
270UF
16V
OSCON
RI=5A
8*8
TMP_QCC72703MD03
20%
PC155
270UF
16V
OSCON
RI=5A
8*8
TMP_QCC72703MD03
20%
PC162
270UF
16V
OSCON
RI=5A
8*8
TMP_QCC72703MD03
20%
SW_P12V_CPU0_FLT
P12V
PL39
CV+20^0MZ04
IND
0.2UH/35A
DCR=0.23MOHM
ISAT=35A
5.7*5.7*7.5
ISAT=44A
10.7*9.5*7.5
PL32
270NH/55A
IND
SP_CV+27^0KZ03
VCCP0_ISEN1_N_R_R
VCCP0_ISEN1_N_R
PR1545
1.37K
1%
1/16W
CHIP
TMP_QCS21372FB19
0402LF
PR1546
1.37K
1%
1/16W
CHIP
TMP_QCS21372FB19
0402LF
VCCP0_ISEN1_N
VCCP0_ISEN1_P
PVCCIN_CPU0
PC74
10UF
4V
20%
X6S
0805
CH6100KMEE3
PC92
560UF
20%
2.5V
OSCON
RDLLF
CC7560JMD03
ESR=7MOHM
5*8MM
CLOSE TO OUTPUT CHOKE
VCCP0_PHASE 2
PX3519
AL003519001
PU38
VCCP0_EN
VCCP0_PWM2
SW_VCCP0_UG2
SW_VCCP0_BT2
SW_VCCP0_PH2
SW_VCCP0_LG2
PC400
1UF
16V
10%
X7R
0603
TMP_QCH5103K1900
PC398
0.1UF
16V
10%
X5R
0402
CH4103K9B09
PQ28
BSZ060NE2LS
IC
BAM060N0001
PQ16
BSC014NE2LSI
SMLF
IC
BAM014N0000
VGS=4.5V(4M/4.8M)
VGS=4.5V(1.1M/1.4M)
PC116
0.1UF
16V
10%
X5R
0402
CH4103K9B09
PC423
10UF
25V
20%
X6S
1206
TMP_QCH61004M2E8
PC133
10UF
25V
20%
X6S
1206
TMP_QCH61004M2E8
PC138
10UF
25V
20%
X6S
1206
TMP_QCH61004M2E8
DCR=0.22MOHM
ISAT=44A
10.7*9.5*7.5
PL33
270NH/55A
IND
SP_CV+27^0KZ03
VCCP0_ISEN2_N_R_R
VCCP0_ISEN2_N_R
PR1549
1.37K
1%
1/16W
CHIP
TMP_QCS21372FB19
0402LF
PR1550
1.37K
1%
1/16W
CHIP
TMP_QCS21372FB19
0402LF
VCCP0_ISEN2_N
VCCP0_ISEN2_P
PVCCIN_CPU0
PC75
10UF
4V
20%
X6S
0805
CH6100KMEE3
PC95
560UF
20%
2.5V
OSCON
RDLLF
CC7560JMD03
ESR=7MOHM
5*8MM
CLOSE TO OUTPUT CHOKE
VCCP0_PHASE 3
PX3519
AL003519001
PU37
VCCP0_EN
VCCP0_PWM3
SW_VCCP0_UG3
SW_VCCP0_BT3
SW_VCCP0_PH3
SW_VCCP0_LG3
PC412
1UF
16V
10%
X7R
0603
TMP_QCH5103K1900
PC396
0.1UF
16V
10%
X5R
0402
CH4103K9B09
BSZ060NE2LS
IC
BAM060N0001
PQ29
IC
BAM014N0000
PQ17
BSC014NE2LSI
SMLF
VGS=4.5V(4M/4.8M)
VGS=4.5V(1.1M/1.4M)
PC121
0.1UF
16V
10%
X5R
0402
CH4103K9B09
PC414
10UF
25V
20%
X6S
1206
TMP_QCH61004M2E8
PC422
10UF
25V
X6S
20%
1206
TMP_QCH61004M2E8
PC413
10UF
25V
20%
X6S
1206
TMP_QCH61004M2E8
DCR=0.22MOHM
ISAT=44A
10.7*9.5*7.5
PL34
270NH/55A
IND
VCCP0_ISEN3_N_R_R
VCCP0_ISEN3_N_R
PR1547
1.37K
1%
1/16W
CHIP
TMP_QCS21372FB19
0402LF
PR1548
1.37K
1%
1/16W
CHIP
TMP_QCS21372FB19
0402LF
VCCP0_ISEN3_N
VCCP0_ISEN3_P
PVCCIN_CPU0
PC76
10UF
4V
20%
X6S
0805
CH6100KMEE3
PC93
560UF
20%
2.5V
OSCON
RDLLF
CC7560JMD03
ESR=7MOHM
5*8MM
CLOSE TO OUTPUT CHOKE
PV_VCCP_CPU0 2 OF 3
Quanta
DEPARTMENT
CCBU
DESIGNER
ALAN HSU
REVIEWER
NICK,PETER,MATT,KUOCHAN
PROJCET
S2B
DOCUMENT NUMBER
DA0S2BMB8A0
REV
1
SIZE C
DATE Mon Nov 16 11:55:35 2015
SHEET 162 OF 188

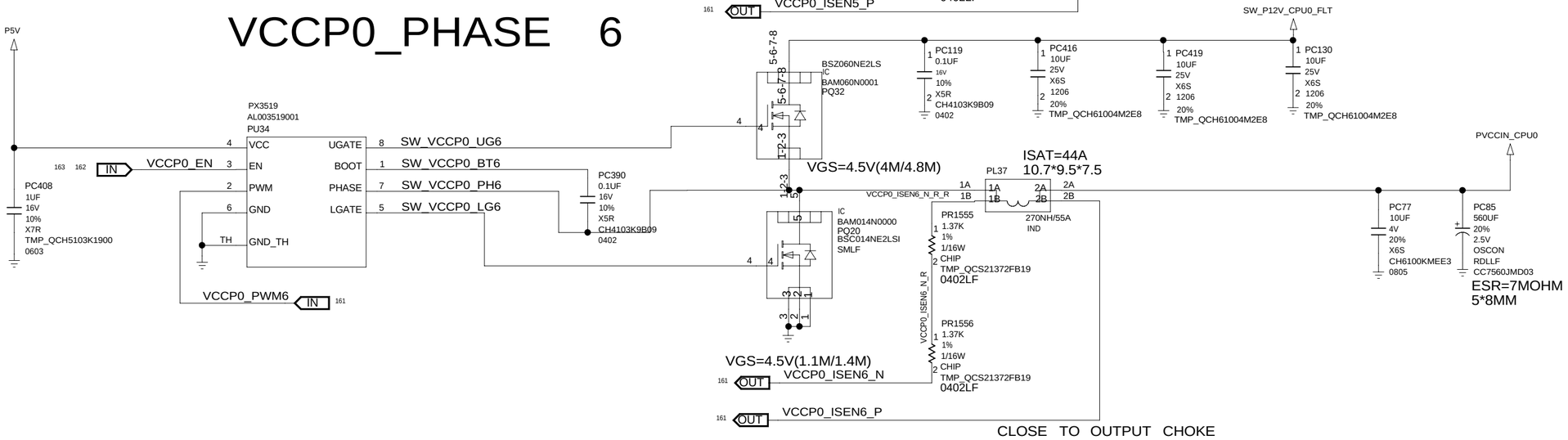
# VCCP0_PHASE 4




# VCCP0_PHASE 5

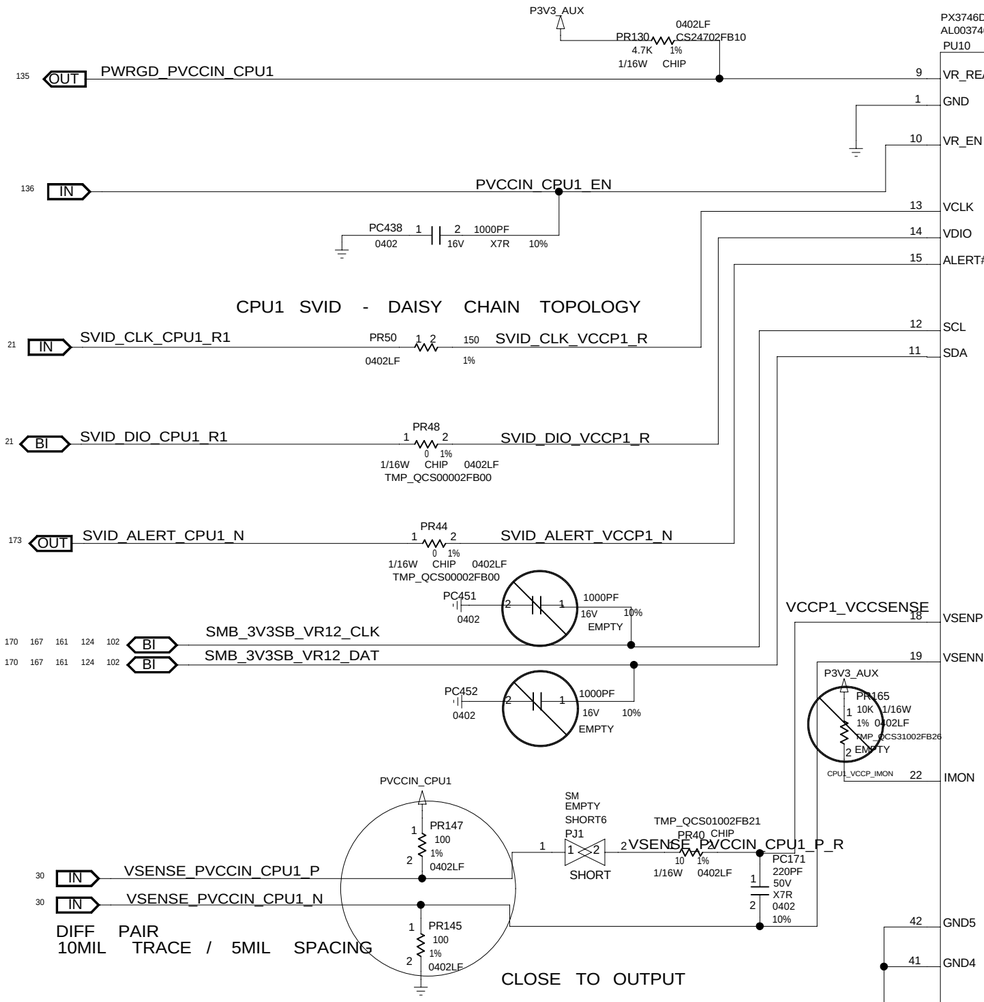



# VCCP0_PHASE 6




PV_VCCP_CPU0 3 0F 3

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER ALAN HSU | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER NICK,PETER,MATT,KUOCHAN | SIZE C | DATE Mon Nov 16 11:55:36 2015 | SHEET 163 OF 188 |




## VCCP1 SPECIFICATION

VOUT=1.7V+/-5MV
AC + RIPPLE=+/-10MV
TOTAL TOB=+/-22MV
TDC=88A
MAX CURRENT=188A
OCP(IMAX*130%)=244A
CURRENT STEP=158A
SLEW RATE=550A/US
WORK FREQUENCY=357KHZ
LOAD-LINE=1.05 MINI OHM

## SVID SLAVE ADDRESS TABLE

| VADDR(PIN17) | SVID SLAVE ADDRESS |
|---|---|
| 2.67 | C |
| 3.16 | A |
| 4.02 | 8 |
| 5.36 | 6 |
| 8.06 | 4 |
| 16.0 | 2 |
| OPEN | 0 |

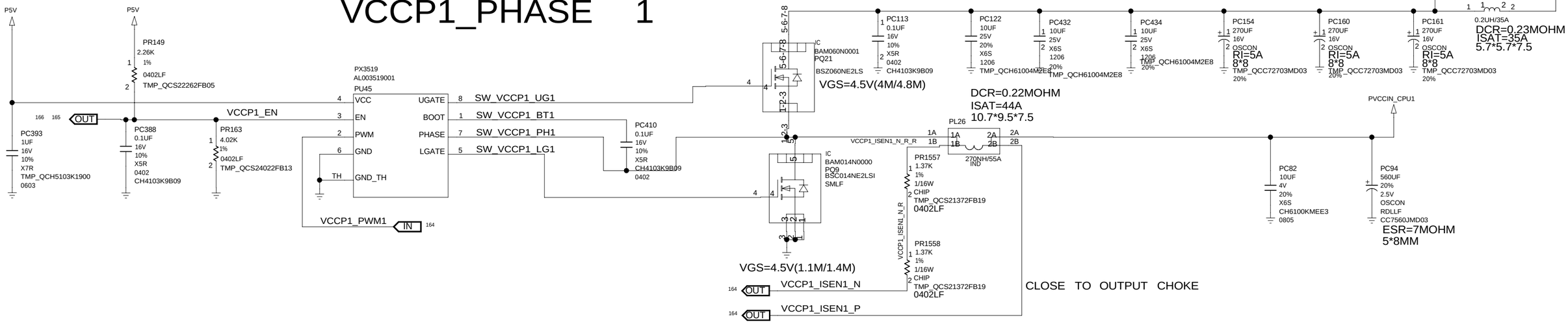
## I2C ADDRESS TABLE

| SADDR_L \ SADDR_M | 2.26 | 2.67 | 3.16 | 4.02 | 5.36 | 8.06 | 16.0 | OPEN |
|---|---|---|---|---|---|---|---|---|
| 2.26 | FC | DC | BC | 9C | 7C | 5C | 3C | 1C |
| 2.67 | F8 | D8 | B8 | 98 | 78 | 58 | 38 | 18 |
| 3.16 | F4 | D4 | B4 | 94 | 74 | 54 | 34 | 14 |
| 4.02 | F0 | D0 | B0 | 90 | 70 | 50 | 30 | 10 |
| 5.36 | EC | CC | AC | 8C | 6C | 4C | 2C | 0C |
| 8.06 | E8 | C8 | A8 | 88 | 68 | 48 | 28 | 08 |
| 16.0 | E4 | C4 | A4 | 84 | 64 | 44 | 24 | 04 |
| OPEN | E0 | C0 | A0 | 80 | 60 | 40 | 20 | RESERVED |

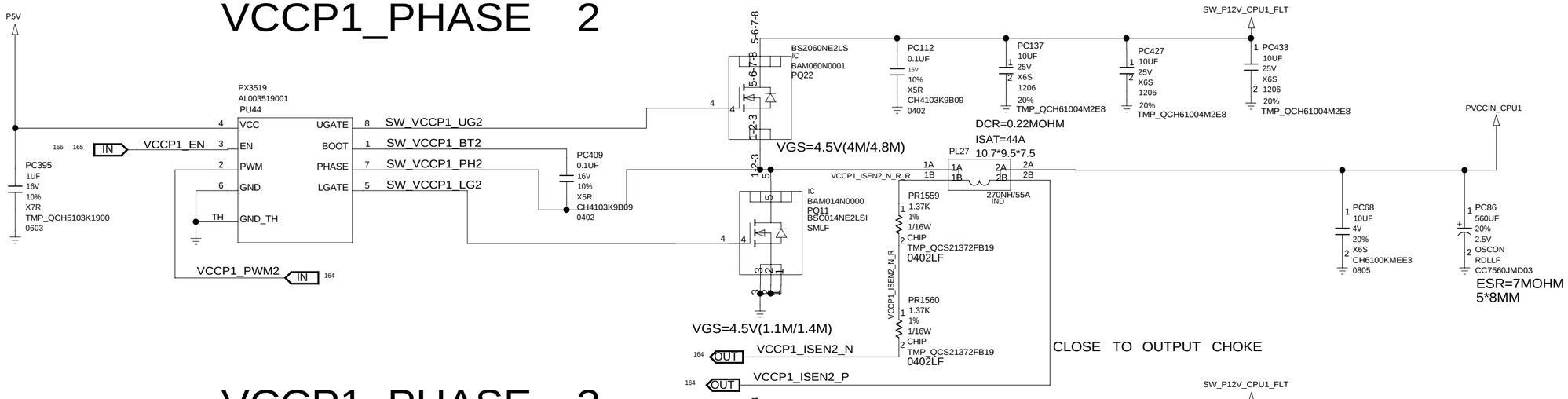
# PV_VCCP_CPU1 1 OF 3

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER ALAN HSU | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER NICK,PETER,MATT,KUOCHAN | SIZE C DATE Mon Nov 16 11:55:38 2015 | SHEET 164 OF 188 | |

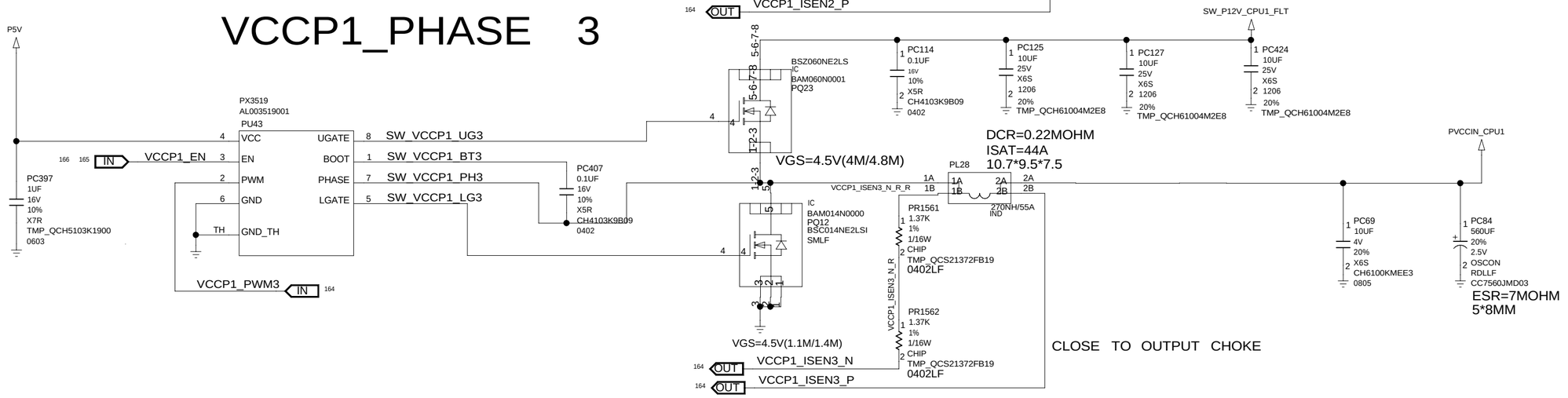
# VCCP1_PHASE 1




# VCCP1_PHASE 2

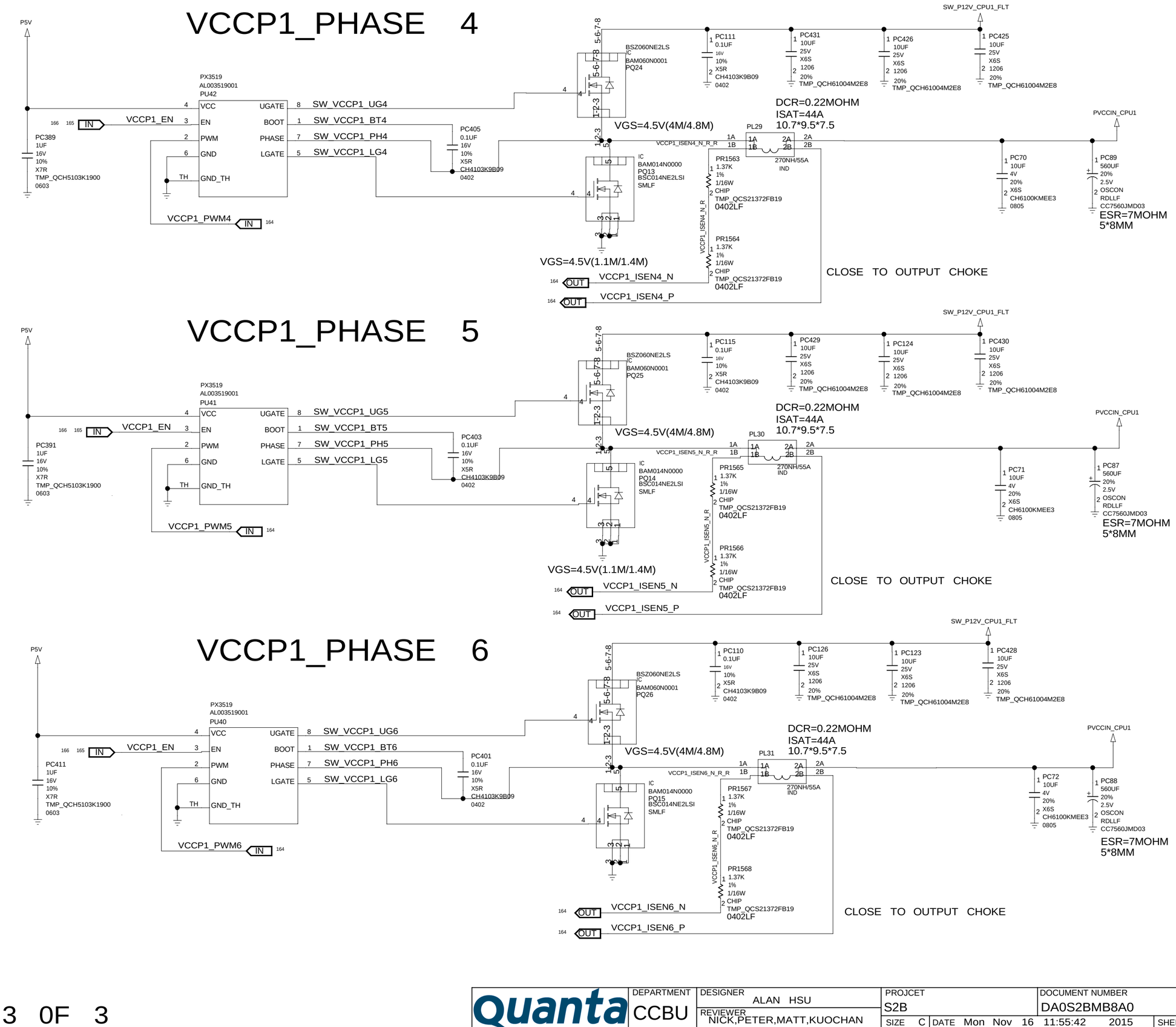



# VCCP1_PHASE 3



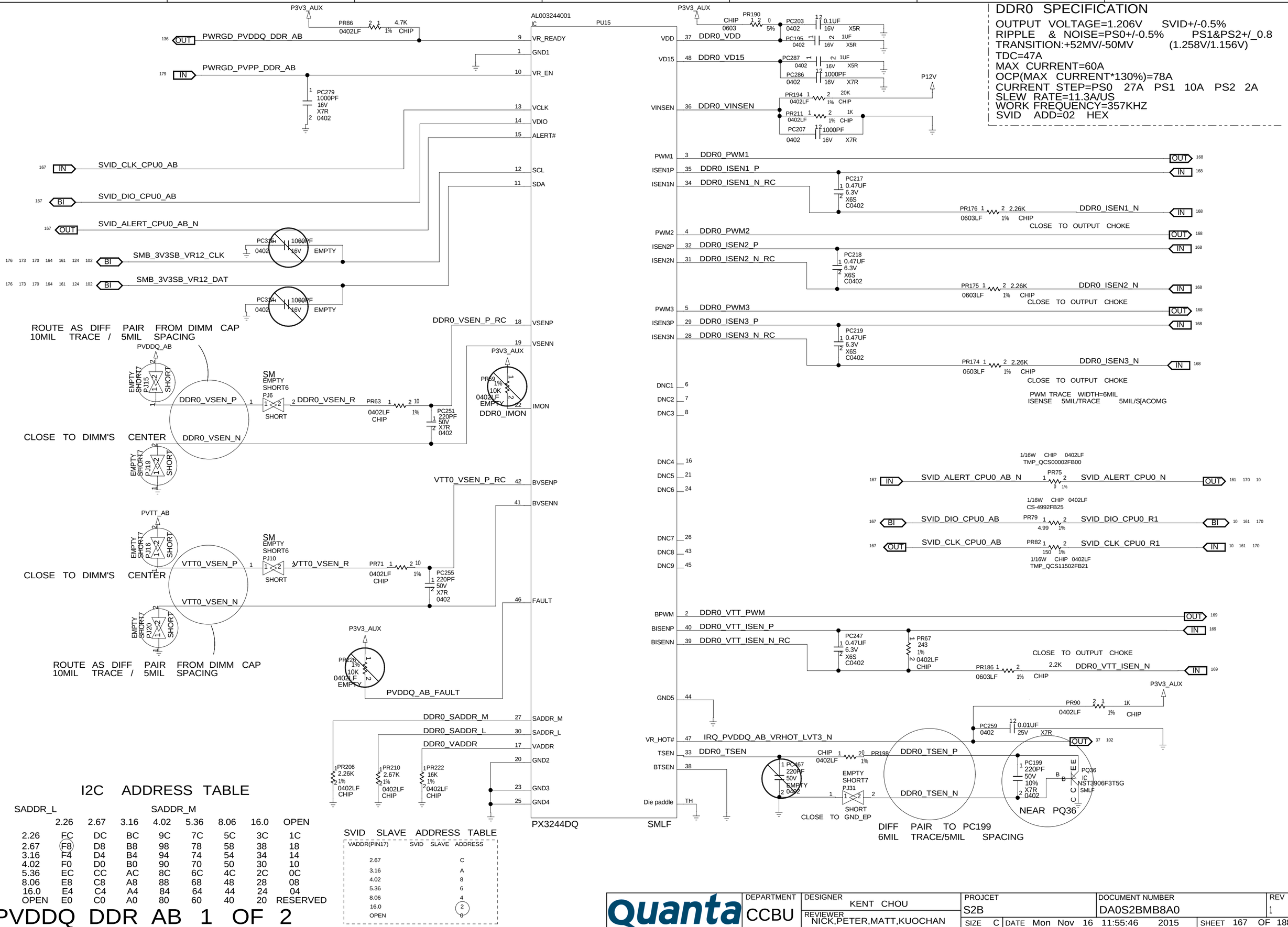

PV_VCCP_CPU1 2 OF 3

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: ALAN HSU | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: NICK,PETER,MATT,KUOCHAN | SIZE: C DATE: Mon Nov 16 11:55:41 2015 | SHEET: 165 OF 188 | |




# PV_VCCP_CPU1 3 0F 3

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: ALAN HSU | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: NICK,PETER,MATT,KUOCHAN | SIZE: C DATE: Mon Nov 16 11:55:42 2015 | SHEET: 166 OF 188 | |




## I2C ADDRESS TABLE

| SADDR_L \ SADDR_M | 2.26 | 2.67 | 3.16 | 4.02 | 5.36 | 8.06 | 16.0 | OPEN |
|---|---|---|---|---|---|---|---|---|
| 2.26 | FC | DC | BC | 9C | 7C | 5C | 3C | 1C |
| 2.67 | F8 | D8 | B8 | 98 | 78 | 58 | 38 | 18 |
| 3.16 | F4 | D4 | B4 | 94 | 74 | 54 | 34 | 14 |
| 4.02 | F0 | D0 | B0 | 90 | 70 | 50 | 30 | 10 |
| 5.36 | EC | CC | AC | 8C | 6C | 4C | 2C | 0C |
| 8.06 | E8 | C8 | A8 | 88 | 68 | 48 | 28 | 08 |
| 16.0 | E4 | C4 | A4 | 84 | 64 | 44 | 24 | 04 |
| OPEN | E0 | C0 | A0 | 80 | 60 | 40 | 20 | RESERVED |

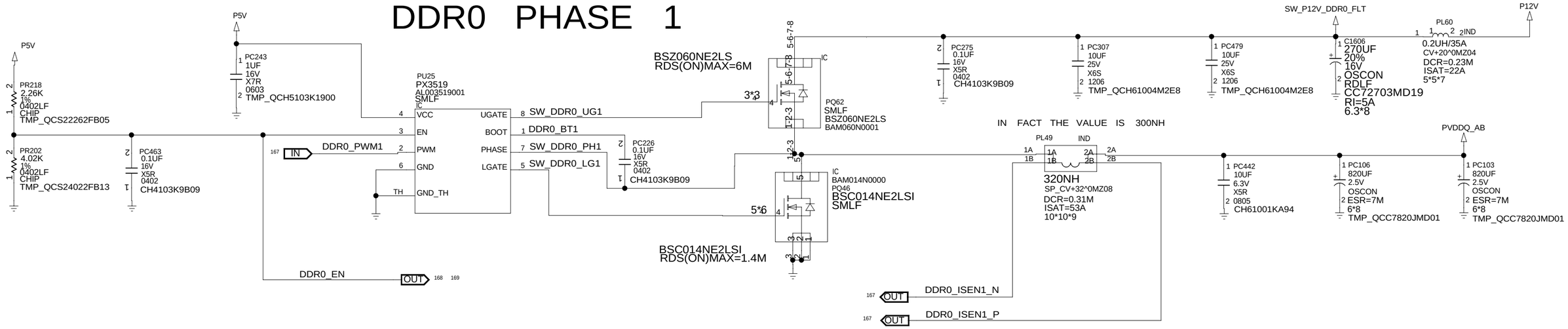
## SVID SLAVE ADDRESS TABLE

| VADDR(PIN17) | SVID SLAVE ADDRESS |
|---|---|
| 2.67 | C |
| 3.16 | A |
| 4.02 | 8 |
| 5.36 | 6 |
| 8.06 | 4 |
| 16.0 | 2 |
| OPEN | 0 |

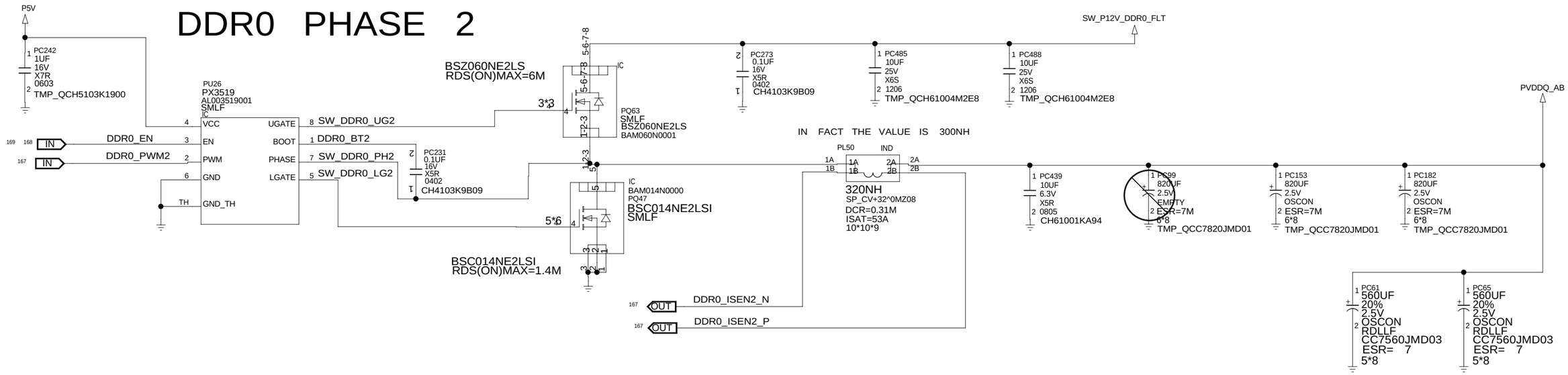
# PVDDQ_DDR_AB 1 OF 2

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER KENT CHOU | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER NICK,PETER,MATT,KUOCHAN | SIZE C | DATE Mon Nov 16 11:55:46 2015 | SHEET 167 OF 188 |

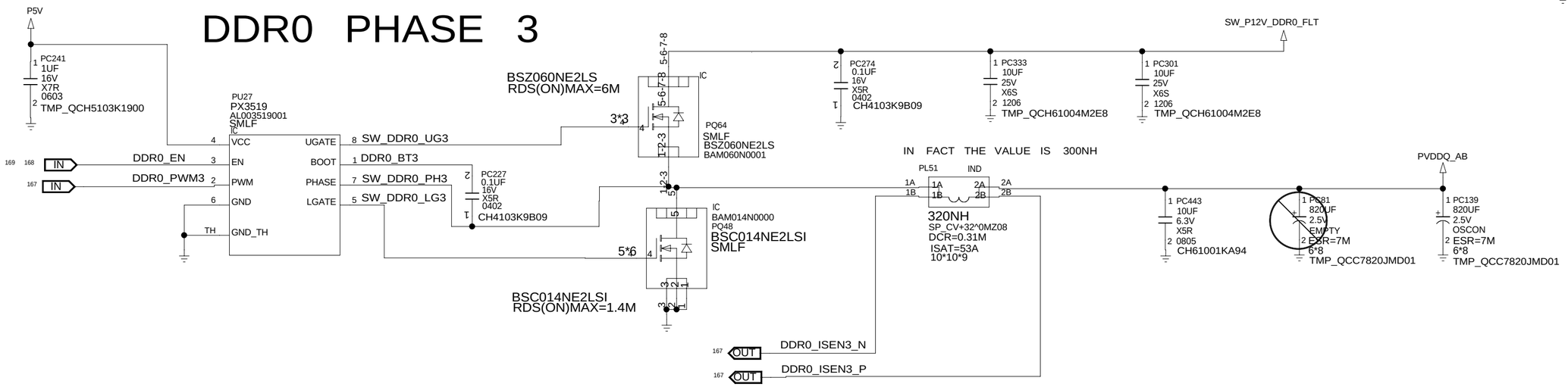
# DDR0 PHASE 1




# DDR0 PHASE 2




# DDR0 PHASE 3




PVDDQ_DDR_AB 2 OF 2

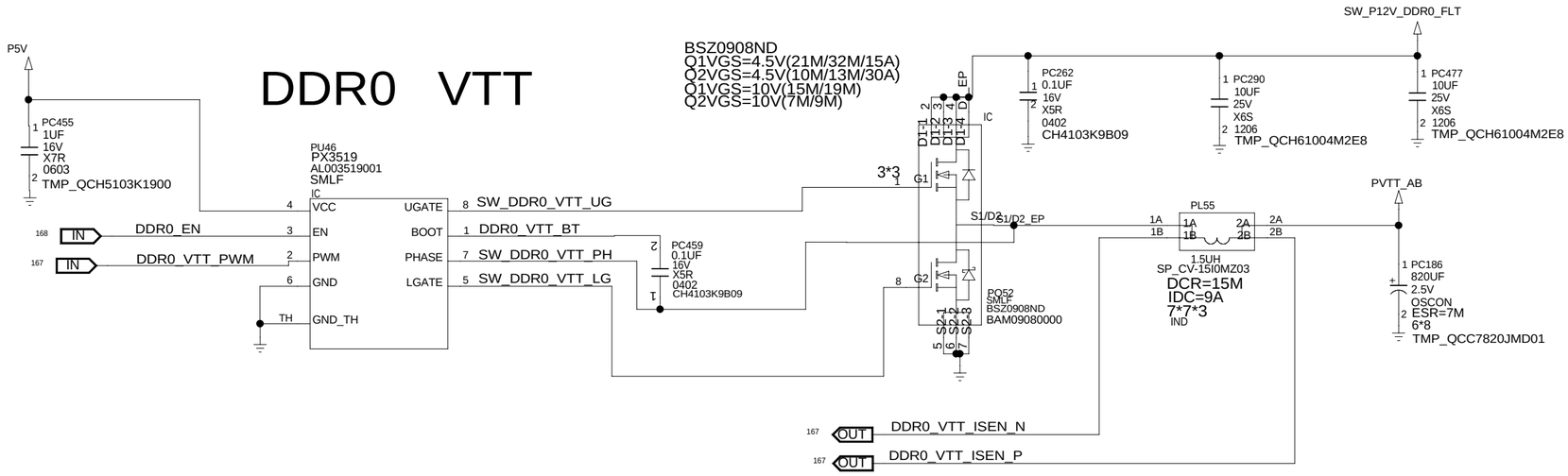
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: KENT CHOU | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: NICK,PETER,MATT,KUOCHAN | SIZE: C DATE: Mon Nov 16 11:55:48 2015 | SHEET: 168 OF 188 | |

# DDR0 VTT

## DDR0_VTT SPECIFICATION

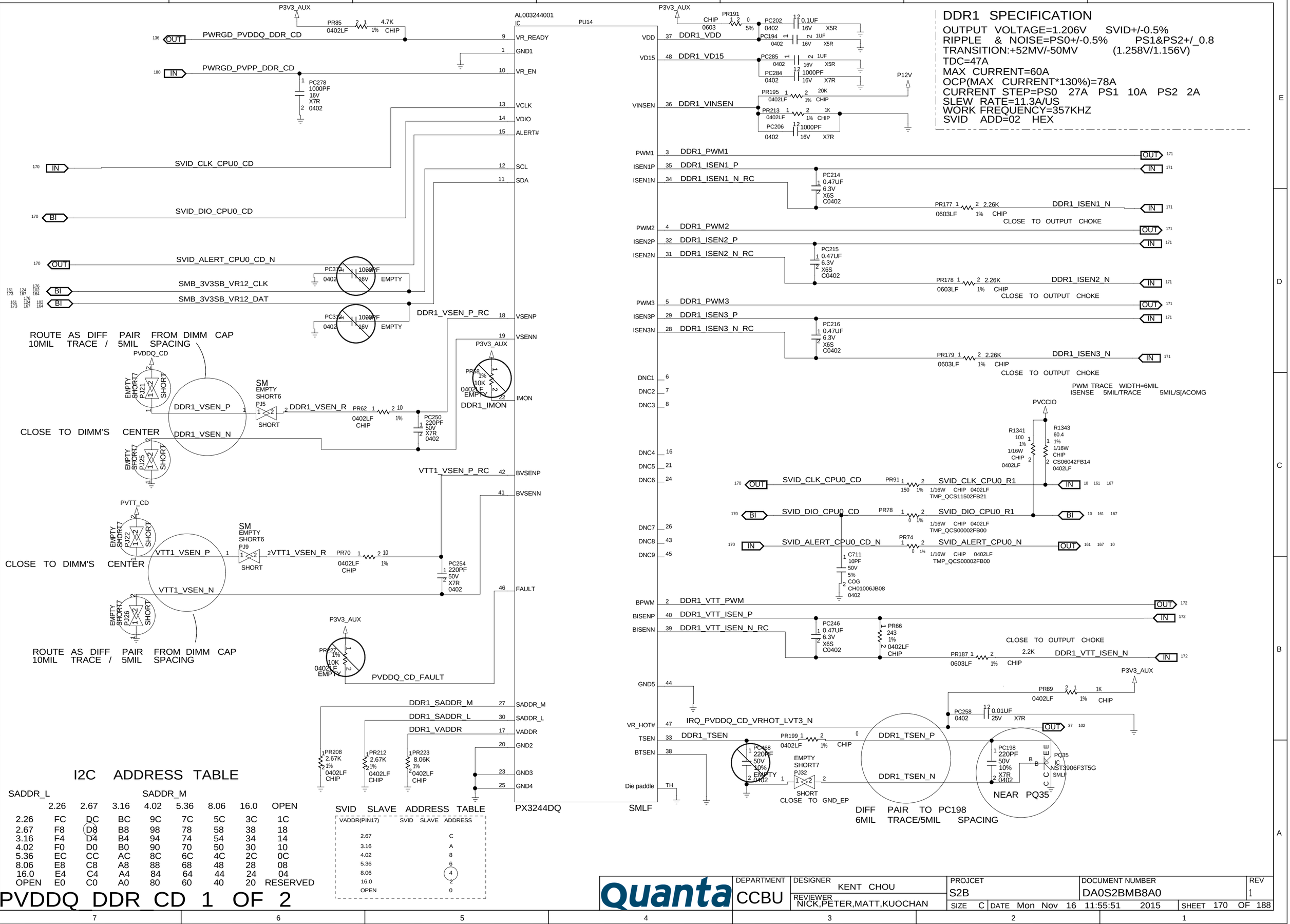
VOUT=1/2 VDDQ+/-1.5%
RIPPLE & NOISE=+/-1%
AC_LL=1/2VDDQ+/-57MV
TDC=+/-3.3A (FOR LRDIMM)
MAX CURRENT=+/-3.6A (FOR LRDIMM)
OCP(MAX CURRENT*130%)=+/-4.68A
CURRENT STEP=0.25A
SLEW RATE=3A/US

BSZ0908ND
Q1VGS=4.5V(21M/32M/15A)
Q2VGS=4.5V(10M/13M/30A)
Q1VGS=10V(15M/19M)
Q2VGS=10V(7M/9M)



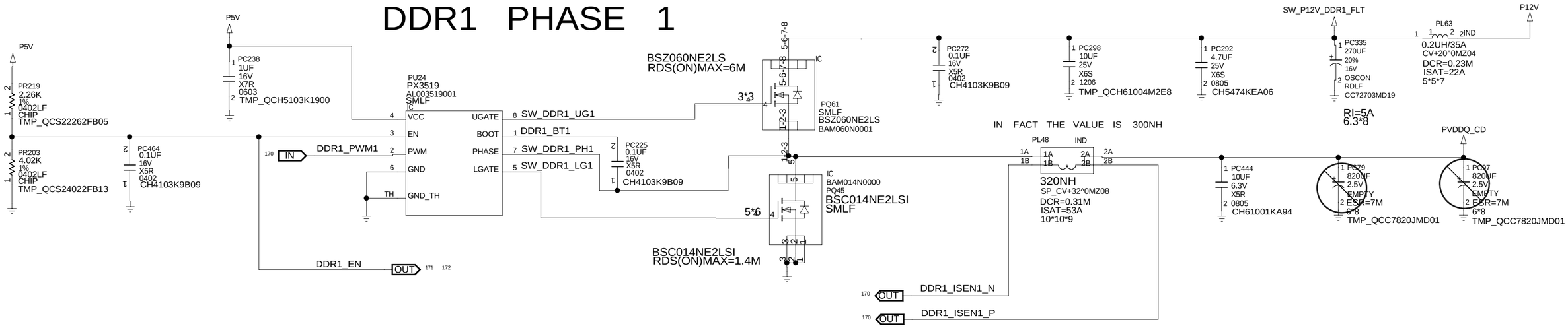

PVTT_DDR_AB

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: KENT CHOU | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: NICK,PETER,MATT,KUOCHAN | SIZE C | DATE Mon Nov 16 11:55:50 2015 | SHEET 169 OF 188 | |

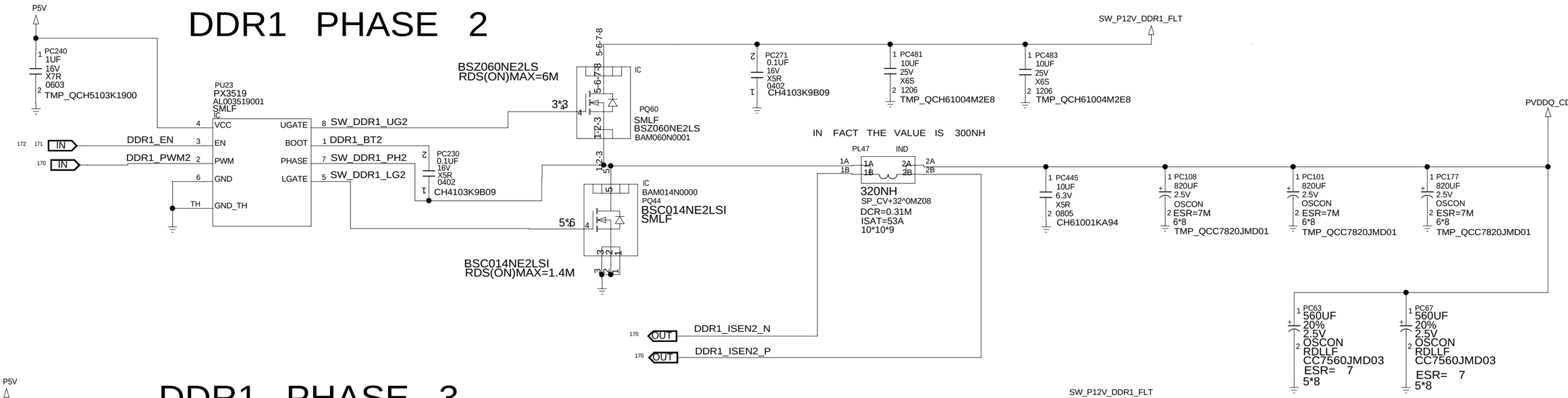



| Quanta | DEPARTMENT | DESIGNER | PROJCET | DOCUMENT NUMBER | REV |
|---|---|---|---|---|---|
| | CCBU | KENT CHOU | S2B | DA0S2BMB8A0 | 1 |
| | | REVIEWER NICK,PETER,MATT,KUOCHAN | SIZE C DATE Mon Nov 16 11:55:51 2015 | SHEET 170 OF 188 | |

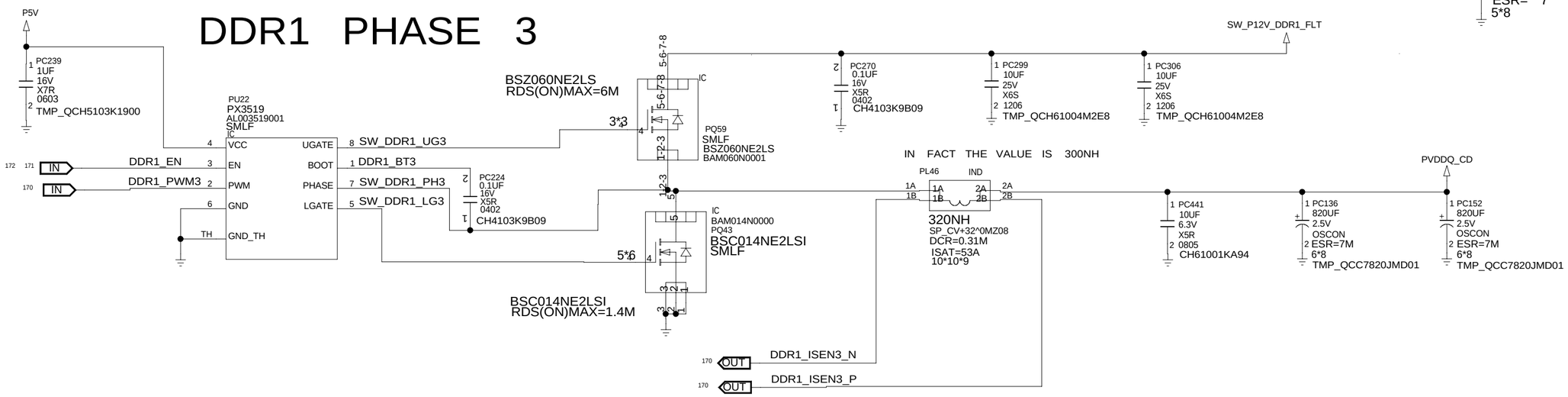
# DDR1 PHASE 1




# DDR1 PHASE 2




# DDR1 PHASE 3




PVDDQ_DDR_CD 2 OF 2

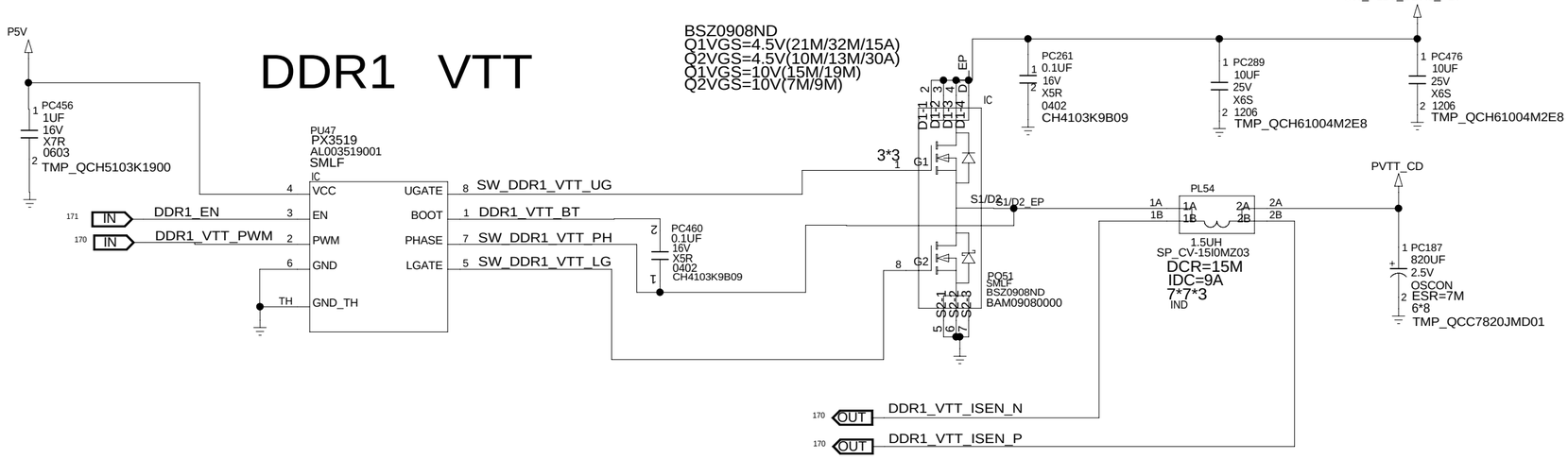
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER KENT CHOU | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER NICK,PETER,MATT,KUOCHAN | SIZE C | DATE Mon Nov 16 11:55:54 2015 | SHEET 171 OF 188 |

# DDR1_VTT SPECIFICATION

VOUT=1/2 VDDQ+/-1.5%
RIPPLE & NOISE=+/-1%
AC_LL=1/2VDDQ+/-57MV
TDC=+/-3.3A (FOR LRDIMM)
MAX CURRENT=+/-3.6A (FOR LRDIMM)
OCP(MAX CURRENT*130%)=+/-4.68A
CURRENT STEP=0.25A
SLEW RATE=3A/US

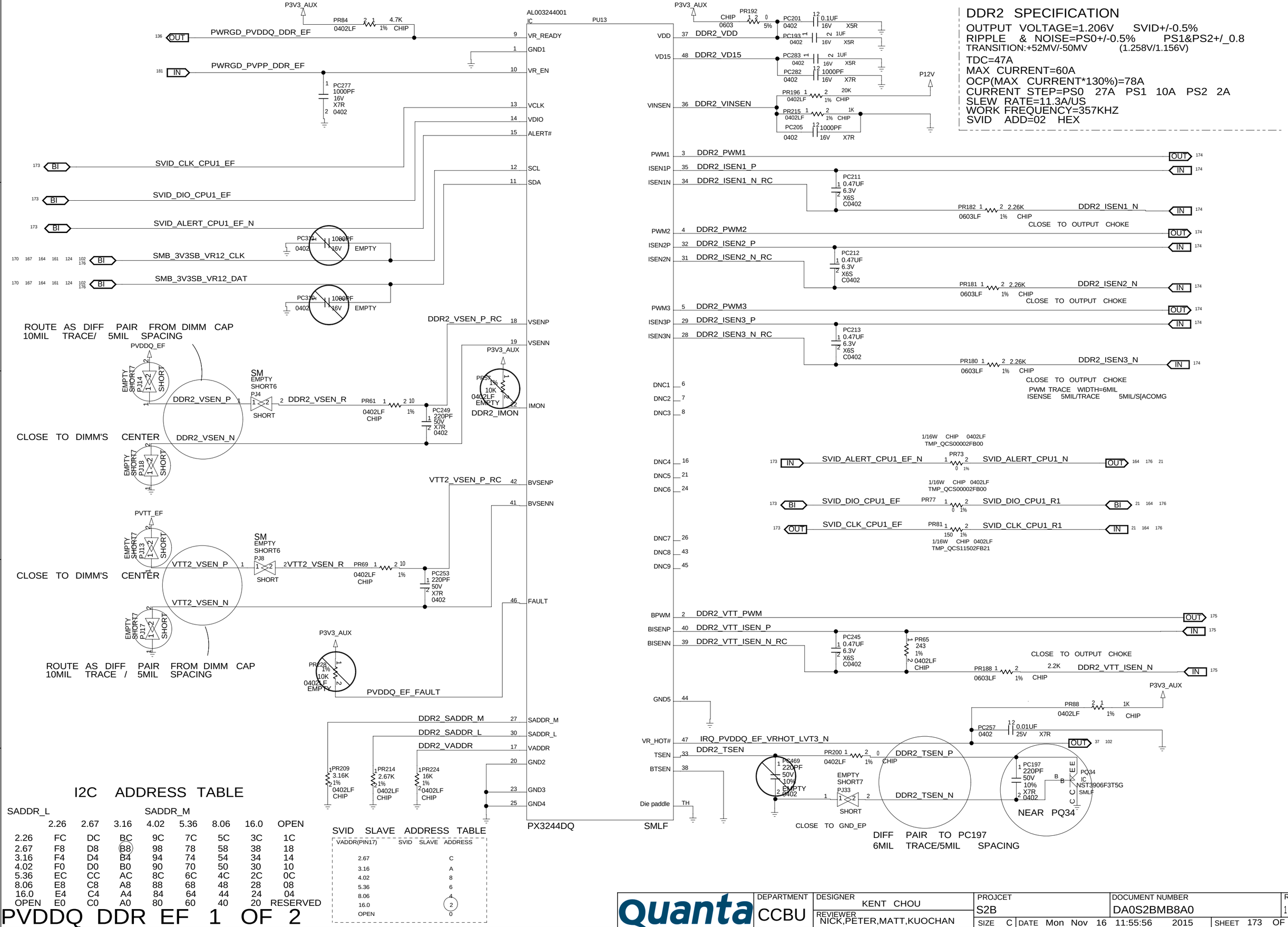
# DDR1 VTT

BSZ0908ND
Q1VGS=4.5V(21M/32M/15A)
Q2VGS=4.5V(10M/13M/30A)
Q1VGS=10V(15M/19M)
Q2VGS=10V(7M/9M)




PVTT_DDR_CD

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: KENT CHOU | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: NICK,PETER,MATT,KUOCHAN | SIZE: C | DATE: Mon Nov 16 11:55:56 2015 | SHEET: 172 OF 188 | |




## DDR2 SPECIFICATION

OUTPUT VOLTAGE=1.206V SVID+/-0.5%
RIPPLE & NOISE=PS0+/-0.5% PS1&PS2+/_0.8
TRANSITION:+52MV/-50MV (1.258V/1.156V)
TDC=47A
MAX CURRENT=60A
OCP(MAX CURRENT*130%)=78A
CURRENT STEP=PS0 27A PS1 10A PS2 2A
SLEW RATE=11.3A/US
WORK FREQUENCY=357KHZ
SVID ADD=02 HEX

## I2C ADDRESS TABLE

| SADDR_L \ SADDR_M | 2.26 | 2.67 | 3.16 | 4.02 | 5.36 | 8.06 | 16.0 | OPEN |
|---|---|---|---|---|---|---|---|---|
| 2.26 | FC | DC | BC | 9C | 7C | 5C | 3C | 1C |
| 2.67 | F8 | D8 | B8 | 98 | 78 | 58 | 38 | 18 |
| 3.16 | F4 | D4 | B4 | 94 | 74 | 54 | 34 | 14 |
| 4.02 | F0 | D0 | B0 | 90 | 70 | 50 | 30 | 10 |
| 5.36 | EC | CC | AC | 8C | 6C | 4C | 2C | 0C |
| 8.06 | E8 | C8 | A8 | 88 | 68 | 48 | 28 | 08 |
| 16.0 | E4 | C4 | A4 | 84 | 64 | 44 | 24 | 04 |
| OPEN | E0 | C0 | A0 | 80 | 60 | 40 | 20 | RESERVED |

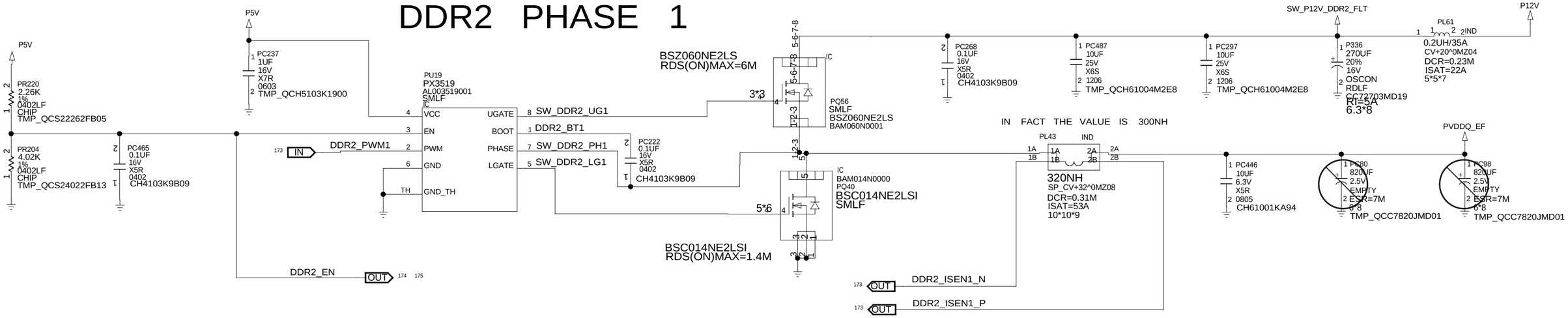
## SVID SLAVE ADDRESS TABLE

| VADDR(PIN17) | SVID SLAVE ADDRESS |
|---|---|
| 2.67 | C |
| 3.16 | A |
| 4.02 | 8 |
| 5.36 | 6 |
| 8.06 | 4 |
| 16.0 | 2 |
| OPEN | 0 |

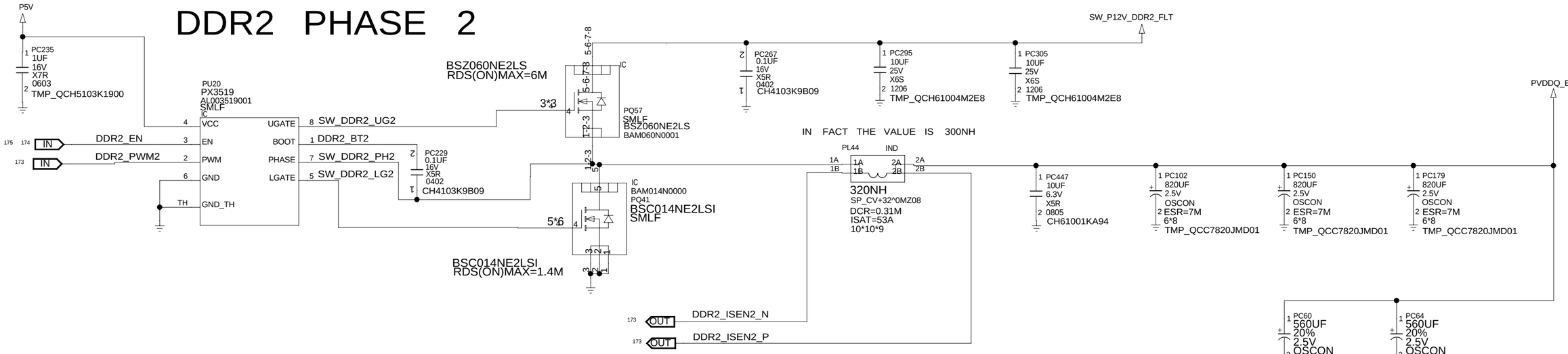
PVDDQ_DDR_EF 1 OF 2

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER KENT CHOU | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER NICK,PETER,MATT,KUOCHAN | SIZE C | DATE Mon Nov 16 11:55:56 2015 | SHEET 173 OF 188 | |

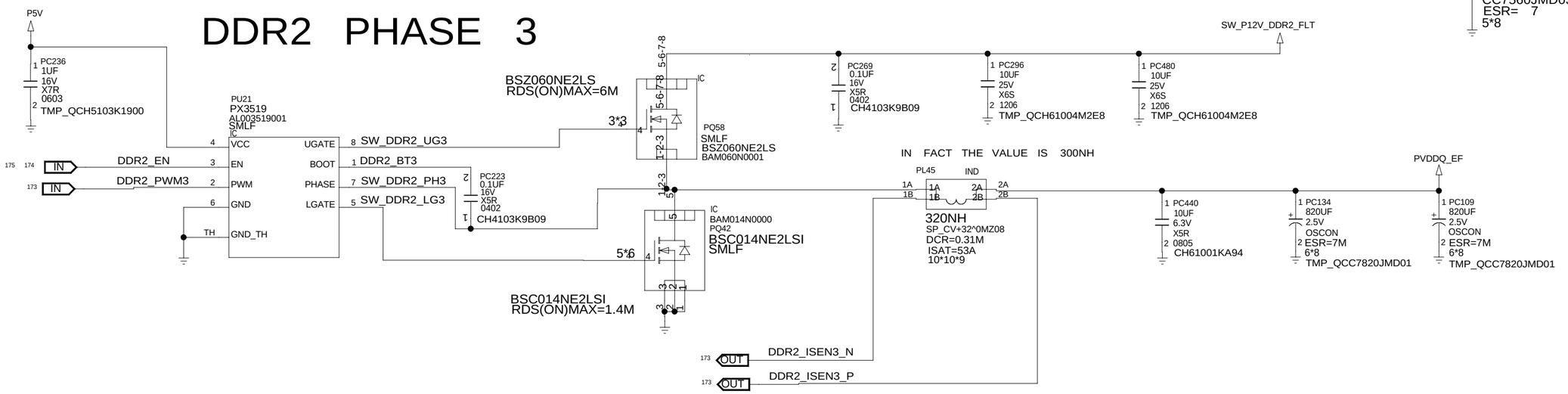
# DDR2 PHASE 1




# DDR2 PHASE 2




# DDR2 PHASE 3




# PVDDQ_DDR_EF 2 OF 2

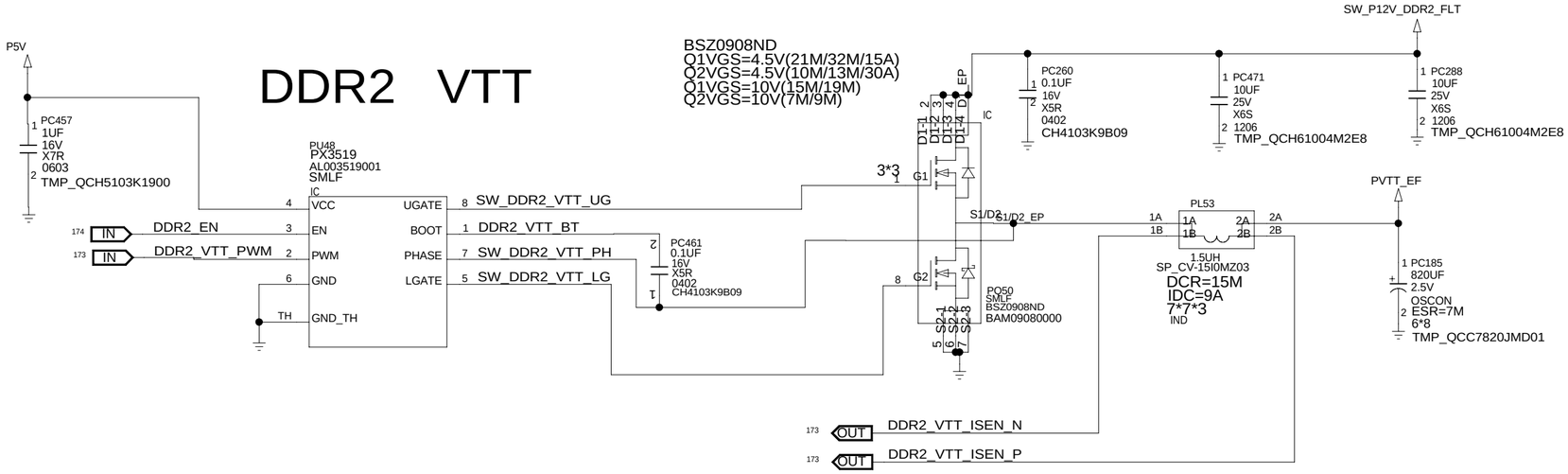
| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: KENT CHOU | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: NICK,PETER,MATT,KUOCHAN | SIZE: C | DATE: Mon Nov 16 11:55:58 2015 | SHEET: 174 OF 188 |

# DDR2_VTT SPECIFICATION

VOUT=1/2 VDDQ+/-1.5%
RIPPLE & NOISE=+/-1%
AC_LL=1/2VDDQ+/-57MV
TDC=+/-3.3A (FOR LRDIMM)
MAX CURRENT=+/-3.6A (FOR LRDIMM)
OCP(MAX CURRENT*130%)=+/-4.68A
CURRENT STEP=0.25A
SLEW RATE=3A/US

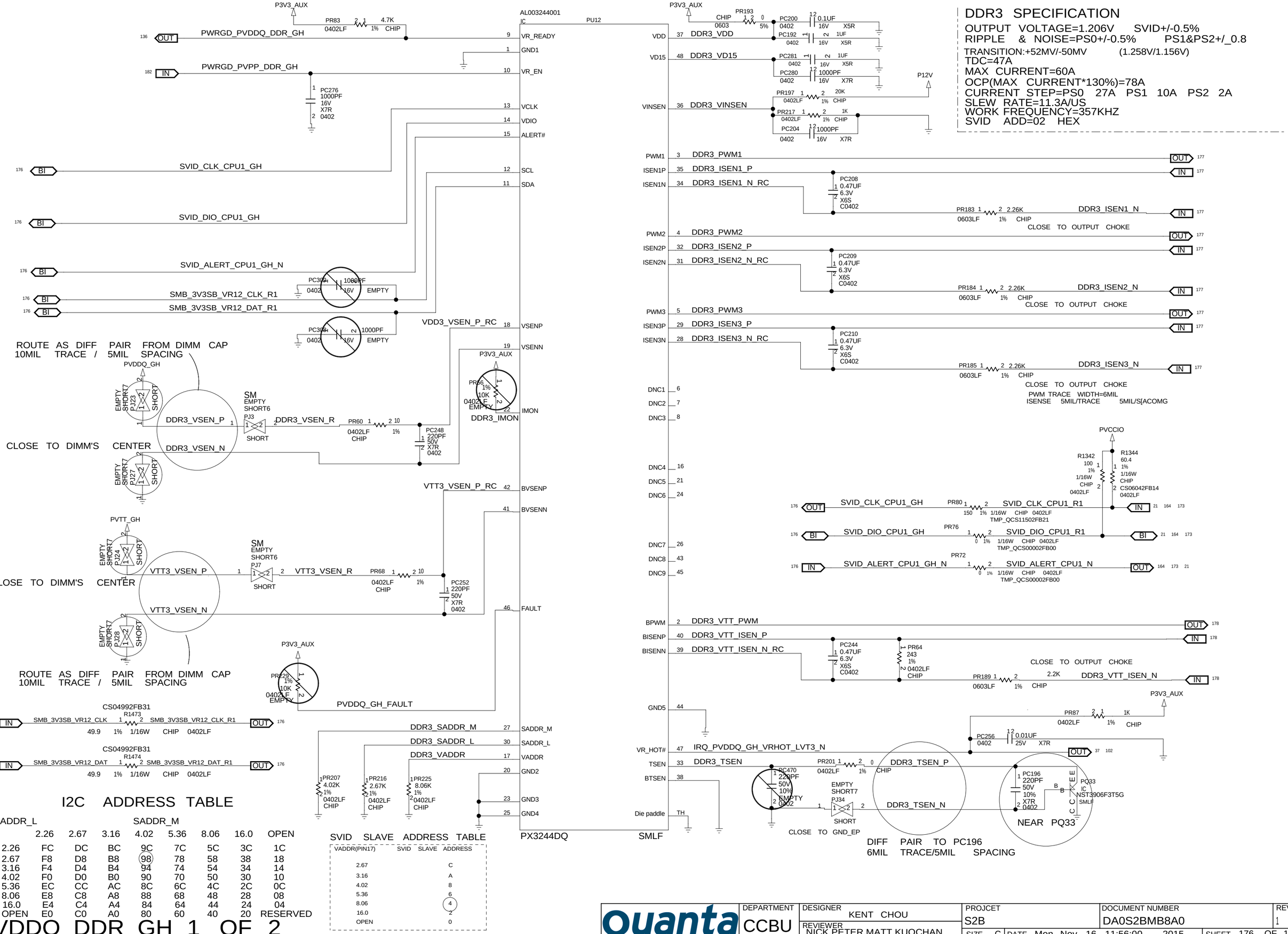
# DDR2 VTT

BSZ0908ND
Q1VGS=4.5V(21M/32M/15A)
Q2VGS=4.5V(10M/13M/30A)
Q1VGS=10V(15M/19M)
Q2VGS=10V(7M/9M)




PVTT_DDR_EF

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER KENT CHOU | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER NICK,PETER,MATT,KUOCHAN | SIZE C | DATE Mon Nov 16 11:56:00 2015 | SHEET 175 OF 188 | |




| | | | |
|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: KENT CHOU | PROJCET: S2B |
| | | REVIEWER: NICK,PETER,MATT,KUOCHAN | DOCUMENT NUMBER: DA0S2BMB8A0 |
| | | SIZE: C DATE: Mon Nov 16 11:56:00 2015 | REV: 1 SHEET: 176 OF 188 |

# DDR3 PHASE 1

P5V
PR221 2.26K 1% 0402LF CHIP TMP_QCS22262FB05
PR205 4.02K 1% 0402LF CHIP TMP_QCS24022FB13
PC466 0.1UF 16V X5R 0402 CH4103K9B09
PC232 1UF 16V X7R 0603 TMP_QCH5103K1900
PU18 PX3519 AL003519001 SMLF
VCC EN PWM GND TH GND_TH
UGATE BOOT PHASE LGATE
SW_DDR3_UG1 DDR3_BT1 SW_DDR3_PH1 SW_DDR3_LG1
DDR3_PWM1 IN
DDR3_EN OUT
PC221 0.1UF 16V X5R 0402 CH4103K9B09
BSZ060NE2LS RDS(ON)MAX=6M
3*3
PQ55 SMLF BSZ060NE2LS BAM060N0001
BSC014NE2LSI RDS(ON)MAX=1.4M
5*6
IC BAM014N0000 PQ39 BSC014NE2LSI SMLF
PC266 0.1UF 16V X5R 0402 CH4103K9B09
PC491 10UF 25V X6S 1206 TMP_QCH61004M2E8
PC294 10UF 25V X6S 1206 TMP_QCH61004M2E8
SW_P12V_DDR3_FLT
PC334 270UF 20% 16V OSCON RDLF CC7703MD19 RI=5A 6.3*8
PL62 0.2UH/35A CV+20^0MZ04 DCR=0.23M ISAT=22A 5*5*7
P12V
IN FACT THE VALUE IS 300NH
PL42 IND
320NH SP_CV+32^0MZ08 DCR=0.31M ISAT=53A 10*10*9
PC450 10UF 6.3V X5R 0805 CH61001KA94
PC96 820UF 2.5V EMPTY ESR=7M 6*8 TMP_QCC7820JMD01
PC100 820UF 2.5V OSCON ESR=7M 6*8 TMP_QCC7820JMD01
PVDDQ_GH
DDR3_ISEN1_N OUT
DDR3_ISEN1_P OUT

# DDR3 PHASE 2

P5V
PC234 1UF 16V X7R 0603 TMP_QCH5103K1900
PU17 PX3519 AL003519001 SMLF
VCC EN PWM GND TH GND_TH
UGATE BOOT PHASE LGATE
SW_DDR3_UG2 DDR3_BT2 SW_DDR3_PH2 SW_DDR3_LG2
DDR3_EN IN
DDR3_PWM2 IN
PC228 0.1UF 16V X5R 0402 CH4103K9B09
BSZ060NE2LS RDS(ON)MAX=6M
3*3
PQ54 SMLF BSZ060NE2LS BAM060N0001
BSC014NE2LSI RDS(ON)MAX=1.4M
5*6
IC BAM014N0000 PQ38 BSC014NE2LSI SMLF
PC265 0.1UF 16V X5R 0402 CH4103K9B09
PC490 10UF 25V X6S 1206 TMP_QCH61004M2E8
PC302 10UF 25V X6S 1206 TMP_QCH61004M2E8
SW_P12V_DDR3_FLT
IN FACT THE VALUE IS 300NH
PL41 IND
320NH SP_CV+32^0MZ08 DCR=0.31M ISAT=53A 10*10*9
PC448 10UF 6.3V X5R 0805 CH61001KA94
PC135 820UF 2.5V OSCON ESR=7M 6*8 TMP_QCC7820JMD01
PC107 820UF 2.5V OSCON ESR=7M 6*8 TMP_QCC7820JMD01
PC578 820UF 2.5V EMPTY ESR=7M 6*8 TMP_QCC7820JMD01
PVDDQ_GH
PC62 560UF 20% 2.5V OSCON RDLLF CC7560JMD03 ESR= 7 5*8
PC66 560UF 20% 2.5V OSCON RDLLF CC7560JMD03 ESR= 7 5*8
DDR3_ISEN2_N OUT
DDR3_ISEN2_P OUT

# DDR3 PHASE 3

P5V
PC233 1UF 16V X7R 0603 TMP_QCH5103K1900
PU16 PX3519 AL003519001 SMLF
VCC EN PWM GND TH GND_TH
UGATE BOOT PHASE LGATE
SW_DDR3_UG3 DDR3_BT3 SW_DDR3_PH3 SW_DDR3_LG3
DDR3_EN IN
DDR3_PWM3 IN
PC220 0.1UF 16V X5R 0402 CH4103K9B09
BSZ060NE2LS RDS(ON)MAX=6M
3*3
PQ53 SMLF BSZ060NE2LS BAM060N0001
BSC014NE2LSI RDS(ON)MAX=1.4M
5*6
IC BAM014N0000 PQ37 BSC014NE2LSI SMLF
PC264 0.1UF 16V X5R 0402 CH4103K9B09
PC303 10UF 25V X6S 1206 TMP_QCH61004M2E8
PC304 10UF 25V X6S 1206 TMP_QCH61004M2E8
SW_P12V_DDR3_FLT
IN FACT THE VALUE IS 300NH
PL40 IND
320NH SP_CV+32^0MZ08 DCR=0.31M ISAT=53A 10*10*9
PC449 10UF 6.3V X5R 0805 CH61001KA94
PC176 820UF 2.5V OSCON ESR=7M 6*8 TMP_QCC7820JMD01
PC151 820UF 2.5V OSCON ESR=7M 6*8 TMP_QCC7820JMD01
PVDDQ_GH
DDR3_ISEN3_N OUT
DDR3_ISEN3_P OUT

PVDDQ_DDR_GH 2 OF 2

Quanta

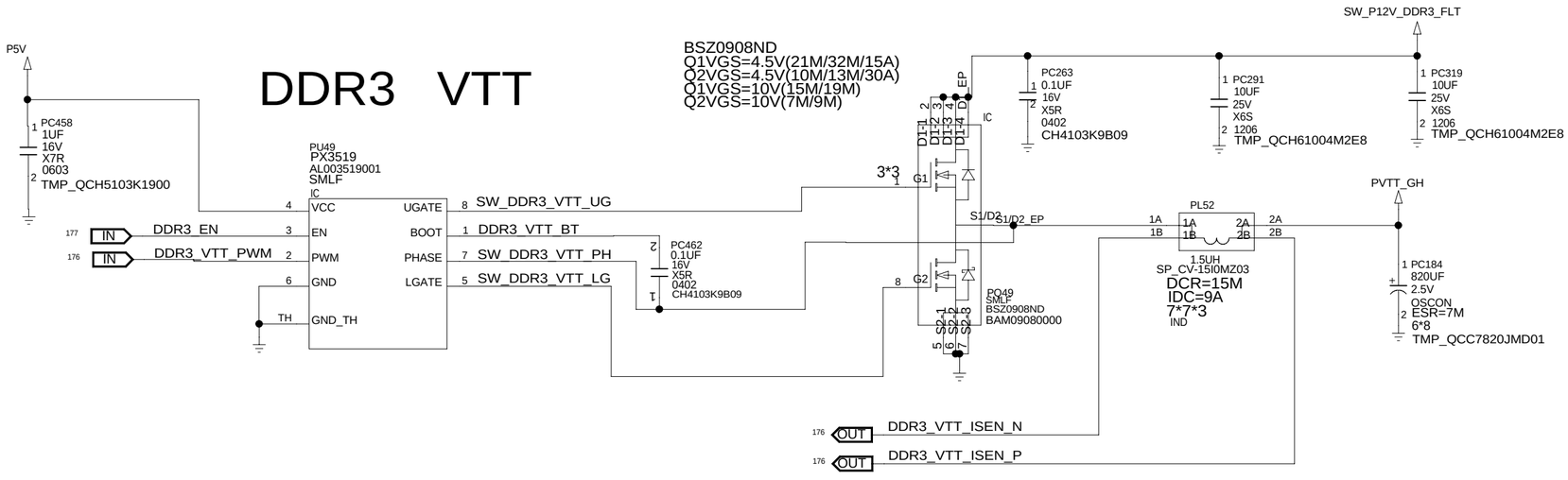
| DEPARTMENT | DESIGNER | PROJCET | DOCUMENT NUMBER | REV |
|---|---|---|---|---|
| CCBU | KENT CHOU | S2B | DA0S2BMB8A0 | 1 |
| | REVIEWER NICK,PETER,MATT,KUOCHAN | SIZE C DATE Mon Nov 16 11:56:02 2015 | SHEET 177 OF 188 | |

# DDR3 VTT

## DDR3_VTT SPECIFICATION

VOUT=1/2 VDDQ+/-1.5%
RIPPLE & NOISE=+/-1%
AC_LL=1/2VDDQ+/-57MV
TDC=+/-3.3A (FOR LRDIMM)
MAX CURRENT=+/-3.6A (FOR LRDIMM)
OCP(MAX CURRENT*130%)=+/-4.68A
CURRENT STEP=0.25A
SLEW RATE=3A/US

BSZ0908ND
Q1VGS=4.5V(21M/32M/15A)
Q2VGS=4.5V(10M/13M/30A)
Q1VGS=10V(15M/19M)
Q2VGS=10V(7M/9M)

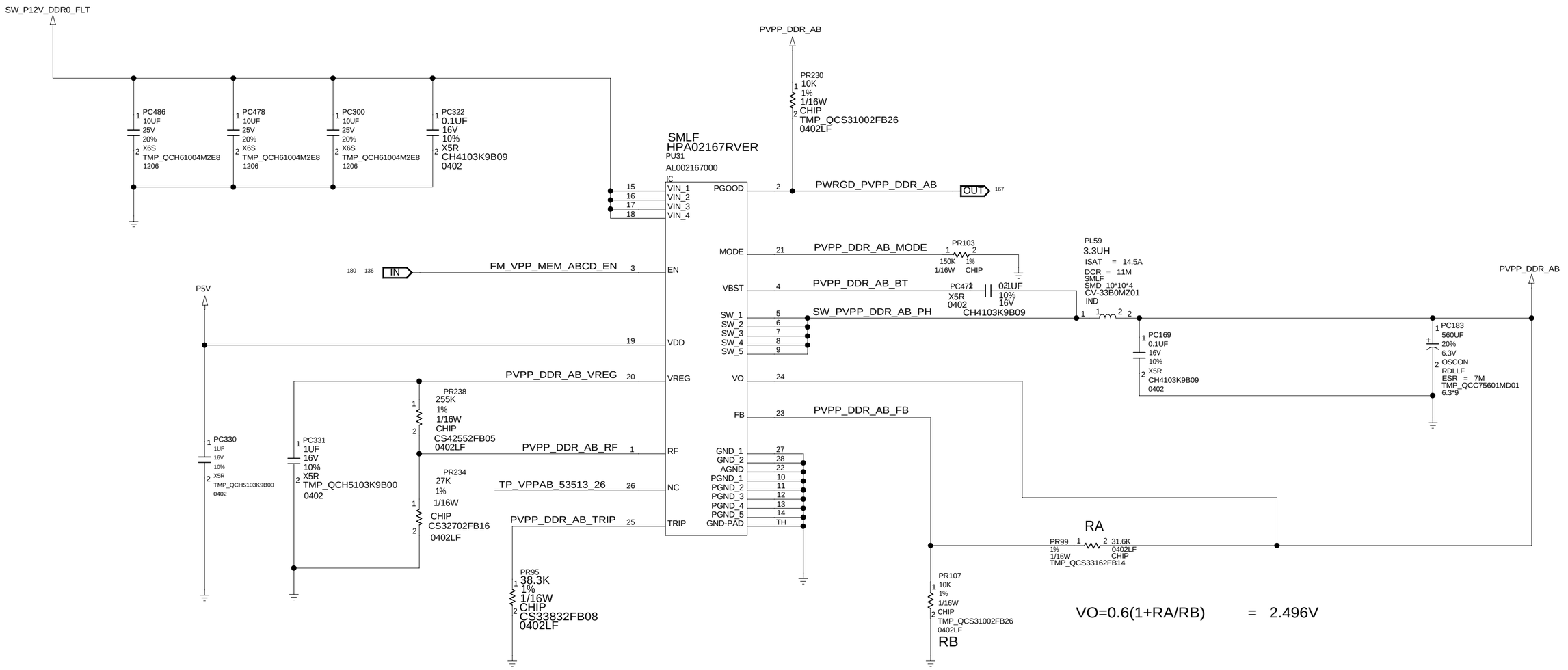



PVTT_DDR_GH

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: KENT CHOU | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: NICK,PETER,MATT,KUOCHAN | SIZE: C | DATE: Mon Nov 16 11:56:04 2015 | SHEET: 178 OF 188 | |

# DESIGN SPECIFICATION

OUTPUT VOLTAGE = 2.5+/-1% DC
OUTPUT RIPPLE & NOISE < 23MV
TRANSIENT TOLERANCE = +130MV/-233MV
TDC = 2.1A
MAX CURRENT = 3.8A
OVER-CURRENT PROTECTION(MAX RATING * 1.3) = 4.94A
CURRENT STEP = 3.1A
SLEW RATE = 25.4A/US
WORK FREQUENCY = 300KHZ
EFFICIENCY > 90% @TDC

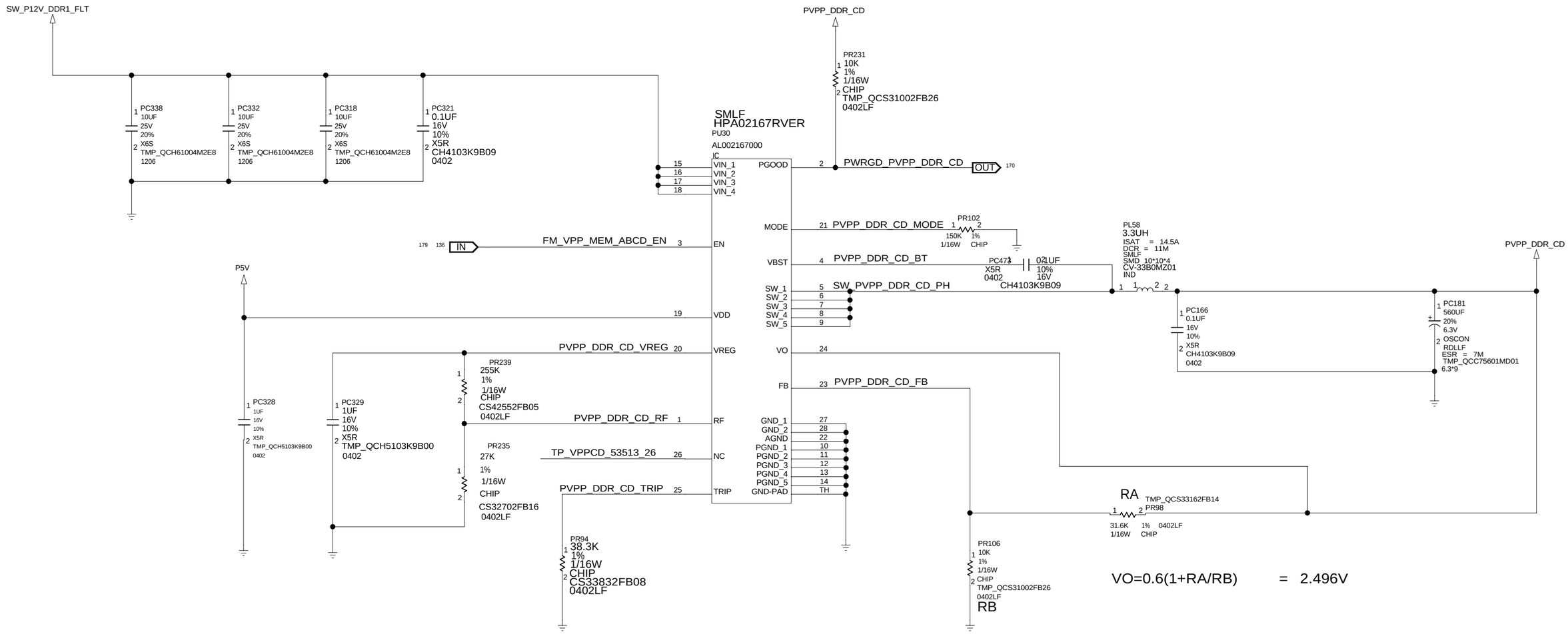



PVPP_DDR_AB

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: BEN CHIANG | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 |
| | | REVIEWER: NICK,PETER,MATT,KUOCHAN | SIZE: C DATE: Mon Nov 16 11:56:04 2015 | SHEET 179 OF 188 | |

# DESIGN SPECIFICATION

OUTPUT VOLTAGE = 2.5+/-1% DC
OUTPUT RIPPLE & NOISE < 23MV
TRANSIENT TOLERANCE = +130MV/-233MV
TDC = 2.1A
MAX CURRENT = 3.8A
OVER-CURRENT PROTECTION(MAX RATING * 1.3) = 4.94A
CURRENT STEP = 3.1A
SLEW RATE = 25.4A/US
WORK FREQUENCY = 300KHZ
EFFICIENCY > 90% @TDC

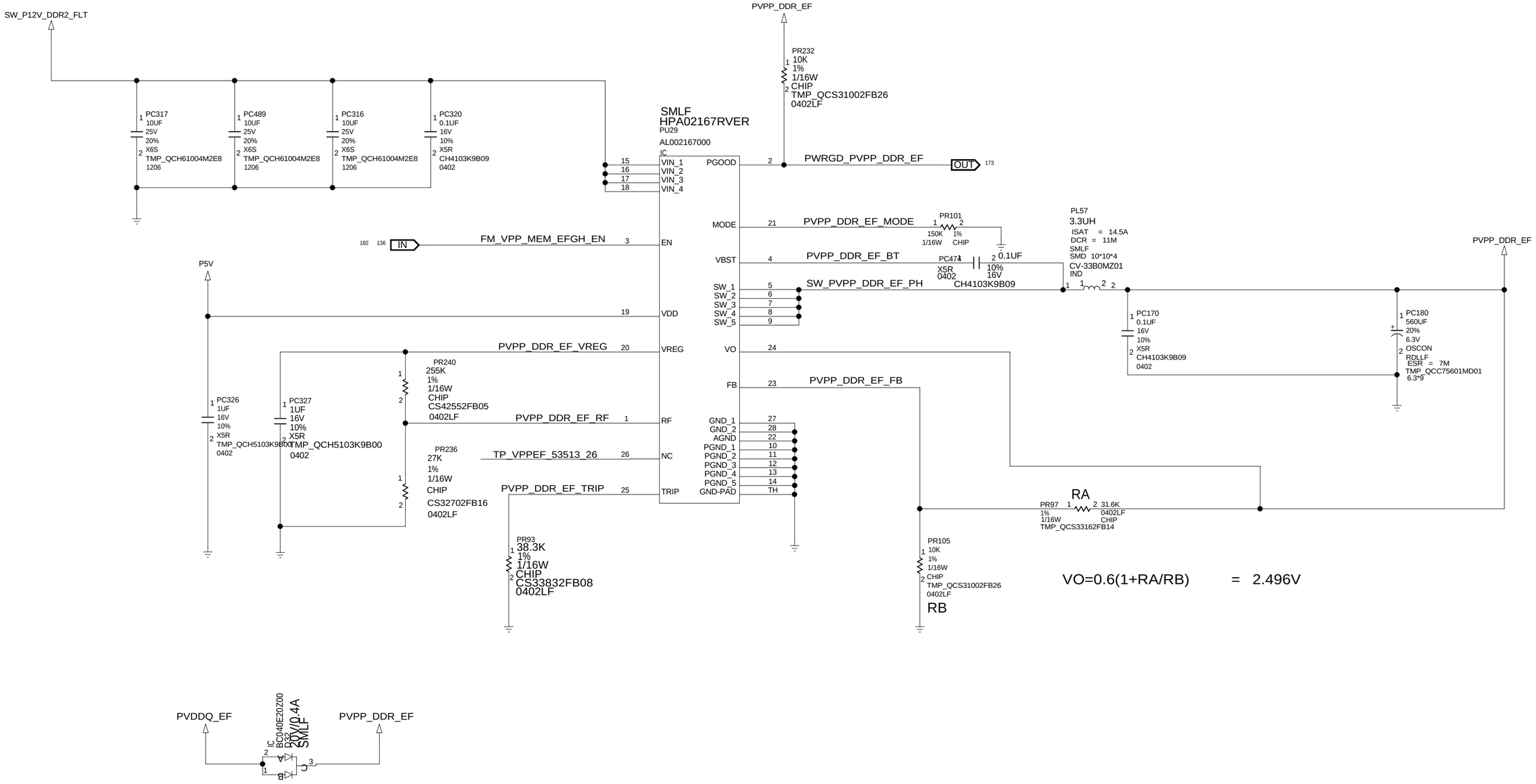



PVPP_DDR_CD

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT: CCBU | DESIGNER: BEN CHIANG | PROJCET: S2B | DOCUMENT NUMBER: DA0S2BMB8A0 | REV: 1 | |
| | | REVIEWER: NICK,PETER,MATT,KUOCHAN | SIZE C | DATE Mon Nov 16 11:56:07 2015 | SHEET 180 OF 188 | |

# DESIGN SPECIFICATION

OUTPUT VOLTAGE = 2.5+/-1% DC
OUTPUT RIPPLE & NOISE < 23MV
TRANSIENT TOLERANCE = +130MV/-233MV
TDC = 2.1A
MAX CURRENT = 3.8A
OVER-CURRENT PROTECTION(MAX RATING * 1.3) = 4.94A
CURRENT STEP = 3.1A
SLEW RATE = 25.4A/US
WORK FREQUENCY = 300KHZ
EFFICIENCY > 90% @TDC

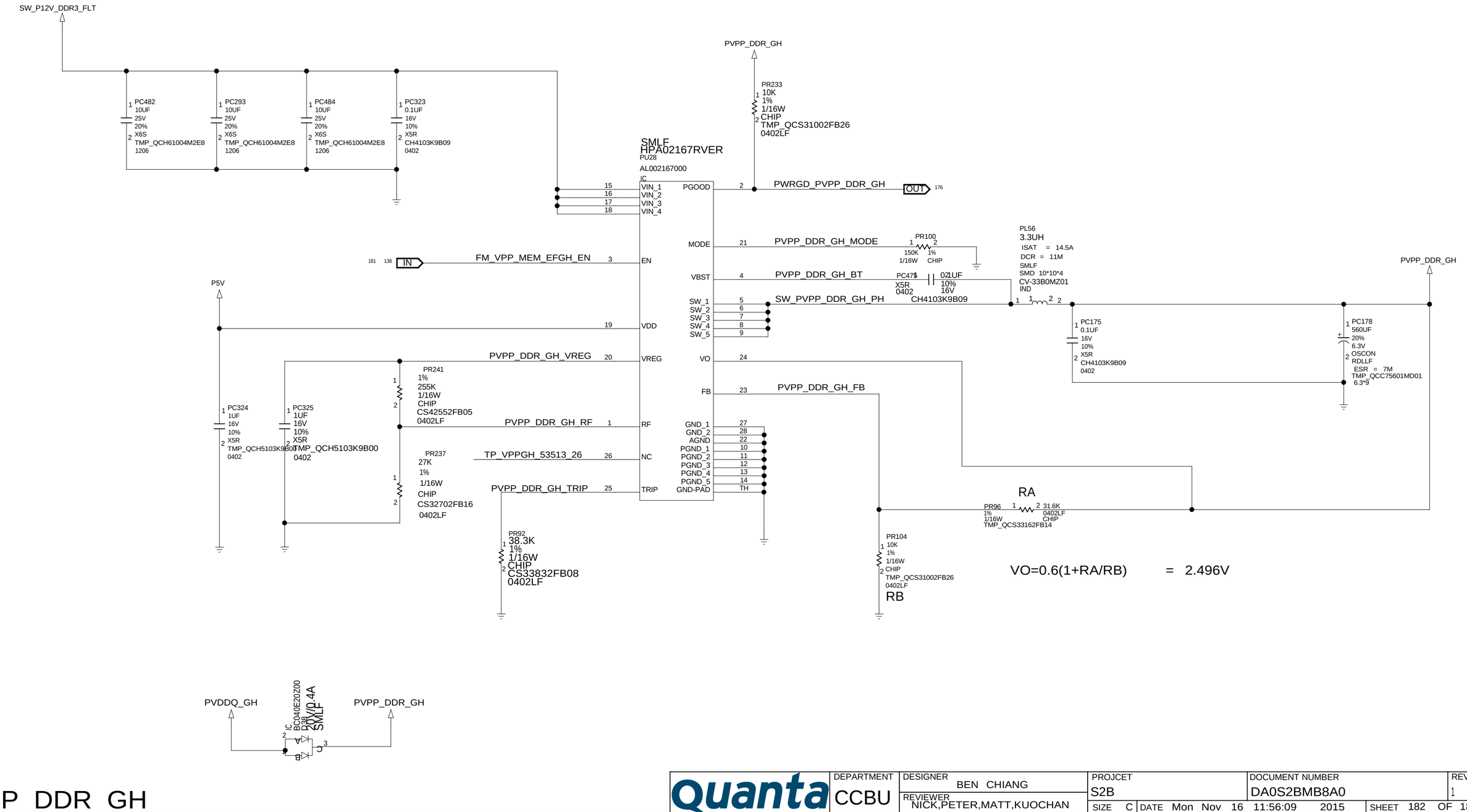



PVPP_DDR_EF

| | | | | | | |
|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER BEN CHIANG | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | |
| | | REVIEWER NICK,PETER,MATT,KUOCHAN | SIZE C | DATE Mon Nov 16 11:56:08 2015 | SHEET 181 OF 188 | |

# DESIGN SPECIFICATION

OUTPUT VOLTAGE = 2.5+/-1% DC
OUTPUT RIPPLE & NOISE < 23MV
TRANSIENT TOLERANCE = +130MV/-233MV
TDC = 2.1A
MAX CURRENT = 3.8A
OVER-CURRENT PROTECTION(MAX RATING * 1.3) = 4.94A
CURRENT STEP = 3.1A
SLEW RATE = 25.4A/US
WORK FREQUENCY = 300KHZ
EFFICIENCY > 90% @TDC




PVPP_DDR_GH

| | | | | | |
|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER BEN CHIANG | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 |
| | | REVIEWER NICK,PETER,MATT,KUOCHAN | SIZE C | DATE Mon Nov 16 11:56:09 2015 | SHEET 182 OF 188 |

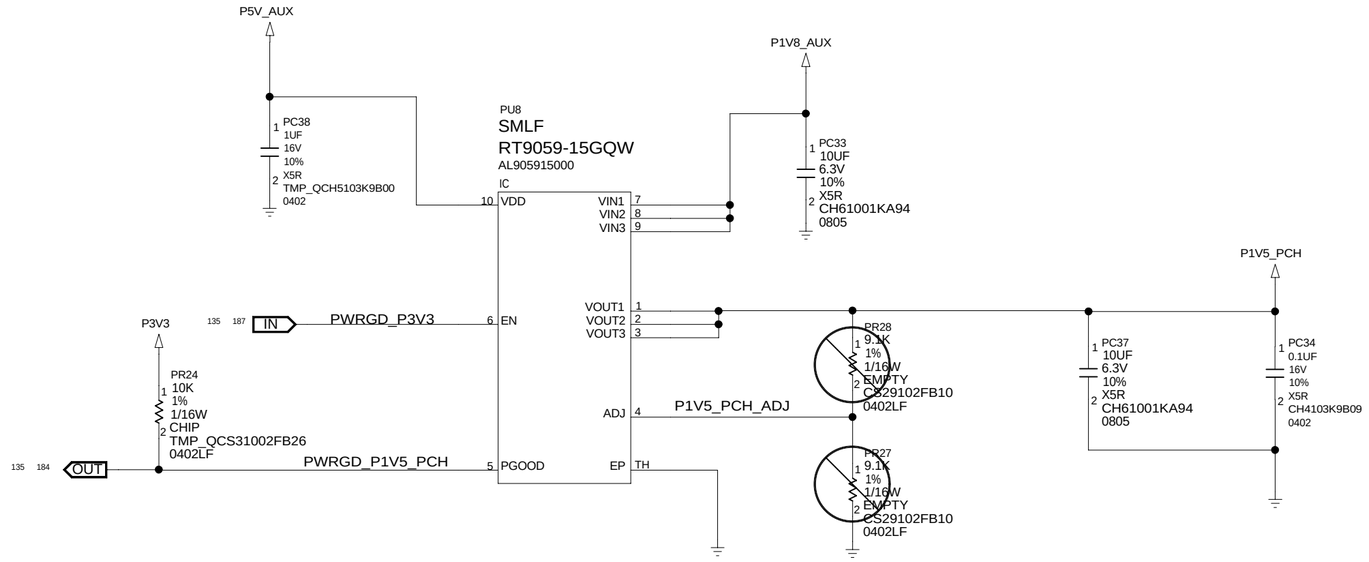
OUTPUT VOLTAGE = 1.5V+/-5%

OUTPUT RIPPLE & NOISE < 30MV

TRANSIENT TOLERANCE = 150MV

MAX CURRENT = 0.2A

PD = (1.8V - 1.5V) * 0.2A = 0.06W




RT9059-15GQW FIXED VOLTAGE 1.5V
ADJUSTABLE VOLTAGE : VOUT=0.8*(1+RA/RB)

P1V5_PCH

| | | | | |
|---|---|---|---|---|
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| | | | | SHEET 183 OF 188 |

# DESIGN SPECIFICATION

OUTPUT VOLTAGE = 1.05+/-2% DC
OUTPUT RIPPLE & NOISE < 21MV
TRANSIENT TOLERANCE = 105MV
TDC = 0.5A
MAX CURRENT = 2A
OVER-CURRENT PROTECTION(MAX RATING * 1.3) = 2.6A
CURRENT STEP = 0.3A
SLEW RATE = 0.3A/US
WORK FREQUENCY = 300KHZ
EFFICIENCY > 90% @TDC

P12V
PL24 0.1UH SMLF SMD 4*4*6 CV+10G0MZ01 IND
SW_PVCCIO_FLT
PC382 10UF 25V 20% X6S TMP_QCH61004M2E8 1206
PC58 10UF 25V 20% X6S TMP_QCH61004M2E8 1206
PC381 10UF 25V 20% EMPTY TMP_QCH61004M2E8 1206
PC57 0.1UF 16V 10% X5R CH4103K9B09 0402

P3V3_AUX
PR143 10K 1% 1/16W EMPTY TMP_QCS31002FB26 0402LF

SMLF HPA02167RVER
PU9
AL002167000
IC
VIN_1 VIN_2 VIN_3 VIN_4 PGOOD MODE VBST SW_1 SW_2 SW_3 SW_4 SW_5 VO FB GND_1 GND_2 AGND PGND_1 PGND_2 PGND_3 PGND_4 PGND_5 GND-PAD TH EN VDD VREG RF NC TRIP

PVCCIO_PG
TMP_QCS00002FB00 R1232 0 1% 1/16W CHIP 0402LF
PWRGD_P1V5_PCH OUT 183 135

185 135 IN FM_VCC_MAIN_EN

PVCCIO_BT
PC383 0.1UF 10% 16V X5R 0402 CH4103K9B09
SW_PVCCIO_PH
PL25 1.5UH ISAT = 33A DCR = 3.8M SMLF SMD 10*10*4 CV-15G0MZ03 IND
PVCCIO
PC59 390UF 20% 2.5V OSCON SMLF ESR = 10M CC7390JMZ01 5*5.8
PC384 10UF 6.3V 10% X5R CH61001KA94 0805
PC385 10UF 6.3V 10% X5R CH61001KA94 0805
PC386 0.1UF 16V 10% X5R CH4103K9B09 0402

P5V_AUX
PC56 1UF 16V 10% X5R TMP_QCH5103K9B00 0402
PC55 1UF 16V 10% X5R TMP_QCH5103K9B00 0402

PVCCIO_VREG
PR141 255K 1% 1/16W CHIP CS42552FB05 0402LF
PVCCIO_RF
PR142 27K 1% 1/16W CHIP CS32702FB16 0402LF
TP_VCCIO_53513_26
PVCCIO_TRIP
PR33 24.9K 1% 1/16W CHIP CS32492FB16 0402LF

PVCCIO_FB
RA
PR32 1 6.98K 1% 1/16W CHIP 0402LF CS26982FB01
PR31 12K 1% 1/16W CHIP TMP_QCS31202FB15 0402LF
RB
PR30 42.2K 1% 1/16W CHIP TMP_QCS34222FB00 0402LF
PVCCIO_FB_R

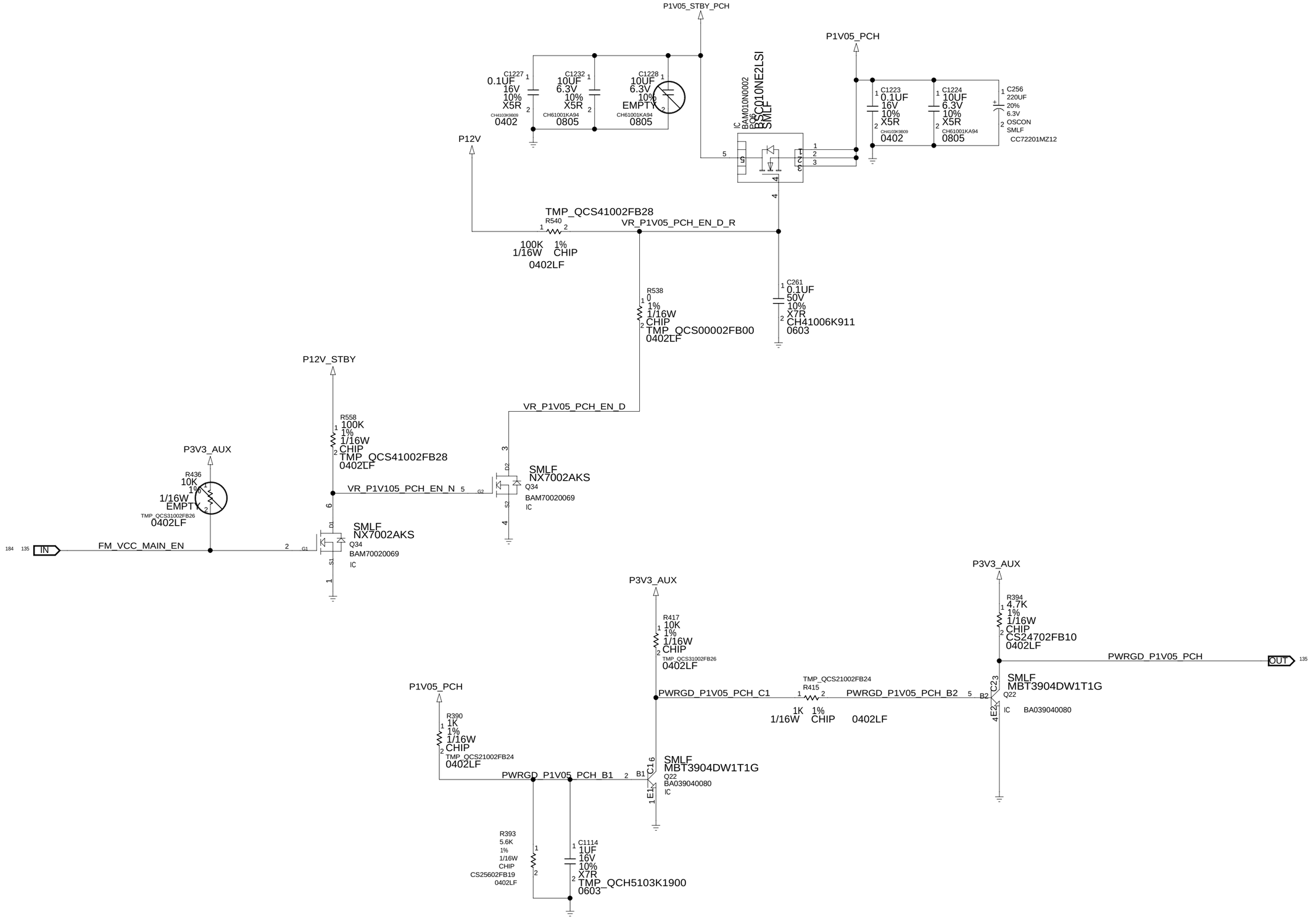
VO=0.6(1+RA/RB) = 0.949V

135 103 41 10 IN FM_CPU0_BDX_PRSNT_LVT3_N
PQ65 SMLF NX7002AK BAM70020062 IC
DRAIN SOURCE GATE

| FM_CPU0_BDX_PRSNT_LVT3_N | OUTPUT VOLTAGE |
|---|---|
| HIGH | 1.05V |
| LOW | 0.949V |

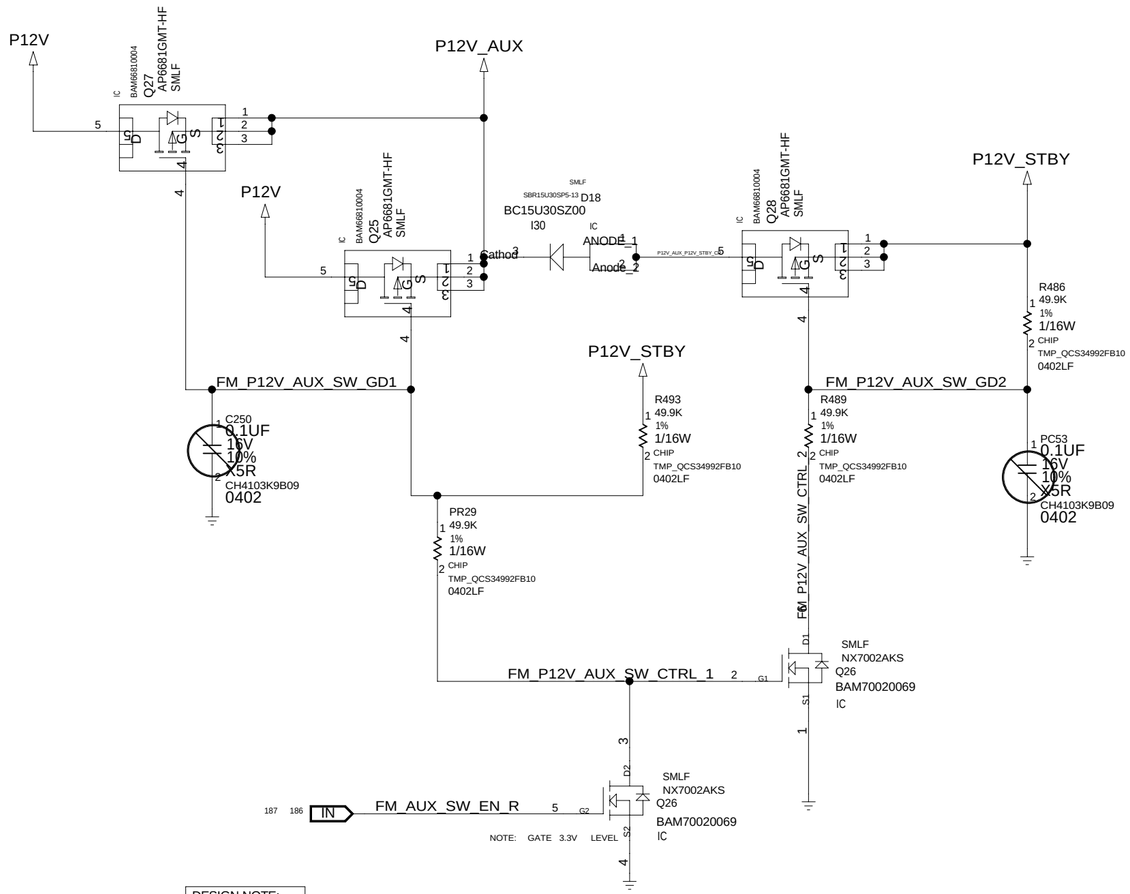
PVCCIO

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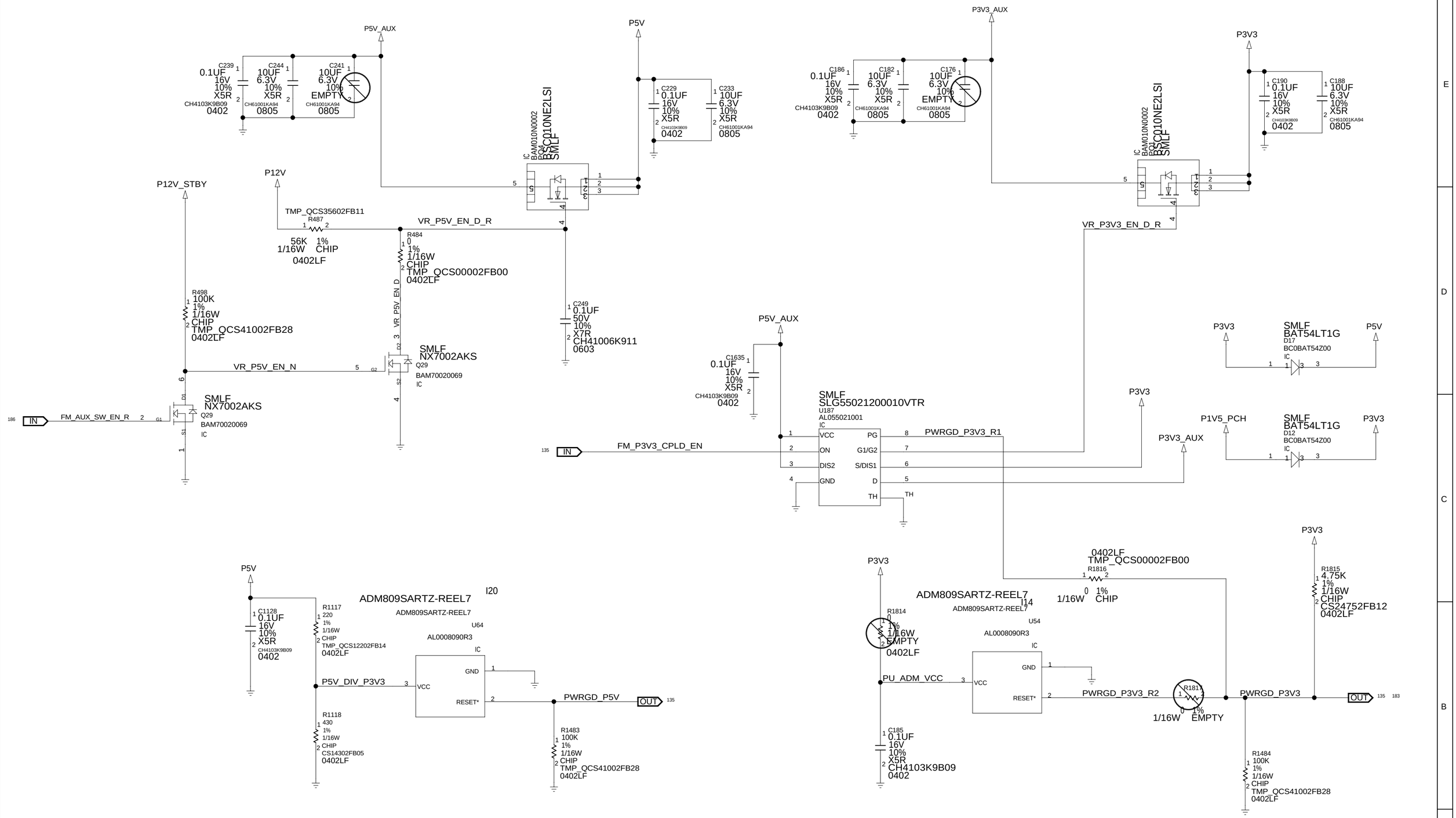

# P1V05_PCH_SWITCH

| | | | | | | |
|---|---|---|---|---|---|---|
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| | | REVIEWER: NICK,PETER,MATT | SIZE: C | DATE: Mon Nov 16 11:56:12 2015 | SHEET: 185 OF 188 | |




# P12V_AUX_SWITCH

| | | | | | | |
|---|---|---|---|---|---|---|
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# P5V P3V3 SWITCH

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Quanta | DEPARTMENT CCBU | DESIGNER NICK | PROJCET S2B | DOCUMENT NUMBER DA0S2BMB8A0 | REV 1 | | |
| | | REVIEWER NICK,PETER,MATT | SIZE C | DATE Mon Nov 16 11:56:16 2015 | SHEET 187 OF 188 | | |

# THUMB SCREW HOLE

TH
H15
HOLE447
EMPTY

TH
H9
HOLE447
EMPTY

SCREW1
SCREW2

FBS2Z042010

# MEZZ SCREW HOLE

TH
H4
HOLE87
EMPTY

TH
H7
HOLE87
EMPTY

TH
H8
HOLE87
EMPTY

TH
H6
HOLE87
EMPTY

NUT1
NUT2
NUT3
NUT4

FBS2Z006010

# TPM SCEW HOLE

TH
H5
HOLE276
EMPTY

MBS4E001010

TH
H10
GND_HOLE347
EMPTY

TH
H14
GND_HOLE347
EMPTY

TH
H1
GND_HOLE347
EMPTY

TH
H13
GND_HOLE347
EMPTY

TH
H3
GND_HOLE347
EMPTY

TH
H2
GND_HOLE347
EMPTY

TH
H12
GND_HOLE347
EMPTY

TH
H16
GND_HOLE347
EMPTY

TH
H17
GND_HOLE347
EMPTY

TH
H11
GND_HOLE347
EMPTY

# HEATSINK ANCHOR

THMTLF
CONN2_HB9003EK
HB9003E-K
JP13
DFHD02MR435
CONN

THMTLF
CONN2_HB9003EK
HB9003E-K
JP12
DFHD02MR435
CONN

THMTLF
CONN2_HB9003EK
HB9003E-K
JP5
DFHD02MR435
CONN

THMTLF
CONN2_HB9003EK
HB9003E-K
JP6
DFHD02MR435
CONN

I151
MECH
LGA2011_R3_MH_4H
TH1
HOLE390
MECH

I138
MECH
LGA2011_R3_MH_4H
TH2
HOLE390
MECH

# SET2DIL

MISC
SET2DIL
J9
TP17
MISC
TOP_85OHM
I206
AGND

MISC
SET2DIL
J70
TP17
MISC
IN1_85_OHM
AGND

MISC
SET2DIL
J21
TP17
MISC
THRU_TOP_85_OHM
I208
AGND

MISC
SET2DIL
J69
TP17
MISC
BOT_85OHM
I207
AGND

MISC
SET2DIL
J56
TP17
MISC
IN2_85_OHM
I205
AGND

# SPARE PART

TP_Q54_SEC2
SMLF
NX7002AKS
Q18
BAM70020069
IC

# MOUNTING HOLE AND COUPON

| | | | | | | |
|---|---|---|---|---|---|---|
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