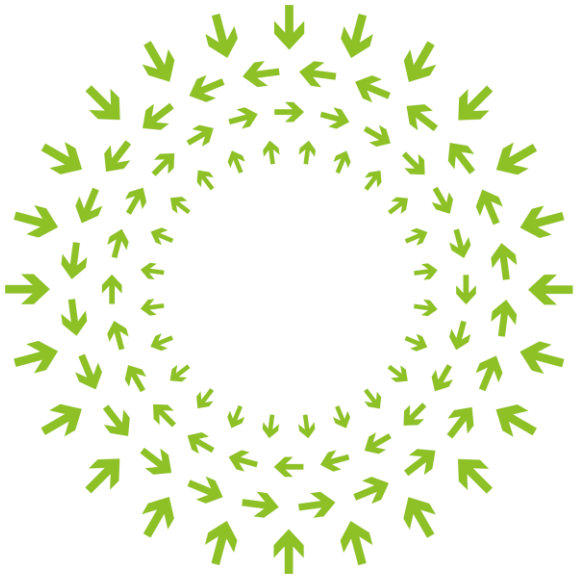


OPEN

Compute Project

QCT Big Basin Specification

Rev 0.1

Author: Alan Chang, Quanta Cloud Technology (QCT)

1. LICENSE OWFa 1.0

Contributions to this Specification are made under the terms and conditions set forth in Open Web Foundation Final Specification Agreement ("OWFa 1.0") ("Contribution License") by:

Quanta Cloud Technology (QCT)

You can review the signed copies of the applicable Contributor License(s) for this Specification on the OCP website at http://www.opencompute.org/products/specsanddesign

Usage of this Specification is governed by the terms and conditions set forth in Open Web Foundation Final Specification Agreement ("OWFa 1.0").

You can review the applicable Specification License(s) executed by the above referenced contributors to this Specification on the OCP website at http://www.opencompute.org/participate/legal-documents/

Note: The following clarifications, which distinguish technology licensed in the Contribution License and/or Specification License from those technologies merely referenced (but not licensed), were accepted by the Incubation Committee of the OCP:

NOTWITHSTANDING THE FOREGOING LICENSES, THIS SPECIFICATION IS PROVIDED BY OCP "AS IS" AND OCP EXPRESSLY DISCLAIMS ANY WARRANTIES (EXPRESS, IMPLIED, OR OTHERWISE), INCLUDING IMPLIED WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, FITNESS FOR A PARTICULAR PURPOSE, OR TITLE, RELATED TO THE SPECIFICATION. NOTICE IS HEREBY GIVEN, THAT OTHER RIGHTS NOT GRANTED AS SET FORTH ABOVE, INCLUDING WITHOUT LIMITATION, RIGHTS OF THIRD PARTIES WHO DID NOT EXECUTE THE ABOVE LICENSES, MAY BE IMPLICATED BY THE IMPLEMENTATION OF OR COMPLIANCE WITH THIS SPECIFICATION. OCP IS NOT RESPONSIBLE FOR IDENTIFYING RIGHTS FOR WHICH A LICENSE MAY BE REQUIRED IN ORDER TO IMPLEMENT THIS SPECIFICATION. THE ENTIRE RISK AS TO IMPLEMENTING OR OTHERWISE USING THE SPECIFICATION IS ASSUMED BY YOU. IN NO EVENT WILL OCP BE LIABLE TO YOU FOR ANY MONETARY DAMAGES WITH RESPECT TO ANY CLAIMS RELATED TO, OR ARISING OUT OF YOUR USE OF THIS SPECIFICATION, INCLUDING BUT NOT LIMITED TO ANY LIABILITY FOR LOST PROFITS OR ANY CONSEQUENTIAL, INCIDENTAL, INDIRECT, SPECIAL OR PUNITIVE DAMAGES OF ANY CHARACTER FROM ANY CAUSES OF ACTION OF ANY KIND WITH RESPECT TO THIS SPECIFICATION, WHETHER BASED ON BREACH OF CONTRACT, TORT (INCLUDING NEGLIGENCE), OR OTHERWISE, AND EVEN IF OCP HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

2. TABLE OF CONTENTS

3. SCOPE

This document defines the technical specifications for the Big Basin used in Open Compute Project Open Rack V2.

4. OVERVIEW

The Big Basin JBOG is 3OU/21" chassis which support eight NVIDIA SXM2 GPU accelerator modules, SXM2 GPU support NVIDIA@NVLINK which is high-bandwidth, energy-efficient interconnect between GPUs. The system communicates with head node through PCIe x16 interface. A Baseboard Management Controller is used to manage the system itself and communicate with head node BMC.

5. RACK COMPATIBILITY

The Big Basin occupies 3 Open U in any rack that is compliant to OCP Open Rack standard 2.0

6. BIG BASIN SPECIFICATIONS

6.1 PRODUCT ARCHITECTURE OVERVIEW

The Big Basin is eight GPU cluster project. The silicon ingredients and features are as follows list:

Table 6-1 System Feature List

Board Name	Big Basin System
GPU Baseboard	8 NVIDIA Tesla P100 SXM2 GPUs X16 PCIe slot x4 PEX 8780 PCIe Switch x2 PEX 8764 PCIe Switch x2
GPU Module	nVidia Tesla series – Pascal (GP100), 300W TDP PCIe x16
Middle Plane Board	ASPEED AST2500, BMC main memory 4Gb DDR4 Lattice CPLD LCMXO2-2000HC-4TG100CTR
IO Board	OCP V1 and V2 debug connectors and single RJ45 (1GbE) connector for dedicated management NIC, and LED/PWR button/PWR LED
Host Retimer Card	IDT Retimer 89HT0832PZCHLG8 4 MiniSAS-HD connector SFF-8644 X16 PCIe bus

Bridge Card W/O Retimer	4 MiniSAS-HD connector SFF-8644 X16 PCIe bus
FAN	Fan Quantity: 4 Fan size(L x W x H in mm): 9276 (76 x 92 x 92)
Power Supply	Through Open Rack Power Bus Bar, Open Rack V2 support
Chassis	3 OU BOX for Open Rack

6.2 PRODUCT ARCHITECTURE BLOCK DIAGRAM

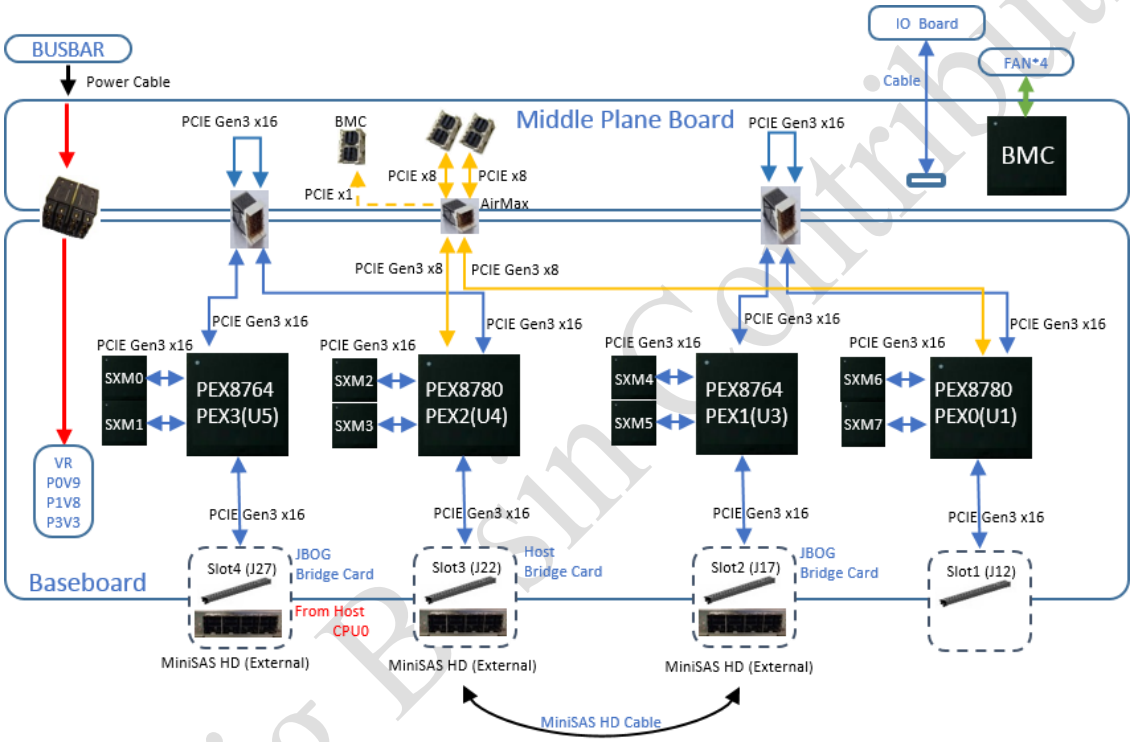


Figure 6-1 System Block Diagram Topology1

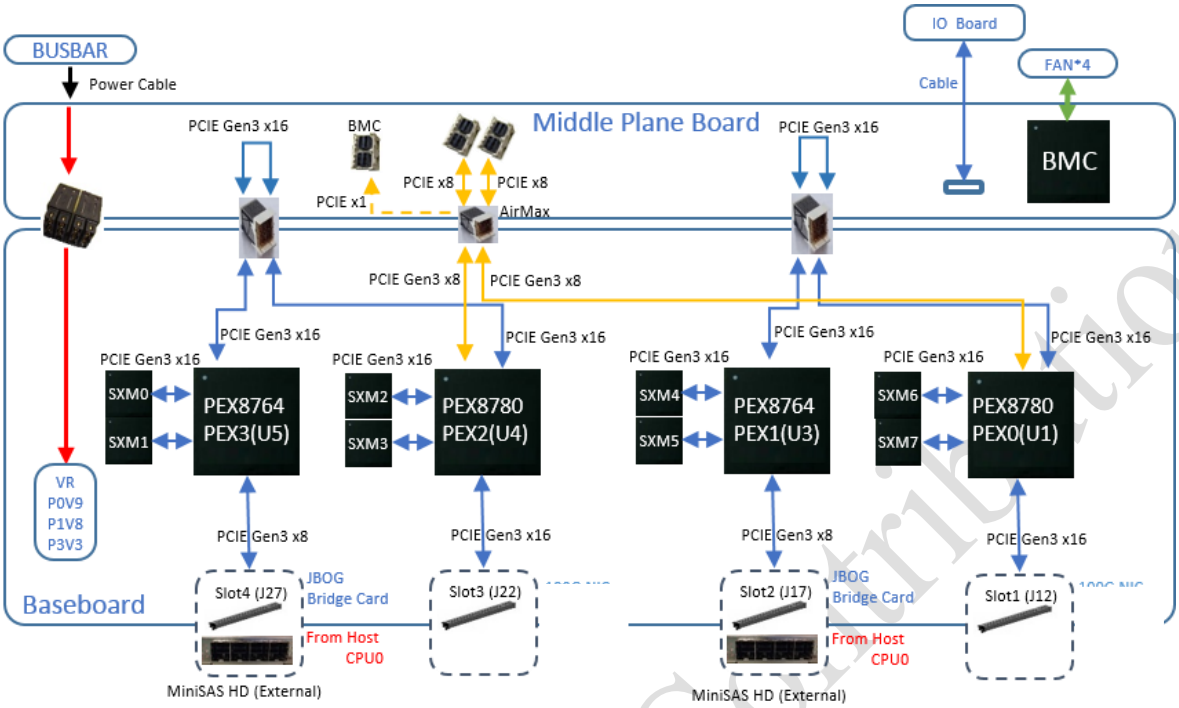


Figure 6-2 System Block Diagram Topology2

6.3 BOARD PLACEMENT

6.3.1 Big Basin Cards Placement

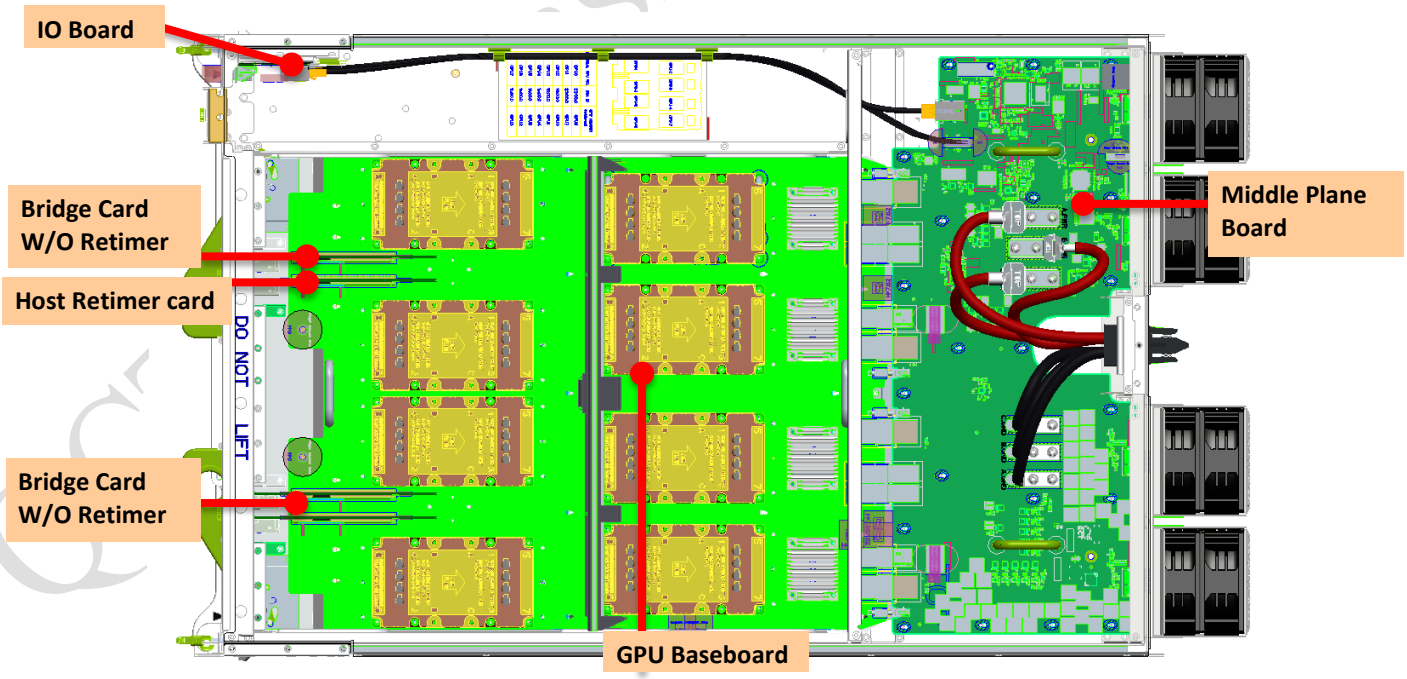


Figure 6-3 System Boards Placement Topology1

IO Board

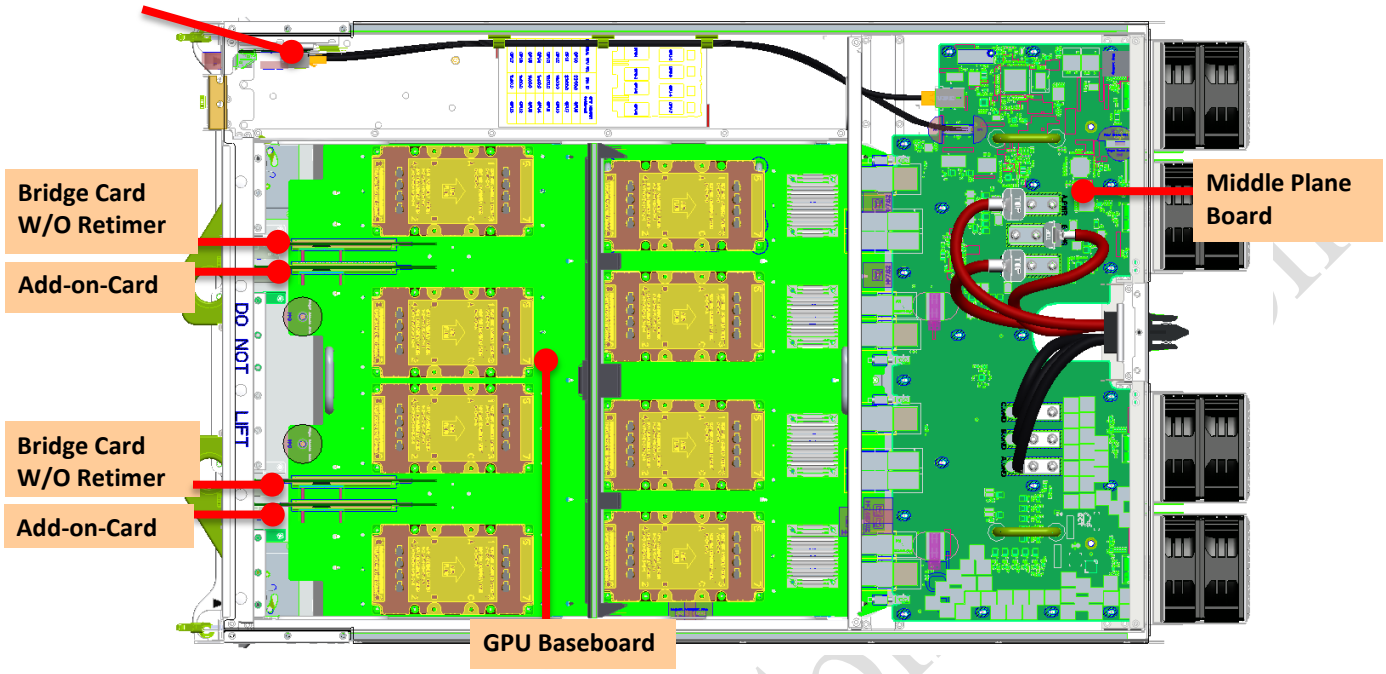


Figure 6-4 System Boards Placement Topology2

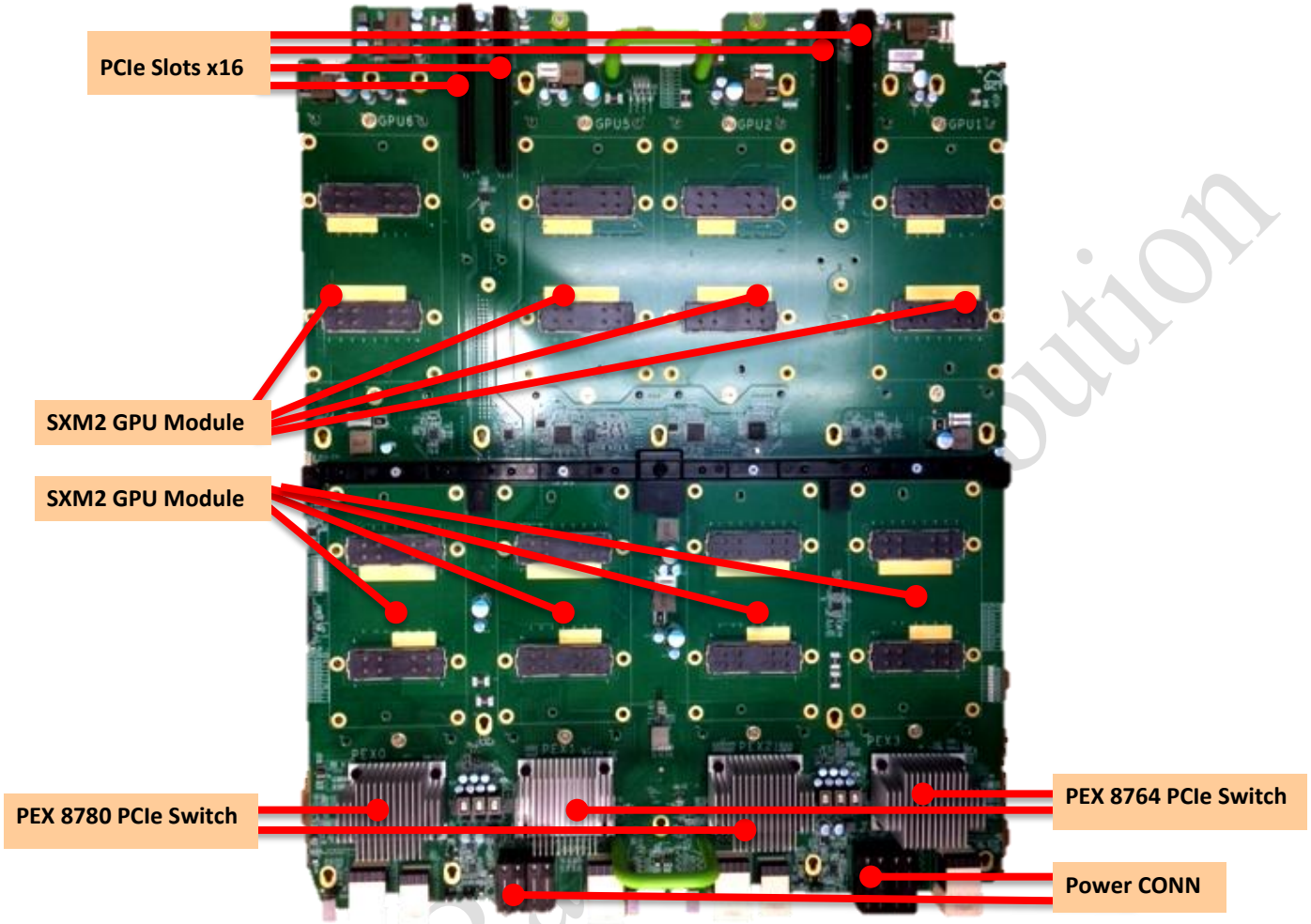


Figure 6-5 GPU Baseboard Placement

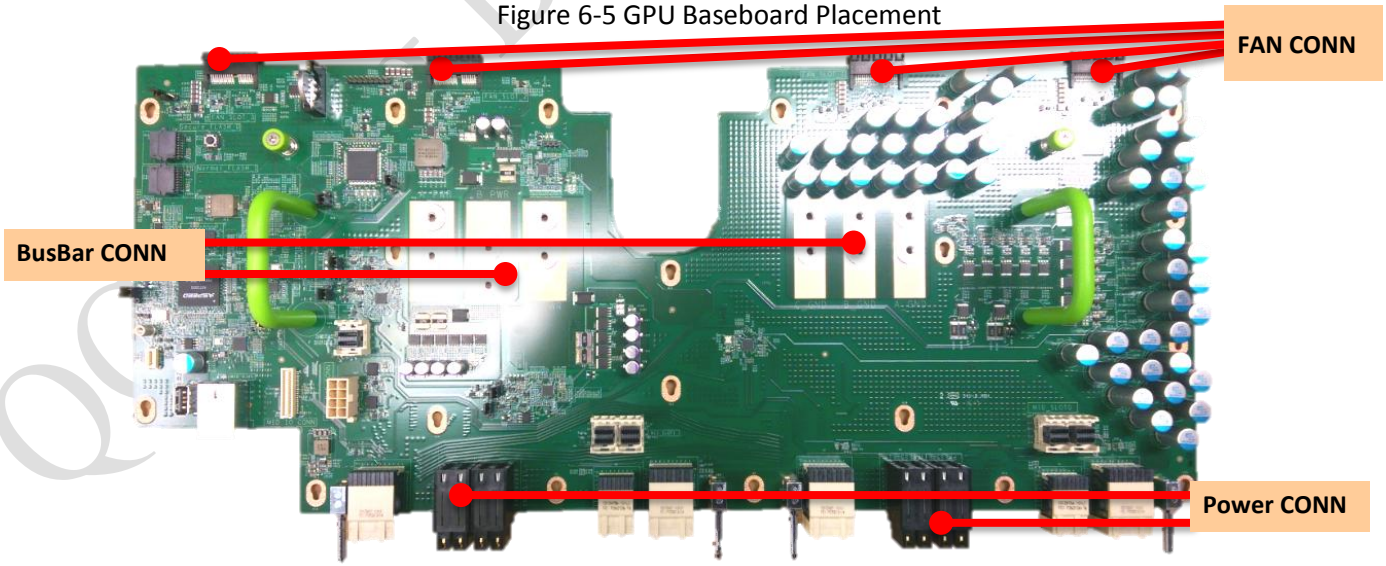


Figure 6-6 Middle Plane Board Placement

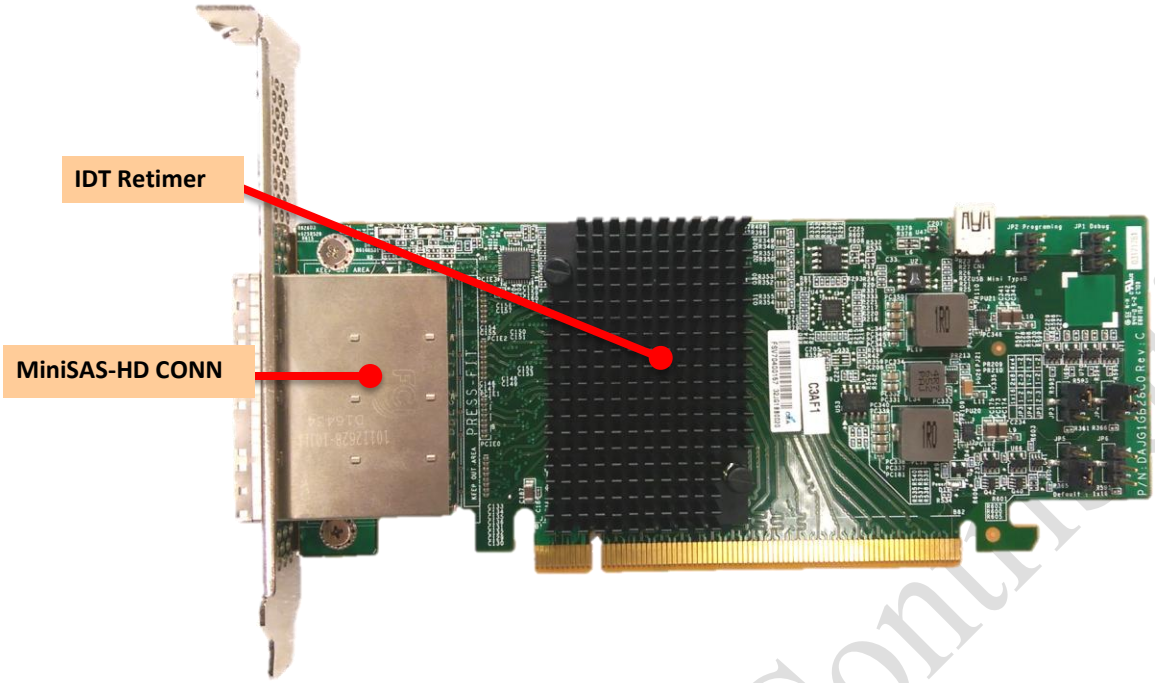


Figure 6-7 Host Retimer Card Placement

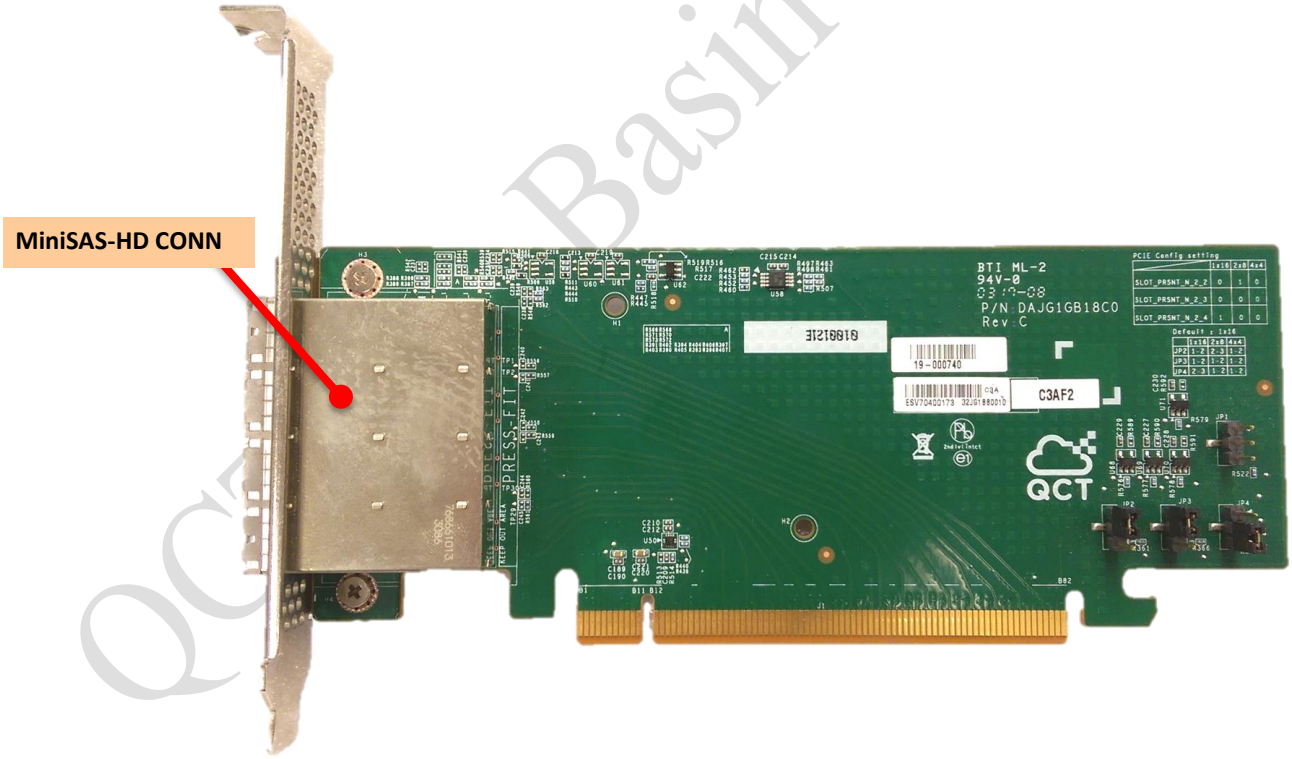


Figure 6-8 Bridge Card W/O Retimer Placement

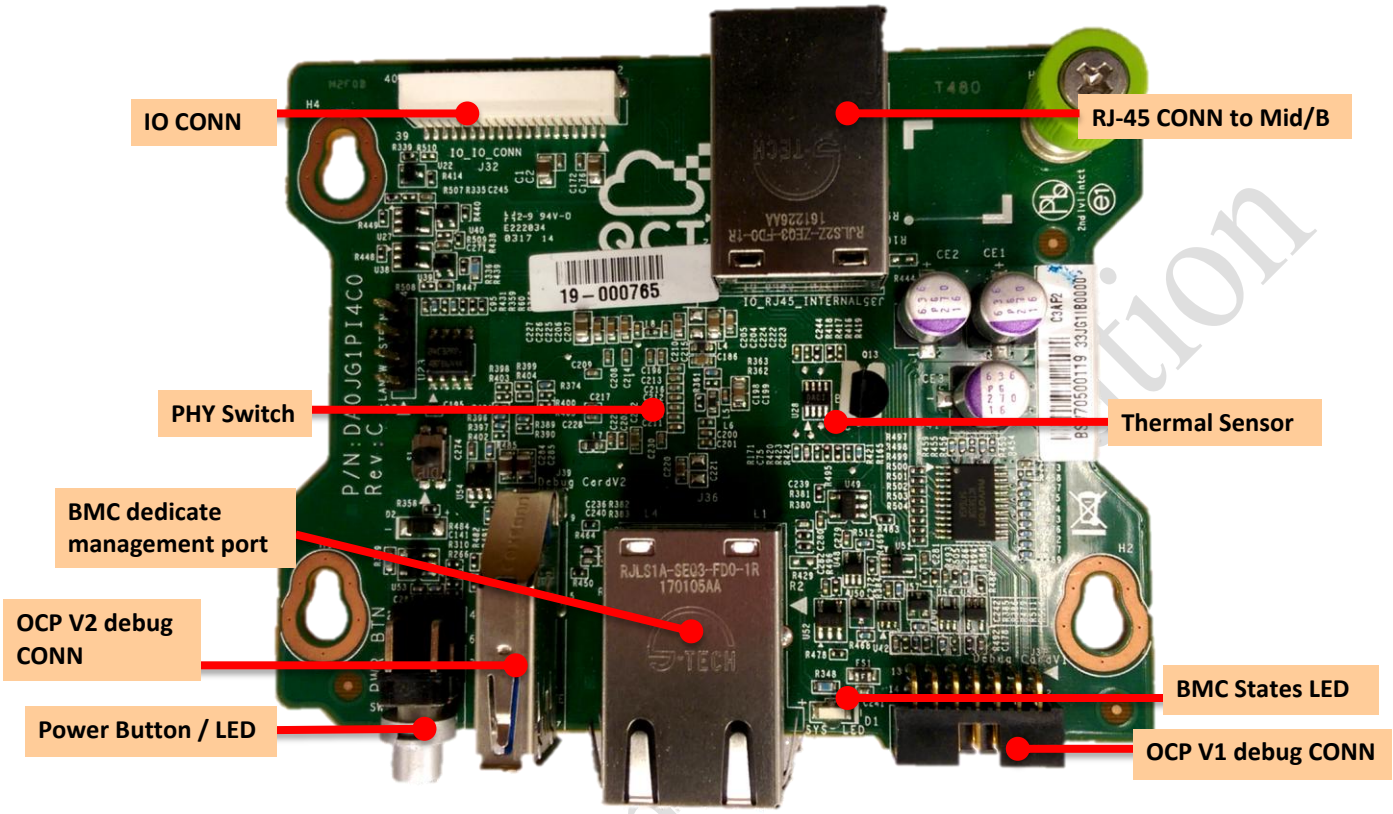


Figure 6-9 IO Board Placement

6.3.2 System Boards Dimension

Table 6-2 Big Basin Boards Dimension

Board name	Board dimension	PCB thickness	Layer count	PCB material
GPU Baseboard	516 x 414	2.654mm	18	IT-968+HVLP
Middle Plane Board	515.4 x 210.4	2.35mm	18	IT-968+HVLP
Host Retimer Card	167.65 x 68.9	1.6mm	8	IT-170GRA1+ RTF
Bridge Card W/O Retimer	167.65 x 68.9	1.6mm	8	IT-170GRA1+ RTF
IO Board	84 x 36	1.6mm	4	IT-170GRA1

6.3.3 System Cards Stackup

STACKUP						Target Z (ohms) - MicroStrip		GCE Stack up proposal Material:IT968+HVLP (5mil core+RTF)		50	Breakout	85		Insertion Loss for 85 ohm(db/inch)			Breakout	
						Target Z (ohms) - StripLine				50		85						
						Z tolerance				±10%		±10%						
						Z Type				Single	Single	Differential		4G Hz	8G Hz	10G Hz	Differential	
Layer#	Description	Copper Weight (oz)	Thickness (mil)	Tolerance (mil)	Er	Glass/Copper Type	Thickness (mil)	Dk	Width	Width	Width	Space				Width	Space
	Soldermask		0.60		3.8	SM	0.50											
1	TOP	0.5+plating	1.95			0.5oz+plating	1.90		5.6	5.6	5.8	7.2				3.5	3.8
	PP		3.00	±0.709	3.2	1080	3.10	3.20	5.6/50.05		5.8/7.2/88.89	6.25/6.75/84.99	-0.554	-1.004	-1.229	3.5/8/111.94	
2	GND	1	1.30			1oz	1.25										
	CORE		3.50	±0.709	3.2	3.5mil(3313)	3.50	3.20									
3	IN1	1	1.30			1oz	1.25		3.3	3.3	3.5	3.8				3.5	3.8
	PP		3.30	±0.709	3.2	106 x 2	3.30	3.20	3.3/50.44		3.5/3.8/88.77	3.75/3.55/85.08	-0.499	-0.862	-1.044	3.5/8/96.28	
4	GND1	1	1.30			1oz	1.25										
	CORE		3.50	±0.709	3.2	3.5mil(3313)	3.50	3.20									
5	IN2	1	1.30			1oz	1.25		3.3	3.3	3.5	3.8				3.5	3.8
	PP		3.30	±0.709	3.2	106 x 2	3.30	3.20	3.3/50.44		3.5/3.8/88.77	3.75/3.55/85.08	-0.499	-0.862	-1.044	3.5/8/96.28	
6	GND2	1	1.30			1oz	1.25										
	CORE		3.50	±0.709	3.2	3.5mil(3313)	3.50	3.20									
7	IN3	1	1.30			1oz	1.25		3.3	3.3	3.5	3.8				3.5	3.8
	PP		3.30	±0.709	3.2	106 x 2	3.30	3.20	3.3/50.44		3.5/3.8/88.77	3.75/3.55/85.08	-0.499	-0.862	-1.044	3.5/8/96.28	
8	GND3	1	1.30			1oz	1.25										
	CORE		5.00	±0.984	3.3	5mil(2116)	5.00	3.30									
9	VCC	2	2.60			2oz	2.61										
	PP		19.20	±1.97	3.3	3313 x5	19.73	3.30									
10	VCC1	2	2.60			2oz	2.61										
	CORE		5.00	±0.984	3.3	5mil(2116)	5.00	3.30									
11	GND4	1	1.30			1oz	1.25										
	PP		3.30	±0.709	3.2	106 x 2	3.30	3.20									
12	IN4	1	1.30			1oz	1.25		3.3	3.3	3.5	3.8				3.5	3.8
	CORE		3.50	±0.709	3.2	3.5mil(3313)	3.50	3.20	3.3/50.44		3.5/3.8/88.77	3.75/3.55/85.08	-0.499	-0.862	-1.044	3.5/8/96.28	
13	GND5	1	1.30			1oz	1.25										
	PP		3.30	±0.709	3.2	106 x 2	3.30	3.20									
14	IN5	1	1.30			1oz	1.25		3.3	3.3	3.5	3.8				3.5	3.8
	CORE		3.50	±0.709	3.2	3.5mil(3313)	3.50	3.20	3.3/50.44		3.5/3.8/88.77	3.75/3.55/85.08	-0.499	-0.862	-1.044	3.5/8/96.28	
15	GND6	1	1.30			1oz	1.25										
	PP		3.30	±0.709	3.2	106 x 2	3.30	3.20									
16	IN6	1	1.30			1oz	1.25		3.3	3.3	3.5	3.8				3.5	3.8
	CORE		3.50	±0.709	3.2	3.5mil(3313)	3.50	3.20	3.3/50.44		3.5/3.8/88.77	3.75/3.55/85.08	-0.499	-0.862	-1.044	3.5/8/96.28	
17	GND7	1	1.30			1oz	1.25										
	PP		3.00	±0.709	3.2	1080	3.10	3.20									
18	BOTTOM	0.5+plating	1.95			0.5oz+plating	1.90		5.6	5.6	5.8	7.2				3.5	3.8
	Soldermask		0.60		3.8	SM	0.50		5.6/50.05		5.8/7.2/88.89	6.25/6.75/84.99	-0.554	-1.004	-1.229	3.5/8/111.94	

Figure 6-10 GPU Baseboard Stackup

STACKUP						Target Z (ohms) - MicroStrip	50		85		100		Breakout	
						Target Z (ohms) - StripLine	50	Breakout	85		100			
						Z tolerance	±10%		±10%		±10%			
						Z Type	Single	Single	Differential		Differential		Differential	
Layer#	Description	Copper Weight (oz)	Thickness (mil)	Tolerance (mil)	Glass Fabric	Er	Width	Width	Width	Space	Width	Space	Width	Space
	Soldermask		0.60			3.8								
1	TOP	0.5+plating	1.95				5.6	5.6	5.8	7.2	4.2	9	3.5	3.8
	PP		3.00	±0.709	1086x1	3.5								
2	GND	1	1.30											
	CORE		3.50	±0.709	3313x1	3.6								
3	IN1	1	1.30				3.3	3.3	3.5	3.8	4.2	8	3.5	3.8
	PP		3.30	±0.709	106x2	3.5								
4	GND1	1	1.30											
	CORE		3.50	±0.709	3313x1	3.6								
5	IN2	1	1.30				3.3	3.3	3.5	3.8			3.5	3.8
	PP		3.30	±0.709	106x2	3.5								
6	GND2	1	1.30											
	CORE		3.50	±0.709	3313x1	3.6								
7	IN3	1	1.30				3.3	3.3	3.5	3.8	NA	NA	3.5	3.8
	PP		3.30	±0.709	106x2	3.5								
8	GND3	1	1.30											
	CORE		4.00	±0.709	1060x2	3.6								
9	VCC	2 (RTF)	2.60											
	PP		9.00	±1.5	1086x1 + 2116x1 + 1086x1	3.6								
10	VCC1	2 (RTF)	2.60											
	CORE		4.00	±0.709	1060x2	3.6								
11	GND4	1	1.30											
	PP		3.30	±0.709	106x2	3.5								
12	IN4	1	1.30				3.3	3.3	3.5	3.8	NA	NA	3.5	3.8
	CORE		3.50	±0.709	3313x1	3.6								
13	GND5	1	1.30											
	PP		3.30	±0.709	106x2	3.5								
14	IN5	1	1.30				3.3	3.3	3.5	3.8			3.5	3.8
	CORE		3.50	±0.709	3313x1	3.6								
15	GND6	1	1.30											
	PP		3.30	±0.709	106x2	3.5								
16	IN6	1	1.30				3.3	3.3	3.5	3.8	4.2	8	3.5	3.8
	CORE		3.50	±0.709	3313x1	3.6								
17	GND7	1	1.30											
	PP		3.00	±0.709	1086x1	3.5								
18	BOTTOM	0.5+plating	1.95				5.6	5.6	5.8	7.2	4.2	9	3.5	3.8
	Soldermask		0.6			3.8								
		Total	92.30	±10%										

Figure 6-11 Middle Plane Board Stackup

Bus						RST / SMBUS / Default	PCIe / CLOCK	CLOCK
Z Type						Single	Differential	Differential
Freq.(MHz)								
Target Z (ohms)						50	85	100
Z tolerance						Outer Layer ± 10% / Inner Layer ± 10%	Outer Layer ± 10% / Inner Layer ± 10%	Outer Layer ± 10% / Inner Layer ± 10%
Layer	Lyr Type	Finished Cu Wt	Thickness(mils)	Tolerance	Er	Trace / Space	Trace / Space / Trace	Trace / Space / Trace
		Soldermask	0.50	+/- 0.5 mil	3.8			
1	TOP	0.5 oz+Platting	1.9	+/- 0.8 mil		4	4.9 / 7.1 / 4.9	4.1 / 14 / 4.1
		Prepreg	2.70	+/- 1 mil	3.7			
2	GND1	1 oz	1.3			GND	GND	GND
		Core	4.00	+/- 1 mil	3.8			
3	IN1	1 oz	1.30			4.5	4.9 / 6.6 / 4.9	4.1 / 10 / 4.1
		Prepreg	15.00	+/- 5 mil	4.2			
4	GND/VCC	2 oz	2.60			VCC/GND	VCC/GND	VCC/GND
		Core	4.00	+/- 1 mil	3.8			
5	GND/VCC	2 oz	2.6			VCC/GND	VCC/GND	VCC/GND
		Prepreg	15.00	+/- 5 mil	4.2			
6	IN2	1 oz	1.30			4.5	4.9 / 6.6 / 4.9	4.1 / 10 / 4.1
		Core	4.00	+/- 1 mil	3.8			
7	GND2	1 oz	1.3			VCC/GND	VCC/GND	VCC/GND
		Prepreg	2.70	+/- 1 mil	3.7			
8	BOT	0.5 oz+Platting	1.9	+/- 0.8 mil		4	4.9 / 7.1 / 4.9	4.1 / 14 / 4.1
		Soldermask	0.50	+/- 0.5 mil	3.8			
Total Thickness			62.60	+8/-5				

Figure 6-12 Host Retimer Card Stackup

Bus						RST / SMBUS / Default	PCIe / CLOCK	CLOCK
Z Type						Single	Differential	Differential
Freq.(MHz)								
Target Z (ohms)						50	85	100
Z tolerance						Outer Layer ± 15% / Inner Layer ± 10%	Outer Layer ± 15% / Inner Layer ± 10%	Outer Layer ± 15% / Inner Layer ± 10%
Layer	Lyr Type	Finished Cu Wt	Thickness(mils)	Tolerance	Er	Trace / Space	Trace / Space / Trace	Trace / Space / Trace
		Soldermask	0.50	+/- 0.5 mil	3.8			
1	TOP	0.5 oz+Platting	1.9	+/- 0.8 mil		4	4.9 / 7.1 / 4.9	4.1 / 14 / 4.1
		Prepreg	2.70	+/- 1 mil	3.7			
2	GND1	1 oz	1.3			GND	GND	GND
		Core	4.00	+/- 1 mil	3.8			
3	IN1	1 oz	1.30			4.5	4.9 / 6.6 / 4.9	4.1 / 10 / 4.1
		Prepreg	15.00	+/- 5 mil	4.2			
4	GND/VCC	2 oz	2.60			VCC/GND	VCC/GND	VCC/GND
		Core	4.00	+/- 1 mil	3.8			
5	GND/VCC	2 oz	2.6			VCC/GND	VCC/GND	VCC/GND
		Prepreg	15.00	+/- 5 mil	4.2			
6	IN2	1 oz	1.30			4.5	4.9 / 6.6 / 4.9	4.1 / 10 / 4.1
		Core	4.00	+/- 1 mil	3.8			
7	GND2	1 oz	1.3			VCC/GND	VCC/GND	VCC/GND
		Prepreg	2.70	+/- 1 mil	3.7			
8	BOT	0.5 oz+Platting	1.9	+/- 0.8 mil		4	4.9 / 7.1 / 4.9	4.1 / 14 / 4.1
		Soldermask	0.50	+/- 0.5 mil	3.8			
Total Thickness			62.60	+8/-5				

Figure 6-13 Bridge Card W/O Retimer Stackup

STACKUP											
				Target Z (ohms) - MicroStrip		50	Breakout	100		Breakout	
				Target Z (ohms) - StripLine							
				Z tolerance		±10%		±10%			
				Z Type		Single	Single	Differential		Differential	
Layer#	Description	Copper Weight (oz)	Thickness (mil)	Tolerance (mil)	Er	Width	Width	Width	Space	Width	Space
	Soldermask		0.60		3.8						
1	TOP	0.5+plating	1.95			5.5	4	5	13	3.9	4.1
	PP		3.70	±0.709	4.1						
2	VCC	2	2.60								
	CORE		45.30	±5.12	5						
3	GND	2	2.60								
	PP		3.70	±0.709	4.1						
4	BOTTOM	0.5+plating	1.95			5.5	4	5	13	3.9	4.1
	Soldermask		0.60		3.8						
		Total	63.00	±10%							

Figure 6-14 IO Board Stackup

6.4 JBOG BMC INTERFACE TO HOST

There are two interfaces from JBOG BMC to Host as below; JBOG BMC FW can be updated from below 2 paths.

1. I2C/IPMB bus to Host BMC.
2. PCIe x1 to Host CPU.

6.5 BIG BASIN CLOCK DIAGRAM

6.5.1 Middle Plane Board Clock Diagram

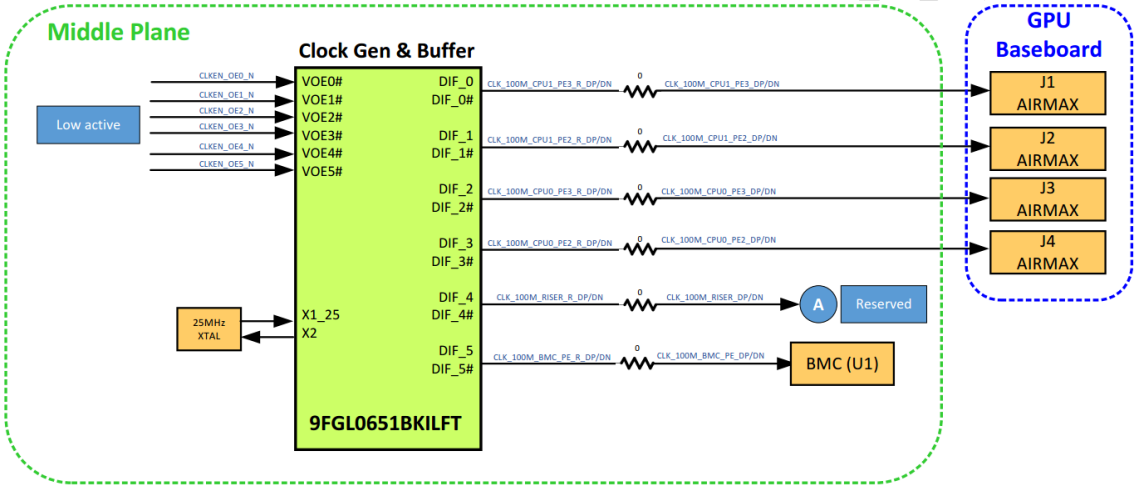


Figure 6-15 Middle Plane Board Clock Diagram

6.5.2 GPU Baseboard Clock Diagram

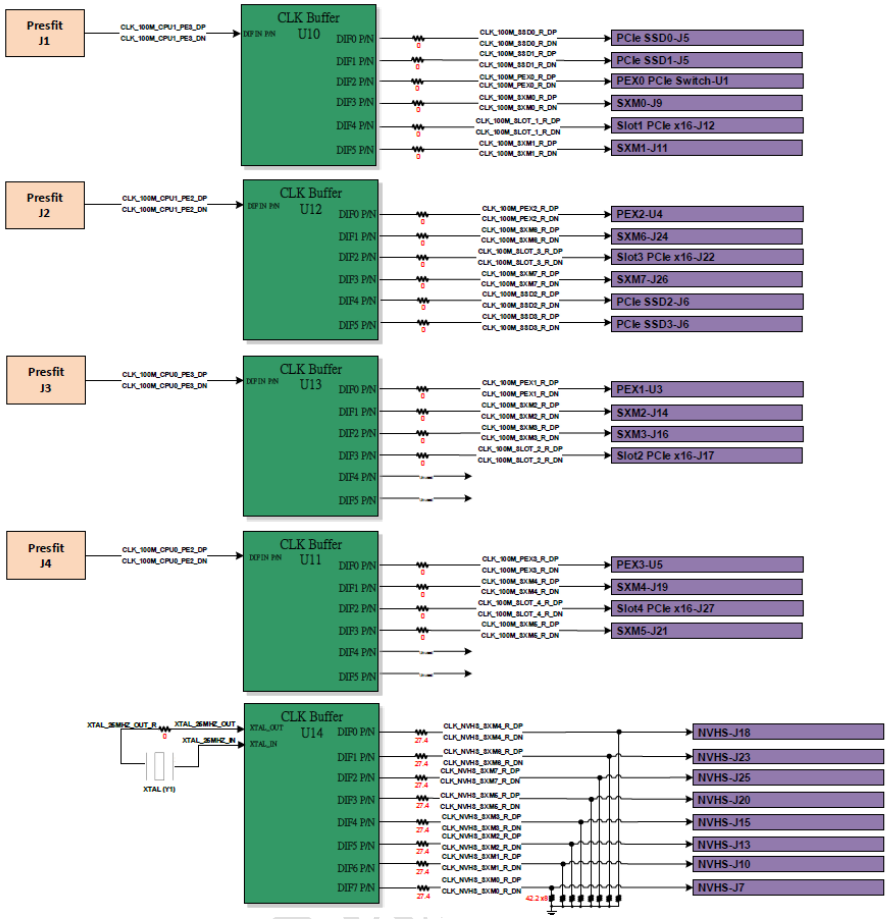


Figure 6-16 GPU Baseboard Clock Diagram

6.6 CPLD

The Big Basin utilizes lattice CPLD LCMXO2-2000HC-4TG100CTR solution on the middle plane board, and provides some features as below.

1. System power control and monitoring
2. Reset control
3. Fan LED control

6.7 DEBUG

6.7.1 OCP V1 Debug Header (J37 on IO Board)

The debug header is to connect OCP Standard debug card.

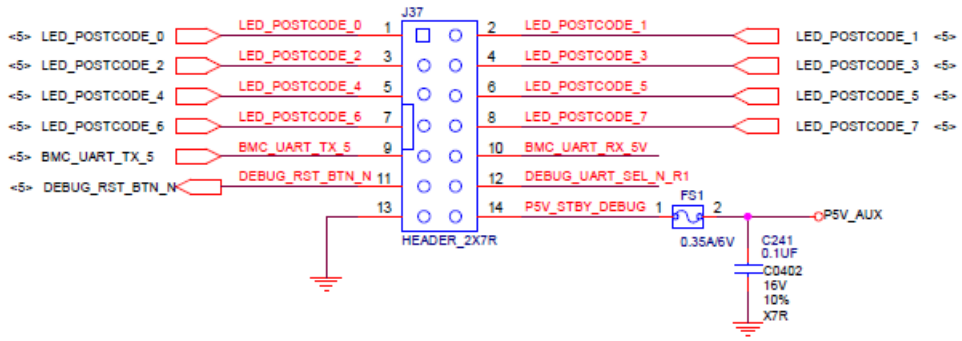


Figure 6-17 OCP V1 Debug Header

6.7.2 OCP V2 Debug Header (J39 on IO Board)

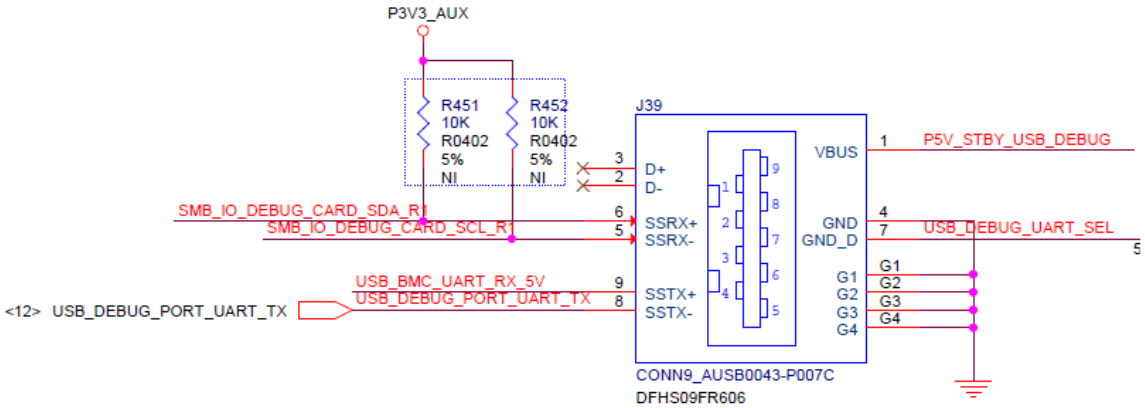


Figure 6-18 OCP V2 Debug Header

6.8 TEMPERATURE SENSORS

6.8.1 GPU Baseboard Temperature Sensor

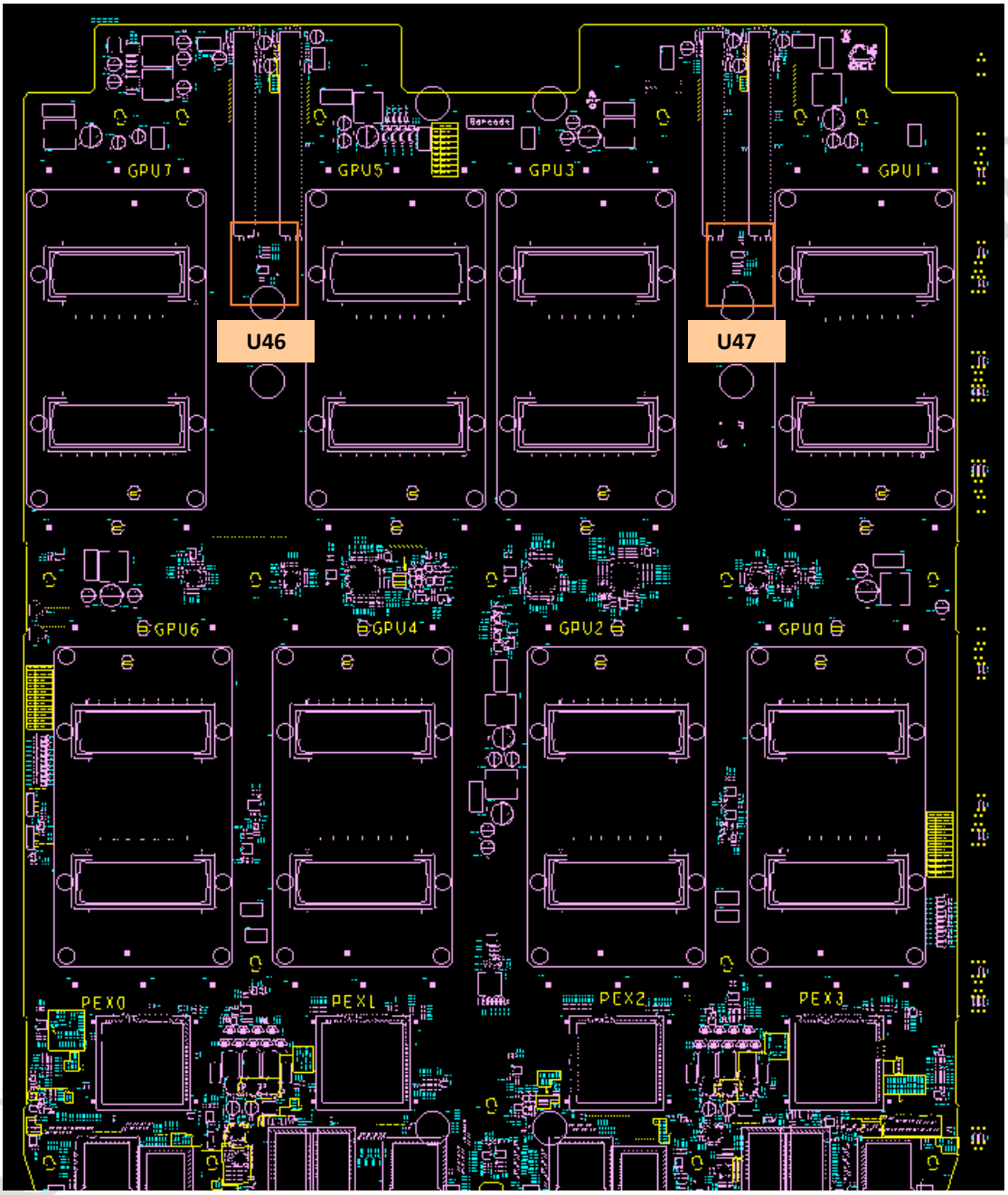


Figure 6-19 GPU Baseboard Temperature Sensor Location

Table 6-3 GPU Baseboard Temperature Sensor List

Device	Part Ref	Implementation
TMP75	U46	Temp Inlet sensor

	U47	Temp Inlet sensor

6.8.2 IO Board Temperature Sensor

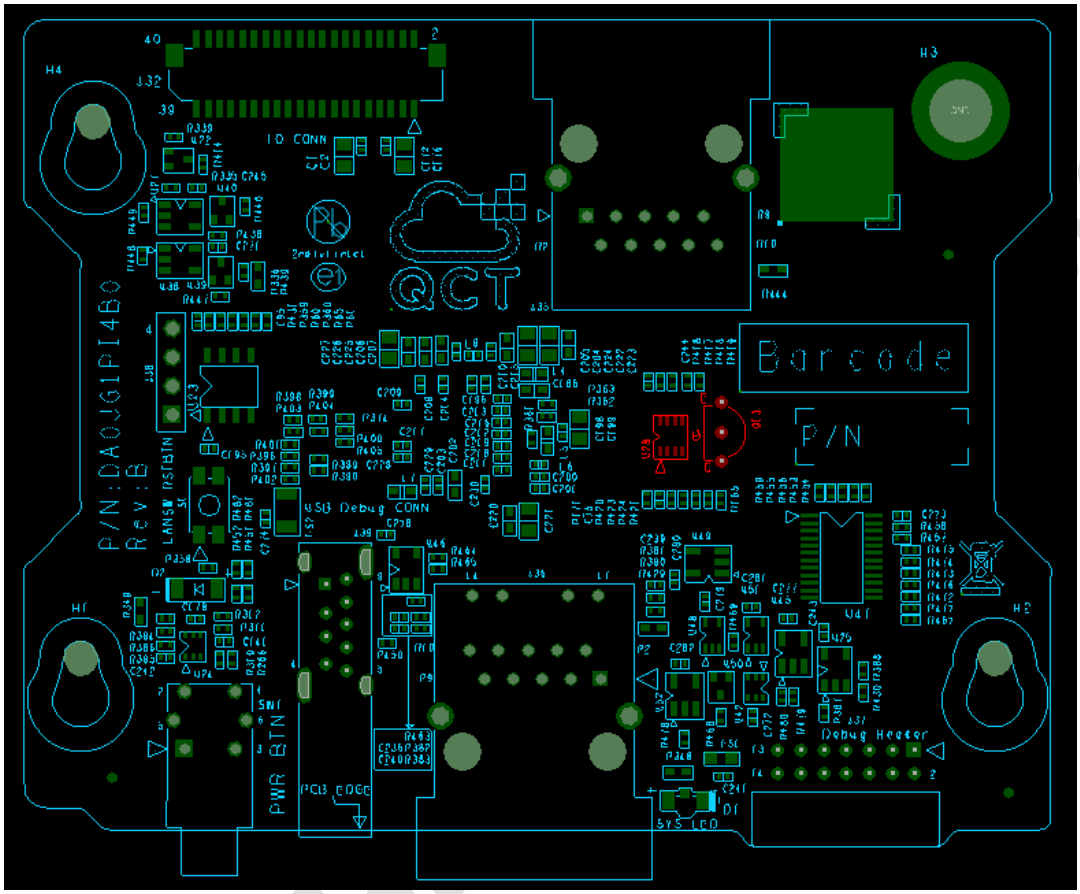


Figure 6-20 IO Board Temperature Sensor Location

Table 6-4 IO Board Temperature Sensor List

Device	Part Ref	Implementation
TMP421	U28	Temp Inlet sensor

6.9 BMC VOLTAGE SENSORS

The voltage sensors are on the JBOG BMC AST2500.

Table 6-5 AST2500 Pin Definition for Voltage Monitor

Pin Number	Pin Name	Implementation
F4	ADC0	P12V_AUX_SCALED
F5	ADC1	P3V3_AUX_SCALED
F2	ADC2	P5V_AUX_SCALED
E1	ADC3	P12V_1_SCALED
F3	ADC4	P12V_2_SCALED
E3	ADC5	GND
G5	ADC6	P12V_SSD_SCALED
G4	ADC7	P3V3_SCALED
F2	ADC8	P3V_BAT_SCALED
G3	ADC9	P12V_FAN_0_SCALED
G2	ADC10	P12V_FAN_1_SCALED
F1	ADC11	P12V_FAN_2_SCALED
H5	ADC12	P12V_FAN_3_SCALED
G1	ADC13	GND
H3	ADC14	GND
H4	ADC15	GND

6.10 SMBUS BLOCK DIAGRAM

This section outlines the platform system specific SMBUS topologies and interconnects.

6.10.1 Middle Plane Board SMBUS Block Diagram

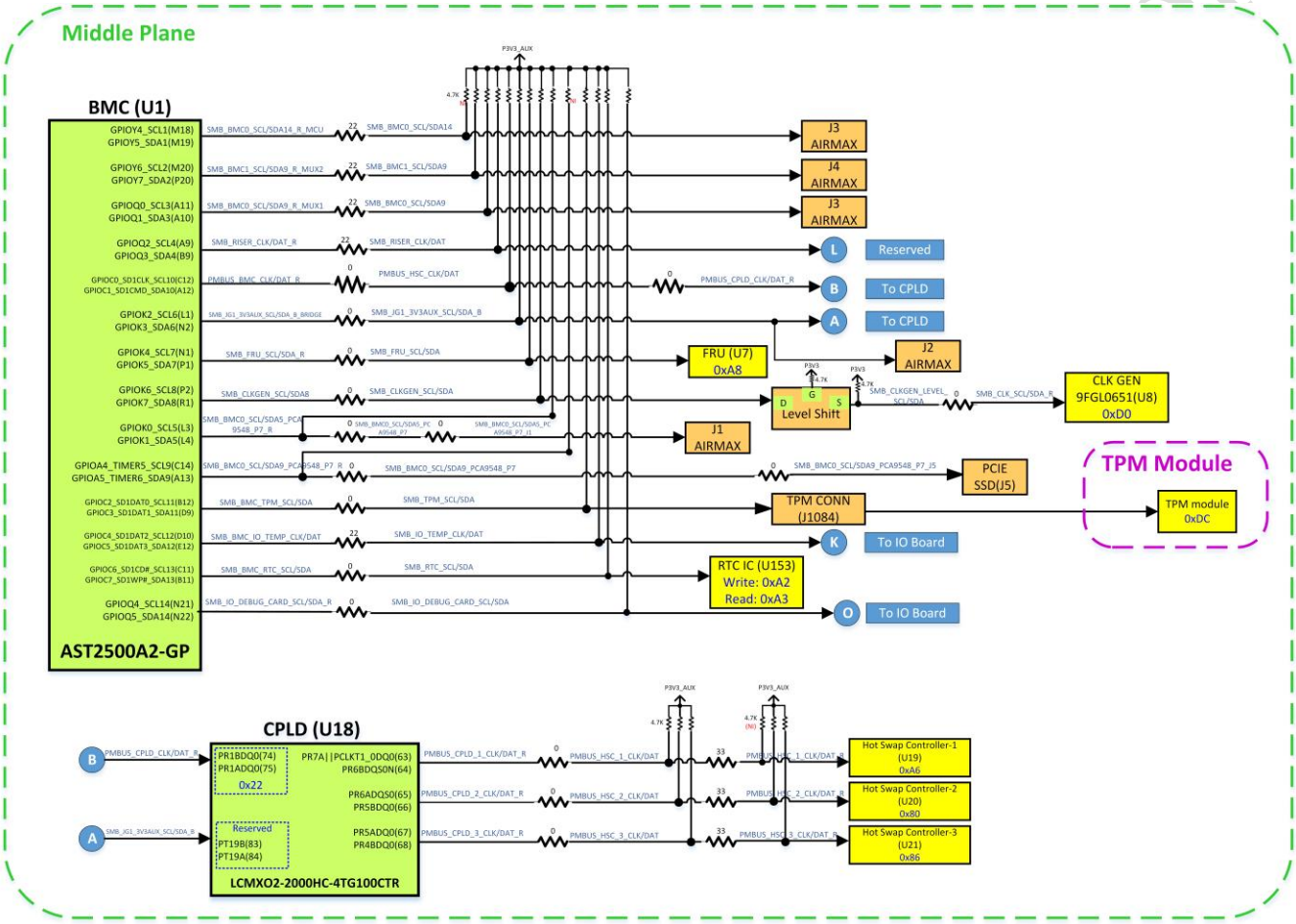


Figure 6-21 Middle Plane Board SMBUS Block Diagram

6.10.2 GPU Baseboard SMBUS Block Diagram

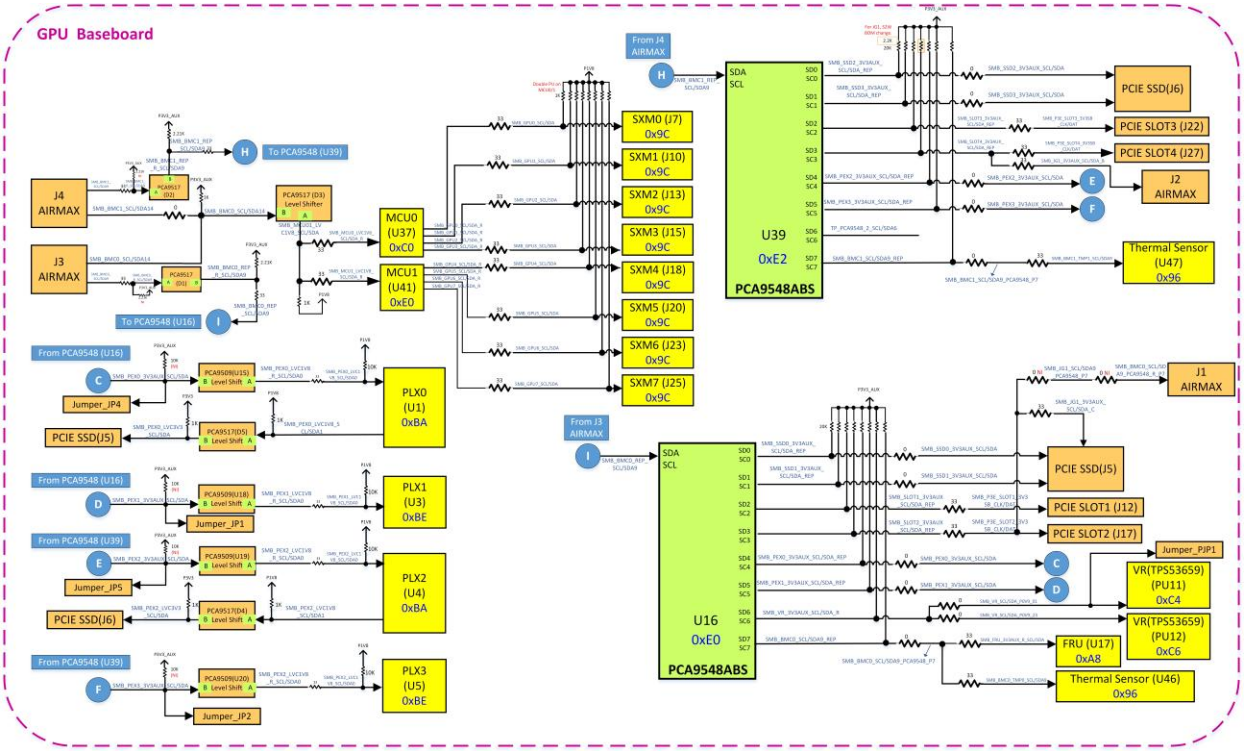


Figure 6-22 GPU Baseboard SMBUS Block Diagram

6.10.3 Bridge Card W/O Retimer SMBUS Block Diagram

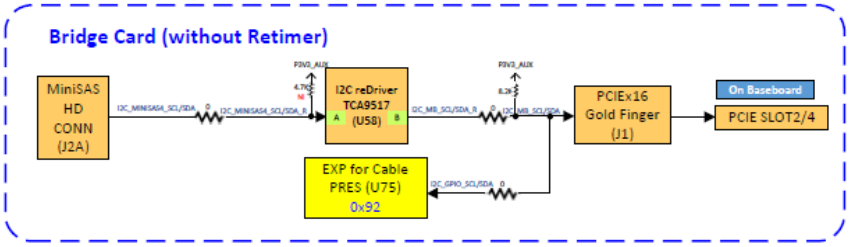


Figure 6-23 Bridge Card W/O Retimer SMBUS Block Diagram

6.10.4 Host Retimer Card SMBUS Block Diagram

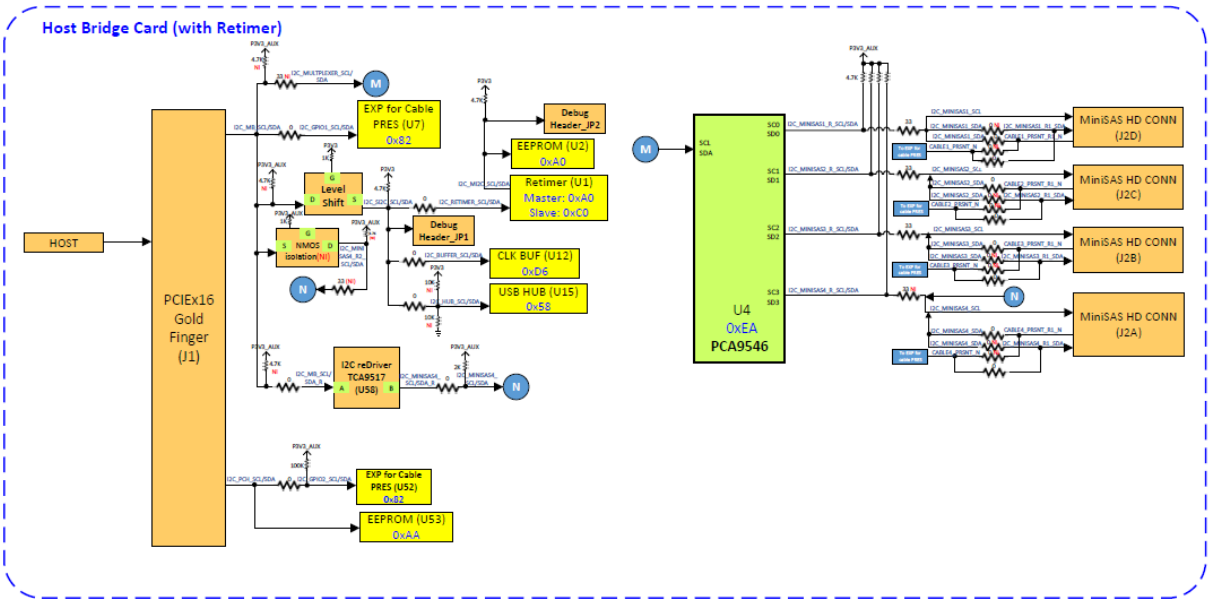


Figure 6-24 Host Retimer Card SMBUS Block Diagram

6.10.5 IO Board SMBUS Block Diagram

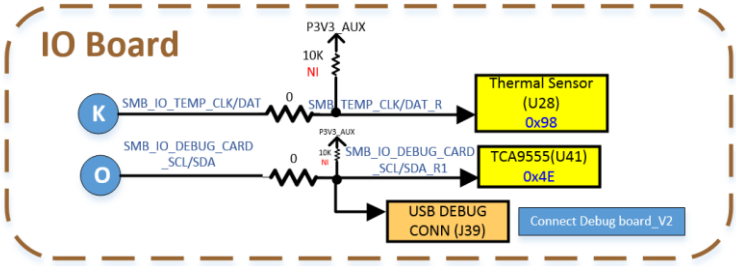


Figure 6-25 IO Board SMBUS Block Diagram

6.11 POWER BUTTON

There is a power button on the IO board for toggling system power.

6.12 SYSTEM LED DEFINITION

6.12.1 Power, Status LEDs (IO Board)

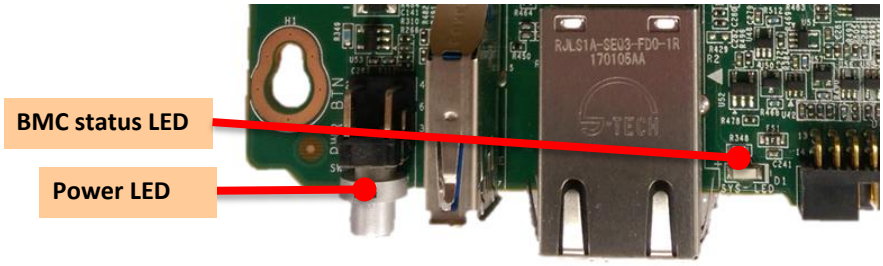


Figure 6-26 Big Basin Power Button and Status LED Location

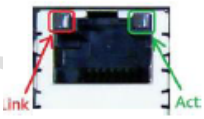
Table 6-6 Big Basin Power LED Behavior

Name	Color	DC Power	System ID	Behavior
Power LED	Blue	OFF	NO	Always OFF
		OFF	YES	On 0.1sec, off for 0.9sec, and loop
		ON	NO	Always ON
		ON	YES	On 0.9sec, off for 0.1sec, and loop

Table 6-7 Big Basin BMC Status LED Behavior

Name	Color	BMC Ready	System Log	Behavior
BMC Status LED	Blue / Orange	NO	x	OFF
		YES	NO	Blue Solid
		YES	YES	Orange Blink

6.12.2 Dedicated RJ-45 MNG Function and Behavior



	Link (Left)	Activity(Right)
Unplug	Dark	Dark
1 G Link with Active	Amber	Green blinking
100M Link with Active	Green	Green blinking
10 M Link with Active	Dark	Green blinking

6.12.3 Error Code Debug LED

Table 6-8 Error Code Debug LED List

Error Code	Description
00	No error
01	No battery detect
02	No TPM detect
03	RTC fail
04	Battery low
05	HSC 1 alert
06	HSC 2 alert
07	HSC 3 alert
08	Fan 0 not detect
09	Fan 1 not detect
0A	Fan 2 not detect
0B	Fan 3 not detect
0C	No BMC PCIe cable detect
0D	No IO cable detect
0E	NA
0F	NA
10	I2C bus 0 fail
11	I2C bus 1 fail
12	I2C bus 2 fail
13	I2C bus 3 fail
14	I2C bus 4 fail
15	I2C bus 5 fail
16	I2C bus 6 fail
17	I2C bus 7 fail
18	I2C bus 8 fail
19	I2C bus 9 fail
1A	I2C bus 10 fail
1B	I2C bus 11 fail
1C	I2C bus 12 fail
1D	I2C bus 13 fail
1E – 2F	NA
30	GPGPU0 overheat
31	GPGPU1 overheat
32	GPGPU2 overheat
33	GPGPU3 overheat
34	GPGPU4 overheat
35	GPGPU5 overheat
36	GPGPU6 overheat
37	GPGPU7 overheat

38 – 3F	NA
40	P12V_AUX voltage sensor critical
41	P3V3_AUX voltage sensor critical
42	P5V_AUX voltage sensor critical
43	P12V_1 voltage sensor critical
44	P12V_2 voltage sensor critical
45	P12V_FAN_0 voltage sensor critical
46	P12V voltage sensor critical
47	P3V3 voltage sensor critical
48	P3V_BAT voltage sensor critical
49	P12V_FAN_1 voltage sensor critical
4A	P12V_FAN_2 voltage sensor critical
4B	P12V_FAN_3 voltage sensor critical
4C	NA
4D	NA
4E	NA
4F	NA
50	PCIe switch PEX0 uncorrectable error
51	PCIe switch PEX1 uncorrectable error
52	PCIe switch PEX2 uncorrectable error
53	PCIe switch PEX3 uncorrectable error
54	PCIe switch PEX0 internal Temp critical
55	PCIe switch PEX1 internal Temp critical
56	PCIe switch PEX2 internal Temp critical
57	PCIe switch PEX3 internal Temp critical
58 – 5F	NA
60	SMART temp critical
61	SMART temp critical
62	SMART temp critical
63	SMART temp critical
64	Fault
65	Fault
66	Fault
67	Fault
68 – 6F	NA
70	Inlet Temp sensorUNC (IO board)
71	Inlet Temp sensorUC (IO board)
72	PCIE inlet temperature sensor 1 UNC(baseboard)
73	PCIE inlet temperature sensor 1 UC(baseboard)
74	PCIE inlet temperature sensor 2 UNC(baseboard)
75	PCIE inlet temperature sensor 2 UC(baseboard)
76 – 7F	NA
80	SEL full
81 – 8F	NA

90	FAN 00 lower critical
91	FAN 01 lower critical
92	FAN 10 lower critical
93	FAN 11 lower critical
94	FAN 20 lower critical
95	FAN 21 lower critical
96	FAN 30 lower critical
97	FAN 31 lower critical
98 – 9F	NA
A0	HSC0 Temp UNC
A1	HSC0 Temp UC
A2	HSC0 input voltage UNC
A3	HSC0 input voltage NC
A4	HSC0 input power UNC
A5	HSC0 input power UC
A6	SC0 output voltage UNC
A7	HSC0 output voltage NC
A8	HSC0 output current UNC
A9	HSC0 output current UC
AA	HSC1 Temp UNC
AB	HSC1 Temp UC
AC	HSC1 input voltage UNC
AD	HSC1 input voltage NC
AE	HSC1 input power UNC
AF	HSC1 input power UC
B0	HSC1 output voltage UNC
B1	HSC1 output voltage NC
B2	HSC1 output current UNC
B3	HSC1 output current UC
B4	HSC2 Temp UNC
B5	HSC2 Temp UC
B6	HSC2 input voltage UNC
B7	HSC2 input voltage NC
B8	HSC2 input power UNC
B9	HSC2 input power UC
BA	HSC2 output voltage UNC
BB	HSC2 output voltage NC
BC	HSC2 output current UNC
BD	HSC2 output current UC
BE	Throttle Alert
BF - FF	NA

6.12.4 FAN LED

Table 6-9 Fan LED Behavior

Name	Color	Condition	Behavior
FAN LED	Blue	On	Normal work
		Off	No power
	Red	On	FAN speed lower than threshold
		Off	Normal work

6.12.5 PCIe Host Retimer Card LED

Table 6-10 PCIe Host Retimer Card LED Definition

LED	PCIE BIFURCATION		
	X16	X8	X4
D4	GREEN	ORANGE	ORANGE
D3	ORANGE	GREEN	ORANGE
D2	ORANGE	ORANGE	GREEN

Figure 6-27 PCIe Host Retimer Card LED Location

6.13 CONNECTORS AND HEADERS OVERVIEW

6.13.1 Middle Plane Board Connector

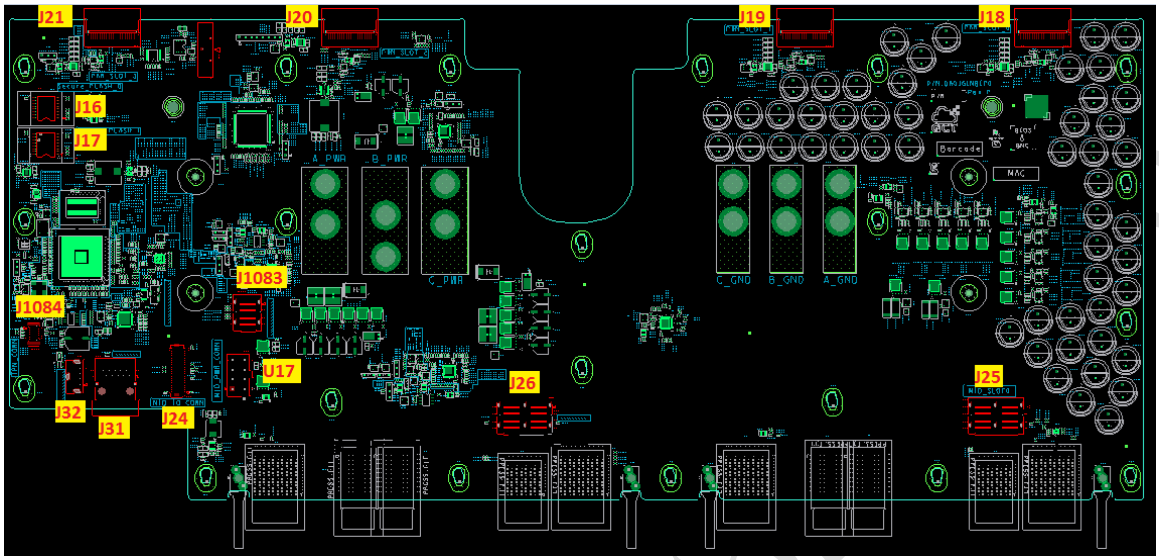


Figure 6-28 Middle Plane Board Connector Location

Table 6-11 Middle Plane Board Connector List

Location	Silkscreen	Description
J18	FAN_SLOT_0	FAN connector
J19	FAN_SLOT_1	FAN connector
J20	FAN_SLOT_2	FAN connector
J21	FAN_SLOT_3	FAN connector
J16	Secure_FLASH_0	BMC flash0 socket
J17	Normal_FLASH_1	BMC flash1 socket
J1084	TPM_CONN	TPM connector
J32	USB_1D1_HOST	BMC USB connector
J31	MID_RJ45	BMC MNG RJ-45 port
U17	MID_PWR_CONN	Power connector
J24	MID_IO_CONN	IO board connector
BT1	BT1	Battery connector
J1083	MID_PCIE_BMC	BMC PCIe connector
J25	MID_SLOT0	PCIe connector
J26	MID_SLOT1	PCIe connector

6.13.2 Host Retimer Card Connector and Jumper

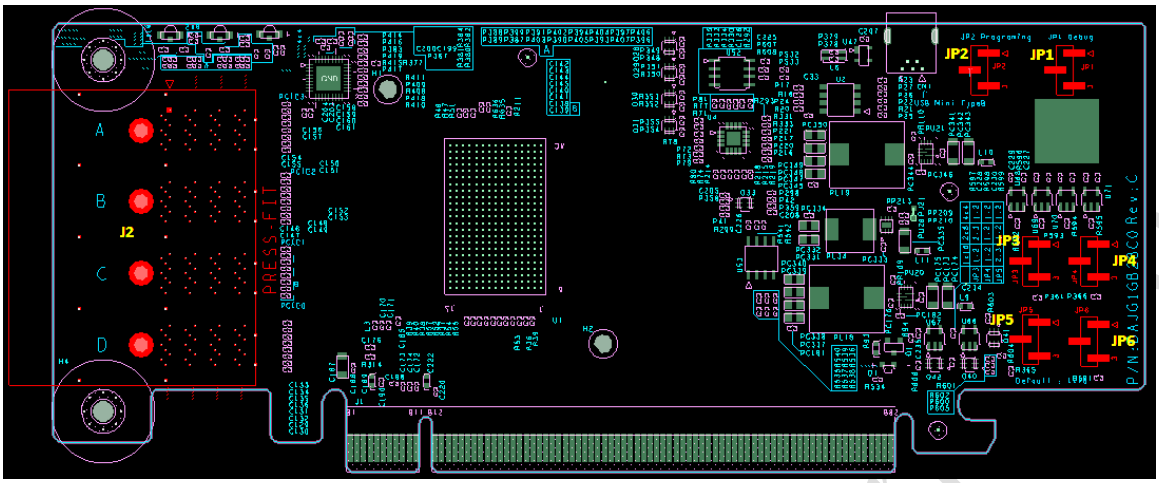


Figure 6-29 Host Retimer Card Connector and Jumper Location

Table 6-12 Host Retimer Card Connector List

Location	Silkscreen	Description
J2	J2	MiniSAS HD Connector
JP1	JP1	IDT Retimer Slave SMBus debug connector
JP2	JP2	IDT Retimer Master SMBus debug connector
JP3	JP3	SLOT_PRSNT_N_24 pin
JP4	JP4	SLOT_PRSNT_N_23 pin
JP5	JP5	SLOT_PRSNT_N_22 pin
JP6	JP6	SLOT_PRSNT_N_21 pin

6.14 JUMPER DEFINITION

6.14.1 Jumper Settings of Host Retimer Card for System PCIe Topologies

The purpose of headers is to configure the PCIe bus width of Host.

Table 6-13 Host Retimer Card Jumper Settings

	1x16 (Topology1)	2x8 (Topology2)	4x4
JP3	1-2	2-3	1-2
JP4	1-2	1-2	1-2
JP5	2-3	1-2	1-2

Figure 6-30 Host Retimer Card Jumpers Location

6.15 INTERNAL CONNECTOR PINOUT

6.15.1 J18-FAN_SYS_0 Connector

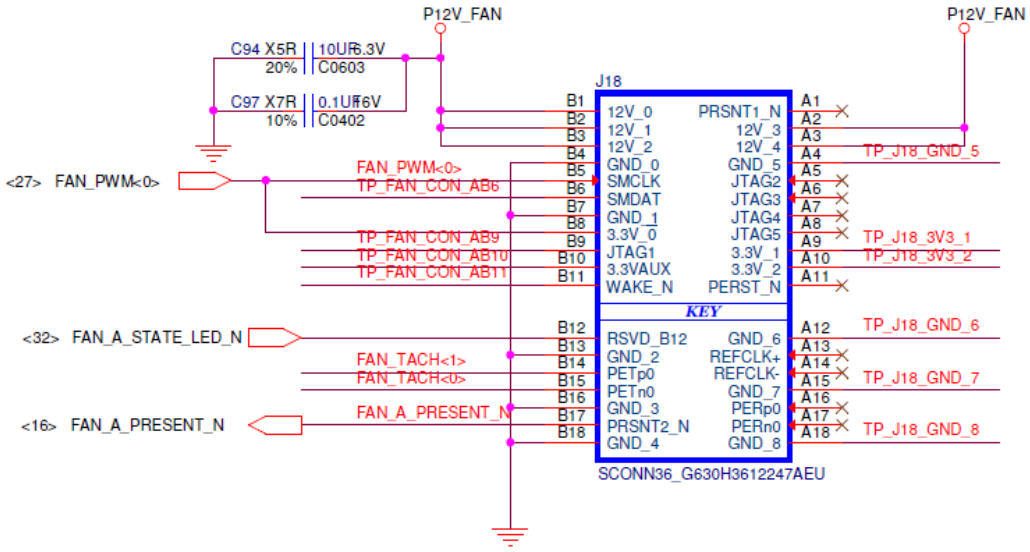


Figure 6-31 J18-FAN_SYS_0 Connector Schematic

Table 6-14 J18-FAN_SYS_0 Connector Pin Definition

Pin	Single name	Pin	Single name
A1		B1	P12V_FAN
A2	P12V_FAN	B2	P12V_FAN
A3	P12V_FAN	B3	P12V_FAN
A4	TP_J18_GND_5	B4	GND
A5		B5	FAN_PWM<0>
A6		B6	TP_FAN_CON_AB6
A7		B7	GND
A8		B8	FAN_PWM<0>
A9	TP_J18_3V3_1	B9	TP_FAN_CON_AB9
A10	TP_J18_3V3_2	B10	TP_FAN_CON_AB10
A11		B11	TP_FAN_CON_AB11
A12	TP_J18_GND_6	B12	FAN_A_STATE_LED_N
A13		B13	GND
A14		B14	FAN_TACH<1>
A15	TP_J18_GND_7	B15	FAN_TACH<0>
A16		B16	GND
A17		B17	FAN_A_PRESENT_N

A18	TP_J18_GND_8	B18	GND

6.15.2 J19-FAN_SYS_1 Connector

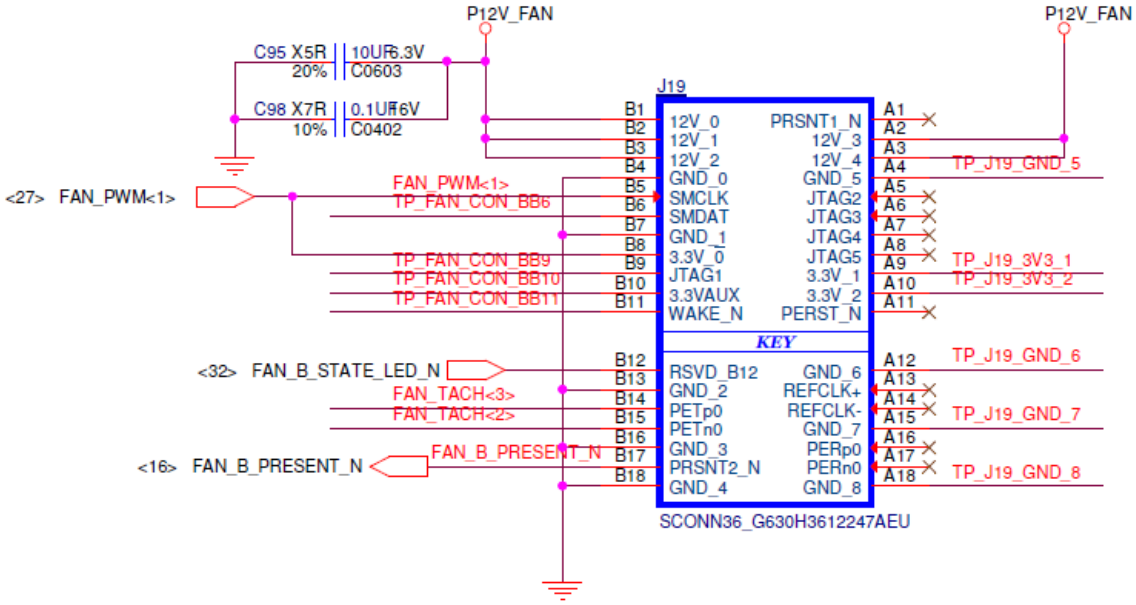


Figure 6-32 J19-FAN_SYS_1 Connector Schematic

Table 6-15 J19-FAN_SYS_1 Connector Pin Definition

Pin	Single name	Pin	Single name
A1		B1	P12V_FAN
A2	P12V_FAN	B2	P12V_FAN
A3	P12V_FAN	B3	P12V_FAN
A4	TP_J19_GND_5	B4	GND
A5		B5	FAN_PWM<1>
A6		B6	TP_FAN_CON_BB6
A7		B7	GND
A8		B8	FAN_PWM<1>
A9	TP_J19_3V3_1	B9	TP_FAN_CON_BB9
A10	TP_J19_3V3_2	B10	TP_FAN_CON_BB10
A11		B11	TP_FAN_CON_BB11
A12	TP_J19_GND_6	B12	FAN_B_STATE_LED_N
A13		B13	GND
A14		B14	FAN_TACH<3>
A15	TP_J19_GND_7	B15	FAN_TACH<2>
A16		B16	GND
A17		B17	FAN_B_PRESENT_N

A18	TP_J19_GND_8	B18	GND

6.15.3 J20-FAN_SYS_2 Connector

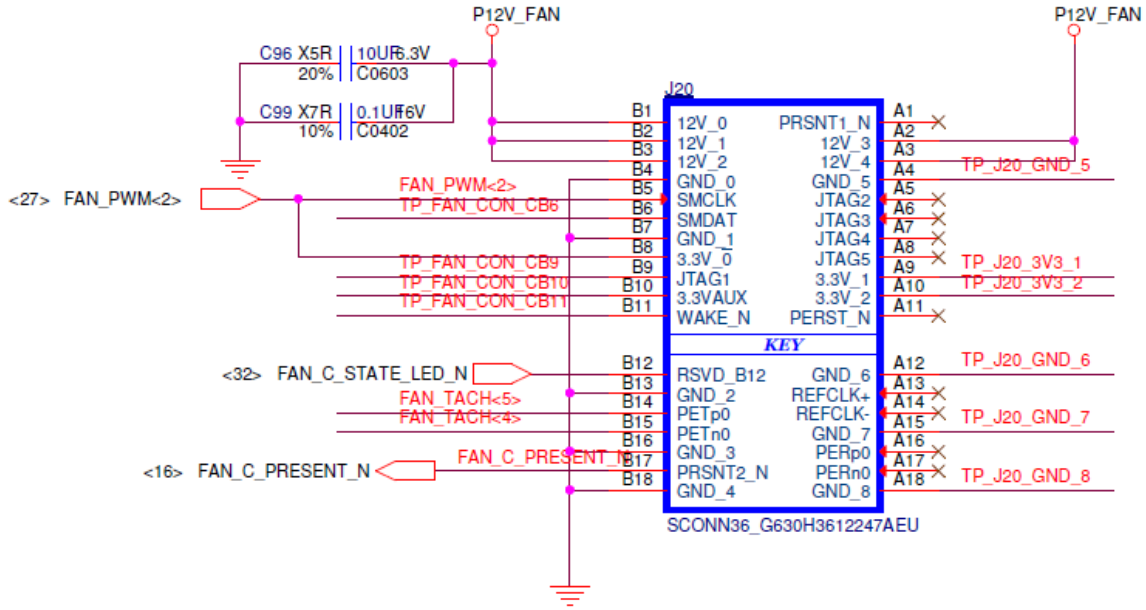


Figure 6-33 J20-FAN_SYS_2 Connector Schematic

Table 6-16 J20-FAN_SYS_2 Connector Pin Definition

Pin	Single name	Pin	Single name
A1		B1	P12V_FAN
A2	P12V_FAN	B2	P12V_FAN
A3	P12V_FAN	B3	P12V_FAN
A4	TP_J20_GND_5	B4	GND
A5		B5	FAN_PWM<2>
A6		B6	TP_FAN_CON_CB6
A7		B7	GND
A8		B8	FAN_PWM<2>
A9	TP_J20_3V3_1	B9	TP_FAN_CON_CB9
A10	TP_J20_3V3_2	B10	TP_FAN_CON_CB10
A11		B11	TP_FAN_CON_CB11
A12	TP_J20_GND_6	B12	FAN_C_STATE_LED_N
A13		B13	GND
A14		B14	FAN_TACH<5>
A15	TP_J20_GND_7	B15	FAN_TACH<4>
A16		B16	GND

A17		B17	FAN_C_PRESENT_N
A18	TP_J20_GND_8	B18	GND

6.15.4 J21-FAN_SYS_3 Connector

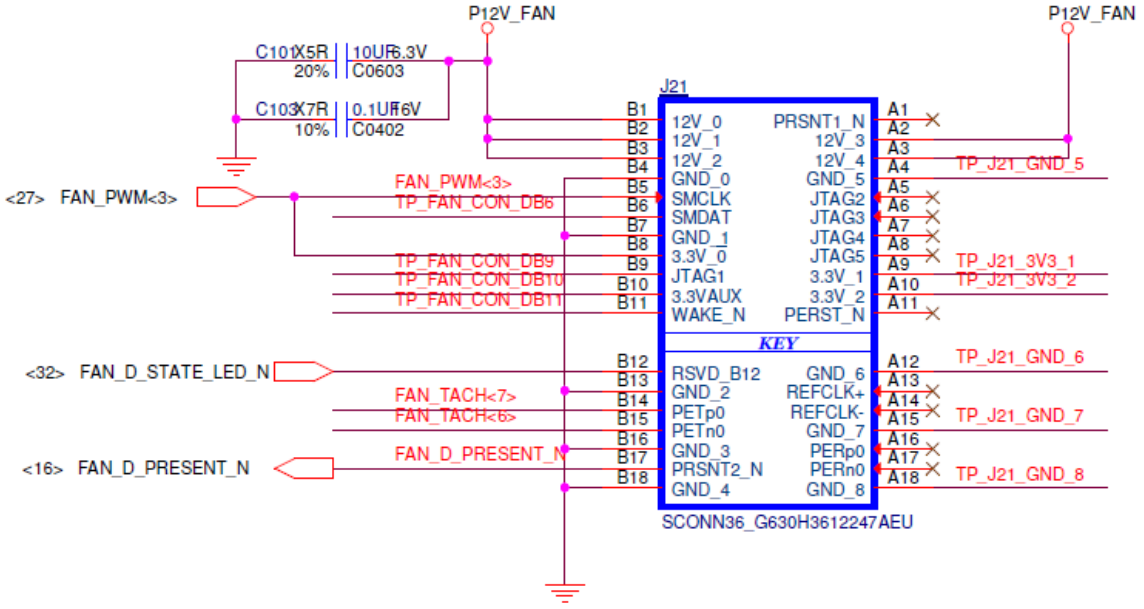


Figure 6-34 J21-FAN_SYS_3 Connector Schematic

Table 6-17 J21-FAN_SYS_3 Connector Pin Definition

Pin	Single name	Pin	Single name
A1		B1	P12V_FAN
A2	P12V_FAN	B2	P12V_FAN
A3	P12V_FAN	B3	P12V_FAN
A4	TP_J21_GND_5	B4	GND
A5		B5	FAN_PWM<3>
A6		B6	TP_FAN_CON_DB6
A7		B7	GND
A8		B8	FAN_PWM<3>
A9	TP_J21_3V3_1	B9	TP_FAN_CON_DB9
A10	TP_J21_3V3_2	B10	TP_FAN_CON_DB10
A11		B11	TP_FAN_CON_DB11
A12	TP_J21_GND_6	B12	FAN_D_STATE_LED_N
A13		B13	GND
A14		B14	FAN_TACH<7>
A15	TP_J21_GND_7	B15	FAN_TACH<6>

A16		B16	GND
A17		B17	FAN_D_PRESENT_N
A18	TP_J21_GND_8	B18	GND

6.15.5 J16-BMC FLASH0 Connector

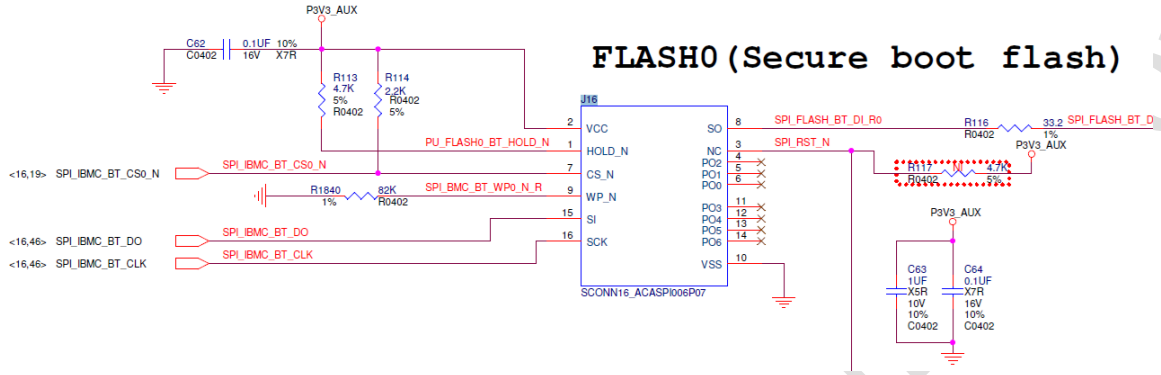


Figure 6-35 J16-BMC FLASH0 Connector Schematic

Table 6-18 J16-BMC FLASH0 Connector Pin Definition

Pin	Single name	Pin	Single name
1	PU_FLASH0_BT_HOLD_N	2	P3V3_AUX
3	SPI_RST_N	4	NC
5	NC	6	NC
7	SPI_IBMC_BT_CS0_N	8	SPI_FLASH_BT_DI_R0
9	SPI_BMC_BT_WP0_N_R	10	GND
11	NC	12	NC
13	NC	14	NC
15	SPI_IBMC_BT_DO	16	SPI_IBMC_BT_CLK

6.15.6 J17-BMC FLASH1 Connector

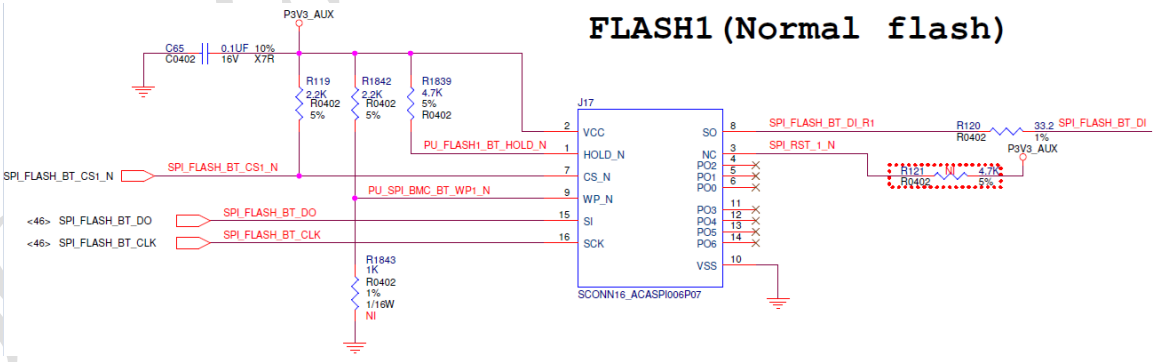


Figure 6-36 J17-BMC FLASH1 Connector Schematic

Table 6-19 J17-BMC FLASH1 Connector Pin Definition

Pin	Single name	Pin	Single name
1	PU_FLASH1_BT_HOLD_N	2	P3V3_AUX
3	SPI_RST_1_N	4	NC
5	NC	6	NC

7	SPI_IBMC_BT_CS1_N	8	SPI_FLASH_BT_DI_R1
9	SPI_BMC_BT_WP1_N_R	10	GND
11	NC	12	NC
13	NC	14	NC
15	SPI_IBMC_BT_DO	16	SPI_IBMC_BT_CLK

6.15.7 J1084_TPM_CONN-TPM Connector

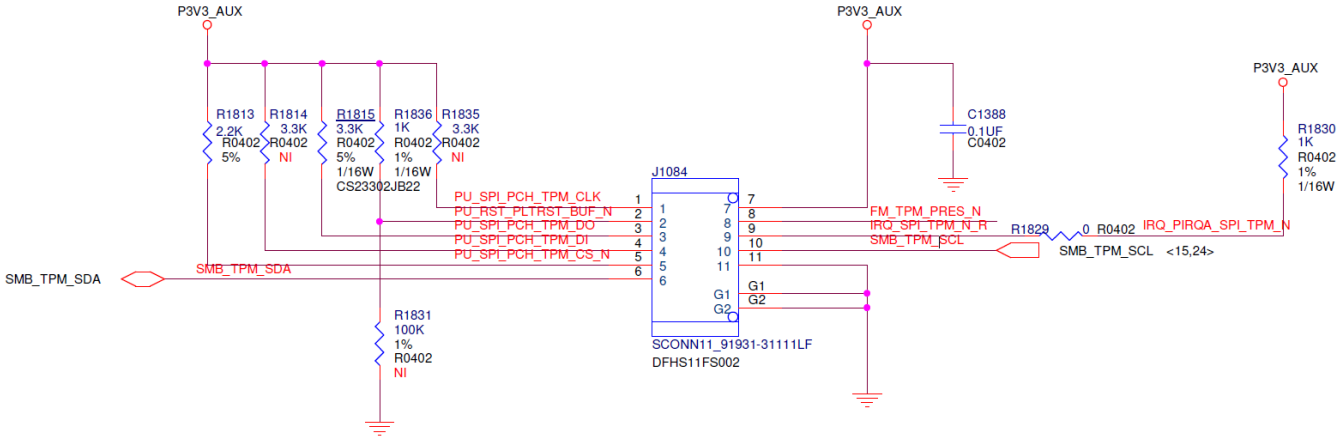


Figure 6-37 J1084_TPM_CONN Schematic

Table 6-20 J1084_TPM_CONN Pin Definition

Pin	Single name	Pin	Single name
1	PU_SPI_PCH_TPM_CLK	2	PU_RST_PLTRST_BUF_N
3	PU_SPI_PCH_TPM_DO	4	PU_SPI_PCH_TPM_DI
5	PU_SPI_PCH_TPM_CS_N	6	SMB_TPM_SDA
7	P3V3_AUX	8	FM_TPM_PRES_N
9	IRQ_SPI_TPM_N_R	10	SMB_TPM_SCL
11	NC		

6.15.8 J25-PCIe SLOT0 Connector

Table 6-21 J25-PCIe SLOT0 Connector Pin Definition

Pin #	Pin Name	Net Name
A1	SB7	CLK_100M_SSDBP_DP
A2	SB0	CLK_100M_SSDBP_DN
A3	GDN1	GND
A4	RX1+	P3E_PEX0_RX_DP<65>
A5	RX1-	P3E_PEX0_RX_DN<65>
A6	GND2	GND
A7	RX3+	P3E_PEX0_RX_DP<67>

A8	RX3-	P3E_PEX0_RX_DN<67>
A9	GDN3	GND
B1	SB3	
B2	SB1	
B3	GND4	GND
B4	RX0+	P3E_PEX0_RX_DP<64>
B5	RX0-	P3E_PEX0_RX_DN<64>
B6	GND5	GND
B7	RX2+	P3E_PEX0_RX_DP<66>
B8	RX2-	P3E_PEX0_RX_DN<66>
B9	GND6	GND
C1	SB4	IRQ_LVC3_W AKE_N
C2	SB2	RST_BUFFER_SSDBP_N
C3	GND7	GND
C4	TX1+	P3E_PEX0_TX_C_DP<65>
C5	TX1-	P3E_PEX0_TX_C_DN<65>
C6	GND8	GND
C7	TX3+	P3E_PEX0_TX_C_DP<67>
C8	TX3-	P3E_PEX0_TX_C_DN<67>
C9	GND9	GND
D1	SB5	PCIE_SLOT0_PRSNT_X4_2_N
D2	SB6	CABLE_DETECT_RISER0
D3	GND10	GND
D4	TX0+	P3E_PEX0_TX_C_DP<64>
D5	TX0-	P3E_PEX0_TX_C_DN<64>
D6	GND11	GND
D7	TX2+	P3E_PEX0_TX_C_DP<66>
D8	TX2-	P3E_PEX0_TX_C_DN<66>
D9	GND12	GND
A10	SB15	
A11	SB8	
A12	GND13	GND
A13	RX5+	P3E_PEX0_RX_DP<69>
A14	RX5-	P3E_PEX0_RX_DN<69>
A15	GND14	GND
A16	RX7+	P3E_PEX0_RX_DP<71>
A17	RX7-	P3E_PEX0_RX_DN<71>
A18	GND15	GND
B10	SB11	SMB_RISER_CLK
B11	SB9	SMB_ RISER _DAT

B12	GND16	GND
B13	RX4+	P3E_PEX0_RX_DP<68>
B14	RX4-	P3E_PEX0_RX_DN<68>
B15	GND17	GND
B16	RX6+	P3E_PEX0_RX_DP<70>
B17	RX6-	P3E_PEX0_RX_DN<70>
B18	GND18	GND
C10	SB12	
C11	SB10	
C12	GND19	GND
C13	TX5+	P3E_PEX0_TX_C_DP<69>
C14	TX5-	P3E_PEX0_TX_C_DN<69>
C15	GND20	GND
C16	TX7+	P3E_PEX0_TX_C_DP<71>
C17	TX7-	P3E_PEX0_TX_C_DN<71>
C18	GND21	GND
D10	SB13	PCIE_SLOT0_PRSNT_X8_2_N
D11	SB14	
D12	GND22	GND
D13	TX4+	P3E_PEX0_TX_C_DP<68>
D14	TX4-	P3E_PEX0_TX_C_DN<68>
D15	GND23	GND
D16	TX6+	P3E_PEX0_TX_C_DP<70>
D17	TX6-	P3E_PEX0_TX_C_DN<70>
D18	GND24	GND

6.15.9 J26-PCIe SLOT1 Connector

Table 6-22 J26-PCIe SLOT1 Connector Pin Definition

Pin #	Pin Name	Net Name
A1	SB7	
A2	SB0	
A3	GDN1	GND
A4	RX1+	P3E_PEX2_RX_DP<65>
A5	RX1-	P3E_PEX2_RX_DN<65>
A6	GND2	GND
A7	RX3+	P3E_PEX2_RX_DP<67>
A8	RX3-	P3E_PEX2_RX_DN<67>
A9	GDN3	GND
B1	SB3	GND

B2	SB1	GND
B3	GND4	GND
B4	RX0+	P3E_PEX2_RX_DP<64>
B5	RX0-	P3E_PEX2_RX_DN<64>
B6	GND5	GND
B7	RX2+	P3E_PEX2_RX_DP<66>
B8	RX2-	P3E_PEX2_RX_DN<66>
B9	GND6	GND
C1	SB4	
C2	SB2	
C3	GND7	GND
C4	TX1+	P3E_PEX2_TX_C_DP<65>
C5	TX1-	P3E_PEX2_TX_C_DN<65>
C6	GND8	GND
C7	TX3+	P3E_PEX2_TX_C_DP<67>
C8	TX3-	P3E_PEX2_TX_C_DN<67>
C9	GND9	GND
D1	SB5	PCIE_SLOT1_PRSNT_X4_2_N
D2	SB6	CABLE_DETECT_RISER1
D3	GND10	GND
D4	TX0+	P3E_PEX2_TX_C_DP<64>
D5	TX0-	P3E_PEX2_TX_C_DN<64>
D6	GND11	GND
D7	TX2+	P3E_PEX2_TX_C_DP<66>
D8	TX2-	P3E_PEX2_TX_C_DN<66>
D9	GND12	GND
A10	SB15	
A11	SB8	
A12	GND13	GND
A13	RX5+	P3E_PEX2_RX_DP<69>
A14	RX5-	P3E_PEX2_RX_DN<69>
A15	GND14	GND
A16	RX7+	P3E_PEX2_RX_DP<71>
A17	RX7-	P3E_PEX2_RX_DN<71>
A18	GND15	GND
B10	SB11	
B11	SB9	
B12	GND16	GND
B13	RX4+	P3E_PEX2_RX_DP<68>
B14	RX4-	P3E_PEX2_RX_DN<68>

B15	GND17	GND
B16	RX6+	P3E_PEX2_RX_DP<70>
B17	RX6-	P3E_PEX2_RX_DN<70>
B18	GND18	GND
C10	SB12	PD_BMC_PE_CABLE_PRESENT_N
C11	SB10	
C12	GND19	GND
C13	TX5+	P3E_PEX2_TX_C_DP<69>
C14	TX5-	P3E_PEX2_TX_C_DN<69>
C15	GND20	GND
C16	TX7+	P3E_PEX2_TX_C_DP<71>
C17	TX7-	P3E_PEX2_TX_C_DN<71>
C18	GND21	GND
D10	SB13	PCIE_SLOT1_PRSNT_X8_2_N
D11	SB14	
D12	GND22	GND
D13	TX4+	P3E_PEX2_TX_C_DP<68>
D14	TX4-	P3E_PEX2_TX_C_DN<68>
D15	GND23	GND
D16	TX6+	P3E_PEX2_TX_C_DP<70>
D17	TX6-	P3E_PEX2_TX_C_DN<70>
D18	GND24	GND

6.15.10 J1083-BMC PCIe Connector

Table 6-23 J1083-BMC PCIe Connector Pin Definition

Pin #	Pin Name	Net Name
A1	SB7	
A2	SB0	
A3	GDN1	GND
A4	RX1+	
A5	RX1-	
A6	GND2	GND
A7	RX3+	
A8	RX3-	
A9	GDN3	GND
B1	SB3	
B2	SB1	
B3	GND4	GND
B4	RX0+	P3E_BMC_PEX2_RX_DP<71>

B5	RX0-	P3E_BMC_PEX2_RX_DN<71>
B6	GND5	GND
B7	RX2+	
B8	RX2-	
B9	GND6	GND
C1	SB4	BMC_PE_CABLE_PRESENT_N
C2	SB2	
C3	GND7	GND
C4	TX1+	
C5	TX1-	
C6	GND8	GND
C7	TX3+	
C8	TX3-	
C9	GND9	GND
D1	SB5	
D2	SB6	
D3	GND10	GND
D4	TX0+	P3E_BMC_PEX2_TX_C_DP<71>
D5	TX0-	P3E_BMC_PEX2_TX_C_DN<71>
D6	GND11	GND
D7	TX2+	
D8	TX2-	
D9	GND12	GND

6.15.11 J24-IO Board Connector

Table 6-24 J24-IO Board Connector Pin Definition

Pin Name	Net Name
1	P5V_AUX
2	IO_CABLE_DETECT_N
3	P5V_AUX
4	GND
5	P5V_AUX
6	GND
7	P5V_AUX
8	GND
9	P3V3_AUX
10	GND
11	P3V3_AUX
12	GND

13	P3V3_AUX
14	GND
15	P3V3_AUX
16	GND
17	
18	GND
19	SYSTEM_GD_LED
20	SMB_IO_TEMP_DAT
21	BMC_PW R_BTN_IN_N
22	SMB_IO_TEMP_CLK
23	SYSTEM_LOG_LED
24	DEBUG_PORT_UART_SEL_BMC_N
25	BMC_READY_N
26	LED_POSTCODE_0
27	PWR_LED
28	LED_POSTCODE_1
29	DEBUG_RST_BTN_N
30	LED_POSTCODE_2
31	SMB_IO_DEBUG_CARD_SDA
32	LED_POSTCODE_3
33	SMB_IO_DEBUG_CARD_SCL
34	LED_POSTCODE_4
35	DEBUG_PORT_UART_TX
36	LED_POSTCODE_5
37	DEBUG_PORT_UART_RX
38	LED_POSTCODE_6
39	IO_CABLE_DETECT_N
40	LED_POSTCODE_7

6.16 EXTERNAL CONNECTORS PINOUT

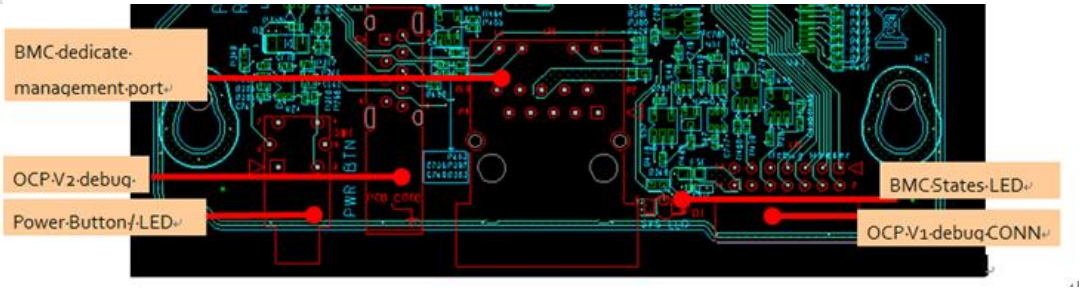


Figure 6-38 External Connectors

6.16.1 BMC Dedicated RJ-45 (IO Board)

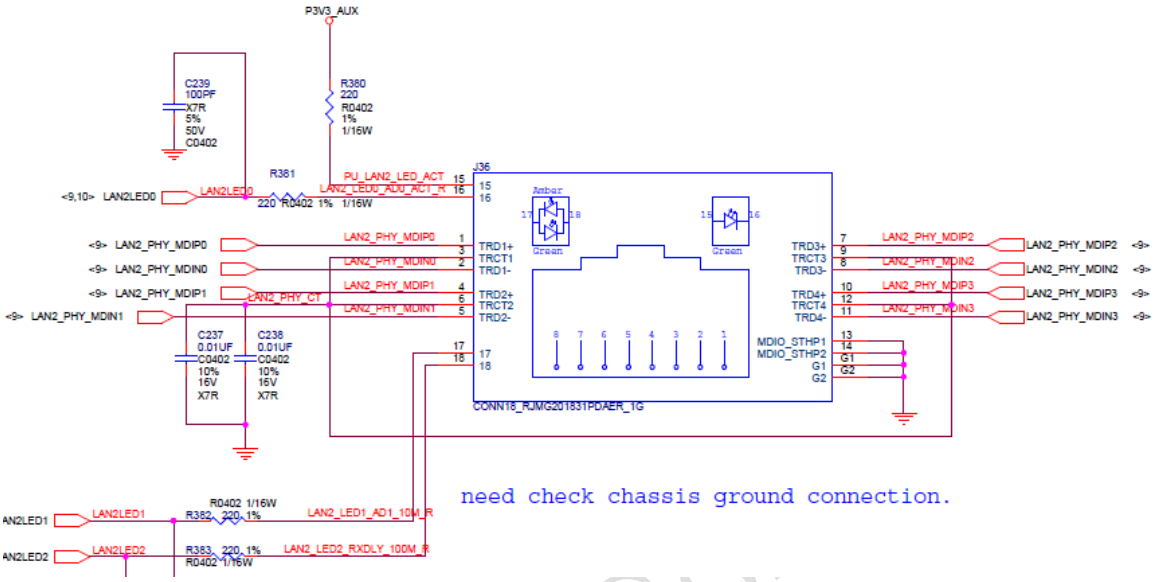


Figure 6-39 BMC Dedicated RJ-45 Schematic

Table 6-25 BMC Dedicated RJ-45 Pin Definition

Pin	Signal Name	Function
1	LAN2_PHY_MDIP0	MDI_1
2	LAN2_PHY_MDIN0	
3	PAN2_PHY_CT	TRCT
4	LAN2_PHY_MDIP1	MDI_2
5	LAN2_PHY_MDIN1	
6	PAN2_PHY_CT	TRCT
7	LAN2_PHY_MDIP2	MDI_3
8	LAN2_PHY_MDIN2	
9	PAN2_PHY_CT	TRCT
10	LAN2_PHY_MDIP3	MDI_4
11	LAN2_PHY_MDIN3	
12	PAN2_PHY_CT	TRCT
13	GND	MDIO_STHP1
14	GND	MDIO_STHP2
15	PU_LAN2_LED_ACT	ACT_LED
16	LAN2_LED0_AD0_ACT_R	LED

17	LAN2_LED1_AD1_10M_R	10M_LED
18	LAN2_LED2_RXDLY_100M_R	100M_LED
19	GND	G1
20	GND	G1

6.16.2 OCP Debug Header (IO Board)

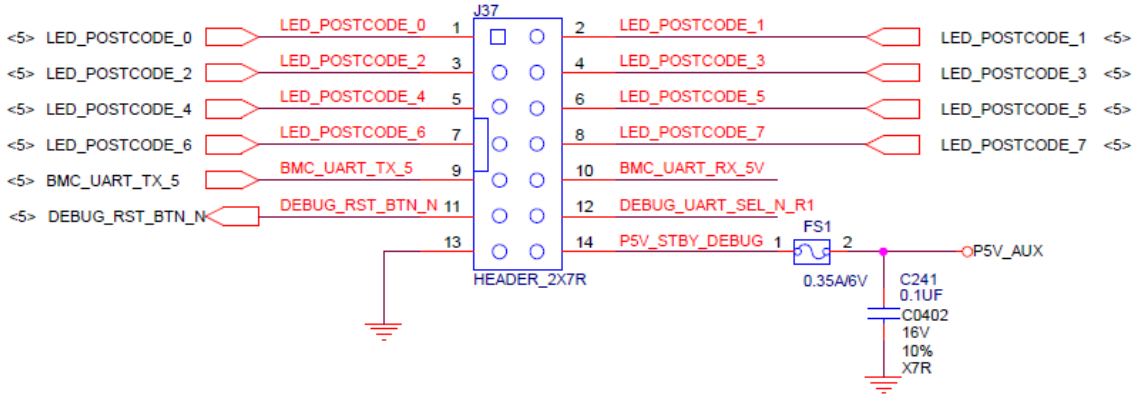


Figure 6-40 OCP Debug Header Schematic

Table 6-26 OCP Debug Header Pin Definition

Pin	Signal Name	Function
1	LED_POSTCODE_0	POST Code
2	LED_POSTCODE_1	POST Code
3	LED_POSTCODE_2	POST Code
4	LED_POSTCODE_3	POST Code
5	LED_POSTCODE_4	POST Code
6	LED_POSTCODE_5	POST Code
7	LED_POSTCODE_6	POST Code
8	LED_POSTCODE_7	POST Code
9	BMC_UART_TX_5	UART
10	BMC_UART_RX_5V	UART
11	DEBUG_RST_BTN_N	RESET BUTTON
12	DEBUG_UART_SEL_N_R	SEL BUTTON
13	GND	GND
14	P5V_STBY_DEBUG	P5V

6.16.3 OCP V2 Debug Header (IO Board)

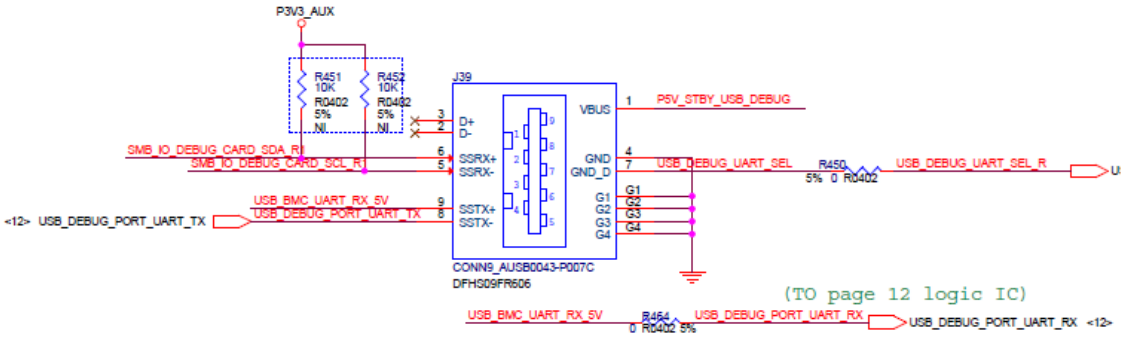


Figure 6-41 OCP V2 Debug Header Schematic

Table 6-27 OCP V2 Debug Header Pin Definition

Pin	Signal Name	Function
1	P5V_STBY_USB_DEBUG	P5V
2	X	Empty
3	X	Empty
4	GND	GND
5	SMB_IO_DEBUG_CARD_SCL_R1	SMBus_SCL
6	SMB_IO_DEBUG_CARD_SDA_R1	SMBus_SDA
7	USB_DEBUG_UART_SEL	UART_SEL
8	USB_DEBUG_PORT_UART_TX	UART TX Signal
9	USB_BMC_UART_RX_5V	UART RX Signal

6.16.4 MiniSAS HD Connector (Host Retimer Card)

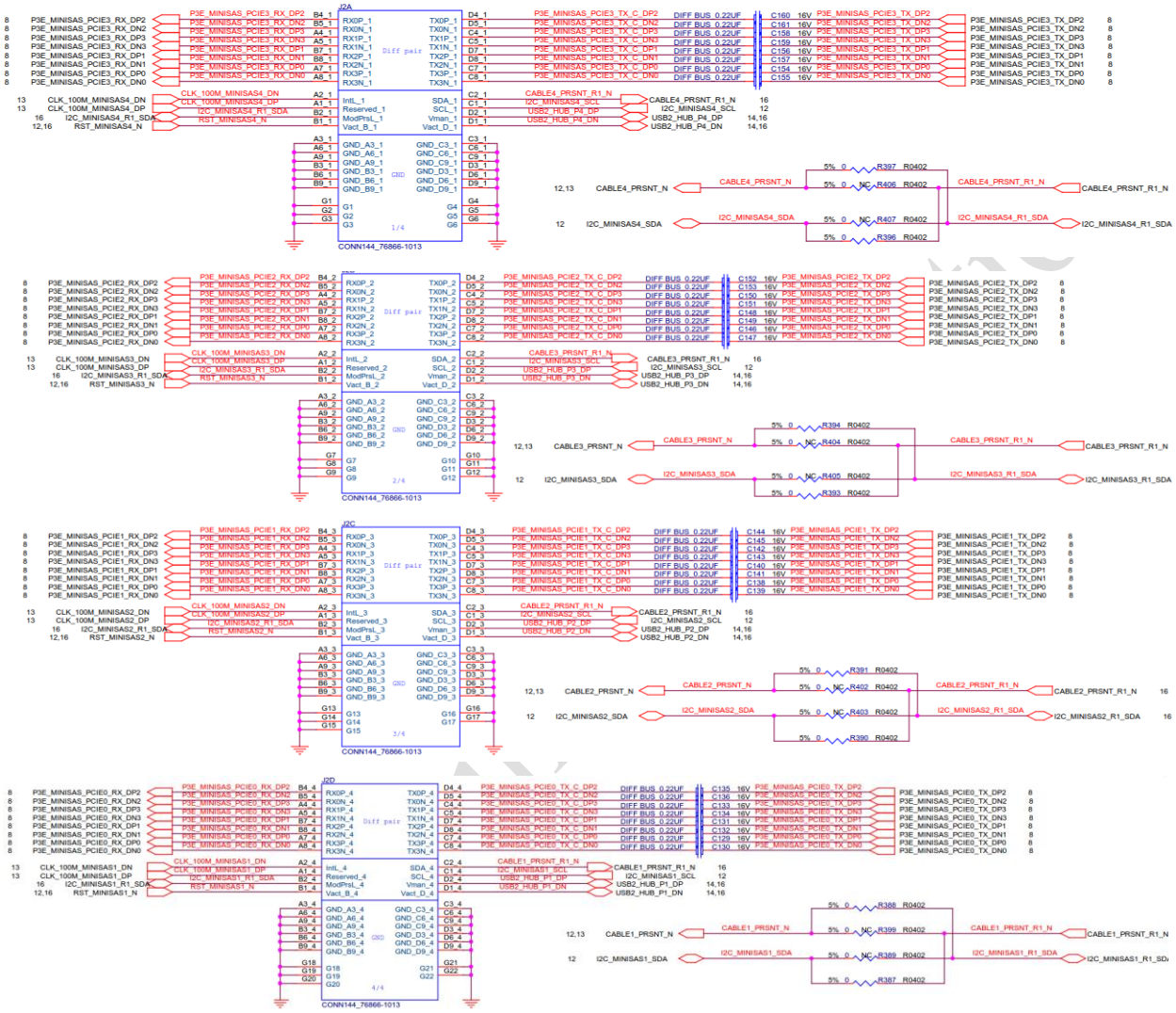


Figure 6-42 MiniSAS HD Connector on Host Retimer Card Schematic

Table 6-28 MiniSAS HD Connector on Host Retimer Card Pin Definition

Pin	Net Name	Pin	Net Name
J2A			
B4_1	P3E_MINISAS_PCIE3_RX_DP2	D4_1	P3E_MINISAS_PCIE3_TX_C_DP2
B5_1	P3E_MINISAS_PCIE3_RX_DN2	D5_1	P3E_MINISAS_PCIE3_TX_C_DN2
A4_1	P3E_MINISAS_PCIE3_RX_DP3	C4_1	P3E_MINISAS_PCIE3_TX_C_DP3
A5_1	P3E_MINISAS_PCIE3_RX_DN3	C5_1	P3E_MINISAS_PCIE3_TX_C_DN3
B7_1	P3E_MINISAS_PCIE3_RX_DP1	D7_1	P3E_MINISAS_PCIE3_TX_C_DP1
B8_1	P3E_MINISAS_PCIE3_RX_DN1	D8_1	P3E_MINISAS_PCIE3_TX_C_DN1
A7_1	P3E_MINISAS_PCIE3_RX_DP0	C7_1	P3E_MINISAS_PCIE3_TX_C_DP0
A8_1	P3E_MINISAS_PCIE3_RX_DN0	C8_1	P3E_MINISAS_PCIE3_TX_C_DN0
A2_1	CLK_100M_MINISAS4_DN	C2_1	CABLE4_PRSNT_R1_N

A1_1	CLK_100M_MINISAS4_DP	C1_1	I2C_MINISAS4_SCL
B2_1	I2C_MINISAS4_R1_SDA	D2_1	USB2_HUB_P4_DP
B1_1	RST_MINISAS4_N	D1_1	USB2_HUB_P4_DN
A3_1	GND	C3_1	GND
A6_1	GND	C6_1	GND
A9_1	GND	C9_1	GND
B3_1	GND	D3_1	GND
B6_1	GND	D6_1	GND
B9_1	GND	D9_1	GND
G1	GND	G4	GND
G2	GND	G5	GND
G3	GND	G6	GND
J2B			
B4_2	P3E_MINISAS_PCIE2_RX_DP2	D4_2	P3E_MINISAS_PCIE2_TX_C_DP2
B5_2	P3E_MINISAS_PCIE2_RX_DN2	D5_2	P3E_MINISAS_PCIE2_TX_C_DN2
A4_2	P3E_MINISAS_PCIE2_RX_DP3	C4_2	P3E_MINISAS_PCIE2_TX_C_DP3
A5_2	P3E_MINISAS_PCIE2_RX_DN3	C5_2	P3E_MINISAS_PCIE2_TX_C_DN3
B7_2	P3E_MINISAS_PCIE2_RX_DP1	D7_2	P3E_MINISAS_PCIE2_TX_C_DP1
B8_2	P3E_MINISAS_PCIE2_RX_DN1	D8_2	P3E_MINISAS_PCIE2_TX_C_DN1
A7_2	P3E_MINISAS_PCIE2_RX_DP0	C7_2	P3E_MINISAS_PCIE2_TX_C_DP0
A8_2	P3E_MINISAS_PCIE2_RX_DN0	C8_2	P3E_MINISAS_PCIE2_TX_C_DN0
A2_2	CLK_100M_MINISAS3_DN	C2_2	CABLE3_PRSNT_R1_N
A1_2	CLK_100M_MINISAS3_DP	C1_2	I2C_MINISAS3_SCL
B2_2	I2C_MINISAS3_R1_SDA	D2_2	USB2_HUB_P3_DP
B1_2	RST_MINISAS3_N	D1_2	USB2_HUB_P3_DN
A3_2	GND	C3_2	GND
A6_2	GND	C6_2	GND
A9_2	GND	C9_2	GND
B3_2	GND	D3_2	GND
B6_2	GND	D6_2	GND
B9_2	GND	D9_2	GND
G1	GND	G4	GND
G2	GND	G5	GND
G3	GND	G6	GND
J2C			
B4_3	P3E_MINISAS_PCIE1_RX_DP2	D4_3	P3E_MINISAS_PCIE1_TX_C_DP2
B5_3	P3E_MINISAS_PCIE1_RX_DN2	D5_3	P3E_MINISAS_PCIE1_TX_C_DN2
A4_3	P3E_MINISAS_PCIE1_RX_DP3	C4_3	P3E_MINISAS_PCIE1_TX_C_DP3
A5_3	P3E_MINISAS_PCIE1_RX_DN3	C5_3	P3E_MINISAS_PCIE1_TX_C_DN3
B7_3	P3E_MINISAS_PCIE1_RX_DP1	D7_3	P3E_MINISAS_PCIE1_TX_C_DP1
B8_3	P3E_MINISAS_PCIE1_RX_DN1	D8_3	P3E_MINISAS_PCIE1_TX_C_DN1
A7_3	P3E_MINISAS_PCIE1_RX_DP0	C7_3	P3E_MINISAS_PCIE1_TX_C_DP0
A8_3	P3E_MINISAS_PCIE1_RX_DN0	C8_3	P3E_MINISAS_PCIE1_TX_C_DN0
A2_3	CLK_100M_MINISAS2_DN	C2_3	CABLE2_PRSNT_R1_N

A1_3	CLK_100M_MINISAS2_DP	C1_3	I2C_MINISAS2_SCL
B2_3	I2C_MINISAS2_R1_SDA	D2_3	USB2_HUB_P2_DP
B1_3	RST_MINISAS2_N	D1_3	USB2_HUB_P2_DN
A3_3	GND	C3_3	GND
A6_3	GND	C6_3	GND
A9_3	GND	C9_3	GND
B3_3	GND	D3_3	GND
B6_3	GND	D6_3	GND
B9_3	GND	D9_3	GND
G1	GND	G4	GND
G2	GND	G5	GND
G3	GND	G6	GND
J2D			
B4_4	P3E_MINISAS_PCIE0_RX_DP2	D4_4	P3E_MINISAS_PCIE0_TX_C_DP2
B5_4	P3E_MINISAS_PCIE0_RX_DN2	D5_4	P3E_MINISAS_PCIE0_TX_C_DN2
A4_4	P3E_MINISAS_PCIE0_RX_DP3	C4_4	P3E_MINISAS_PCIE0_TX_C_DP3
A5_4	P3E_MINISAS_PCIE0_RX_DN3	C5_4	P3E_MINISAS_PCIE0_TX_C_DN3
B7_4	P3E_MINISAS_PCIE0_RX_DP1	D7_4	P3E_MINISAS_PCIE0_TX_C_DP1
B8_4	P3E_MINISAS_PCIE0_RX_DN1	D8_4	P3E_MINISAS_PCIE0_TX_C_DN1
A7_4	P3E_MINISAS_PCIE0_RX_DP0	C7_4	P3E_MINISAS_PCIE0_TX_C_DP0
A8_4	P3E_MINISAS_PCIE0_RX_DN0	C8_4	P3E_MINISAS_PCIE0_TX_C_DN0
A2_4	CLK_100M_MINISAS1_DN	C2_4	CABLE1_PRSNT_R1_N
A1_4	CLK_100M_MINISAS1_DP	C1_4	I2C_MINISAS1_SCL
B2_4	I2C_MINISAS1_R1_SDA	D2_4	USB2_HUB_P1_DP
B1_4	RST_MINISAS1_N	D1_4	USB2_HUB_P1_DN
A3_4	GND	C3_4	GND
A6_4	GND	C6_4	GND
A9_4	GND	C9_4	GND
B3_4	GND	D3_4	GND
B6_4	GND	D6_4	GND
B9_4	GND	D9_4	GND
G1	GND	G4	GND
G2	GND	G5	GND
G3	GND	G6	GND

7. EXTERNAL CABLES DEFINITION

The follow table descripts the external cables information of Big Basin system.

Table 7-1 Big Basin External Cables

Supplier	Length	Type	Part Number
Amphenol	520mm	X8	NEEECA-Q107
Amphenol	350mm	X8	NEEECA-Q106
JPC	520mm	X8	P4103B250550-1
JPC	350mm	X8	P4103B250400-1