

# Programmable PON FPGA Design

OCP Telco Engineering Workshop 05.14.2018



**OPEN**  
Compute Project

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# Use of FPGA in OCP Telco

Engagement with FPGA and IP core providers

Business model similar to ASIC

Standard IP core made available for an OCP Spec

Option to customize for Operator requirements

Spec under development for Programmable PON (10G and 25G)

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# Programmable PON OLT

Design OLT spec for XGSPON; hardware capable of 25G PON upgrade in future

OLT port density of 24 for 1RU

What is desired from Operators?

- 19" 1 RU OLT design
- Open Sled design for CG-OpenRack-19



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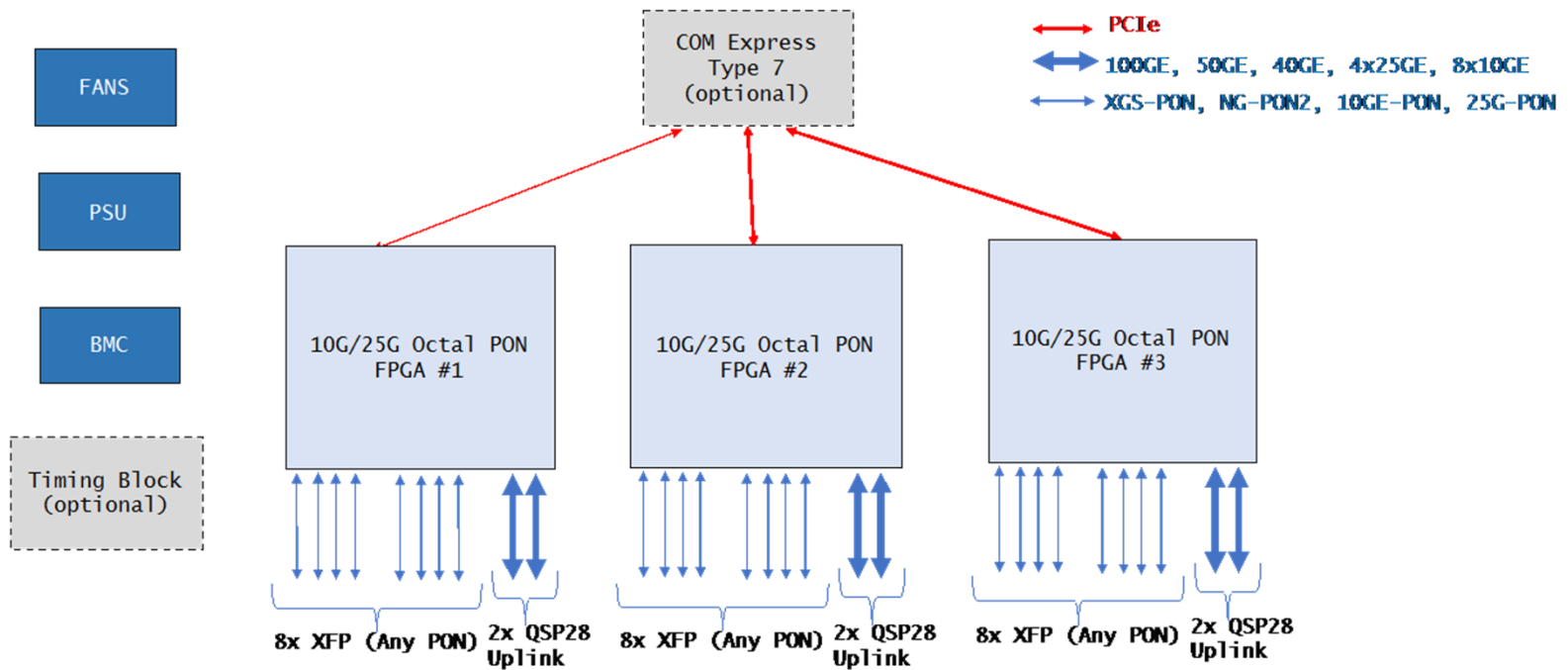
# Programmable PON OLT

Partnering with Xilinx and Feneck  
Build FPGA modules for PON MAC  
(8) 10G ports per FPGA design  
No aggregation in the OLT  
Optional CPU  
BMC Support

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# Block Diagram



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# Open Access Architecture

## Open Source Access Manager (OSAM)

Vendor agnostic operation interface for managing consumer broadband devices and services

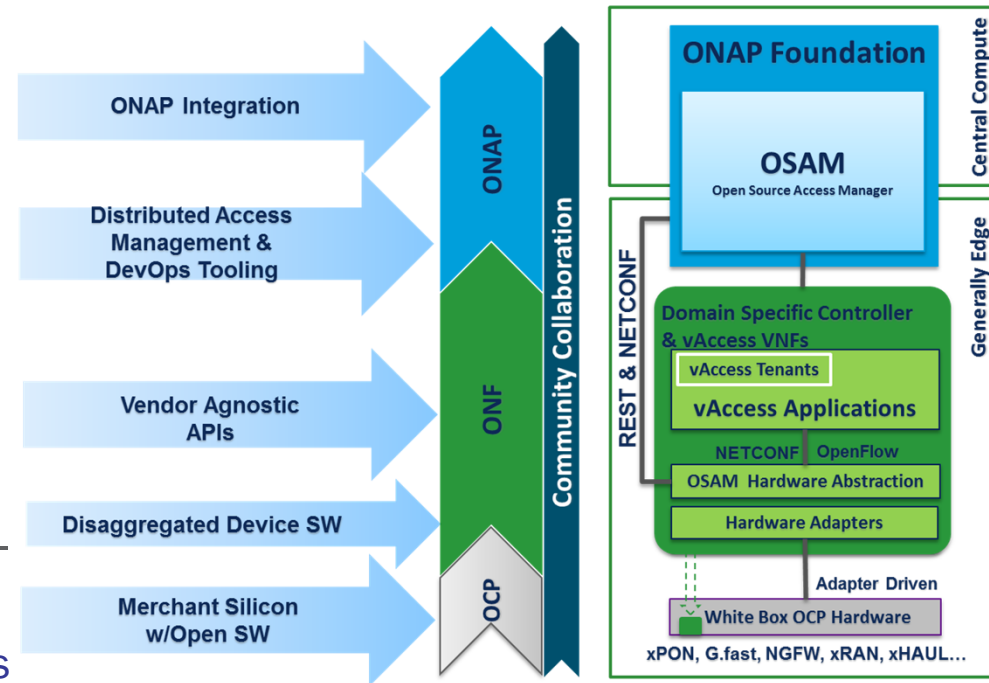
Integrated to the ONAP framework

## Domain Specific Controller (DSC)

Disaggregation of control and management plane

## Hardware abstraction (VOLTHA/OSAM-HA)

Abstract and harmonize hardware interfaces and data



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# G.fast Specification

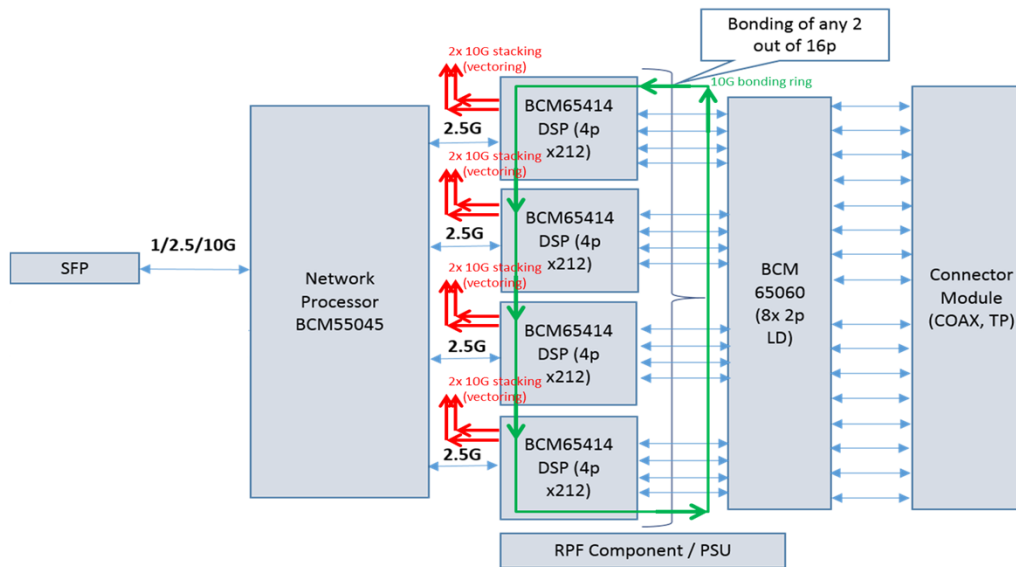
- 16 port DPU-Broadcom Spec
- 16 port DPU-Skipio Spec

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# 16 port DPU-Broadcom Spec

- Coax and twisted pair
- Reverse power feed
- Uplink- 1G, 2.5G, 10G Ethernet or GPON/XGSPON

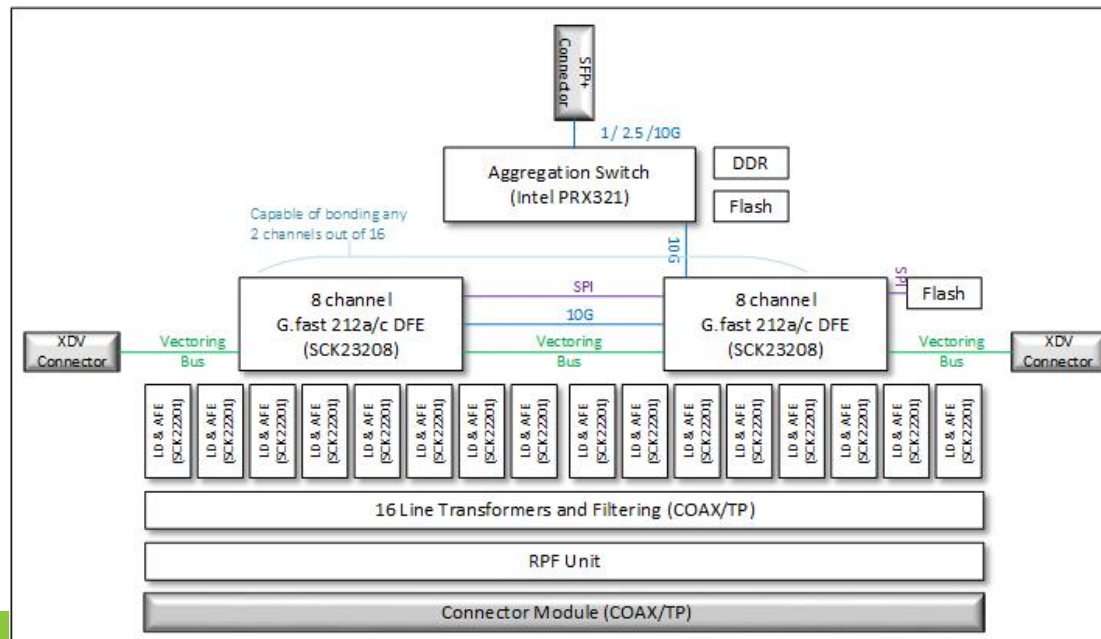


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# 16 port DPU-Sckipio Spec

- Updated NPU – PRX321
- Coax and twisted pair
- Reverse power feed
- Uplink- 1G, 2.5G, 10G Ethernet or GPON/XGSPON



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# Call to Action

Collaboration/feedback to define detailed spec for Programmable PON OLT, FDH

Review of Spec -16 port DPU-Skipio v2.0, 16 port DPU-Broadcom v2.0

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# OCP SUMMIT