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Compute Project

Open Accelerator Infrastructure

--- Universal Baseboard Design Specification **v1.0**

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2. Acknowledgement

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3. Introduction and Scope

Open Accelerator Infrastructure (OAI) is an initiative within the OCP Server Project to define a modular, interoperable architecture for systems targeting Machine Learning, Deep Learning, and High-Performance Computing workloads. Beginning with the OCP Accelerator Modules (OAI-**OAM**), OAI defines the logical and physical attributes of all the basic building blocks of an accelerator system design.

A standard way to connect this Open Accelerator Infrastructure to a CPU Box in a rack is shown in Figure1.

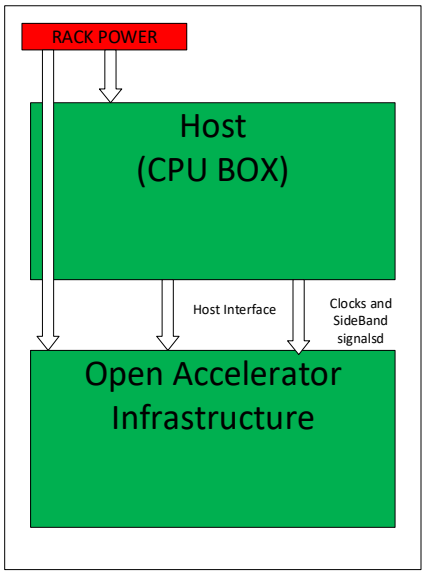


Figure 1 OAI as a disaggregated compute for AI in a Rack.

The Universal Baseboard (UBB) specification is the next step in defining a complete solution for this accelerator infrastructure, leveraging the progress in defining the OAM module and carrying forward the goals of openness and modularity.

The Open Accelerator Infrastructure will be composed of these base building blocks:

- OAI Power Distribution (OAI-**PDB**): It provides the translation between Rack Power to UBB module power needs.
- OAI Host Interface (OAI-**HIB**): The HIB provides the interface links between the UBB and head node(s).
- OAI Security, Control, and Management (OAI-**SCM**): This module provides management, power sequencing, and security for OAI.
- OAI Universal Baseboard (OAI-**UBB**): The UBB Baseboard supports 8 OAM modules in various fabric and interconnect topologies.
- OCP Accelerator Module (OAI-**OAM**): Specification 1.0 defines the mezzanine module accelerator.
- OAI Expansion (Scale-out) Beyond UBB (OAI-**Expansion**): Specifications describes connections between multiple OAI systems in the same rack or across different racks.
- OAI-**Tray:** The tray provides mechanical support to adapt various UBBs to both 19” and 21” Chassis and Racks
- OAI-**Chassis:** This chapter discusses both **air-cooled** and **liquid-cooled** implementations.

Specifications for each of these components will cover logic, power, mechanical, connector interfaces and thermal infrastructure definitions to ensure interoperability between all the OAI elements.

These elements and its interactions are represented in the figure2.

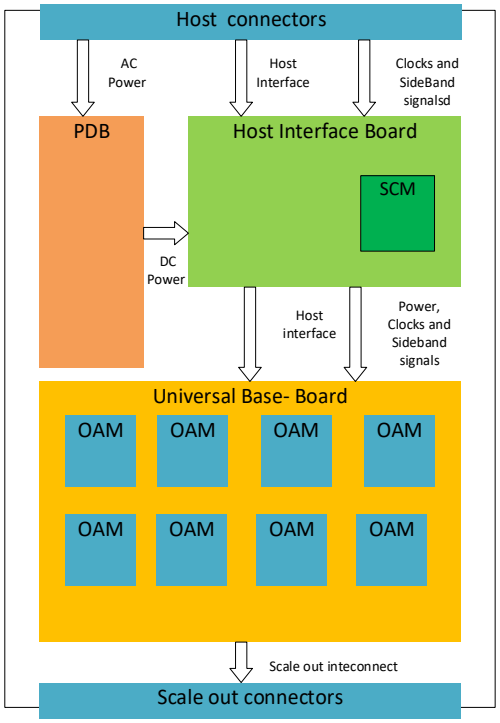


Figure 2 OAI building blocks

The figure below shows an example system from Inspur as a composite of various OAI building blocks.

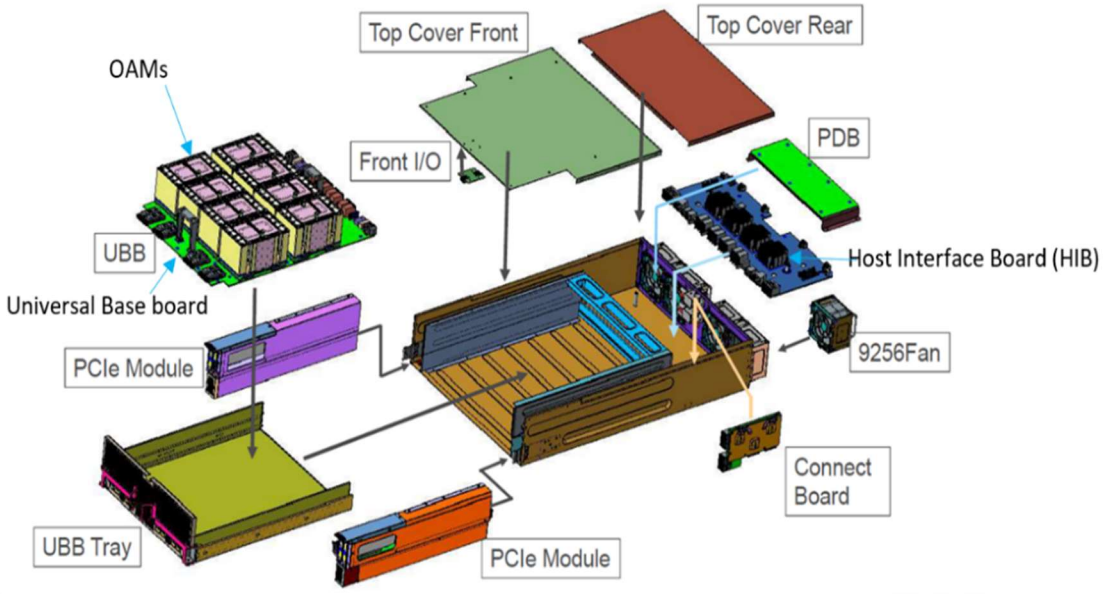


Figure 3 Example OAI System Building Blocks

4. Universal Baseboard (OAI-UBB) High level Description

The Universal Baseboard is designed to be modular and flexible in supporting current and future OAM modules and providing maximum design flexibility for many conceivable system designs. The UBB supports 8 OAM modules but the board has been engineered to support a wide options of interconnect fabrics and topologies, power domains, TDP's, cooling solutions, and scale out options. While the board is optimized for a few common configurations and released OAM modules, great care was taken to accommodate future trends and customer needs.

The Universal Based Board (UBB) is a building block that supports:

OAM Support	• Various interconnect topologies for the 8 OAMs • Air or liquid cooling • OAM powered by 12V nominal up to 350W (*) • OAM powered by 54V/48V nominal up to 700W (*) • One x16 host interface per OAM

Interface to HIB (Host Interface Board)	• 8 x16 connectors for host interface connections (one per OAM)
	  • Each Host Interface up to x16 lanes (for example PCIe Gen4)
	  • Support for PCIe Gen5 and other future host interfaces
	• Power: 12V, 54V, 12V standby, etc.
	• Side band signals: I2C, Reset, Reference clocks, JTAG, Power management, etc.

Scale out Capabilities	• QSFP-DD connectors for scale-out interconnect** • Exposed from UBB to the exterior of the UBB Tray/System Chassis
Electrical Interoperability	• Current UBB reference design supports SERDES links up to 28 Gbps NRZ, and up to 56 Gbps PAM4 • Two Micro USB connectors are exposed from the UBB to the exterior of the chassis for debug (UART to USB)
Mechanical Interoperability	• PCB dimensions: 417mm wide x 585mm long • Supports both 19" and 21" rack chassis infrastructures • Defined mounting hole sizes and locations

Table 1 Universal Based Board (UBB) is a building block

Note:

* Different UBB design may have different power support, check UBB providers for specific product spec.

**Number of QSFP-DD connector is flexible, based on different UBB design.

The figure 2 shows the major physical features of the UBB board. In red you can see power delivery connections to OAM module, in yellow you can follow Host interface, clock and SCM signals to OAM module and in green you can see scale out (SERDES) interconnect from OAM module to external connectors.

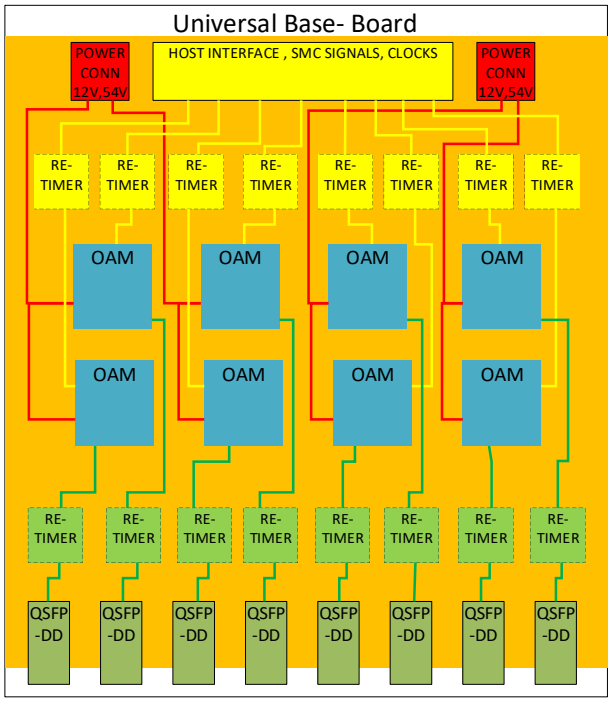


Figure 4 Example UBB System Building Blocks

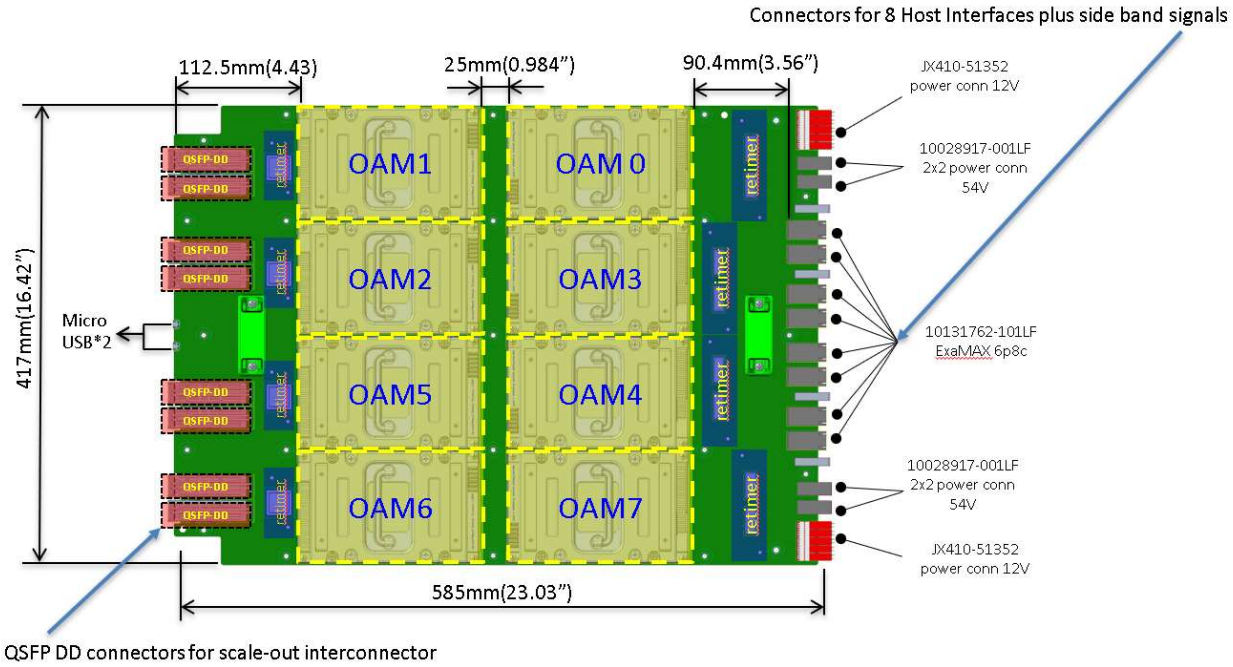


Figure 5 Universal Reference Base Board (UBB)

5. Input and Output Interfaces

The UBB board is the carrier board that houses the 8 OAM modules, and it defines five main interfaces to other boards in a complete system design:

1 OAM Interface: Interface to the Open Accelerator Modules
2 Host Fabric interface: Required interface to host(s) via PCIe or other fabric. The interface fabric is routed to the Host Interface Board where it connects to either a host node integrated within the same chassis or a disaggregated host node.
3 Scale out interface: Optional interface that allows multiple UBB boards to be connected through QSFP-DD connectors.
4 Miscellaneous Signal Interface – SMBus, USB, Clocks, side band signals provided by the Host Interface board.
5 Input Power Interface – 54V/48V, 12V, and 3.3V Aux inputs to the UBB.

5.1. OAM Interconnect Interface

As outlined in the OAM 1.0 design specification, each OAM has up to eight x16 interconnect links. Each OAM to OAM connections can support different interconnect topologies based on how many links are supported by the specific OAM populated on the UBB.

Please refer to Section 7 to for more details on the supported UBB interconnect topologies and the 1.0 OAM Specification for pin-out and accelerator module information.

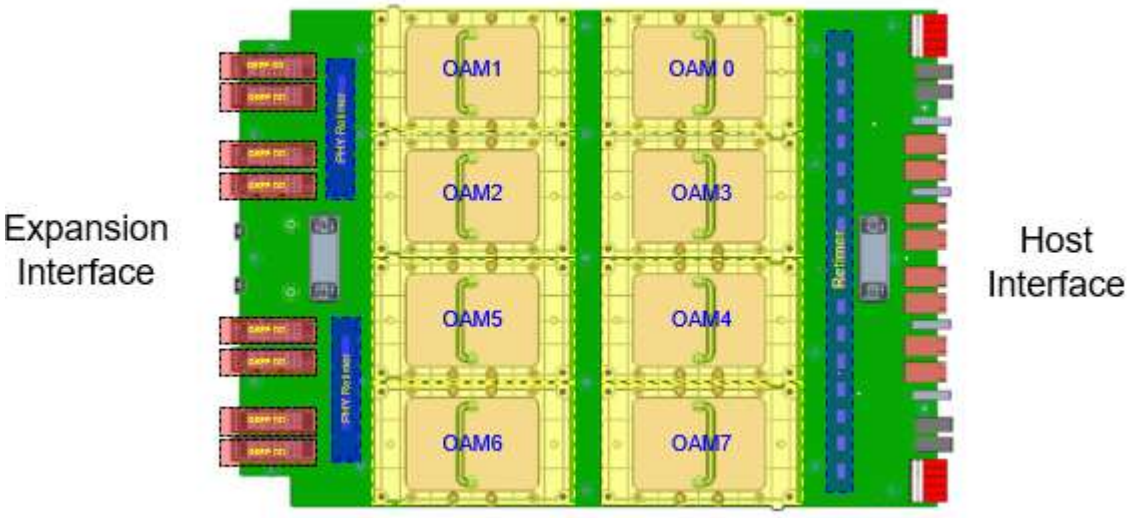


Figure 6 UBB Host and Expansion (scale-out) Interfaces

5.2. Host Fabric Interface

This section describes the host interface to the HIB board including supported fabrics and speeds.

5.2.1. Host Interface: High speed interface

There are eight x16 SerDes links dedicated for host interface connections. Each OAM module on the UBB routes a x16 link to a dedicated ExaMAX connector (shown in Figure 3) which connects to the Host Interface Board.

Different implementations of the Host Interface Board provide customized topologies that allow the UBB to interface to a single host node or to multiple hosts in various configurations. System designs can also be designed to support either integrated head nodes that reside in the same chassis as the UBB or disaggregated head nodes, which cable to a separate UBB chassis within the rack.

The specification supports the use of industry standard host protocols such as PCIe Gen4, CXL, Infinity Fabric and other alternate protocols. Space has been allocated on the UBB for re-timers that may be needed to support certain protocols or configurations needed with different OAM and system designs.

5.2.2. Pin list

A detailed pinout is provided in section 6.2.1

5.3. Scale Out Interface

The UBB uses QFSP-DD connectors to allow scale out topologies that connect multiple UBB boards together through high speed cables. The number of QSFP-DD connectors varies based on different design.

5.3.1. High speed support

The QSFP-DD connectors are exposed on the exterior of the UBB tray and system chassis to allow connections to other UBB systems. The QSFP-DD connection can be through passive or active copper cables.

OAI UBB reference board is designed to support SerDes data rates up to 28Gbps NRZ or 56Gbps PAM4. In addition, to support future configurations, space for re-timers has been allocated on the UBB board while SI studies are conducted against various system and cable configurations.

5.3.2. I2C

An I2C interface is included on each QSFP-DD connector to enable cable re-driver tuning and FRU access.

5.3.3. Pin list

Refer to section 6.2.1

5.4. Miscellaneous Signal Interface

The UBB also receives important ancillary signals from the host interface board that are defined for security, control and board management.

5.4.1. Clock and I2C Signals

The UBB receives its primary clock, AUX clock, downstream clock from the HIB. Please refer to section 6.1.1 for details.

5.4.2. Board management

There are I2C, JTAG, UART for UBB management.

- I2C is used to read OAM information, status and UBB FRU.
- OAM Reset is controlled by the host node through HIB CPLD to UBB CPLD.
- JTAG is used for debug and FW upgrade.
- UART is used for OAM debug.

5.4.3. Power management

There are PWREN, PWROK, PWRBRK#, thermtrip# signals for power management.

- PWREN: UBB power ready assert OAM power enable.
- PWROK: Indicates OAM power is stable and assert PWROK to CPLD
- PWRBRK#: There are two sources to trigger PWRBRK#. One is from BMC, the other is from PSU alert
- Thermtrip#: it indicates OAM silicon has reached an elevated temperature. OAM will power off itself when thermtrip# is triggered. UBB may or may not shutdown entire board. It depends on different system design requirement.
- UBB Power Ready (UBB_PWR_READY): Assert UBB_PWR_READY to notice BMC on HIB when all of UBB powers are ready.

5.5. Input Power Interface

The UBB supports two OAM power types: 54V/48V OAM modules with TDPs up to 700W and 12V OAMs with TDPs up to 350W. DC Power for the UBB is supplied by a group of connectors on the edge of the board.

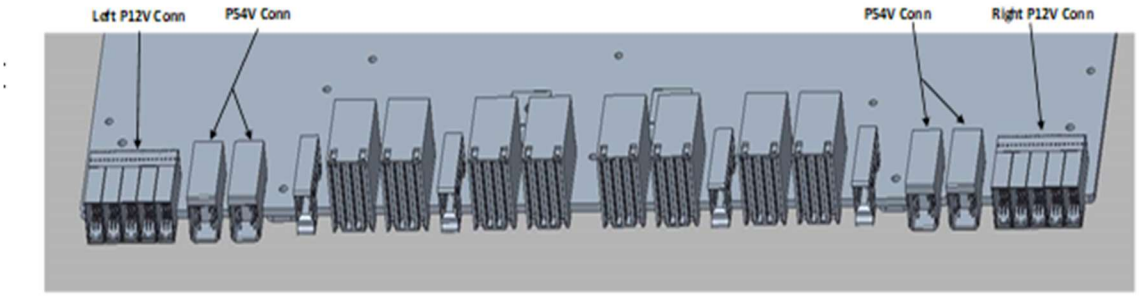


Figure 7 Input Power connectors Placement

There are four dedicated 54V/48V connectors delivering power from the HIB to the UBB. In addition, two connectors provide 12V power to the OAMs and other UBB components from the host interface board (HIB). One of the 12V power sources is used to power PCIe Retimers, SerDes Retimers and the 3.3 voltage converter to the QSFP-DD connectors. 3.3V Auxiliary is used to power the CPLDs and other board management components during DC power off stage.

Because the UBB is destined for different rack infrastructures and form factors, it is designed to interface to different system specific HIB and PDB implementations that support both bus bar or discrete power supply solutions. A typical implementation is shown below:

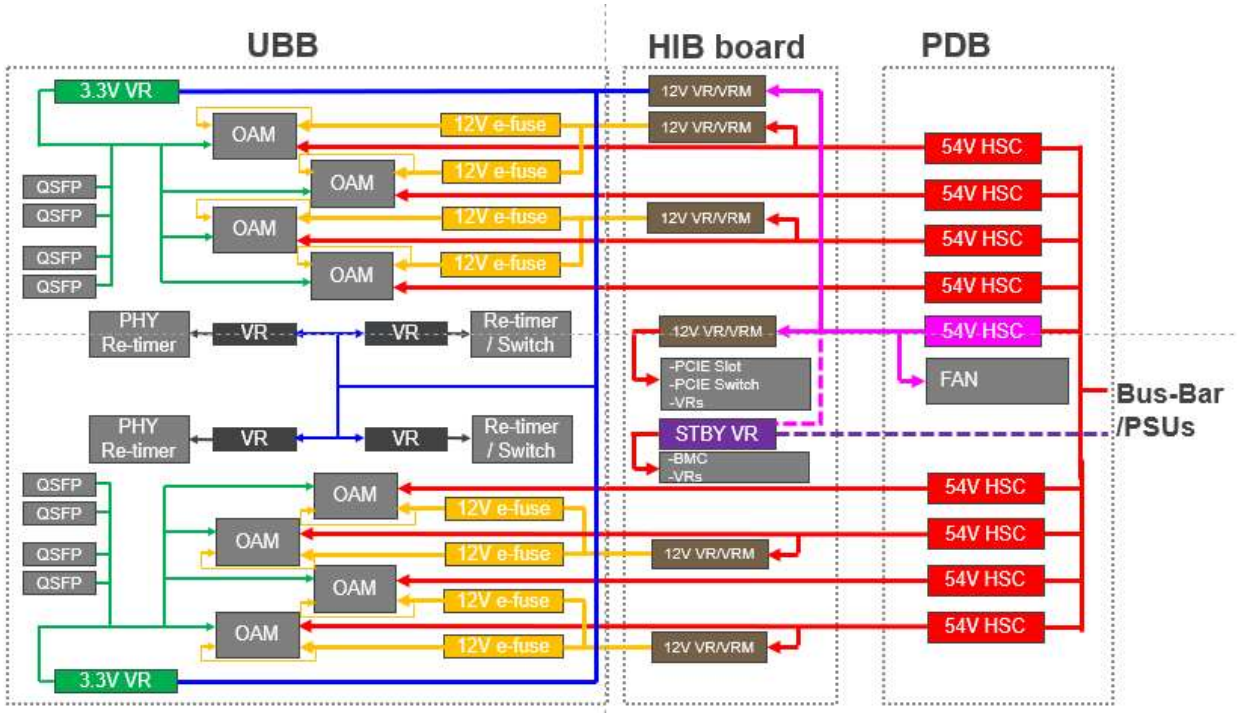


Figure 8 OAI Reference UBB power Delivery Diagram

5.5.1. UBB System Power

UBB is part of the OAI system infrastructure, which supports two distinct power architectures.

One is centralized power in the rack with a busbar, which is often energized by an in-rack power shelf with several 54V/48V PSUs.

The other method utilizes PSUs integrated in the individual OAI system chassis itself. The PSU's input is from an AC supply and its output is 54V or 12V. For example, 54V 3000W Platinum PSUs with 3+3 redundancy is one known OAI system implementation.

Please refer to Section 6.2 for power connector pin list.

5.5.2. 54V/48V based OAM power input

Each OAM has isolated source from 54v/48v through dedicated hotswap controller(on power distributed board aka OAI-PDB) . System provider who designs the OAI system shall implement bulk capacitors to support OAM 54V/48V power rails in order to support OAM EDP. The implementation shall be at the HIB power connectors side. Pls refer to section 5.5.4 for detail excursion power support.

The following table summarizes the voltage range UBB supports.

	Minimum	Nominal	Maximum
Operating voltage	40.0V	48.0/54.0V	59.5V

Table 2 UBB input voltage range

The recommended range includes DC level, noise, and other transients. The input rails must remain within 40 to 59.5v.

Although specific UBB has certain OAM TDP support target based on specific design, UBB could support up to 700W TDP OAM . Linear interpolation can be used to approximate the continuous current specification for nominal input voltages between 48.0V and 54.0V.

Specification	Voltage(nominal)	Maximum Value	Moving Average
Input 54V	54.0V	103.7A	continuous
Input 48V	48.0V	116.7A	continuous
Total baseboard power	48.0V to 54.0V	5600W	continuous

Table 3 UBB(up to 700W OAM) input continuous current specifications

UBB system provider shall check with OAM vendor to get detail excursion support requirement and apply design accordingly. OAI UBB reference boards support OAM's excursion design power (EDP) of 1.6x TDP (500w based on 48/54V) for a 2ms duration.

Voltage	EDP	Current *	Duration
54V or 48V	2x TDP	200%*103.7A(or 116.7A)	<= 20us
	1.6x TDP	160%*103.7A(or 116.7A)	<= 2ms
	1.5x TDP	150%* 103.7A(or 116.7A)	<= 5ms
	1.2x TDP	120%*103.7A(or 116.7A)	<= 10ms
	1.1x TDP	110%*103.7A(or 116.7A)	<= 20ms

Table 4 UBB(up to 700W OAM) EDP support example

5.5.3. 12V based OAM Power input

The 12V input to the UBB could support an EDP of 1.5x for a 5ms duration. The UBB shall provide an isolated 12V rail to each OAM through dedicated E-fuses on the boards. These E-fuses have over current protection and prevent OAM modules from being damaged or affected by over current failures.

The 12V pin assignment is provided in UBB spec package.

The following table summarizes the voltage range UBB supports.

	Minimum	Nominal	Maximum
Operating voltage	11.0V	12.2V (11.6V~12.8V)	13.2V

Table 5 UBB operation voltage range

Input electrical design point peak specifications are based on nominal voltages, with the continuous current specifications shown in the table below. Linear interpolation can be used to approximate the continuous current specification for nominal input voltages 12V.

Specification	Voltage(nominal)	Maximum Value	Moving Average
Input 12V	12.2V	230A	continuous
Total baseboard power	12.2V	2800W	continuous

Table 6 UBB input continuous current specifications

UBB system provider shall check with OAM vendor to get detail excursion support requirement and apply design accordingly. OAI UBB reference boards support OAM's excursion design power (EDP) of 1.6x TDP(350w) based on 12V for a 2ms duration.

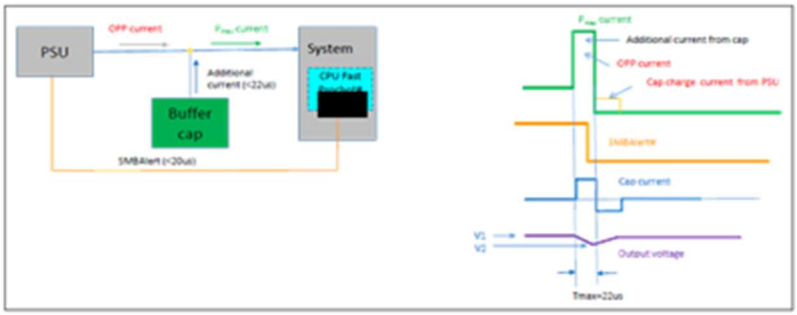
Voltage	EDP	Current *	Duration
12V	2x TDP	200%*230A	<= 20us
	1.6x TDP	160%*230A	<= 2ms
	1.5x TDP	150%* *230A	<= 5ms
	1.2x TDP	120%**230A	<= 10ms
	1.1x TDP	110%**230A	<= 20ms

Table 7 UBB(up to 350w 12v based OAM) EDP support example

5.5.4. OAM Excursion Power Support

This section describes 12V/54V power design guide based on UBB reference system.

Figure below is based on peak current requirement to calculate Cmin capacitance for micro second(uS) for reference.



The total required Min buffer capacitance to support P_{max} can be calculated as follows:

$$C_{min}(\mu F) = 2 \times (P_{max} - P_{opp}) \cdot \frac{T_{max}(\mu s)}{V^2{}_1 - V^2{}_2}$$

Figure Figure 9 Cmin calculation for OAM peak current

- Cmin: Min buffer cap size assuming PSU(s) has 0uF output capacitance and 0uF on the baseboard power rail.
- Pmax: the max system power, due to CPU Pmax virus condition.
- Popp: the PSU minimum OPP power level, and it is always set above system power budget corresponding with CPU's Pmax.app
- Tmax: the throttle time delay after the system power exceeds the pre-defined power threshold.
- V1 and V2: The PSU output voltage levels at the beginning and the end of Pmax time interval (Tmax)

Table is an example for 54V/12V power at 2x EDP 20us calculation result based on reference UBB design. The 54V OAM 700W EDP with 20us duration is about 66uF of Cmin, and the 12V OAM 350W EDP with 20us duration is about 699uF of Cmin. The designer should trade off your PCB space and cost to provide VR/Cap solution for peak power reqirement.

700W EDP / 54V OAM	
Cmin(uF) =	66
P_EDP(2x TDP) =	1400
P_TDP =	700
Tmax(uS) =	20
V1(54V_Busbar Vmin spec, -10%) =	48.6
V2(OAM Vmin spec) =	44

350W EDP / 12V OAM	
Cmin(uF) =	699
P_EDP(2x TDP) =	700
P_TDP =	350
Tmax(uS) =	20
V1(12.5V_VR Vmin spec, -5%) =	11.875
V2(OAM Vmin spec) =	11

Table 8 Cmin requirement at 2x EDP 20us

5.6. 40V ~ 59.5V power layout guidance

Due to the high voltages on the UBB, risks that manufacturing defects can result in a shorts or faults across large voltage differentials need to be addressed.

Industry safety standards (IEC CDV 62368) require additional safe guards (i.e. creepage/ clearance distances, access restrictions, etc.) for systems with voltages that exceed 60V. Voltage differential of less than 60Vdc are classified as ES1 voltage sources. While ES1 systems do not require explicit safety safeguards, the guidelines below will minimize the risk of a fault that could cause high energy dissipation or fire.

Layout Recommendations before Hot Swap Controller / Fuse	**Minimum spacing between conductors with high potential differences >40V**
Internal Layer	25 mils (0.64mm)
External Layer	120 mils (3.0mm)
Z-Axis	17 mils (0.43mm) spacing or 3-ply prepreg
Layout Recommendations after Hot Swap Controller / Fuse	**Minimum spacing between conductors with high potential differences >40V**
Internal Layer	25 mils (0.64mm)
External Layer	60 mils (1.5mm)
Z-Axis	3 mils (0.076mm)

Table 9 40V ~ 59.5V layout guidance

Exceptions may be necessary due to inherent spacing of components and should be fully evaluated with DFMEA on a case by case basis.

Proper power and ground isolation for an external layer on the UBB is shown below.

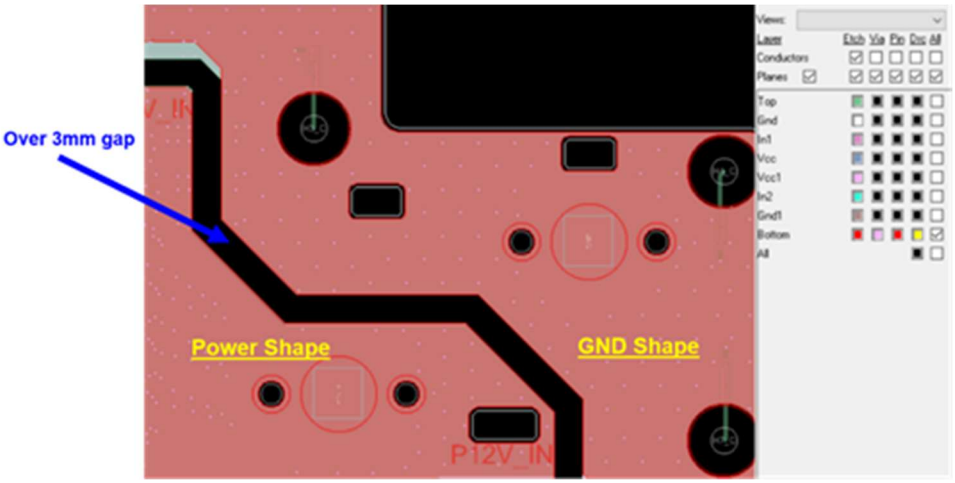


Figure 10 power and GND isolation

6. UBB Electrical Specification

This chapter describes details of the UBB electrical design.

6.1. Board Architecture specification

The OAI- UBB boards will share a common hardware architecture definition for various design areas such as Clock distribution, Power Sequence Control, Telemetry, I2C, and GPIO assignments. The intention for the common hardware specification is to have a single Firmware and Software definition that can cover all different designs and to re-use the hardware solutions as much as possible across the different products.
The common hardware architecture components include the following definitions.

- Power Delivery
- Clock Distribution
- I2C Interconnectivity
- Power and Reset control
- Power and Reset Sequence
- GPIO definition

6.1.1. System Clock Architecture

Host to HIB will run in SRIS mode. HIB to UBB will be common clock mode. SRIS also supports Spread-Spectrum Clocking (SSC) for EMC/ EMI.

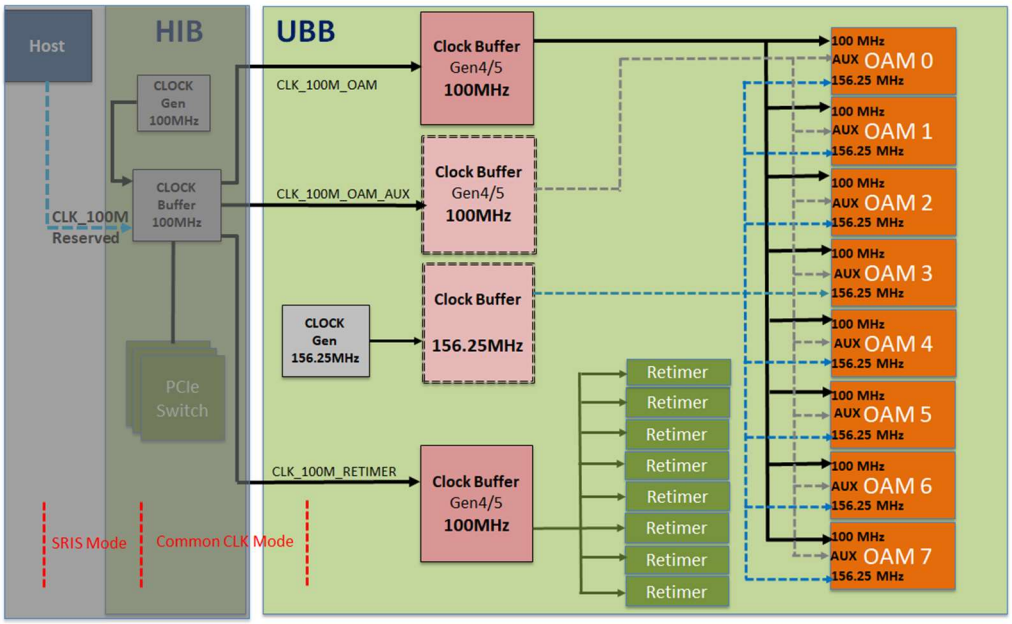


Figure 11 OAI Reference UBB clock diagram

6.1.2. I2C architecture

Considering bus traffic, there are 5 I2C buses as illustrated in diagram below.

Bus1 is for 12V HSC sensor polling.

Bus2 is for OAM sensor information and FW update. PCA9555 IO expander with GPIO control is also on this bus.

Bus3 connects SERDES clock gen/ clk buffer as well as retimers.

Bus4 is for scale out PHY FW update and sensors.

Bus5 is for UBB sensor readings and UBB CPLD FW update.

There're 2 FRU EEPROM in UBB board. FRU 0 is dedicated for BMC, and FRU 1 is shared with BMC and OAM #0. Refer to section 10.6 for detail.

Below describes how UBB I2C pull up resistor is calculated. Each board designer has to calculate pull up time they need.

The minimum resistance calculation as

$$R_p(min)=(V_{cc}-V_{OL}(max))/I_{OL}$$

V_{cc} is the bus voltage, $V_{OL}(max)$ is the maximum voltage that can be read as logic-low and the maximum current that the pins can sink when at or below V_{OL}.

The maximum resistance calculation as:

$$R_p(max)=t_T/(0.8473xC_b)$$

t_T is the maximum allowed rise time of the bus and C_b is the total bus capacitance.

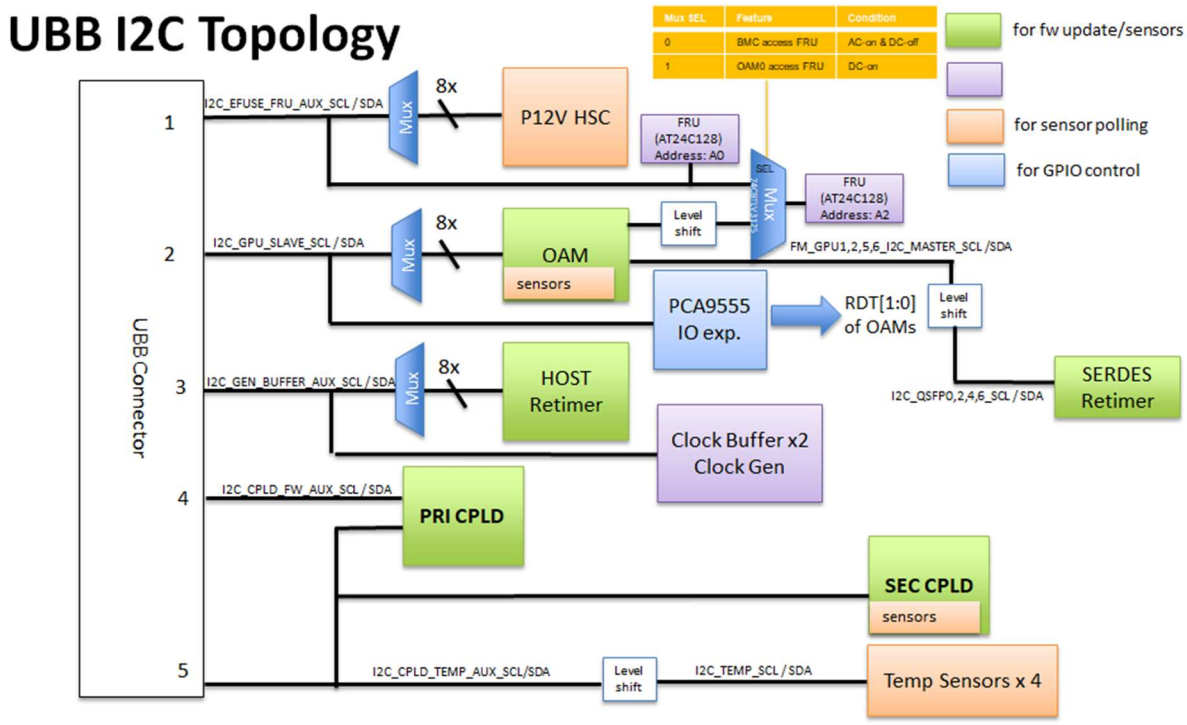


Figure 12 I2C/SMBus Block Diagram

6.1.3. Power control

The UBB provides 12V and 54V/48V to 8x OAMs, the 12V is provided by HIB power connector (P12V_1 and P12V_2) through eFuse (ex: MP5023) control. And the 54V/48V power is connected from HIB power connector (P54_0, P54_1, P54_2 and P54_3) directly.

All voltage power on/off could be controlled by the management device of HIB through I2C bus to CPLD. The UBB provide the 12V power over 2400W (8x 300W) and 54V/48V over 4000W (8x 500w), therefor, All OAM power enable will be controlled by CPLD to do time slot for series power on. The duration of time slot will be updated in the next version.

6.1.4. Reset

The following figure shows the UBB reset diagram from HIB management device (ex, BMC) to UBB device via CPLD, all device reset could be controlled by I2C bus of HIB setting to CPLD. UBB on board device is including OAM, OAM uplink serdes retimer and OAM scale out serdes phy retimer.

The below are each signal naming function:

OAM_PERST_[7:0]#: OAM up-link serdes reset signal from HIB via CPLD at the OAI system or host power on reset.

OAM_WARMRST_[7:0]#: OAM warm reset signal from HIB via CPLD at the OAI system reboot or after firmware update.

RETIMER_PERST_[7:0]_A/B#: OAM up-link serder Retimer-A/B device reset signal from HIB via CPLD.

SERDES_RESET_[7:0]#: OAM expansion serdes PHY retimer device reset signal from HIB via CPLD.

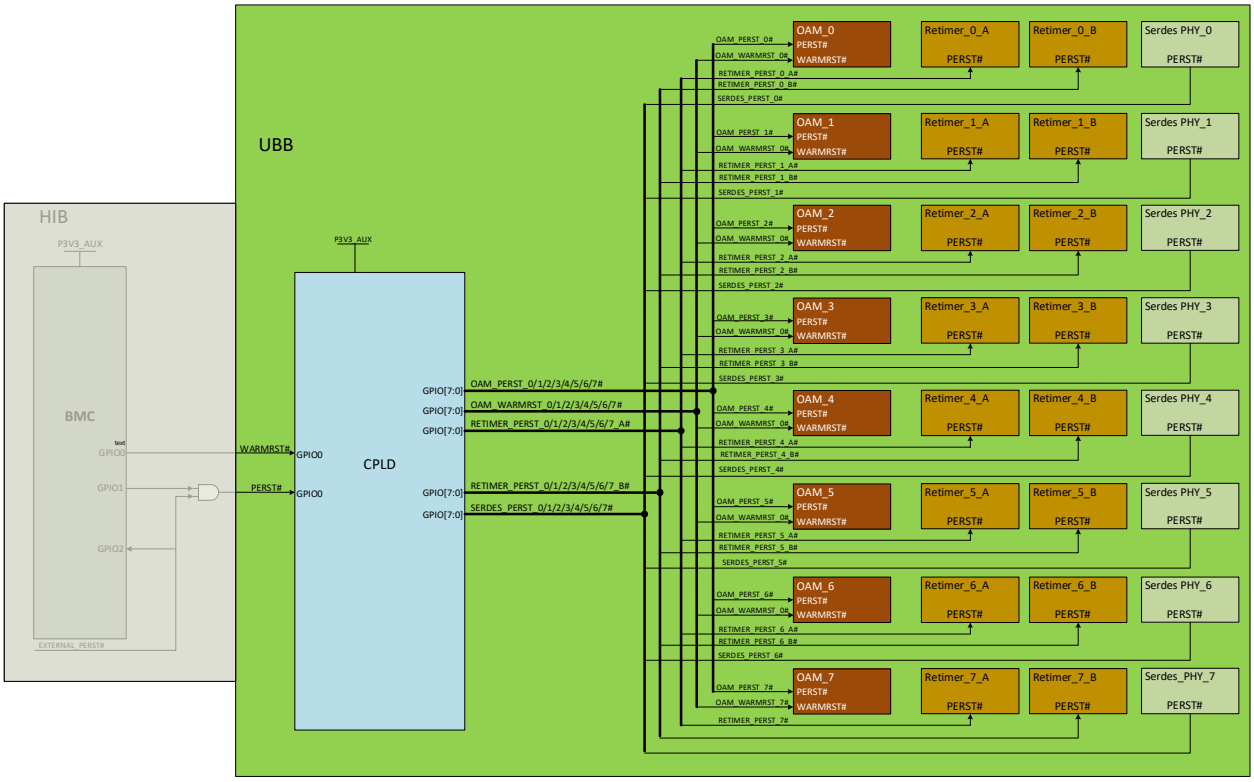


Figure 13 UBB Reset signals diagram

6.1.5. Power Diagram

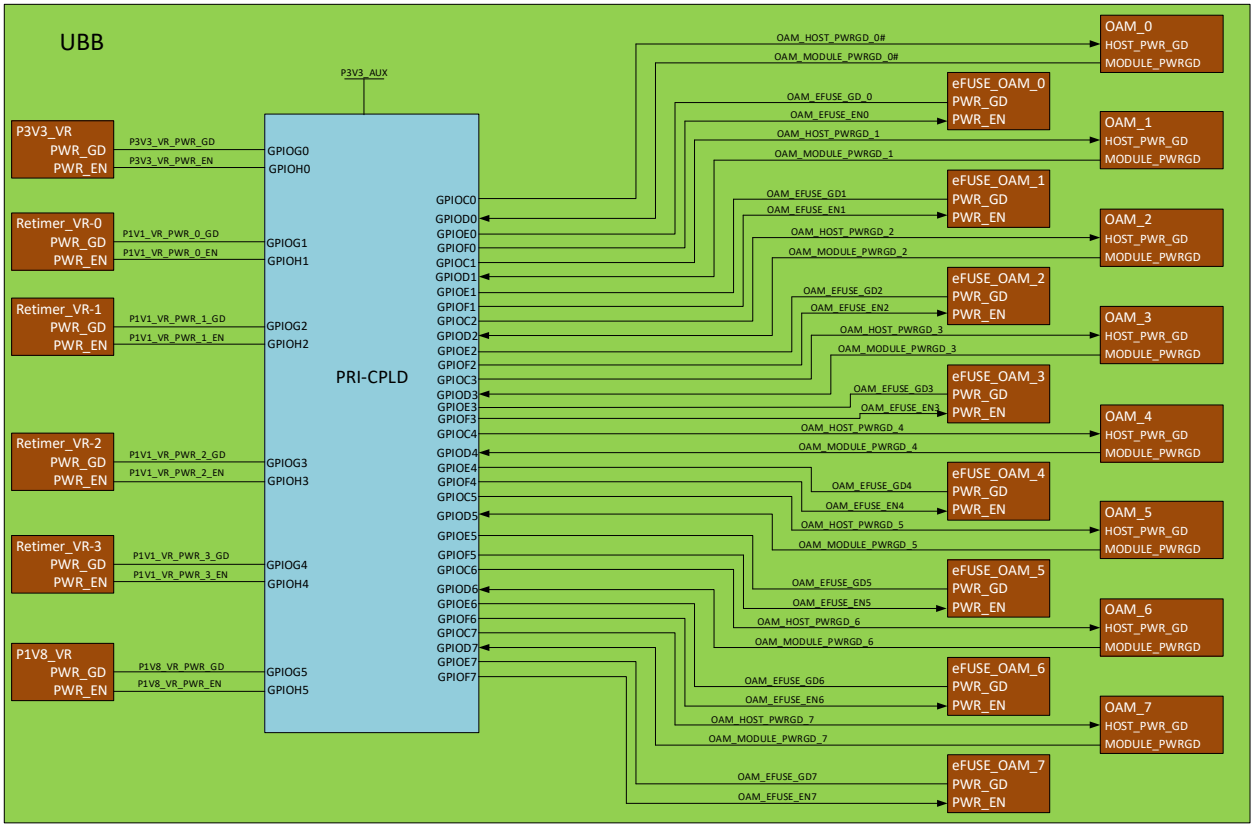


Figure 14 Power Control Block Diagram

6.1.6. Strap pins

6.1.6.1. Module ID

The following figure shows the MODULE_ID[4:0] strapping for physical orientation of modules when 8 interconnected Accelerators are used.

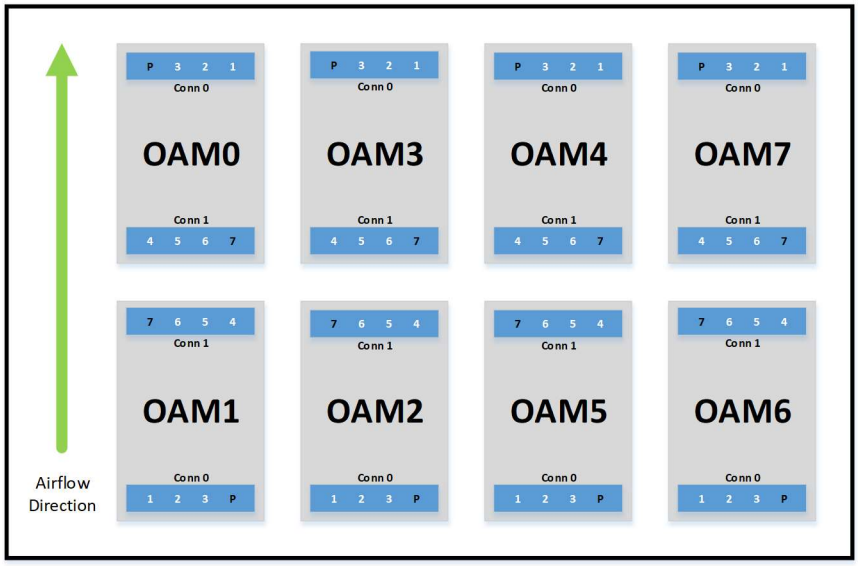


Figure 15 Required MODULE_ID[4:0] assignments for baseboards with 8 interconnected modules

Detail port to port assignment is based on system placement and routing length. Module to module interconnect may decrease to 4 ports if the module only supports 4. Module to module interconnect link may only utilize 8 lanes if the module defines 8 lanes per link.

The following Figure shows the required MODULE_ID[4:0] assignments when only 4 modules are connected as two rows of two.

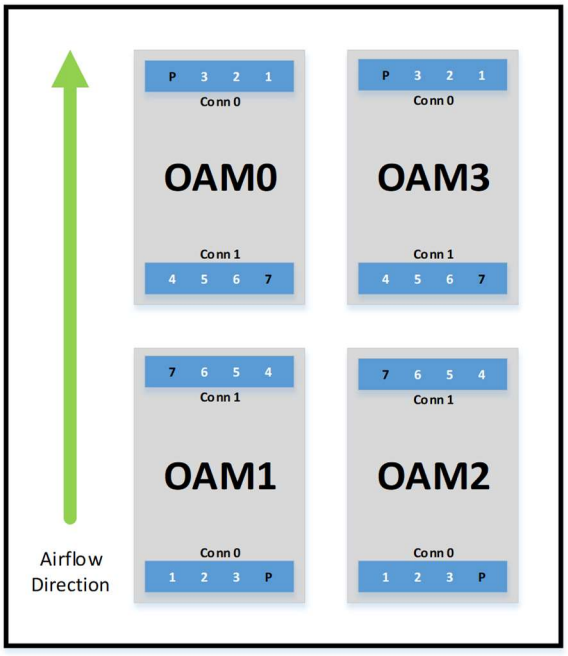


Figure 16 Module_ID[4:0] assignments when four only in two rows of two

MODULE_ID can be used as the I2C address strap pins if needed.

OAM	Module ID
OAM0	00000

OAM1	00001
OAM2	00010
OAM3	00011
OAM4	00100
OAM5	00101
OAM6	00110
OAM7	00111

Table 10 MODULE_ID

6.1.6.2. Link_Config[4:0]

The 5 link configuration strapping bits are pulled up on modules that use them. These bits are strapped to ground on the baseboard to select logic 0, or left floating on the baseboard to select logic 1. Some OAMs use these LINK_CONFIG[4:0] strapping bits to determine the interconnect topology for the links between modules and to determine the protocol of the "P" Link. Refer to Chapter 7.2 for details.

6.1.6.3. PE_BIF[1:0]

x16 Host Interface Bifurcation Configuration. This output of the module informs the host if it needs to bifurcate the PCIe interface to the module.

00 = one x16 PCIe host interface
01 = bifurcation into two x8 PCIe host interfaces
10 = bifurcation into four x4 PCIe host interfaces
11 = reserved

6.1.7. Debug interface

There are two OAM debug interfaces on UBB, one is JTAG and the other is UART interface. UART supports both microUSB local access or BMC's remote debug feature. BMC can access 8 OAM UART output at a time.

There is also one debug header on UBB to support OAM debug through dongle.

Below are JTAG, UART and debug header diagrams.

6.1.8. JTAG Interface

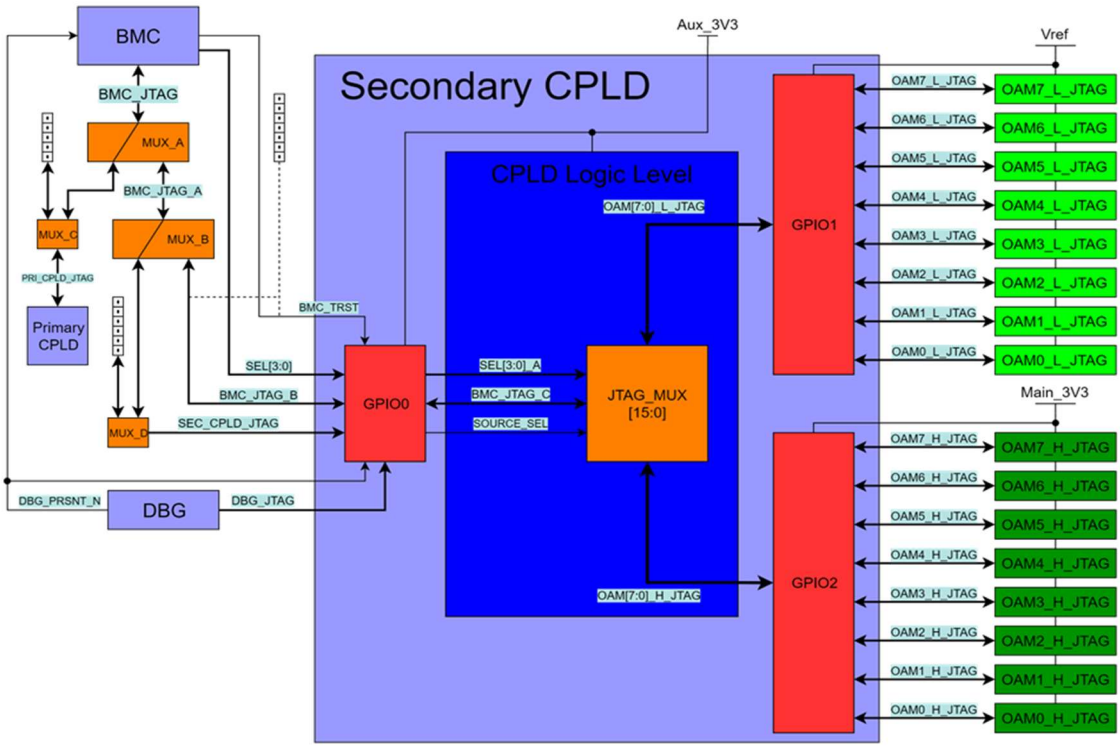


Figure 17 JTAG diagram

JTAG Truth Table:

MUX_A

SELECTION	DESCRIPTION	REMARK
LOW	PRI CPLD FW UPDATE	
HIGH	GO TO SEC CPLD	Default

MUX_B

SELECTION	DESCRIPTION	REMARK
LOW	UPDATE SEC CPLD	
HIGH	OAM JTAG CHAIN	Default

MUX_C

SELECTION	DESCRIPTION	REMARK
LOW	UPDATE BY HEADER	
HIGH	UPDATE BY BMC	Default

MUX_D

SELECTION	DESCRIPTION	REMARK

LOW	UPDATE BY HEADER	
HIGH	UPDATE BY BMC	Default

Table 11 JTAG Truth Table

6.1.9. UART

There are microUSB and BMC two interfaces for OAM UART access through USB Mux and USB Hub illustrated below. MicroUSB takes the priority if it is plugged. BMC be notified once a micro USB connector is plugged through USB_Mux_Sel signals on HIF_5 conenctor N8, O8 pins.

BMC console can see 8 OAM UART at a time.

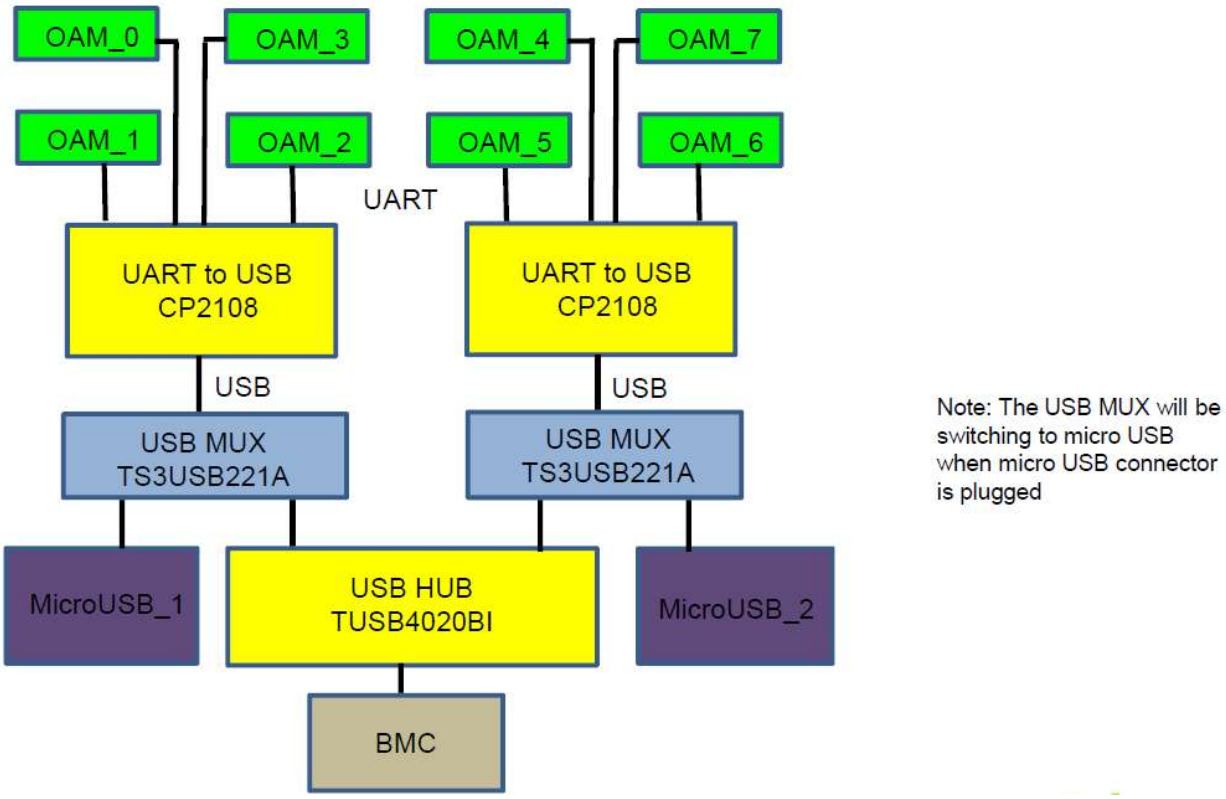


Figure 18 UART Diagram

6.1.10. Debug Header

There is a debug header combined proprietory debug interfaces from different OAM vendors by using OAM test pins. This debug header is optional in UBB spec. The header used in OAI UBB reference design is Molex 501190-4017 with pin definition below:

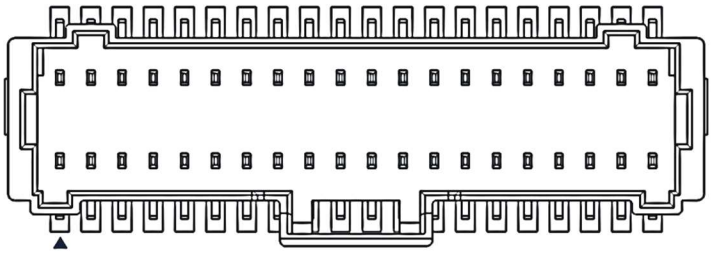


Figure 19 UBB reference board debug header

2	OAM_TEST_0	NC	1
4	OAM_TEST_1	NC	3
6	OAM_TEST_2	NC	5
8	OAM_TEST_3	NC	7
10	OAM_TEST_4	NC	9
12	OAM_TEST_5	NC	11
14	OAM_TEST_6	GND	13
16	OAM_TEST_7	GND	15
18	OAM_TEST_8	GND	17
20	OAM_TEST_9	GND	19
22	OAM_TEST_10	GND	21
24	OAM_TEST_11	JTAG_HOOK0	23
26	OAM_TEST_12	JTAG_HOOK6	25
28	OAM_TEST_13	JTAG_HOOK7	27
30	OAM_TEST_14	GND	29
32	GND	JTAG_TCK	31
34	NC	JTAG_TDO	33
36	VREF	JTAG_TRST	35
38	NC	JTAG_TDI	37
40	DEBUG_PRESENT_N	JTAG_TMS	39

Table 12 UBB debug header pin definition

6.1.11. UBB Power sequence

UBB board power sequence is diagramed below.

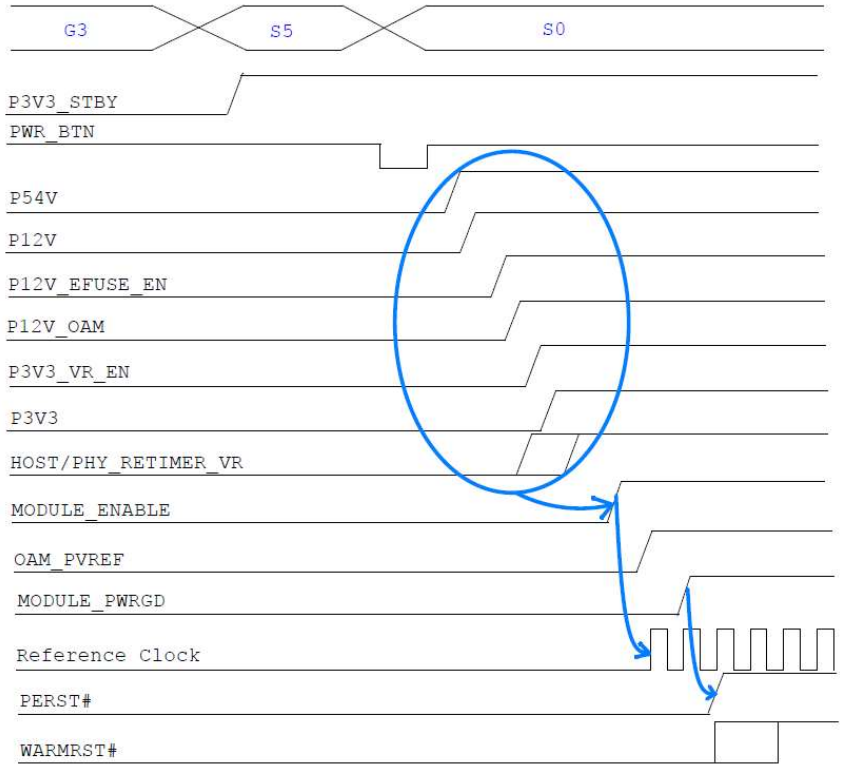


Figure 20 UBB Power on sequence

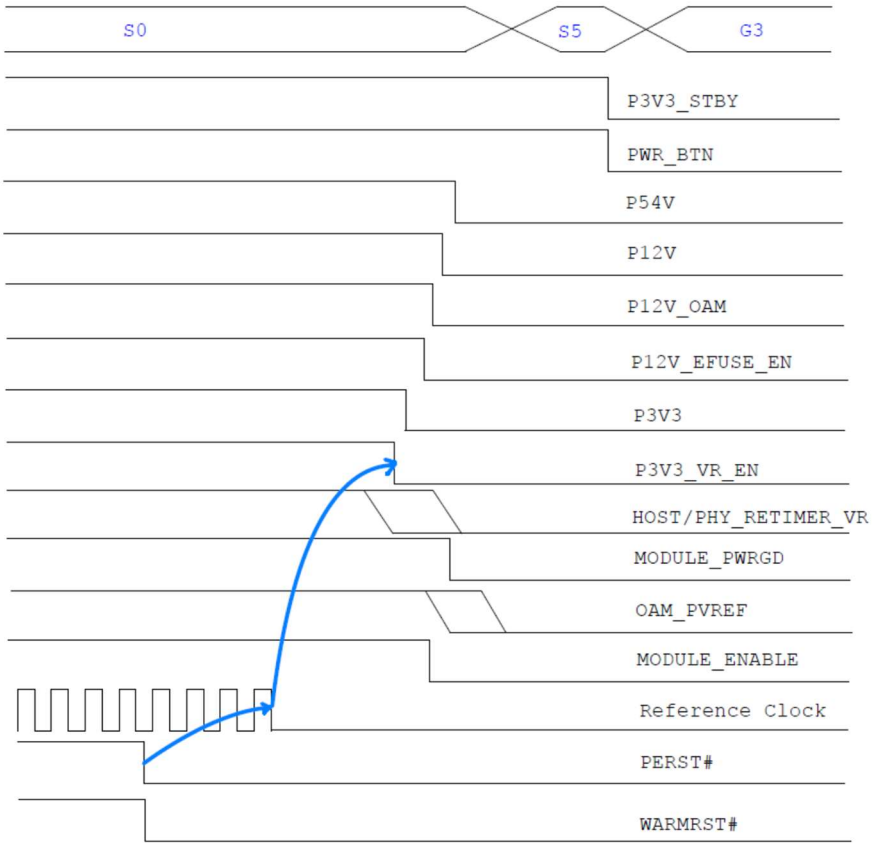


Figure 21 UBB Power down sequence

Notes:

1. All voltages on the UBB must be within specification before MODULE_ENABLE is asserted.
2. HOST/PHY_RETIMER_VR depends on system provider's design whether they are included in UBB design.
3. The MODULE_ENABLE is the UBB power good indication signal.
4. As the voltage planes on the UBB ramp up, the reference clocks from the UBB will begin to run.
5. After all the voltages on the module are within specification, the module asserts MODULE_PWRGD to the UBB.
6. At least 100ms after MODULE_PWRGD assertion, the UBB will de-assert the PCIe reset signal(PERST#) to the module.
7. The optional WARMRST# signal de-asserts at the same time or later than the PERST# signal is de-asserted.

6.1.12. FRU

Please refer to section 10.3 for detail FRU format. BMC controls MUX selection via BMC GPIO:

- When DC is off, BMC switches FRU1 access to BMC.
- When DC is on, BMC switches FRU1 access to OAM0

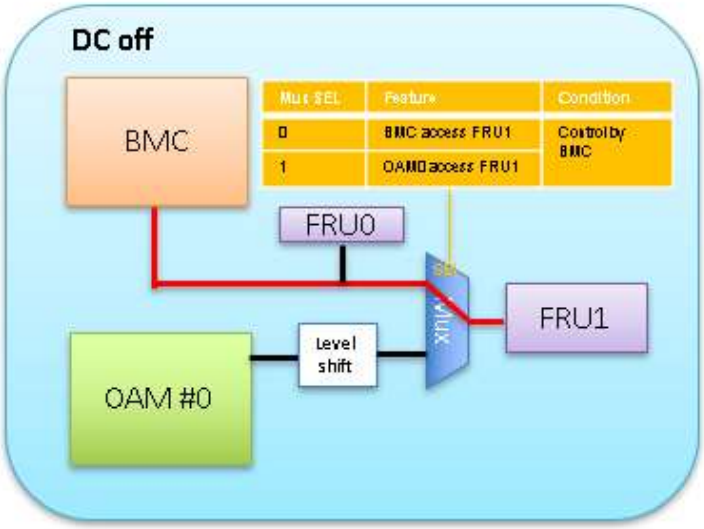


Figure 22 DC is off, BMC switches FRU1 access to BMC

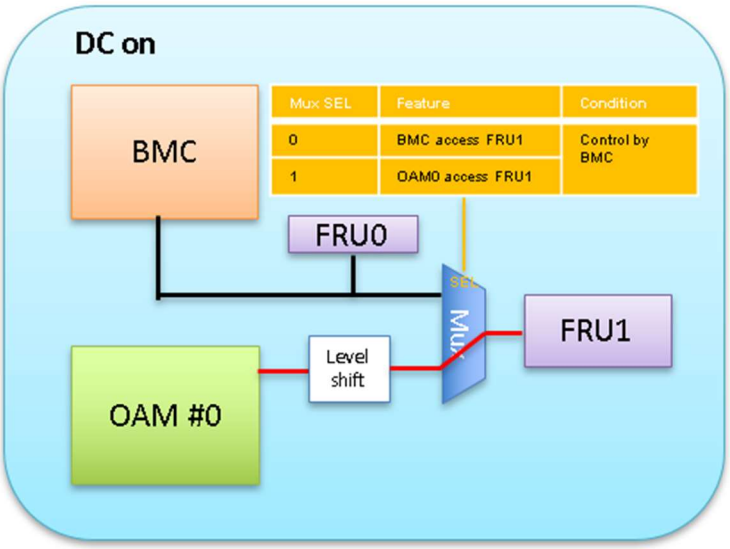


Figure 23 When DC is on, BMC switches FRU1 access to OAM0

Case 1: DC off

1. BMC switches MUX to BMC access.
2. If FRU0 is changed, copy FRU0 to FRU1

Case 2: DC on

1. BMC switches MUX to OAM #0.
2. OAM #0 to update link topology by FRU1.

Case 3: OAM reset

1. User send OAM reset command to BMC
2. BMC pulls down OAM reset and then switch MUX to BMC.
3. If FRU0 is changed, copy FRU0 to FRU1.
4. Switch MUX to OAM #0, and then release OAM reset signal.

Case 4: User update FRU0

1. User updated FRU0 via BMC OOB interface.
2. BMC stores these changes in FRU0, and wait for events of DC off or OAM reset.
3. DC off: use “Case 1: DC off” above to update FRU1.
4. OAM reset: use “Case 3: OAM reset” above to update FRU1.

6.2. UBB Connectors

UBB has 8 6x8 high density connectors, 16 OAM Mezz connectors, 8 OSFP-DD connectors for scale-out, 4 mechanical guide pins, 4 54V power connectors, 2 12V power connectors(can be repurposed for 54V power delivery, see 6.2.1.4), 2 microUSB UART ports. Details are outlined in the table below.

Board	Vendor	Vendor PN	Description	Q'ty	Desination	TYPE	R/V	Solder Type
UBB	Amphenol	10131762-101LF	High Density Connector	8	SW	Receptacle	RA	Press-Fit
	Molex	2093111115	OAM Connector	16	OAM Module	Mirror type	VT	SMT
	Amphenol	UE36-A 1070-3000T	QSFP-DD Connector	8	UBB	Receptacle	RA	SMT
	Amphenol	UE36B 16221-06A5A	QSFP-DD Cage	8	UBB	Receptacle	RA	Press-Fit
	Amphenol	10037909-101LF	Guide Pin	4	UBB	Receptacle	RA	Press-Fit
	Amphenol	10028917-001LF	54V Connector	4	SW	Header	RA	Press-Fit
	Amphenol	JX410-513xx	12V Connector	2	SW	Header	RA	Press-Fit
	ACES	59493-0050D-CH1	Micro USB Connector	2	UBB		RA	SMT

Table 13 UBB connector list

6.2.1. UBB Connector pin list

This chapter describes connectors including Host Interface, 12V power , 54V power, QSFP-DD, debug header.

6.2.1.1. QSFP-DD connector pin list

Each of QSFP-DD Tx and Rx are AC-coupled 100 ohm differential lines that shout be terminated with 100 ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the QSFP-DD module and not required on the Host board.

The QSFP-DD low speed electrical specifications are given in below table. This specification ensures compatibility between host bus masters and the I2C interface.

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3mA for fast mode, 20ma for Fast-mode plus
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	VCC*0.7	Vcc+0.5	V	
InitMode, ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
IntL	VOL	0	0.4	V	IOL=2.0mA

	VOH	VCC-0.5	VCC+0.3	V	10k ohms pull-up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC-0.5	VCC+0.3	V	ModPrsL can be implemented as a short-circuit to GND on the module

Table 14 QSFP-DD low speed electrical specifications

For detail QSFP-DD information, please refer to "QSFP-DD Hardware Specification for QSFP DOUBLE DENSITY 8X PLUGGABLE TRANSCEIVER – Rev 5.0."

QSFP-DD Connector 0~7 pin list (Input, Output are based on UBB side)

All signals direction below are based on UBB side

Signal	UBB Direction POV	Description	Voltage	Total Diff Pins	Total Single Pins
GND	GND	GND	GND		24
Vcc1	PWR	+3.3V Power supply	3.3V		1
Vcc2	PWR	3.3V Power Supply	3.3V		1
VccTx	PWR	+3.3V Power supply transmitter	3.3V		1
VccTx1	PWR	3.3V Power Supply	3.3V		1
VccRx	PWR	+3.3V Power Supply Receiver	3.3V		1
VccRx1	PWR	3.3V Power Supply	3.3V		
PETp/n [8:1]	Output	PCIe or equivalent link Transmit differential pairs. OAM module Transmit, QSFP-DD connector Receive.		16	16
PERp/n [8:1]	Input	PCIe or equivalent link Receive differential pairs. OAM module Receive, QSFP-DD connector Transmit.		16	16
I2C_SLV_D	Bi-directional	Slave I2C data	3.3V		1
I2C_SLV_CLK	Output	Slave I2C clock	3.3V		1
RESETL	Output	QSFP-DD Module Reset	3.3V		1
INTL	Input	QSFP-DD Module Interrupt	3.3V		1
MODSELL	Output	QSFP-DD Module Select	3.3V		1

MODPRSL	Input	QSFP-DD Module Present for inform OAM cable insert or not.	3.3V		1
INITMODE	Outut	**Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE**	3.3V		**1**

Table 15 QSFP-DD connector 0~7 pin list

6.2.1.2. 54V power connector pin list

Base on temperature rise under 30˚C, 18Amp per contact (POS).

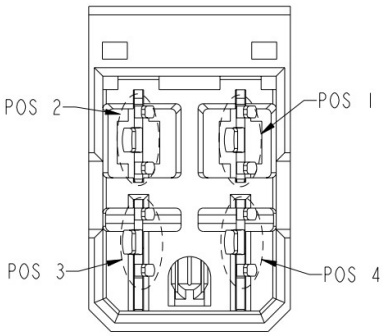


Figure 24 54V power connector

P54V_0 Pin Definition:

POS 1 & 2	54V_1	54V_0
POS 3 & 4	GND	GND

Table 16 P54V_0 Pin Definition

P54V_1 Pin Definition:

POS 1 & 2	54V_2	54V_3
POS 3 & 4	GND	GND

Table 17 P54V_1 Pin Definition

P54V_2 Pin Definition:

POS 1 & 2	54V_4	54V_5
POS 3 & 4	GND	GND

Table 18 P54V_2 Pin Definition

P54V_3 Pin Definition:

POS 1 & 2	54V_7	54V_6
POS 3 & 4	GND	GND

Table 19 P54V_3 Pin Definition

6.2.1.3. 12V power connector pin list

Base on temperature rise under 30˚C, 10Amp per contact (POS).

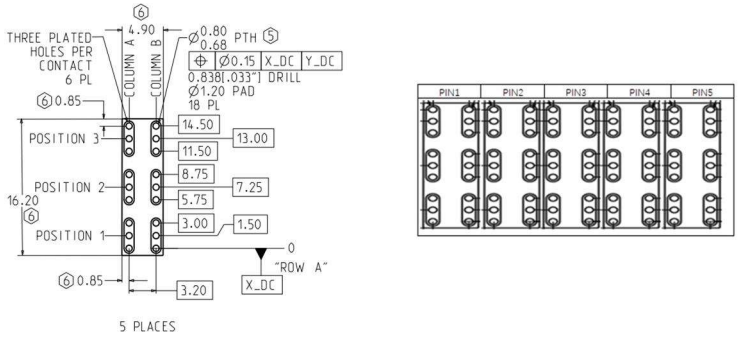


Figure 25 12V power connector pin list

P12V_0 CONN	PIN 1		PIN 2		PIN 3		PIN 4		PIN 5	
	COLMN A	COLMN B	COLMN A	COLMN B	COLMNA	COLMNB	COLMN A	COLMN B	COLMN A	COLMN B
POS3	P12V_VR1	P12V_VR1	P12V_VR1	P12V_VR1	P12V_UBB	P12V_UBB	P12V_VR0	P12V_VR0	P12V_VR0	P12V_VR0
POS2	P12V_VR1	P12V_VR1	GND	GND	P12V_UBB	GND	GND	GND	P12V_VR0	P12V_VR0
POS1	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND

Table 20 P12V_0 power connector pin list

P12V_1 CONN	PIN 1		PIN 2		PIN 3		PIN 4		PIN 5	
	COLMN A	COLMN B	COLMN A	COLMN B	COLMN A	COLMN B	COLMN A	COLMN B	COLMN A	COLMN B
POS3	P12V_VR2	P12V_VR2	P12V_VR2	P12V_VR2	GND	GND	P12V_VR3	P12V_VR3	P12V_VR3	P12V_VR3
POS2	P12V_VR2	P12V_VR2	GND	GND	GND	GND	GND	GND	P12V_VR3	P12V_VR3
POS1	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND

Table 21 P12V_1 power connector pin list

6.2.1.4. 12V power connector re-purpose for 54V

12V power connector (JX410-513xx) also can be used for 54V application in order to support more than 700W OAM, ODM should notice creepage and clearance design (see 11.3 in detail) for this connector, please refer to the suggestion pin list below:

P12V CONN	PIN 1		PIN 2		PIN 3		PIN 4		PIN 5	
	COLMN A	COLMN B	COLMN A	COLMN B	COLMN A	COLMN B	COLMN A	COLMN B	COLMN A	COLMN B
POS3	P54V	P54V	P54V	P54V	NC	NC	GND	GND	GND	GND
POS2	P54V	P54V	P54V	P54V	NC	NC	GND	GND	GND	GND
POS1	P54V	P54V	P54V	P54V	NC	NC	GND	GND	GND	GND

6.2.1.5. Host Interface Connector (HIF) pin list

This chapter describes Host Interface connector (HIF). There are 8 connectors. Signal direction of HIF0~7 in table below is based on UBB side. Detail pin map is in UBB spec package available on OAI WiKi:

https://www.opencompute.org/wiki/Server/OAI

HIF_0 connector (host interface can be opencapi or others)

High Speed Connector: (used when it is PCIE interface. For other interfaces, refer to other future section to be provided)

Signal	UBB Direction POV	Description	Voltage	Required or Optional	Total Diff Pins	Total Single Pins
GND		GND		Required		68
P3V3_AUX	Power input	3.3V AUX Power for UBB borad	3.3V	Required		4
PETp/n [15:0]	Output	PCIe or equivalent host link Transmit differential pairs. Module Transmit, Host Receive.		Required	32	32
PERp/n [15:0]	Input	PCIe or equivalent host link Receive differential pairs. Module Receive, Host Transmit.		Required	32	32
UBB_DETECT_LOOP		UBB board PRSNT pin. Pull down this pin with 100ohm resistor on HIB side.	3.3V	Required		1

Table 22 HIF_0 connector pin list

(*) Note: UBB_DETECT_LOOP on HIF_0 and on HIF_7 are same signal. This pin is to inform HIB BMC when UBB is detected. Connect this pin together on UBB side.

HIF_1 connector (host interface can be opencapi or others)

High Speed Connector: (used when it is PCIE interface. For other interfaces, refer to other future section to be provided)

Signal	UBB Direction POV	Description	Voltage	Required or Optional	Total Diff Pins	Total Single Pins
GND		GND		Required		64
PETp/n [15:0]	Output	PCIe or equivalent host link Transmit differential pairs. Module Transmit, Host Receive.		Required	32	32
PERp/n [15:0]	Input	PCIe or equivalent host link Receive differential pairs. Module Receive, Host Transmit.		Required	32	32
UART_SEL_0	Input	UART SEL pin	3.3V	Required		1
UART_SEL_1	Input	UART SEL pin	3.3V	Required		1
UART_SEL_2	Input	UART SEL pin	3.3V	Required		1
UART_MUX_EN_N	Input	UART MUX enable pin	3.3V	Required		1
BMC_MDC/MDIO	Bi-direction	MDC/MDIO signal.		Required		2

Table 23 HIF_1 connector pin list

HIF_2 connector (host interface can be opencapi or others)

High Speed Connector: (used when it is PCIE interface. For other interfaces, refer to other future section to be provided)

Signal	UBB Direction POV	Description	Voltage	Required or Optional	Total Diff Pins	Total Single Pins
GND		GND		Required		64
PETp/n [15:0]	Output	PCIe or equivalent host link Transmit differential pairs. Module Transmit, Host Receive.		Required	32	32

PERp/n [15:0]	Input	PCIe or equivalent host link Receive differential pairs. Module Receive, Host Transmit.		Required	32	32
CLK_100M_OAM_DP/N	Input	PCIe Reference Clock for OAM. 100MHz PCIe Gen 4 compliant.		Required	1	2
CLK_100M_RETIMER_DP/N	Input	PCIe Reference Clock for retimer. 100MHz PCIe Gen 4 compliant.		Required	1	2
CLK_100M_OAM_AUX_DP/N	Input	PCIe Reference Clock for Aux. 100MHz PCIe Gen 4 compliant.		Required	1	2
I2C_EFUSE_FRU_AUX_SDA	Bi-directional	I2C for each 12V EFUSE	3.3V	Required	0	2
I2C_OAM_SLAVE_AUX_SDA/SCL	Bi-directional	I2C for each OAM	3.3V	Required	0	2
I2C_GEN_BUFFER_AUX_SDA	Bi-directional	I2C for each clock Gen and Buffer	3.3V	Required	0	2
I2C_CPLD_TEMP_AUX_SDA	Bi-directional	I2C for each temperature sensor and CPLD.	3.3V	Required	0	2
I2C_CPLD_FW_AUX_SDA	Bi-directional	I2C for each CPLD FW update.	3.3V	Required	0	2
UART_TXD	Output	Serial Port Transmit	3.3V	Required	0	1
UART_RXD	Input	Serial Port Receive	3.3V	Required	0	1
JTAG_MUX_EN_N	Input	JTAG MUX enable pin	3.3V	Required	0	2
JTAG_MUX_SEL	Input	JTAG MUX SEL pin	3.3V	Required	0	2
BMC_JTAG_SELECT_[3:0]	Input	JTAG SEL to CPLD pin	3.3V	Required	0	4

PWR_BTN	Input	Power BTN to UBB board	3.3V	Required	0	1
I2C_OAM_SLAVE_AUX_ALERT_N	Output	Slave I2C alert indication	3.3V	Required	0	1
I2C_EFUSE_FRU_AUX_ALERT_N	Output	I2C ALERT for each 12V eFuse.	3.3V	Required	0	1
I2C_CPLD_TEMP_AUX_ALERT_N	Output	2C ALERT for each temperature sensor.	3.3V	Required	0	1
CPLD_PRI_FW_UPDATE_EN_N	Input	Enable PRI CPLD FW update.	3.3V	Required	0	1
CPLD_SEC_FW_UPDATE_EN_N	Input	Enable SEC CPLD FW update.	3.3V	Required	0	1

Table 24 HIF_2 connector pin list

HIF_3 connector (host interface can be opencapi or others)

High Speed Connector: (used when it is PCIE interface. For other interfaces, refer to other future section to be provided)

Signal	UBB Direction POV	Description	Voltage	Required or Optional	Total Diff Pins	Total Single Pins
GND		GND		Required		64
PETp/n [15:0]	Output	PCIe or equivalent host link Transmit differential pairs. Module Transmit, Host Receive.		Required	32	32
PERp/n [15:0]	Input	PCIe or equivalent host link Receive differential pairs. Module Receive, Host Transmit.		Required	32	32
RSV_BMC_PRI_CPLD[15:1]	Bi-directional	RSVD GPIO between BMC and CPLD	3.3V	Option		15
RSV_PETp/n [3:0]	Output	RSVD for PCIe interface		Option	8	8
RSV_PERp/n	Input	RSVD for PCIe interface		Option	8	8

[3:0]						
UBB_PWR_READY	Output	UBB power ready to HIB BMC	3.3V	Required	0	1

Table 25 HIF_3 connector pin list

HIF_4 connector (host interface can be opencapi or others)

High Speed Connector: (used when it is PCIE interface. For other interfaces, refer to other future section to be provided)

Signal	UBB Direction POV	Description	Voltage	Required or Optional	Total Diff Pins	Total Single Pins
GND		GND		Required		64
PETp/n [15:0]	Output	PCIe or equivalent host link Transmit differential pairs. Module Transmit, Host Receive.		Required	32	32
PERp/n [15:0]	Input	PCIe or equivalent host link Receive differential pairs. Module Receive, Host Transmit.		Required	32	32
WARMRST#	Input	Warm Reset	3.3V	Option		4
JTAG_TMS	Input	Low Voltage ASIC/GPU JTAG Test Mode Select	3.3V	Required		1
JTAG_TDI	Input	JTAG master data output	3.3V	Required		1
JTAG_TCK	Input	ARM JTAG clock output	3.3V	Required		1
JTAG_TDO	Output	JTAG master data input	3.3V	Required		1
JTAG_TRST	Input	JTAG master reset output	3.3V	Required		1
SW[3:0]_PE_RESET_N	Input	RSVD SW to UBB CPLD sideband signal for PERESET_N	3.3V	Option		4
RSV_BMC_SEC_CPLD[3:0]	Bi-direction	RSVD GPIO between BMC and CPLD	3.3V	Option		4

	al					
FRU_SEL	Input	Level shift IC enable pin	3.3V	Required		1
OAM_PWRBRK_N	Input	Emergency power reduction. CEM Compliant Power Brake	3.3V	Required		1
UBB_FRU[1:0]_WP	Input	Signal for BMC to control UBB FRU write-protect function	3.3V	Required		2

Table 26 HIF_4 connector pin list

HIF_5 connector (host interface can be opencapi or others)

High Speed Connector: (used when it is PCIE interface. For other interfaces, refer to other future section to be provided)

Signal	UBB Direction POV	Description	Voltage	Required or Optional	Total Diff Pins	Total Single Pins
GND		GND		Required		64
PETp/n [15:0]	Output	PCIe or equivalent host link Transmit differential pairs. Module Transmit, Host Receive.		Required	32	32
PERp/n [15:0]	Input	PCIe or equivalent host link Receive differential pairs. Module Receive, Host Transmit.		Required	32	32
USB_MUX_SEL_[1:0]	Input	For USB Mux selection	3.3V	Optional	0	2
SGPIO_CLK/ LOAD/DIN/ DOUT	Bi-direction	SGPIO signal for UBB CPLD to BMC		Optional	0	4

CLK_100M_NVSW_DP/N	Input	For NVSW clock		Optional	1	2
USB_DP/M_DN[1:0]	Bi-directional	USB signal		Optional	2	4

Table 27 HIF_5 connector pin list

HIF_6 connector (host interface can be opencapi or others)

High Speed Connector: (used when it is PCIE interface. For other interfaces, refer to other future section to be provided)

Signal	UBB Direction POV	Description	Voltage	Required or Optional	Total Diff Pins	Total Single Pins
GND		GND		Required		64
PETp/n [15:0]	Output	PCIe or equivalent host link Transmit differential pairs. Module Transmit, Host Receive.		Required	32	32
PERp/n [15:0]	Input	PCIe or equivalent host link Receive differential pairs. Module Receive, Host Transmit.		Required	32	32

Table 28 HIF_6 connector pin list

HIF_7 connector (host interface can be opencapi or others)

High Speed Connector: (used when it is PCIE interface. For other interfaces, refer to other future section to be provided)

Signal	UBB Direction POV	Description	Voltage	Required or Optional	Total Diff Pins	Total Single Pins
GND		GND		Required		64
PETp/n [15:0]	Output	PCIe or equivalent host link Transmit differential pairs. Module Transmit, Host		Required	32	32

		Receive.				
PERp/n [15:0]	Input	PCIe or equivalent host link Receive differential pairs. Module Receive, Host Transmit.		Required	32	32
UBB_DETECT_LOOP (*)		UBB board PRSNT pin. Connect directly with UBB_DETECT_LOOP pin on HIF_7 on UBB. Pull up with 4.7k ohm resistor on HIB side and connect to BMC with a level shift.	3.3V	Required		1

Table 29 HIF_7 connector pin list

***Note:** UBB_DETECT_LOOP is the same signal as it is defined in HIF_0. Connect these two pins together on UBB side.

6.2.1.6. OAM Debug connector pin list

Molex 501190-4017 is selected, total pin count is 40pin

Current – Maximum per contact is 1A

Voltage – Maximum is 50V AC (RMS)/DC

All signals direction are based on UBB side

Signal	UBB Direction POV	Description	Voltage	Required or Optional	Pin Assignment	Total Single Pins
GND		GND		Required	13,15,17,19,21,29,32	7
JTAG_TMS	Input	Low Voltage ASIC/GPU JTAG Test Mode Select	Vref(OAM)	Required	39	1
JTAG_TDI	Input	JTAG master data output	Vref(OAM)	Required	37	1
JTAG_TCK	Input	ARM JTAG clock output	Vref(OAM)	Required	31	1

JTAG_TDO	Output	JTAG master data input	Vref(OAM)	Required	33	1
JTAG_TRST	Input	JTAG master reset output	Vref(OAM)	Required	35	1
DEBUG_PRESENT_N	Input	Present of debug connector	3.3V	Required	40	1
P1V8 (*)	Power input	Power for debug connector	Vref(OAM)	Required	36	1
Hook[0]	Output	Debug signals	3.3V	Required	23	1
Hook[6,7]	Output	Debug signals	Vref(OAM)	Required	25,27	2
OAM_TEST[0-14]	Input/Output	Debug signals	Vref(OAM)	Required	2,4,6,8,10,12,14,16,18,20,22,24,26,28,30	15
NC					1,3,5,7,9,11,34,38	8

Table 30 OAM Debug connector pin list

***Note:** This power pin is for debug connector, ODM should design the using voltage based on its debug tool.

6.3. PCB Stack-Up

This section describe OAM UBB reference board stack-up and requirements. The OAI UBB reference boards uses a 22 PCB stack-up with ultra low loss material. In order to support high TDP OAM(54V/48V up to 500w, 12V up to 300w) and high interconnect speed(up to 28Gbps NRZ or 56Gbps PAM4), the PCB stack up adheres to the following requirements:

- PCB with up to two 2oz layers was selected to meet required copper density
- 85 & 90 Ohms differential traces in internal signal layers as needed.
- 45 & 50 Ohms or single ended traces as needed (Depend on chip vendor's design guide)
- PCB material is depended on maximum trace length of topology design and to meet vendor's channel loss criteria (ex. -30dB@14GHz for Intel OAM module).
- Back Drilling for signals on Layer 16, 14, 9, 5 and 3 to remove stubs from SerDes and PCI-e Gen4 via transitions. Limit back drilling to 1mm from top layer to help press fit contact.

UBB reference board uses the below stackup. Each vendor needs to fine tune the width/spacing design based on material target and impedance control table below.

Layer	Plane Description		Copper (OZ)	Thickness (mil)
		Solder mask		0.5
L1	Top	Signal/PWR	0.5oz + plating	1.9
		PrePreg		2.6
L2	GND1	Ground	1.0	1.2
		Core (1/1)		4

L3	IN1	Signal/PWR	1.0	1.2
		PrePreg		5
L4	GND2	Ground	1.0	1.2
		Core (1/1)		4
L5	IN2	Signal/PWR	1.0	1.2
		PrePreg		5
L6	GND3	Ground	1.0	1.2
		Core (1/1)		4
L7	IN3	Signal/PWR	1.0	1.2
		PrePreg		5
L8	GND4	Ground	1.0	1.2
		Core (1/1)		4
L9	IN4	Signal/PWR	1.0	1.2
		PrePreg		5
L10	GND5	Ground	1.0	1.2
		Core (1/2)		4
L11	VCC1	Power	2.0	2.4
		PrePreg		12
L12	VCC2	Power	2.0	2.4
		Core (1/2)		4
L13	GND6	Ground	1.0	1.2
		PrePreg		5
L14	IN5	Signal/PWR	1.0	1.2
		Core (1/1)		4
L15	GND7	Ground	1.0	1.2
		PrePreg		5
L16	IN6	Signal/PWR	1.0	1.2
		Core (1/1)		4
L17	GND8	Ground	1.0	1.2
		PrePreg		5
L18	IN7	Signal/PWR	1.0	1.2
		Core (1/1)		4
L19	GND9	Ground	1.0	1.2
		PrePreg		5
L20	IN8	Signal/PWR	1.0	1.2
		Core (1/1)		4
L21	GND10	Ground	1.0	1.2
		PrePreg		2.6
L22	BOT	Signal/PWR	0.5oz + plating	1.9
		Solder Mask		0.5
		Total		128.4 mil (with +/- 10% tolerance)

Table 31 UBB reference Stack-Up

Trace Width (mil)	Air Gap Spacing (mil)	Impedance Type	Layer	Impedance Target (ohm)	Tolerance (+/- %)
6.0		Single-Ended	1,22	45	10%
5.3		Single-Ended	1,22	50	10%
5.3	5.6	Differential	1,22	85	10%
4.8	6.1	Differential	1,22	90	10%
5.8		Single-Ended	3,5,7,9,14,16,18,20	45	10%
5.0		Single-Ended	3,5,7,9,14,16,18,20	50	10%
5.7	5.2	Differential	3,5,7,9,14,16,18,20	85	10%
5.0	5.8	Differential	3,5,7,9,14,16,18,20	90	10%

Table 32 UBB Impedance control

6.4. CPLD

6.4.1. Block Diagram of UBB Primary CPLD

The primary CPLD is working for UBB control without testing and debug signal function

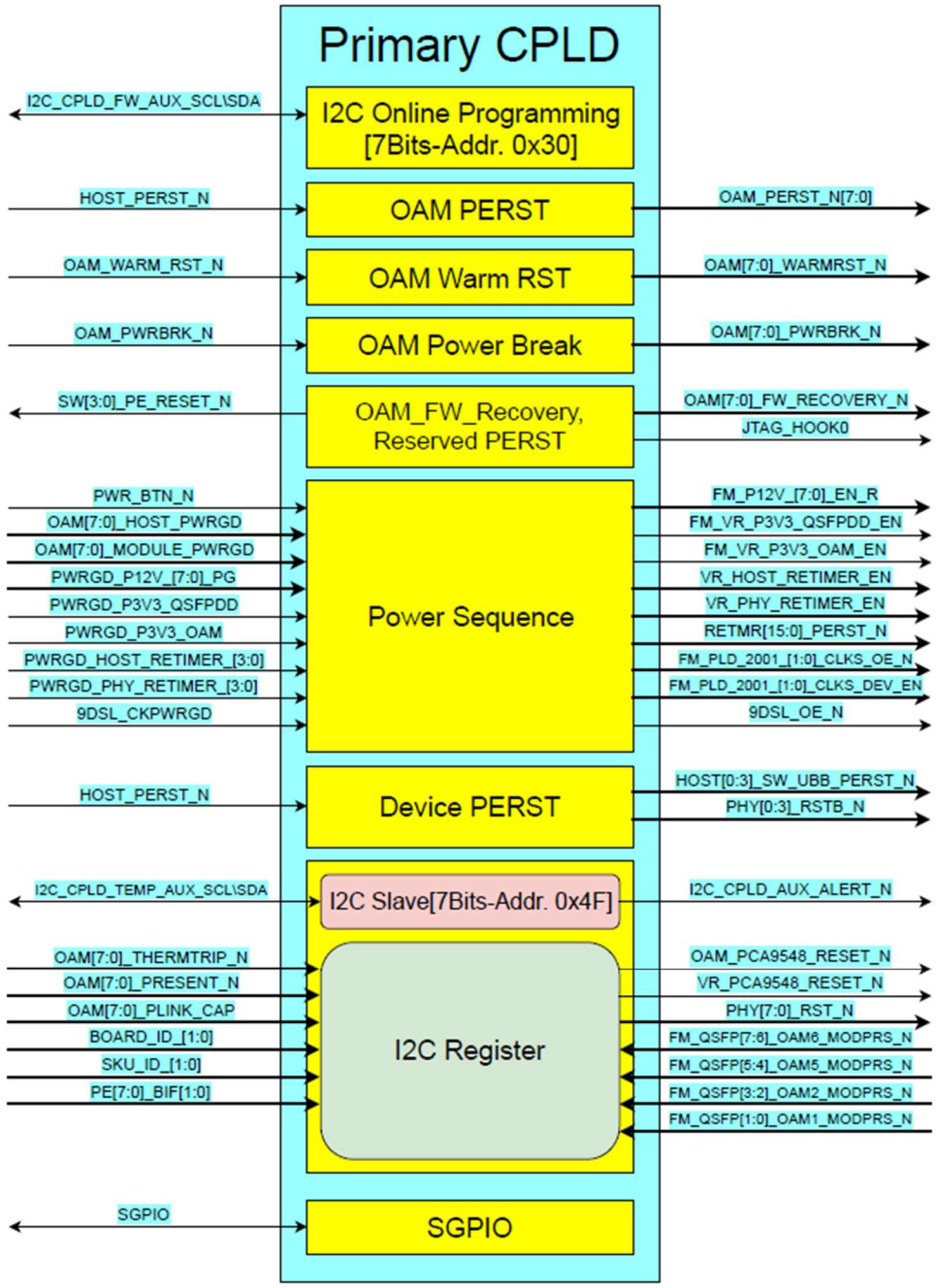


Figure 26 Priminary CPLD diagram

The above is block diagram of UBB primary CPLD with features below :

1. Primary CPLD I2C online programming feature.

2. Fan-out signal to 8 OAMs:

- OAM PERST from host PCIE
- OAM Warm Reset from host
- OAM power brake from host interface board (HIB)

3. Power sequence, power control state machine.

4. Slave I2C address for HIB.

5. OAM FW recovery

6. CPLD FW update via JTAG

7. Reserved PERST for multi-host

6.4.2. Primary I2C Online Programming Feature

User can program the CPLD through BMC after the CPLD enters the user mode.

Specification of I2C Programming Slave is as follows.

I2C Slave Address	7Bit[0x30]
I2C Bus Performance	400KHz
I2C Port	PT18C(SCL) PT18D(SDA)
Port Hysteresis	450mV

Table 33 Primary COLD I2C Programming Slave

6.4.3. Fan-out signal to 8 OAMs

CPLD receives the PERST, Warm_RST and PWRBRK signals from host interface board, and then fan out 8-way to the outputs to the 8 OAMs, shown as below.

Module	Input	Fan Out
OAM_PERST	HOST_PERST_N	OAM[7:0]_PERST_N
OAM_Warm_Reset	OAM_WARM_RST_N	OAM[7:0]_WARMRST_N
OAM_Power_Break	OAM_PWRBRK_N	OAM[7:0]_PWRBRK_N

Table 34 Primary CPLD Fan-out to OAMs

6.4.4. Slave I2C address for HIB

The UBB primary CPLD has an I2C slave to provide the BMC read/write.The UBB primary CPLD has an I2C slave to provide the BMC read/write.The specification of the I2C slave is as follows.

I2C Slave Address	7Bit[0x4F]
I2C Bus Performance	400KHz
I2C Port	PR3C(SCL) PR3D(SDA)
Port Hysteresis	450mV

Table 35 Priminary CPLD Slave I2C address for HIB

The Register Map of the I2C Slave

Addr.	Bit	Signal Name	R/W	Def.	Note
0x09	7	1'b0	RO	-	
	6	JTAG_HOOK0	RO	-	
	5	BOARD_ID_[1:0]	RO	-	
	4		RO	-	
	3	SKU_ID_[1:0]	RO	-	
	2		RO	-	
	1	OAM_PCA9548_RESET_N	R/W	-	
	0	VR_PCA9548_RESET_N	R/W	-	
0x08	7	FM_QSFP7_OAM6_MODPRS_N	RO	-	Indicate QSFP_DD cable is plugged or not. Need to add a level shift between QSFP-DD connector and CPLD.
	6	FM_QSFP6_OAM6_MODPRS_N	RO	-	
	5	FM_QSFP5_OAM5_MODPRS_N	RO	-	
	4	FM_QSFP4_OAM5_MODPRS_N	RO	-	
	3	FM_QSFP3_OAM2_MODPRS_N	RO	-	
	2	FM_QSFP2_OAM2_MODPRS_N	RO	-	
	1	FM_QSFP1_OAM1_MODPRS_N	RO	-	
	0	FM_QSFP0_OAM1_MODPRS_N	RO	-	
0x07	7	OAM7_FW_RECOVERY_N	R/W	-	Reserved for future.
	6	OAM6_FW_RECOVERY_N	R/W	-	
	5	OAM5_FW_RECOVERY_N	R/W	-	
	4	OAM4_FW_RECOVERY_N	R/W	-	
	3	OAM3_FW_RECOVERY_N	R/W	-	
	2	OAM2_FW_RECOVERY_N	R/W	-	
	1	OAM1_FW_RECOVERY_N	R/W	-	
	0	OAM0_FW_RECOVERY_N	R/W	-	
0x06	7	PHY7_RST_N	R/W	-	Reserved for future.
	6	PHY6_RST_N	R/W	-	

	5	PHY5_RST_N	R/W	-	
	4	PHY4_RST_N	R/W	-	
	3	PHY3_RST_N	R/W	-	
	2	PHY2_RST_N	R/W	-	
	1	PHY1_RST_N	R/W	-	
	0	PHY0_RST_N	R/W	-	
0x05	7	OAM_PE7_BIF[1:0]	RO	-	These pin inicate each OAM PCIe bifurcation. It should add a level shift between OAM and CPLD. On OAM side, voltage level is VREF.
	6				
	5	OAM_PE6_BIF[1:0]	RO	-	
	4				
	3	OAM_PE5_BIF[1:0]	RO	-	
	2				
	1	OAM_PE4_BIF[1:0]	RO	-	
	0				
0x04	7	OAM_PE3_BIF[1:0]	RO	-	These pin inicate each OAM PCIe bifurcation. It should add a level shift between OAM and CPLD. On OAM side, voltage level is VREF.
	6				
	5	OAM_PE2_BIF[1:0]	RO	-	
	4				
	3	OAM_PE1_BIF[1:0]	RO	-	
	2				
	1	OAM_PE0_BIF[1:0]	RO	-	
	0				
0x03	7	OAM7_PLINK_CAP	RO	Lo	Indicate port module capability support.
	6	OAM6_PLINK_CAP	RO	Lo	
	5	OAM5_PLINK_CAP	RO	Lo	
	4	OAM4_PLINK_CAP	RO	Lo	
	3	OAM3_PLINK_CAP	RO	Lo	

	2	OAM2_PLINK_CAP	RO	Lo	
	1	OAM1_PLINK_CAP	RO	Lo	
	0	OAM0_PLINK_CAP	RO	Lo	
0x02	7	OAM7_PRESENT_N	RO	Hi	OAM module present pin.
	6	OAM6_PRESENT_N	RO	Hi	
	5	OAM5_PRESENT_N	RO	Hi	
	4	OAM4_PRESENT_N	RO	Hi	
	3	OAM3_PRESENT_N	RO	Hi	
	2	OAM2_PRESENT_N	RO	Hi	
	1	OAM1_PRESENT_N	RO	Hi	
	0	OAM0_PRESENT_N	RO	Hi	
0x01	7	OAM7_THERMTRIP_N	RO	Hi	These pins indicate each OAM has catastropic thermal event. Active low and latched by module until power recycle.
	6	OAM6_THERMTRIP_N	RO	Hi	
	5	OAM5_THERMTRIP_N	RO	Hi	
	4	OAM4_THERMTRIP_N	RO	Hi	
	3	OAM3_THERMTRIP_N	RO	Hi	
	2	OAM2_THERMTRIP_N	RO	Hi	
	1	OAM1_THERMTRIP_N	RO	Hi	
	0	OAM0_THERMTRIP_N	RO	Hi	
0x00	7	CPLD_REVISION[7:0]	RO	8'h00	Current CPLD Revision.
	6				
	5				
	4				
	3				
	2				
	1				
	0				

Table 36 Priminary CPLD I2C slave register map

6.4.5. Reserved PERST for Multi-host

Reserved "SW[3:0]_PE_RESET_N" signals for future.

6.5. Block Diagram of UBB Secondary CPLD

The UBB on-board secondary CPLD provide the following debug function.

- The CPLD connects with both High and low voltage JTAG connection for OAM internal debug and ROM flash.
- The management device (ex BMC) remote debug through JTAG interface.
- UBB on-board implements a JTAG connector to CPLD for all OAM or individual OAM debug.
- All testing pin of OAM have connected to CPLD, the is reserved for flexible debug for other OAM signal usage.

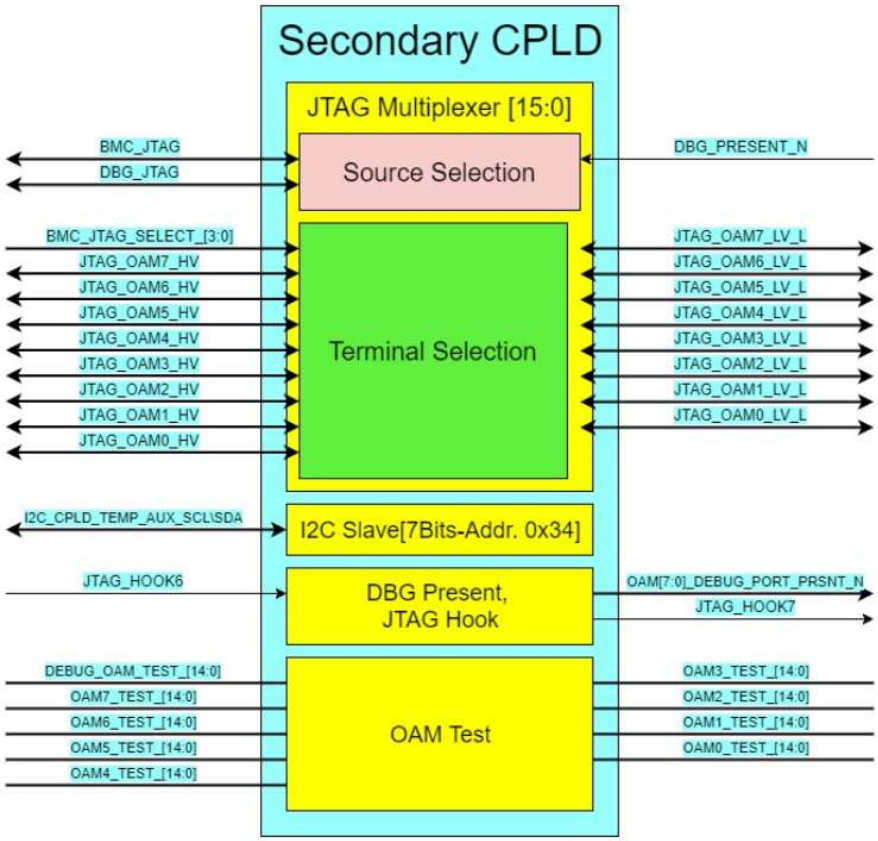


Figure 27 Secondary CPLD Diagram

The above is the block diagram of the UBB secondary CPLD with features:

1. JTAG and debug present.

2. OAM test pins

3. I2C Slave.

4. JTAG multiplexer of OAM.

6.5.1. JTAG and debug present

This module is 1 to 8 buffer gate structures.

Receive an input signal and then fan out 8-way to the output.

Input	Fan Out
Debug_Present_N	OAM[7:0]_DEBUG_PORT_PRSNT_N

Table 37 JTAG debug present

6.5.2. OAM Test Pins

OAM test pins go to CPLD and gather to debug header for debug purpose. Below is pin list of these 14 test pins.

Signal	Module Direction POV	Description	Voltage	Required or Optional
OAM_TEST0	Output	Test pin	V_{ref}	Optional
OAM_TEST1	Output	Test pin	V_{ref}	Optional
OAM_TEST2	Output	Test pin	V_{ref}	Optional
OAM_TEST3	Output	Test pin	V_{ref}	Optional
OAM_TEST4	Output	Test pin	V_{ref}	Optional
OAM_TEST5	Input/Output	Test pin	V_{ref}	Optional
OAM_TEST6	Input/Output	Test pin	V_{ref}	Optional
OAM_TEST7	Input	Test pin	V_{ref}	Optional
OAM_TEST8	Output	Test pin	V_{ref}	Optional
OAM_TEST9	Output	Test pin	V_{ref}	Optional
OAM_TEST10	Output	Test pin	V_{ref}	Optional
OAM_TEST11	Input	Test pin	V_{ref}	Optional
OAM_TEST12	Output	Test pin	V_{ref}	Optional
OAM_TEST13	Output	Test pin	V_{ref}	Optional
OAM_TEST14	Output	Test pin	V_{ref}	Optional

Table 38 OAM test pins definition

6.5.3. I2C Slave of Secondary CPLD

The UBB secondary CPLD has a user I2C slave which is a 3.3V base to provide BMC read/write path to CPLD.

The specification of the user I2C slave is as follows.

I2C Slave Address	7Bit[0x34]
I2C Bus Performance	400KHz
I2C Port	PT20C(SCL) PT20D(SDA)
Port Hysteresis	450mV

Table 39 Secondary CPLD I2C Slave spec

6.5.4. JTAG Multiplexer of OAM

This module provides BMC control the multiplexer for connecting which OAM.

Source Selection	
DBG_PRSNT_N	Result
1'b1	BMC_JTAG
1'b0	DBG_JTAG

Table 40 JTAG multiplexer of OAM

Terminal Selection	
SEL[3:0]	Result
4'hF	Connect to OAM7_H_JTAG
4'hE	Connect to OAM6_H_JTAG
4'hD	Connect to OAM5_H_JTAG
4'hC	Connect to OAM4_H_JTAG
4'hB	Connect to OAM3_H_JTAG
4'hA	Connect to OAM2_H_JTAG
4'h9	Connect to OAM1_H_JTAG
4'h8	Connect to OAM0_H_JTAG
4'h7	Connect to OAM7_L_JTAG
4'h6	Connect to OAM6_L_JTAG
4'h5	Connect to OAM5_L_JTAG
4'h4	Connect to OAM4_L_JTAG
4'h3	Connect to OAM3_L_JTAG
4'h2	Connect to OAM2_L_JTAG
4'h1	Connect to OAM1_L_JTAG
4'h0	Connect to OAM0_L_JTAG

Table 41 JTAG multiplexer terminal Selection

6.5.5. CPLD Pin list

This section tabulates all the CPLD pin list, including Primary and secondary CPLDs.

Primary CPLD pin list

Signal	UBB Direction POV	Description	Voltage	Required or Optional	Total Single Pins
VCC_3V3_PRI	Power input	Vcc core power of primary CPLD	3.3V	Required	9
VCCIO1_PRI	Power input	Vccio power of primary CPLD	3.3V	Required	14
VCCIO2_PRI	Power input	Vccio power of primary CPLD	1.2~3.3V*	Required	2
OAM[7:0]_PE_BIF_0	Input	x16 Host Interface Bifurcation Configuration. This output of the module informs the host if it needs to bifurcate the PCIe interface to the module. 00 = one x16 PCIe host interface 01 = bifurcation into two x8 PCIe host interfaces 10 = bifurcation into four x4 PCIe host interfaces 11 = reserved" Tied to GND on module for logic 0, leave open on module for logic 1; pull up on baseboard	Vref(OAM)	Required	8
OAM[7:0]_PE_BIF_1	Input	x16 Host Interface Bifurcation Configuration. This output of the module informs the host if it needs to bifurcate the PCIe interface to the module. 00 = one x16 PCIe host interface 01 = bifurcation into two x8 PCIe host interfaces 10 = bifurcation into four x4 PCIe host interfaces 11 = reserved" Tied to GND on module for logic 0, leave open on module for logic 1; pull up on baseboard	Vref(OAM)	Required	8
OAM[7:0]_PLINK_CAP	Input	"P" Port Module Capability support: '0' = PCIe only support '1' = Alternate protocol supported The host system requests an alternate host link protocol by pulling up LINK_CONFIG[0] and the Module informs the system of protocol support	Vref(OAM)	Required	8

		on the "P" link via this pin. If the module only supports PCIe as host, this signal is grounded on the module.			
OAM[7:0]_PRESENT_N	Input	Module present pin. Tied to GND on module side	GND	Required	8
RETMR[7:0]_PERST_N	Output	Host retimer PERST	3.3V	Required	8
FM_QSFP_OAM_MODPRS_N	Output	QSFP-DD Connector Module Present	Vref(OAM)	Option	8
CPLD_FW_TCK	Output	JTAG Test Clock of CPLD	3.3V	Required	1
CPLD_FW_TDI	Output	JTAG Test Input of CPLD	3.3V	Required	1
CPLD_FW_TDO	Input	JTAG Test Output of CPLD	3.3V	Required	1
CPLD_FW_TMS	Output	JTAG Test Mode Selec of CPLD	3.3V	Required	1
I2C_CPLD_SCL	Input	Slave I2C clock	3.3V	Required	2
I2C_CPLD_SDA	IO	Slave I2C data	3.3V	Required	2
JTAG_HOOK0	Output	Debug pin	3.3V	Required	1
PWR_BTN_N	Input	System power bottom	3.3V	Required	1
CLKS_DEV_EN	Output	CLK Buffer and CLK gen CKPWRGD	3.3V	Required	3
CLKS_OE_N	Output	CLK Buffer and CLK gen output enable	3.3V	Required	3
BOARD_ID	Input	Board ID of UBB	3.3V	Required	2
SKU_ID	Input	SKU ID of UBB	3.3V	Required	2
RSV_BMC_PRI_CPLD[15:1]	IO	RSVD	3.3V	Option	15
OAM[7:0]_THERMTRIP_N	Input	Catastrophic thermal event for module components. Active low and latched by the Module logic. Released when the UBB power cycles the module input voltages	3.3V	Required	8
OAM[7:0]_PWRBRK_N	Output	Emergency power reduction. CEM Compliant Power Brake	3.3V	Required	8
OAM_PWRBRK_N	Input	BMC to CPLD GPU Emergency power reduction	3.3V	Required	1
HOST[3:0]_WARM_RST_N	Input	BMC to CPLD Warm reset	3.3V	Required	4
HOST_PERST_N	Input	BMC to CPLD PERST	3.3V	Required	1
I2C_CPLD_AUX_ALERT_N	Input	Temperature Sensor Alert	3.3V	Required	1
FM_P12V_[7:0]_EN_R	Output	Efuse enable pin	3.3V	Required	8
OAM[7:0]_HOST_PWRGD	Output	Host power good. Active high when P48V, P12V1/P12V2, P3V3 voltages are stable and within specifications. This is considered the “Power	3.3V	Required	8

		Enable" signal for the module.			
OAM[7:0]_MODULE_PWRGD	Input	Module power good. Active high when the module has completed its own power up sequence and is ready for PERST# de-assertion	3.3V	Required	8
PWRGD_P12V_[7:0]_PG	Input	Efuse PWRGOOD pin	3.3V	Required	8
PWRGD_PHY_RETIMER_[3:0]	Input	VR IC PWRGOOD pin	3.3V	Required	4
PWRGD_HOST_RETIMER_[3:0]	Input	VR IC PWRGOOD pin	3.3V	Required	4
PWRGD_P3V3_OAM	Input	VR IC PWRGOOD pin	3.3V	Required	1
PWRGD_P3V3_QSFPDD	Input	VR IC PWRGOOD pin	3.3V	Required	1
VR_PHY_RETIMER_EN	Output	VR IC enable pin	3.3V	Required	1
VR_HOST_RETIMER_EN	Output	VR IC enable pin	3.3V	Required	1
FM_VR_P3V3_OAM_EN	Output	VR IC enable pin	3.3V	Required	1
FM_VR_P3V3_QSFPDD_EN	Output	VR IC enable pin	3.3V	Required	1
OAM[7:0]_WARMRST_N	Output	Warm Reset	Vref(OAM)	Option	8
OAM[7:0]_PERST_N	Output	CEM Compliant PCIe Reset	3.3V	Required	8
OAM_PCA9548_RESET_N	Output	I2C Switch Reset	3.3V	Required	1
VR_PCA9548_RESET_N	Output	I2C Switch Reset	3.3V	Required	1
SW[0:3]_PE_RESET_N	Input	RSVD from SW to UBB CPLD sideband signal for PERESET_N	3.3V	Option	4
OAM[0:7]_FW_RECOVERY_N	Input	On board manageability boot recovery mode 1: Normal operation 0: Firmware Recovery boot mode	3.3V	Required	8
CLK_50M_CPLD1	Input	Clock input pin	3.3V	Option	1
PRI_CPLD_DONE	Input	Programming pin (Reserved.)	3.3V	Option	1
PRI_CPLD_INITN	Input	Programming pin (Reserved.)	3.3V	Option	1
PRI_CPLD_JTAGEN	Input	Programming pin (Reserved.)	3.3V	Option	1
PRI_CPLD_PROGRAM	Input	Programming pin (Reserved.)	3.3V	Option	1

PRI_CPLD_SN	Input	Programming pin , Usage instead of the HWRST.	3.3V	Required	1
PHY[0:3]_RSTB_N	Output	PHY retimer reset	Vref (PHY)	Required	4
SGPIO	IO	SGPIO interface between BMC & UBB CPLD	3.3V	Option	4

Table 42 Primary CPLD pin list

Secondary CPLD pin list

Signal	UBB Direction POV	Description	Voltage	Required or Optional	Total Single Pins
JTAG_OAM_HV_TCK[7:0]	Output	High Voltage JTAG Test Clock	3.3V	Required	8
JTAG_OAM_HV_TDI[7:0]	Output	High Voltage JTAG Test Input	3.3V	Required	8
JTAG_OAM_HV_TDO[7:0]	Input	High Voltage JTAG Test Output	3.3V	Required	8
JTAG_OAM_HV_TMS[7:0]	Output	High Voltage JTAG Test Mode Selec	3.3V	Required	8
JTAG_OAM_HV_TRST[7:0]	Output	High Voltage JTAG Test Reset	3.3V	Required	8
JTAG_OAM_LV_TCK [7:0]	Output	Low Voltage JTAG Test Clock	Vref(OAM)	Required	8
JTAG_OAM_LV_TDI[7:0]	Output	Low Voltage JTAG Test Input	Vref(OAM)	Required	8
JTAG_OAM_LV_TDO[7:0]	Input	Low Voltage JTAG Test Output	Vref(OAM)	Required	8
JTAG_OAM_LV_TMS[7:0]	Output	Low Voltage JTAG Test Mode Selec	Vref(OAM)	Required	8
JTAG_OAM_LV_TRST [7:0]	Output	Low Voltage JTAG Test Reset	Vref(OAM)	Required	8
OAM_DEBUG_PORT_PRSNT_N[7:0]	Output	Presence signal for debug port in motherboard. Notifies logic in the module the debug access is being used by the motherboard debug connector. Debug port on baseboard present when logic low	GND	Required	8
VCC_3V3_SEC	Power input	Vcc core power of secondary CPLD	3.3V	Required	8
VCCIO1_SEC	Power input	Vccio power of secondary CPLD	3.3V	Required	5
VCCIO2_SEC	Power input	Vccio power of secondary CPLD	1.2~3.3 V*	Required	12
CPLD_FW_TCK	Output	JTAG Test Clock of CPLD	3.3V	Required	1

CPLD_FW_TDI	Output	JTAG Test Input of CPLD	3.3V	Required	1
CPLD_FW_TDO	Input	JTAG Test Output of CPLD	3.3V	Required	1
CPLD_FW_TMS	Output	JTAG Test Mode Selec of CPLD	3.3V	Required	1
JTAG_TCK	Output	JTAG Test Clock of CPLD	Vref(OAM)	Required	1
JTAG_TDI	Output	JTAG Test Input of CPLD	Vref(OAM)	Required	1
JTAG_TDO	Input	JTAG Test Output of CPLD	Vref(OAM)	Required	1
JTAG_TMS	Output	JTAG Test Mode Selec of CPLD	Vref(OAM)	Required	1
JTAG_TRST	Output	JTAG Test Reset of CPLD	Vref(OAM)	Required	1
JTAG_BMC_OAM_TDO	Output	OAM Debug from BMC	3.3V	Required	1
JTAG_BMC_OAM_TDI	Input	OAM Debug from BMC	3.3V	Required	1
JTAG_BMC_OAM_TMS	Output	OAM Debug from BMC	3.3V	Required	1
JTAG_BMC_OAM_TRST	Output	OAM Debug from BMC	3.3V	Required	1
JTAG_BMC_OAM_TCK	Output	OAM Debug from BMC	3.3V	Required	1
OAM0_TEST[14:0]	IO	OAM0 test pin	Vref(OAM)	Option	15
OAM1_TEST[14:0]	IO	OAM1 test pin	Vref(OAM)	Option	15
OAM2_TEST[14:0]	IO	OAM2 test pin	Vref(OAM)	Option	15
OAM3_TEST[14:0]	IO	OAM3 test pin	Vref(OAM)	Option	15
OAM4_TEST[14:0]	IO	OAM4 test pin	Vref(OAM)	Option	15
OAM5_TEST[14:0]	IO	OAM5 test pin	Vref(OAM)	Option	15
OAM6_TEST[14:0]	IO	OAM6 test pin	Vref(OAM)	Option	15
OAM7_TEST[14:0]	IO	OAM7 test pin	Vref(OAM)	Option	15
DEBUG_OAM_TEST_[14:0]	IO	OAM for JTAG test pin	Vref(OAM)	Option	15
RSV_BMC_SEC_CPLD[3:0]	IO	RSVD	3.3V	Option	4
DEBUG_PRESENT_N	Input	Debug port PRSNT pin	3.3V	Required	1
I2C_CPLD_TEMP_AUX_SCL	Input	Slave I2C clock	3.3V	Required	1
I2C_CPLD_TEMP_AUX_SDA	IO	Slave I2C data	3.3V	Required	1

BMC_JTAG_SELECT_[0:3]	Input	BMC JTAG Select pin	3.3V	Option	4
JTAG_HOOK6	Input	Debug pin	Vref(OAM)	Required	1
JTAG_HOOK7	Output	Debug pin	Vref(OAM)	Required	1
SEC_CPLD_PROGRAM	Input	Programming pin (Reserved.)	3.3V	Option	1
SEC_CPLD_SN	Input	Programming pin (Reserved.)	3.3V	Option	1

Table 43 Secondary CPLD pin list

Note: *UBB designer should check OAM SPEC for Vref power rail (OAI UBB reference design selected 1.5V as VCCIO power to support 1.2V~3.3V OAM Vref).

OAM Vref output is 1.2V~3.3V, all the CPLD VCCIO2_PRI(SEC) IO pins output to OAM must be open drain.

6.5.6. OAM Vref based IO Pin

Table below shows OAM Vref based miscellaneous signal list. The level shift devises and open drain output are for reference only.

All miscellaneous signal power source have to connect to its OAM Vref output per the block diagram illustrated. For open drain I/O connects to OAM Vref signal, the pull-up resistors power are connected from its OAM Vref. For level shift device with two power sources, the high voltage power source comes from UBB power and the low voltage power souce comes from its OAM Vref power. The level shift component (ex: NXP NTS0104) is required to act as a power isolation device between OAM Vref and CPLD, High Density connector, QSFP-DD connector.

OAM Miscellaneous Vref signals				
Signal	Direction	I/O Type	UBB Connection Device	Connector
VREF	Power Output	Power	OAM Output (1.2V ~ 3.3V)	Conn0
WARMRST#	Input		PRI_CPLD GPIO.OD w/ PU	Conn0
MODULE_ID	Input	Internal 47K PU	0: 100ohm 1: Floating	Conn0
LINK_CONFIG[4:0]	Input	Internal 47K PU	0: 100ohm 1: Floating	Conn1
PE_BIF[1:0]	Output	0: 1K ohm PD 1: 10K ohm PU	100K ohm PU	Conn1
PLINK_CAP	Output	0: 1K ohm PD 1: 10K ohm PU	100K ohm PU	Conn1
I2C_D	I/O	I/OD	PCA9617A w/PU	Conn0
I2C_CLK	Output	OD	PCA9617A w/PU	Conn0
JTAG0_TRST	Input		SEC_CPLD GPIO.OD w/PU	Conn0
JTAG0_TMS	Input		SEC_CPLD GPIO.OD w/PU	Conn0

JTAG0_TCK	Input		SEC_CPLD GPIO.OD w/PU	Conn0
JTAG0_TDO	Output	Push-Pull	SEC_CPLD GPIO Input	Conn0
JTAG0_TDI	Input		SEC_CPLD GPIO.OD w/PU	Conn0
CONN1_INITMODE	Output	Push-Pull	QSFP via level shift device	Conn1
CONN1_INT#	Input		QSFP via level shift device	Conn1
CONN1_MODPRS#	Input		QSFP via level shift device	Conn1
CONN1_MODSEL#	Output	Push-Pull	QSFP via level shift device	Conn1
CONN1_RESET#	Output	Push-Pull	QSFP via level shift device	Conn1
CONN1_GREEN_LED	Output	Push-Pull	LED via FET	Conn1
CONN1_YELLOW_LED	Output	Push-Pull	LED via FET	Conn1
CONN2_INITMODE	Output	Push-Pull	QSFP via level shift device	Conn1
CONN2_INT#	Input		QSFP via level shift device	Conn1
CONN2_MODPRS#	Input		QSFP via level shift device	Conn1
CONN2_MODSEL#	Output	Push-Pull	QSFP via level shift device	Conn1
CONN2_RESET#	Output	Push-Pull	QSFP via level shift device	Conn1
CONN2_GREEN_LED	Output	Push-Pull	LED via FET.G	Conn1
CONN2_YELLOW_LED	Output	Push-Pull	LED via FET.G	Conn1
DEBUG_PORT_PRSNT#	Input		SEC_CPLD GPIO.OD	Conn1
TEST[0:4]	Input		SEC_CPLD GPIO.OD	Conn0
TEST[5:9]	I/O	Push-Pull (I/O)	SEC_CPLD GPIO.OD w/PU or level shift device	Conn0
TEST[10:14]	I/O	Push-Pull (I/O)	SEC_CPLD GPIO.OD w/PU or level shift device	Conn1
TEST_MODE#	Input		DIP_SW w/PU	Conn0

Table 44 OAM Vref Signal usage

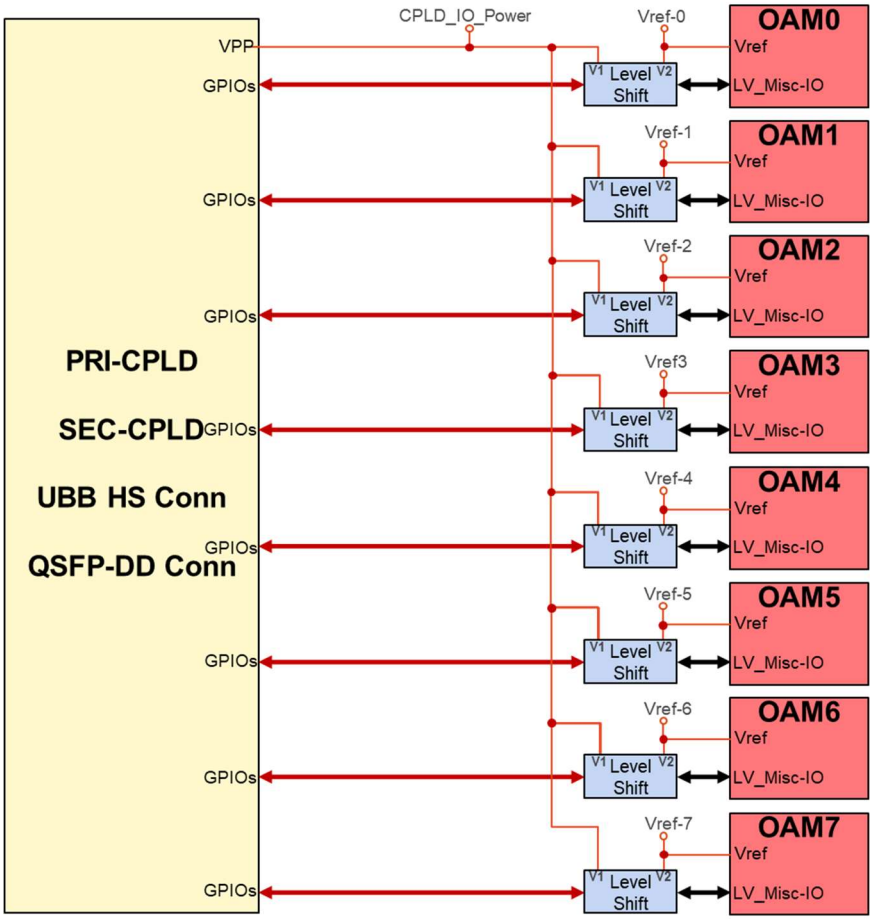


Figure 28 Vref Signal Block Diagram

Table below shows CPLD Vccio power source and input/output pin power level from Lattice MachXO2 for reference. The Vccio power source has to be connected from UBB VR power output, not from OAM Vref output. The CPLD Vccio 1.5V supports OAM input I/O voltage wider rang (1.2V ~ 3.3V), the output I/O should be set to open-drain fro wider rang Vref.

	Inputs					Outputs				
V_{CCIO}	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V
1.2 V	YES	YES[6]				YES				
1.5 V	YES[1]	YES	YES[6]	YES[6]	YES[6]		YES			
1.8 V	YES[1]	YES[5]	YES	YES[6]	YES[6]			YES		
2.5 V	YES[1]	YES[2, 5, 7]	YES[3, 5, 7]	YES	YES[6]				YES	
3.3 V	YES[1]	YES[2, 5, 7]	YES[3, 5, 7]	YES[4, 5, 7]	YES					YES

Table 45 Mixed Voltage Support for LVCMOS and LVTTL I/O Types (copied from Lattice MachXO2 datasheet)

6.6. Host retimer

System design decides whether host retimers are needed for their UBB design. OAI reference UBBs implemented eight of the 16x lane retimer device (ex: PCIe G4, 16GT/s) to near ExaMAX connector. Each 16x lane retimer supports common clock between HIB and retimer as well as retimer to OAM (refer to 6.1.1). The upstream of retimer lane is HIB lane root port. The retimer topology is illustrated in the figure below.

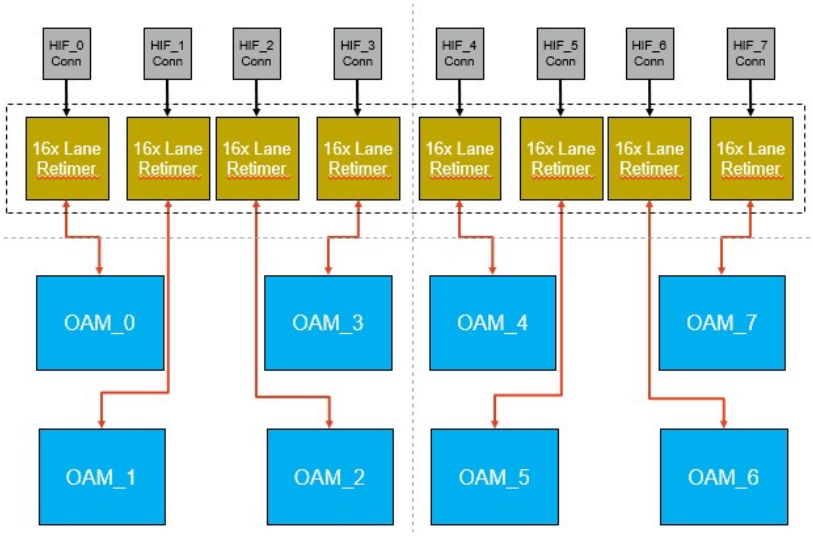


Figure 29 HIB Lane Retimer Topology

6.7. SERDES PHY Retimer

System design decides whether phy retimers are needed for their UBB design. In UBB reference boards, the PHY retimers are placed near QSFP-DD connectors which supports max passive QSFP-DD cable length up to 2 meters for UBB expansion/ scal-out. The PHY retimer connection is illustrated in figure below.

There is also MDC/MDIO interface designed from HIF_0 connector to each Serdes PHY for configuration.

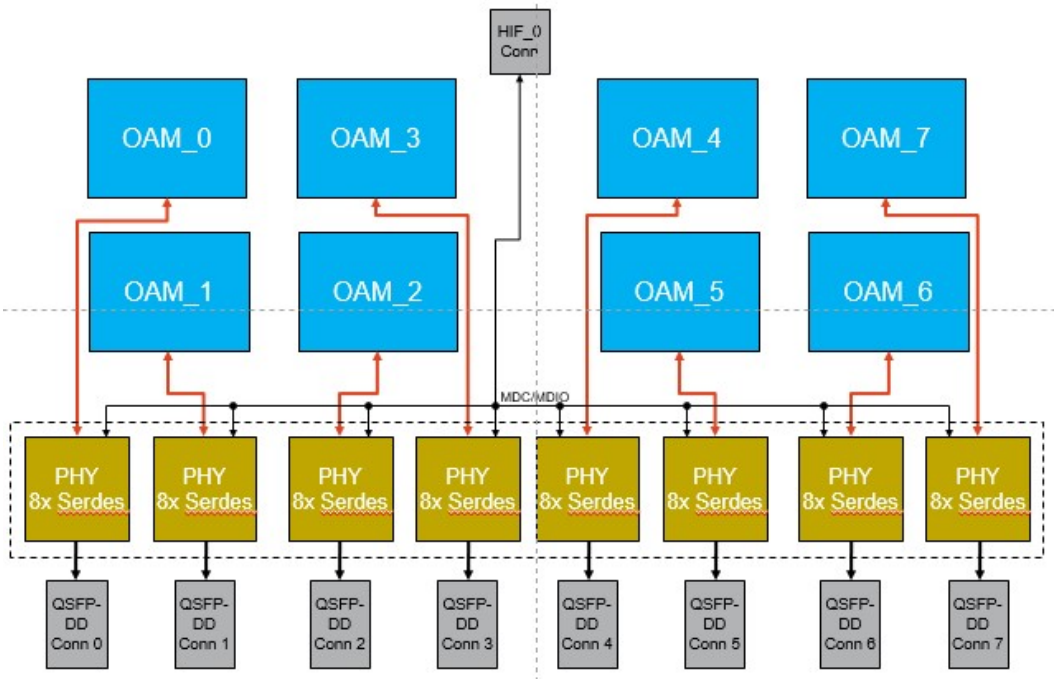


Figure 30 UBB Scale Out Serdes PHY Topology (Example)

OAI system designers have to to check serdes PHY supplier for FW support to enable specific link speed with OAMs. Further contact Hyve/ Inspur/ ZT/ Inventec for SERDES PHY application in OAI reference systems if needed.

6.8. High Speed SI guidance

This guidance is to recommend routing rule & fan-out pattern design of mirror mezzanine connector to have high speed SI performance. It also shows measurement data including test procedure & environment settings with test fixture for reference. Please refer to UBB SI guidance in Wiki for detail:

https://www.opencompute.org/wiki/Server/OAI

7. Interconnect Topology

Uniersal baseboard supports 8 OAMs and can support different topologies described in OCP Acclerators Design specification v1.0* session 9. In this session we will describe two reference interconnect topologies that used in our UBB reference boards.
(http://files.opencompute.org/oc/public.php?service=files&t=938c61e5b1d3c5c2b5c33f95525b1412&download&path=//OCP%20Accelerator%20Module%20Design%20Specification_v1p0.pdf)

7.1. Module ID

There are 5 module ID pins defined in OAM specification. UBB sets these pins based on below figure: reference to Section6 for details.

OAM	Module ID
OAM0	00000
OAM1	00001
OAM2	00010
OAM3	00011
OAM4	00100
OAM5	00101
OAM6	00110
OAM7	00111

Table 46 UBB OAM module IDs

7.2. LINK_CONFIG ID

Link_config ID pins are defined in OCP Accelerator Module Design Specification section 9.3. The 5 link configuration strapping bits are pulled up on modules that use them. These bits are strapped to ground on the UBB baseboard to select logic 0, or left floating on the baseboard to select logic 1. Some accelerators use these LINK_CONFIG[4:0] strapping bits to determine the interconnect topology for the links between modules and to determine the protocol of the “P” Link. UBB should set the Link_Config ID based on the table defined in OAM spec.

LINK_CONFIG[4:0]	Definition
00000	Reserved for OAM. Test use by OAM Vendor.
xxxx0 (except for 00000)	Indicates the “P” link is PCIe
01000	6 link HCM, 4 link HCM, and two 3 link fully connected quads as connected
00110	7 x16 fully connected
01010	6 x 16 link Chordal Ring (Almost Fully Connected) as connected
01011	6 x 16 link Chordal Ring (Almost Fully Connected) using alternate host interface protocol as connected
01100	8 link HCM
xxxx1 (except for 11111)	Indicates the “P” link is an alternate protocol other than PCIe
10000	Combined FC/6-Port HCM
11111	Indicates an alternate means for identifying the link interconnect topology and configuration is used

Table 47 LINK_CONFIG[4:0] Encoding Definitions

*This table is copied from OAM spec v1.1. Encodings not listed in the table below are currently un-defined in OAM spec v1.1. Please refer to latest OAM spec (https://www.opencompute.org/wiki/Server/OAI) to get the latest Link_config definitions.

The following figure shows the OAM ID and Configure ID connection. OAM ID has its individual MODULE_ID[4:0] connection to identify its module ID number. The configure ID has to connect to all OAM LINK_CONFIG[4:0] and BMC.

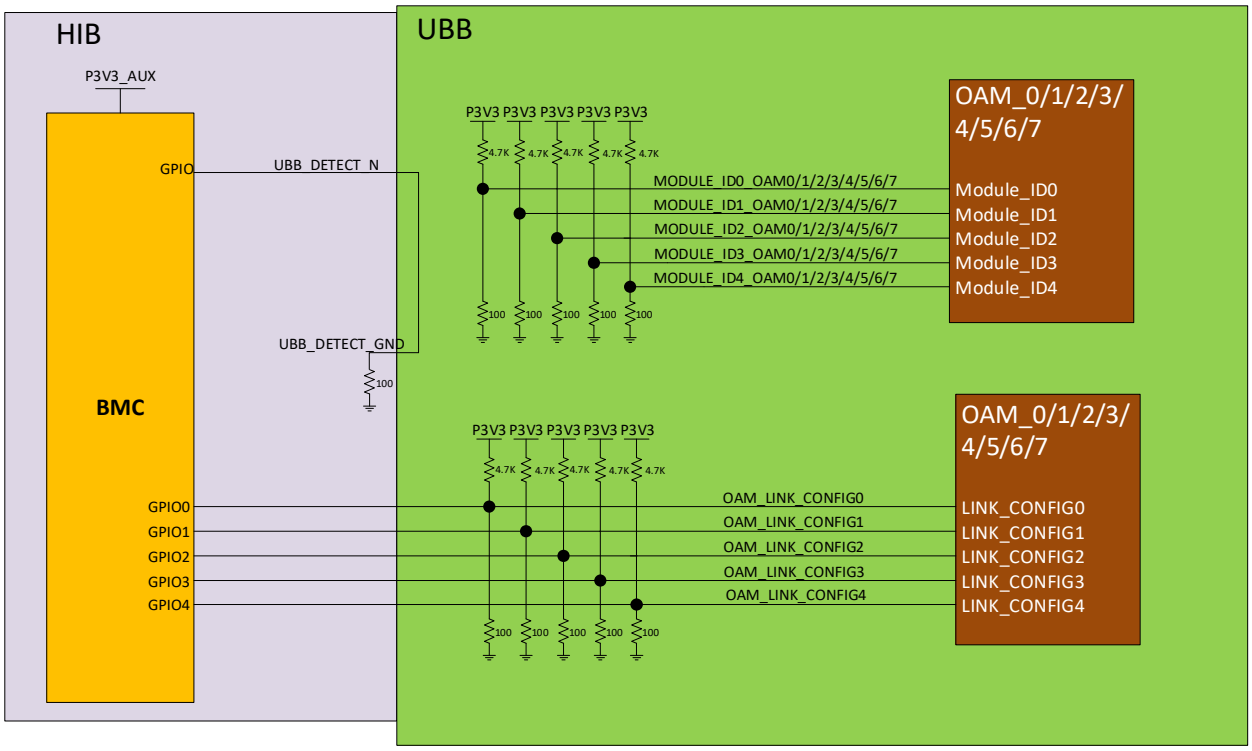


Figure 31 LINK_CONFIG ID

7.3. Combined Fully Connected and 6-port Hybrid Cube Mesh Topology

For fully connect with expansion consideration, the UBB link is routed as X8(1st X8 of each port, 1L-7L), leaving 2nd X8 of each SerDes port for expansion or embedding other topology. Here is 8 port HCM UBB reference board 7X8 fully connected topology combined with 6X8 hybrid cube mesh topology (X8 FC + X8 6 port HCM):

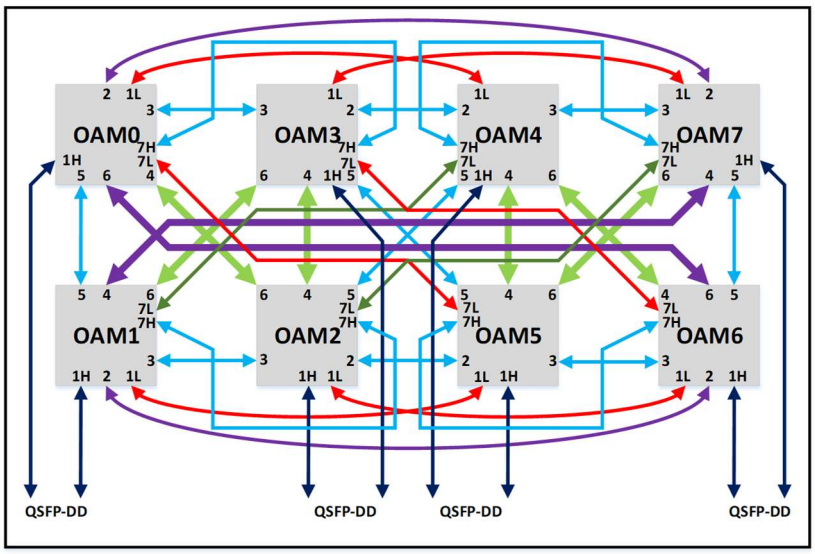


Figure 32 Combined FC/6-Port HCM Topology

Port 1,4,6,7 has total 16 lanes and Port 2,3,5 has total 8 lanes in Figure 32:

- Fully connected: 7 x8 links using port 1-7 first X8(1L-7L);
- 2nd half of port 1s(1H) are connected to QSFP-DD for expansion (scale out);
- 6 port HCM: all 6 ports are in connector 1 only. X16 link for port 4/6, X8 link(5L) for port 5 and 2nd half of port 7(7H)

Below figure shows the detail port mapping and routing guide:

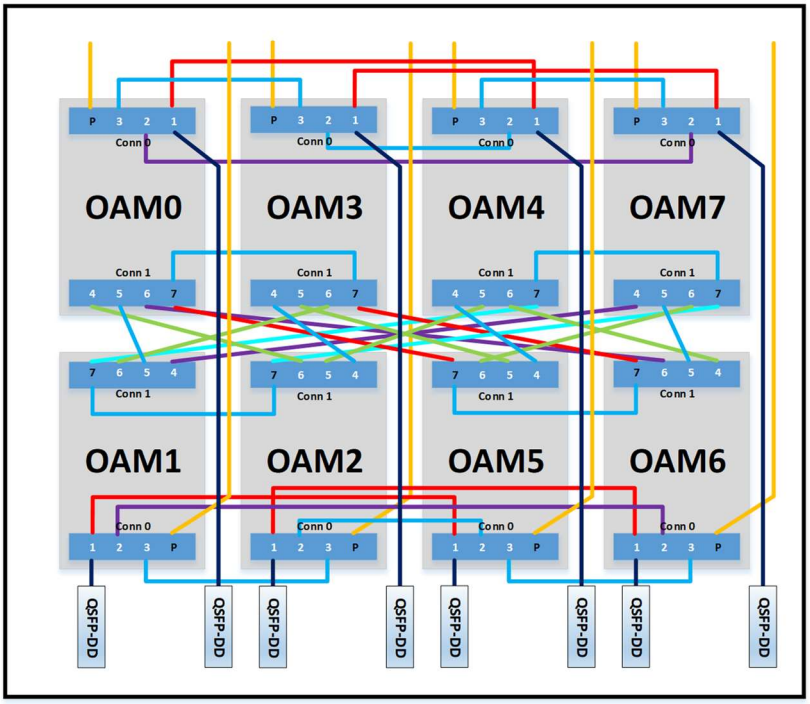


Figure 33 Detail port mapping and routing guidance

Port 4/6(both 4L/6L and 4H/6H), port 5L, 7H are used for 6X8 HCM. This is how it's embedded to this combined topology:

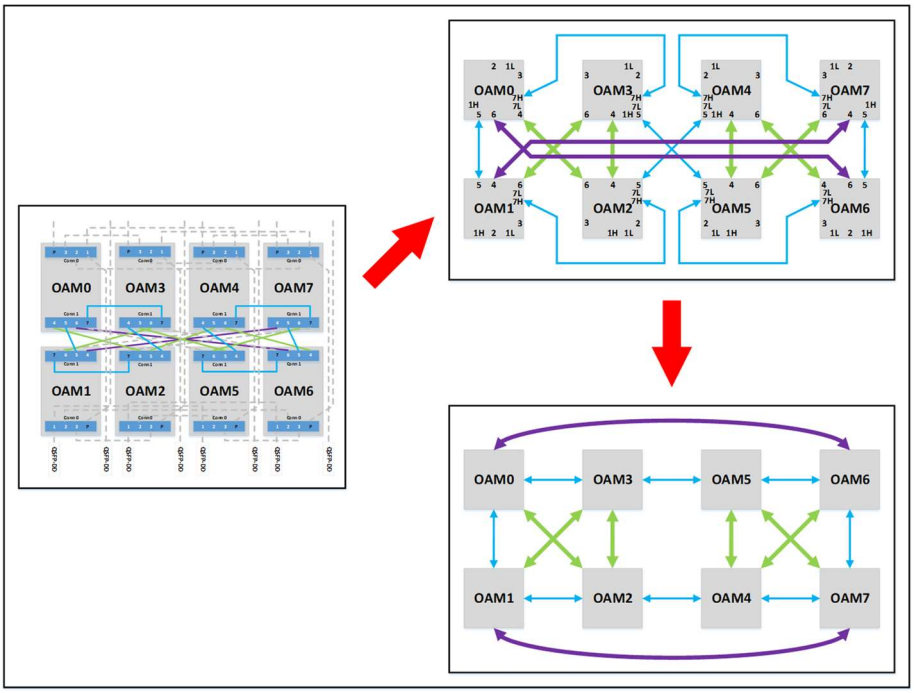


Figure 34 Embedded HCM Topology

7.4. 8-port Hybrid Cube Mesh Topology

The Figure below shows 8 port HCM(Hybrid Cube Mesh) topology of 8 modules in a UBB. Please follow port mapping to design OAM in order to be able to fit in the universal OAM baseboard. Port 4/6 are connected through QSFP-DD cables for single 8 module system. These QSFP-DD cables can also be used for expansion (scale out).

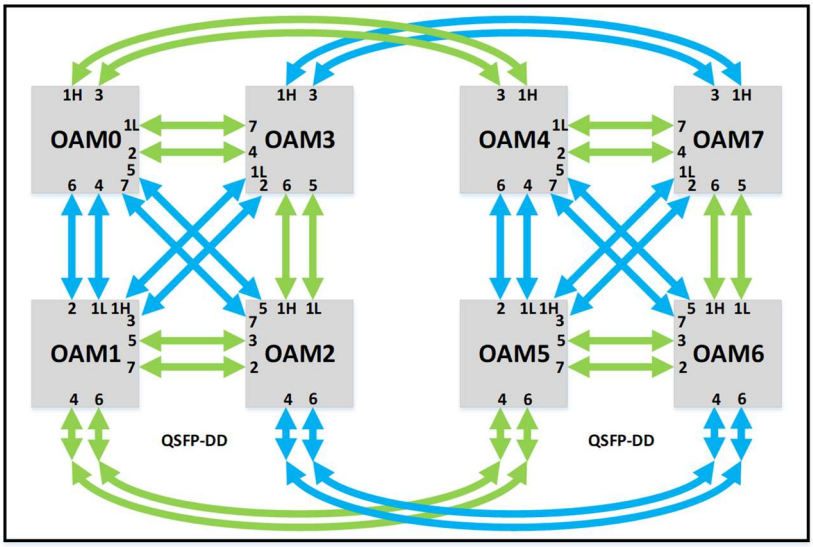


Figure 35 8-port Hybrid Cube Mesh Topology

- links HCM using links: 1, 2, 3, 4, 5, 6, 7
- SerDes Port 2, 3, 4, 5, 6, 7 are x8 lanes

- SerDes Port 1 is 2 x8 lanes
- 1L –Lower 8-bit, 1H –Upper 8-bit
- Links: 4, 6 (OAM #1, #2, #5 and #6) are used for scale out, can be connected through QSFP-DD cables.

And here is routing suggestion: total 4 layer, two layers for TX, two layers for RX. Port 4/6 are connected through cables.

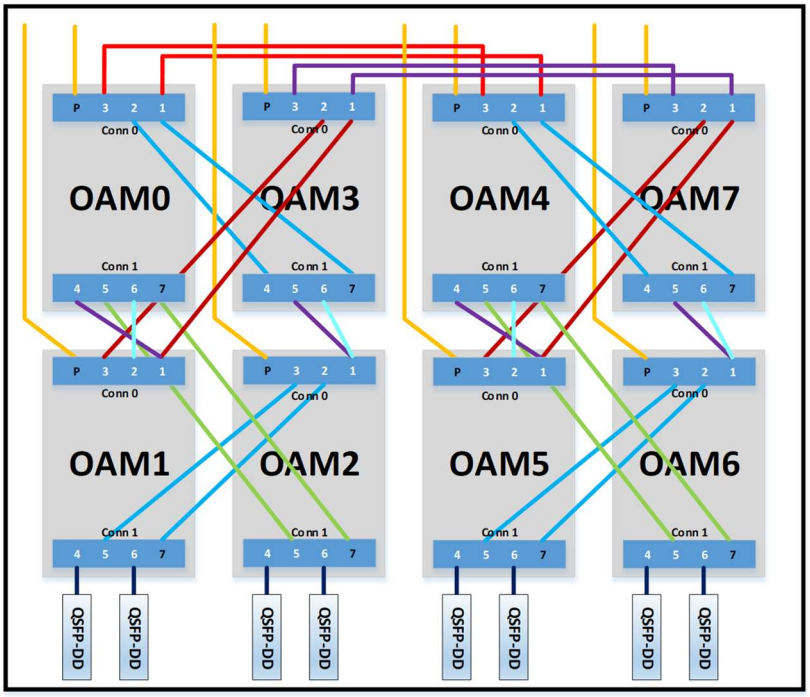


Figure 36 8-port HCM topology routing guide

7.5. UBB Reference boards

System providers Inspur, HyveDesignSolutions, ZT systems/Inventec designed the first two UBB reference boards: combined FC(Full connected) + 6 link HCM and 8 link HCM (Hybric Cube Mesh). Refer to Mechanical portion in chapter8 for detail Mezz orientation definition.

7.6. UBB silkscreen

OAM silkscreen shall follow module ID naming as OAM0, OAM1, OAM2 etc. Scale out QSFP-DD connector silkscreen shall follow Qdd_0, Qdd_1, Qdd_2 etc.

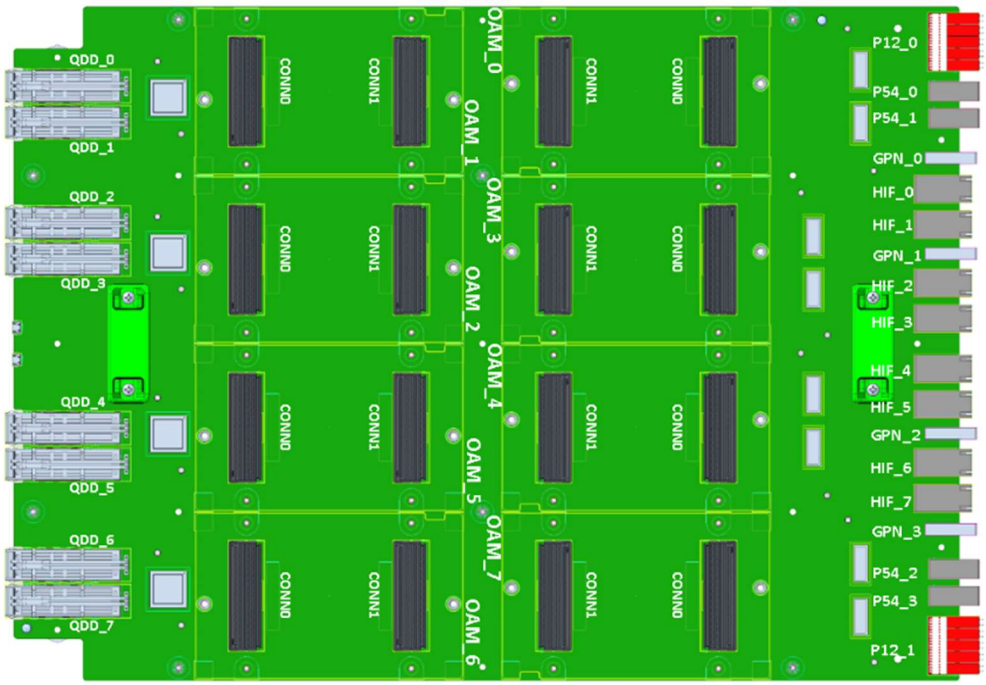


Figure 37 UBB silkscreen example

8. Mechanical Specification

8.1. Board dimension

Board dimension is limited to 585mm x 417mm x 3.2mm (L x W x T). The handle design and interface for the UBB assembly is not defined in this specification, and may be customized as needed. The outline of the board is fixed as shown in the drawings, and may not be altered or customized.

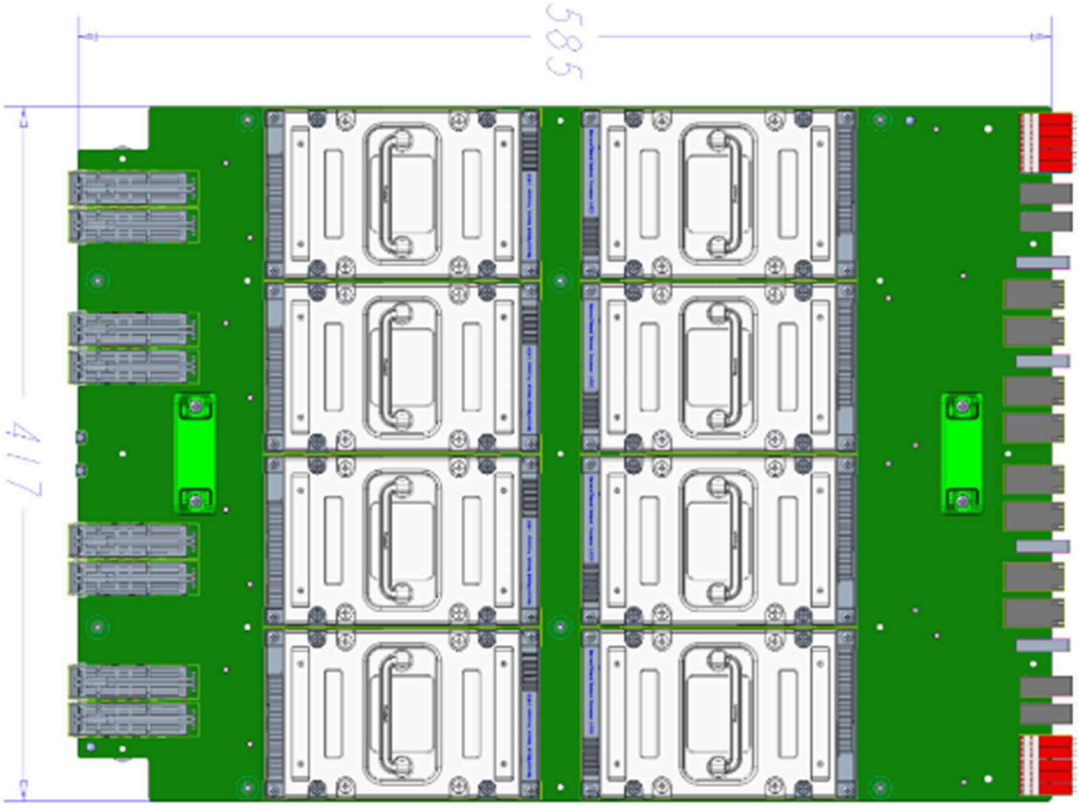


Figure 38 UBB board dimension

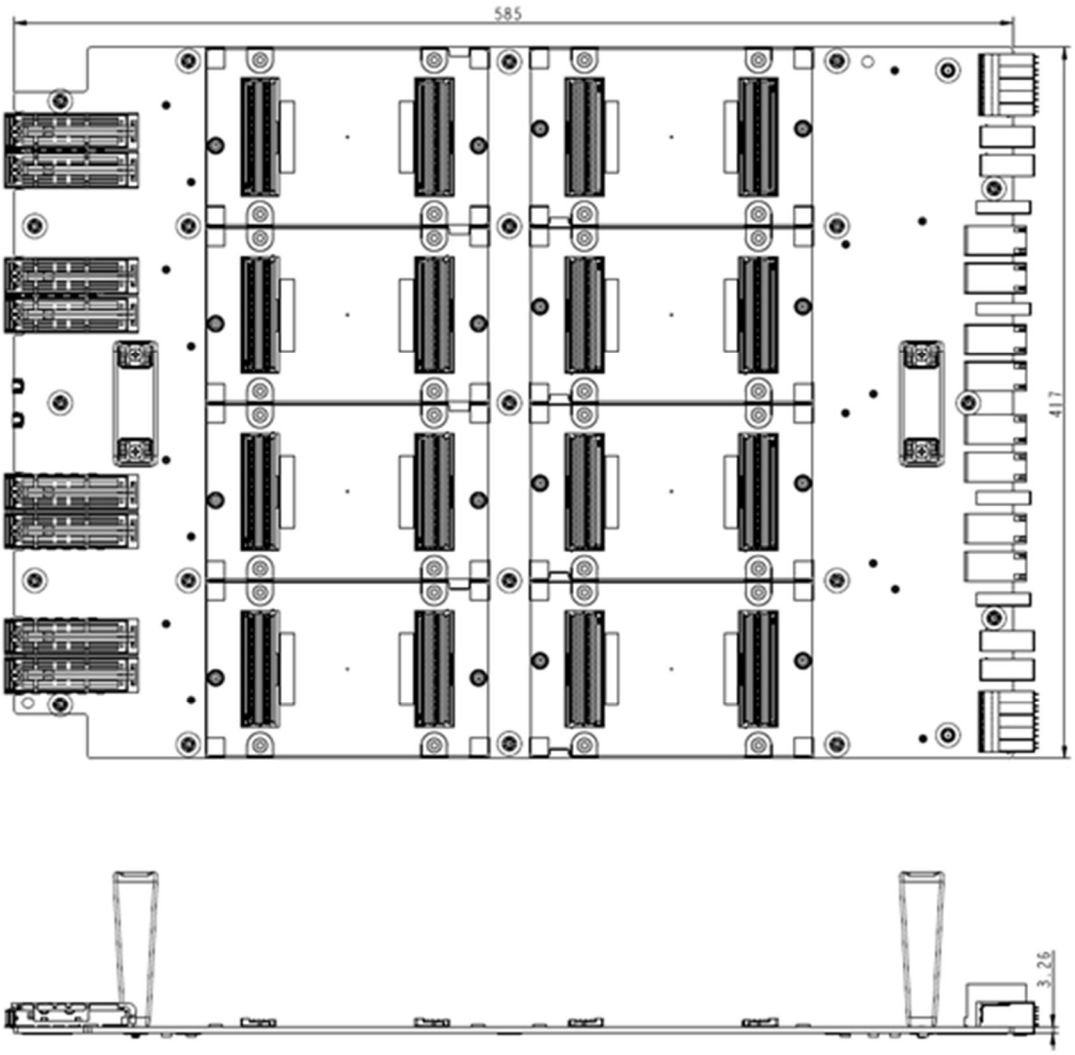


Figure 39 UBB board Top and side views

8.2. Required Components

8.2.1. OAM Placement / Molex Connectors

There are two different topologies with different connector orientations. The figures below highlight connector numbers and pin 1 locations to distinguish the two architectures.

FC (Fully connected)

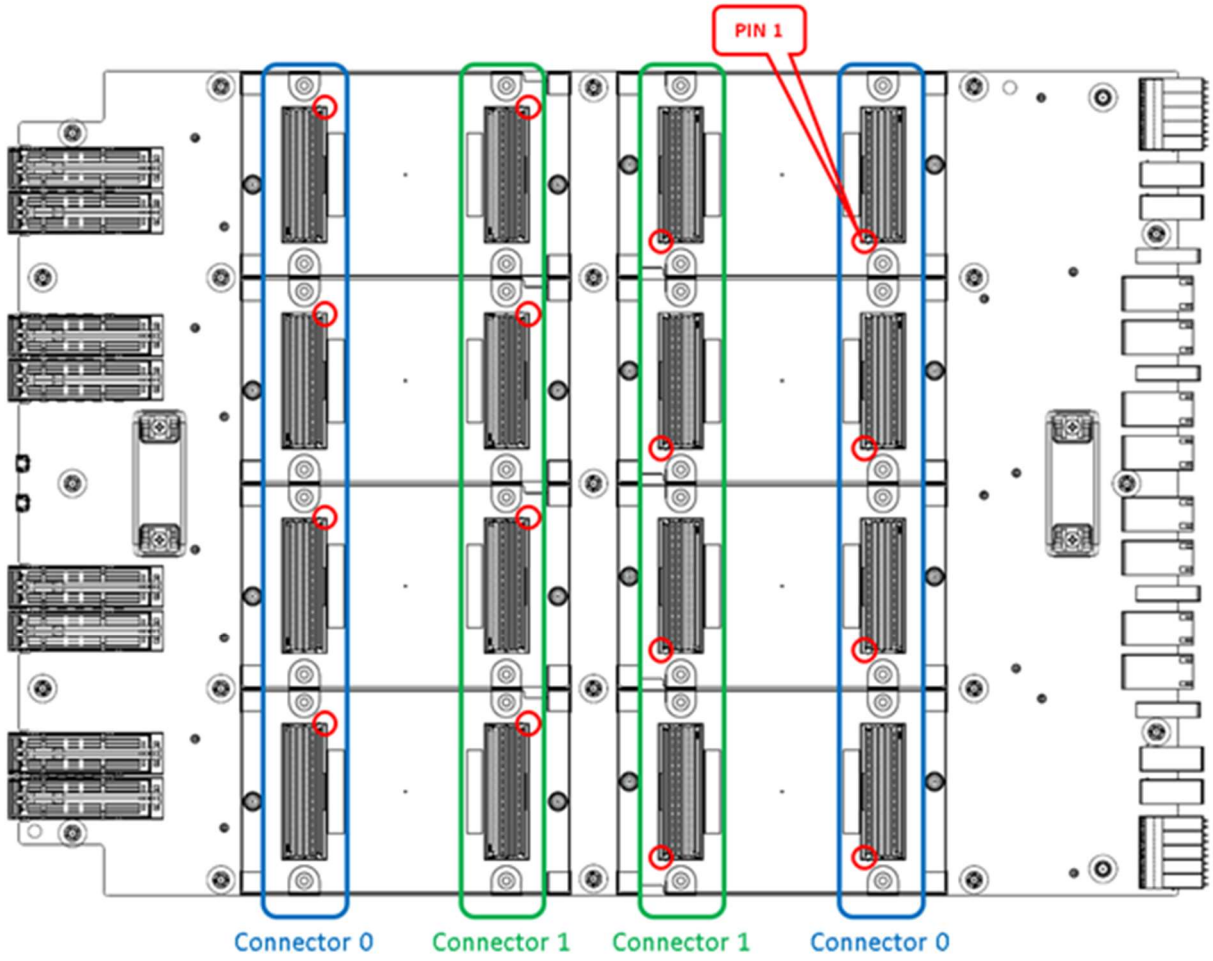


Figure 40 OAM Molex Mezz connector pin1 orientation_FC

.

HCM (Hybrid Cube Mesh) connection

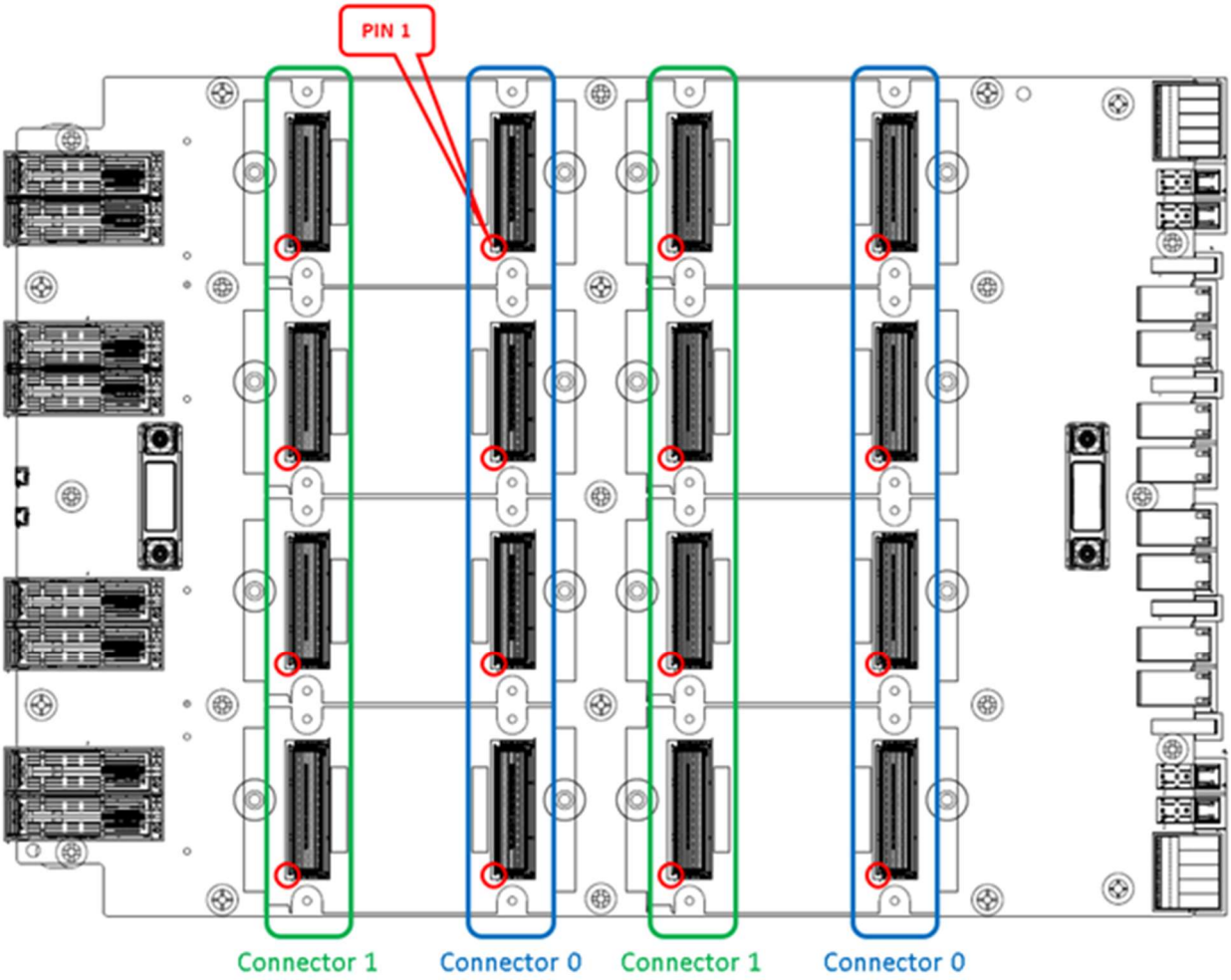


Figure 41 OAM Molex Mezz connector pin1 orientation_HCM

8.2.2. I/O Connectors

QSFP-DD connectors are used for multi system scale out. Two Micro USB connectors are also exposed from the UBB to the exterior of the chassis for debug

Item	Vendors	Model number	Descriptions
1	Amphenol	UE36-A1070-3000T	QSFP-DD Connector
2	Amphenol	UE36-B16221-06A5A	QSFP-DD Cage
3	Molex	105017-0001	Micro USB Connector

Table 48 UBB IO connectors

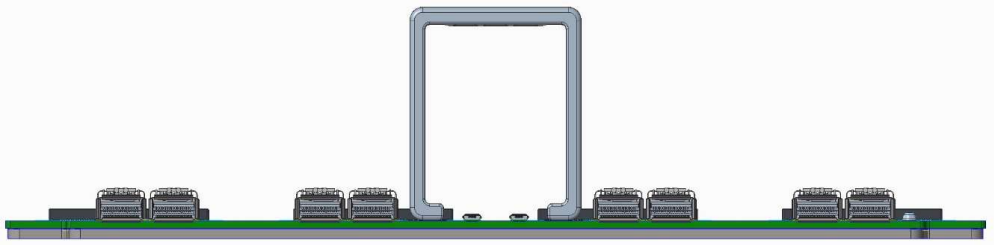


Figure 42 UBB Front IOs

High speed and Power Conenctor

Item	Vendors	Model number	Descriptions	Qty
1	Amphenol	10131762-101LF	High Density Connector	8
2	Amphenol	10037909-101LF	Guide Pin	4
3	Amphenol	10028917-001LF	54V Connector	4
4	Amphenol	JX410-513xx	12V Connector	2

Table 49 High speed and Power Conenctor

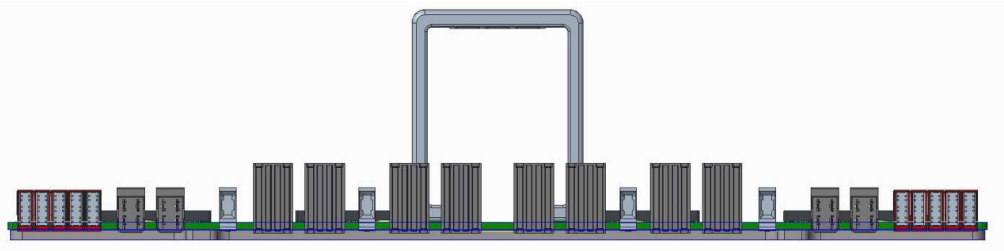


Figure 43 UBB high speed and power connectors to HIB

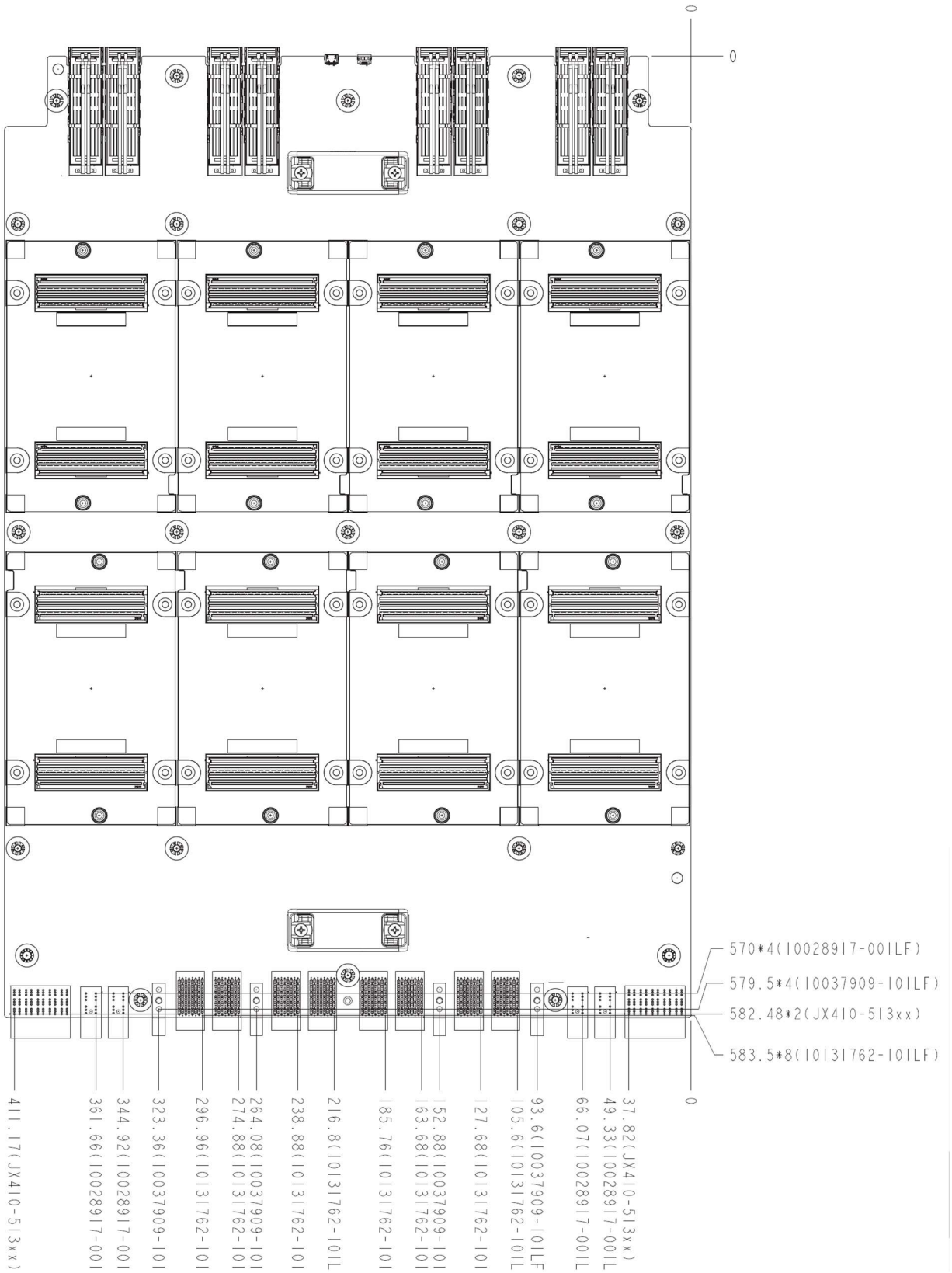


Figure 44 UBB high speed and power connectors coordinate

8.2.3. Screw Mounting Holes

Screw hole sizes and locations are defined in this chapter. 3D files can be found on the OCP-OAI wiki.

Mounting holes to UBB tray :

There are 15 screw mounting holes to fix UBB to UBB tray.

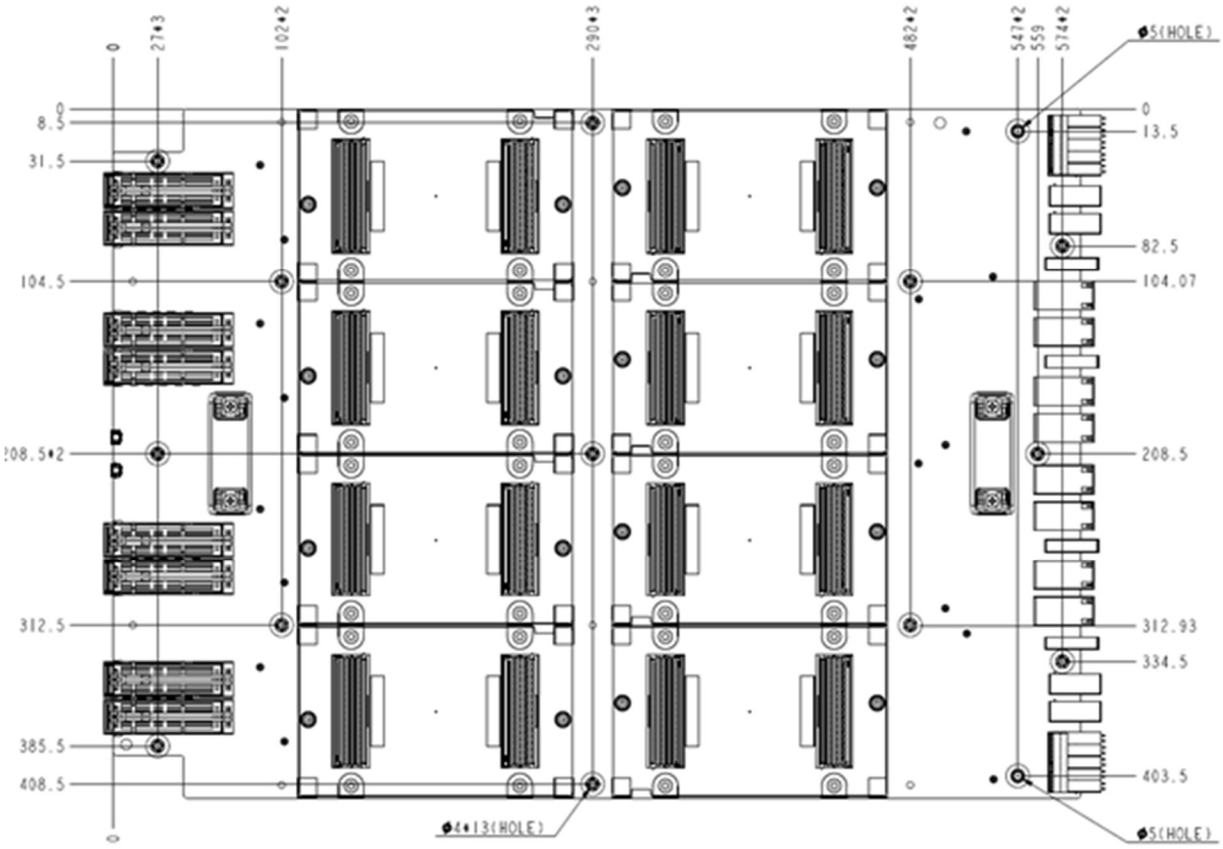


Figure 45 mounting holes

Through holes for OAMs:

There are 32 through holes for OAMs screwing down to bolster.

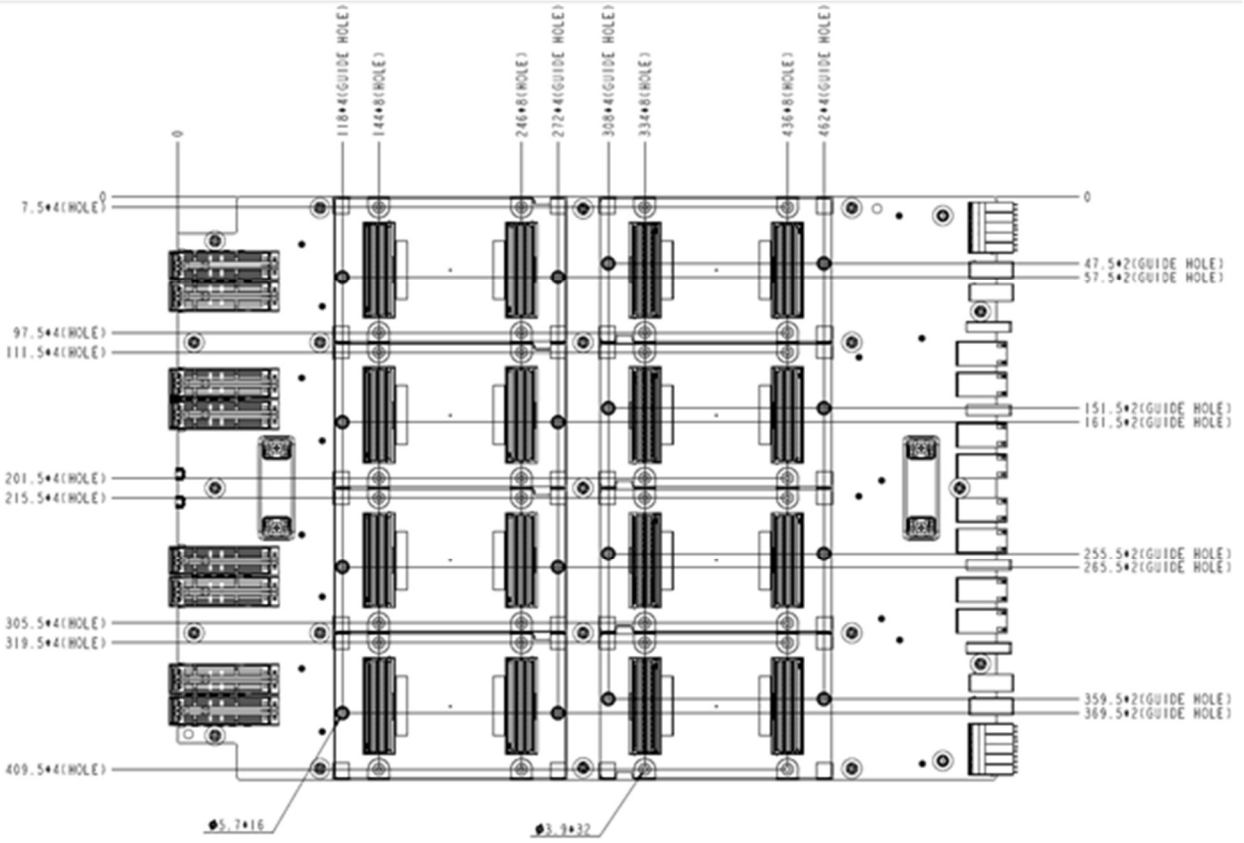


Figure 46 OAM through holes

OAM guide hole (SMT Nut):

SMT nut illustrated below is soldered to UBB at the loations of 5.7mm diameter holes specified in Figure 38 above.

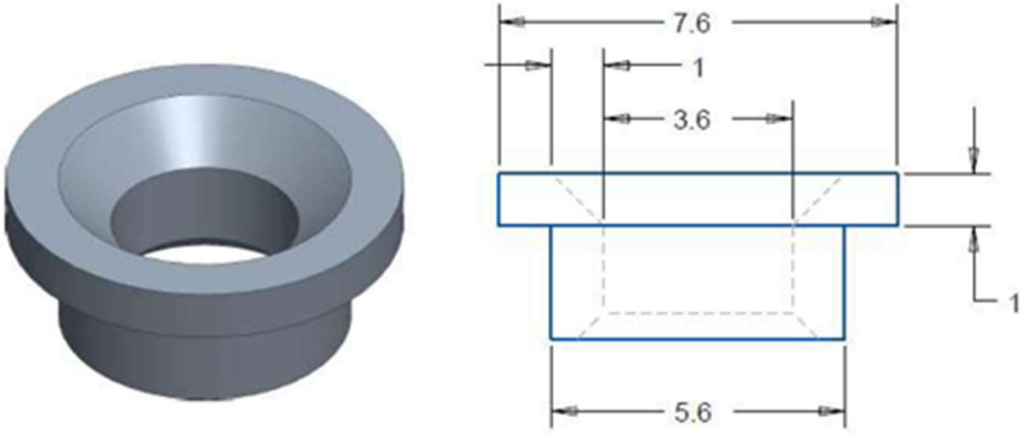


Figure 47 OAM guide hole

Mounting holes for bolster:

There are 2 guide holes to align UBB and bolster first, then 8 mounting holes used for fastening UBB with bolster.

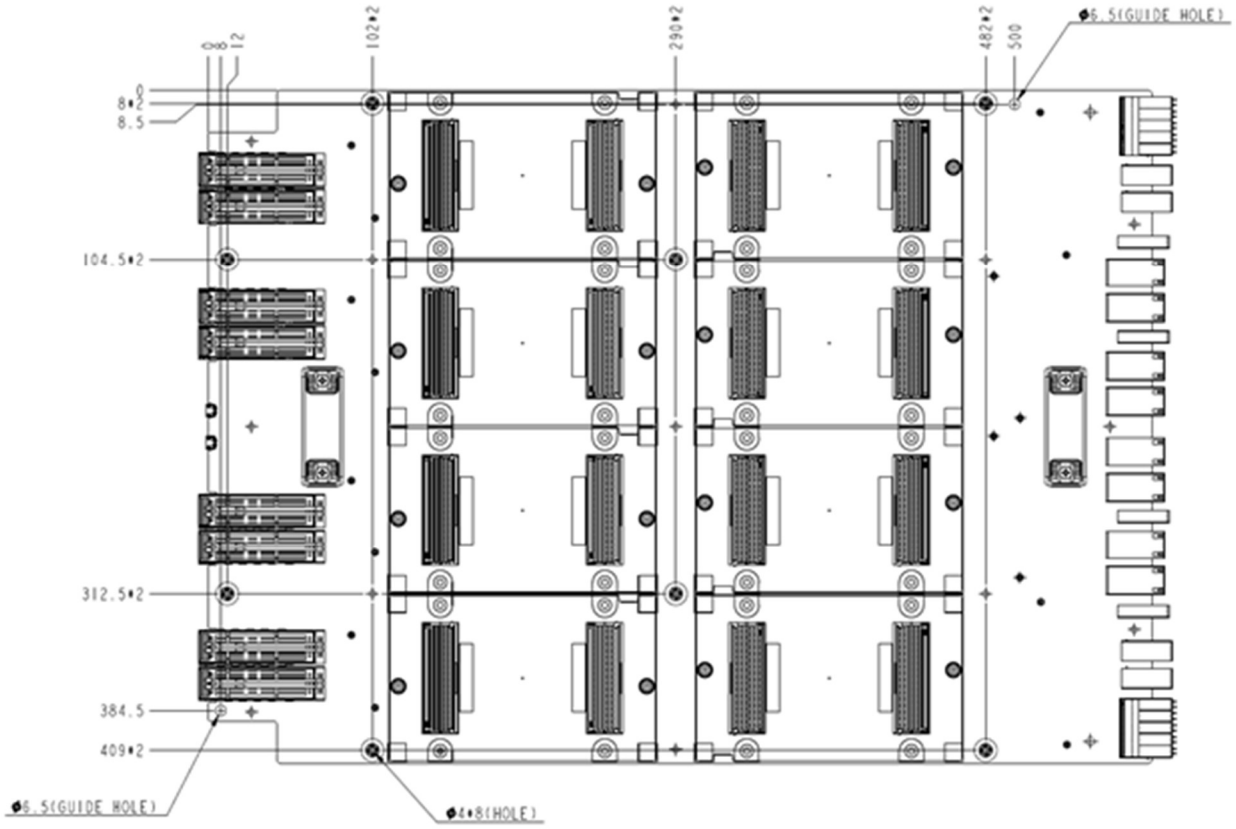


Figure 48 Mounting holes for bolster

8.3. Recommended Components

8.3.1. Air Baffle Holes

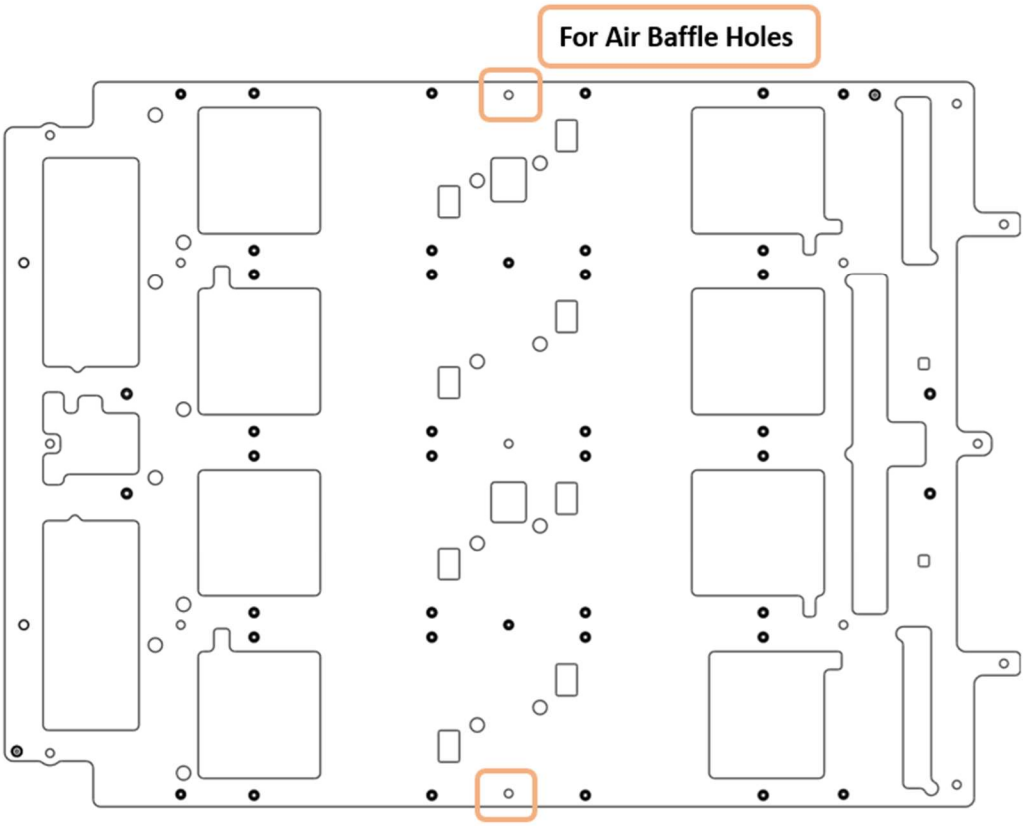


Figure 49 Air Baffle mounting holes on stiffener

Hole sizes and locations are recommended and may be customized for individual needs. The presence of an air baffle in the system is highly recommended, and reference designs are available as part of the 3D package.

8.3.2. UBB Handles

Southco handle (PN: P8-99-236)

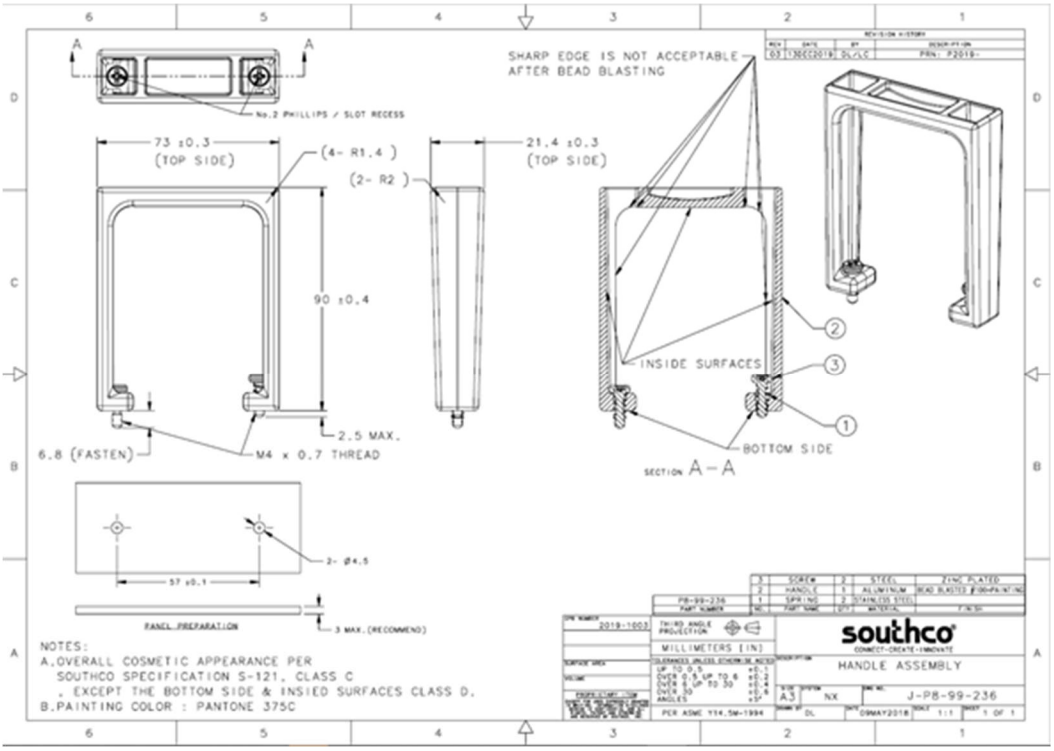


Figure 50 Reference UBB handle

UBB handles are intended for ease of assembly of the baseboard into the system. It is not intended to be used to lift the chassis in its entirety. The presence of these handles is highly recommended, although the exact size and type may be customized as part of the system design.

8.4. Assembly

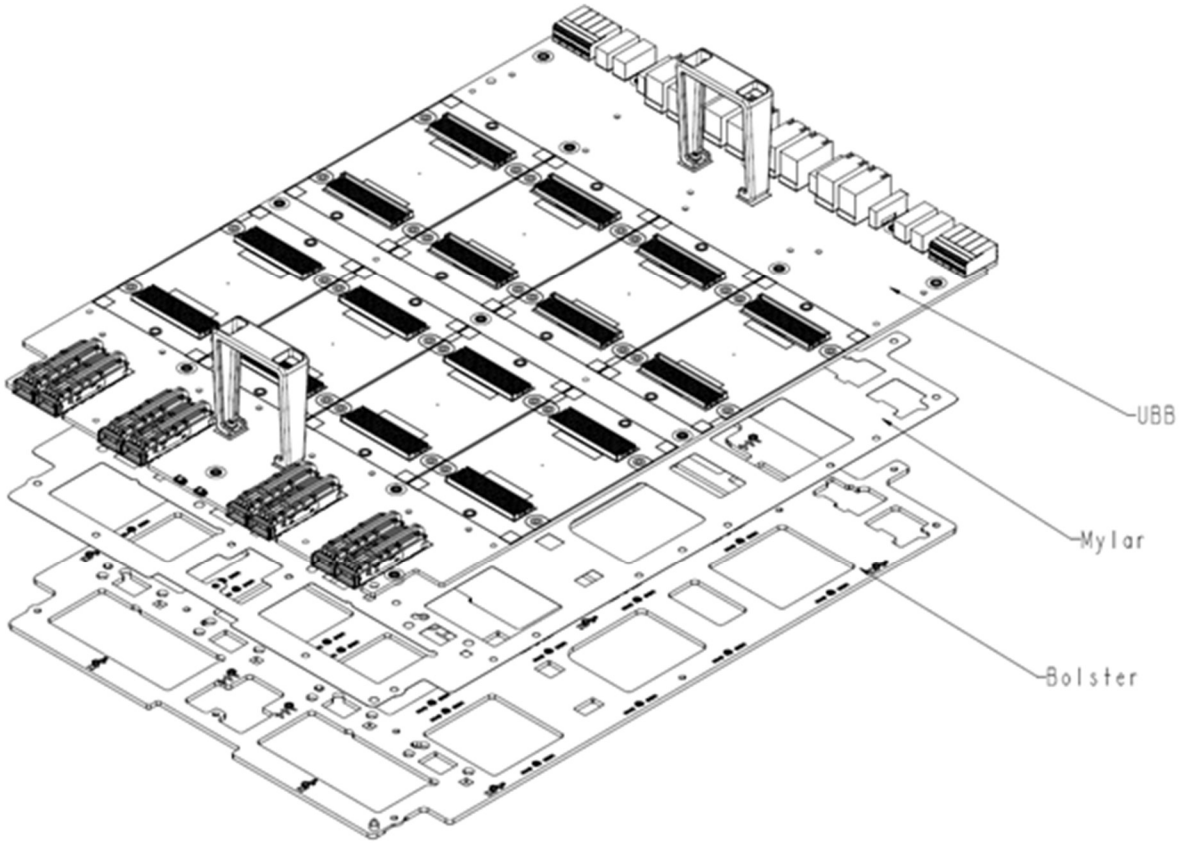


Figure 51 UBB assembly dwg

8.4.1. Screw Torque

Thread Type	Kgf-cm
M3.5	9
#6-32	9
M4	14

Table 50 Screw size and torque spec

8.4.2. Reference Bolster Plate

OAM module, handle with UBB board can be mounted to bolster via mounting screws.

thickness: 4 mm

material: Aluminum alloy

Mounting standoff: #6-32, M3.5 and M4 threaded

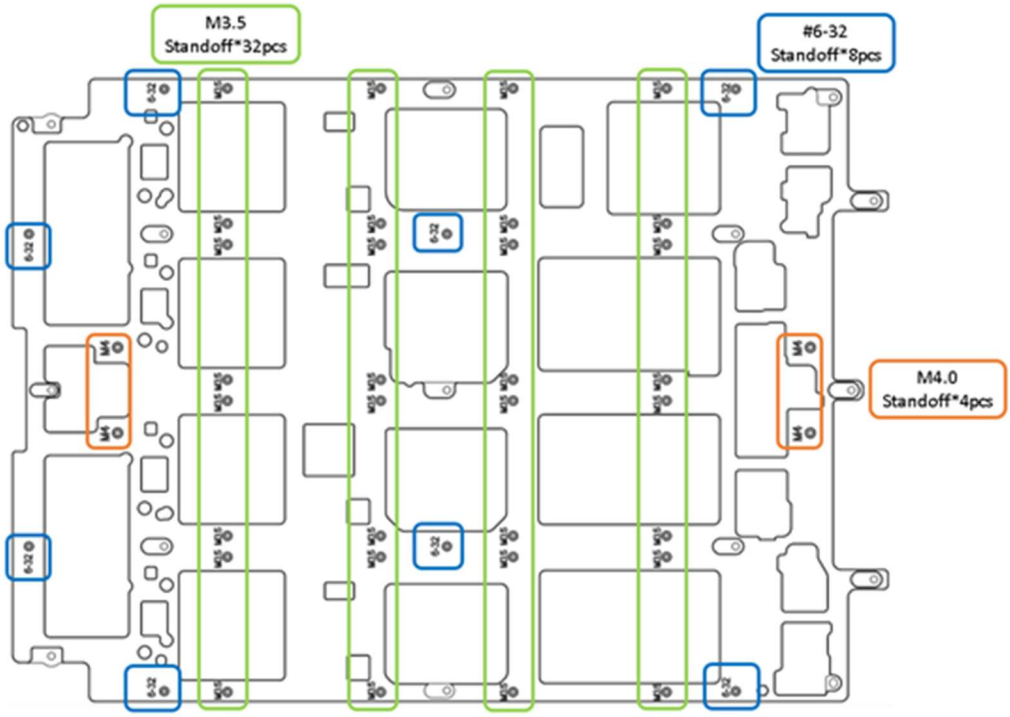


Figure 52 Bolster plate reference design

8.4.3. Mylar

Mylar insulators are located between the top and bottom bolster and UBB surface

thickness: 0.25 mm(include adhesive)

material: PC1870A/EFR85(reference)

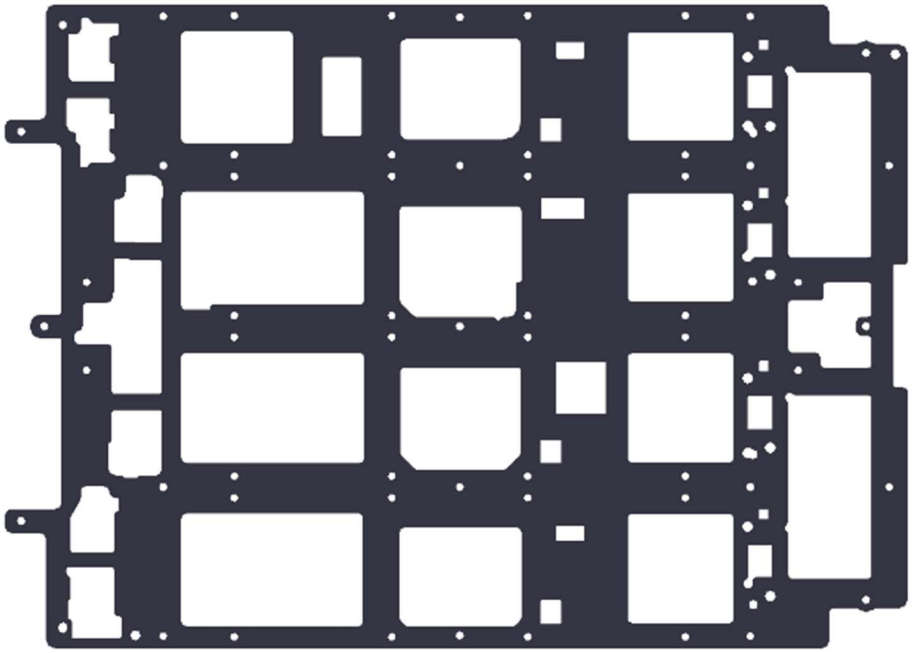


Figure 53 UBB mylar

9. Thermal and Cooling Specification

9.1. Environmental Conditions

To meet the thermal reliability requirement, the thermal and cooling solution should dissipate heat from the components when the components on UBB are operating at their thermal design power. The UBB module should be able to operate in the following environmental conditions without any throttling or thermal issues:

- Ambient temperature: 5°C to 35 °C
- Board surface approach temperature: 10°C to 55 °C
- Altitude: sea level to 3000 ft, without temperature deration
- Relative Humidity: 20% to 90%

Cold boot temperature: module should be able to boot and operate at an initial temperature of 10°C

In addition, the UBB should be able to remain unaffected at non-operational storage temperature range of -20°C to 85°C.

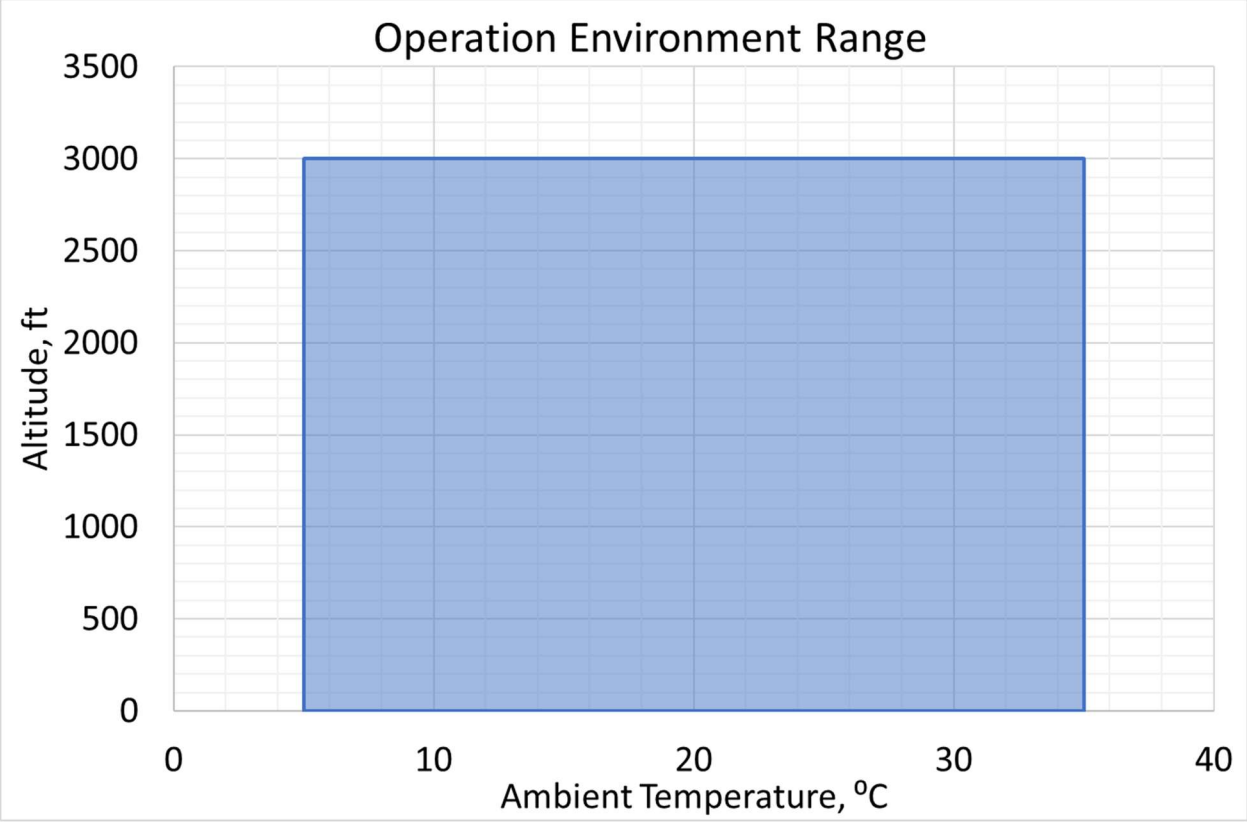


Figure 54 Module Operation Ambient Temperature

9.2. Air Flow Direction

The UBB is designed to operate at two different airflow directions which are:

1. QSFP connectors to OAMs to High Density Connectors
2. High Density Connectors to OAMs to QSFP Connectors

If the UBB is placed in airflow direction 1, the downstream components behind UBB might become thermally critical; if the UBB is placed in airflow direction 2, the QSFP connectors might become thermally critical.

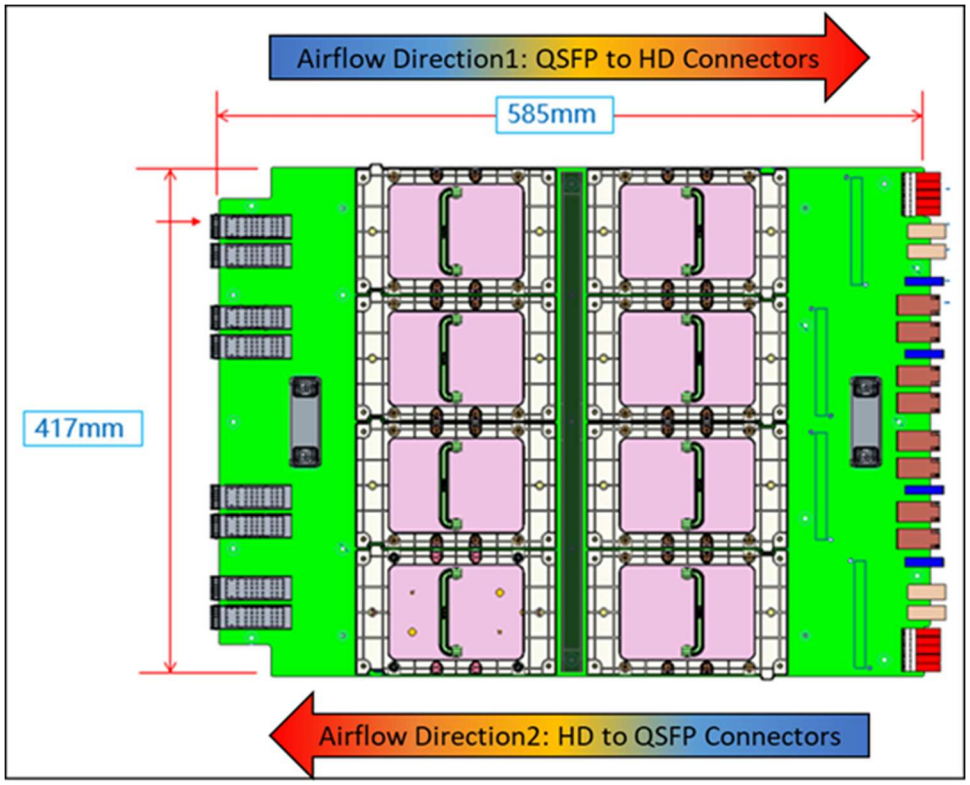


Figure 55 UBB at different airflow directions

9.3. Keep Out Zone

The heatsink manufacturing process such as diecasting and punching may have the tolerance lower than 0.3mm for contour, so for the stack up tolerance, it is recommended that to keep things out from the heatsink boundary at least 1mm away and preventing to place anything higher than the OAM chipset module to keep the heatsink In/Outlet flow area fluently.

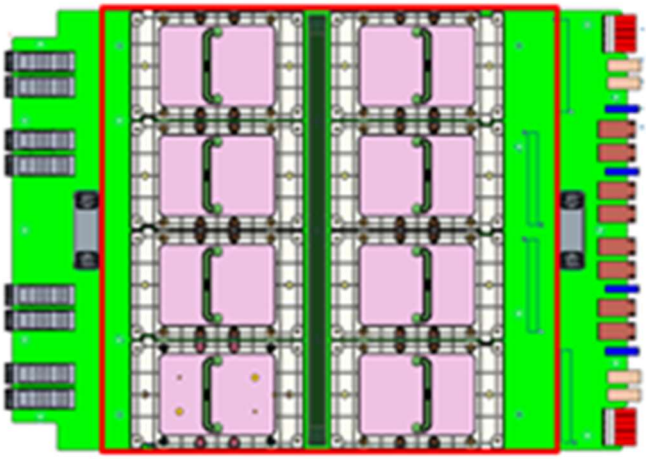


Figure 56 UBB heatsink recommended airflow area keep out

Extrude w/ push pin heatsink for small chips, the tolerance will be about +-0.3mm, it is recommended to follow the 1mm keep out and the height limit need to make sure everything under the heatsink lower than the chipset height, preventing to cover the area over heatsink for better assembly space and cooling.

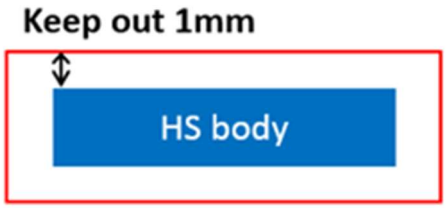


Figure 57 small heatsink keep out

9.4. Temperature Report

9.4.1. Temperature Sensors

Local ambient sensor on UBB board for Air cooling control or protecting shutdown, there are 6 sensors location for reference to monitoring the upstream and downstream flow, may base on the system requirement to choose the sensor location and quantity, sensors need to support both UBB downstream and upstream placement. And main inlet temperature sensor requirement is better to keep accuracy in ±3°C, the encountered accuracy is generally better than this. This inlet sensor should locate at the front end of the UBB board.

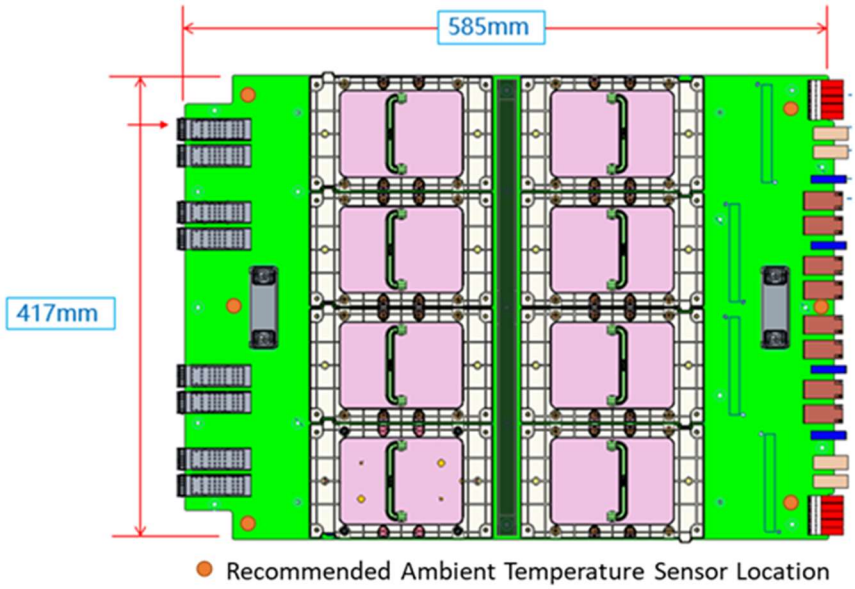


Figure 58 Recommended Ambient Temperature Sensor Map

If any sensitivity components cannot feedback itself, then will need an extra sensor nearby to ensure the location can reflect needs of the area of the system want to protect. They shall be placed as required to provide adequate protection for each major section of the system such as re-timer, QSFP and try to avoid power trace or something hot nearby. If the heat source cannot be avoided, the sensor must be inserted vertically.

The temperature sensor reading needs to be carefully calibrated for the operating temperature range specified in section 9.1, at different stress conditions. It's recommended to using 'standing' type temperature sensor instead of surface mounted type, and keep significant distance from heat sources, to avoid impact from adjacent heating.

9.5. Thermal Recommendation

9.5.1. Airflow Budget

It is recommended that the UBB module (contains 8*OAM and other on board hardware like retimer/switch, PHY, etc.) operates with full performance should be at or lower than airflow/power ratio of 0.158 CFM/W with ambient temperature 35°C at sea level. This is equivalent to an inlet/outlet air temperature increase of 20.2°F/11.2°C.

To keep downstream airflow meet 55°C common PCIe spec. Maximum inlet/ outlet temperature rise of UBB shall not be larger than 20°C at 35°C sea level.

- For operation at altitude, the same air temperature difference of 20.2°F/11.2°C or higher is recommended.
- Airflow (CFM) is defined as the total airflow supplied cross UBB.
- Power (Watts) is defined as max total power of all components on the UBB, on the same plane as the UBB (upstream/downstream components)

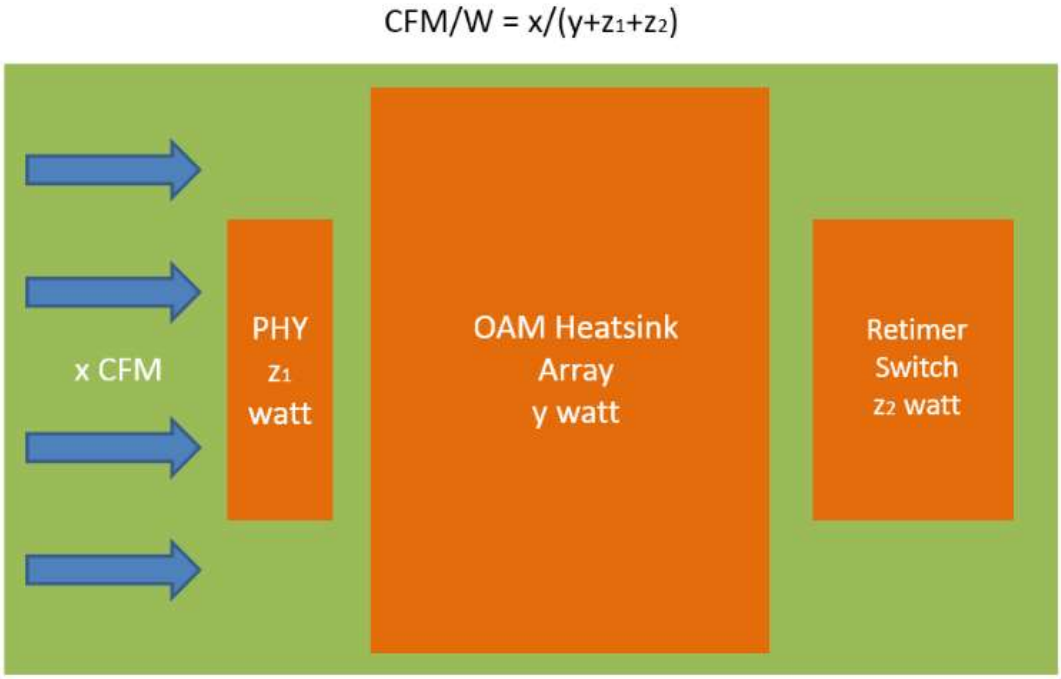


Figure 59 CFM per Watt definition for UBB

9.5.2. Reference Heatsink Design

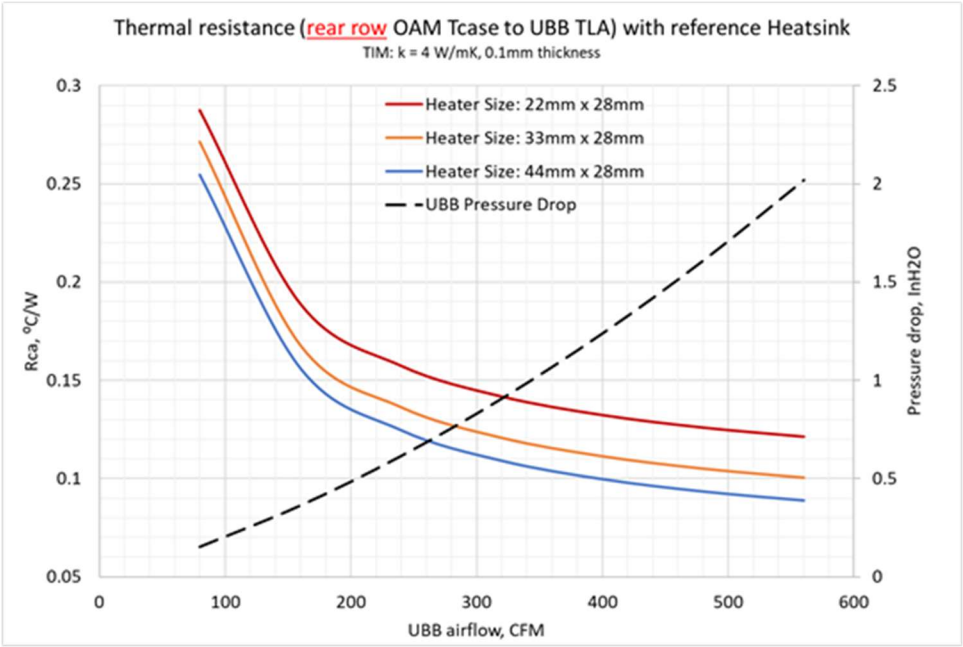


Figure 60 Thermal resistance and air pressure drop of UBB based on reference OAM Heatsink

Based on the OAM reference heatsink, the thermal resistance of the rear row OAM Tcase and the airflow pressure drop across the UBB are shown in Figure 9-7,9-8. Noted that the thermal resistance is calculated based on case temperature of the rear row (downstream) OAM, single OAM power, UBB total airflow rate and approach air temperature to the UBB front row.

$$R_{ca} = \frac{T_{case\_rear\ row\_OAM} - T_{UBB\_LA}}{P_{singleOAM}}$$

When the heatsink design fixed, the target Rca data can combine with the basic thermal capacitance calculation to roughly estimate the front row heatsink outlet temperature. May use this temperature outlet as rear row heatsinks inlet local ambient, and the Tcase and OAM Power input could refer to the chipset spec, and these parameters may find out the reference flow rate which system needed as the following equations.

$$T_{case\_rear\_row\_OAM} = T_{UBB_{inlet}} + \frac{4 \times P_{\_singleOAM}}{0.52 \times CFM} + P_{\_singleOAM} \times R_{\_heatsink}$$ Or

$$R_{\_heatsink\_target} = \frac{T_{\_case\_rear\_row\_OAM\_target} - T_{\_UBB\_inlet} - \frac{4 \times P_{\_singleOAM}}{0.52 \times CFM}}{P_{\ singleOAM}}$$

We recommend supplying airflow higher than 460CFM through the UBB to support the cooling of 400W OAMs at 35°C and sea-level. Cooling performance of the OAM reference heatsinks will start saturating beyond 500CFM (125CFM per heatsink). The performance of air-cooled heatsinks will become a limiting factor for higher approach air temperature or higher OAM power.

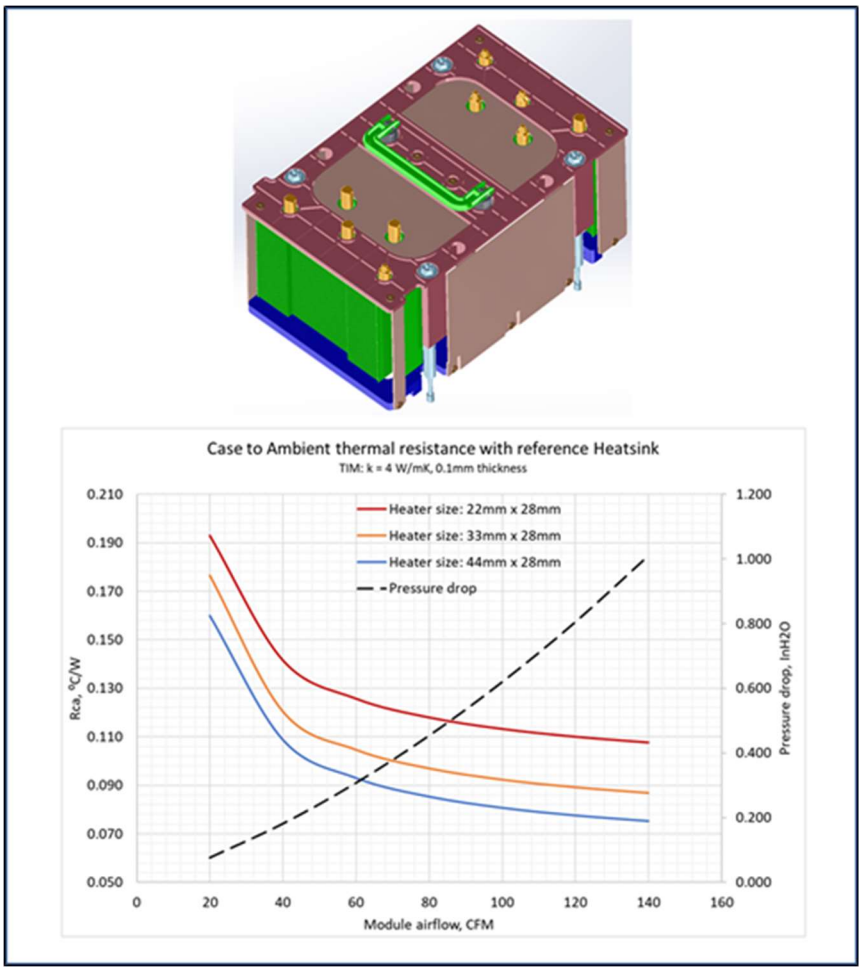


Figure 61 Thermal resistance of single OAM Reference Heatsink

9.5.3. Reference Liquid Cooling Design

Liuqid cooling design specification and guidance for OAM and OAI system is also under-developing. A high level introduction is provided in this section. The current liquid cooling solution considers using direct liquid cooled cold plates for OAM modules. It is a full OAI chassis level design for operating the cold plates. The goals of liquid cooling design are, that different OAM products and same liquid cooling solutions can be used in the same system; and the same OAM product and same liquid cooling solution can be used in multiple systems. The specifications are provided for standardization and design guidelines to expedite product development and deployment with minimized redesign efforts. Liquid cooling solution in this specification is aimed at supporting OAM power up to 700W.The liquid cooling design specification and guidance will consist of

- OAM cold plate
- Liquid cooling module
- Cold plate loop and fluid distribution
- Connectors
- System assembly
- Coolant requirement and hardware material
- Operating conditions

- Validation and Maintenance

At OAM level, an universal interface between OAM and coldplate will be defined. Particularly for bare-die products, a mechanical lid adapter will be introduced to establish thermal conduction path between components on the PCB (including package) and the coldplate. The lid adapter defines a universal interface for cold plates, allowing different cold plates to be mounted on different OAM products. In the case of a lidded-die package, an universal interface for cold plates is also defined including mechanical stiffeners.

Cooling module introduction: Liquid cooling module considers a design including all the liquid cooling components as one fully integrated unit, including OAM cold plates, cold plate loop and connections, fluid distribution, and auxiliary components if any. The entire cooling module is assembled and tested before assembling in a server chassis. This design improves reliability, minimizes leakage impact and damage in server chassis, improves serviceability and enables ease of operation. Derivative reference design slutions supporting 2 or 4 assemblies will also be provided.

A reference liquid cooling design for UBB is demonstrated in Figure 62. Cold plates cover the OAMs and the remaining components on UBB can be either air cooled or liquid cooled with extra coolant loops. The coolant supply to the UBB is divided into 4 parallel loops, each loop is assembled with two coldplates. The connectors interfacing with external coolant loops can be routed to different locations on the chassis, to match the rack level manifold design.

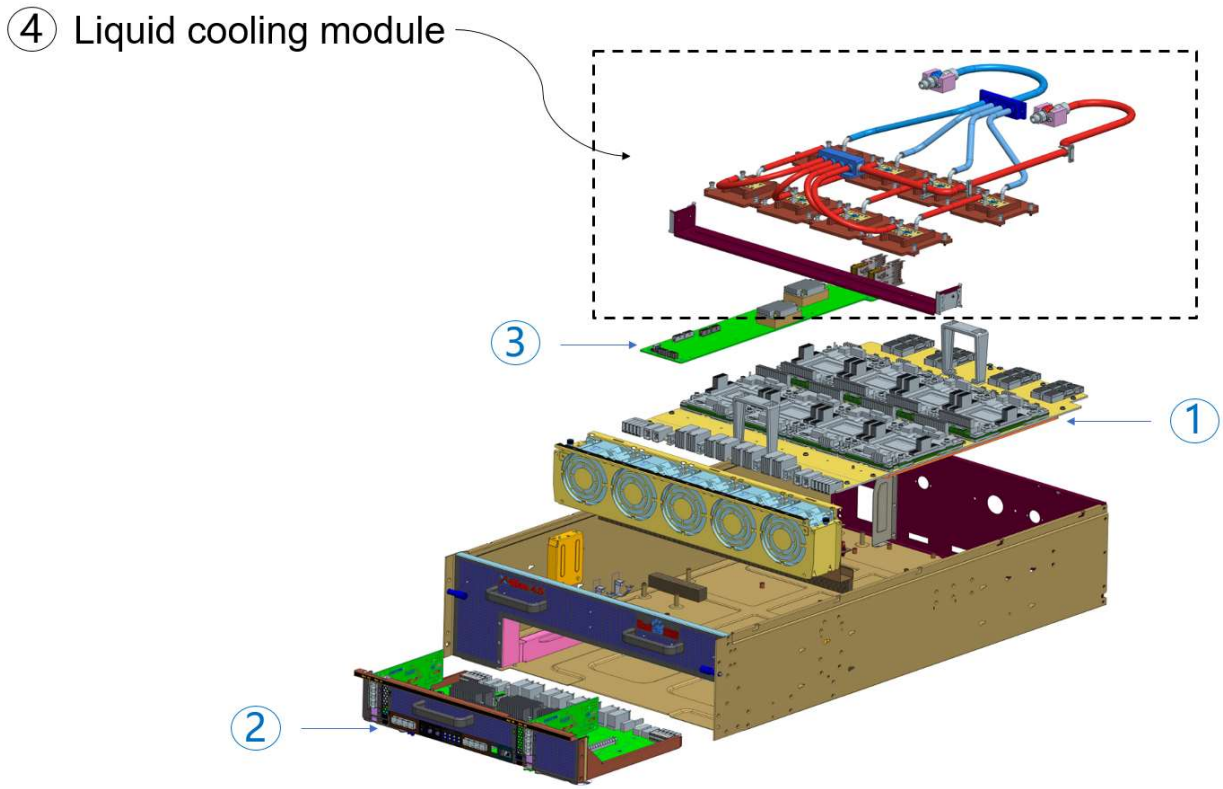


Figure 62 Reference Liquid Cooling Design for UBB. 1: Univiersal Base Board; 2: Host Interface Board; 3: Power Distribution Board; 4: Liquid Cooling Module. The cooling components and OAMs in the figure are just for concept demonstration and do not represent real solutions.

Currently, detailed liquid cooling specifications for OAI system are under developing, a full solution and detailed specifications will be released in a later version.

10. System Management

10.1. UBB I2C Topology

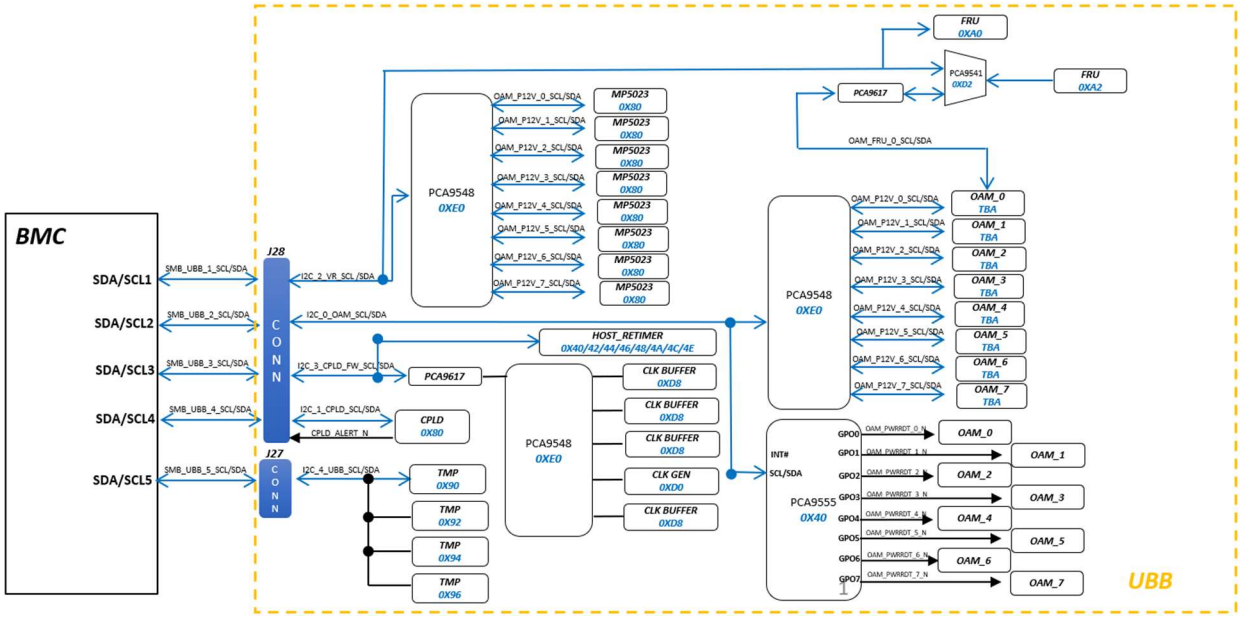


Figure 63 UBB I2C Topology

10.2. Sensors and Events

SEL Definition List

Term	Full Name
LNC	Lower non-recoverable
LC	Lower Critical (Critical low)
LNC	Lower Non-Critical
UNC	Upper Non-critical
UC	Upper Critical
UNR	Upper non-Recoverable
A	Assertion
D	De-assertion

S	Settable (Threshold sensor only)
R	Readable

Table 51 SEL Definition List

Sensor Name	Slave Addr.	Event/Reading Type	Event Triggers	Sensor Unit Type code
OAM_TEMP_0 OAM_TEMP_1 OAM_TEMP_2 OAM_TEMP_3 OAM_TEMP_4 OAM_TEMP_5 OAM_TEMP_6 OAM_TEMP_7	** Define by OAM vendor.	Threshold – 01h	9h: Upper critical going high (A, D, S, R)2h: Lower critical going low (A, D, S, R) A=2204 D=2204 R=1212	Degree C 01h
OAM_ PWR_0 OAM_ PWR_1 OAM_ PWR_2 OAM_ PWR_3 OAM_ PWR_4 OAM_ PWR_5 OAM_ PWR_6 OAM_ PWR_7	** Define by OAM vendor.	Threshold – 01h	9h: Upper critical going high (A, D, S, R) A=200 D=2200 R=1010	Watts 06h
OAM_PRSNT_0 OAM_PRSNT_1 OAM_PRSNT_2 OAM_PRSNT_3 OAM_PRSNT_4 OAM_PRSNT_5	0x80 CPLD	Discrete – 08h	0h: Device Absent 1h: Device Presnet <Event Only Type>	Unspecified 00h

OAM_PRSNT_6 OAM_PRSNT_7				
OAM_THERMTRIP_0 OAM_THERMTRIP_1 OAM_THERMTRIP_2 OAM_THERMTRIP_3 OAM_THERMTRIP_4 OAM_THERMTRIP_5 OAM_THERMTRIP_6 OAM_THERMTRIP_7	0x80 CPLD	Discrete – 03h	0h: State Deasserted 1h: State Asserted <Event Only Type>	Discrete 00h
HSC_P12V_VIN_0 HSC_P12V_VIN_1 HSC_P12V_VIN_2 HSC_P12V_VIN_3 HSC_P12V_VIN_4 HSC_P12V_VIN_5 HSC_P12V_VIN_6 HSC_P12V_VIN_7	0x80 HSC	Threshold – 01h	9h: Upper critical going high (A, D, S, R) 2h: Lower critical going low (A, D, S, R) A=2204 D=2204 R=1212	Volt 04h
HSC_P12V_VOUT_0 HSC_P12V_VOUT_1 HSC_P12V_VOUT_2 HSC_P12V_VOUT_3 HSC_P12V_VOUT_4 HSC_P12V_VOUT_5 HSC_P12V_VOUT_6 HSC_P12V_VOUT_7	0x80 HSC	Threshold – 01h	9h: Upper critical going high (A, D, S, R) 2h: Lower critical going low (A, D, S, R) A=2204 D=2204 R=1212	Volt 04h
HSC_P12V_IOUT_0	0x80 HSC	Threshold – 01h	9h: Upper critical going high (A, D, S, R)	Amps

HSC_P12V_IOUT_1 HSC_P12V_IOUT_2 HSC_P12V_IOUT_3 HSC_P12V_IOUT_4 HSC_P12V_IOUT_5 HSC_P12V_IOUT_6 HSC_P12V_IOUT_7			A=200 D=2200 R=1010	05h
HSC_P12V_PIN_0 HSC_P12V_PIN_1 HSC_P12V_PIN_2 HSC_P12V_PIN_3 HSC_P12V_PIN_4 HSC_P12V_PIN_5 HSC_P12V_PIN_6 HSC_P12V_PIN_7	0x80 HSC	Threshold – 01h	9h: Upper critical going high (A, D, S, R) A=200 D=2200 R=1010	Watts 06h
HSC_P12V_STS_0 HSC_P12V_STS_1 HSC_P12V_STS_2 HSC_P12V_STS_3 HSC_P12V_STS_4 HSC_P12V_STS_5 HSC_P12V_STS_6 HSC_P12V_STS_7	0x80 HSC	Sensor Specific - 6Fh	1h: Power Supply Failure detected (A, D, R). 2h: Predictive Failure (A, D, R) A=0006 D=0006 R=0006	Unspecified ooh
TEMP_INLET_0 TEMP_INLET_1 TEMP_OUTLET_0 TEMP_OUTLET_1	0x90 0x92	Threshold – 01h	9h: Upper critical going high (A, D, S, R) 2h: Lower critical going low (A, D, S, R)	Degree C 01h

			A=2204 D=2204 R=1212	

Table 52 Sensor name and Event table

10.3. UBB FRU Format

There're 2 FRU EEPROM in UBB board. FRU 0 is dedicated for BMC, and FRU 1 is shared with BMC and OAM #0. See next section for the FRU access mechanism.

FRU 0 and FRU1 are identical which contains both IPMI standard FRU format and UBB OAM Interconnect FRU. See below 2 pictures for the relationship of FRU 0 and FRU 1.

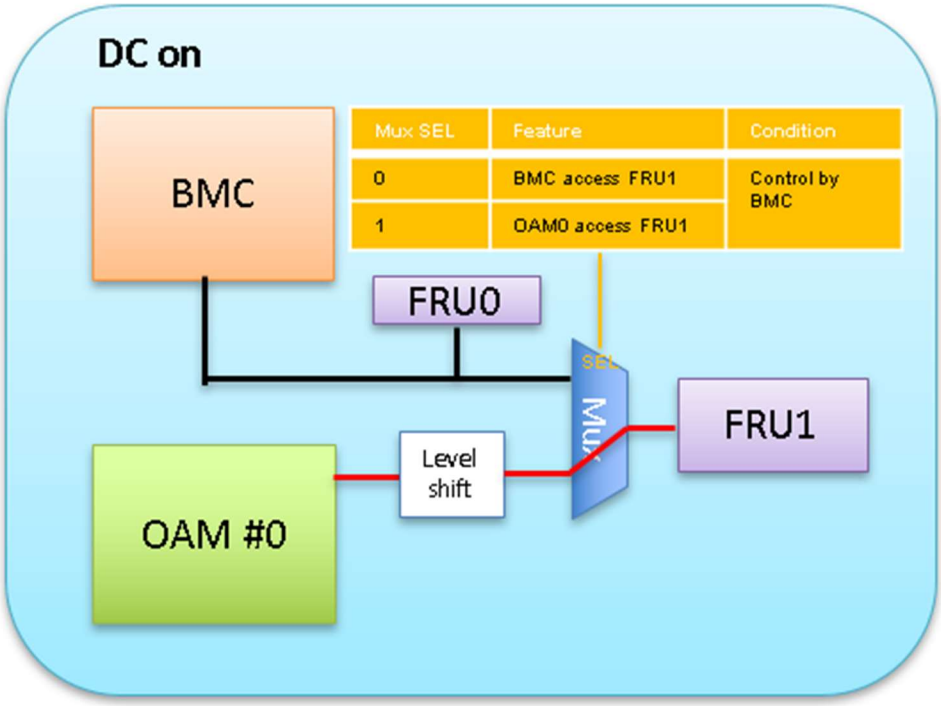


Figure 64 FRU diagram

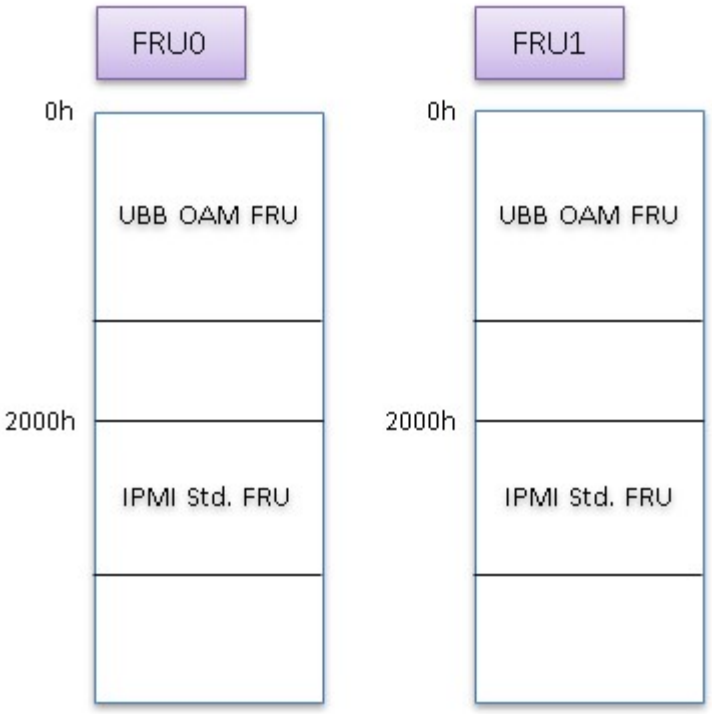


Figure 65 FRU0 and FRU1

IPMI standard FRU format: (offset 2000h)

IPMI standard FRU value is defined by ODM.

Field Name	Value
Board Mfg. Date	Example: “Fri Oct 11 05:58:00 2019”
Board Mfg.	Example: “HyveDesingSolutions” “ZT Systems” “Inspur”
Board Product	“OAI-UBB”
Board Serial	Defined by ODM.
Board Part Number	Defined by ODM.
Board Custom Info 1 for UBB type	String type of following: “3/4/6 Links HCM” “8 Links HCM” “FC” “FC+6 Links HCM”
Board Custom Info 2 for version	Example: “v1.00”

Table 53 FRU content-standard IPMI

UBB OAM Interconnect FRU format: (offset 0h)

Address (Hex)		Description	

000	UBB Type	Refer to OAM LINK_CONFIG Spec	Ex. 8'bxxx01000 – 3/4/6 Links HCM 8'bxxx01010 – FC + 4/6 Links HCM 8'bxxx01100 – 8 Links HCM 8'bxxx0xxxx0 – Reserved
001	UBB Spec Version	Supported UBB Spec Version	8'bxx
002	UBB SerDes width	OAM SerDes interconnect bus width	8'b00 – 2 bits 8'b01 – 4 bits 8'b10 – 8 bits 8'b11 – 16 bits
003	Number of OAM section	Total number of OAM section, for example OAM#0 to OAM#1 data is on 010h to 01Fh, total 16 bytes.	
004 – 00E		RESERVED	
00F	Zero-checksum	Zero-checksum for header, offset 0h to Eh, total 15 bytes.	
010	OAM#0 to OAM#1: SerDes Ports Mapping 1	OAM#0 to OAM#1 SerDes Port Mapping (lower 8 bits)	Ex. If OAM#0 SerDes port 1 and 5 are connected to OAM#1, then the setting is 8'b00010001
011	OAM#0 to OAM#1: SerDes Ports Mapping 2	OAM#0 to OAM#1 SerDes Port Mapping (upper 8 bits)	Ex. If OAM#0 SerDes port 2 and 4 are connected to OAM#1, then the setting is 8'b00001010
012	OAM#0 to OAM#1: Lane Reversal 1	OAM#0 SerDes Tx Ports lane reversal in x8 (lower 8 bits)	Ex. If OAM#0 SerDes port 3 and 5 are lane reversal, then the setting is 8'b00010100
013	OAM#0 to OAM#1: Lane Reversal 2	OAM#0 SerDes Tx Ports lane reversal in x8 (upper 8 bits)	Ex. If OAM#0 SerDes port 1 and 7 are lane reversal, then the setting is 8'b01000001
014	OAM#0 to OAM#1: Polarity Inversion 1	OAM#0 SerDes Tx Ports polarity inversion in x8 (lower 8 bits)	Ex. If OAM#0 SerDes port 3 and 5 are polarity inversion, then the setting is 8'b00010100
015	OAM#0 to OAM#1: Polarity Inversion 2	OAM#0 SerDes Tx Ports polarity inversion in x8 (upper 8 bits)	Ex. If OAM#0 SerDes port 1 and 7 are polarity inversion, then the setting is 8'b01000001
016	OAM#0 to OAM#1: Shortest PCB trace length	OAM#0 Tx to OAM#1 Rx shortest trace length	Ex. 0.5 inches stepping. If the trace length is 2.5inches, then the setting is 8'b0000101 (5)
017	OAM#0 to OAM#1: Longest PCB trace length	OAM#0 Tx to OAM#1 Rx longest trace length	Ex. 0.5 inches stepping. If the trace length is 16.5inches, then the setting is 8'b00100001 (33)
018 – 01E	OAM#0 to OAM#1:	RESERVED	
01F	Zero-checksum	Zero-checksum for OAM section, for example 010h to 01Eh, totoal 15 bytes.	
020 – 02F	OAM#0 to OAM#2	Refer to OAM#0 to OAM#1 description	

030 – 03F	OAM#0 to OAM#3	Refer to OAM#0 to OAM#1 description	
040 – 04F	OAM#0 to OAM#4	Refer to OAM#0 to OAM#1 description	
050 – 05F	OAM#0 to OAM#5	Refer to OAM#0 to OAM#1 description	
060 – 06F	OAM#0 to OAM#6	Refer to OAM#0 to OAM#1 description	
070 – 07F	OAM#0 to OAM#7	Refer to OAM#0 to OAM#1 description	
080 – 08F	OAM#0 to QDD	Refer to OAM#0 to OAM#1 description	
090 – 10F	OAM#1 to OAM#0 – 7 & QDD	Refer to OAM#0 to OAM#1 description	
110 – 18F	OAM#2 to OAM#0 – 7 & QDD	Refer to OAM#0 to OAM#1 description	
190 – 20F	OAM#3 to OAM#0 – 7 & QDD	Refer to OAM#0 to OAM#1 description	
210 – 28F	OAM#4 to OAM#0 – 7 & QDD	Refer to OAM#0 to OAM#1 description	
290 – 30F	OAM#5 to OAM#0 – 7 & QDD	Refer to OAM#0 to OAM#1 description	
310 – 38F	OAM#6 to OAM#0 – 7 & QDD	Refer to OAM#0 to OAM#1 description	
390 – 40F	OAM#7 to OAM#0 – 7 & QDD	Refer to OAM#0 to OAM#1 description	
410	QDD_0** to OAM# Connection 1	QDD to OAM# Connection (lower 8 bits)	Ex. If QDD is connected to OAM#5, then the setting is 8’b00010000
411	QDD_0** to OAM# Connection 2	QDD to OAM# Connection (upper 8 bits)	Ex. If QDD is connected to OAM#5, then the setting is 8’b00010000
412	QDD_0 to OAM# SerDes Ports Mapping 1	QDD to OAM SerDes Port Mapping (lower 8 bits)	Ex. If QDD is connected to OAM SerDes port 2, then the setting is 8’b00000010
413	QDD_0 to OAM# SerDes Ports Mapping 2	QDD to OAM SerDes Port Mapping (upper 8 bits)	Ex. If QDD is connected to OAM SerDes port 4, then the setting is 8’b00001000
414	QDD_0 Lane Reversal 1	QDD Tx port lane reversal in x8 (lower 8 bits)	Ex. If QDD Tx port is lane reversal, then the setting is 8’b00000001
415	QDD_0 Lane Reversal 2	QDD Tx port lane reversal in x8 (upper 8 bits)	Ex. If QDD Tx port is lane reversal, then the setting is 8’b00000001
416	QDD_0 Polarity Inversion 1	QDD Tx port polarity inversion in x8 (lower 8 bits)	Ex. If QDD Tx port is polarity inversion, then the setting is 8’b00000001
417	QDD_0 Polarity Inversion 2	QDD Tx port polarity inversion in x8 (upper 8 bits)	Ex. If QDD Tx port is polarity inversion, then the setting is 8’b00000001

418	QDD_0 Tx shortest PCB trace length	QDD Tx shortest PCB trace length	Ex. 0.5 inches stepping. If the trace length is 2.5inches, then the setting is 8'b0000101 (5)
419	QDD_0 Tx longest PCB trace length	QDD Tx longest PCB trace length	Ex. 0.5 inches stepping. If the trace length is 16.5inches, then the setting is 8'b00100001 (33)
41A -41E	QDD_0 to OAM#	RESERVED	
41F	Zero-checksum	Zero-checksum for QDD section, for example 410h to 41Eh, totoal 15 bytes.	
420 – 42F	QDD_1 to to OAM#	Refer to QDD_0 to OAM# description	
430 – 43F	QDD_2 to to OAM#	Refer to QDD_0 to OAM# description	
440 – 44F	QDD_3 to to OAM#	Refer to QDD_0 to OAM# description	
450 – 45F	QDD_4 to to OAM#	Refer to QDD_0 to OAM# description	
460 – 46F	QDD_5 to to OAM#	Refer to QDD_0 to OAM# description	
470 – 47F	QDD_6 to to OAM#	Refer to QDD_0 to OAM# description	
480 – 48F	QDD_7 to to OAM#	Refer to QDD_0 to OAM# description	
490 – 7FF	RESERVED	RESERVED	

**QDD_0 (QDD1_1), QDD_1(QDD1_2), QDD_2 (QDD2_1), QDD_3 (QDD2_2), QDD_4 (QDD5_1), QDD_5(QDD5_2), QDD_6 (QDD6_1), QDD_7 (QDD6_2)

Table 54 UBB OAM Interconnect FRU

11. 54V/48V Safety Requirement

11.1. Pollution Degrees

Pollution degrees are classified as follows:

- Pollution degree 1.

No pollution or only dry, nonconductive pollution occurs. The pollution has no influence. (example: sealed or potted products).

- Pollution degree 2.

Normally only nonconductive pollution occurs. Occasionally a temporary conductivity caused by condensation must be expected (example: product used in typical office environment).

- Pollution degree 3.

Conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to expected condensation (example: products used in heavy industrial environments that are typically exposed to pollution such as dust).

CREEPAGE DISTANCES in mm									
RMS Working Voltage up to and including V	1			2			3		
	Material Group								
	I	II	III	I	II	III	I	II	III
10	0.025	0.04	0.08	0.4	0.4	0.4	1.0	1.0	1.0
12.5	0.025	0.04	0.09	0.42	0.42	0.42	1.05	1.05	1.05
16	0.025	0.04	0.1	0.45	0.45	0.45	1.1	1.1	1.1
20	0.025	0.04	0.11	0.48	0.48	0.48	1.2	1.2	1.2
25	0.025	0.04	0.125	0.5	0.5	0.5	1.25	1.25	1.25
32	0.025	0.04	0.14	0.53	0.53	0.53	1.3	1.3	1.3
40	0.025	0.04	0.16	0.56	0.56	0.8	1.1	1.6	1.8
50	0.025	0.04	0.18	0.6	0.6	0.85	1.2	1.7	1.9
63	0.04	0.063	0.2	0.63	0.9	1.25	1.6	1.8	2.0

Table 55 Minimum creepage distances

11.2. Determination of minimum clearances

For equipment to be operated at more than 2000m above sea level, the minimum clearances should be multiplied by the factor give in IEC 60664-1.

Altitude (M)	Normal barometric pressure (kPa)	Multiplication factor for clearances
2000	80.0	1.00
3000	70.0	1.14
4000	62.0	1.29
5000	54.0	1.48
6000	47.0	1.70

Table 56 Altitude correction factors

11.3. Creepage and Clearance in Practice

Per OAM spec v1.0, the environmental requirements are operating altitude with no de-ratings

3048m (10000feet)- recommended as this is a Facebook spec and standard for Telco operation.

The clearance distance is about 2.58mm (2.0mm x 1.29) as below condition:

Pollution degree 3 and 63V: 2.0mm

Altitude 4000meter correction factor: 1.29

Please check your SAFETY certification vender what testing must be added if the clearance can't meet pollution distance and altitude factory.

12. Acronyms

Acronym	Definition
ASIC	Application Specific Integrated Circuit
OAM	OCP Accelerator Module
BGA	Ball Grid Array
BMC	Baseboard Management Controller
TDP	Thermal Design Power
EDP	Excursion Design Power
GPU	Graphic Processing Unit
MPN	Manufacturing Part Number
DXF	Drawing eXchange Format
PCBA	Printed Circuit Board Assembly

Table 57 Acronyms

13. Revision History

Revision	Date	Notes
v0.1	6/27/2019	First draft.
v0.42	10/23/2019	First draft to OCP community.
v1.0	6/28/2020	1. Update OAM power support, QSFP-DD description (Chapter 4, 5 , 5.3) 2. Add UBB behavior when OAM Thermal Trip (Chapter 5.4.3) 3. Add add UBB Power Ready “UBB_PWR_READY” description (Chapter 5.4.3) 4. Update OAM support power. 54V/12V power input and add power design guide (Chapter 5.5, 5.5.2, 5.5.3, 5.5.4) 5. Update System Clock Architecture description: Host to HIB in SRIS mode. HIB to UBB is common clock mode (Chapter 6.1.1) 6. Update I2C architecture/Topology with host retimer and PHY/SERDES retimer (Chapter 6.1.2) 7. Correct “SW board” typo to “HIB” (Chapter 6.1.4 , 7.2) 8. Power Control Block Diagram update: revise retimer VR wording from specific voltage value to Retimer_VR-0~3 (Chapter 6.1.5) 9. Update Module ID, Link_Config[4:0] based on OAM1.1 spec. (Chapter 6.1.6.1, 6.1.6.2) 10. update default JTAG MUX setting in JTAG Truth Table (Chapter 6.1.8) 11. Update UART description (Chapter 6.1.9) 12. Update debug header to optional (Chapter 6.1.10) 13. Update UBB power on sequence: add add P3V3_STBY, HOST_RETIMER_VR_EN, HOST_RETIMER_PWRGD, PHY_RETIMER_VR_EN, PHY_RETIMER_PWRGD . Modify retimer/PHY VR_EN, sequence and add notes (Chapter 6.1.11) 14. Add UBB power down sequence, also to revise UBB_PWRGD” to ”“MODULE_ENABLE” (Chapter 6.1.11) 15. Update 12V power connector vendor PN in UBB connector list. (Chapter 6.2) 16. Update HIF , QSFP-DD, OAM debug connector voltage level based on UBB standpoint. (Chapter 6.2.1) 17. Update high density connector pin list: HIF0-7: add SGPIO, PHY MDC/MDIO. Add 100Mhz clk. Add one more USB for UART. Add USB mux select. Remove EEPROM_WP in HIF4. Add UBB power ready pin. Correct some typo. (Chapter 6.2.1) 18. Update QSFP-DD, HIF0-7, Debug connector pin definition. Modify pin direction based on UBB stand point. Add HIF pin map info. (Chapter 6.2.1.4) 19. Update priminary CPLD block diag: add sequence, Reset, SGPIO (Chapter 6.4.1) 20. Correct CPLD “Truth Table” wording to “Primary CPLD Fan-out to OAMs” (Chapter 6.4.3) 21. Update I2C Slave register Map (Chapter 6.4.4) 22. Update priminary CPLD pin list: add SGPIO, host retimer/PHY retimer reset, host retimer/PHY retimer power enable/power good. (Chapter 6.5.5)

		23. Update CPLD IO bank 1.5V to support 1.2v-3.3V OAM vref, and the CPLD 1.5V level output in open-drain design (Chapter 6.5.5) 24. Add OAM Vref Based IO Pin chapter (Chapter 6.5.6) 25. Add host retimer section (Chapter 6.6) 26. Add SERDES PHY retimer section (Chapter 6.7) 27. Add High Speed SI guidance (Chapter 6.8) 28. Drawings update, sync with OAM v1.1 (Chapter 7) 29. Add UBB silkscreen (Chapter 7.6) 30. Update mechanical mounting holes, Grounding pads per OAM spec. Update bolster, SMT nuts and add detail ME drawings. (Chapter 8.2, 8.3, 8.4) 31. Add UBB connectors coordinate (Chapter 8.2.2) 32. Update Thermal airflow budget (Chapter 9.5.1) 33. Update Reference Liquid Cooling (Chapter 9.5.3) 34. Update UBB I2C tolology address: add FRU, host retimer, add 100MHz OAM clk buffer, correct and modify it to match i2c diag (Chapter 10.1) 35. Update UBB OAM FRU (Chapter 10.3) 36. Correct Figures and Tables Index 37. Modify table 13 for connectors type. 38. Delete words “(Input, Output are based on OAM UBB side)” in section 6.2.1.1. 39. Modify table 15, for changing I2C_SLV_CLK UBB direction POV from input to output. 40. Modify figure 24 for correcting connector drawing 41. Modify figure 25 for correcting connector drawing. 42. Modify table 20, connector position order to align connector spec. 43. Modify table 21, connector position order to align connector spec. 44. Add section 6.2.1.4 12V power connector re-purpose for 54V 45. Modify table 30 for correcting wording XDP to debug, correcting hook[6,7]’s voltage, add note for signal P1V8.

Table 58 Revision History