MF1 M/B

Avoton Micro-Server

PCB REV: C
PCBA REV: C2A
FAB: 3
SCH Rev:001
LAST UPDATE: 2015/02/03 1530

COVER PAGE

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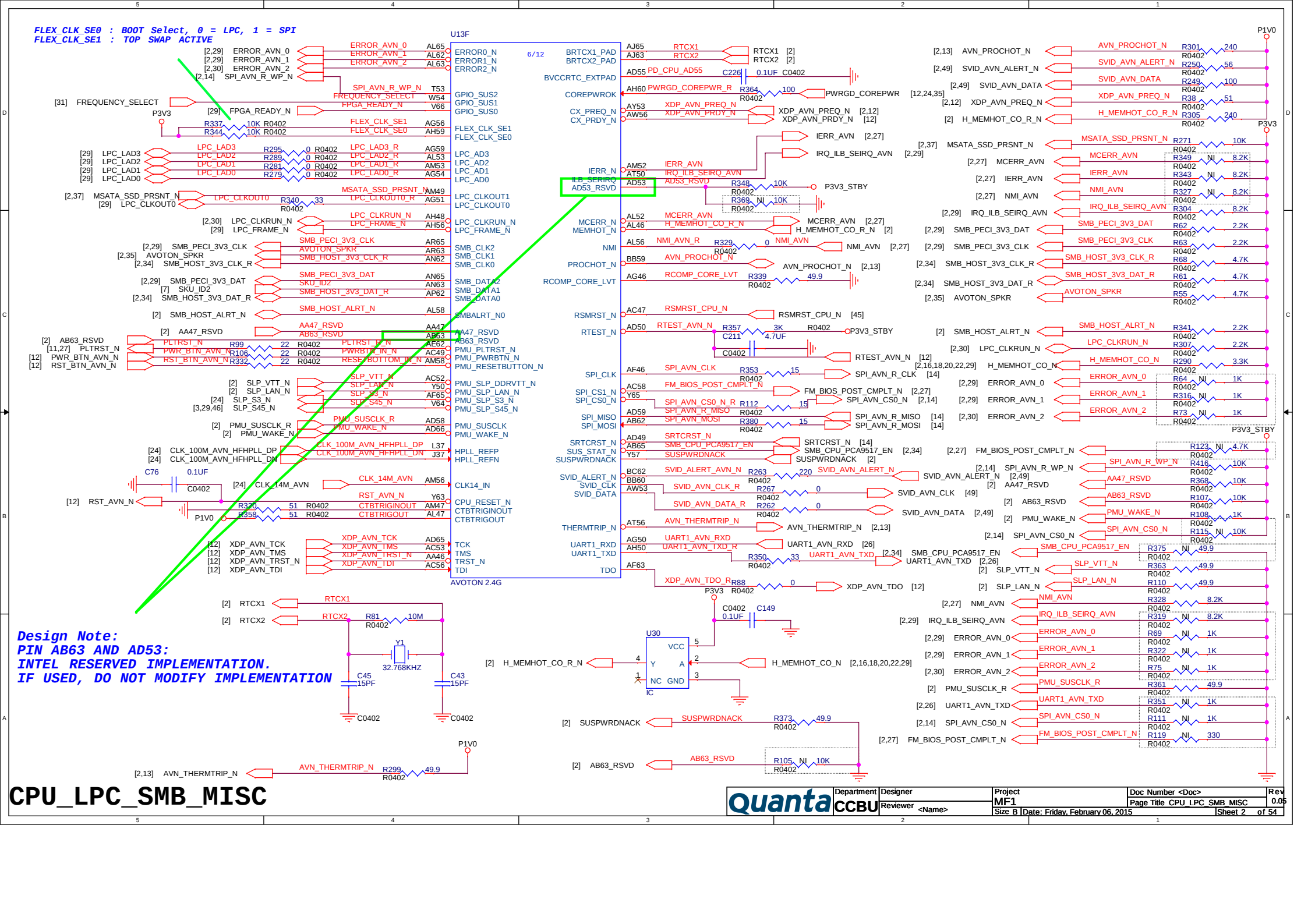
		Reviewer <Name>		Page Title Cover Page	
			Size B Date: Friday, February 06, 2015		Sheet 1 of 54


FLEX_CLK_SE0 : BOOT Select, 0 = LPC, 1 = SPI
FLEX_CLK_SE1 : TOP SWAP ACTIVE
U13F
6/12
AVOTON 2.4G
Design Note:
PIN AB63 AND AD53:
INTEL RESERVED IMPLEMENTATION.
IF USED, DO NOT MODIFY IMPLEMENTATION
CPU_LPC_SMB_MISC
Quanta
Department CCBU
Designer
Reviewer <Name>
Project MF1
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Page Title CPU_LPC_SMB_MISC
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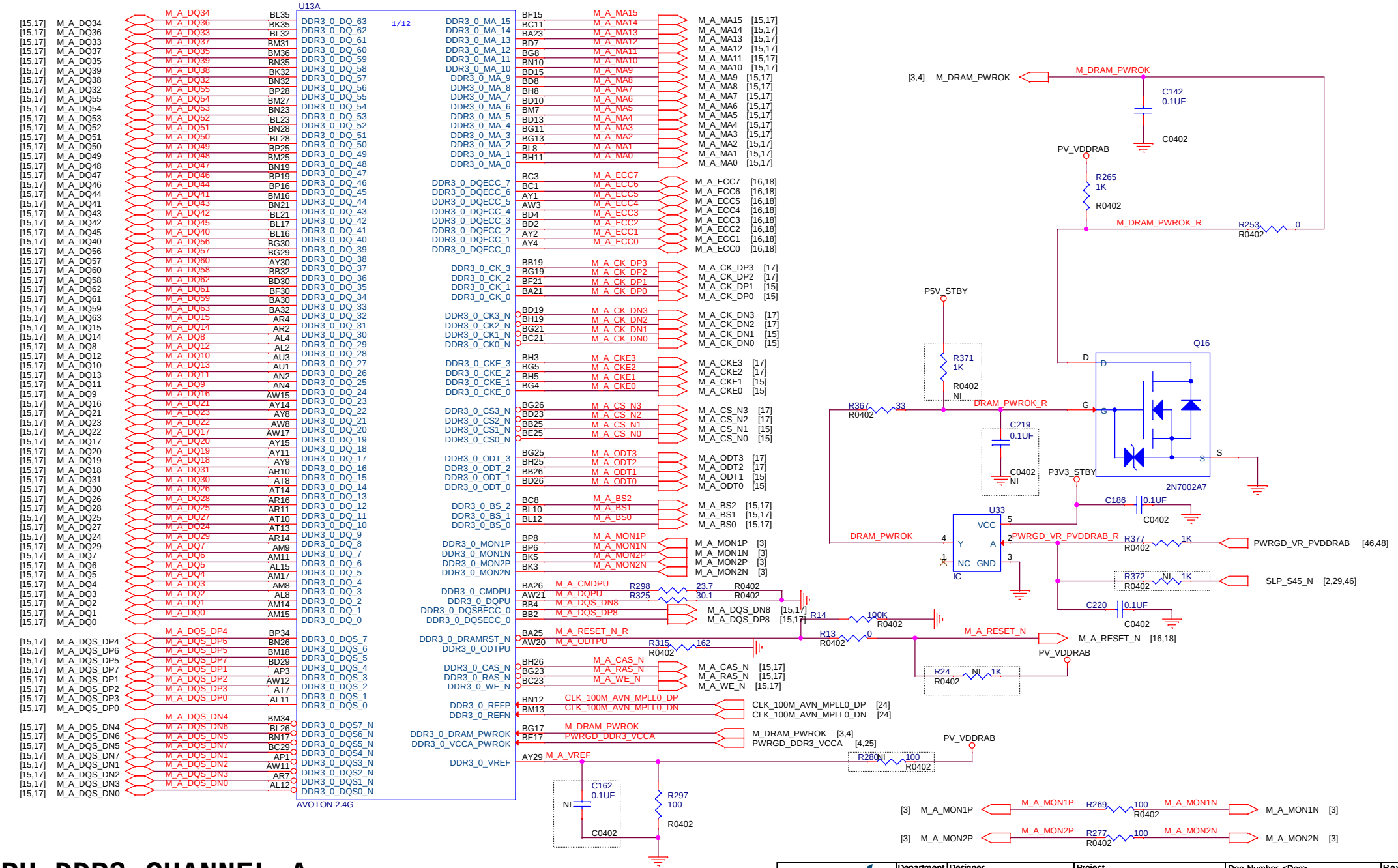

CPU_DDR3_CHANNEL_A

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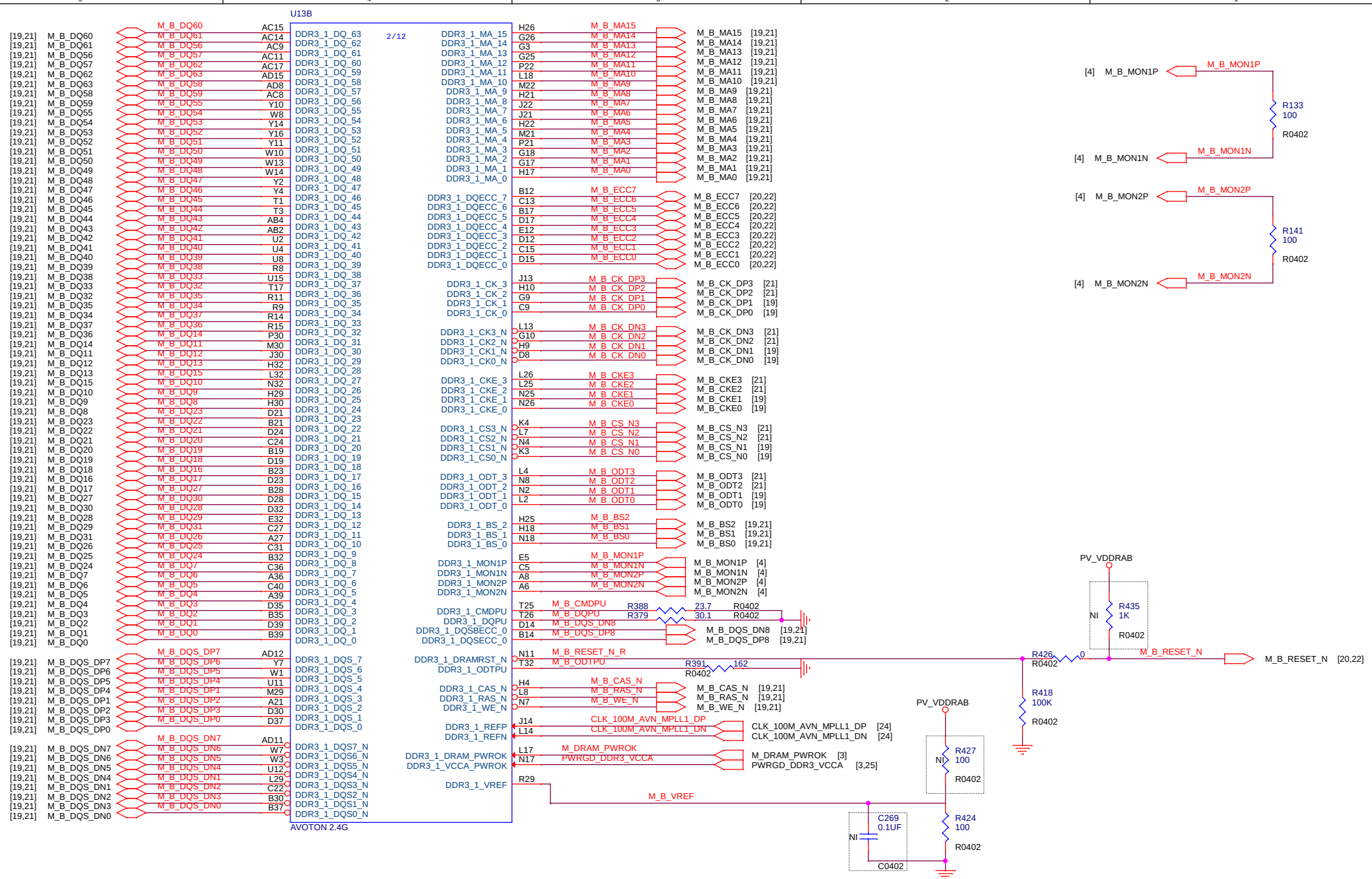
		Reviewer <Name>	Size B Date: Friday, February 06, 2015	Page Title CPU_DDR3_CHANNEL_A Sheet 3 of 54



CPU_DDR3_CHANNEL_B

Quanta	Department: CCBU	Designer	Project: MF1
	Reviewer: <Name>		Size: B Date: Friday, February 06, 2015

Doc Number	<Doc>
Page Title	CPU_DDR3_CHANNEL_B
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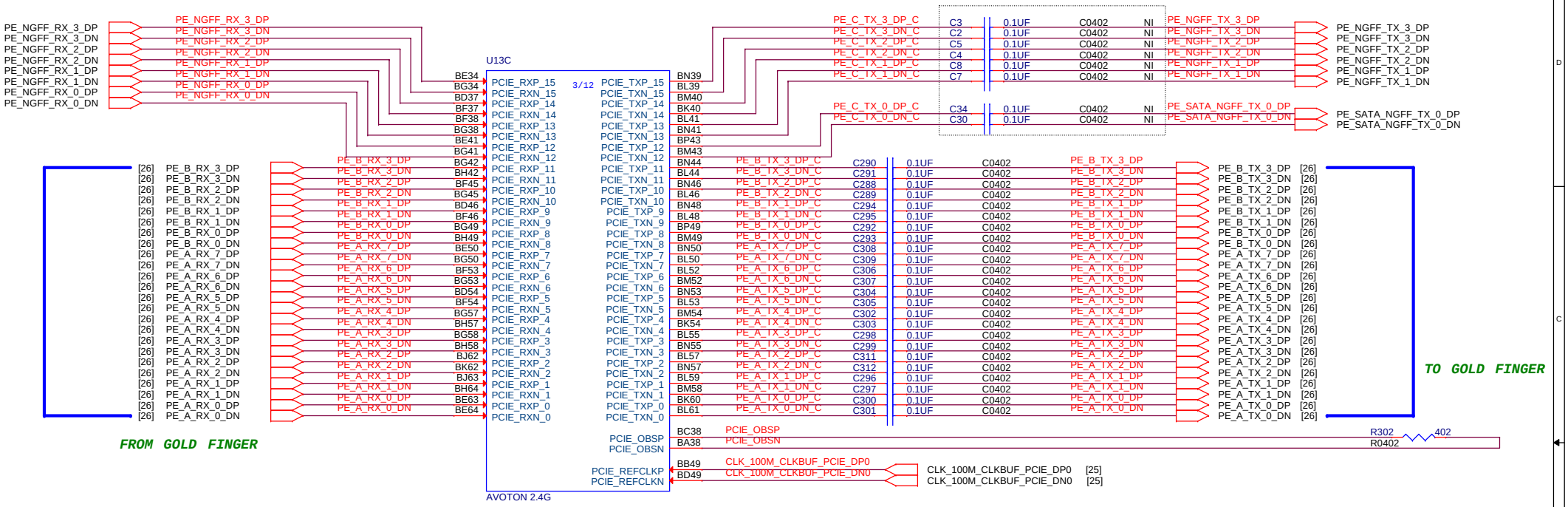
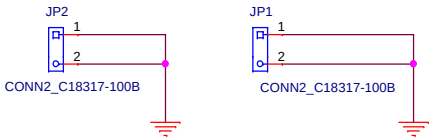


Bifurcation Control Register

Bifurcation Control 0 (BIFCTL0)	Lane Widths	Lane Numbers Assigned to Each Lane-Width Choice
000	x4 x4 x4 x4	Lanes 15:12 operate as x4 Lanes 11:8 operate as x4 Lanes 7:4 operate as x4 Lanes 3:0 operate as x4
001	x4 x4 x8	Lanes 15:12 operate as x4 Lanes 11:8 operate as x4 Lanes 7:0 operate as x8
010	x8 x4 x4	Lanes 15:8 operate as x8 Lanes 7:4 operate as x4 Lanes 3:0 operates as x4
011	x8 x8	Lanes 15:8 operate as x8 Lanes 7:0 operate as x8
100	x16	Lanes 15:0 operate as x16
101 - 111	Reserved	



CPU_PCIE_GEN2

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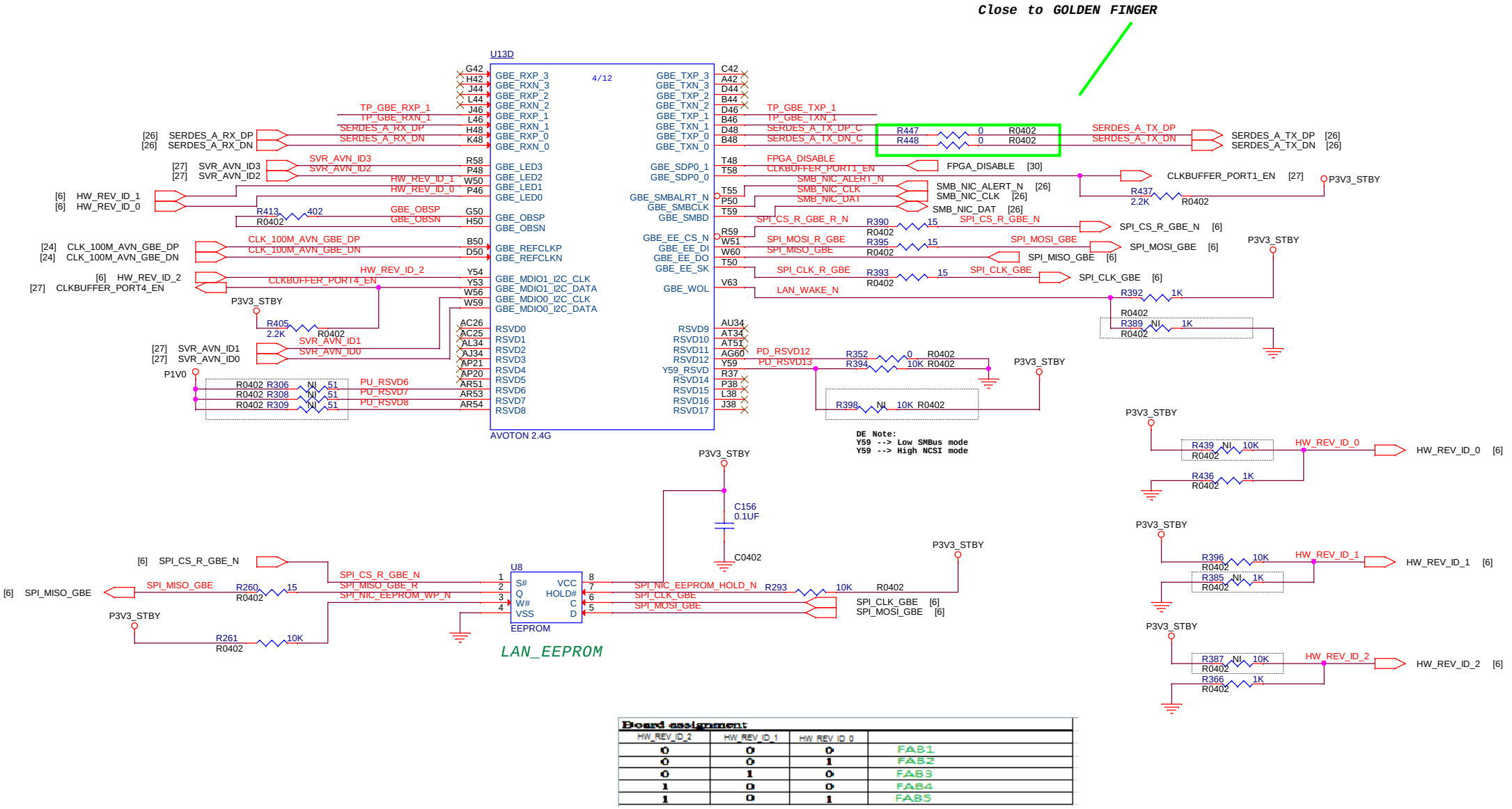
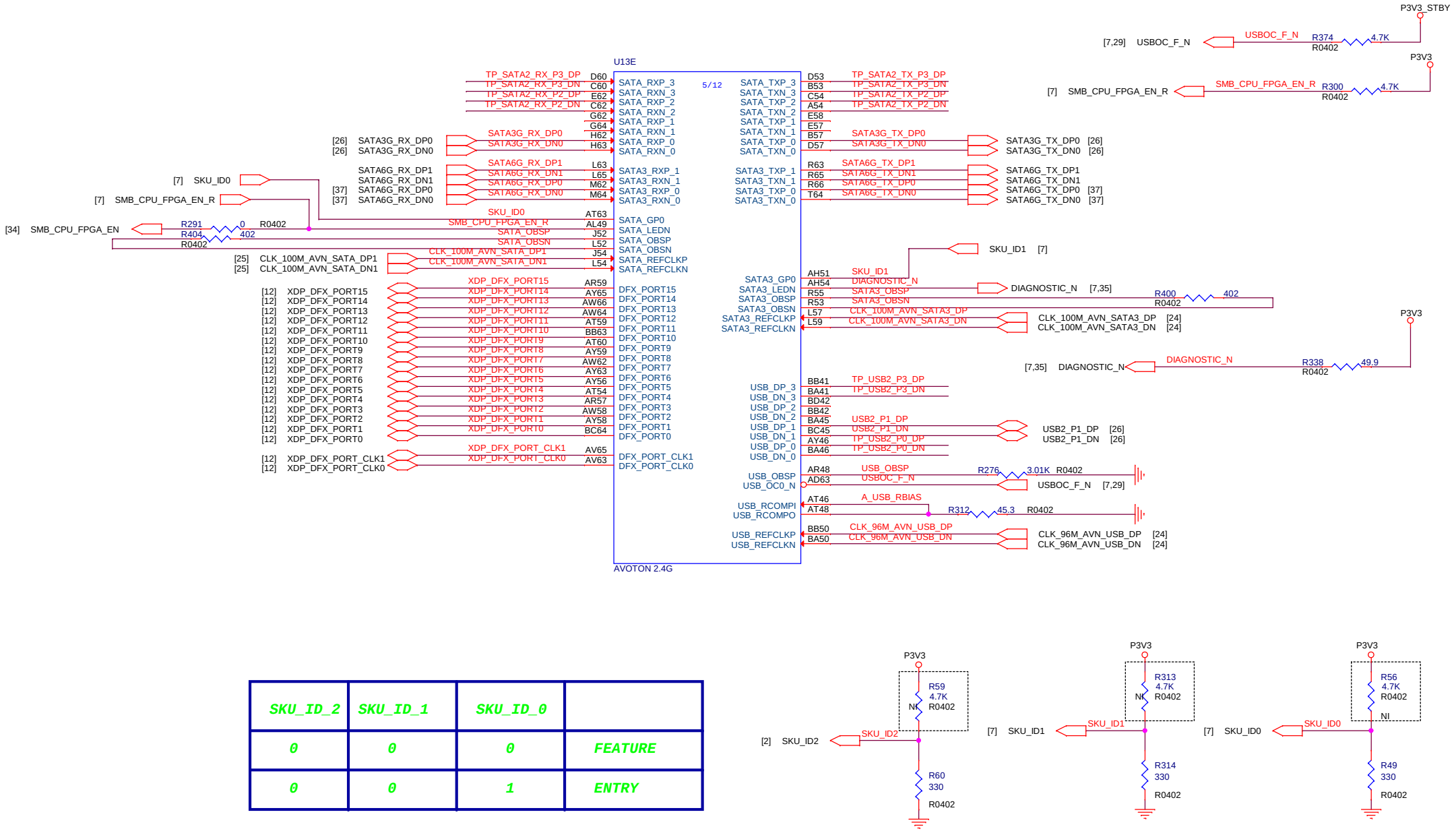


Board assignment

HW_REV_ID_2	HW_REV_ID_1	HW_REV_ID_0	
0	0	0	FAB1
0	0	1	FAB2
0	1	0	FAB3
1	0	0	FAB4
1	0	1	FAB5

CPU_GBE

Quanta	Department CCBU	Designer	Project MF1	Doc Number <Doc> Rev 0.05
		Reviewer <Name>	Size B Date: Friday, February 06, 2015	Page Title CPU_GbE Sheet 6 of 54



SKU_ID_2	SKU_ID_1	SKU_ID_0	
0	0	0	FEATURE
0	0	1	ENTRY

CPU_SATA_USB

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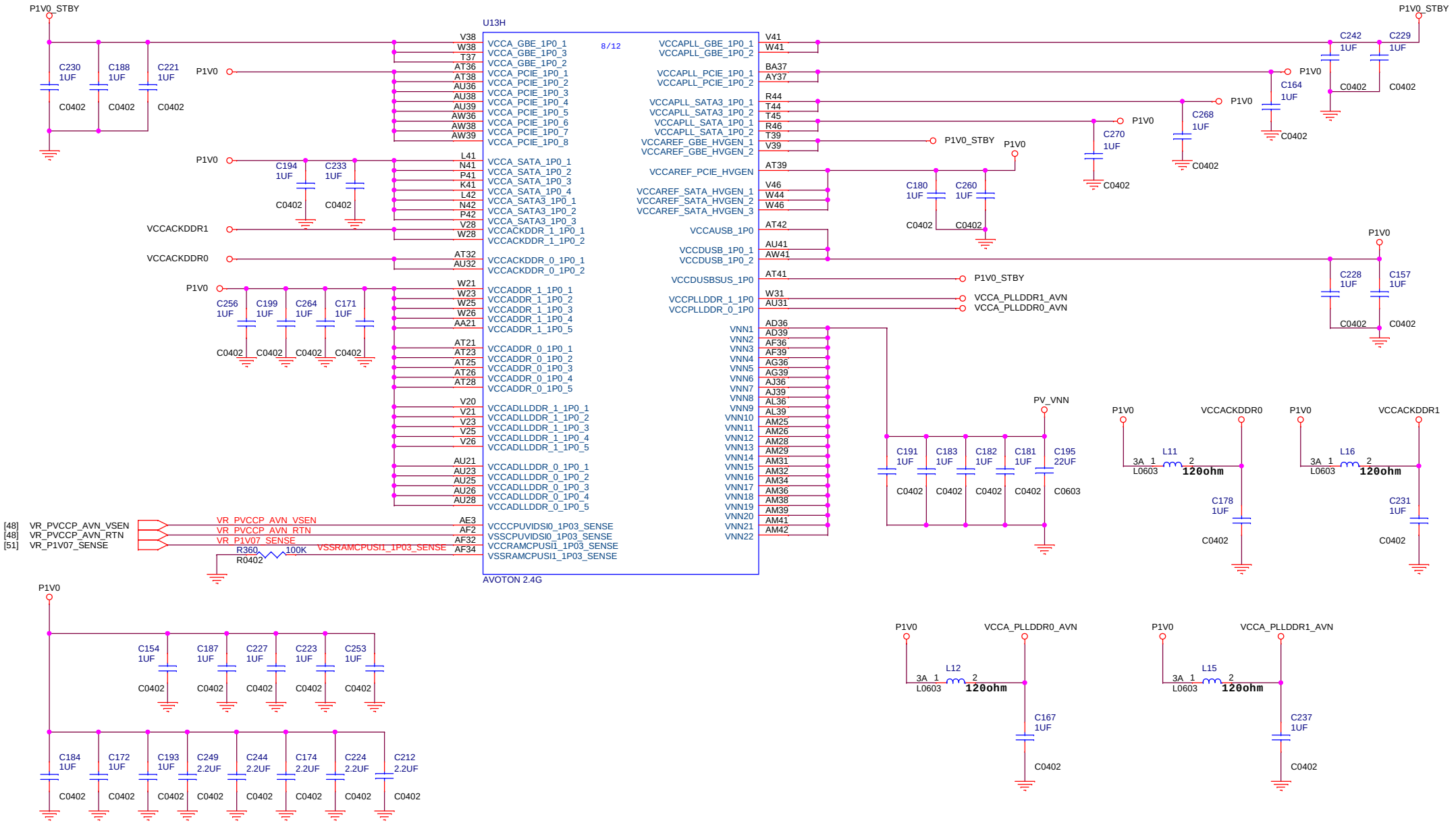
U13H
8/12
AVOTON 2.4G
P1V0_STBY
P1V0
VCCACKDDR1
VCCACKDDR0
PV_VNN
VCCA_PLLDDR1_AVN
VCCA_PLLDDR0_AVN
[48] VR_PVCCP_AVN_VSEN
[48] VR_PVCCP_AVN_RTN
[51] VR_P1V07_SENSE
VR_PVCCP_AVN_VSEN
VR_PVCCP_AVN_RTN
VR_P1V07_SENSE
R360 100K
R0402
VSSRAMCPUSI1_1P03_SENSE
120ohm
L0603
Quanta
CCBU
Tony_Chung
MF1
Page Title CPU_POWER_I
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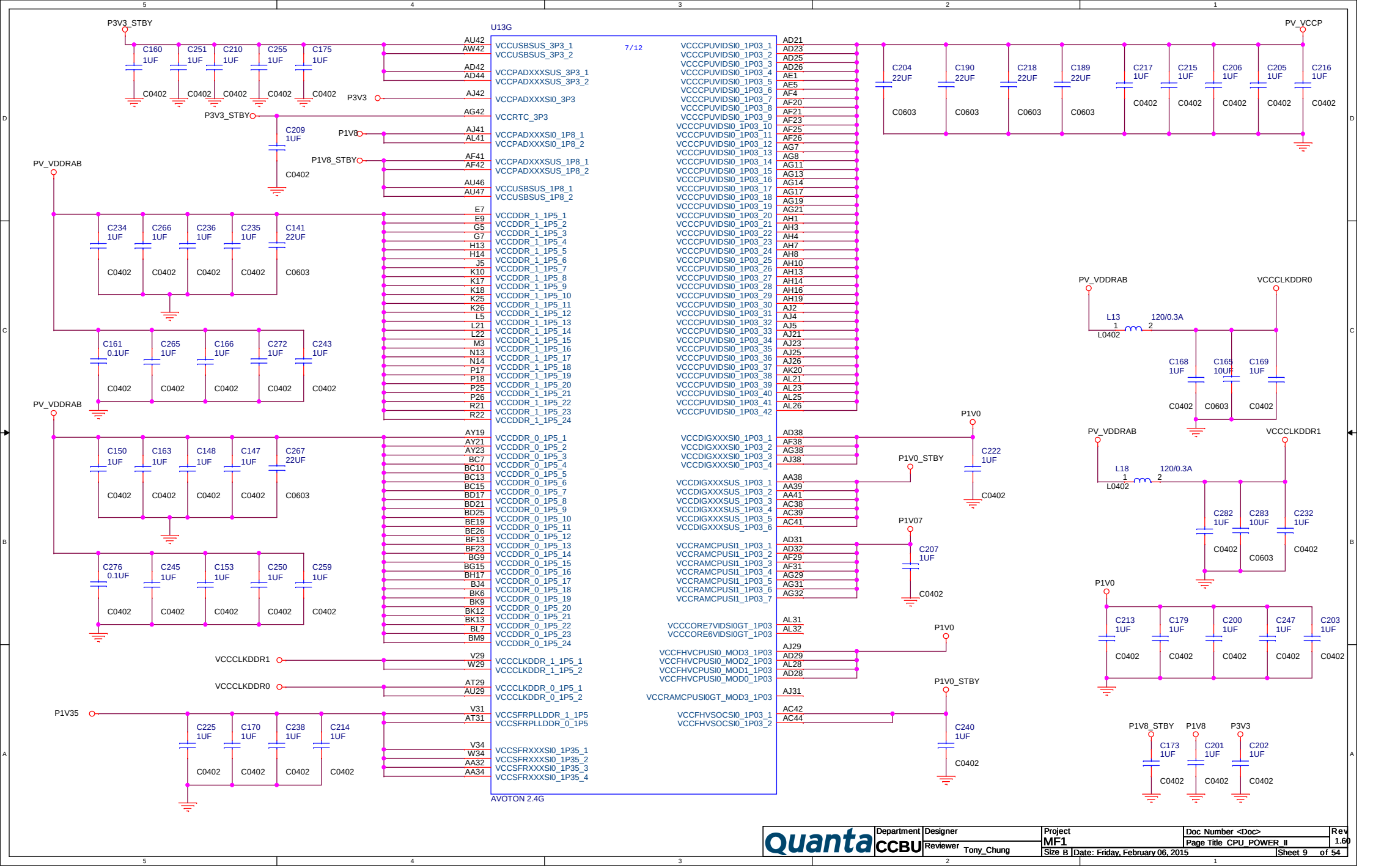
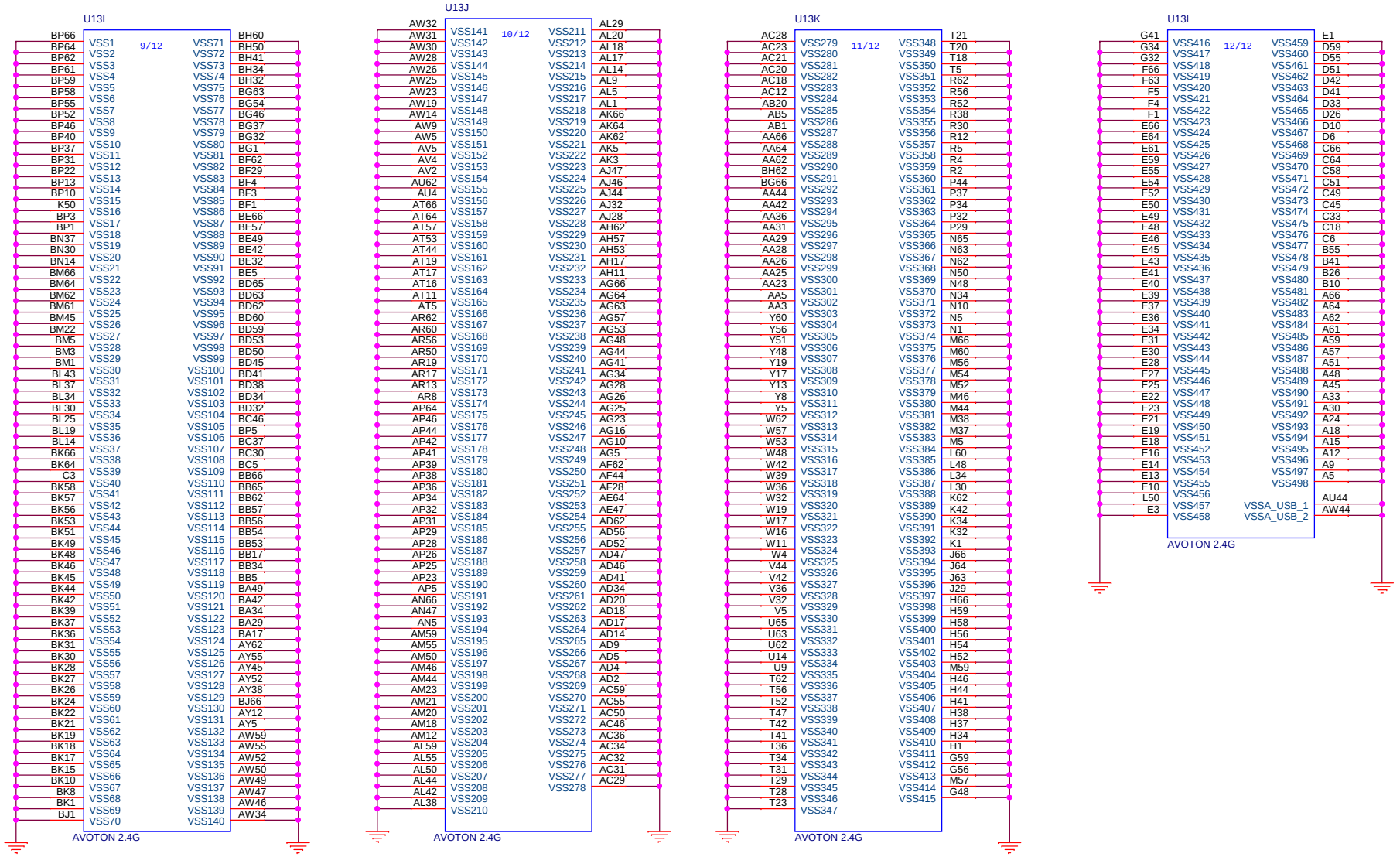
1.60



Quanta	Department CCBU	Designer	Project MF1	Doc Number <Doc>
		Reviewer Tony_Chung		Page Title CPU_POWER II
			Size B Date: Friday, February 06, 2015	Sheet 9 of 54

Rev 1.60



CPU_GND

Quanta	Department: CCBU	Designer	Project: MF1	Doc Number <Doc> / Rev 0.05
		Reviewer <Name>		Page Title CPU_GND
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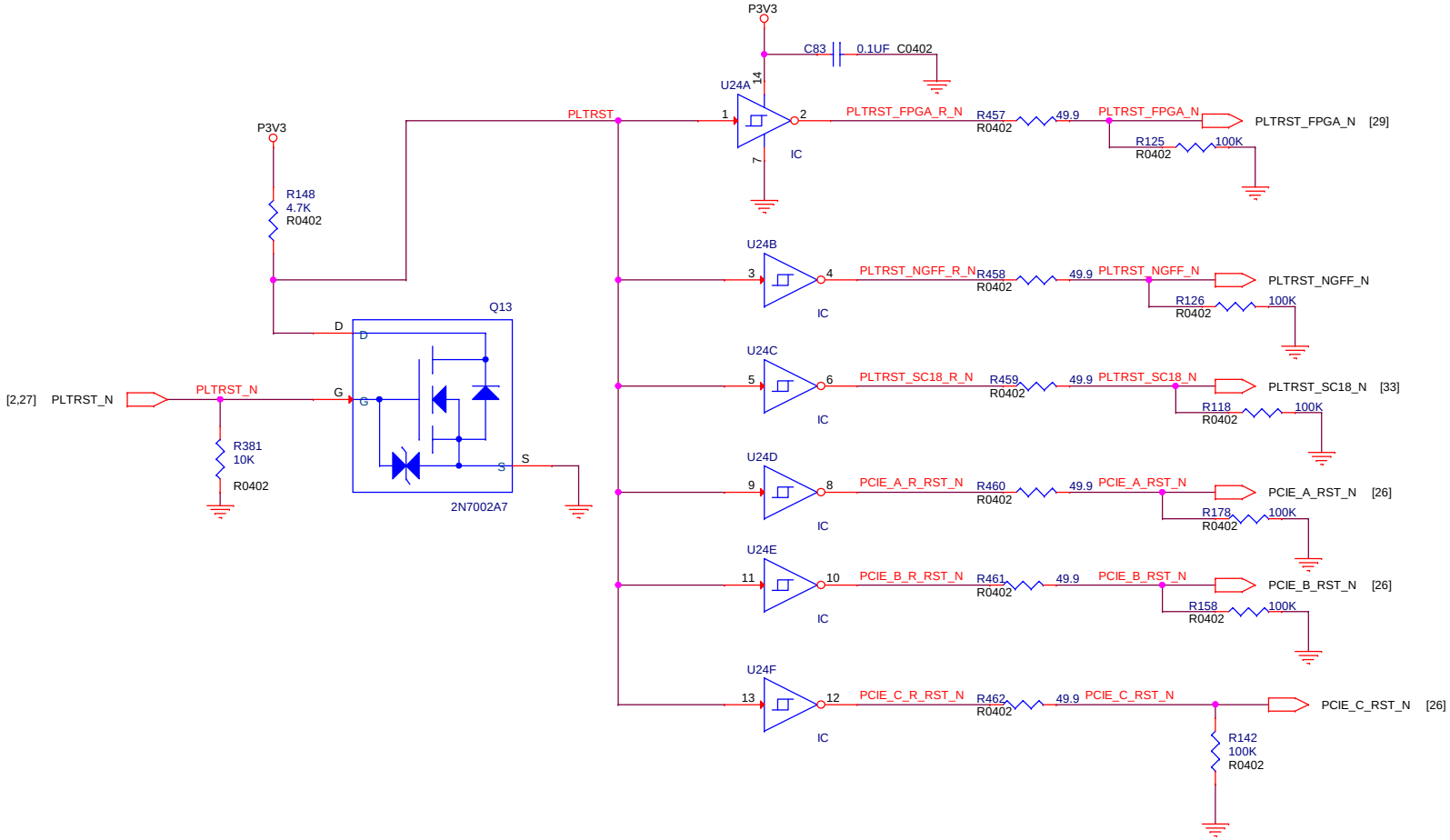
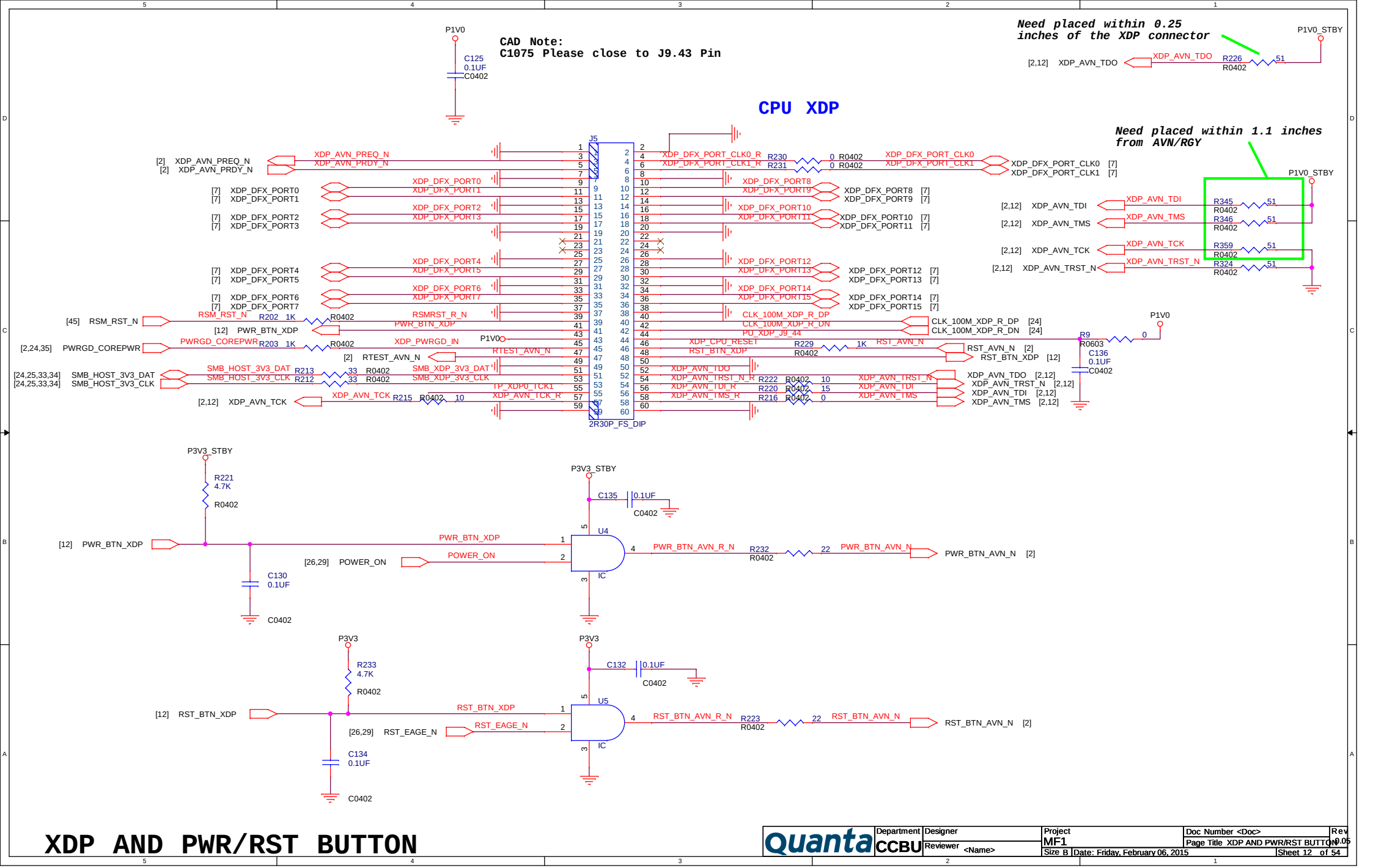


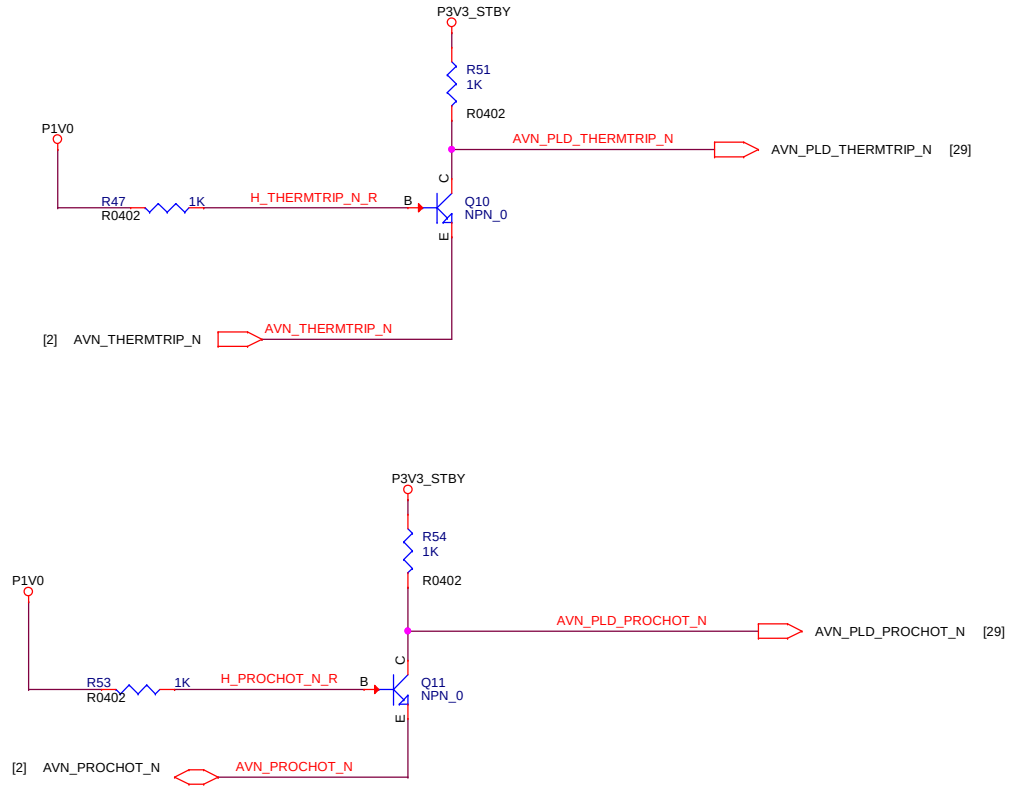
PLTRST_BUFFER

Quanta	Department CCBU	Designer	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title PLTRST_BUFFER	
			Size B	Date: Friday, February 06, 2015	Sheet 11 of 54



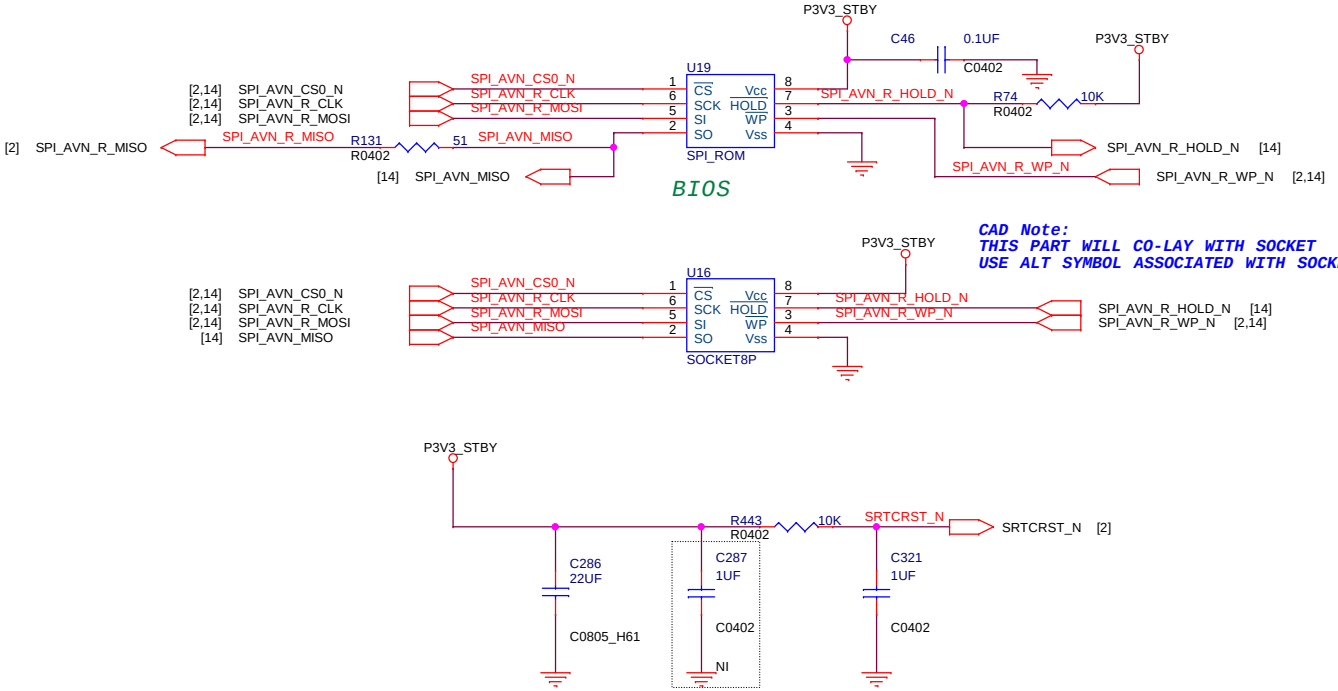
XDP AND PWR/RST BUTTON

Quanta	Department CCBU	Designer	Project MF1	Doc Number <Doc> Rev 0.05
		Reviewer <Name>	Page Title XDP AND PWR/RST BUTTON	
			Size B Date: Friday, February 06, 2015	Sheet 12 of 54



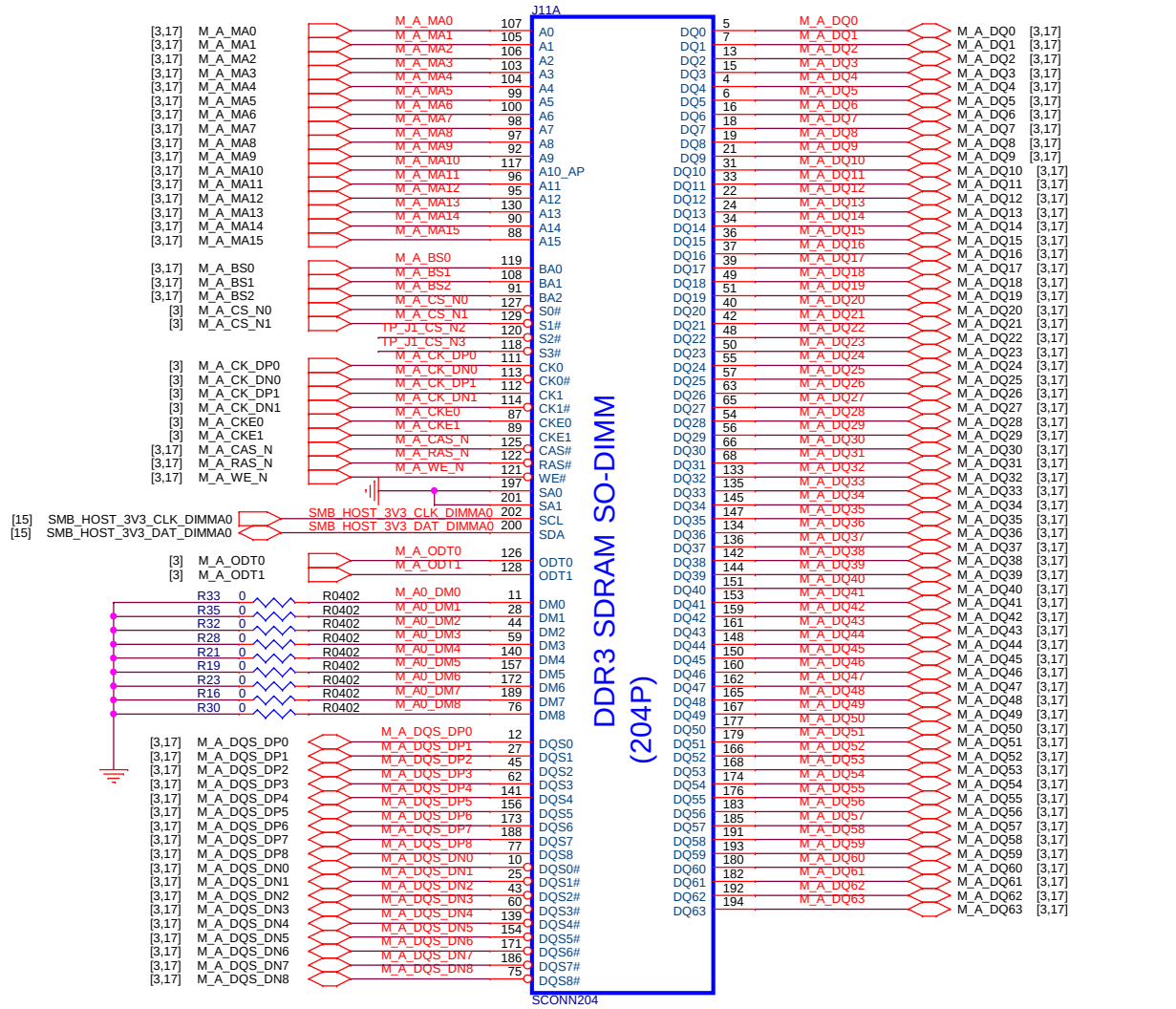
ERROR CNTL

Quanta	Department CCBU	Designer	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title ERROR CNTL	
			Size B Date: Friday, February 06, 2015		Sheet 13 of 54



CPU SPI

Quanta	Department CCBU	Designer	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title CPU_SPI	
			Size B Date: Friday, February 06, 2015		Sheet 14 of 54



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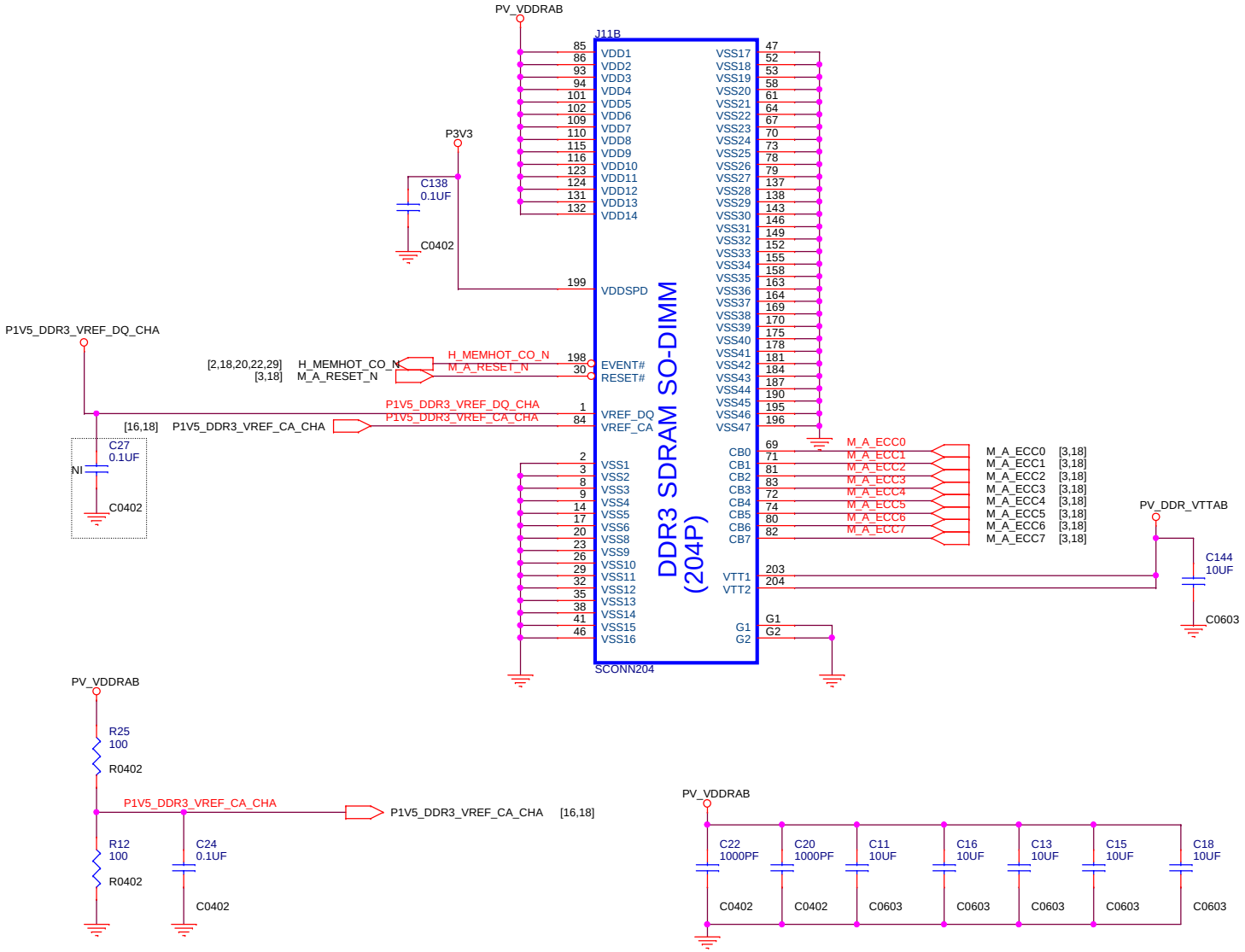
DDR3_SODIMM_CHA0_1

Quanta	Department CCBU	Designer	Project MF1	Doc Number <Doc> Rev 0.57
		Reviewer Chih-Ta Chen 92081366	Size B Date: Friday, February 06, 2015	Page Title DDR3_SODIMM_CHA0 Sheet 15 of 54



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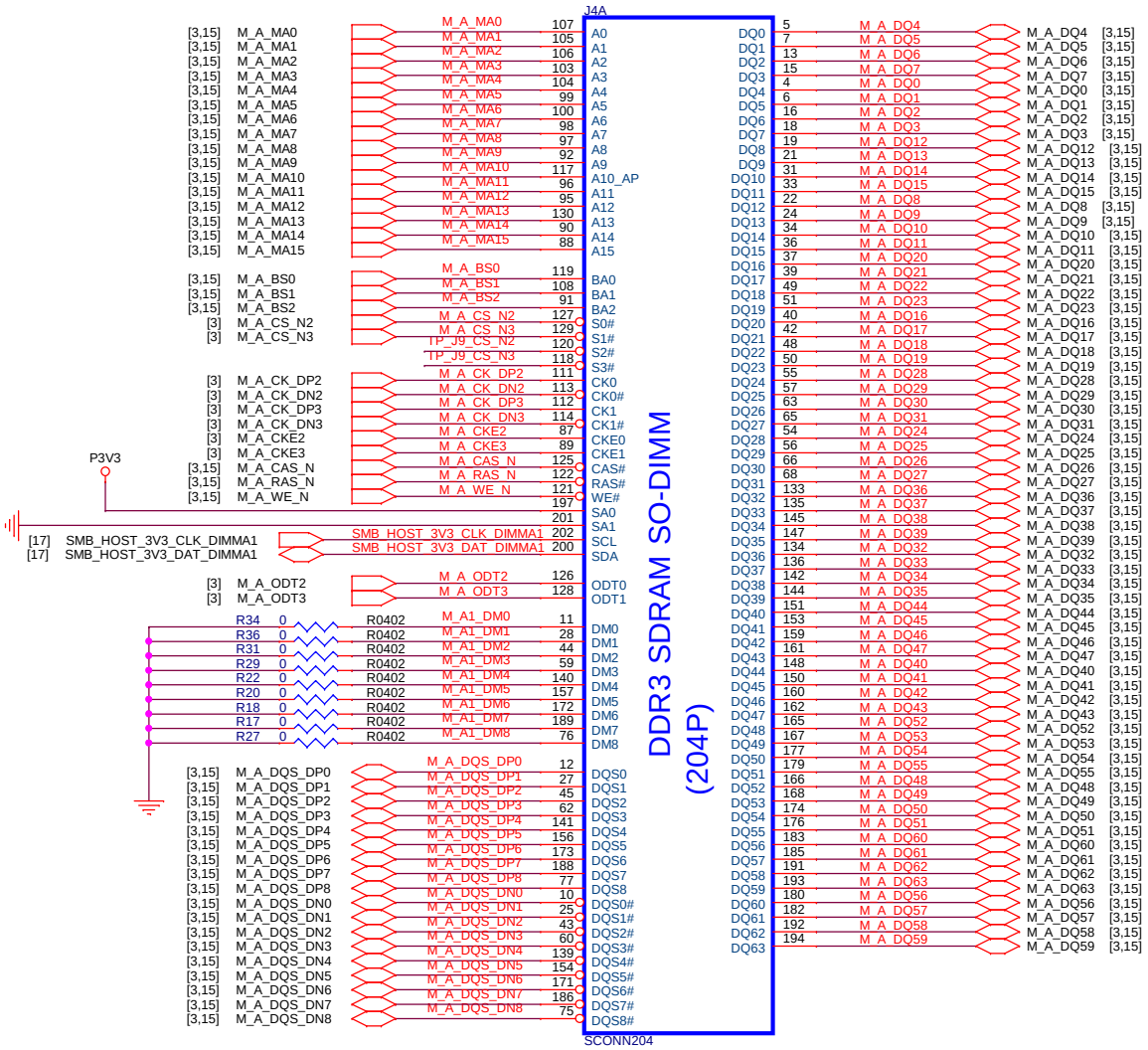
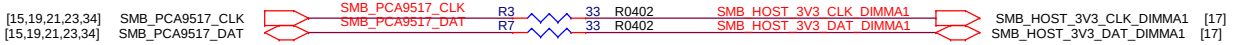
Quanta	Department CCBU	Designer	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>	Size B Date: Friday, February 06, 2015	Page Title BLANK	Sheet 16 of 54





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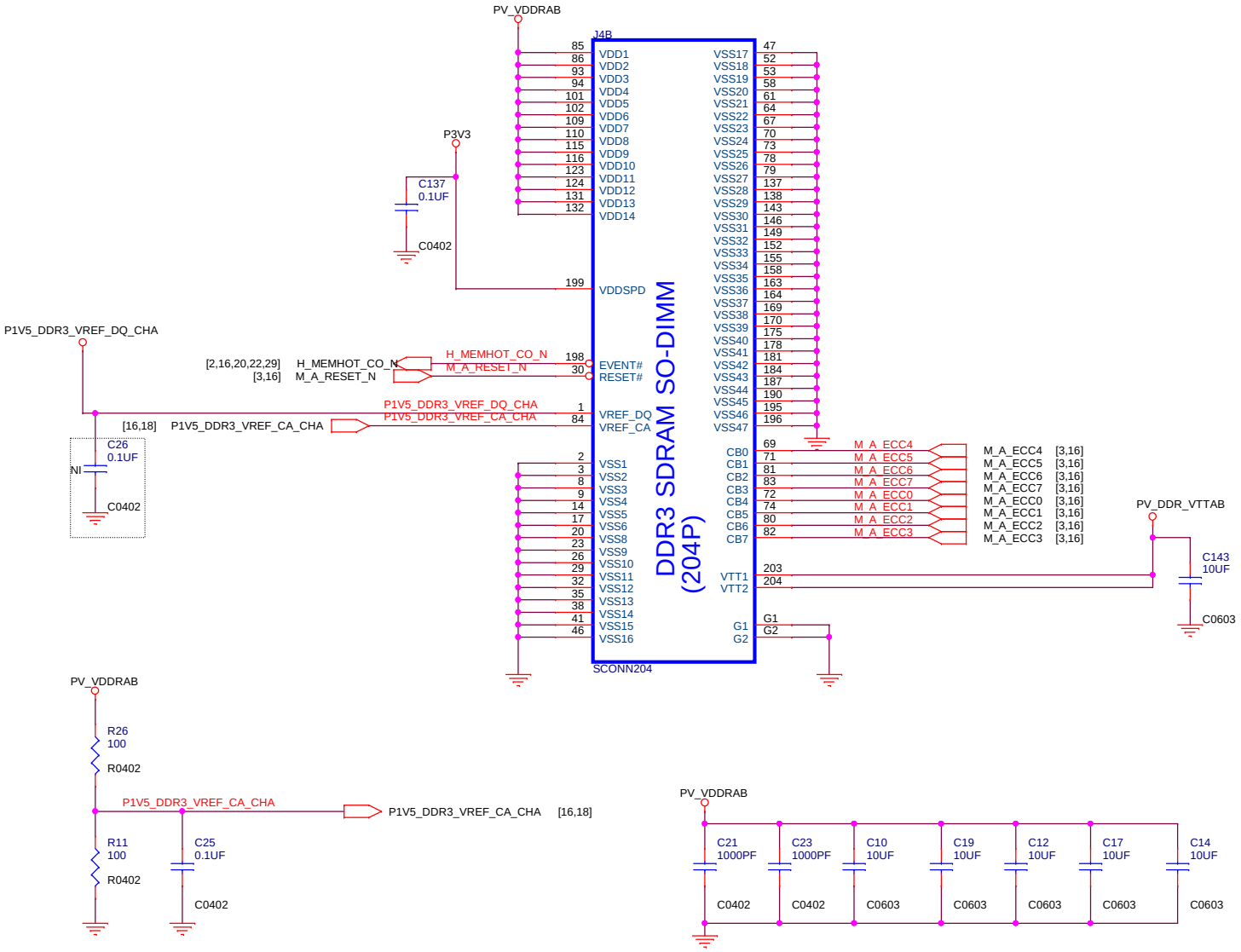
		Size B	Date: Friday, February 06, 2015	Sheet 17 of 54



DDR3_SODIMM_CHA1_2

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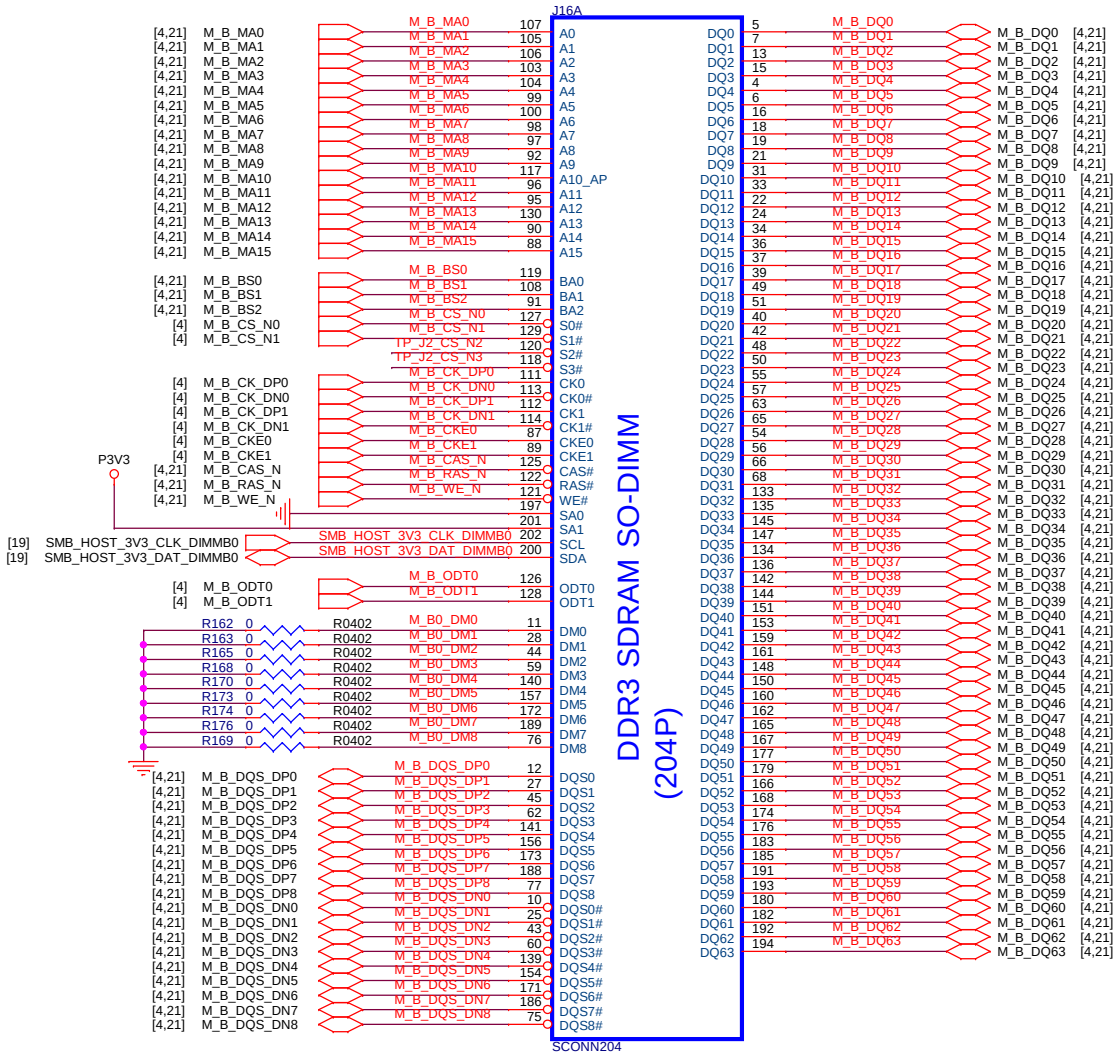
		Reviewer <Name>	Size B Date: Friday, February 06, 2015	Page Title BLANK	Sheet 18 of 54



[15,17,21,23,34] SMB_PCA9517_CLK
[15,17,21,23,34] SMB_PCA9517_DAT
SMB_PCA9517_CLK
SMB_PCA9517_DAT
R455 33 R0402 SMB_HOST_3V3_CLK_DIMMB0
R454 33 R0402 SMB_HOST_3V3_DAT_DIMMB0
SMB_HOST_3V3_CLK_DIMMB0 [19]
SMB_HOST_3V3_DAT_DIMMB0 [19]

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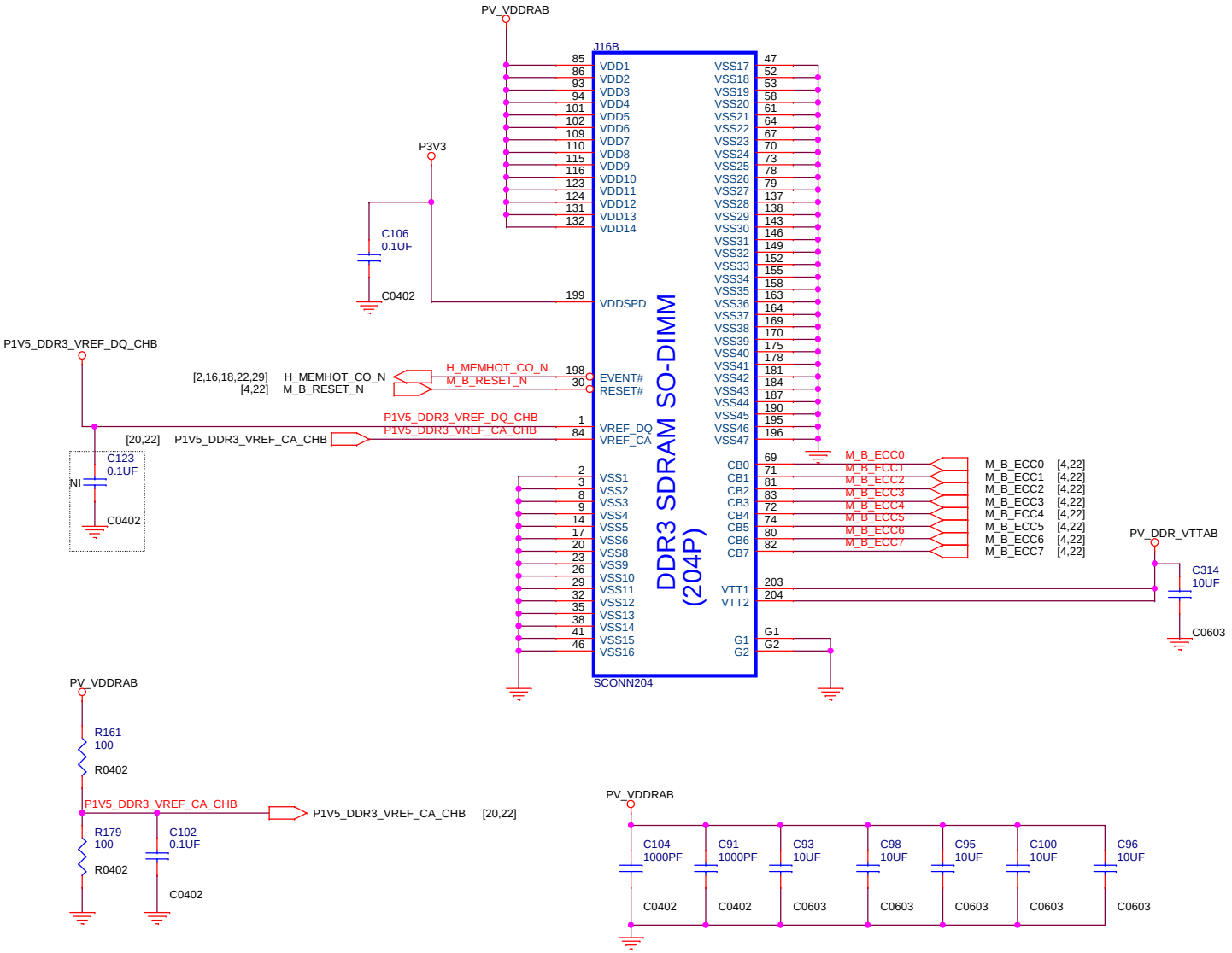
DDR3_SODIMM_CHB0_1

Quanta	Department CCBU	Designer	Project MF1	Doc Number <Doc> Rev 0.57
		Reviewer Chih-Ta Chen 92081366	Size B Date: Friday, February 06, 2015	Page Title DDR3_SODIMM_CHB0 Sheet 19 of 54



DDR3_SODIMM_CHB0_2

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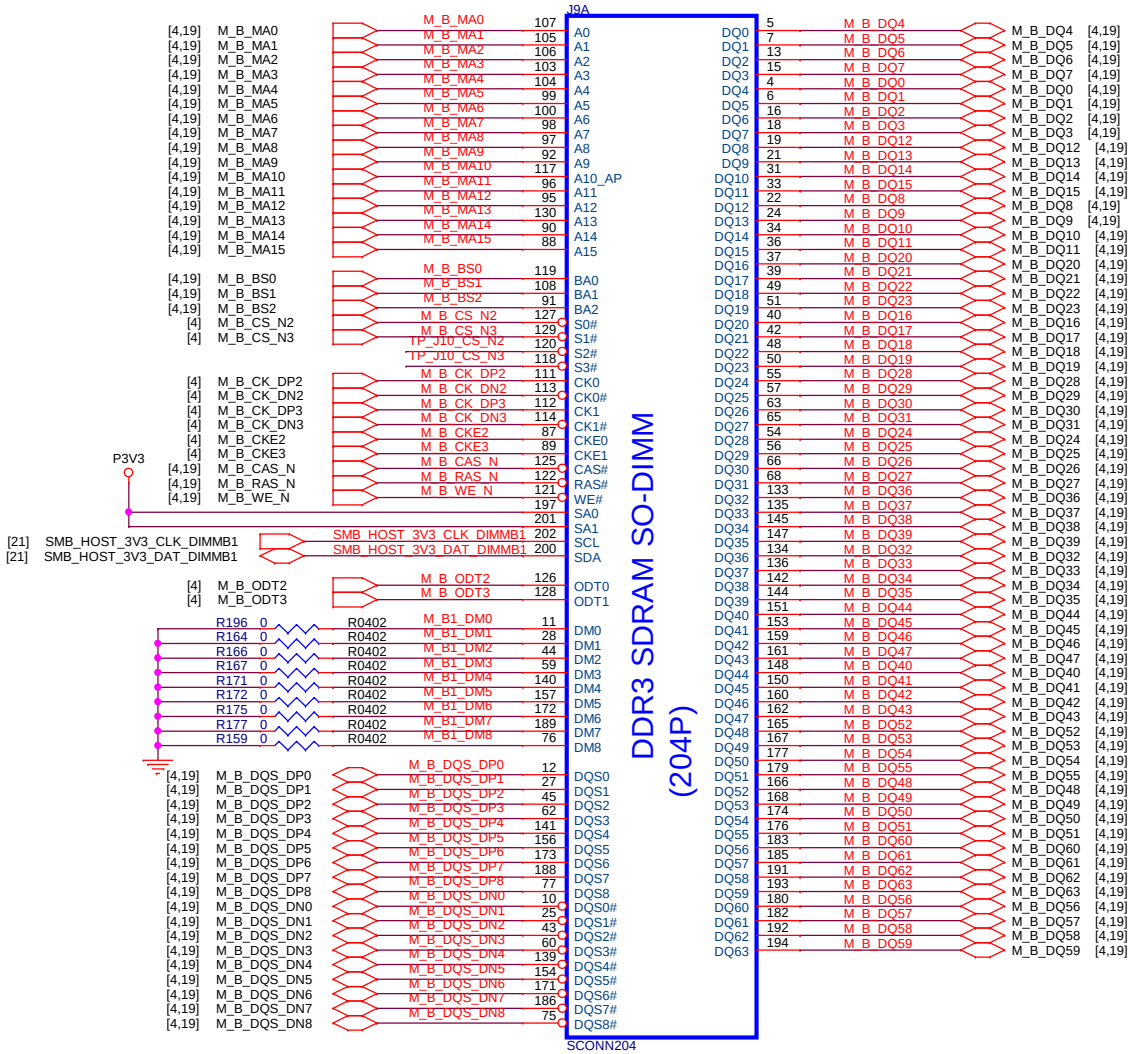

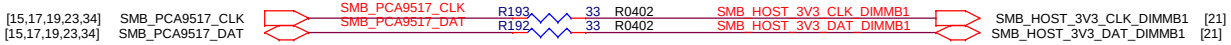

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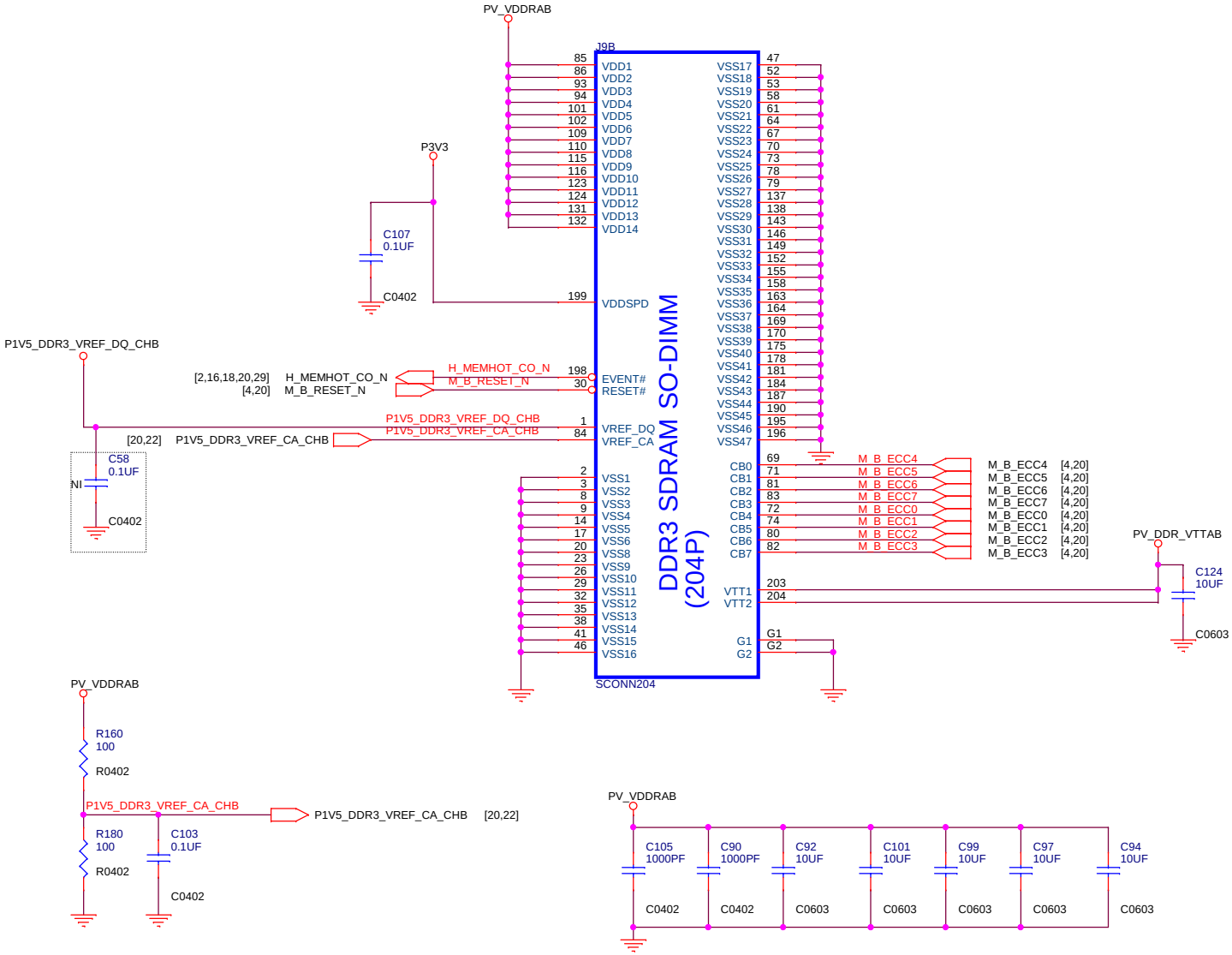
		Reviewer Chih-Ta Chen 92081366	Size B Date: Friday, February 06, 2015	Page Title DDR3_SODIMM_CHB1 Sheet 21 of 54



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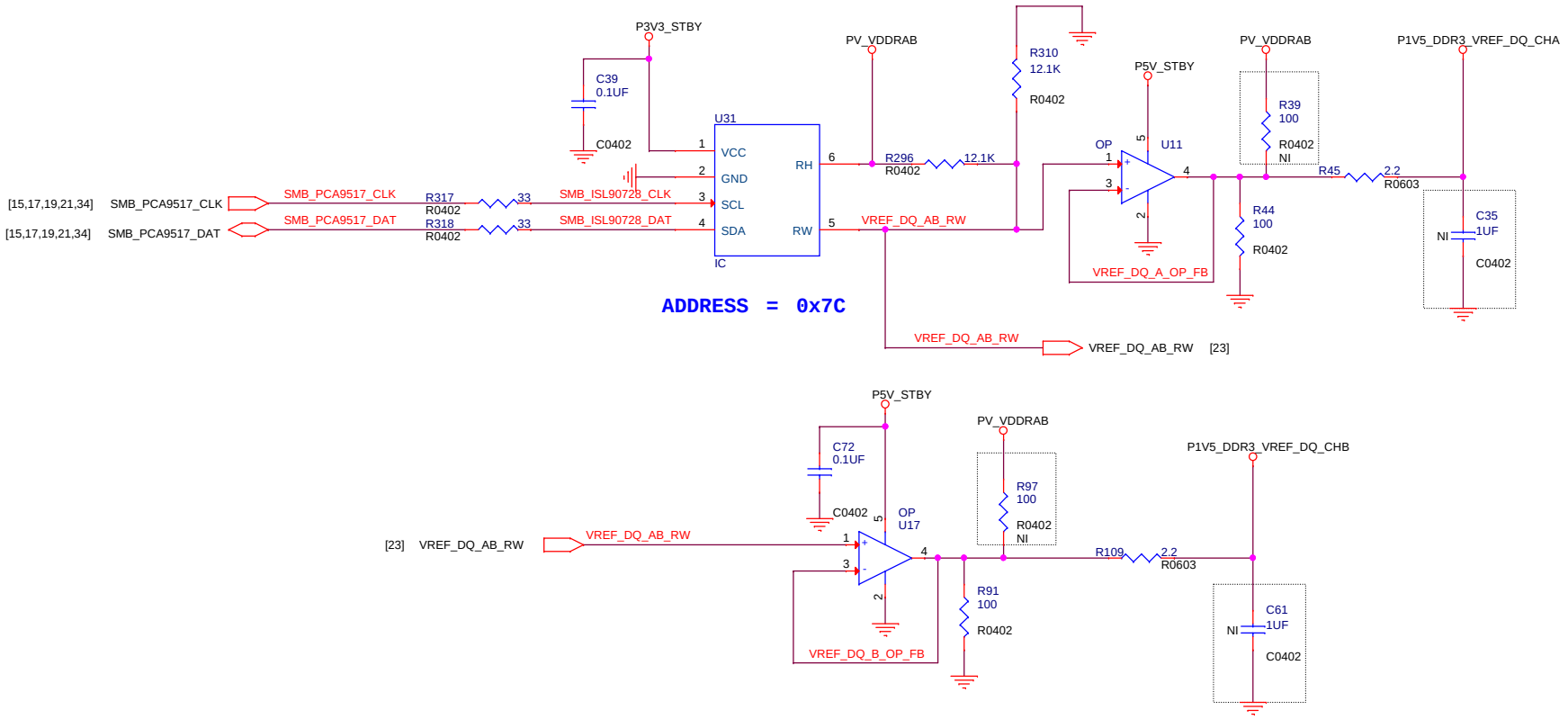

DIMM VREF

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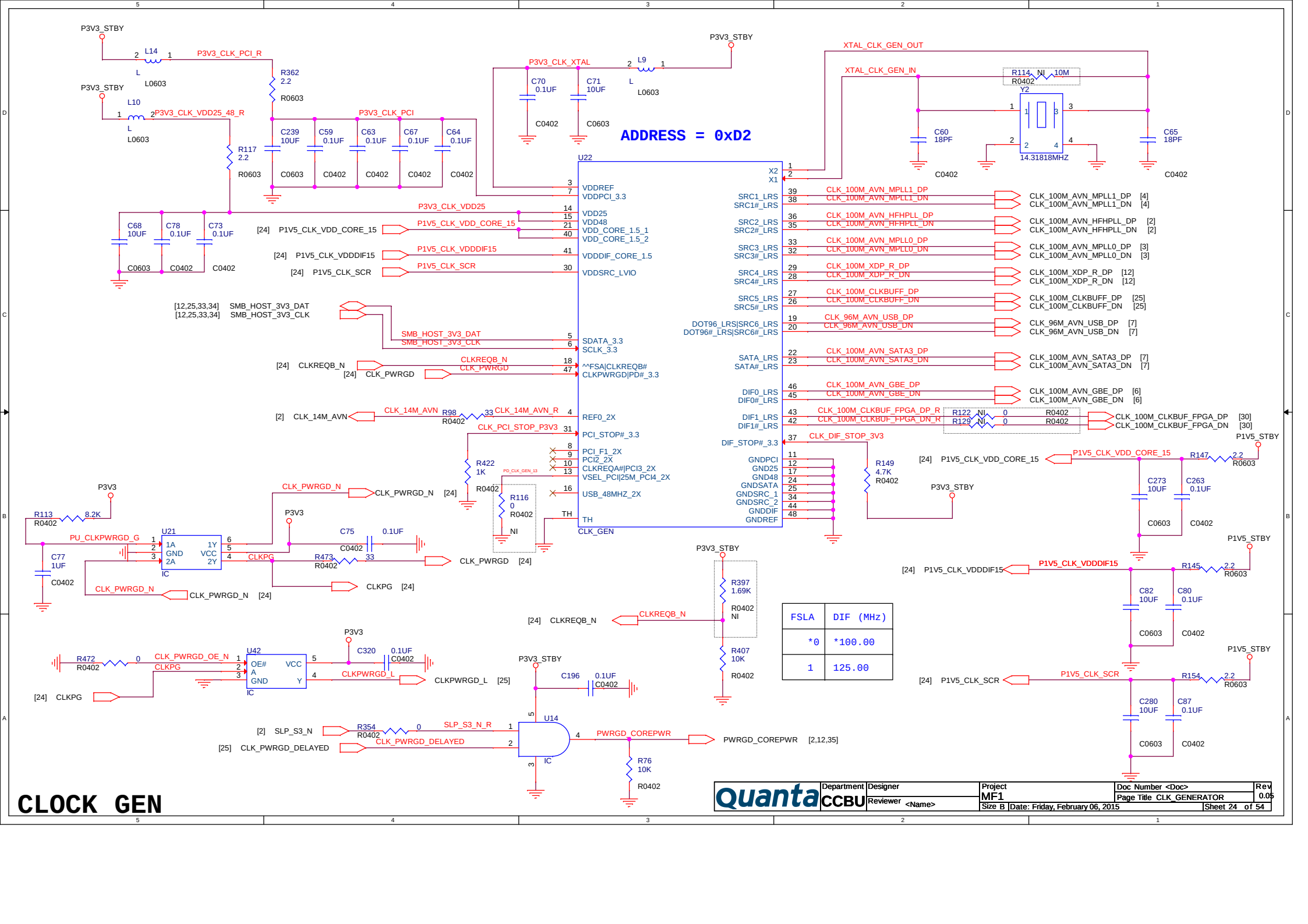
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P3V3_STBY
P3V3_CLK_PCI_R
P3V3_CLK_VDD25_48_R
P3V3_CLK_PCI
P3V3_CLK_XTAL
P3V3_CLK_VDD25
P1V5_CLK_VDD_CORE_15
P1V5_CLK_VDDDIF15
P1V5_CLK_SCR
SMB_HOST_3V3_DAT
SMB_HOST_3V3_CLK
CLKREQB_N
CLK_PWRGD
CLK_14M_AVN
CLK_14M_AVN_R
CLK_PCI_STOP_P3V3
CLK_DIF_STOP_3V3
XTAL_CLK_GEN_OUT
XTAL_CLK_GEN_IN
14.31818MHZ
CLK_100M_AVN_MPLL1_DP
CLK_100M_AVN_MPLL1_DN
CLK_100M_AVN_HFHPLL_DP
CLK_100M_AVN_HFHPLL_DN
CLK_100M_AVN_MPLL0_DP
CLK_100M_AVN_MPLL0_DN
CLK_100M_XDP_R_DP
CLK_100M_XDP_R_DN
CLK_100M_CLKBUFF_DP
CLK_100M_CLKBUFF_DN
CLK_96M_AVN_USB_DP
CLK_96M_AVN_USB_DN
CLK_100M_AVN_SATA3_DP
CLK_100M_AVN_SATA3_DN
CLK_100M_AVN_GBE_DP
CLK_100M_AVN_GBE_DN
CLK_100M_CLKBUF_FPGA_DP_R
CLK_100M_CLKBUF_FPGA_DN_R
CLK_100M_CLKBUF_FPGA_DP
CLK_100M_CLKBUF_FPGA_DN
PU_CLKPWRGD_G
CLK_PWRGD_N
CLKPG
CLK_PWRGD_OE_N
CLKPWRGD_L
SLP_S3_N
SLP_S3_N_R
CLK_PWRGD_DELAYED
PWRGD_COREPWR
FSLA
DIF (MHz)
*0
*100.00
1
125.00
CLOCK GEN
Quanta
Department CCBU
Designer
Reviewer <Name>
Project MF1
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Page Title CLK_GENERATOR
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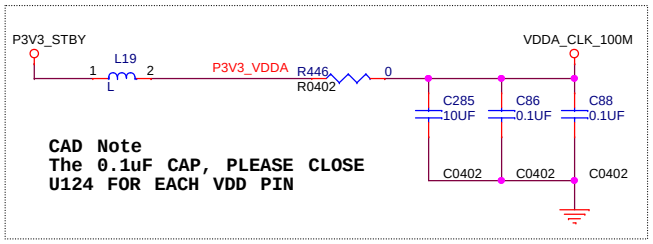
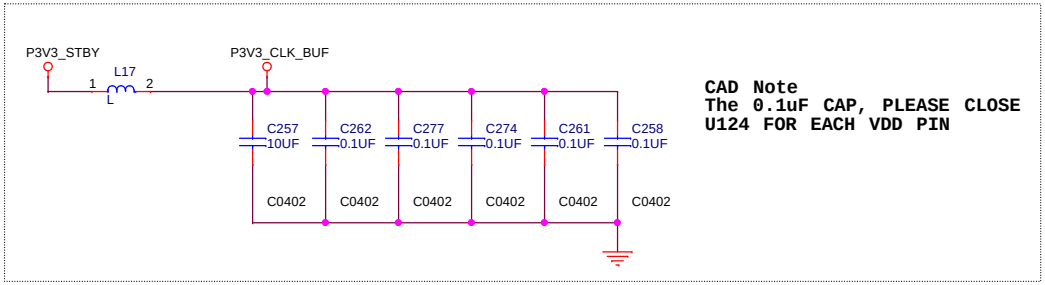
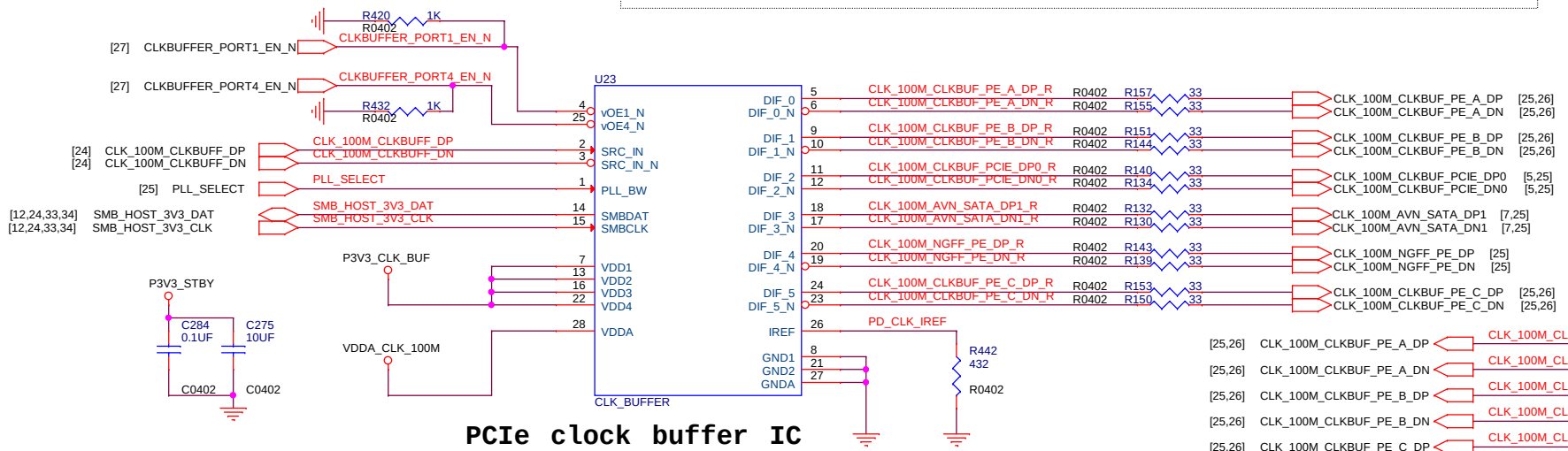






TO Gold finger

TO Gold finger

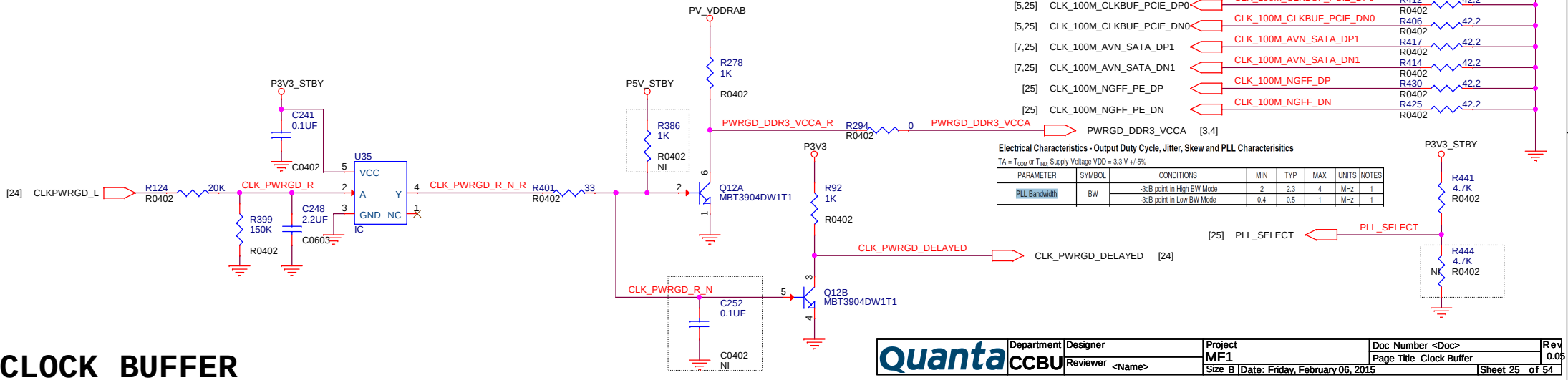
TO CPU

TO CPU

TO NGFF

TO Gold finger

PCIe clock buffer IC
SMB address: D4/D5



Electrical Characteristics - Output Duty Cycle, Jitter, Skew and PLL Characterisitics

TA = T_{COM} or T_{IND}, Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PLL Bandwidth	BW	-3dB point in High BW Mode	2	2.3	4	MHz	1
		-3dB point in Low BW Mode	0.4	0.5	1	MHz	1

CLOCK BUFFER

Quanta	Department CCBU	Designer	Project MF1	Doc Number <Doc> Rev 0.05
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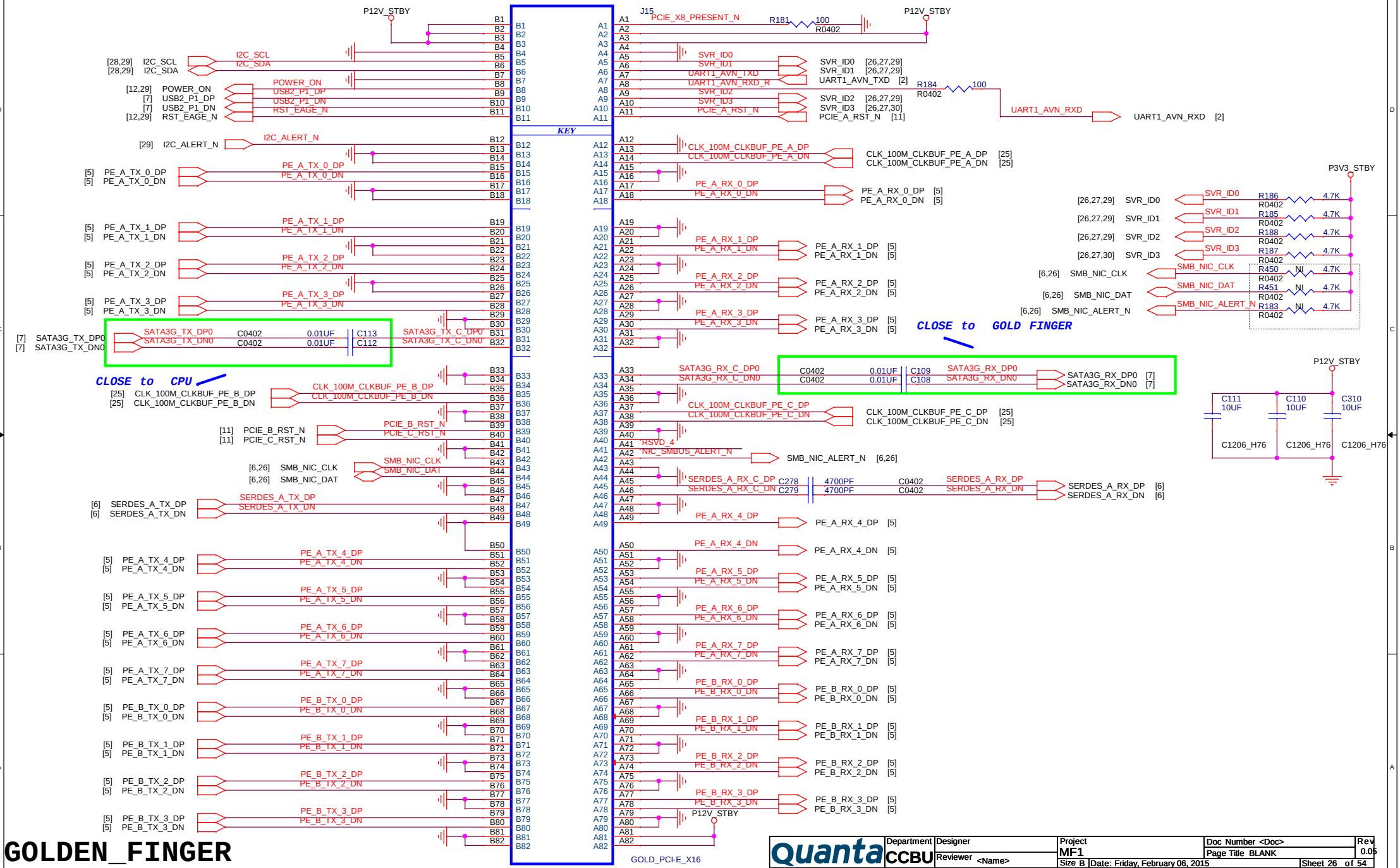
P12V_STBY
J15
PCIE_X8_PRESENT_N
R181
100
R0402
P12V_STBY
I2C_SCL
I2C_SDA
[28,29] I2C_SCL
[28,29] I2C_SDA
POWER_ON
USB2_P1_DP
USB2_P1_DN
RST_EAGE_N
[12,29] POWER_ON
[7] USB2_P1_DP
[7] USB2_P1_DN
[12,29] RST_EAGE_N
SVR_ID0
SVR_ID1
UART1_AVN_TXD
UART1_AVN_RXD_R
SVR_ID2
SVR_ID3
PCIE_A_RST_N
SVR_ID0 [26,27,29]
SVR_ID1 [26,27,29]
UART1_AVN_TXD [2]
SVR_ID2 [26,27,29]
SVR_ID3 [26,27,30]
PCIE_A_RST_N [11]
R184
100
R0402
UART1_AVN_RXD
UART1_AVN_RXD [2]
KEY
I2C_ALERT_N
[29] I2C_ALERT_N
CLK_100M_CLKBUF_PE_A_DP
CLK_100M_CLKBUF_PE_A_DN
CLK_100M_CLKBUF_PE_A_DP [25]
CLK_100M_CLKBUF_PE_A_DN [25]
PE_A_TX_0_DP
PE_A_TX_0_DN
[5] PE_A_TX_0_DP
[5] PE_A_TX_0_DN
PE_A_RX_0_DP
PE_A_RX_0_DN
PE_A_RX_0_DP [5]
PE_A_RX_0_DN [5]
P3V3_STBY
[26,27,29] SVR_ID0
[26,27,29] SVR_ID1
[26,27,29] SVR_ID2
[26,27,30] SVR_ID3
[6,26] SMB_NIC_CLK
[6,26] SMB_NIC_DAT
[6,26] SMB_NIC_ALERT_N
R186 4.7K
R185 4.7K
R188 4.7K
R187 4.7K
R450 NI 4.7K
R451 NI 4.7K
R183 NI 4.7K
R0402
PE_A_TX_1_DP
PE_A_TX_1_DN
[5] PE_A_TX_1_DP
[5] PE_A_TX_1_DN
PE_A_RX_1_DP
PE_A_RX_1_DN
PE_A_RX_1_DP [5]
PE_A_RX_1_DN [5]
PE_A_TX_2_DP
PE_A_TX_2_DN
[5] PE_A_TX_2_DP
[5] PE_A_TX_2_DN
PE_A_RX_2_DP
PE_A_RX_2_DN
PE_A_RX_2_DP [5]
PE_A_RX_2_DN [5]
PE_A_TX_3_DP
PE_A_TX_3_DN
[5] PE_A_TX_3_DP
[5] PE_A_TX_3_DN
PE_A_RX_3_DP
PE_A_RX_3_DN
PE_A_RX_3_DP [5]
PE_A_RX_3_DN [5]
CLOSE to GOLD FINGER
[7] SATA3G_TX_DP0
[7] SATA3G_TX_DN0
SATA3G_TX_DP0
SATA3G_TX_DN0
C0402 0.01UF C113
C0402 0.01UF C112
SATA3G_TX_C_DP0
SATA3G_TX_C_DN0
SATA3G_RX_C_DP0
SATA3G_RX_C_DN0
C0402 0.01UF C109
C0402 0.01UF C108
SATA3G_RX_DP0
SATA3G_RX_DN0
SATA3G_RX_DP0 [7]
SATA3G_RX_DN0 [7]
P12V_STBY
C111 10UF
C110 10UF
C310 10UF
C1206_H76
CLOSE to CPU
[25] CLK_100M_CLKBUF_PE_B_DP
[25] CLK_100M_CLKBUF_PE_B_DN
CLK_100M_CLKBUF_PE_B_DP
CLK_100M_CLKBUF_PE_B_DN
CLK_100M_CLKBUF_PE_C_DP
CLK_100M_CLKBUF_PE_C_DN
CLK_100M_CLKBUF_PE_C_DP [25]
CLK_100M_CLKBUF_PE_C_DN [25]
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[11] PCIE_C_RST_N
PCIE_B_RST_N
PCIE_C_RST_N
RSVD_4
NIC_SMBUS_ALERT_N
SMB_NIC_ALERT_N [6,26]
[6,26] SMB_NIC_CLK
[6,26] SMB_NIC_DAT
SMB_NIC_CLK
SMB_NIC_DAT
SERDES_A_RX_C_DP
SERDES_A_RX_C_DN
C278 4700PF C0402 SERDES_A_RX_DP
C279 4700PF C0402 SERDES_A_RX_DN
SERDES_A_RX_DP [6]
SERDES_A_RX_DN [6]
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[6] SERDES_A_TX_DN
SERDES_A_TX_DP
SERDES_A_TX_DN
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PE_A_RX_4_DN
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PE_A_RX_4_DN [5]
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PE_A_RX_6_DN
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PE_B_TX_3_DN
[5] PE_B_TX_3_DP
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P12V_STBY
GOLD_PCI-E_X16
GOLDEN_FINGER
Quanta
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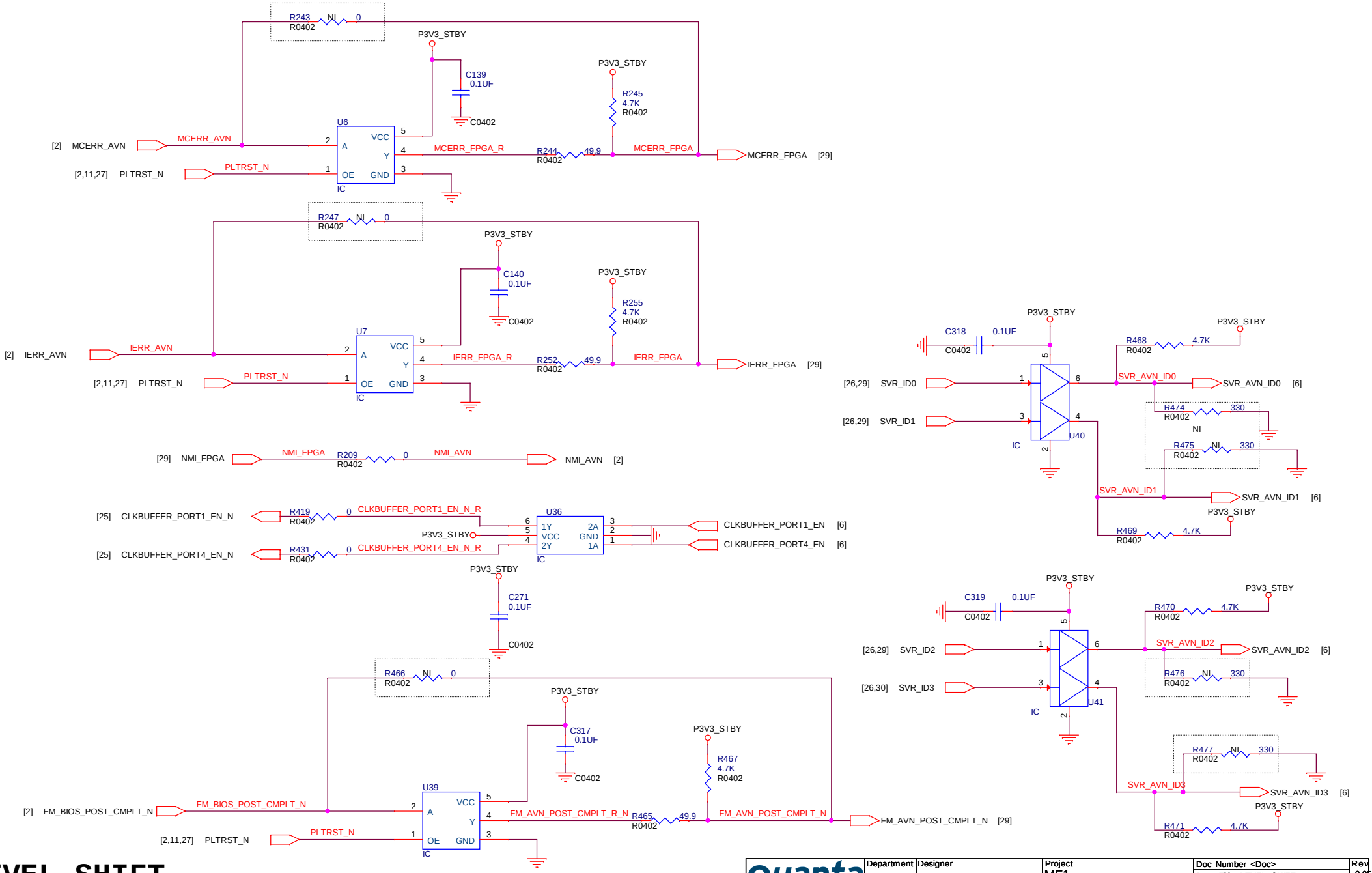

LEVEL_SHIFT

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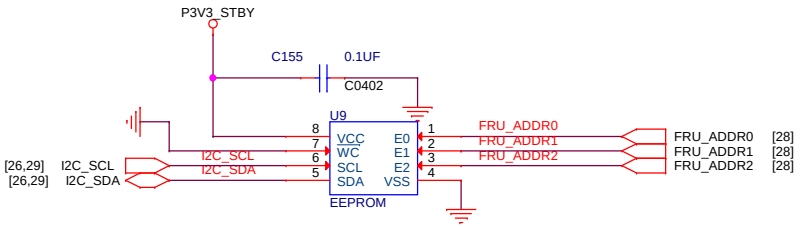
SMBus (8-bit) Address:0xA2

FRU



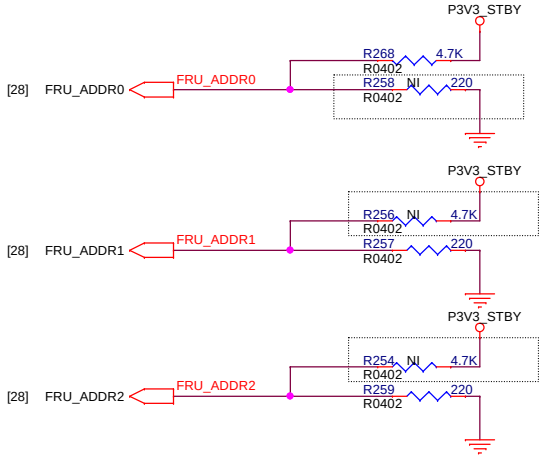


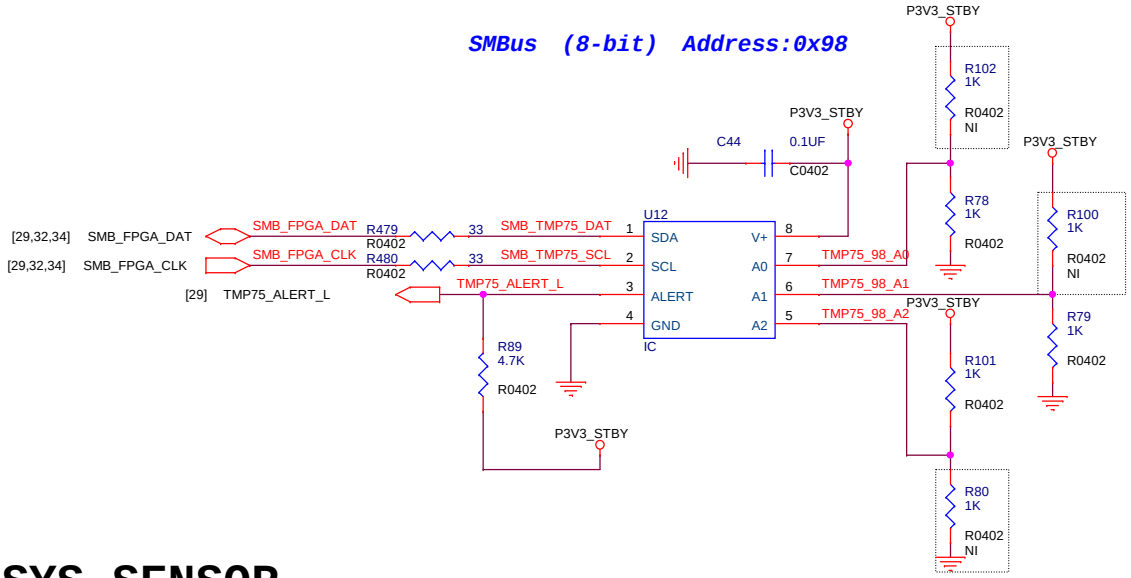
Table 2. Device Select Code

	Device Type Identifier[1]				Chip Enable Address[2]			$\overline{RW}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select Code	1	0	1	0	E2	E1	E0	$\overline{RW}$

Note: 1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.

FRU address

SMBus (8-bit) Address:0x98



A2	A1	A0	SLAVE ADDRESS
0	0	0	1001000
0	0	1	1001001
0	1	0	1001010
0	1	1	1001011
1	0	0	1001100
1	0	1	1001101
1	1	0	1001110
1	1	1	1001111

Table 12. Address Pins and Slave Addresses for the TMP75

SYS_SENSOR

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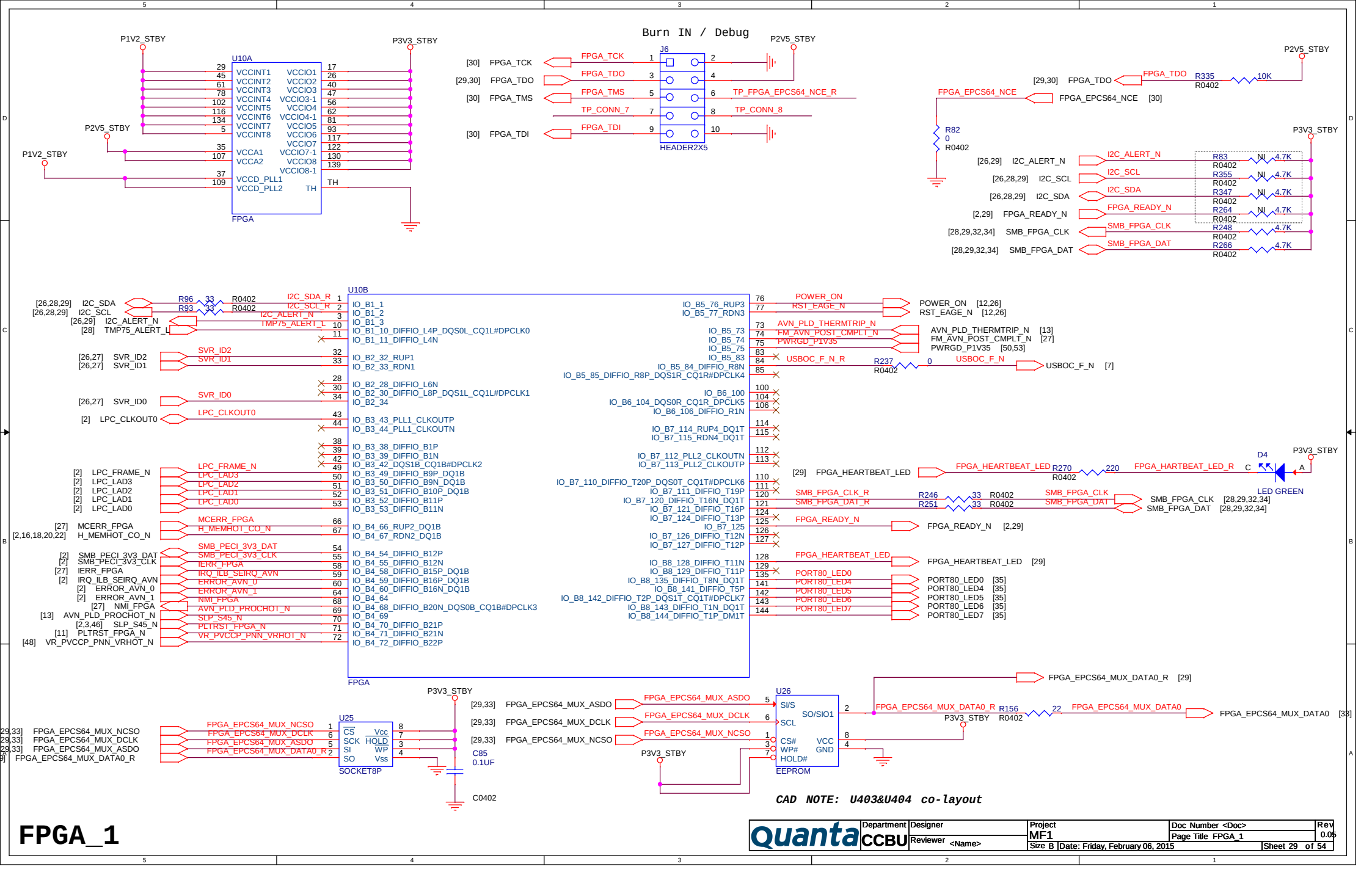

FPGA_1

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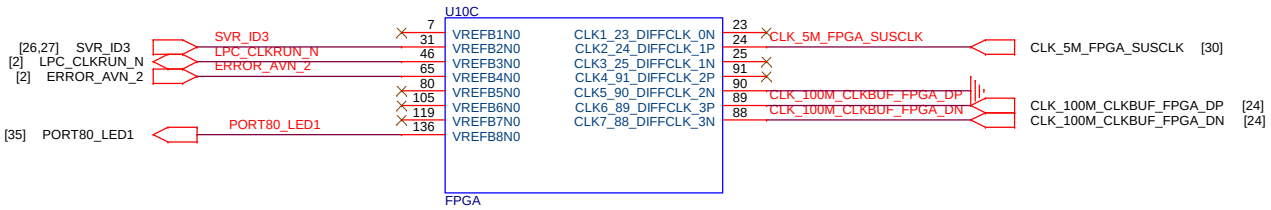
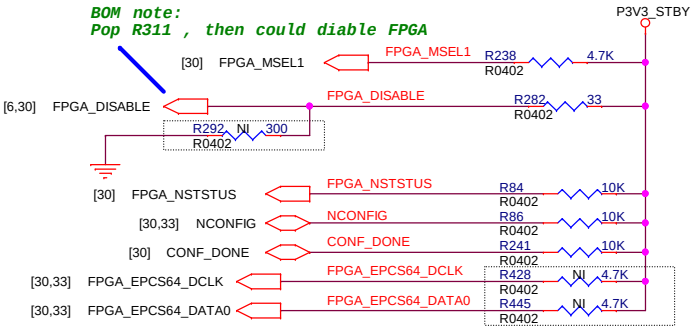
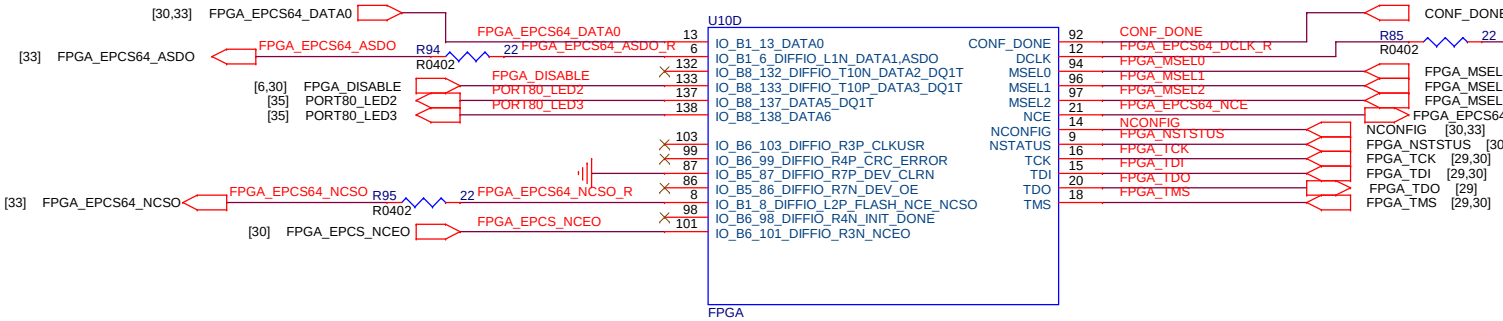
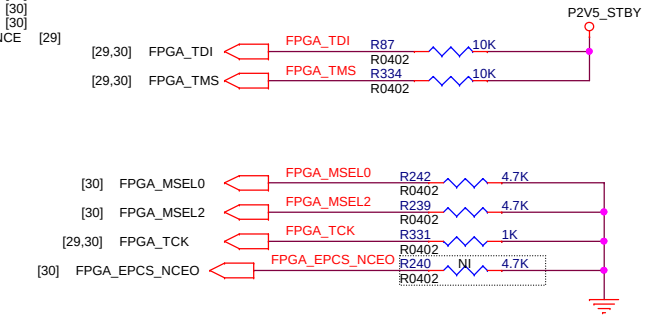
				Page Title FPGA_1	



BOM note:
Pop R311 , then could diable FPGA







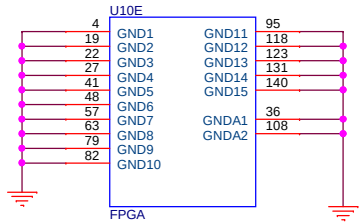
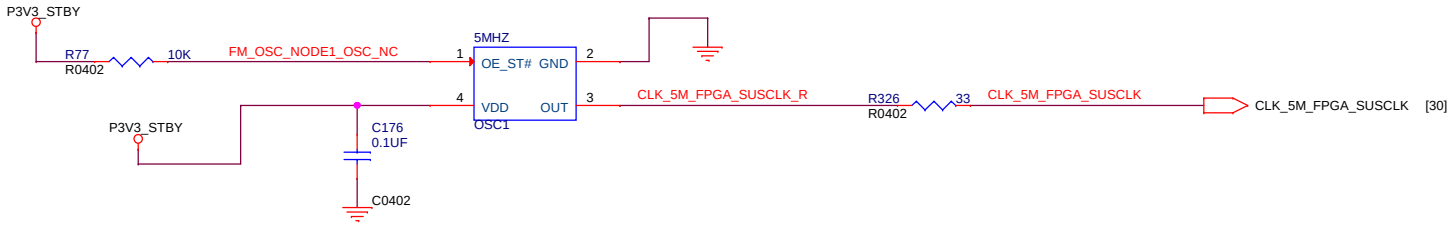


Table 8–5. Configuration Schemes for Cyclone IV E Devices

Configuration Scheme	MSEL3	MSEL2	MSEL1	MSEL0	POR Delay	Configuration Voltage Standard (V) *(1)*
AS	1	1	0	1	Fast	3.3
	0	1	0	0	Fast	3.0, 2.5
	0	0	1	0	Standard	3.3
	0	0	1	1	Standard	3.0, 2.5



FPGA_2

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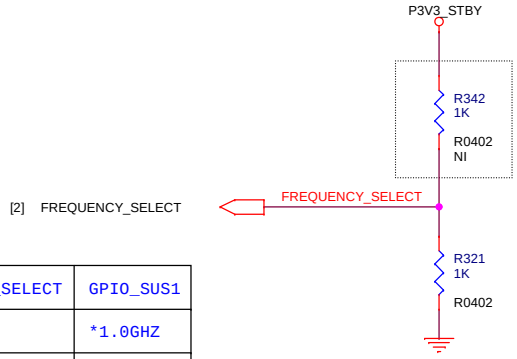

FREQUENCY_SELECT	GPIO_SUS1
*0	*1.0GHZ
1	2.5GHZ

CPU_LAN_FREQUENCY_SWITCH

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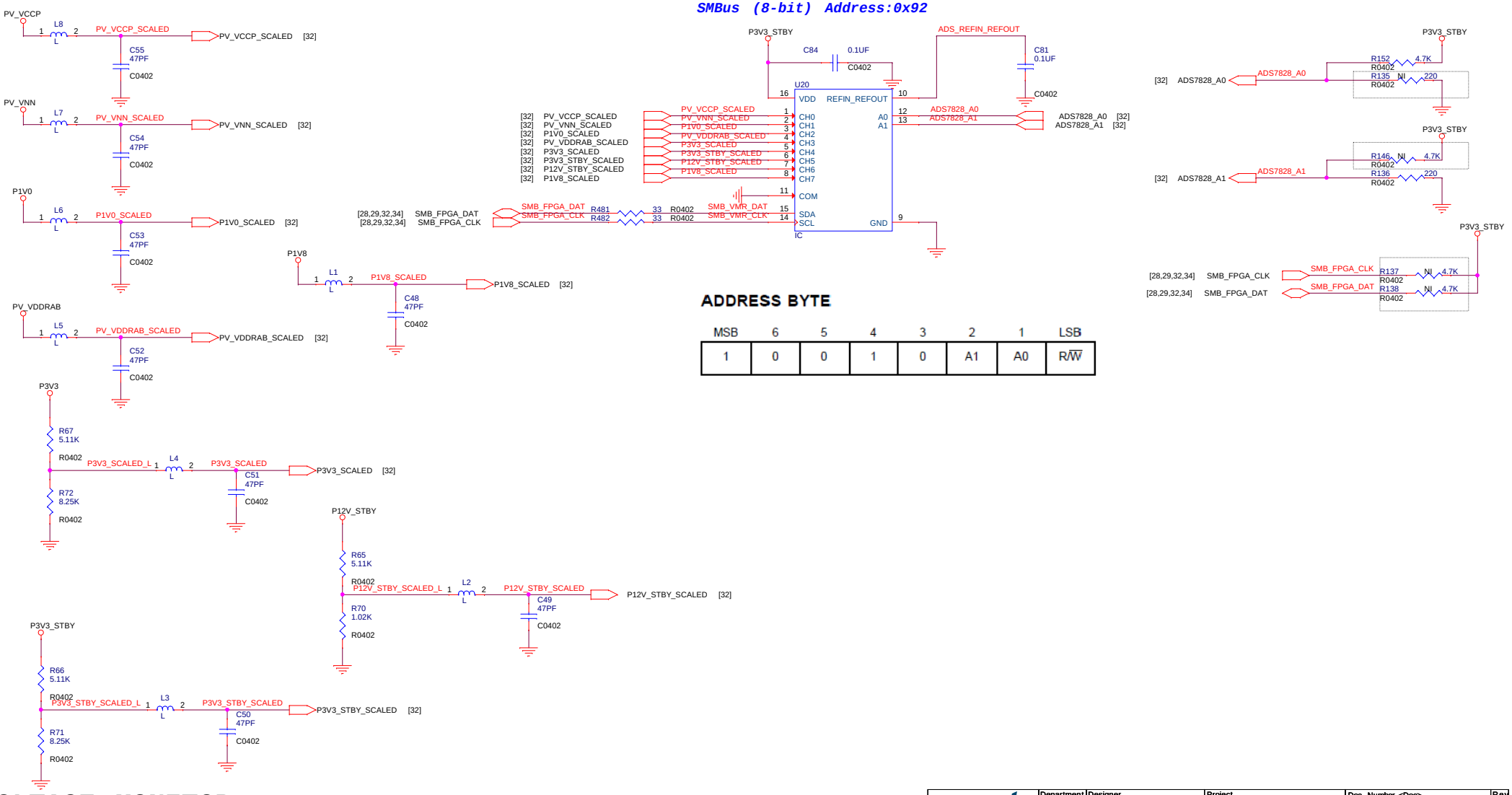

ADDRESS BYTE

MSB	6	5	4	3	2	1	LSB
1	0	0	1	0	A1	A0	R/$\overline{W}$

VOLTAGE MONITOR

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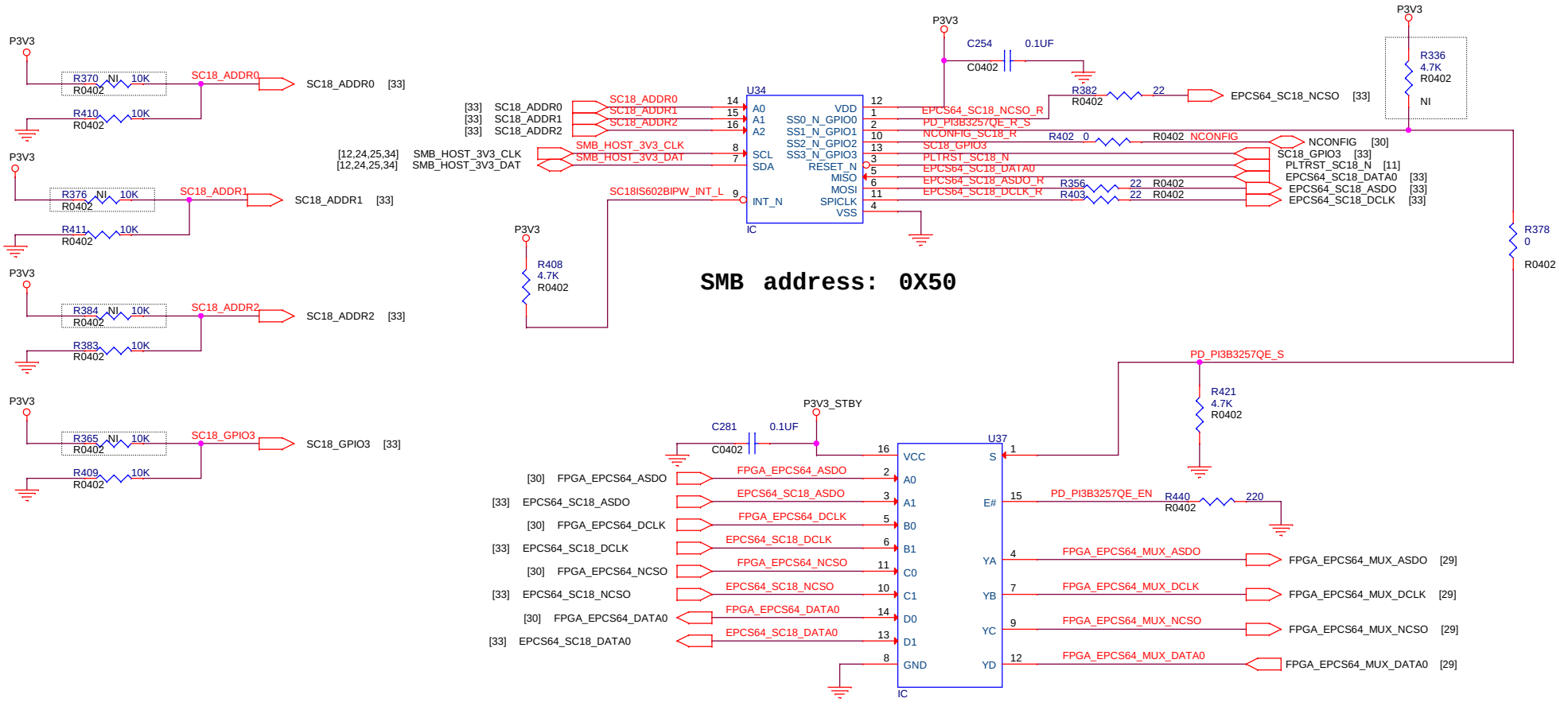

Truth Table[1]

$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

Note:
1. H = High Voltage Level, L = Low Voltage Level

Pin Description

Pin Name	Description
IAn-IDn	Data Inputs
S	Select Inputs
$\overline{E}$	Enable
YA-YD	Data Outputs
GND	Ground
Vcc	Power
NC	No Connect

I2C-BUS TO SPI BRIDGE

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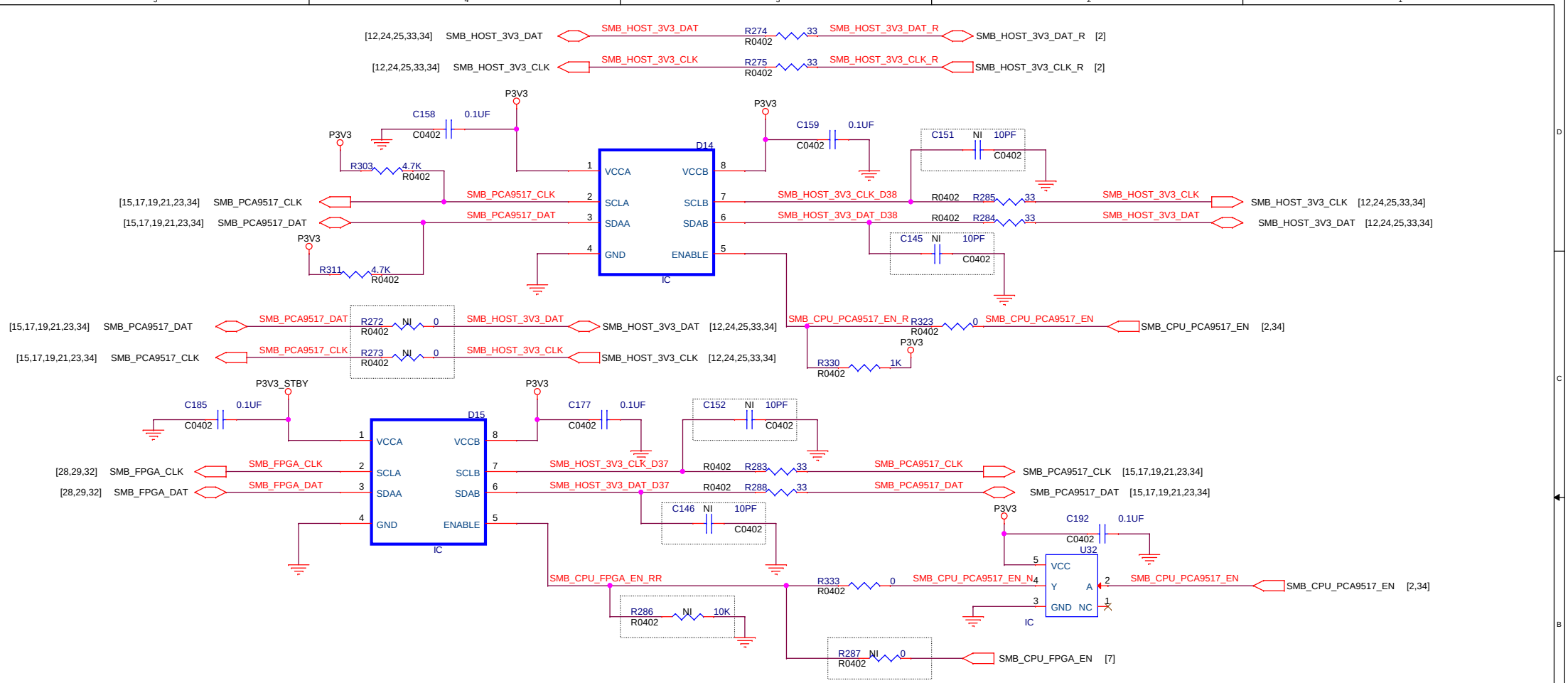

SMBUS ISOLATOR

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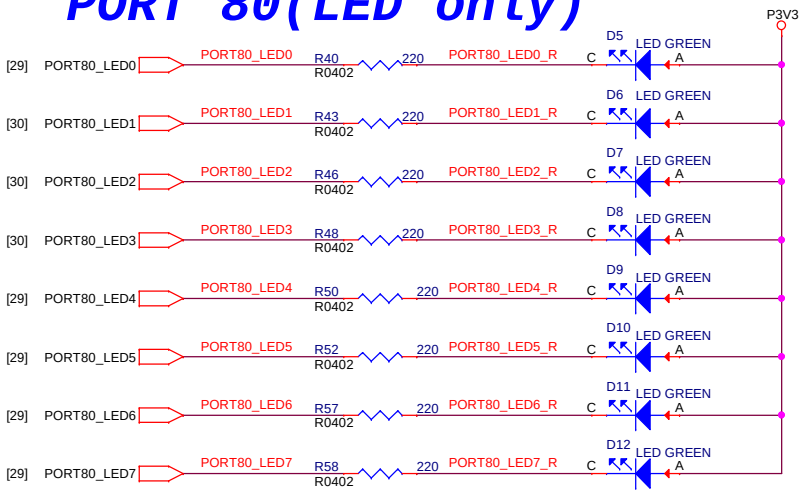
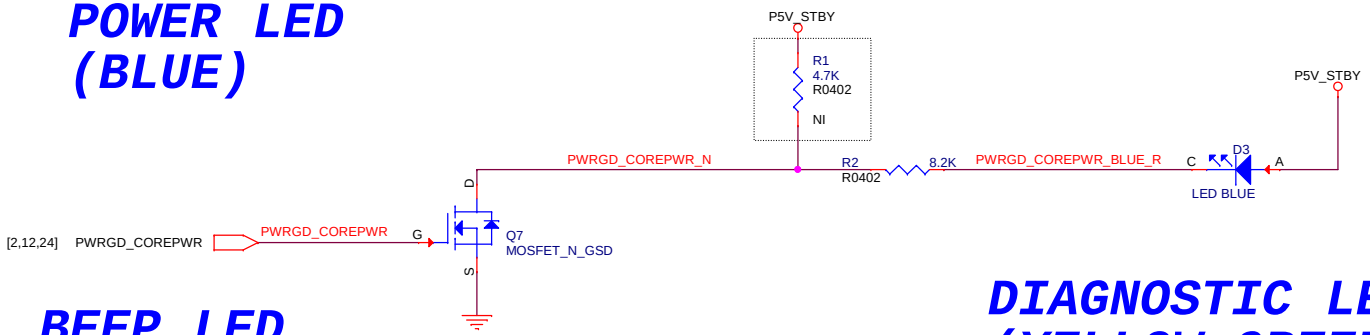
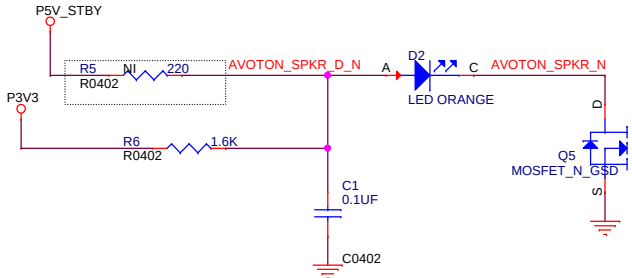
PORT 80(LED only)



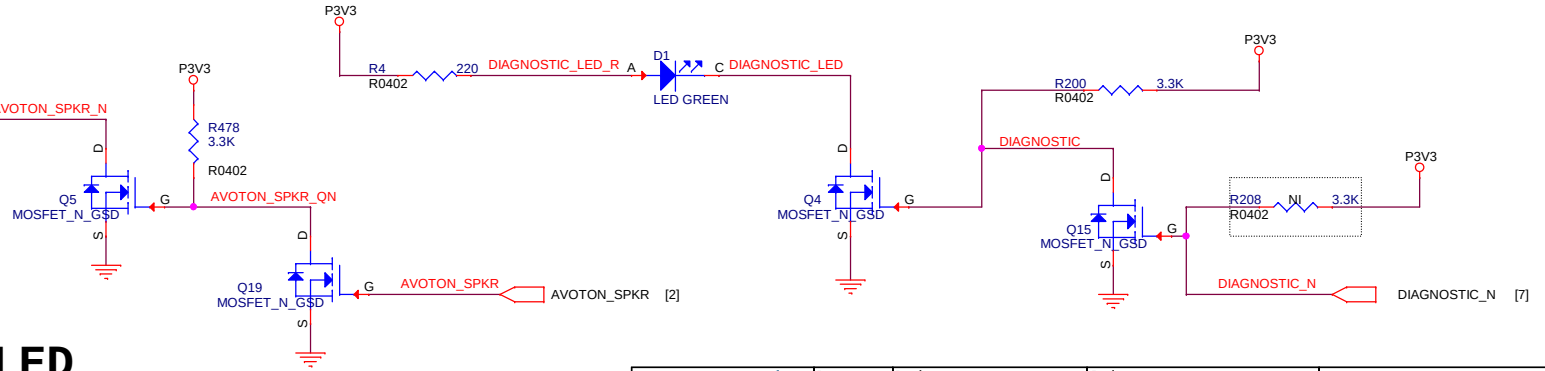
POWER LED (BLUE)



BEEP LED (Orange)



DIAGNOSTIC LED (YELLOW-GREEN)



PWR/ BEEP/ PORT 80 LED

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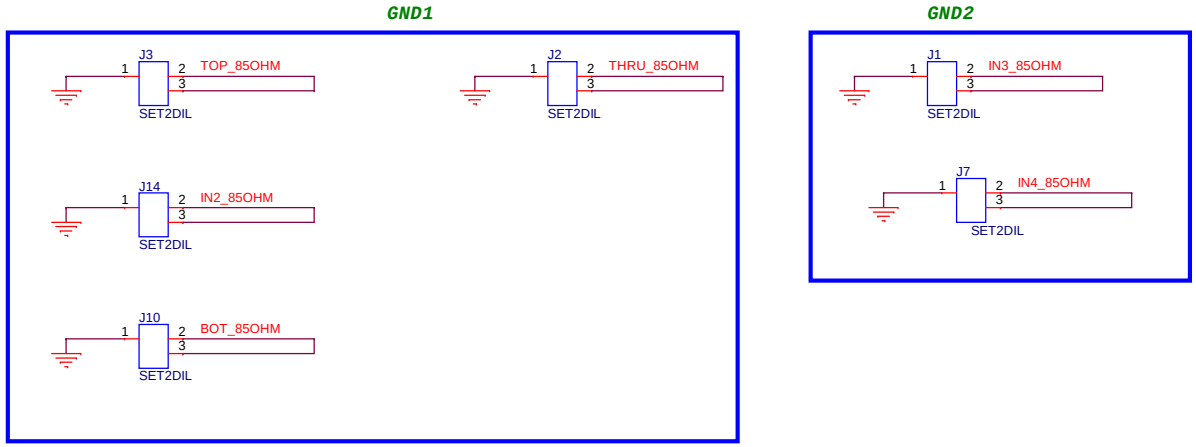
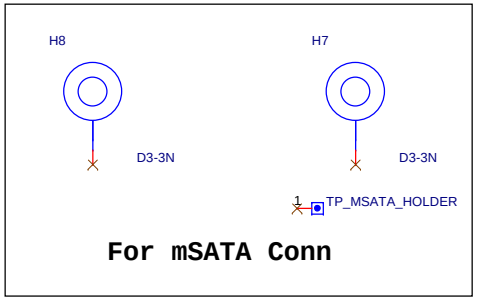
SET2DEL



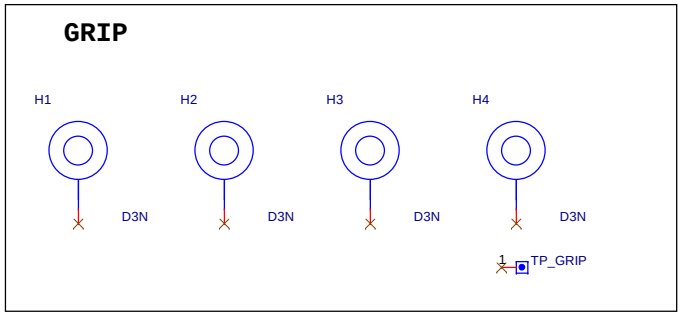
Screw Hole

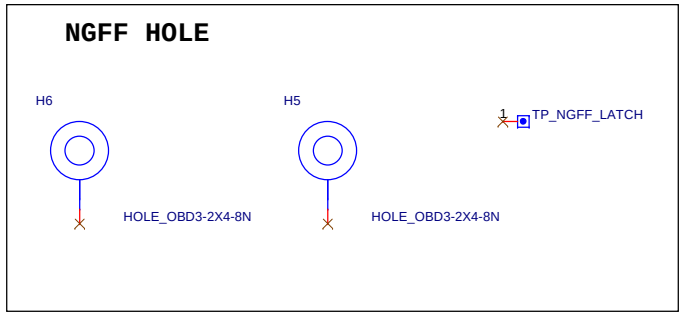


TP_HEAT_SINK1

TP_SCREW_1

TP_SCREW_2





SCREW/TP

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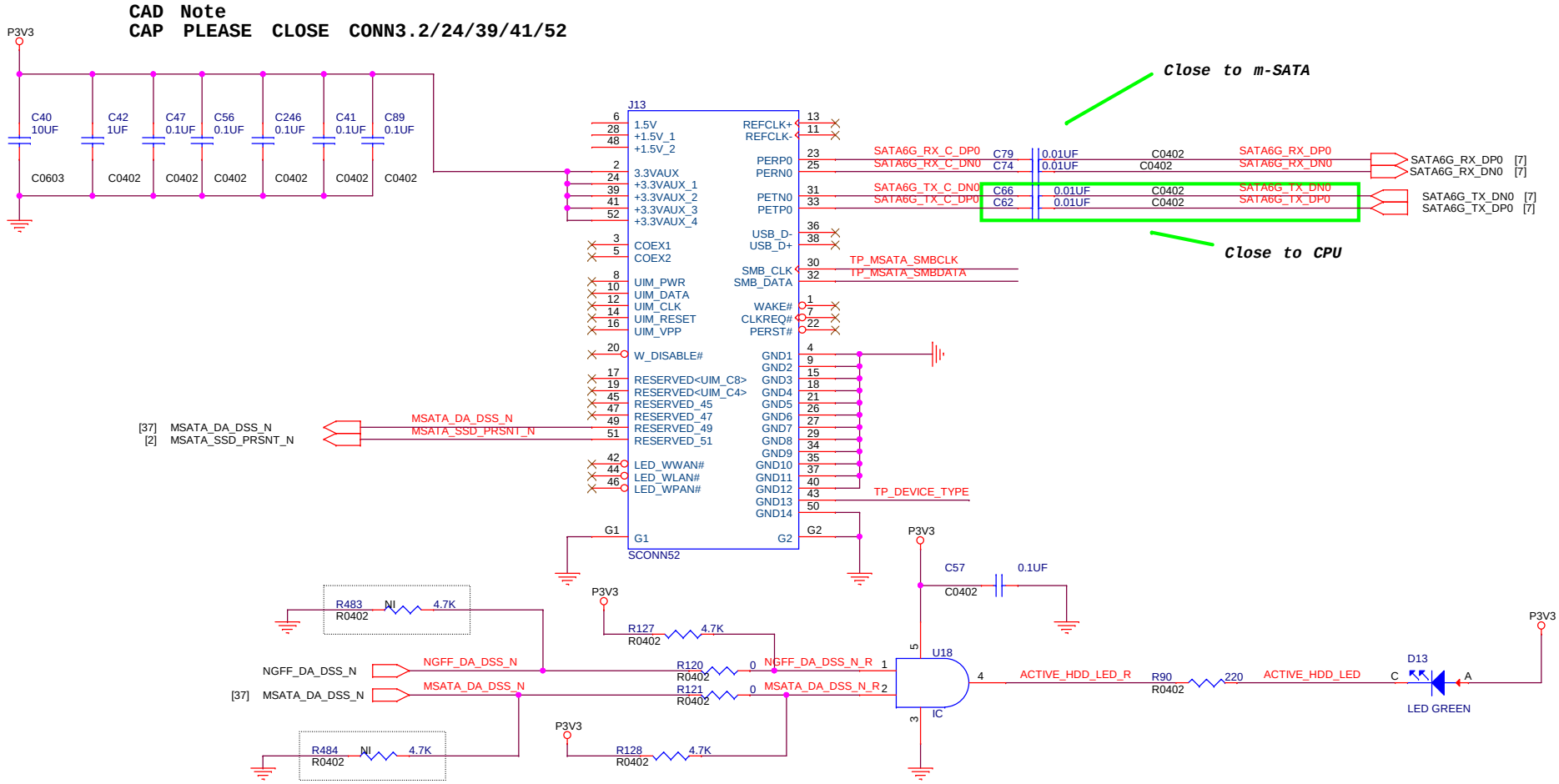

mSATA CONN

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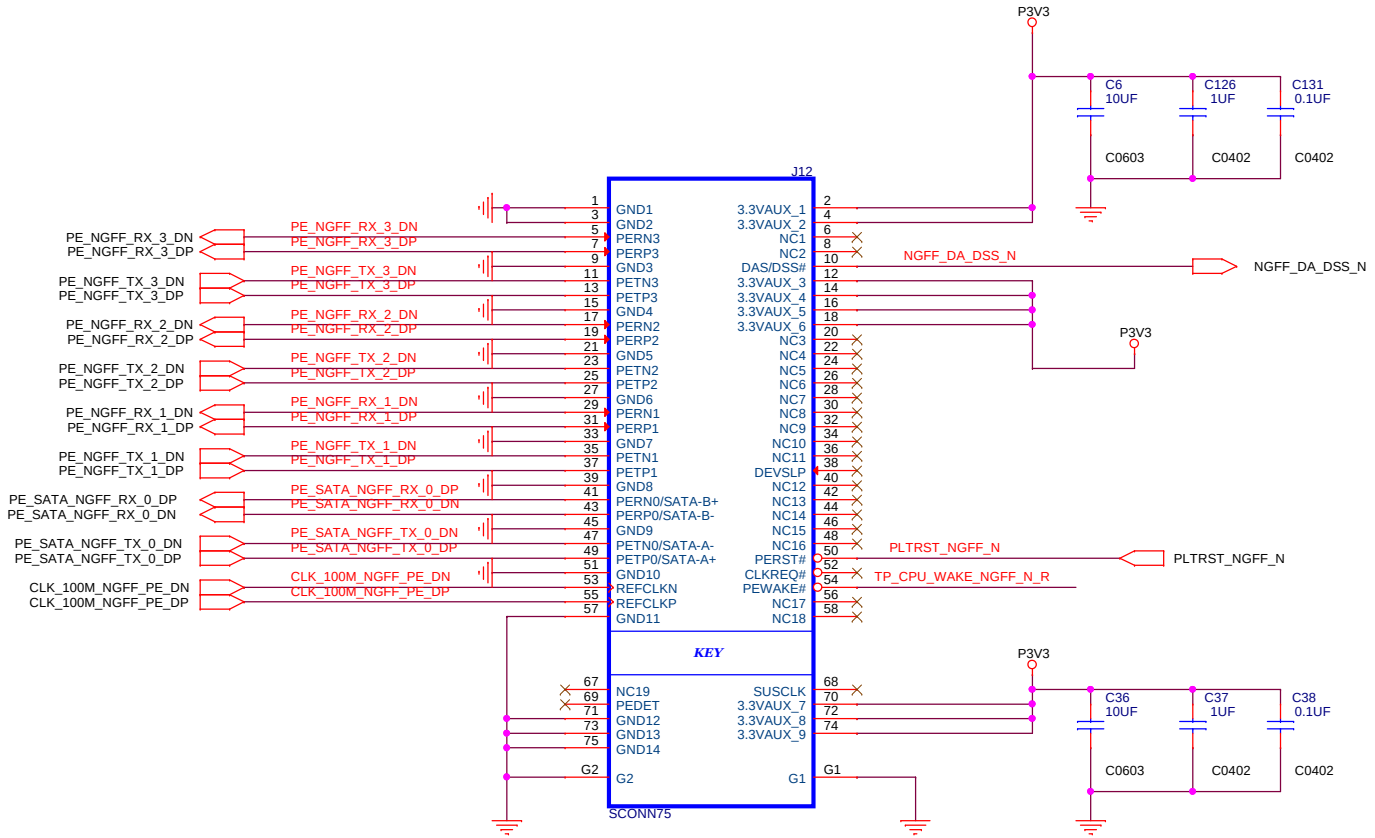

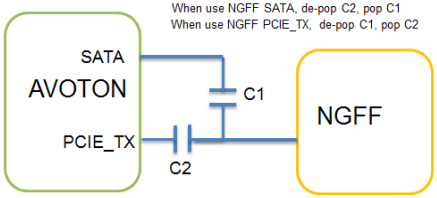

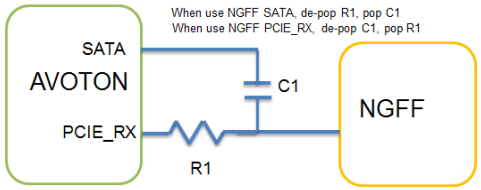

NGFF PCIEx4

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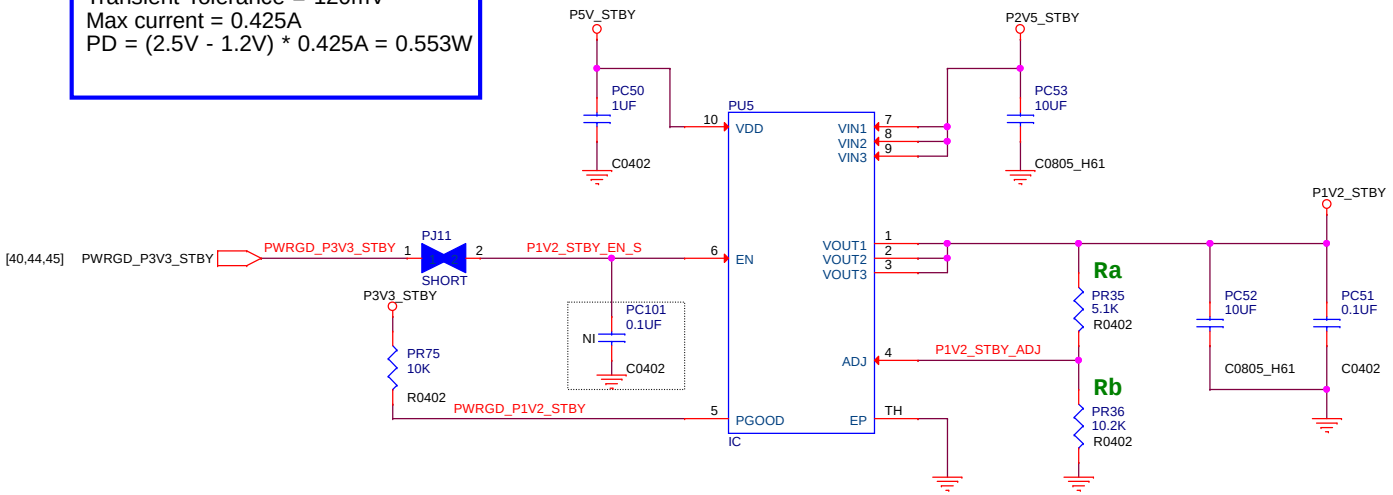
Output Voltage = 1.2V+/-5%
Output Ripple & Noise < 30mV
Transient Tolerance = 120mV
Max current = 0.425A
PD = (2.5V - 1.2V) * 0.425A = 0.553W



Vnom=0.8(1+Ra/Rb)=1.2 V

P1V2_STBY

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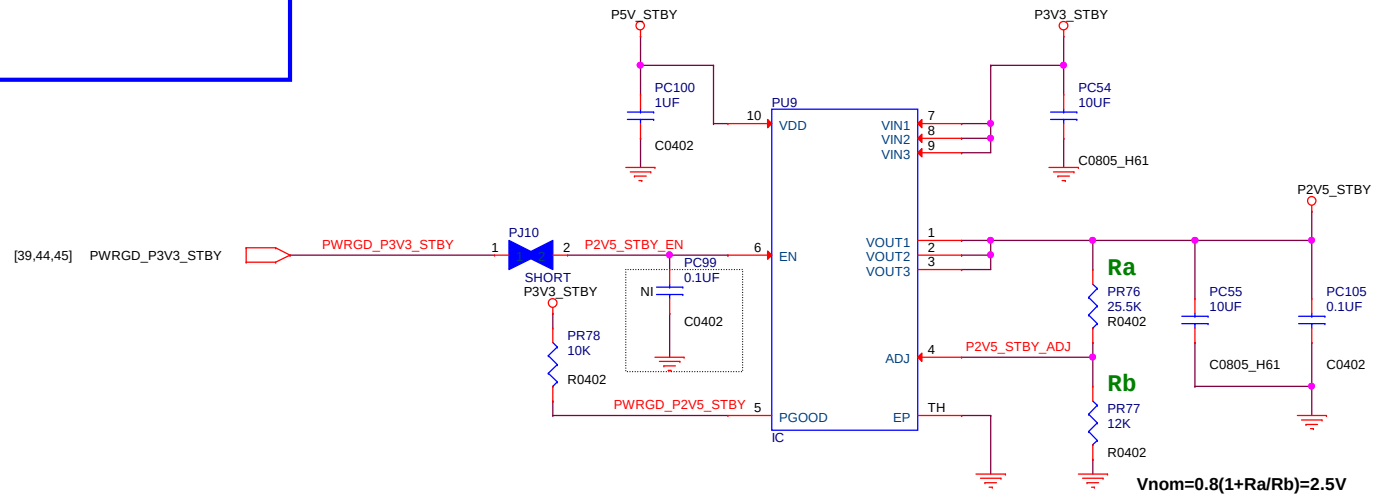
Output Voltage = 2.5V+/-5%
Output Ripple & Noise < 30mV
Transient Tolerance = 250mV
Max current = 0.525A
PD = (3.3V - 2.5V) * 0.525A = 0.42W



P2V5_STBY

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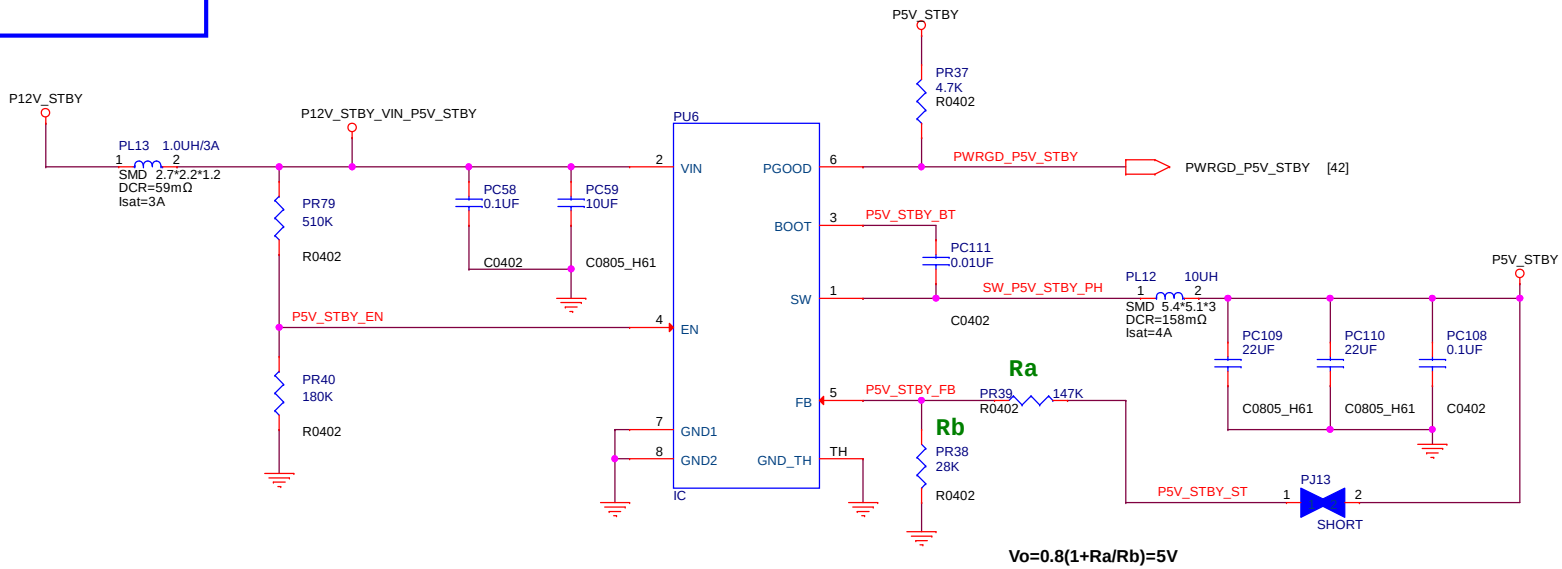
Design specification

Output Voltage = 5V± 5 %
Output Ripple & Noise < 50mV
Transient Tolerance = 500mV
TDC = 0.5A
Max current = 0.7A
Over-Current Protection(IC Rating) = 2.6A
Current Step = 0.2A
Slew Rate = 2.5A/us
Work frequency = 800KHZ
Efficiency > 85% @TDC



P5V_STBY

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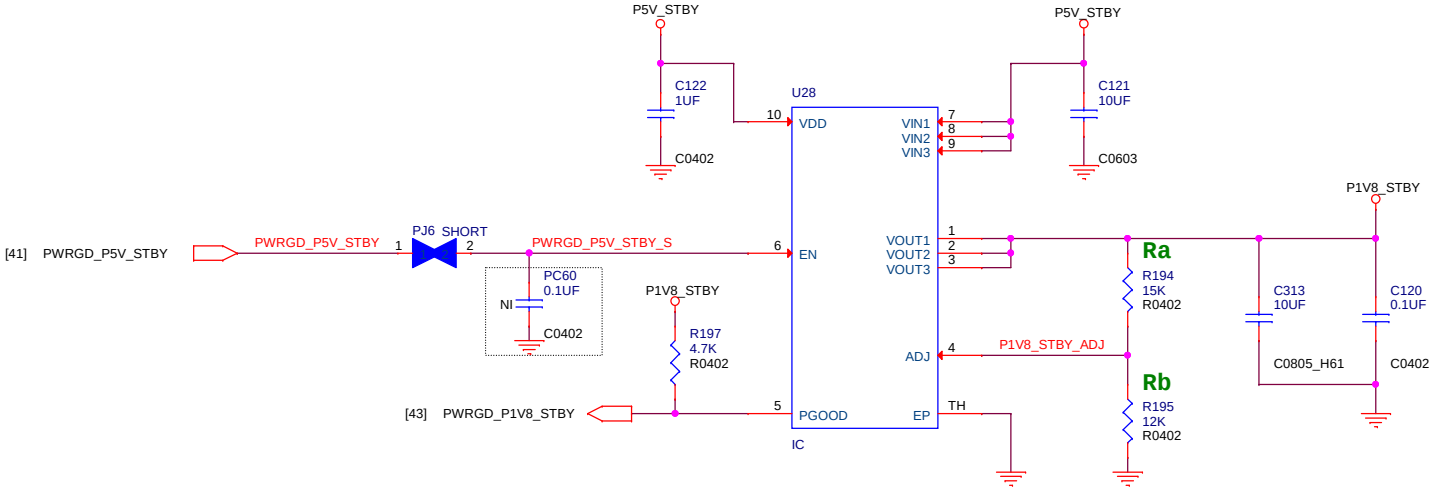
Output Voltage = 1.8V+/-5%
Output Ripple & Noise < 30mV
Transient Tolerance = 180mV
Max current = 0.15A
PD = (5.0V - 1.8V) * 0.15A = 0.48W



VOUT=0.8*(Ra+Rb)/Rb=1.8V

P1V8_STBY

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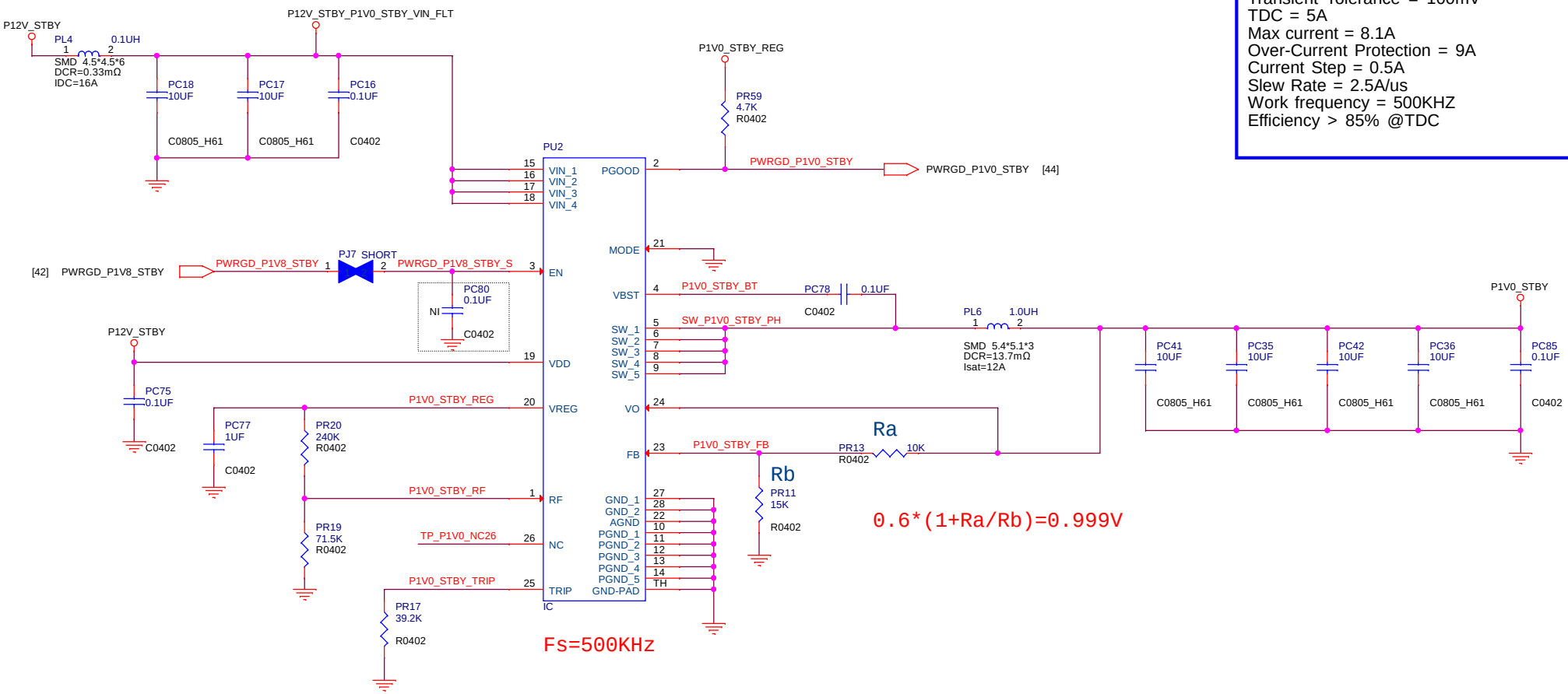

Design specification

Output Voltage = 1.0V± 5 %
Output Ripple & Noise < 50mV
Transient Tolerance = 100mV
TDC = 5A
Max current = 8.1A
Over-Current Protection = 9A
Current Step = 0.5A
Slew Rate = 2.5A/us
Work frequency = 500KHZ
Efficiency > 85% @TDC

P1V0_STBY

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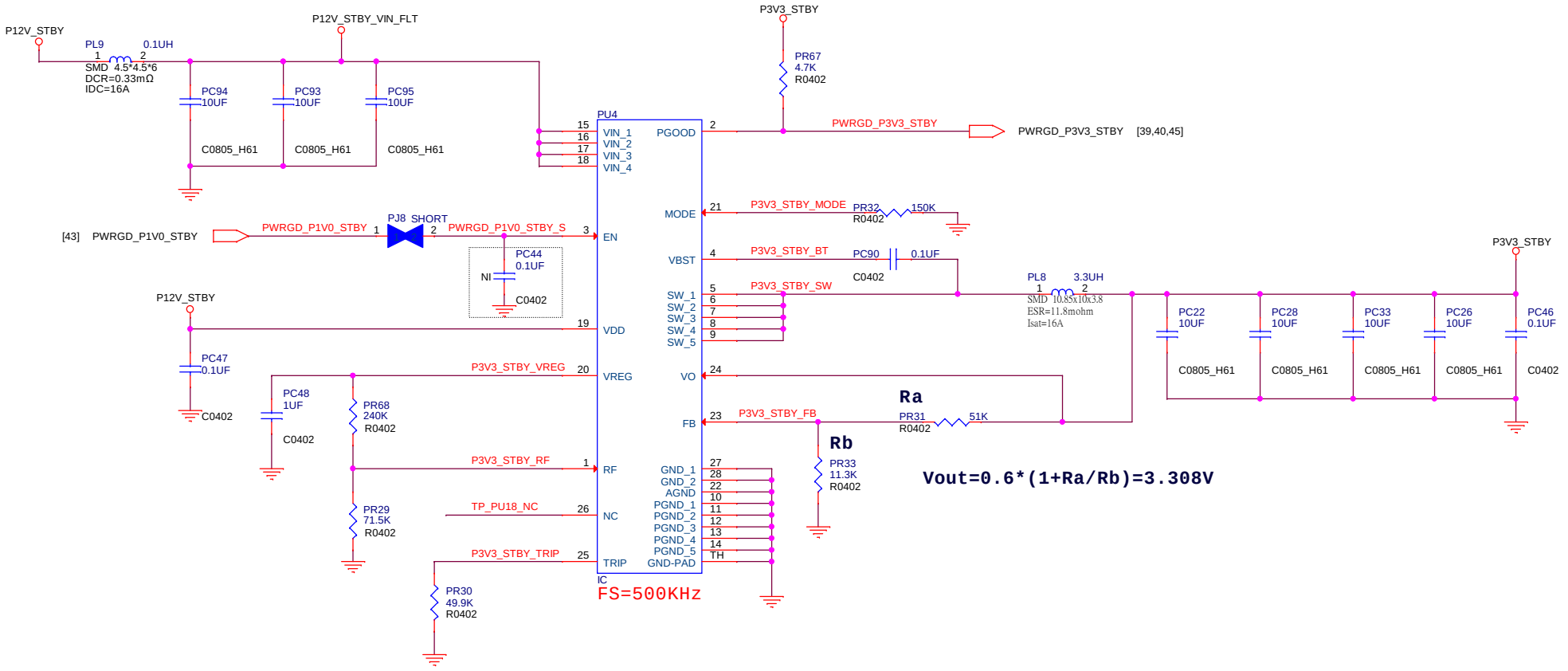
Design specification

Output Voltage = 3.3V± 5 %
Output Ripple & Noise < 30mV
Transient Tolerance = 330mV
TDC = 7A
Max current = 8A
Over-Current Protection(Max current * 1.4) = 11.2A
Current Step = 3.5A
Slew Rate = 2.5A/us
Work frequency = 500KHZ
Efficiency > 85% @TDC



P3V3_STBY

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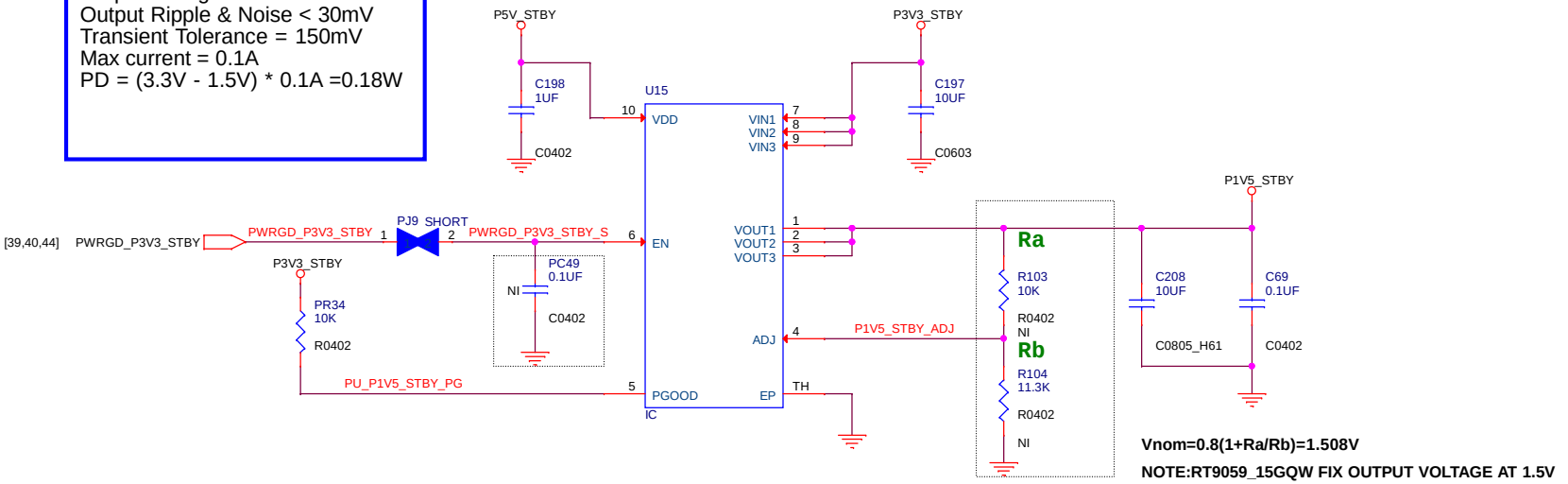
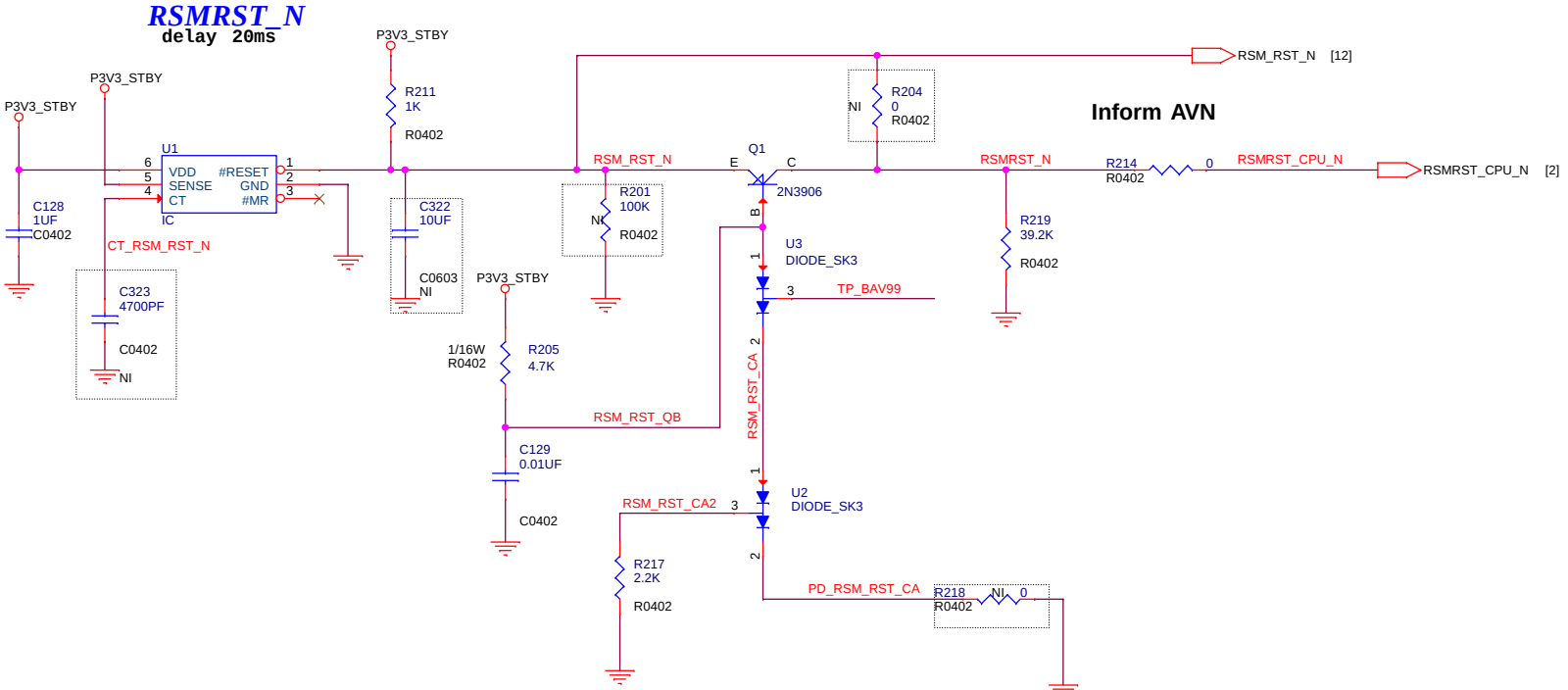
Output Voltage = 1.5V+/-5%
Output Ripple & Noise < 30mV
Transient Tolerance = 150mV
Max current = 0.1A
PD = (3.3V - 1.5V) * 0.1A =0.18W





P1V5_STBY & RSMRST

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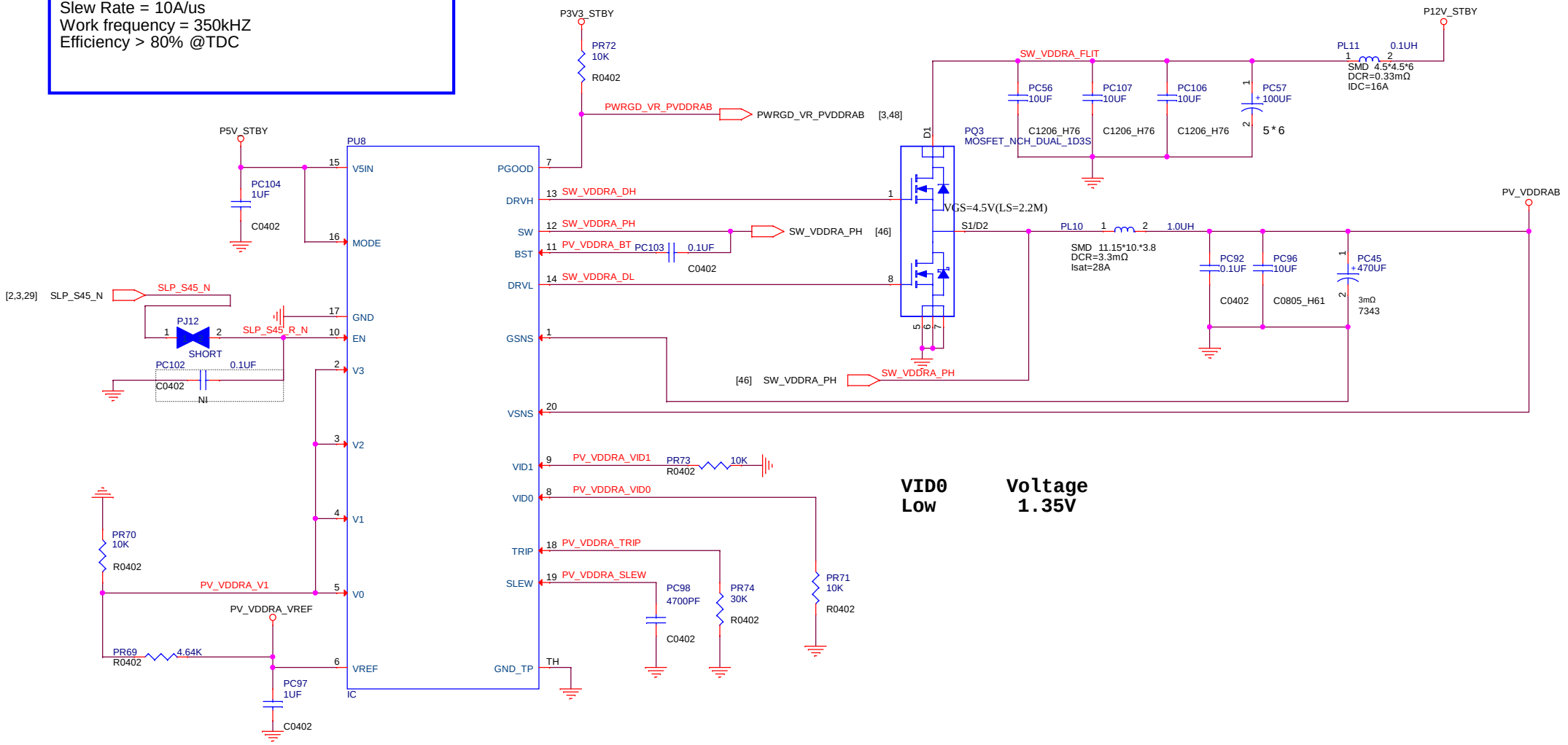
Design specification

Output Voltage = 1.35V± 4 %(DC=± 1. 5)%
Output Ripple & Noise = <15mV or 13mV
Transient Tolerance = +/-4%
TDC =19.3 A
Max current = 22.3A
Over-Current Protection = 25.6A
Current Step = 9.6A
Slew Rate = 10A/us
Work frequency = 350kHZ
Efficiency > 80% @TDC



VID0	Voltage
Low	1.35V

VDDRAB

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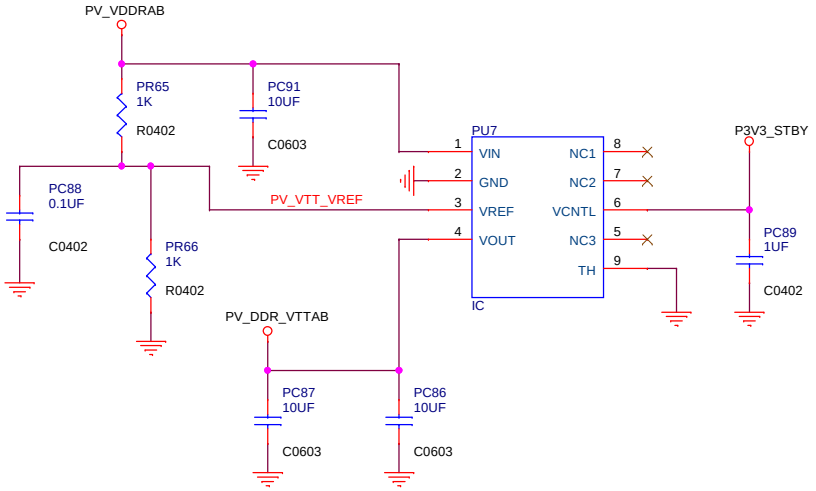
Output Voltage = 0.75V+/-5%
Output Ripple & Noise < 30mV
Transient Tolerance = 75mV
Max current = 0.1A
PD = (1.5V - 0.75V) * 0.1A = 0.075W



VTTAB

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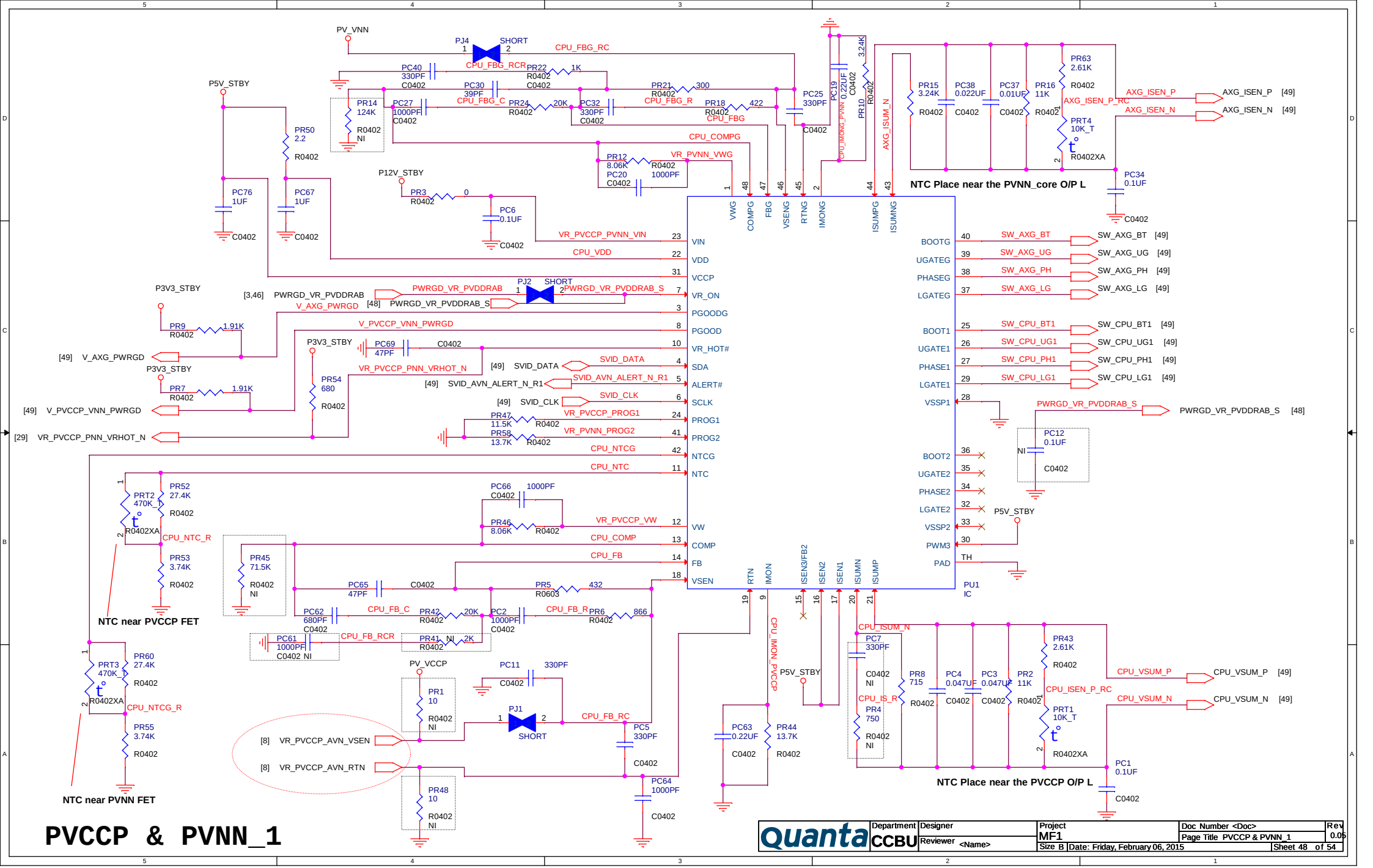
PV_VNN
PJ4
SHORT
CPU_FBG_RC
CPU_FBG_RCR
PC40 330PF C0402
PR22 1K R0402 C0402
PR21 300 R0402
PC30 39PF
CPU_FBG_C
PR24 20K R0402
PC32 330PF C0402
CPU_FBG_R
PR18 422 R0402
CPU_FBG
PR14 124K R0402 NI
PC27 1000PF C0402
P5V_STBY
PR50 2.2 R0402
PC76 1UF C0402
PC67 1UF C0402
P12V_STBY
PR3 0 R0402
PC6 0.1UF C0402
CPU_COMPG
PR12 8.06K R0402
PC20 1000PF C0402
VR_PVNN_VWG
PC25 330PF
PC19 0.22UF C0402
CPU_IMONG_PVNN
PR10 3.24K R0402
AXG_ISUM_N
PR15 3.24K R0402
PC38 0.022UF C0402
PC37 0.01UF C0402
PR16 11K R0402
PR63 2.61K R0402
PRT4 10K_T R0402XA
AXG_ISEN_P
AXG_ISEN_P_RC
AXG_ISEN_N
AXG_ISEN_P [49]
AXG_ISEN_N [49]
NTC Place near the PVNN_core O/P L
PC34 0.1UF C0402
VWG
COMPG
FBG
VSENG
RTNG
IMONG
ISUMPG
ISUMNG
VR_PVCCP_PVNN_VIN
CPU_VDD
VIN
VDD
VCCP
VR_ON
PGOODG
PGOOD
VR_HOT#
SDA
ALERT#
SCLK
PROG1
PROG2
NTCG
NTC
VW
COMP
FB
VSEN
RTN
IMON
ISEN3/FB2
ISEN2
ISEN1
ISUMN
ISUMP
PU1
IC
BOOTG
UGATEG
PHASEG
LGATEG
BOOT1
UGATE1
PHASE1
LGATE1
VSSP1
BOOT2
UGATE2
PHASE2
LGATE2
VSSP2
PWM3
PAD
SW_AXG_BT [49]
SW_AXG_UG [49]
SW_AXG_PH [49]
SW_AXG_LG [49]
SW_CPU_BT1 [49]
SW_CPU_UG1 [49]
SW_CPU_PH1 [49]
SW_CPU_LG1 [49]
PWRGD_VR_PVDDRAB_S [48]
PC12 0.1UF NI C0402
P5V_STBY
P3V3_STBY
[3,46] PWRGD_VR_PVDDRAB
PJ2 SHORT
PWRGD_VR_PVDDRAB_S
V_AXG_PWRGD
PR9 1.91K R0402
[49] V_AXG_PWRGD
V_PVCCP_VNN_PWRGD
PR7 1.91K R0402
[49] V_PVCCP_VNN_PWRGD
PC69 47PF C0402
PR54 680 R0402
VR_PVCCP_PNN_VRHOT_N
[29] VR_PVCCP_PNN_VRHOT_N
[49] SVID_DATA
[49] SVID_AVN_ALERT_N_R1
[49] SVID_CLK
SVID_DATA
SVID_AVN_ALERT_N_R1
SVID_CLK
PR47 11.5K R0402
PR58 13.7K R0402
VR_PVCCP_PROG1
VR_PVNN_PROG2
CPU_NTCG
CPU_NTC
PRT2 470K_T R0402XA
PR52 27.4K R0402
CPU_NTC_R
PR53 3.74K R0402
PR45 71.5K R0402 NI
NTC near PVCCP FET
PRT3 470K_T R0402XA
PR60 27.4K R0402
CPU_NTCG_R
PR55 3.74K R0402
NTC near PVNN FET
PC66 1000PF C0402
PR46 8.06K R0402
VR_PVCCP_VW
CPU_COMP
CPU_FB
PC65 47PF C0402
PR5 432 R0603
PC62 680PF C0402
CPU_FB_C
PR42 20K R0402
PC2 1000PF C0402
CPU_FB_R
PR6 866 R0402
PC61 1000PF C0402 NI
CPU_FB_RCR
PR41 NI 2K R0402
PV_VCCP
PR1 10 R0402 NI
PC11 330PF C0402
PJ1 SHORT
CPU_FB_RC
[8] VR_PVCCP_AVN_VSEN
[8] VR_PVCCP_AVN_RTN
PR48 10 R0402 NI
PC5 330PF C0402
PC64 1000PF C0402
CPU_IMON_PVCCP
PC63 0.22UF C0402
PR44 13.7K R0402
CPU_ISUM_N
PC7 330PF C0402 NI
CPU_IS_R
PR4 750 R0402 NI
PR8 715 R0402
PC4 0.047UF C0402
PC3 0.047UF C0402
PR2 11K R0402
PR43 2.61K R0402
PRT1 10K_T R0402XA
CPU_ISEN_P_RC
CPU_VSUM_P
CPU_VSUM_N
CPU_VSUM_P [49]
CPU_VSUM_N [49]
PC1 0.1UF C0402
NTC Place near the PVCCP O/P L
PVCCP & PVNN_1
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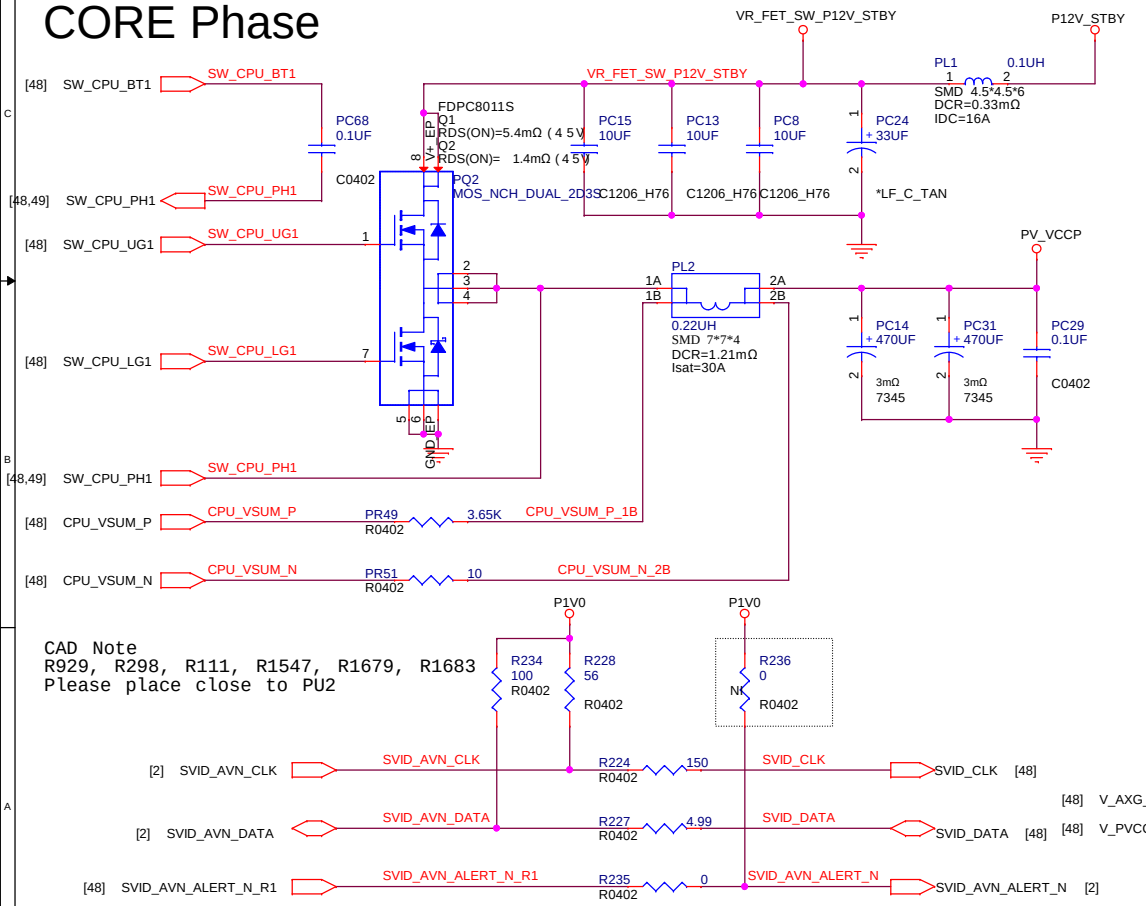
Vcore Design specification

VR12 Avoton Platform
Output Voltage = SVID[7:0] = 0.65~1.3V (VR12)
Output Ripple & Noise < +- 4.5mV
Total TOB = +-54mV
TDC = 11A
Max current = 23.2A
Over-Current Protection(Max Current*120%) = 28A
Current Step = 13A
Slew Rate = 100A/ns
Work frequency = 300kHZ
Load-Line = 0mΩ
Efficiency > 85% @TDC

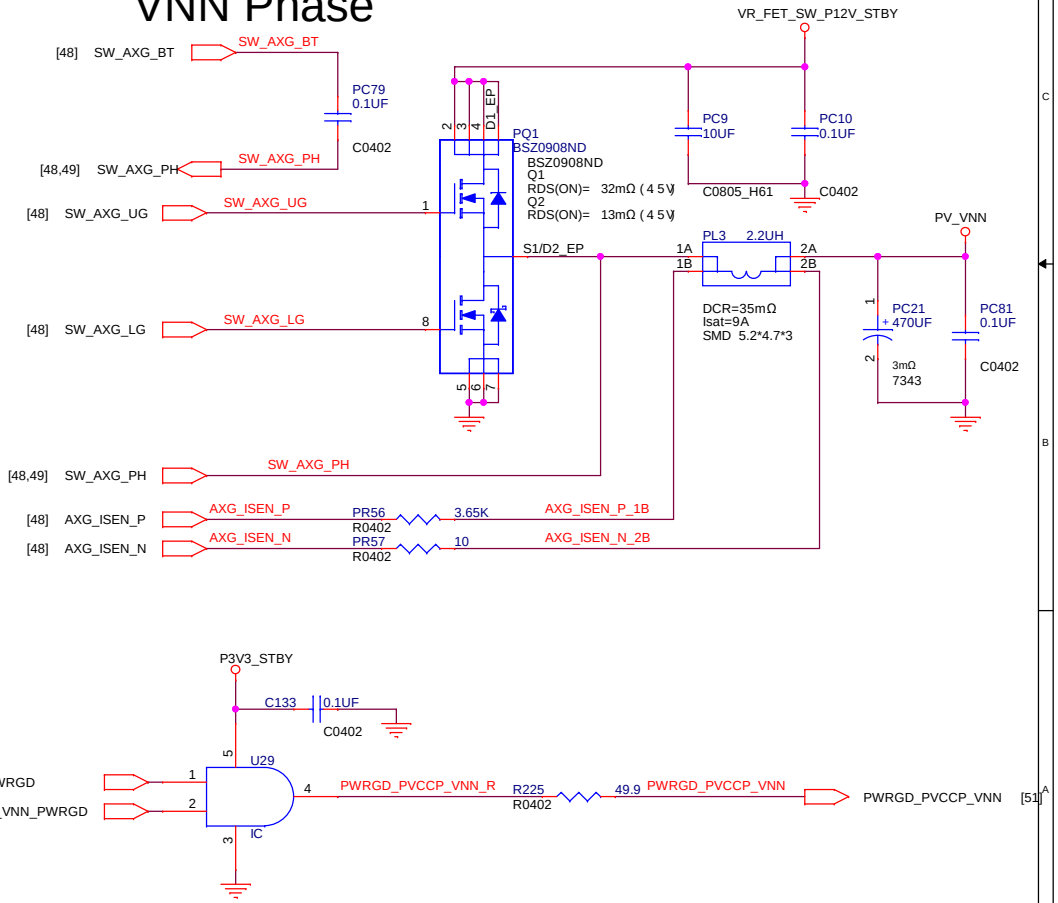
AXG Design specification

VR12 Edisonville Platform
Output Voltage = SVID[7:0] = 0.65~1.3V (VR12)
Output Ripple & Noise < +- 4.5mV
Total TOB = 19mV
TDC = 1A
Max current = 2.2A
Over-Current Protection(Max Current*200%) = 4.5A
Current Step = 1.3A
Slew Rate = 50A/ns
Work frequency = 300kHZ
Load-Line = 0mΩ
Efficiency > 85% @TDC

CORE Phase



VNN Phase



PVCCP & PVNN_2

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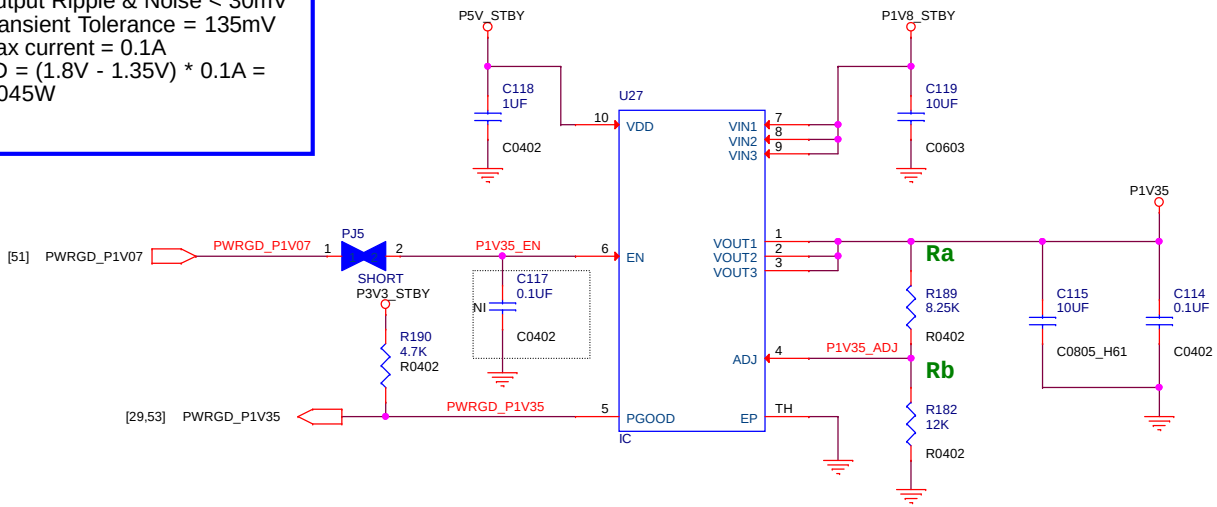
Output Voltage = 1.35V+/-5%
Output Ripple & Noise < 30mV
Transient Tolerance = 135mV
Max current = 0.1A
PD = (1.8V - 1.35V) * 0.1A = 0.045W



Vnom=0.8(1+Ra/Rb)=1.35V

P1V35

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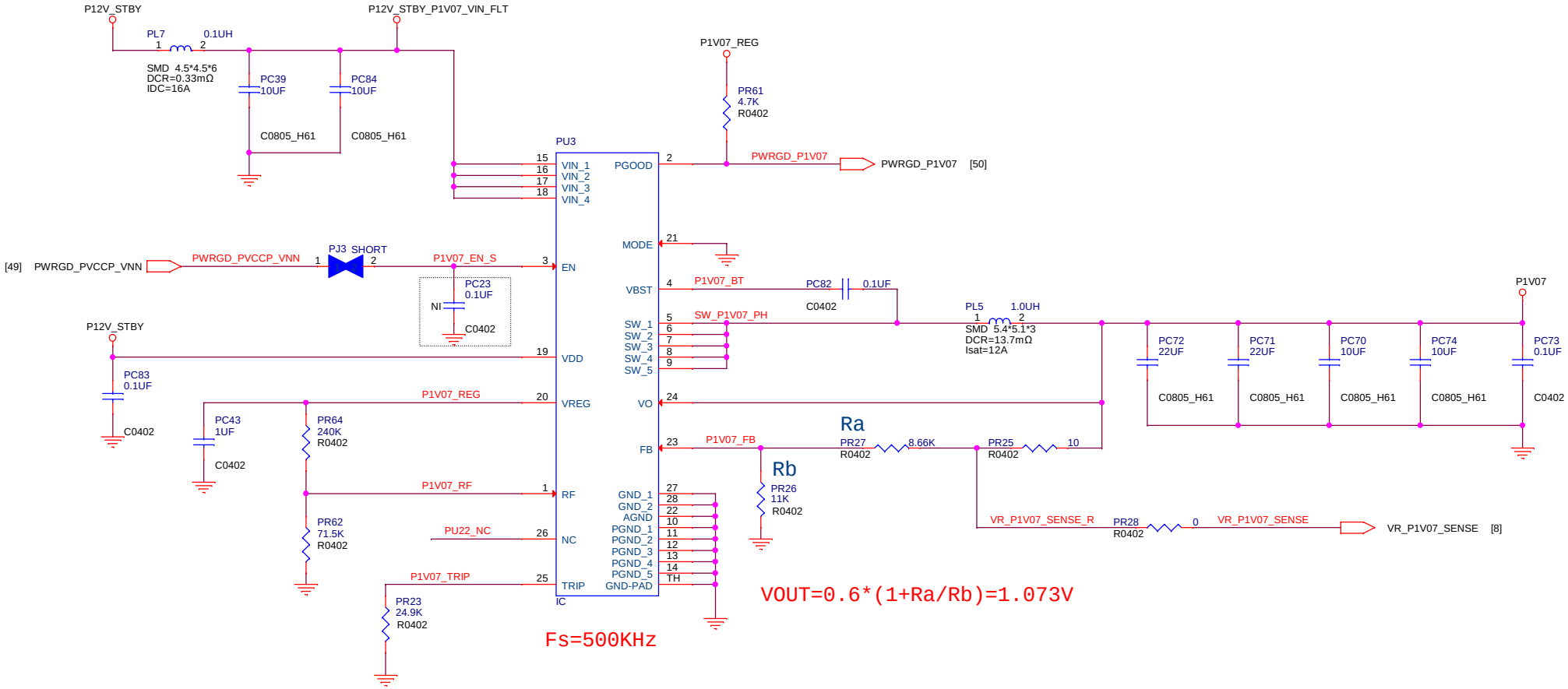
Design specification

Output Voltage = 1.07V± 5 %
Output Ripple & Noise < 50mV
Transient Tolerance = 107mV
TDC = 2.5A
Max current = 2.8A
Over-Current Protection(Max Rating × 1 3) =3 7 A
Current Step = 1.4A
Slew Rate = 2.5A/us
Work frequency = 500KHZ
Efficiency > 85% @TDC



P1V07

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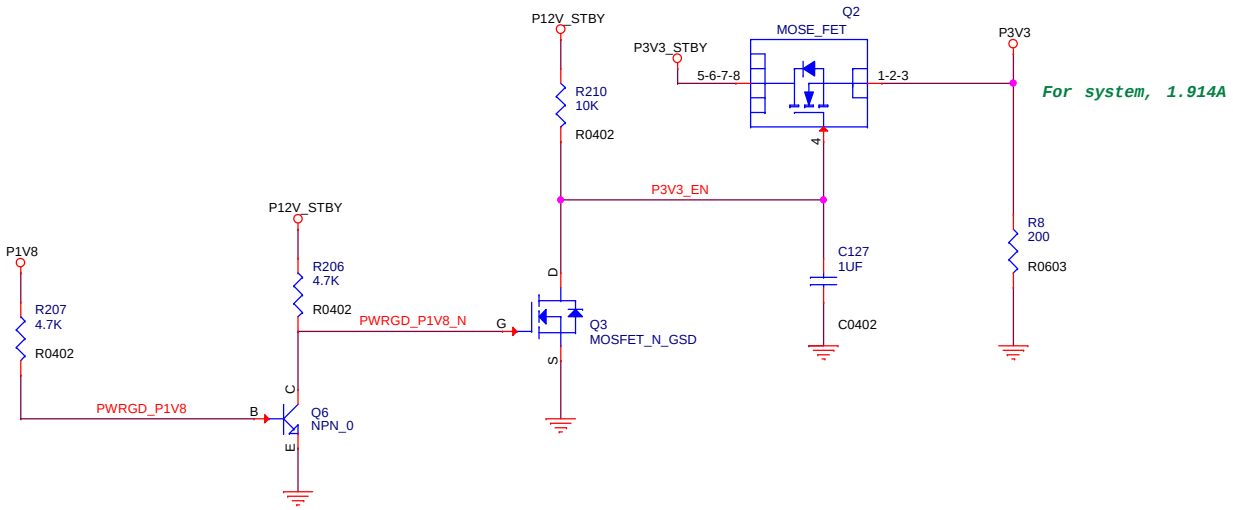
Vds = 25V
Id = 40A (at Vgs=10V)
Rds(on)=8.1m ohm (at Vgs=4.5V)
Rds(on)=6.0 m ohm(at Vgs=10.0V)



P3V3

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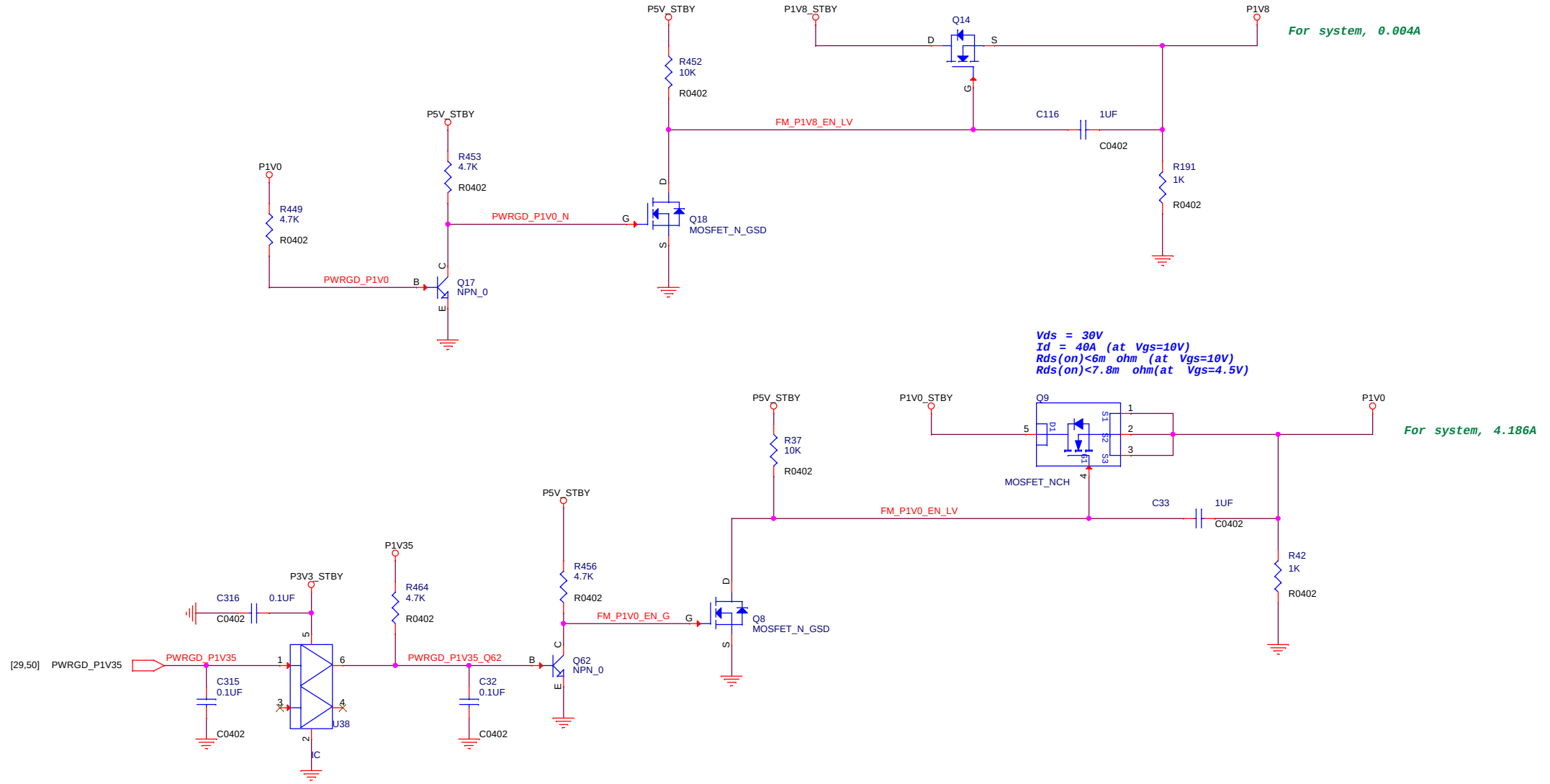

P1V0_P1V8

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