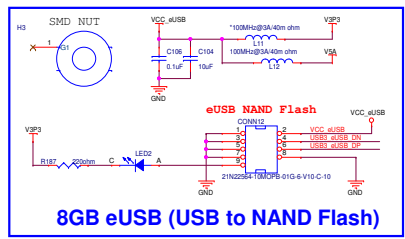
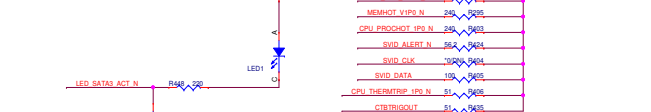
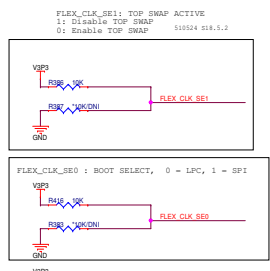
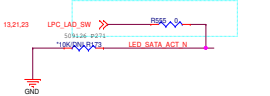
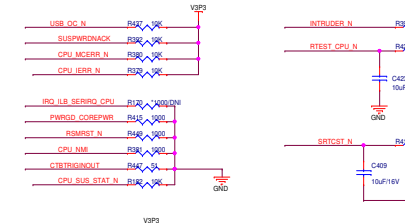
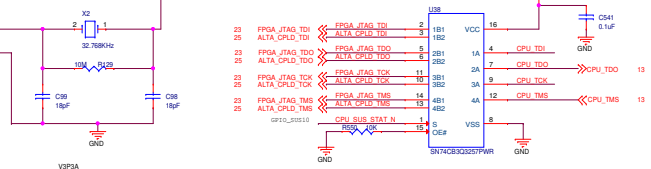
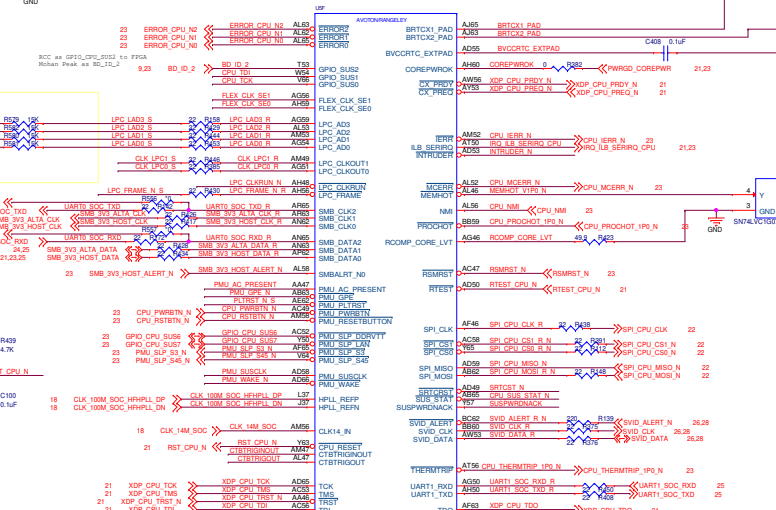
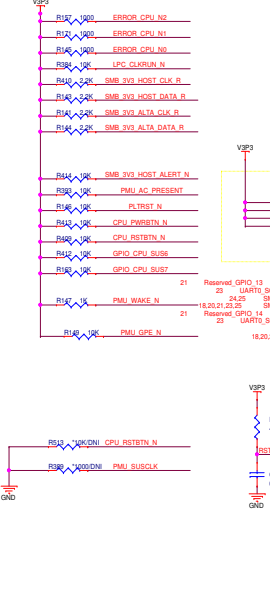


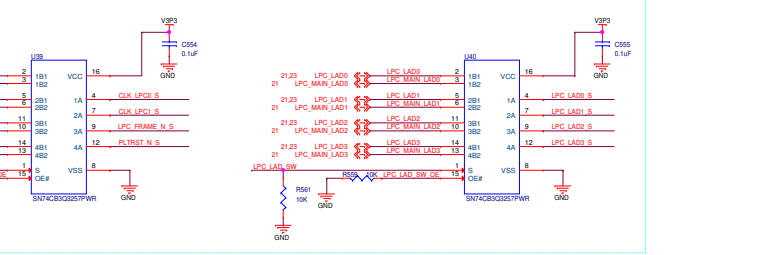
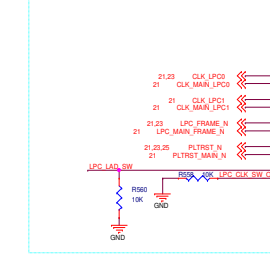
Modification for LPC interface



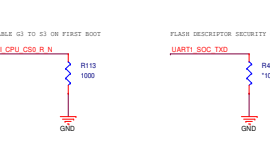
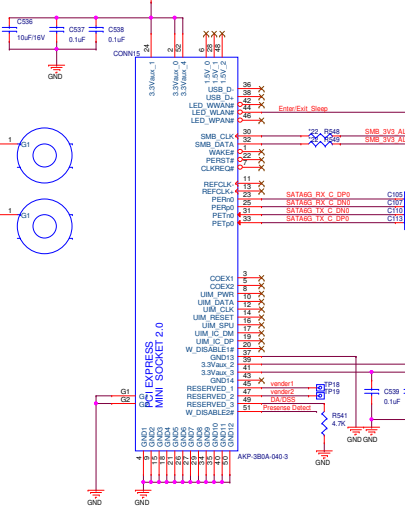
FUNCTION TABLE with columns for DE, S, INPUTS, and FUNCTION.



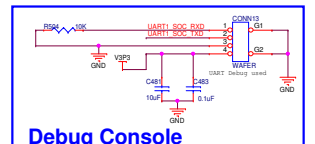
Modification for LPC interface



mSATA CONNECTOR SIGNAL ASSIGNMENTS table with columns for PIN, NAME, and PINN, NAME.



Reserve Console



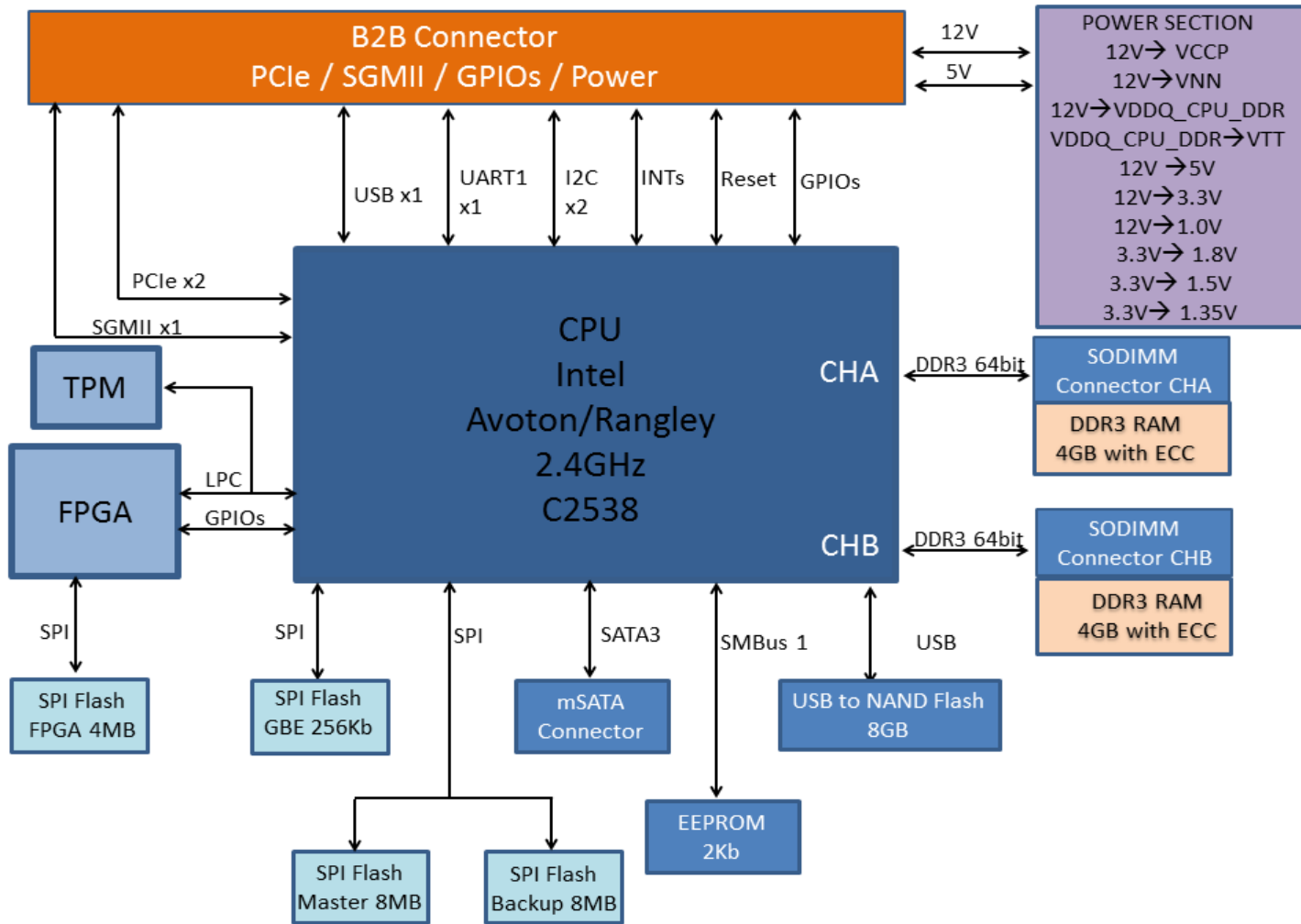
Debug Console (CPU to Mainboard)

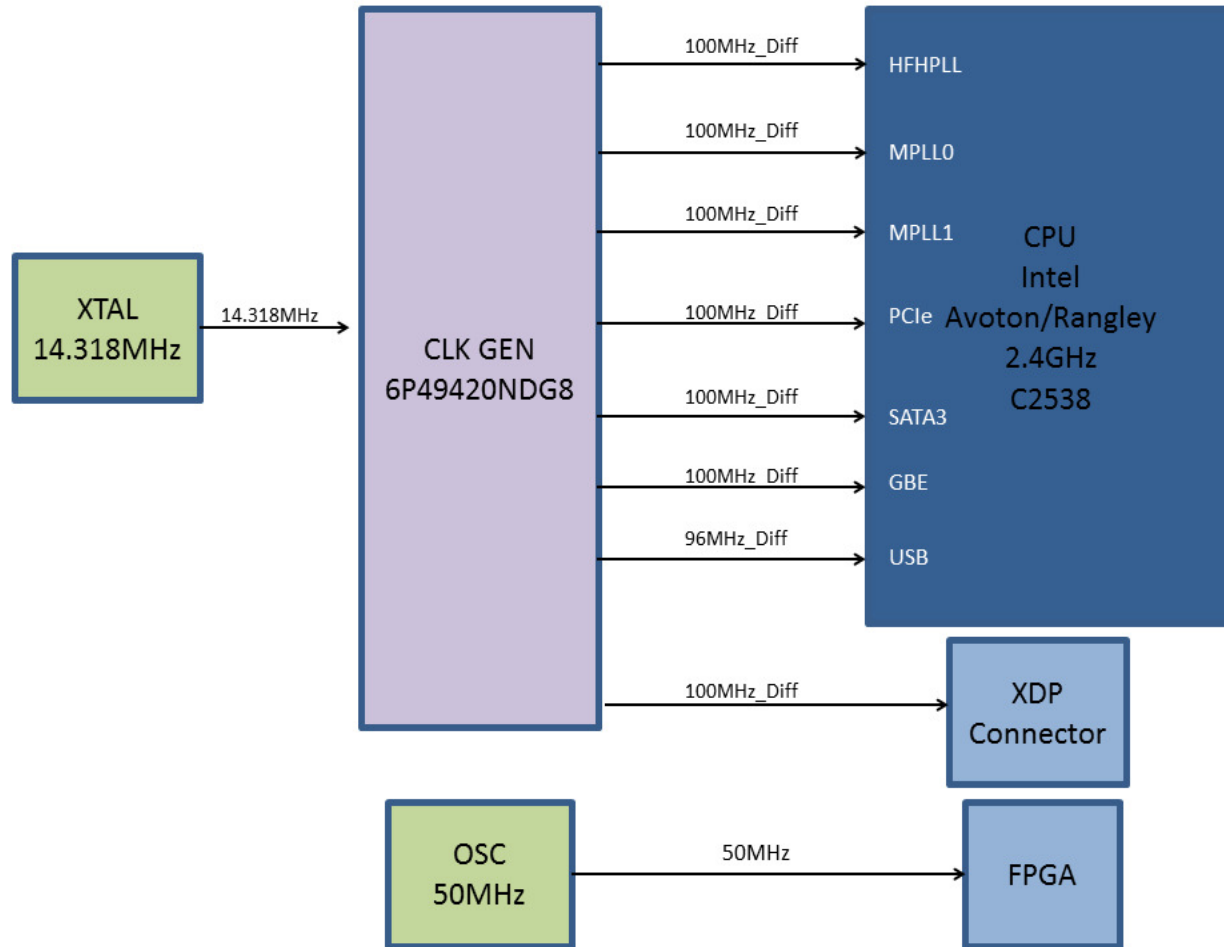
Table of Contents

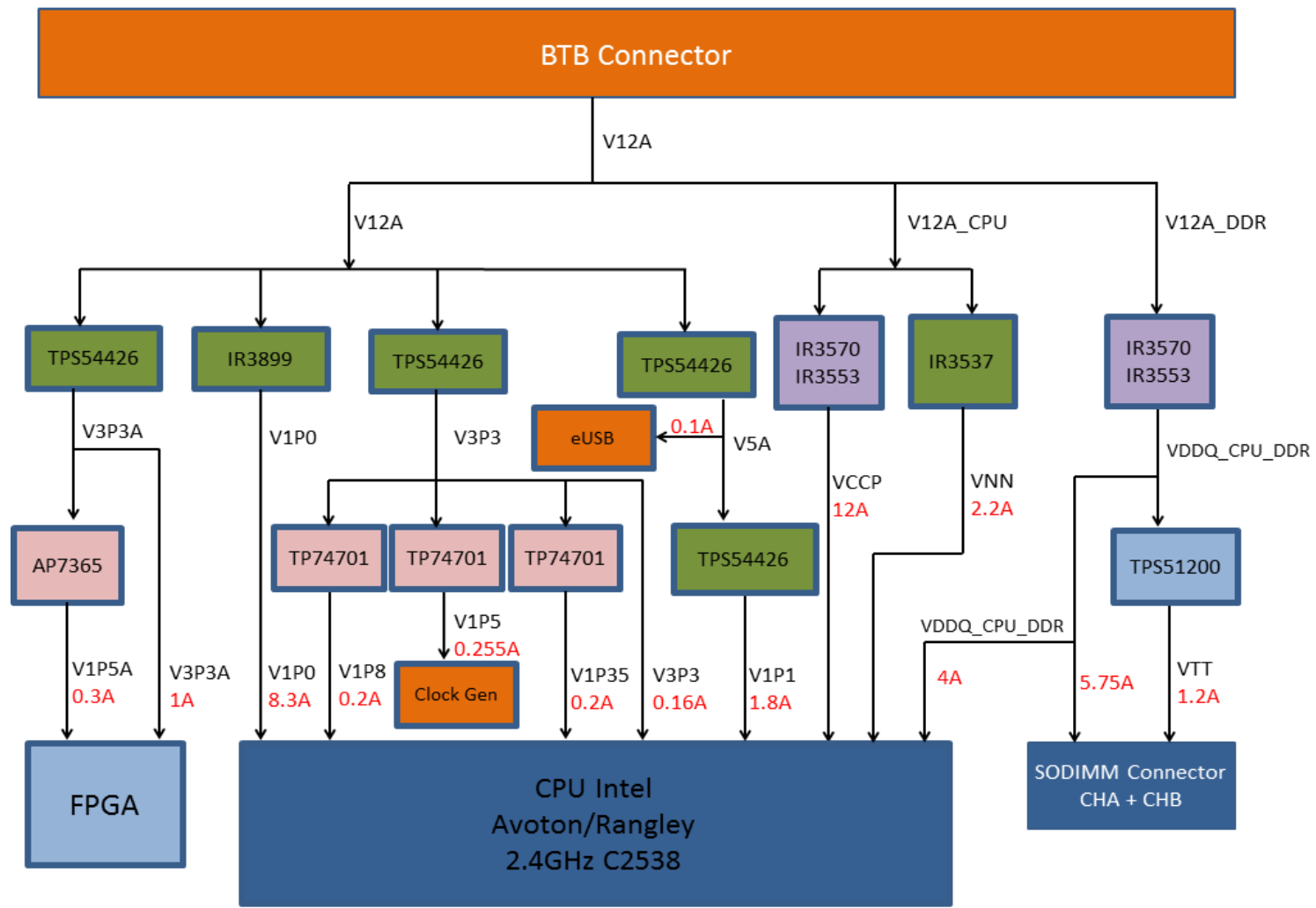
1	Cover Page	18	Clocks
2	History	19	DDR3 SODIMM_CH0
3	Block Diagram	20	DDR3 SODIMM_CH1
4	Clock Tree	21	XDP_PORT80 Debug
5	Power Tree	22	SPI_SCREW_HS_RPCAP
6	SMBus Tree	23	FPGA_Management
7	Reset Tree	24	FPGA_POWER
8	Power Sequence	25	B2B & SATA Connectors
9	GPIO Table	26	VCCP_VNN_PWM
10	JTAG Tree	27	VCCP_VNN_MOS
11	Rangeley_DDRIII_CH0	28	VDDQ_VTT
12	Rangeley_DDRIII_CH1	29	V1P0
13	Rangeley_PCIE, GBE	30	V3P3A_V1P1
14	Rangeley SATA, USB, MISC	31	V5A_V3P3
15	Rangeley Power	32	LDO_V1P8_V1P5_V1P35_V1P5A
16	Rangeley Power	33	Debug LED
17	Rangeley Power_GND		

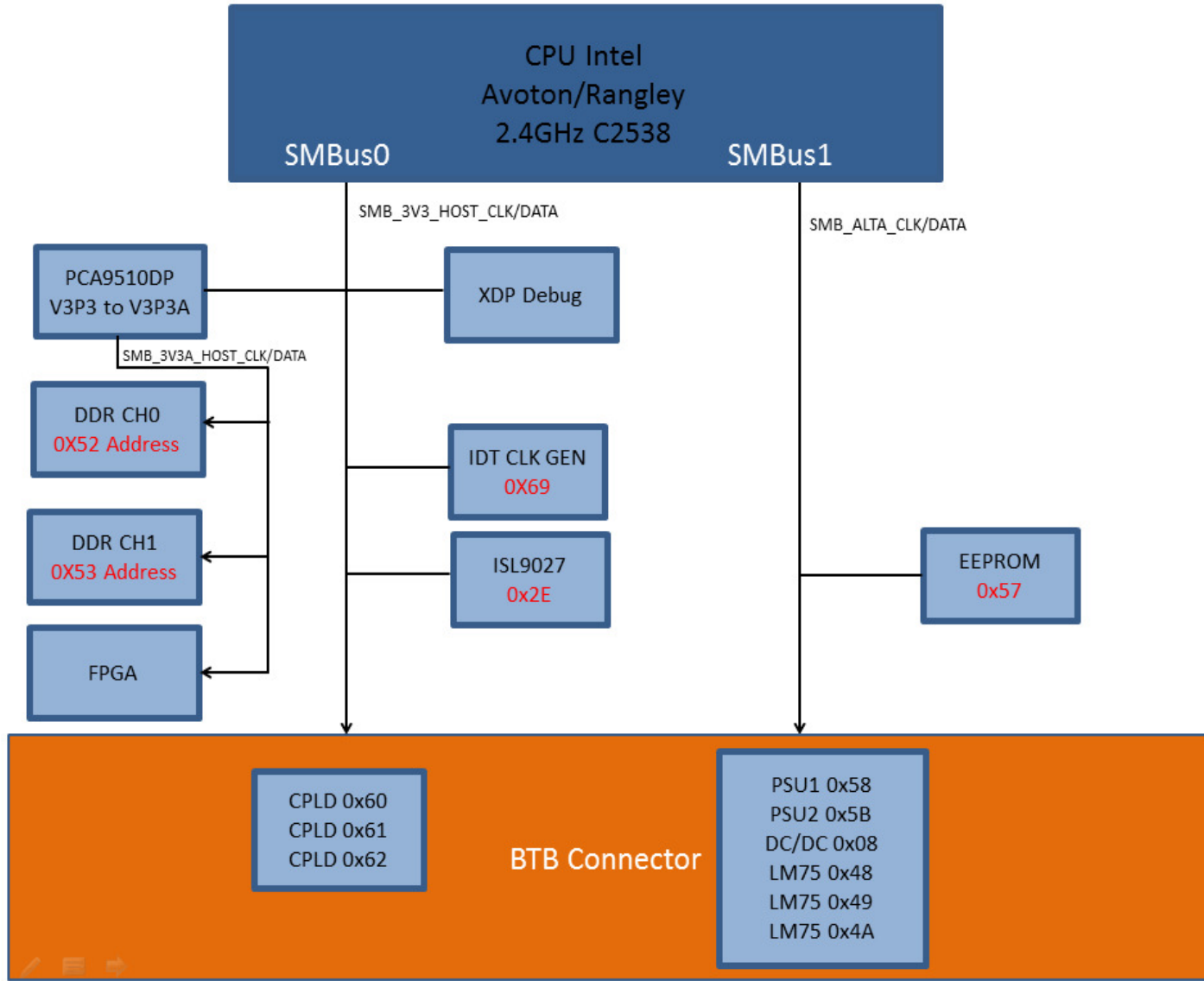
History

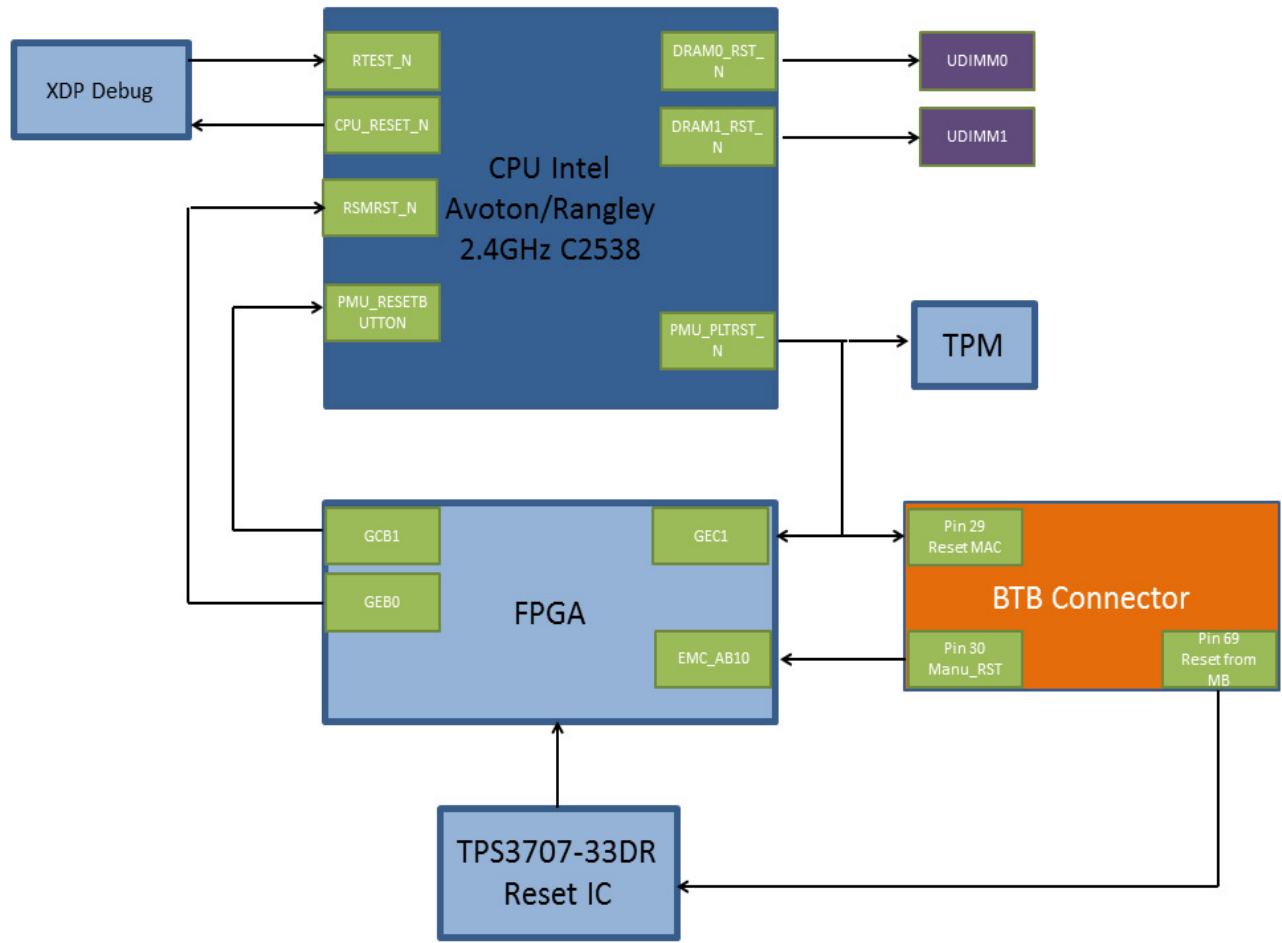
SCH Version	Date	Description
R0A	2014/03/05	Initial Version
R01	2014/06/30	Release to MP

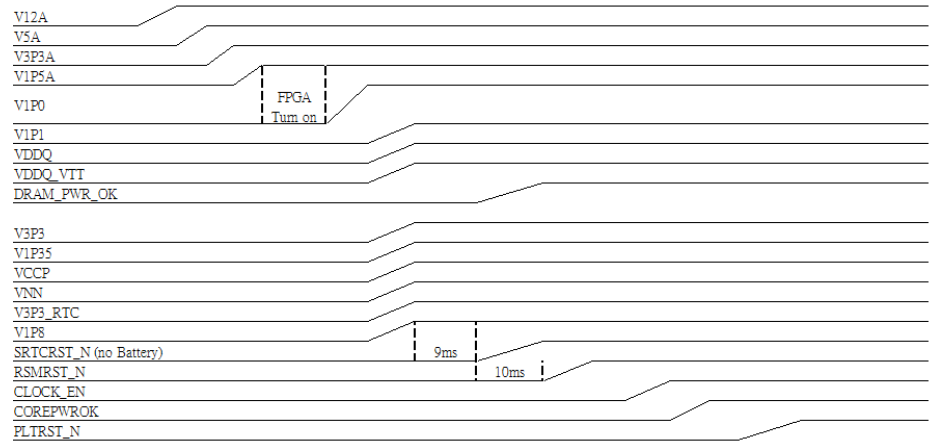






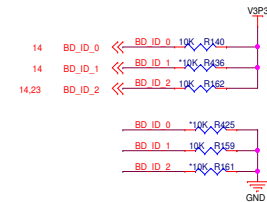






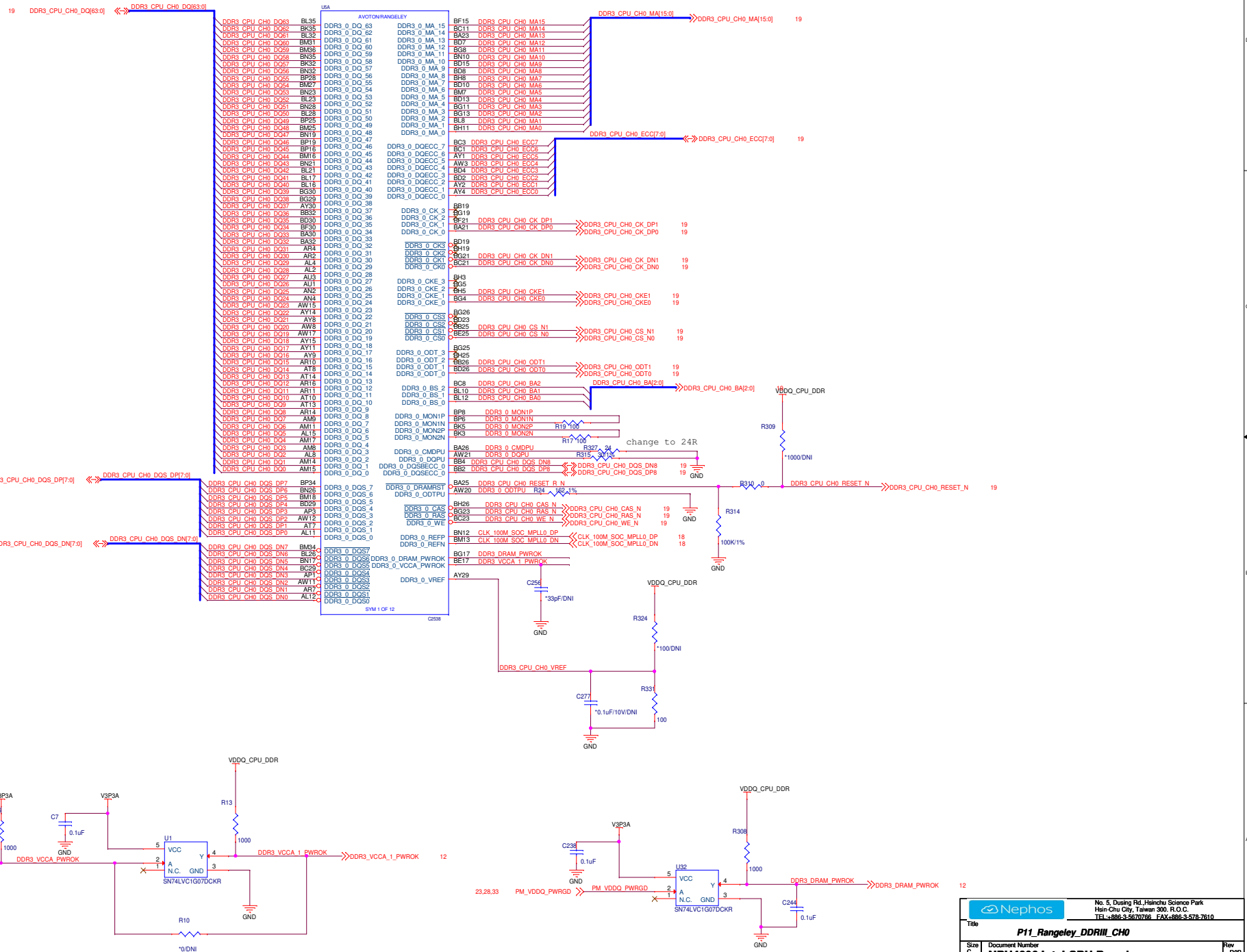
GPIOs	Pin#	Alternate Function	Rangeley Configuration
GPIO_0	AL56	NMI	Alternate Function
GPIO_1	AL63	ERROR2_B	Alternate Function
GPIO_2	AL62	ERROR1_B	Alternate Function
GPIO_3	AL65	ERROR0_B	Alternate Function
GPIO_4	AM52	IRERR_B	Alternate Function
GPIO_5	AL52	MCERR_B	Alternate Function
GPIO_6	AG50	UART1_RXD	Alternate Function
GPIO_7	AH50	UART1_TXD	Alternate Function
GPIO_8	AN62	SMB_CLK0	Alternate Function
GPIO_9	AP62	SMB_DATA0	Alternate Function
GPIO_10	AL58	SMB_ALRT_NO	Alternate Function
GPIO_11	AN63	SMB_DATA1	Goes to Mainboard
GPIO_12	AR63	SMB_CLK1	Goes to Mainboard
GPIO_13	AN65	SMB_DATA2	UART0_TXD
GPIO_14	AR65	SMB_CLK2	UART0_RXD
GPIO_15	AT63	SATA_GPO	BD_ID_0
GPIO_16	AL49	SATA_LEDN	N/A
GPIO_17	AH51	SATA3_GPO	BD_ID_1
GPIO_18	AH54	SATA3_LEDN	Alternate Function
GPIO_19	AH59	FLEX_CLK_SBD	Alternate Function
GPIO_20	AG56	FLEX_CLK_SE1	Alternate Function
GPIO_21	AG54	LPC_LAD0	Alternate Function
GPIO_22	AM53	LPC_LAD1	Alternate Function
GPIO_23	AL53	LPC_LAD2	Alternate Function
GPIO_24	AG59	LPC_LAD3	Alternate Function
GPIO_25	AH56	LPC_FRAMEB	Alternate Function
GPIO_26	AG51	LPC_CLKOUT0	Alternate Function
GPIO_27	AM49	LPC_CLKOUT1	Alternate Function
GPIO_28	AH48	LPC_CLKRUNB	Alternate Function
GPIO_29	AT50	ILB_SERIRQ	Alternate Function
GPIO_30	AM58	PMU_RESETBUTTON_B	Alternate Function

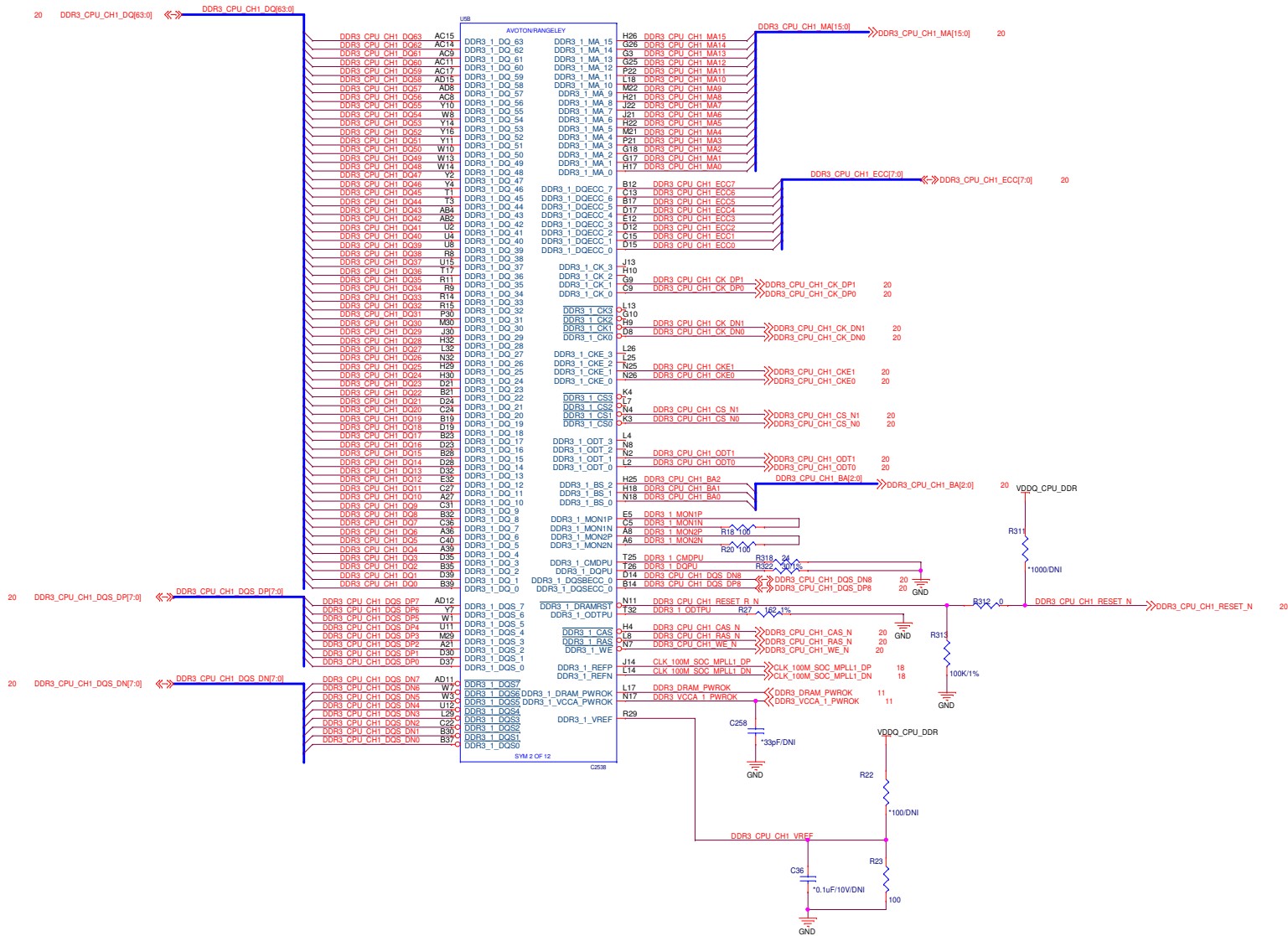
GPIOs	Pin#	Alternate Function	Rangeley Configuration
GPIO_SUS0	V66	N/A	ALTA_CPLD_TCK
GPIO_SUS1	W54	N/A	ALTA_CPLD_TDI
GPIO_SUS2	T53	N/A	BD_ID_2
GPIO_SUS3	Y63	CPU_RESET_B	Alternate Function
GPIO_SUS4	Y57	SUSPWRDNACK	N/A ; pull up
GPIO_SUS5	AD58	PMU_SUSCLK	N/A
GPIO_SUS6	AC52	PMU_SLP_DDRVTT_B	Goes to FPGA, Output
GPIO_SUS7	Y50	PMU_SLP_LAN_B	Goes to FPGA, Output
GPIO_SUS8	AD66	PMU_WAKE_B	Alternate Function
GPIO_SUS9	AC49	PMU_PWRBTN_B	Alternate Function
GPIO_SUS10	AB65	SUS_STAT_B	N/A, pull down
GPIO_SUS11	AD63	USB_OCO_B	Alternate Function
GPIO_SUS12	AC58	SPI_CS1_B	Alternate Function
GPIO_SUS13	W51	GBE_EE_DI	Alternate Function
GPIO_SUS14	W60	GBE_EE_DO	Alternate Function
GPIO_SUS15	T50	GBE_EE_SK	Alternate Function
GPIO_SUS16	R59	GBE_EE_CS	Alternate Function
GPIO_SUS17	T58	GBE_SDF0_0	CPLD_INT_L
GPIO_SUS18	T48	GBE_SDF0_1	CPLD2_INT_L
GPIO_SUS19	P46	GBE_LED0	N/A, pull down
GPIO_SUS20	W50	GBE_LED1	N/A, pull down
GPIO_SUS21	P48	GBE_LED2	N/A, pull down
GPIO_SUS22	R58	GBE_LED3	N/A, pull down
GPIO_SUS23	V63	GBE_WOL	N/A, pull down
GPIO_SUS24	W56	GBE_MDIO0_I2C_CLK	MDIO0_CLK
GPIO_SUS25	W59	GBE_MDIO0_I2C_DATA	MDIO0_DATA
GPIO_SUS26	Y54	GBE_MDIO1_I2C_CLK	ALTA_CPLD_TDO
GPIO_SUS27	Y53	GBE_MDIO1_I2C_DATA	ALTA_CPLD_TMS

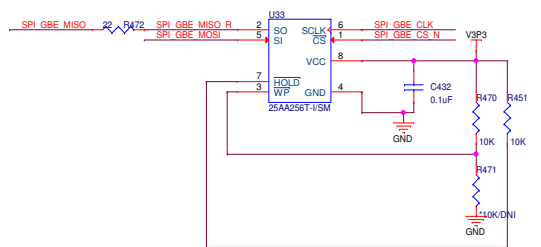
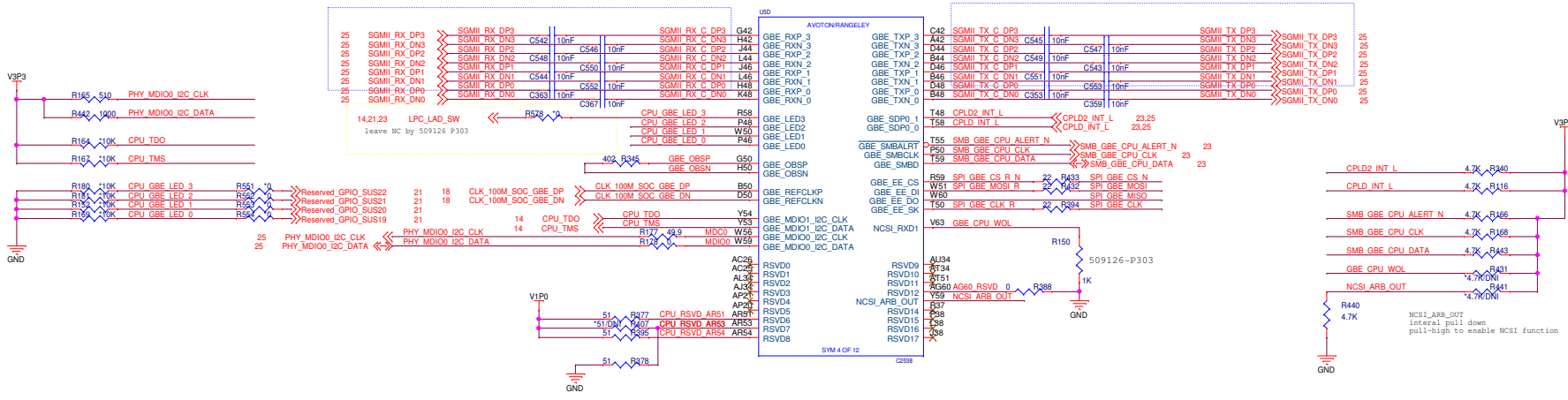
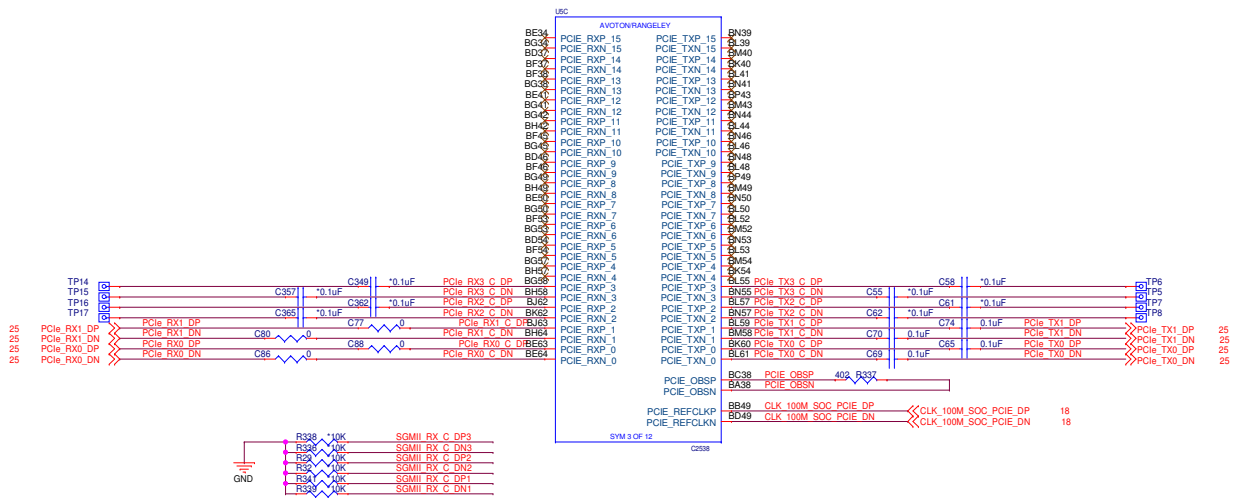


BD_ID_2	BD_ID_1	BD_ID_0	Board Type
0	0	0	Lyon Peak SV
0	0	1	Lyon Peak BDV
0	1	0	Lyon Peak PPV
1	0	0	Mohon Peak
1	0	1	Intel Project 2
1	1	0	Tiger Cove

BLANK PAGE







USK		
AC29	AVOTONRANGELEY	T21
AC29	VSS_279	VSS_348
AC23	VSS_280	VSS_349
AC21	VSS_281	VSS_350
AC20	VSS_282	VSS_351
AC18	VSS_283	VSS_352
AC17	VSS_284	VSS_353
AC12	VSS_285	VSS_354
AE20	VSS_286	VSS_355
ABS	VSS_287	VSS_356
AB1	VSS_288	VSS_357
AA98	VSS_289	VSS_358
AA64	VSS_290	VSS_359
AA62	VSS_291	VSS_360
AA62	VSS_292	VSS_361
AA42	VSS_293	VSS_362
AA36	VSS_294	VSS_363
AA31	VSS_295	VSS_364
AA29	VSS_296	VSS_365
AA28	VSS_297	VSS_366
AA26	VSS_298	VSS_367
AA25	VSS_299	VSS_368
AA23	VSS_300	VSS_369
AA5	VSS_301	VSS_370
AA3	VSS_302	VSS_371
V56	VSS_303	VSS_372
Y51	VSS_304	VSS_373
Y48	VSS_305	VSS_374
Y19	VSS_306	VSS_375
Y17	VSS_307	VSS_376
Y13	VSS_308	VSS_377
Y8	VSS_309	VSS_378
V5	VSS_310	VSS_379
W82	VSS_311	VSS_380
W57	VSS_312	VSS_381
W53	VSS_313	VSS_382
W48	VSS_314	VSS_383
W42	VSS_315	VSS_384
W39	VSS_316	VSS_385
W36	VSS_317	VSS_386
W32	VSS_318	VSS_387
W19	VSS_319	VSS_388
W17	VSS_320	VSS_389
W16	VSS_321	VSS_390
W11	VSS_322	VSS_391
W4	VSS_323	VSS_392
V44	VSS_324	VSS_393
V42	VSS_325	VSS_394
V36	VSS_326	VSS_395
V32	VSS_327	VSS_396
V5	VSS_328	VSS_397
U65	VSS_329	VSS_398
U63	VSS_330	VSS_399
U62	VSS_331	VSS_400
U14	VSS_332	VSS_401
U9	VSS_333	VSS_402
T62	VSS_334	VSS_403
T56	VSS_335	VSS_404
T52	VSS_336	VSS_405
T47	VSS_337	VSS_406
T42	VSS_338	VSS_407
T41	VSS_339	VSS_408
T36	VSS_340	VSS_409
T34	VSS_341	VSS_410
T31	VSS_342	VSS_411
T29	VSS_343	VSS_412
T28	VSS_344	VSS_413
T26	VSS_345	VSS_414
T23	VSS_346	VSS_415
VSS_347		

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USL		
G41	AVOTONRANGELEY	E1
G41	VSS_416	VSS_459
G34	VSS_417	VSS_460
G32	VSS_418	VSS_461
F66	VSS_419	VSS_462
F63	VSS_420	VSS_463
F4	VSS_421	VSS_464
F1	VSS_422	VSS_465
E66	VSS_423	VSS_466
E61	VSS_424	VSS_467
E59	VSS_425	VSS_468
E55	VSS_426	VSS_469
E54	VSS_427	VSS_470
E51	VSS_428	VSS_471
E52	VSS_429	VSS_472
E50	VSS_430	VSS_473
E49	VSS_431	VSS_474
E48	VSS_432	VSS_475
E46	VSS_433	VSS_476
E45	VSS_434	VSS_477
E43	VSS_435	VSS_478
E41	VSS_436	VSS_479
E40	VSS_437	VSS_480
E39	VSS_438	VSS_481
E37	VSS_439	VSS_482
E36	VSS_440	VSS_483
E34	VSS_441	VSS_484
E31	VSS_442	VSS_485
E30	VSS_443	VSS_486
E28	VSS_444	VSS_487
E27	VSS_445	VSS_488
E25	VSS_446	VSS_489
E23	VSS_447	VSS_490
E22	VSS_448	VSS_491
E21	VSS_449	VSS_492
E19	VSS_450	VSS_493
E18	VSS_451	VSS_494
E16	VSS_452	VSS_495
E14	VSS_453	VSS_496
E13	VSS_454	VSS_497
E10	VSS_455	VSS_498
L50	VSS_456	
E5	VSS_457/SSA_USB_1	AA44
	VSS_458/SSA_USB_2	AU44

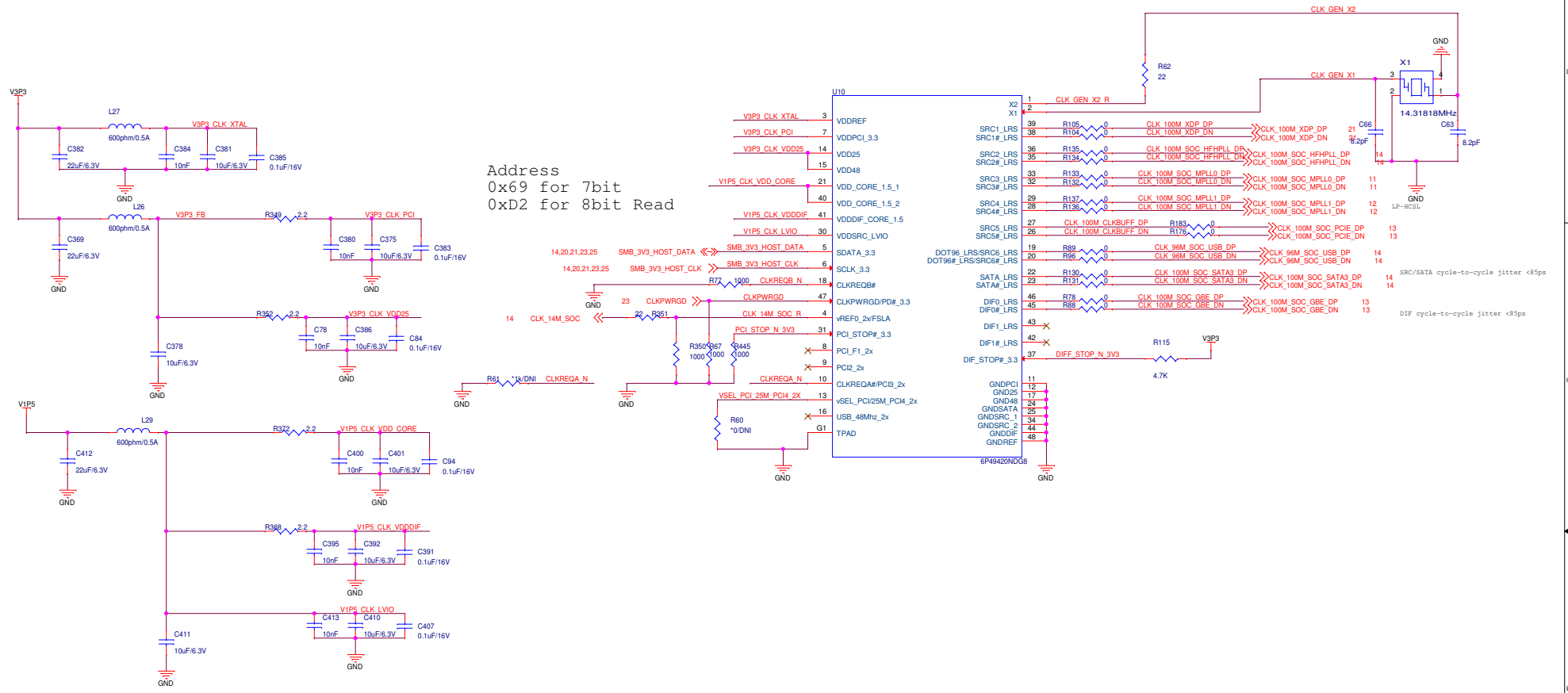
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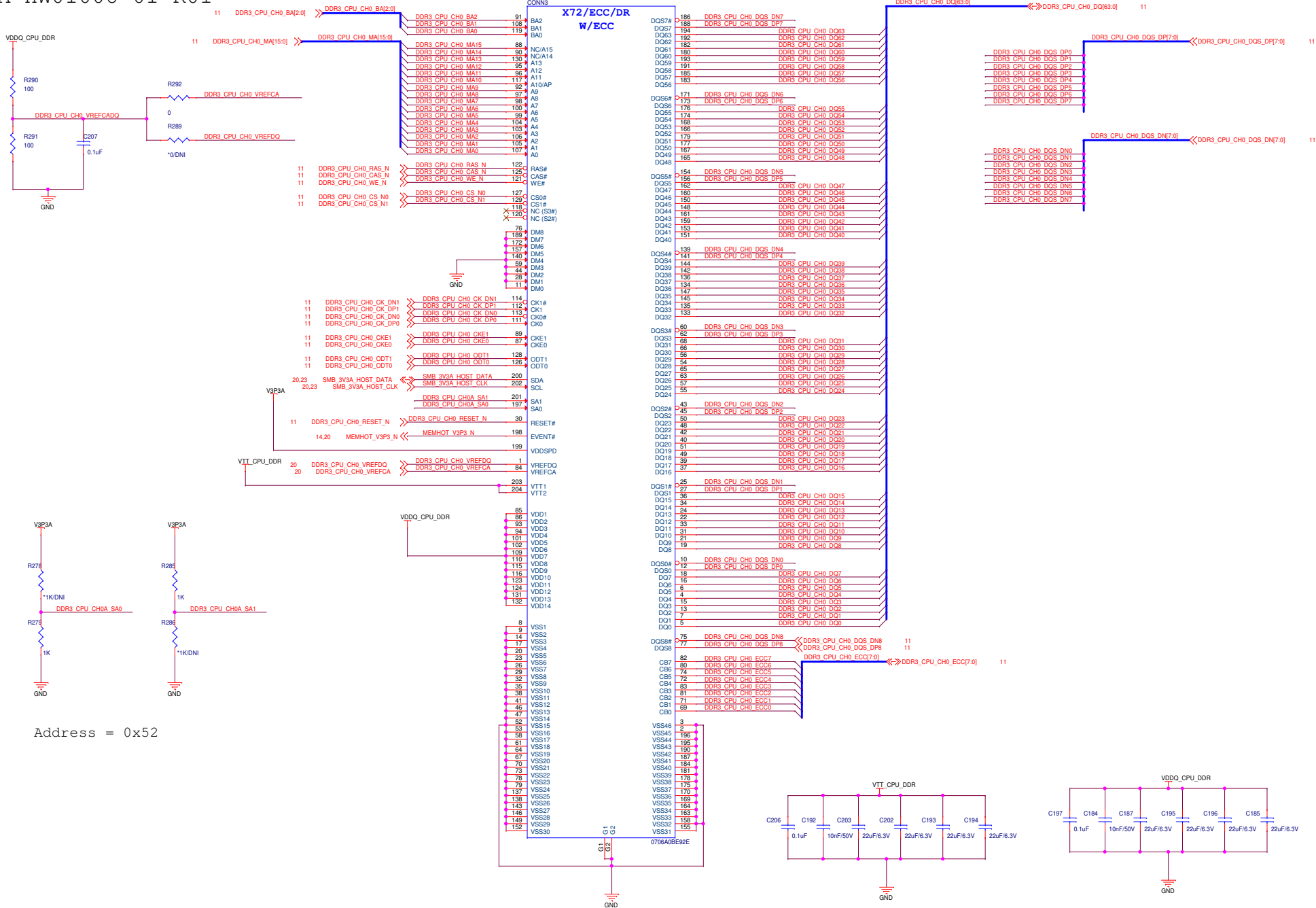
USJ		
BP66	AVOTONRANGELEY	BH60
BP64	VSS_2	VSS_71
BP62	VSS_3	VSS_72
BP61	VSS_4	VSS_73
BP59	VSS_5	VSS_74
BP58	VSS_6	VSS_75
BP55	VSS_7	VSS_76
BP54	VSS_8	VSS_77
BP46	VSS_9	VSS_78
BP40	VSS_10	VSS_79
BP37	VSS_11	VSS_81
BP31	VSS_12	VSS_82
BP13	VSS_13	VSS_83
BP10	VSS_14	VSS_84
K50	VSS_15	VSS_85
K49	VSS_16	VSS_86
BP1	VSS_17	VSS_87
BN37	VSS_18	VSS_88
BN30	VSS_19	VSS_89
BN14	VSS_20	VSS_90
BM66	VSS_21	VSS_91
BM64	VSS_22	VSS_92
BM62	VSS_23	VSS_93
BM61	VSS_24	VSS_94
BM45	VSS_25	VSS_95
BM22	VSS_26	VSS_96
BM5	VSS_27	VSS_97
BM3	VSS_28	VSS_98
BM1	VSS_29	VSS_99
BL43	VSS_30	VSS_100
BL37	VSS_31	VSS_101
BL34	VSS_32	VSS_102
BL30	VSS_33	VSS_103
BL26	VSS_34	VSS_104
BL19	VSS_35	VSS_105
BL14	VSS_36	VSS_106
BL1	VSS_37	VSS_107
BK66	VSS_38	VSS_108
BK64	VSS_39	VSS_109
BK62	VSS_40	VSS_110
BK57	VSS_41	VSS_111
BK56	VSS_42	VSS_112
BK53	VSS_43	VSS_113
BK51	VSS_44	VSS_114
BK49	VSS_45	VSS_115
BK48	VSS_46	VSS_116
BK45	VSS_47	VSS_117
BK44	VSS_48	VSS_118
BK42	VSS_49	VSS_119
BK39	VSS_50	VSS_120
BK37	VSS_51	VSS_121
BK36	VSS_52	VSS_122
BK31	VSS_53	VSS_123
BK30	VSS_54	VSS_124
BK27	VSS_55	VSS_125
BK28	VSS_56	VSS_126
BK26	VSS_57	VSS_127
BK24	VSS_58	VSS_128
BK22	VSS_59	VSS_129
BK21	VSS_60	VSS_130
BK19	VSS_61	VSS_131
BK18	VSS_62	VSS_132
BK17	VSS_63	VSS_133
BK15	VSS_64	VSS_134
BK14	VSS_65	VSS_135
BK9	VSS_66	VSS_136
BK1	VSS_67	VSS_137
BK1	VSS_68	VSS_138
BK1	VSS_69	VSS_139
BK1	VSS_70	VSS_140

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USK		
AW32	AVOTONRANGELEY	AL20
AW31	VSS_141	VSS_211
AW30	VSS_142	VSS_212
AW28	VSS_143	VSS_213
AW26	VSS_144	VSS_214
AW25	VSS_145	VSS_215
AW23	VSS_146	VSS_216
AW19	VSS_147	VSS_217
AW14	VSS_148	VSS_218
AW9	VSS_149	VSS_219
AW5	VSS_150	VSS_220
AV5	VSS_151	VSS_221
AV4	VSS_152	VSS_222
AV2	VSS_153	VSS_223
AV1	VSS_154	VSS_224
AU4	VSS_155	VSS_225
AT66	VSS_156	VSS_226
AT64	VSS_157	VSS_227
AT57	VSS_158	VSS_228
AT53	VSS_159	VSS_229
AT19	VSS_160	VSS_230
AT17	VSS_161	VSS_231
AT16	VSS_162	VSS_232
AT11	VSS_163	VSS_233
AT11	VSS_164	VSS_234
AT11	VSS_165	VSS_235
AT5	VSS_166	VSS_236
AR60	VSS_167	VSS_237
AR56	VSS_168	VSS_238
AR50	VSS_169	VSS_239
AR19	VSS_170	VSS_240
AR17	VSS_171	VSS_241
AR13	VSS_172	VSS_242
AR8	VSS_173	VSS_243
AP44	VSS_174	VSS_244
AP46	VSS_175	VSS_245
AP44	VSS_176	VSS_246
AP41	VSS_177	VSS_247
AP39	VSS_178	VSS_248
AP38	VSS_179	VSS_249
AP36	VSS_180	VSS_250
AP36	VSS_181	VSS_251
AP34	VSS_182	VSS_252
AP32	VSS_183	VSS_253
AP31	VSS_184	VSS_254
AP29	VSS_185	VSS_255
AP28	VSS_186	VSS_256
AP26	VSS_187	VSS_257
AP25	VSS_188	VSS_258
AP23	VSS_189	VSS_259
AP5	VSS_190	VSS_260
AN65	VSS_191	VSS_261
AN47	VSS_192	VSS_262
AN5	VSS_193	VSS_263
AM59	VSS_194	VSS_264
AM55	VSS_195	VSS_265
AM50	VSS_196	VSS_266
AM45	VSS_197	VSS_267
AM44	VSS_198	VSS_268
AM23	VSS_199	VSS_269
AM21	VSS_200	VSS_270
AM20	VSS_201	VSS_271
AM18	VSS_202	VSS_272
AM12	VSS_203	VSS_273
AL59	VSS_204	VSS_274
AL55	VSS_205	VSS_275
AL50	VSS_206	VSS_276
AL44	VSS_207	VSS_277
AL42	VSS_208	VSS_278
AL38	VSS_209	

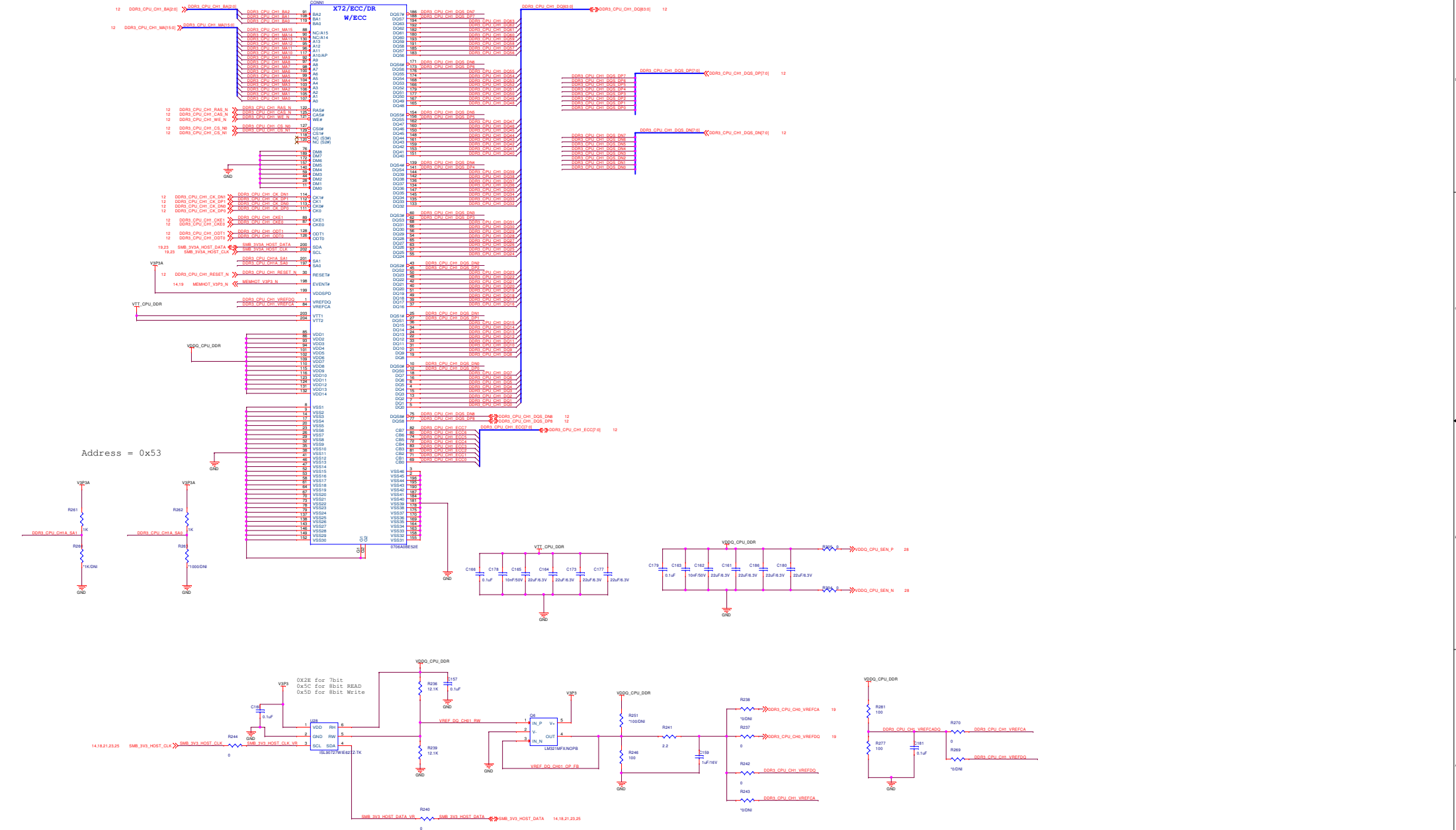
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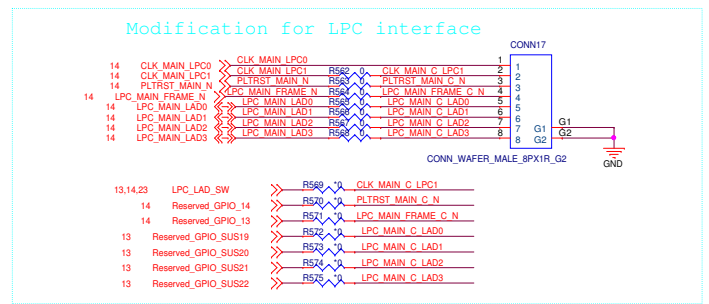
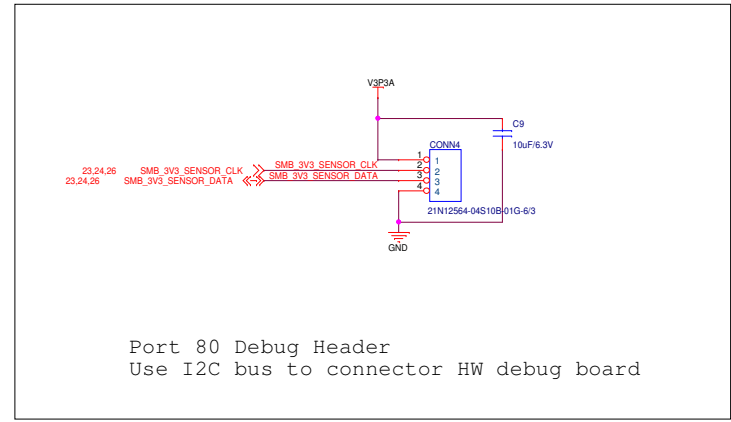
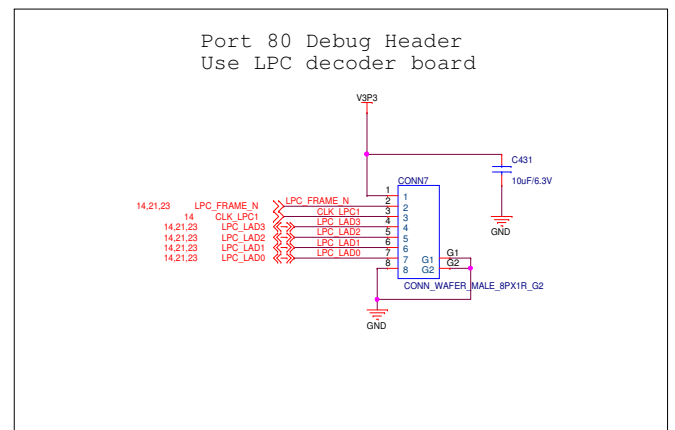
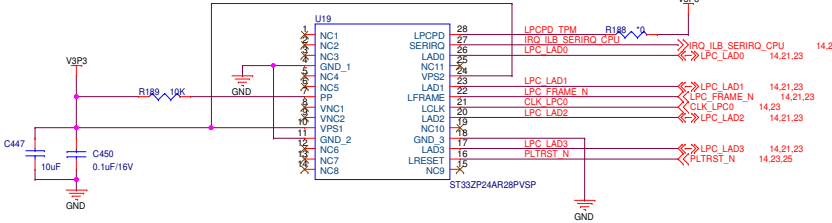
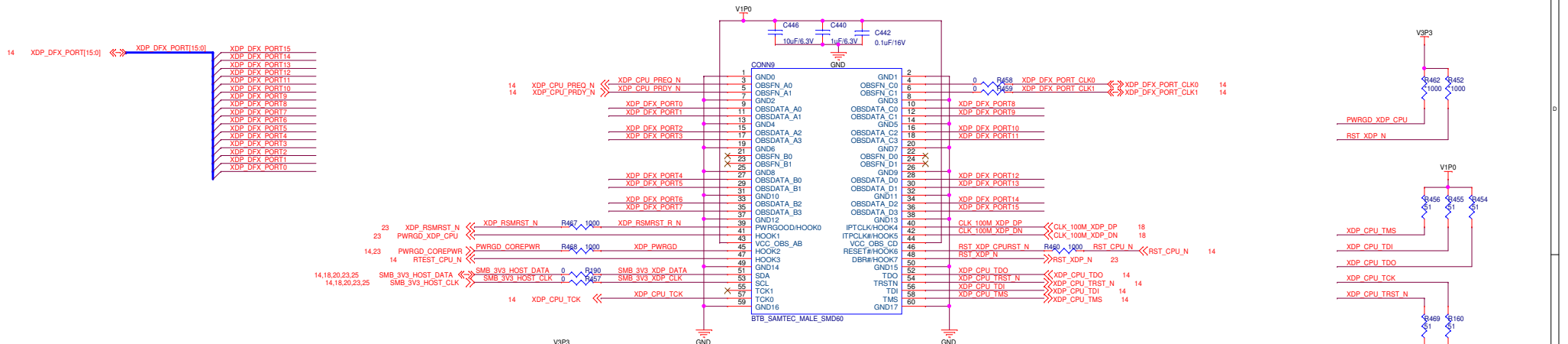


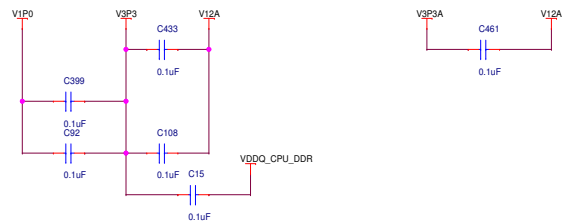
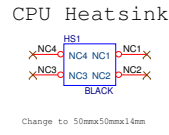
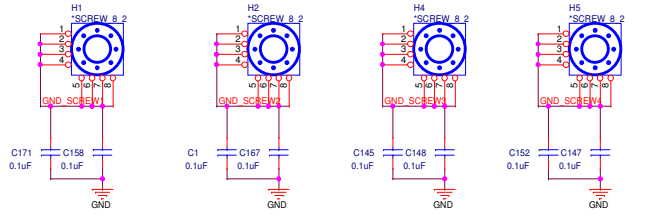
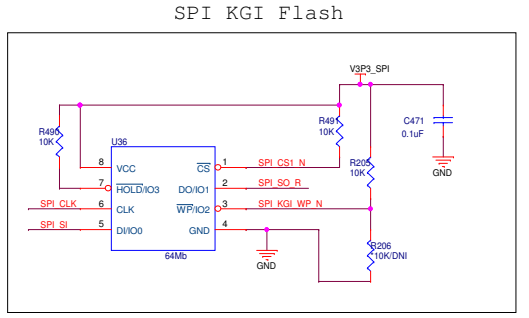
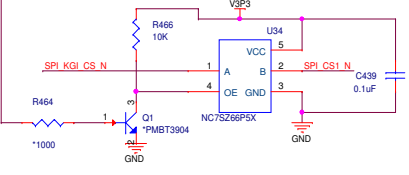
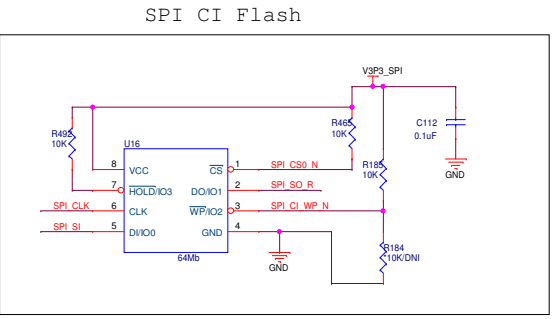
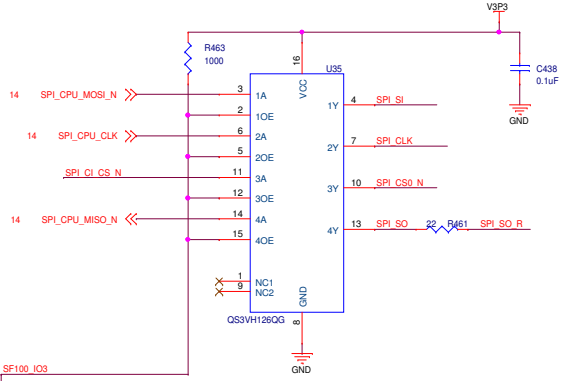
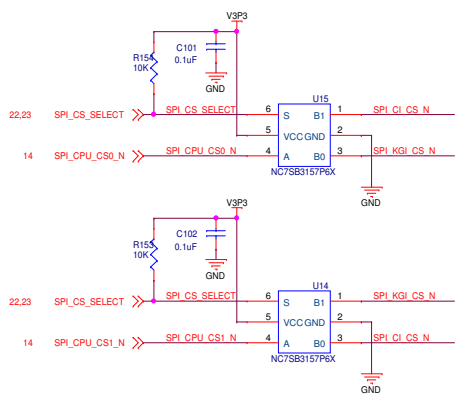
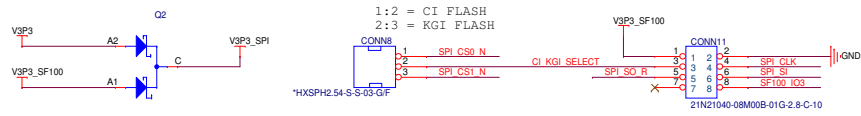
Address = 0x52

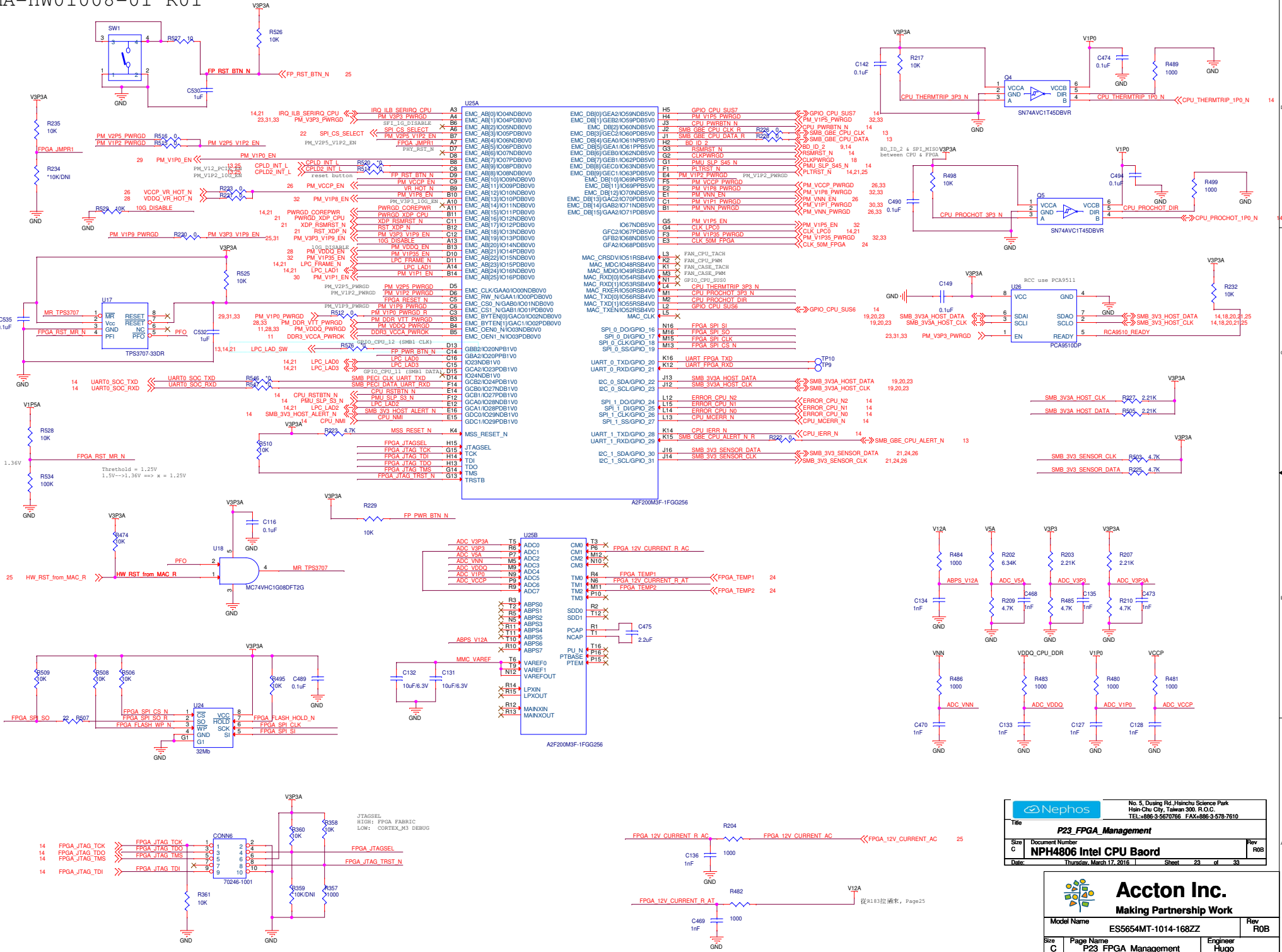
H = 5.2mm



Address = 0x53



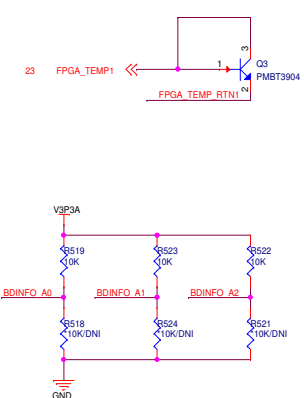
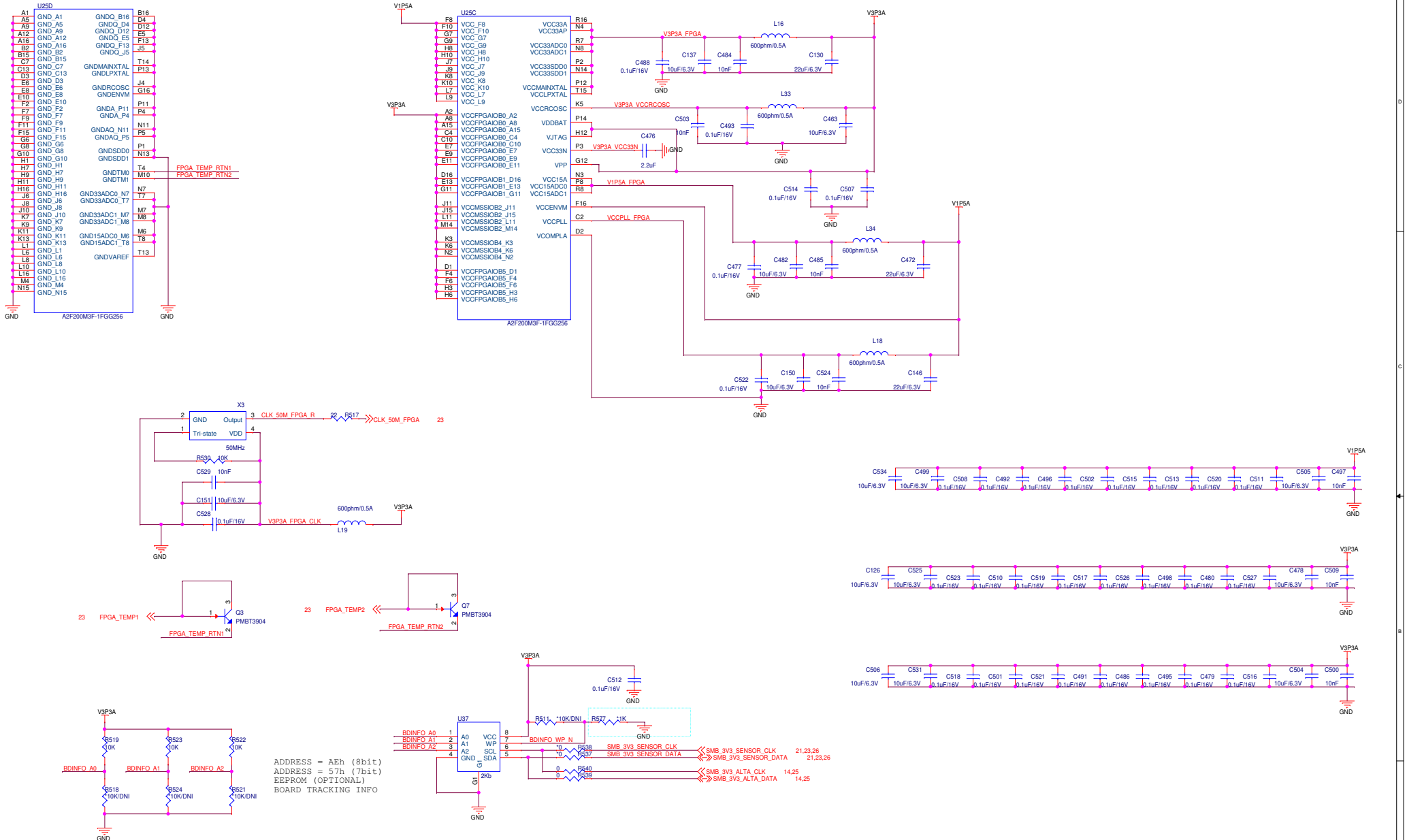




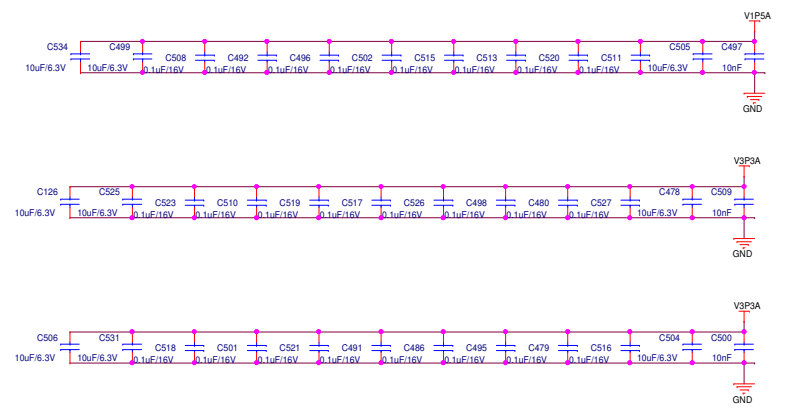
		No. 5, Duxing Rd., Hsinchu Science Park Hsin-Chu City, Taiwan 300, R.O.C. TEL: +886-3-5670766 FAX: +886-3-5787610	
Title: P23 FPGA Management			
Size C	Document Number	Rev	
	NPH4806 Intel CPU Board	ROB	
Date:	Thursday, March 17, 2016	Sheet	23 of 33

		Accton Inc. Making Partnership Work	
Model Name	ES5654MT-1014-168ZZ		Rev
			ROB
Size C	Page Name	Engineer	
	P23 FPGA Management	Hugo	
Date:	Thursday, March 17, 2016	Sheet	23 of 33

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ADDRESS = AEh (8bit)
 ADDRESS = 57h (7bit)
 EEPROM (OPTIONAL)
 BOARD TRACKING INFO

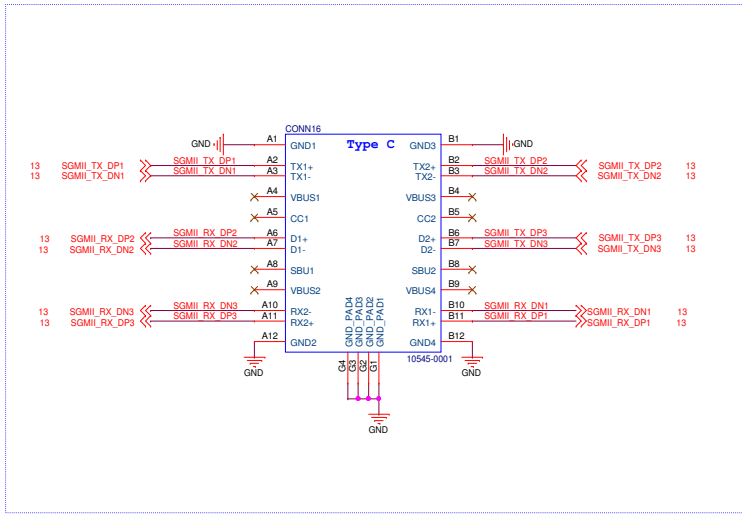
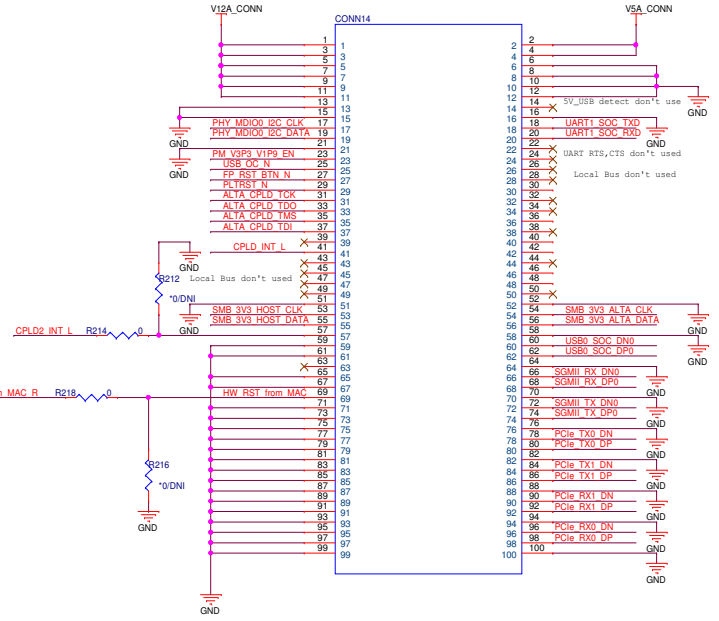
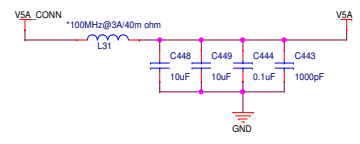
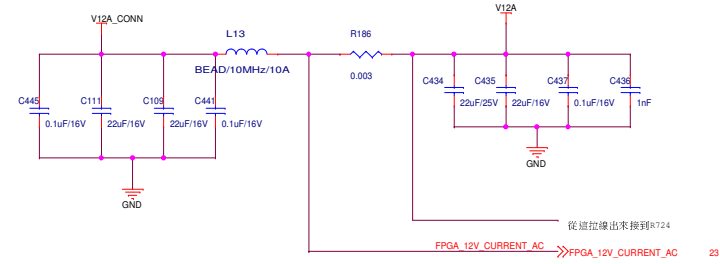
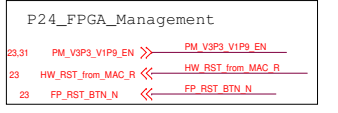
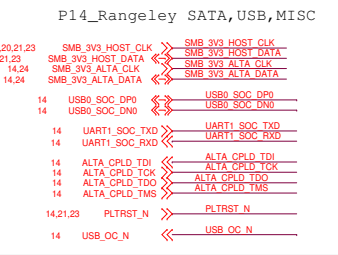
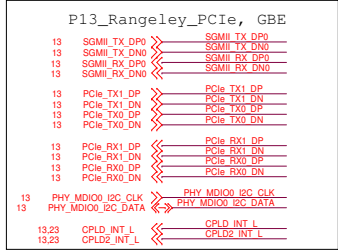


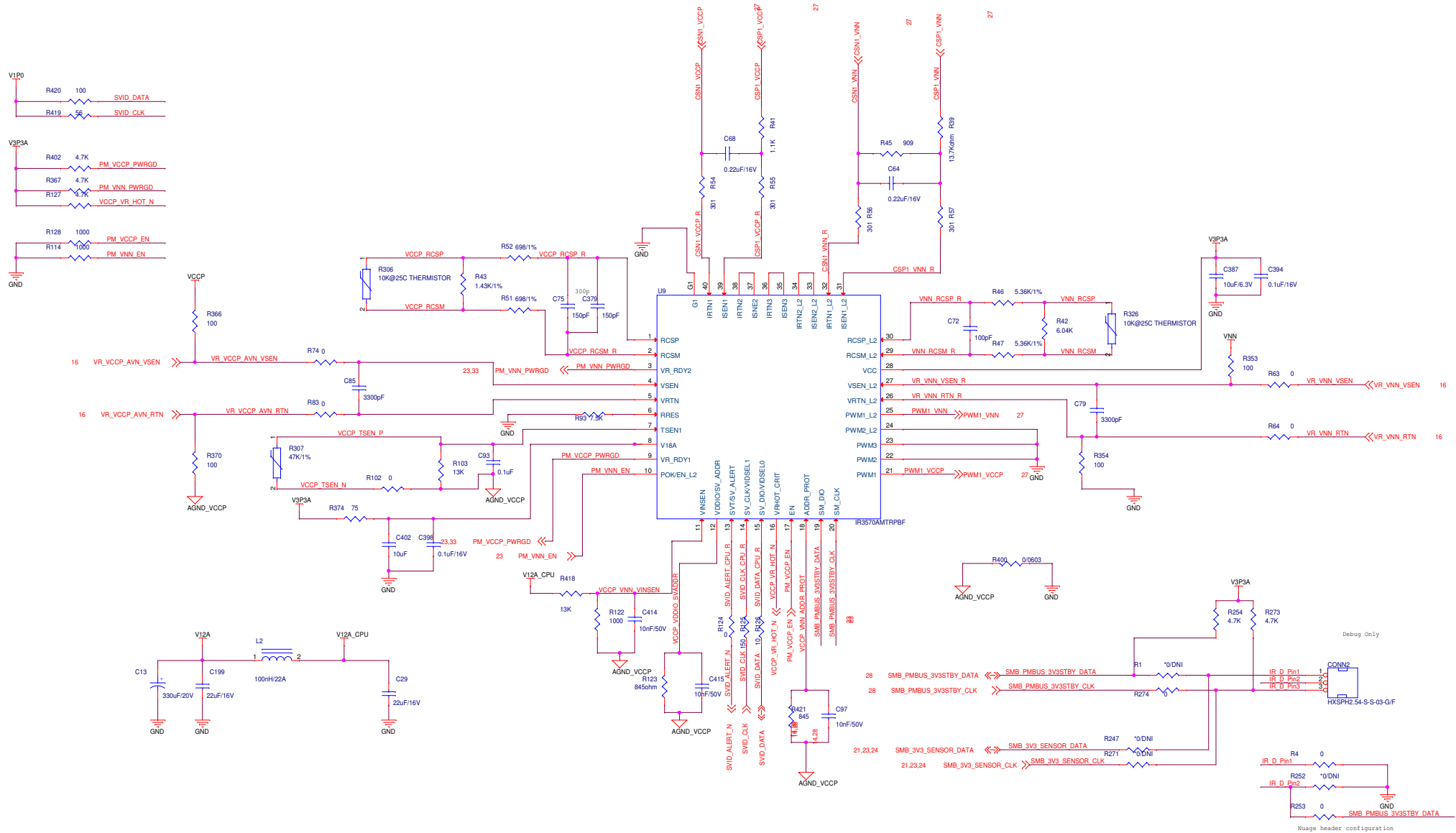
		No. 5, Daxing Rd., Hsinchu Science Park Hsin-Chu City, Taiwan 300, R.O.C. TEL.: 886-3-5670766 FAX: 886-3-578-7610	
Title P24_FPGA_POWER			
Size C	Document Number NPH4806 Intel CPU Board	Rev R06	
Date:	Thursday, March 17, 2016	Sheet 24	of 33

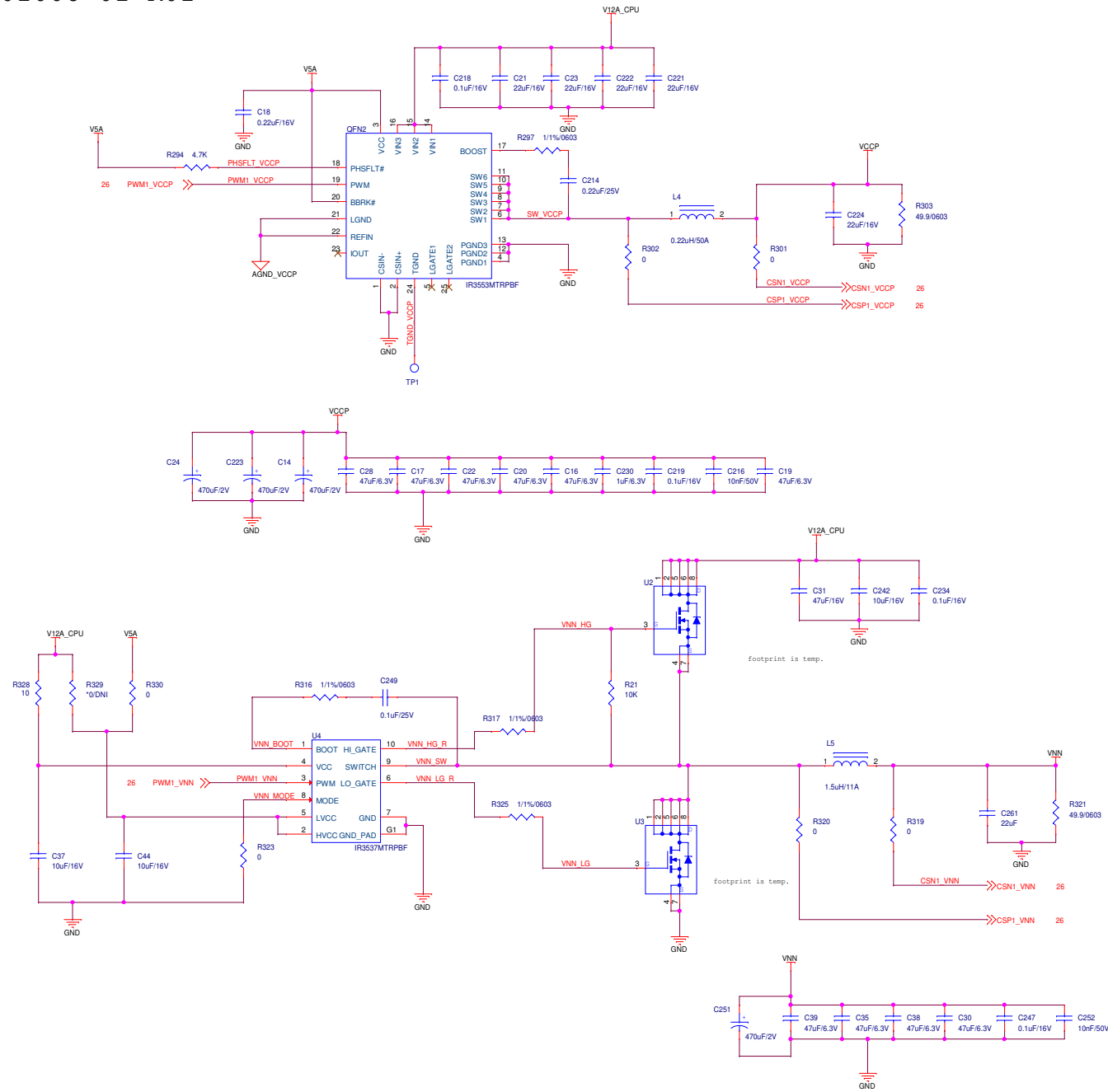
Accton Inc.
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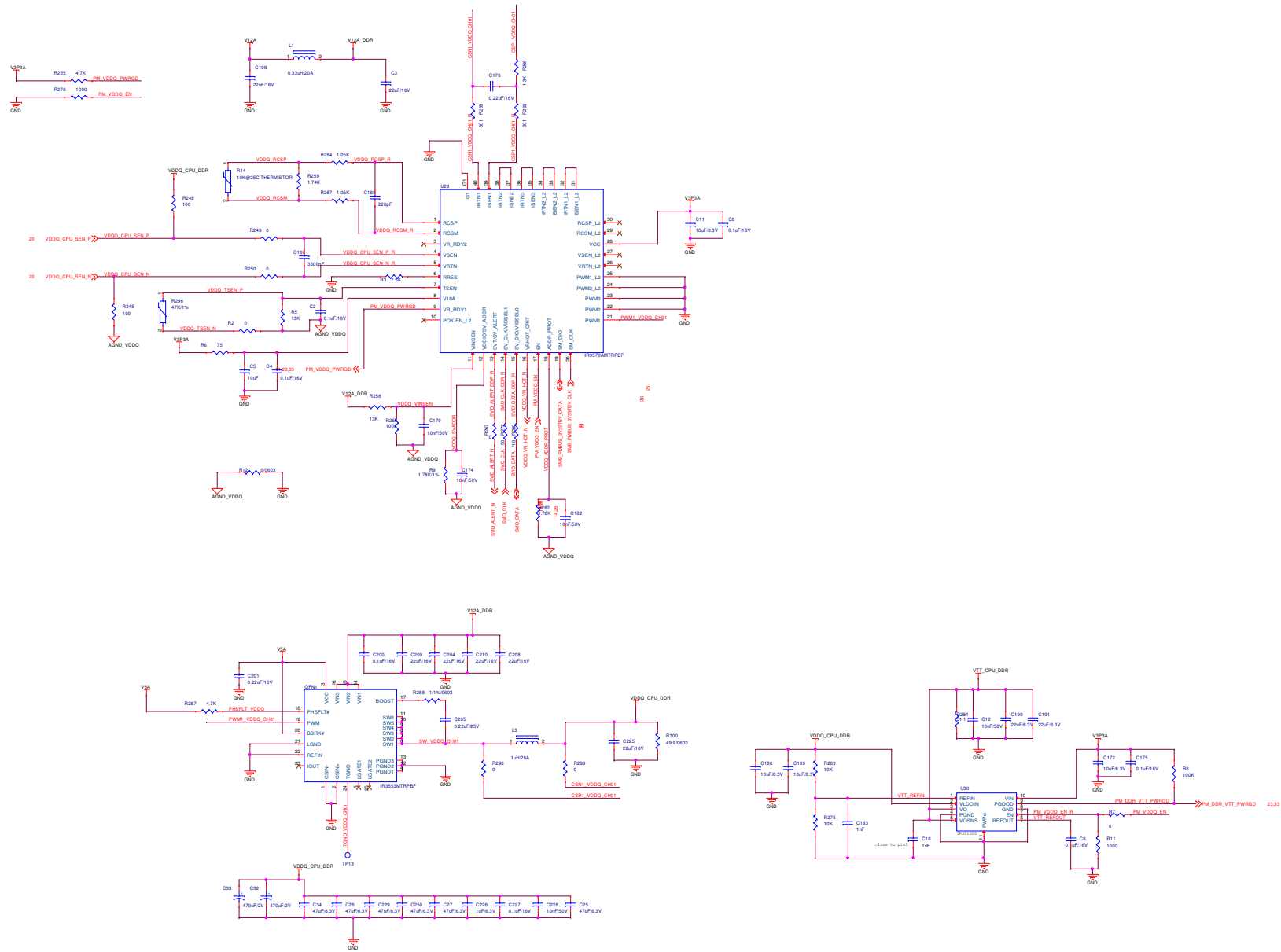
Model Name	ES5654MT-1014-168ZZ	Rev	R0B
Size C	Page Name P24_FPGA_POWER	Engineer	Hugo
Date:	Thursday, March 17, 2016	Sheet	24 of 33

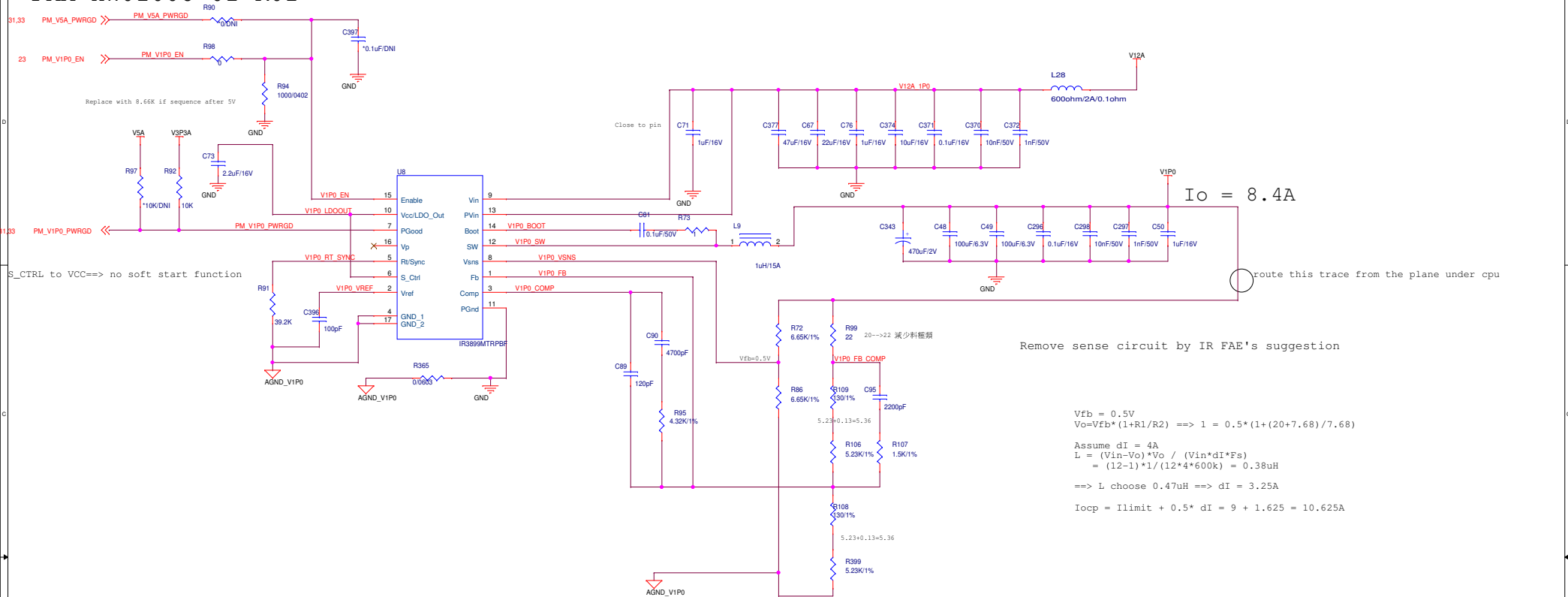
Resistor	96+0	96+8	48+6	32x40
R467	DI (Yes)	DNI (NO)	DNI (NO)	DNI (NO)
R495	DI (Yes)	DNI (NO)	DNI (NO)	DNI (NO)
R476	DNI (NO)	DI (Yes)	DI (Yes)	DI (Yes)
R477	DNI (NO)	DI (Yes)	DI (Yes)	DI (Yes)











$I_O = 8.4A$

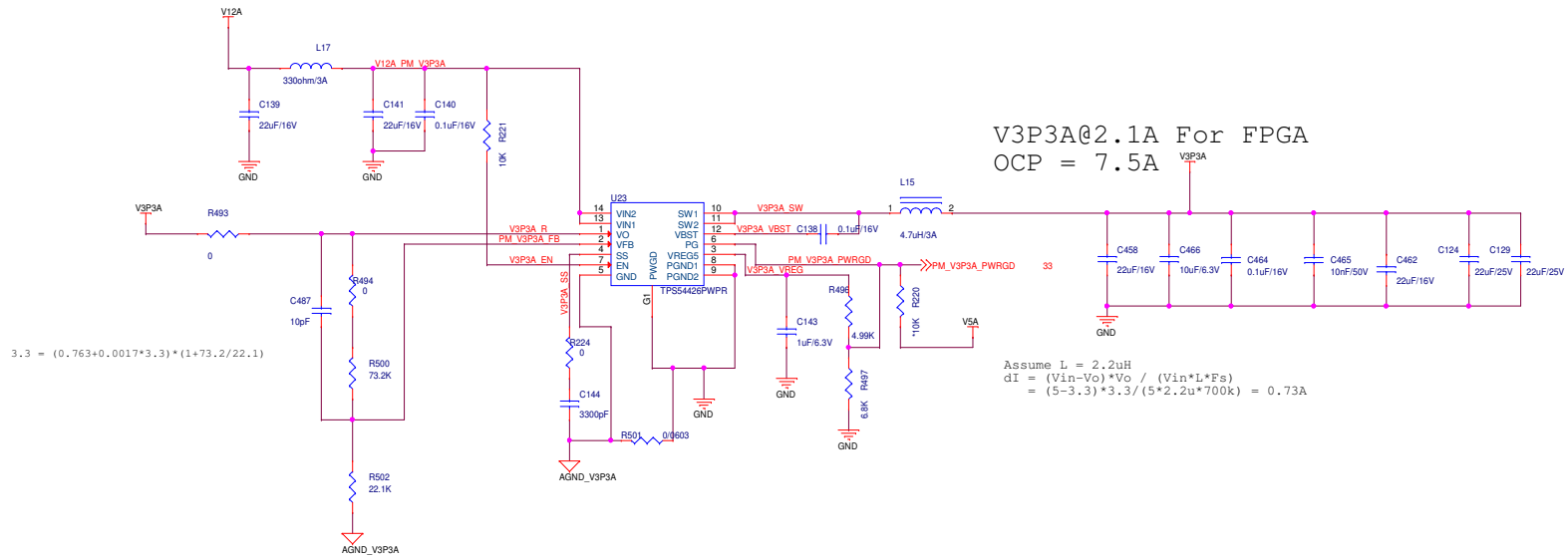
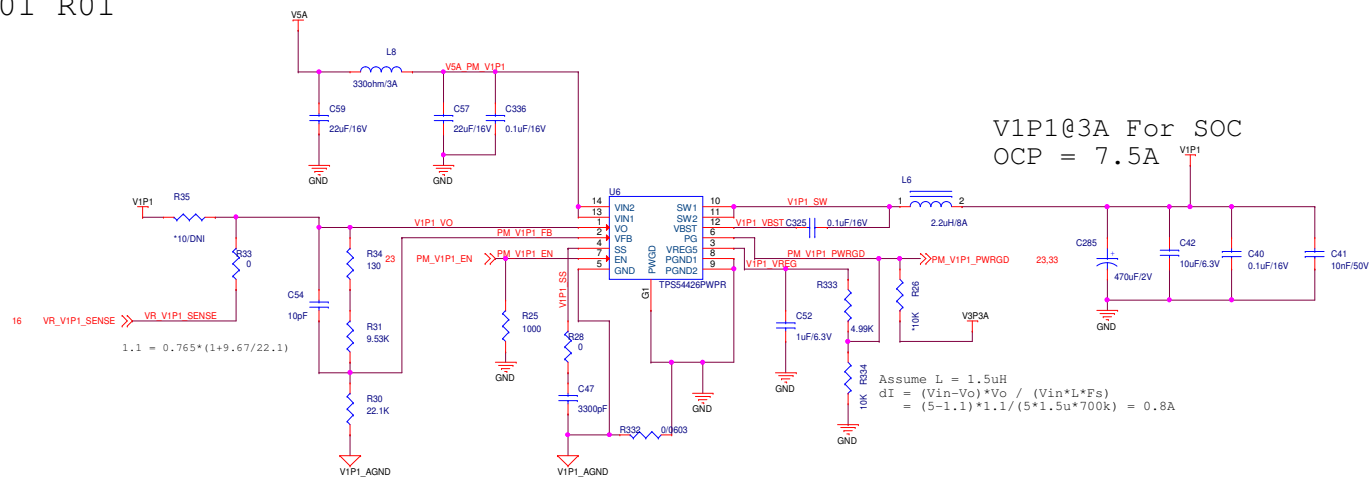
route this trace from the plane under cpu

Remove sense circuit by IR FAE's suggestion

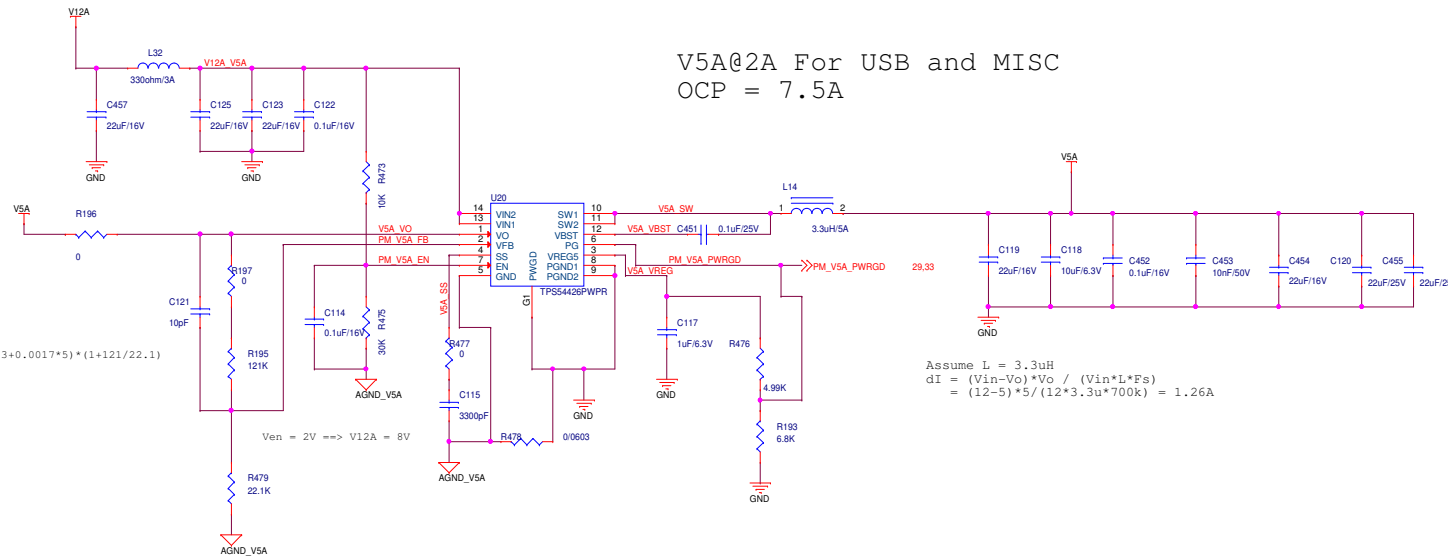
$V_{fb} = 0.5V$
 $V_o = V_{fb} * (1 + R1/R2) \implies 1 = 0.5 * (1 + (20 + 7.68) / 7.68)$
 Assume $dI = 4A$
 $L = (V_{in} - V_o) * V_o / (V_{in} * dI * F_s)$
 $= (12 - 1) * 1 / (12 * 4 * 600k) = 0.38\mu H$
 $\implies L$ choose $0.47\mu H \implies dI = 3.25A$
 $I_{ocp} = I_{limit} + 0.5 * dI = 9 + 1.625 = 10.625A$

S_CTRL to VCC==> no soft start function

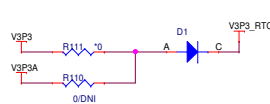
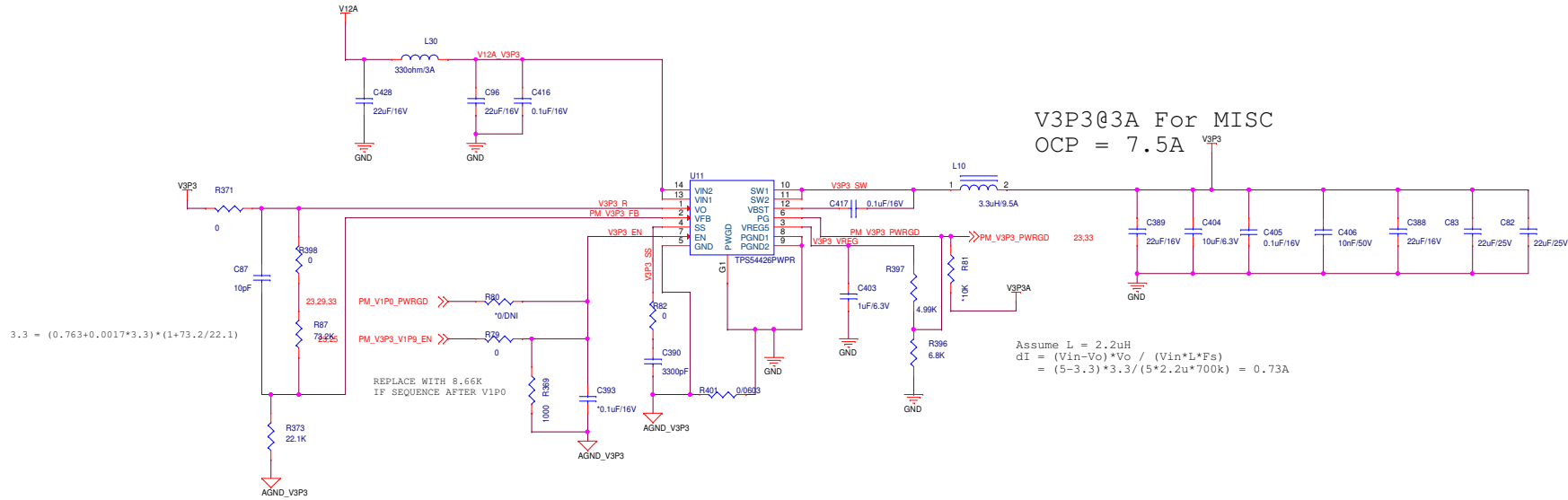
Replace with 8.66K if sequence after 5V

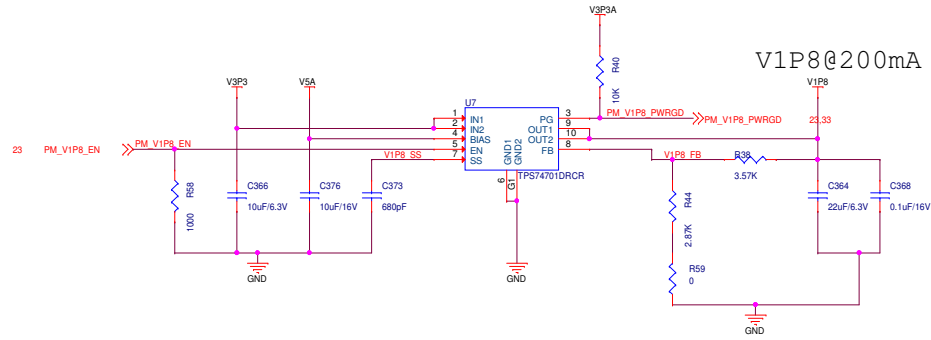


V5A@2A For USB and MISC
OCP = 7.5A

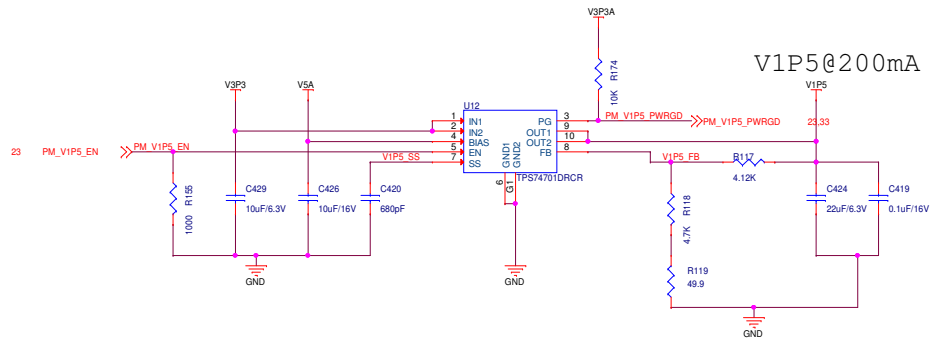


V3P3@3A For MISC
OCP = 7.5A

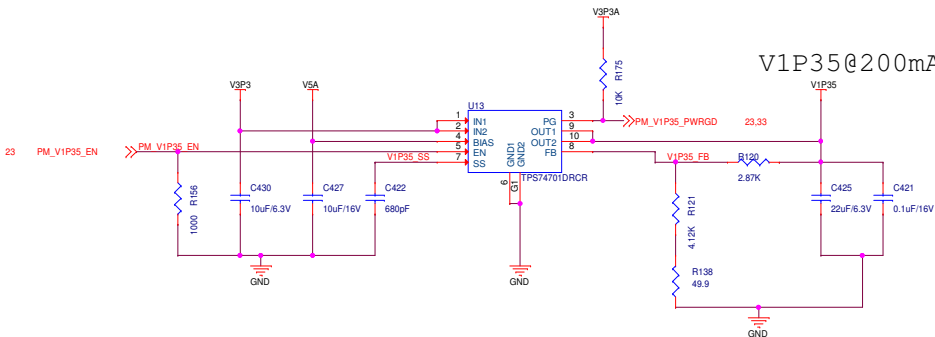




$$1.8 = 0.8 * (1 + 3.57 / 2.87)$$

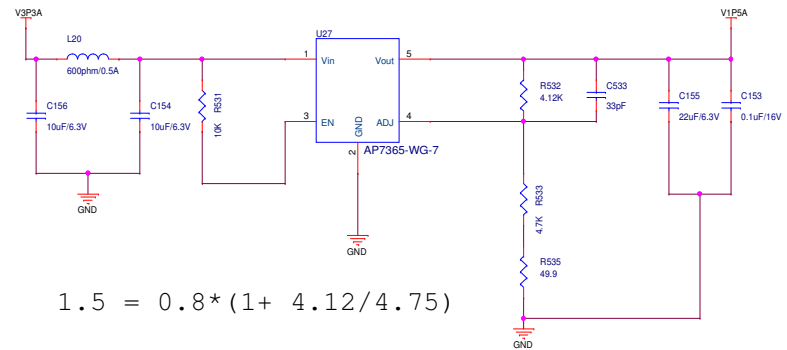


$$1.5 = 0.8 * (1 + 4.12 / 4.75)$$



$$1.35 = 0.8 * (1 + 2.87 / 4.12)$$

V1P5A@300mA for FPGA



$$1.5 = 0.8 * (1 + 4.12 / 4.75)$$

Sequence

1. V5A / V3P3A
2. V1P5A
3. V1P0
4. V1P1 / VDDQ/VTT...else power

