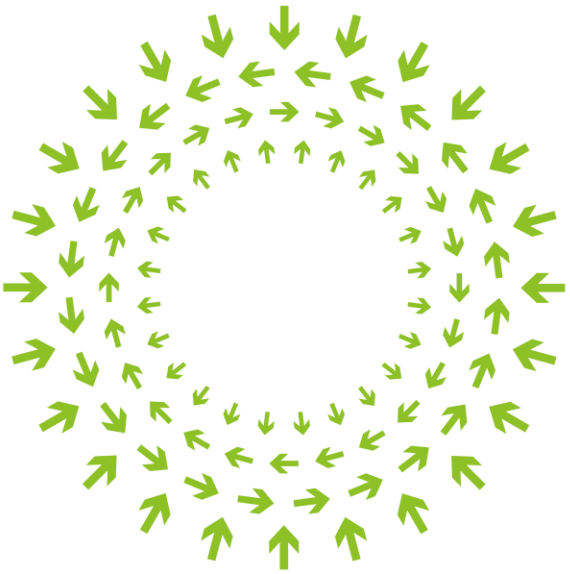

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Compute Project

Honey Badger – Light Weight Compute Module in Open Vault Storage V0.7

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1 Contents

2 Scope

This document describes the technical specifications used in the design of a light weight compute module for the Open Vault Storage of Open Compute Project, known as the Honey Badger.

3 Overview

When data center design and hardware design move in concert, they can improve efficiency and reduce power consumption. To this end, the Open Compute Project is a set of technologies that reduces energy consumption and cost, increases reliability and choice in the marketplace, and simplifies operations and maintenance. One key objective is openness -- the project is starting with the opening of the specifications and mechanical designs for the major components of a data center, and the efficiency results achieved at facilities using Open Compute technologies.

A new component of this project is the Honey Badger, a light weight compute module that works in Open Vault Storage (Knox). By leveraging the Open Vault platform, Honey Badger turns Knox from a JBOD into a light weight storage server. It is a simple and cost-effective solution for those application software that don't request very strong compute capability. Honey Badger comes with a modularized design concept: by adopting the new version Micro-Server card, it maximizes the flexibility to accept different compute modules for different use cases, also enables the capability to upgrade the compute and the storage subsystem in different pace. For the network interface, Honey Badger also supports the same OCP mezzanine cards as the OCP servers: 10G Ethernet now and will be 40G Ethernet in future.

3.1 License

4 Honey Badger Overview

4.1 Overall Design Approach

The Honey Badger compute module design is based on an architecture that contains a baseboard and an add-in Micro-Server card.

- The add-in Micro-Server card should be compatible with the Micro-Server x16 card specification, supporting below interfaces in its configuration. Current design uses an Intel Avoton based Micro-Server card, known as Panther+.
    - One PCI-E x4 port
    - One PCI-E x8 port
    - One USB 2.0 port
    - One UART port
    - One I2C bus for management bridge IC (FPGA)
    - Four pins for slot ID (or hardware revision)
    - One pin for power button
    - One pin for system reset
- The baseboard is functioning as a storage host bus adapter (HBA) with 12G SAS solution. Major components on baseboard will be: 8 port SAS IOC, 24 port SAS expander which is also responsible for storage enclosure management, external Mini-SAS connector for expansion, PCI-E Mezz Card for 10GbE port, baseboard management controller (BMC) for system enclosure management, debug header, switch buttons, LEDs, etc.

Figure 1 shows the concept of Honey Badger baseboard and Panther+ Micro-Server card:

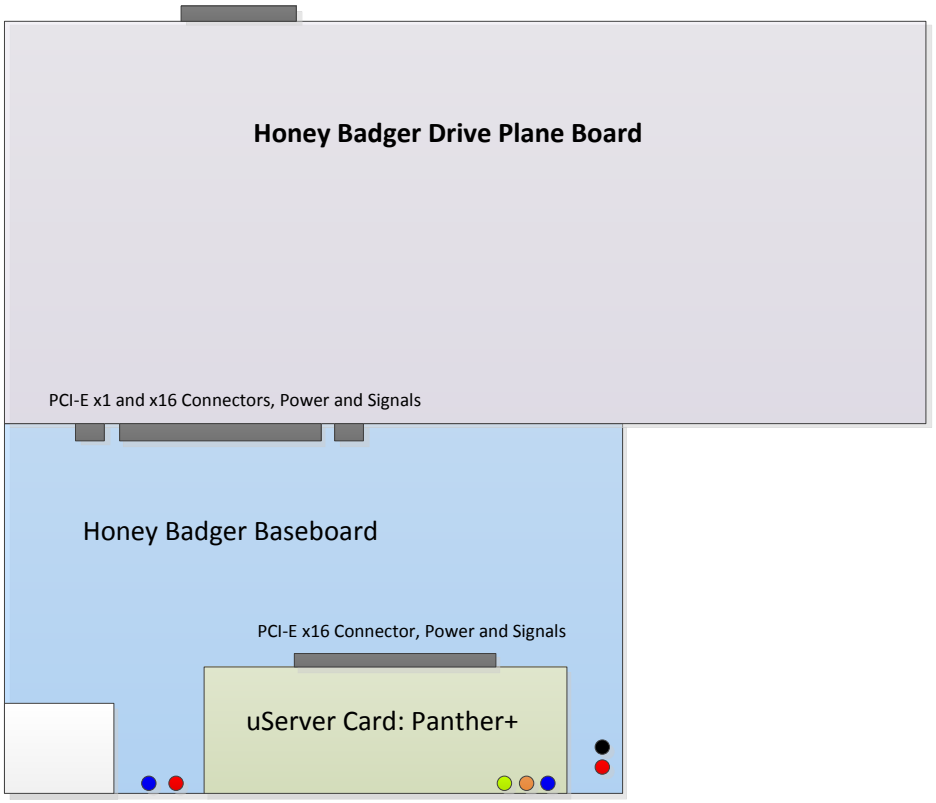

Figure 1 Honey Badger Compute Module Overview

Figure 2 shows an overview of the Honey Badger compute module in a Knox system.

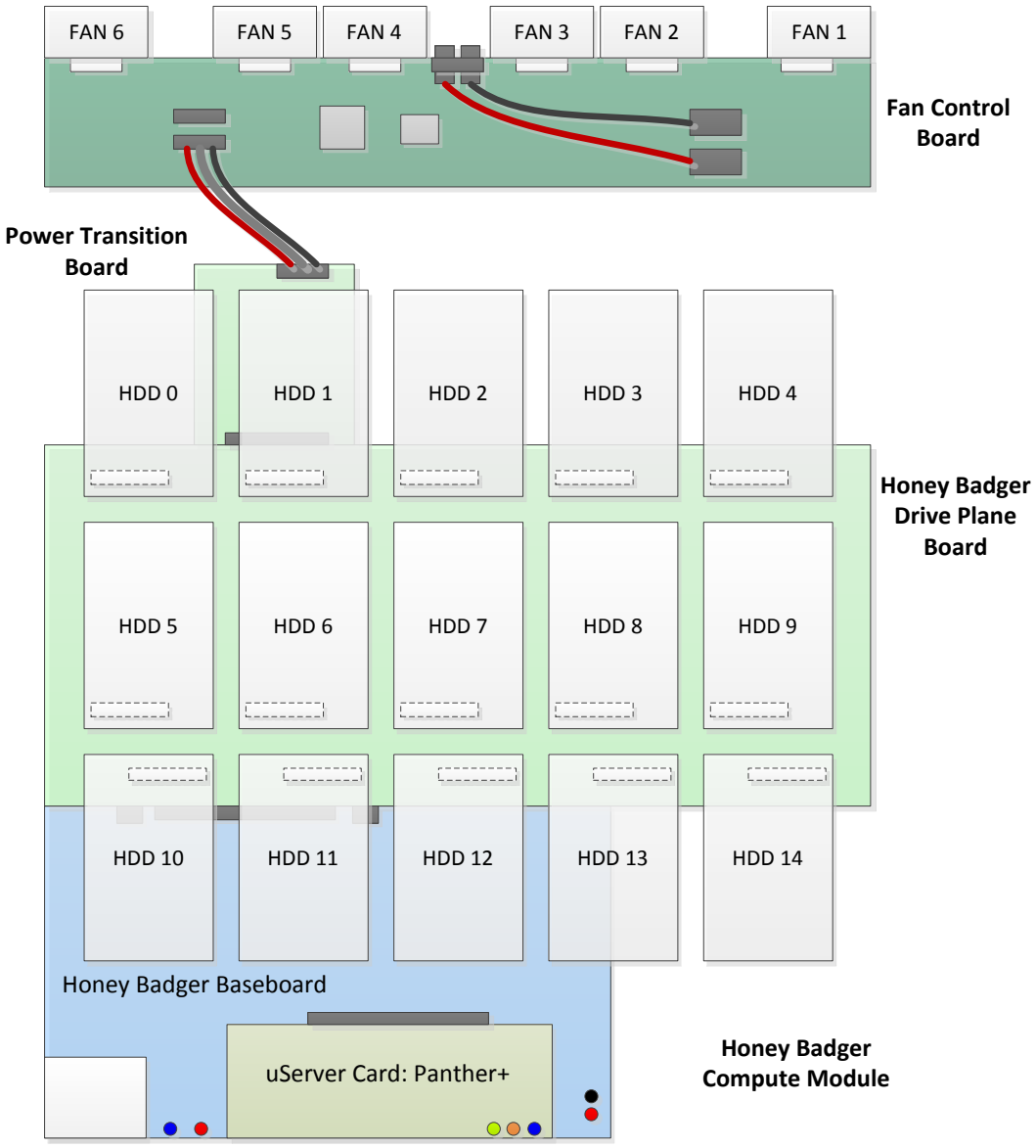

Figure 2 Honey Badger Compute Module in a Knox System

4.2 Key Accessible Items

The equipment accessible on the Panther+ card of Honey Badger includes:

- Up to four DDR3 ECC SO-DIMM slot, two on each side
- One mSATA SSD module, SATA3 interface
- One NGFF Flash card, SATA3 or PCI-E x4 interface (BOM Option)
- Three status LEDs for Micro-Server card information

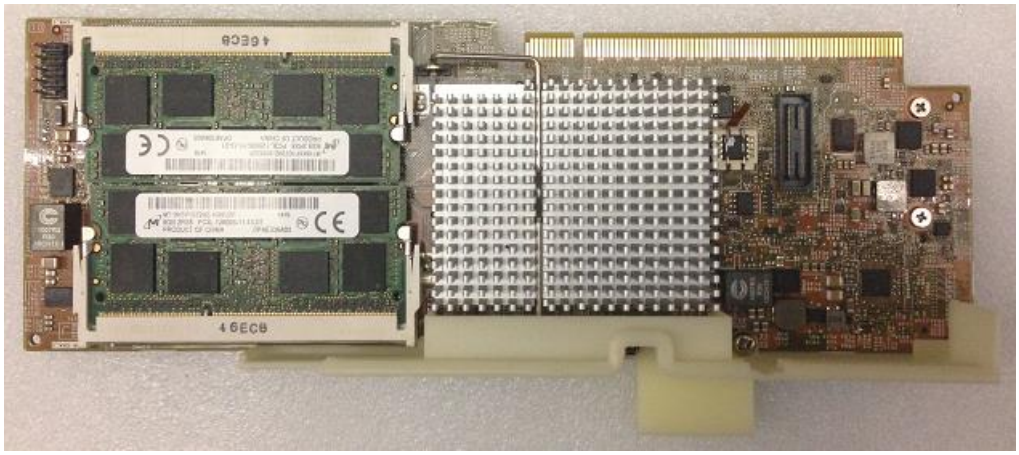

Figure 3 Key Accessible Items on Panther+ Micro-Server Card, Top Side

Figure 4 Key Accessible Items on Panther+ Micro-Server Card, Bottom Side

The equipment accessible from the front of the Honey Badger baseboard includes:

- One External Mini-SAS Conn (SFF-8088 form factor)
- One Internal Mini-SAS Conn (SFF-8087 form factor), with Status LED
- One 10GbE port (SFP+ form factor, with Link / Activity Status LEDs)
- One USB 2.0 port
- One OCP Debug Header, with slide switch and LED indicator
- Two Switch Buttons for power and reset
- Two Status LEDs for system information

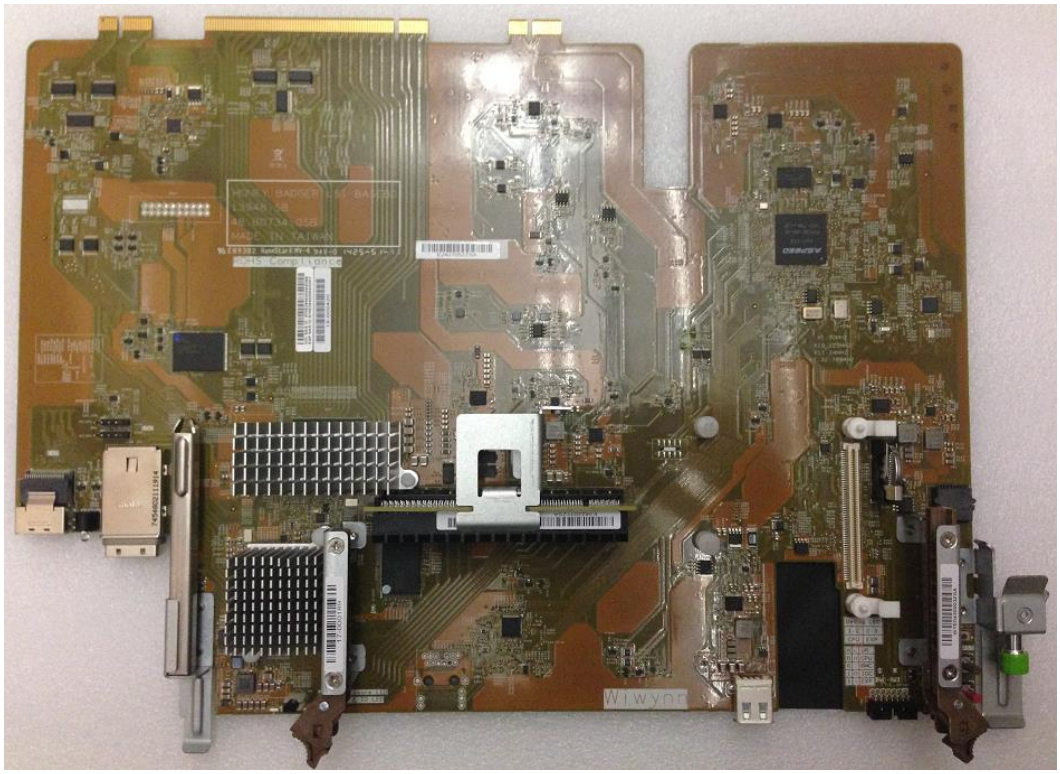

Figure 5 Key Accessible Items on Honey Badger Baseboard

4.3 Functional Block Diagram

There are two solutions for the storage sub-system design on Honey Badger baseboard as below. They are dual-sourced to each other. So far solution 1 is the POR configuration, while solution 2 has also been developed and verified by the vendors.

- Solution 1: Based on Avago / LSI 12G SAS IOC and 12G SAS Expander. The part number of the 8-port IOC is *LSI SAS3008*, the part number of the 24-port expander is LSI *SAS3x24RLC1*.
- Solution 2: Based on PMC-Sierra 12G SAS IOC and 12G SAS expander. The part number of the 8-port IOC is *PM8074*, the part number of the 24-port expander is *PM8043*.

Figure 6 shows a high-level functional block diagram of Honey Badger, with an Avago / LSI 12G SAS controller and a SAS expander.

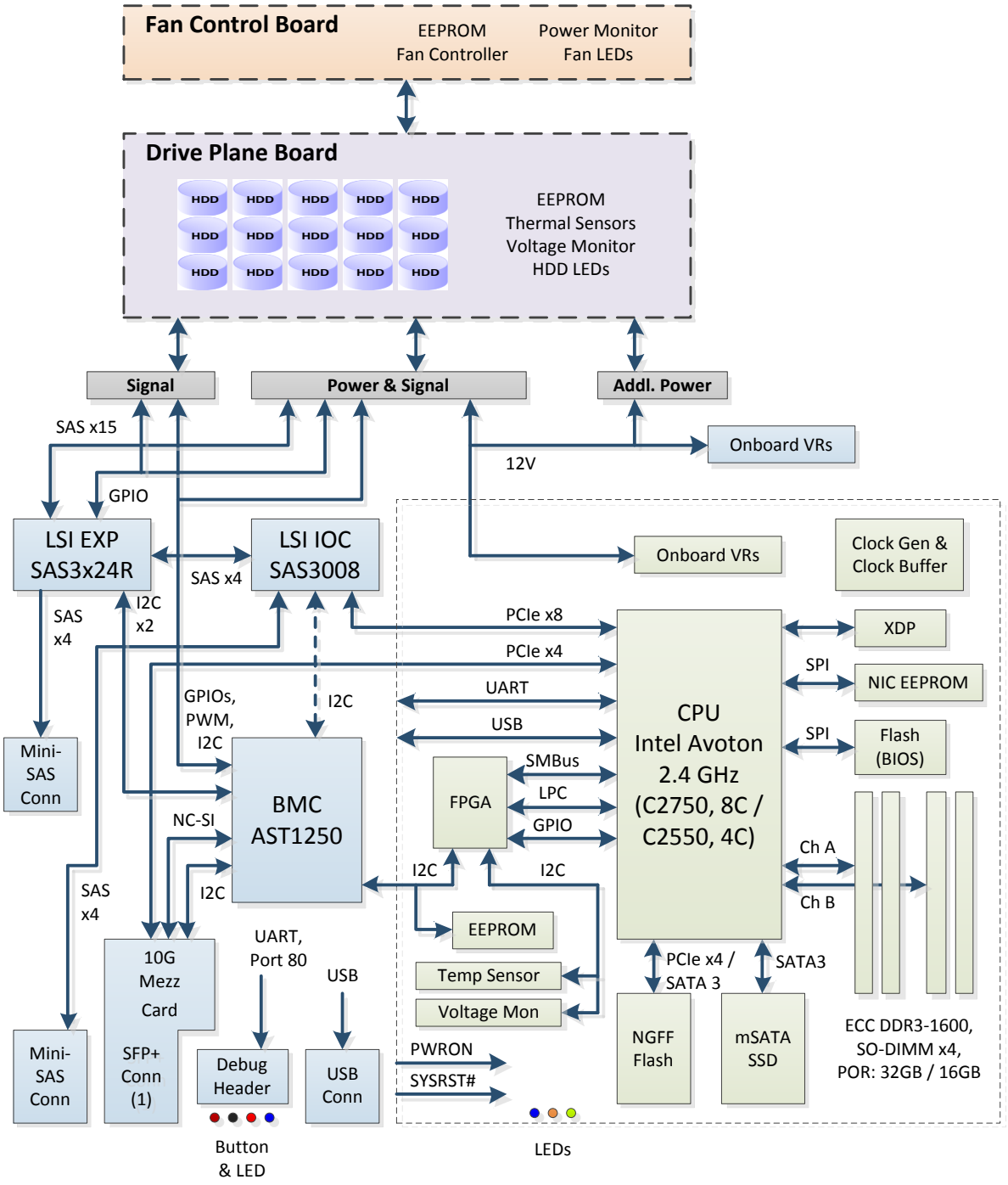

Figure 6 Honey Badger Functional Block Diagram, LSI solution

Figure 7 shows a high-level functional block diagram of Honey Badger, with a PMC-Sierra 12G SAS controller and a SAS expander.

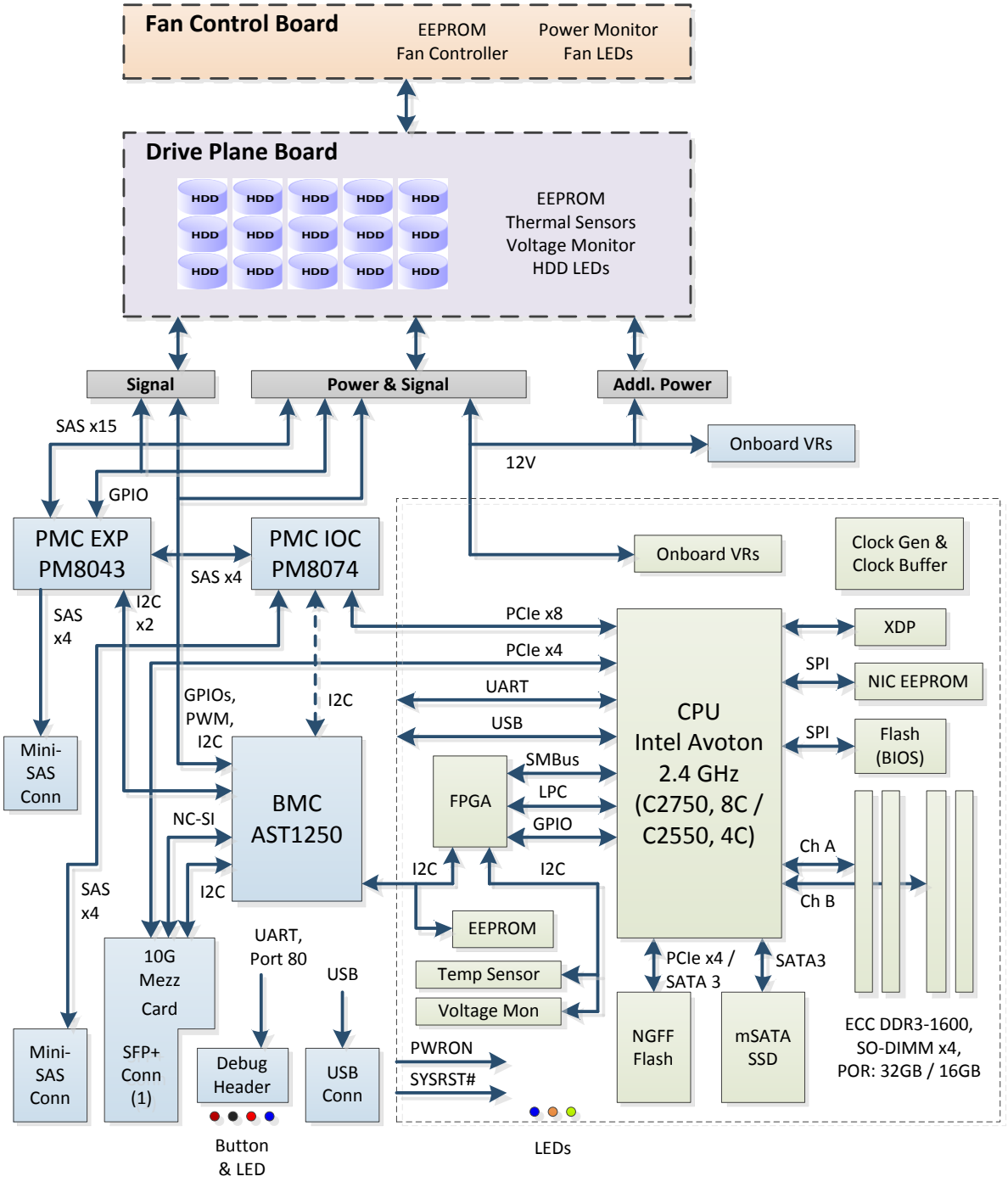

Figure 7 Honey Badger Functional Block Diagram, PMC solution

4.4 System Block Diagram

This section contains the system block diagrams for the Honey Badger compute module in a Knox system. It mainly addresses the PCI-E and SAS data paths. Each module has the following cable connectors, which are accessible from the cold aisle:

- One 10GbE port in SFP+ form factor, to top of rack switch
  - Passive copper Ethernet cable
  - Max cable length: TBD
- One external Mini-SAS port in SFF-8088 form factor. It is connected to the Knox SEB in another tray within the same Honey Badger system:
  - External mini-SAS cable
  - Max cable length: 7m
- One internal Mini-SAS port in SFF-8087 form factor. It is reserved to for cascading purpose (to connect Knox SEB in another system).
  - Internal mini-SAS cable
  - Max cable length: 1.5m

Figure 8 shows the typical use case of a 1:30 compute node to hard disk drive ratio:

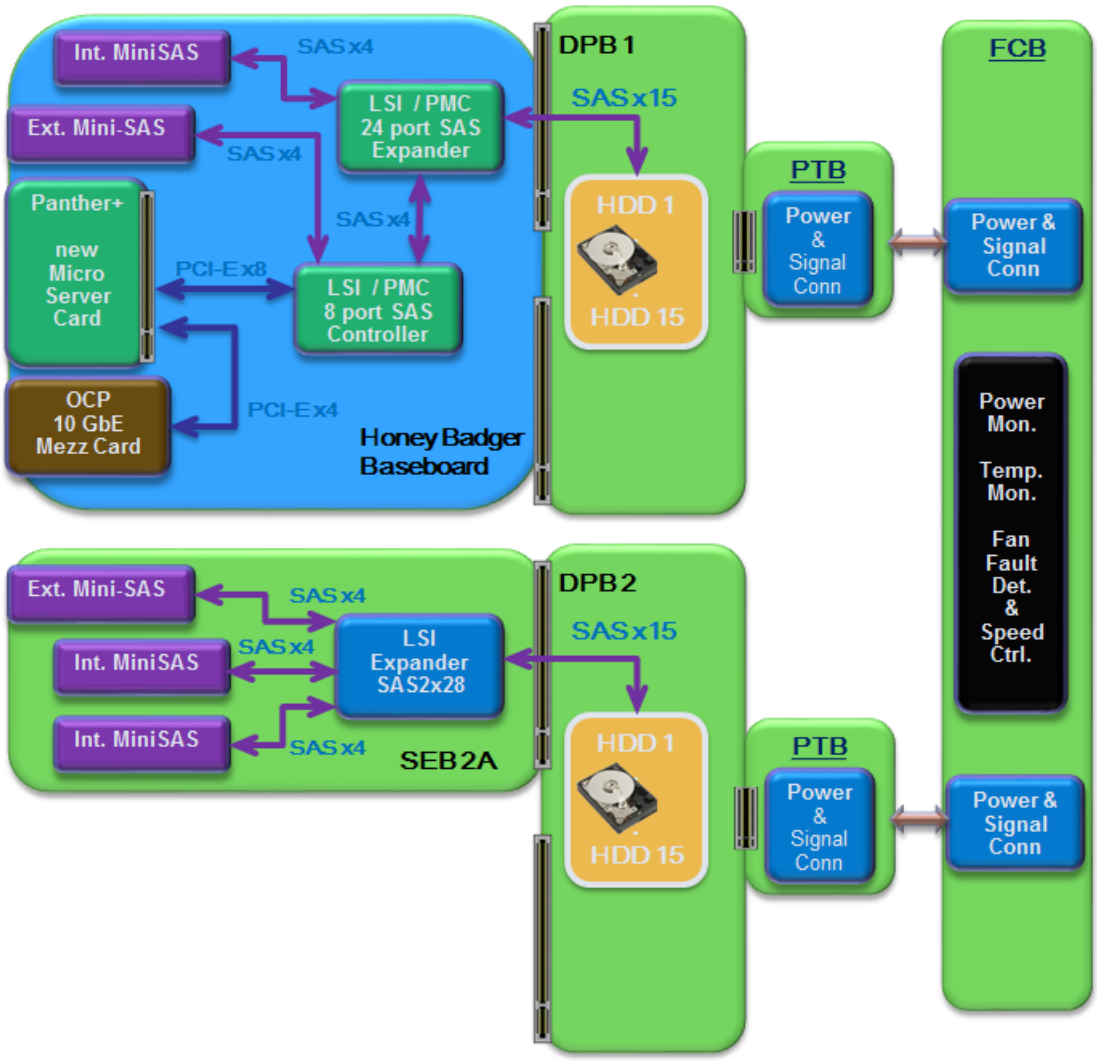

Figure 8 Honey Badger System Block Diagram (Use Case 1:30)

Note: According to the new Honey Badger tray design that to accept both Honey Badger baseboard and Knox SEB, the Knox SEB can only be placed on the A-side.

Figure 9 shows another typical use case of a 1:15 compute node to hard disk drive ratio:

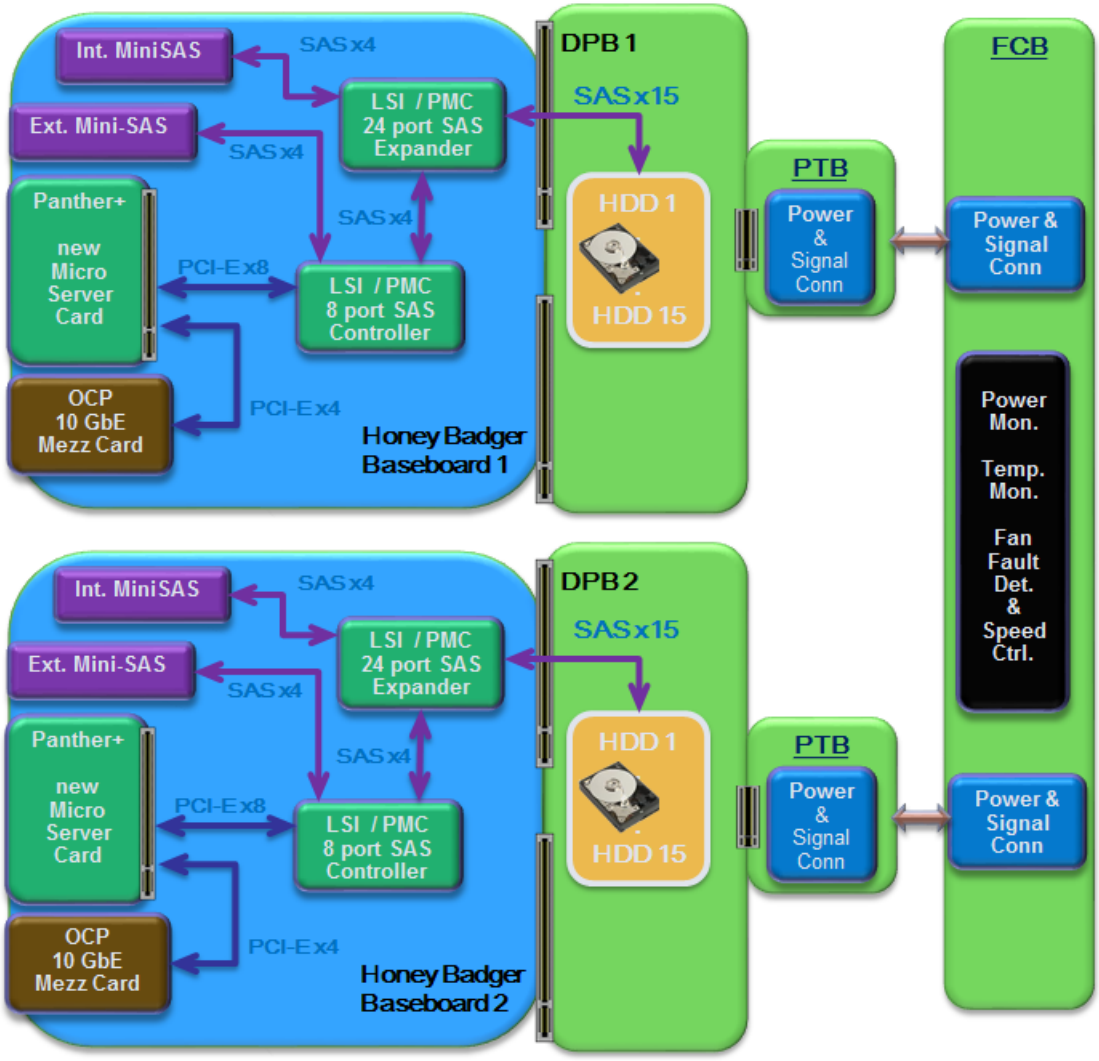

Figure 9 Honey Badger System Block Diagram (Use Case 1:15)

4.5 System I2C Topology

Figure 10 and Figure 11 show the system I2C topology of the Honey Badger compute module in a Knox system, with a 1:30 or 1:15 compute node to hard disk drive ratio, respectively. They show the enclosure management structure of the Honey Badger module and the system.

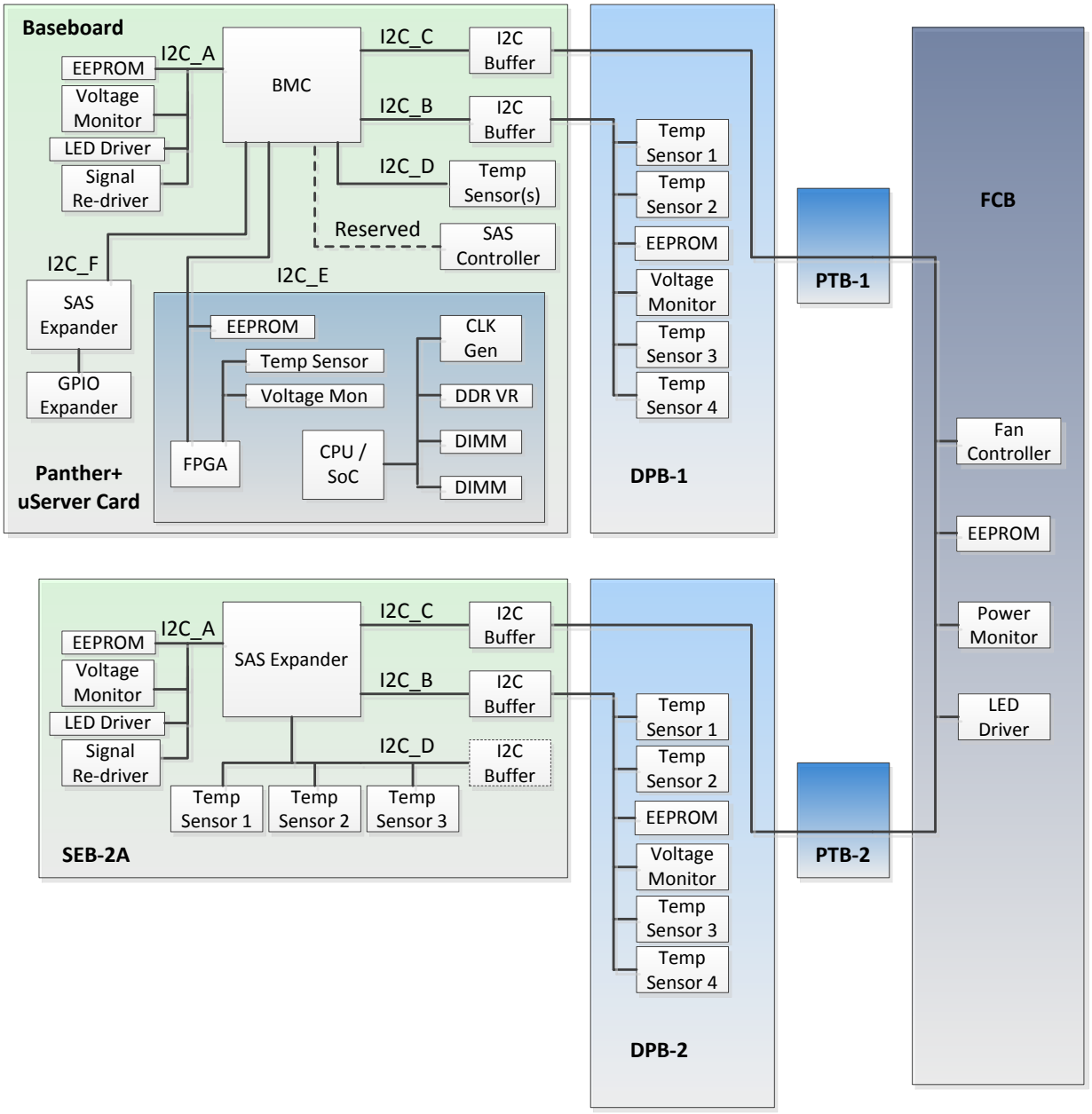

Figure 10 Honey Badger System I2C Topology (Use Case 1:30)

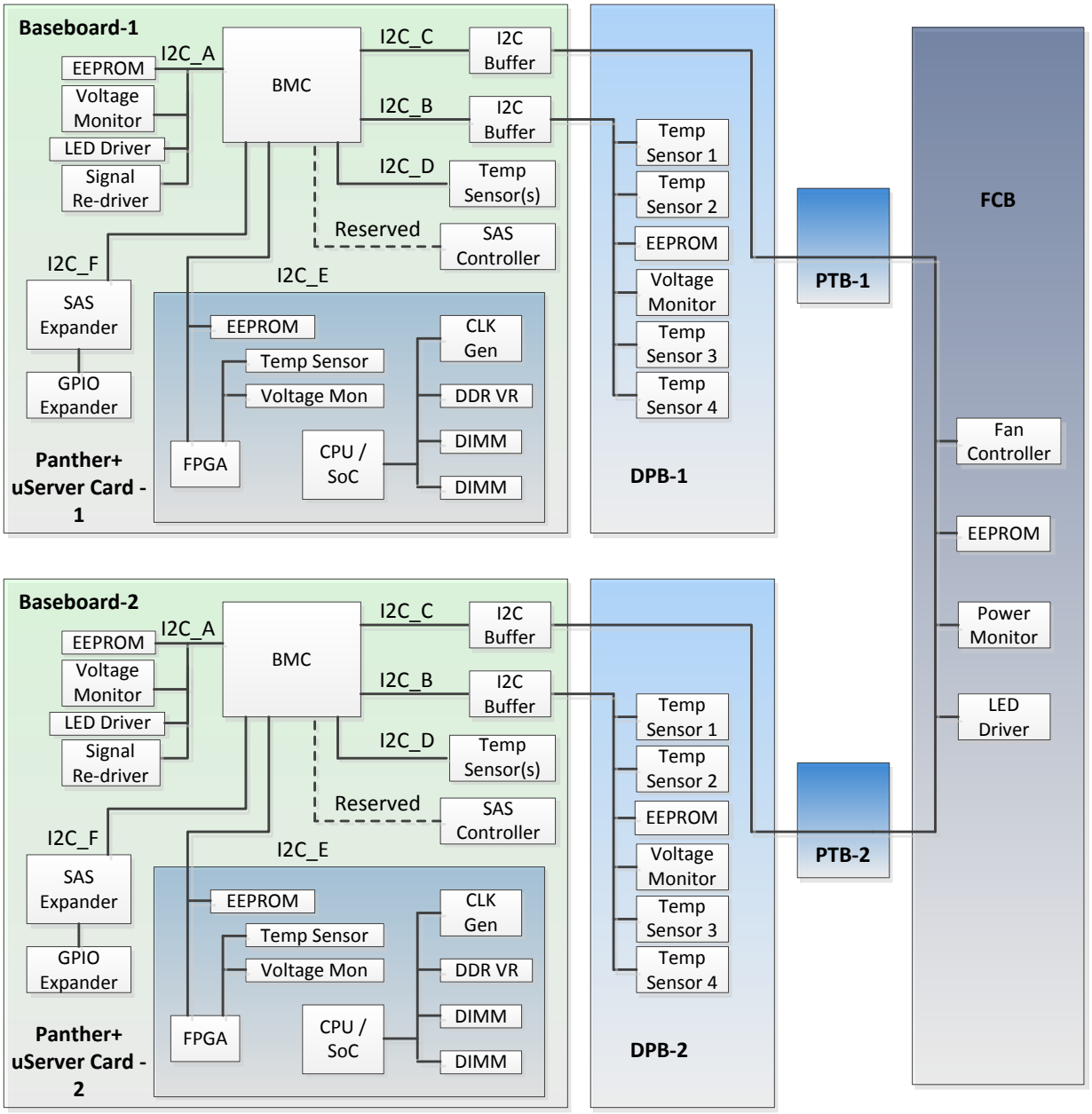

Figure 11 Honey Badger System I2C Topology (Use Case 1:15)

5 New Honey Badger Tray and DPB

5.1 Open Vault Storage Specification

Honey Badger system is based on the Open Vault Storage system, known as Knox. Relevant specification can be found on the Open Compute Project website:

- Open_Vault_Storage_Hardware_v0.8.pdf
- From: http://www.opencompute.org/projects/storage/
- Or: http://www.opencompute.org/wiki/Storage/Dev

5.2 Modifications on Honey Badger Tray

Below design changes have been made on Honey Badger tray from Knox tray, to accommodate to the new use case of Honey Badger:

- New card guide for Honey Badger baseboard which is wider than Knox SEB. Circled item in Figure 12 below.
- Shortened center card guide to accept both Honey Badger baseboard and Knox SEB. Circled item in Figure 13 below.
- Non-tilting tray / Fixed hinge to avoid interference between the upper tray and the lower tray when tilted down.

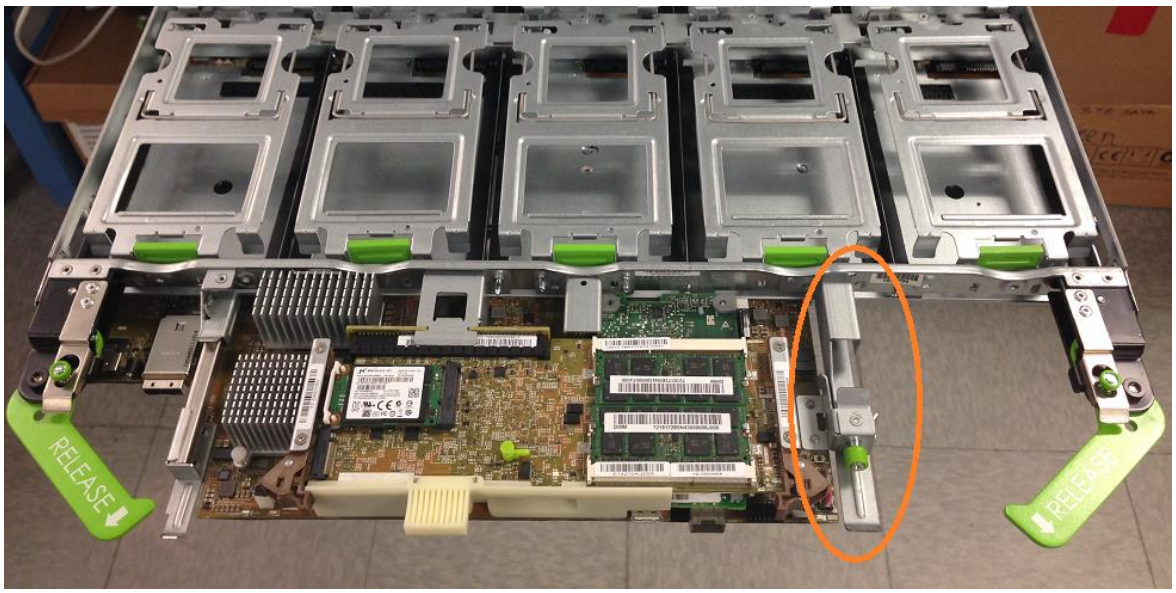

Figure 12 New Honey Badger Tray, Front View

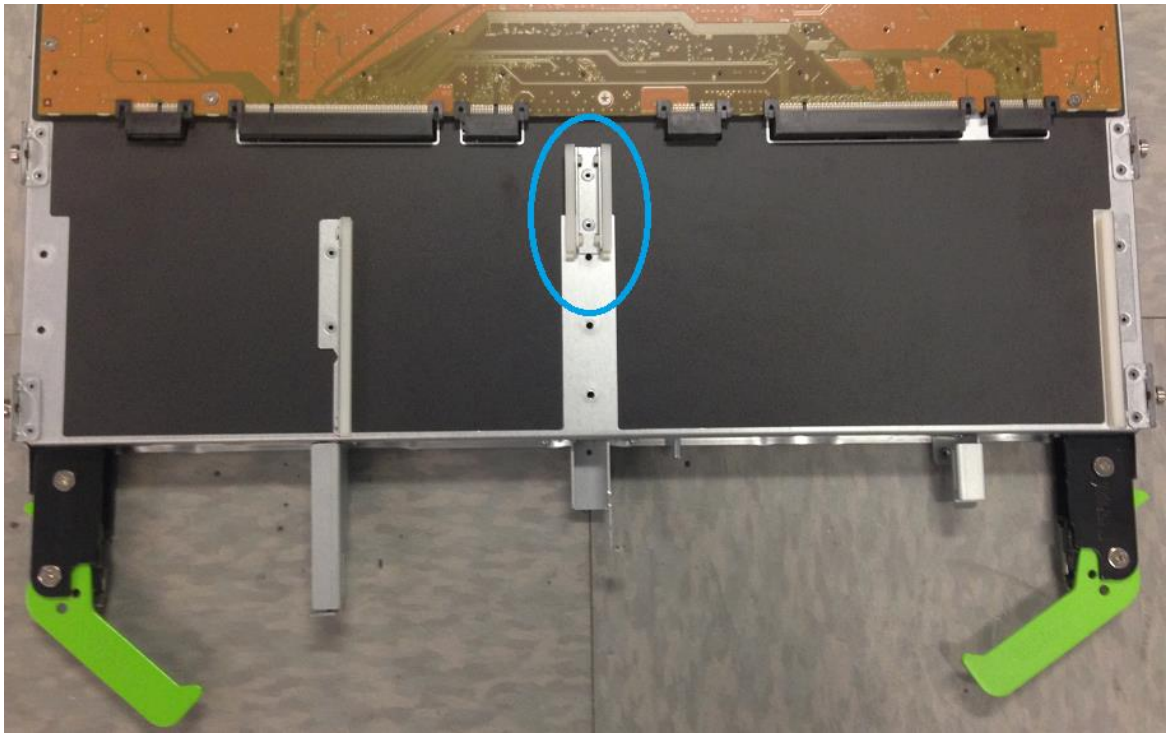

Figure 13 New Honey Badger Tray, Bottom View

5.3 Modifications on Honey Badger DPB

Below design changes have been made on Honey Badger DPB (Drive Plane Board) from Knox DPB, to accommodate to the new use case of Honey Badger:

- Add one PCI-E x1 connector to provide more power / current, on both A-side and B-side. Circled items in Figure 14.
- Adopting low loss PCB material, to reserve enough margin for SATA 6G signal integrity.

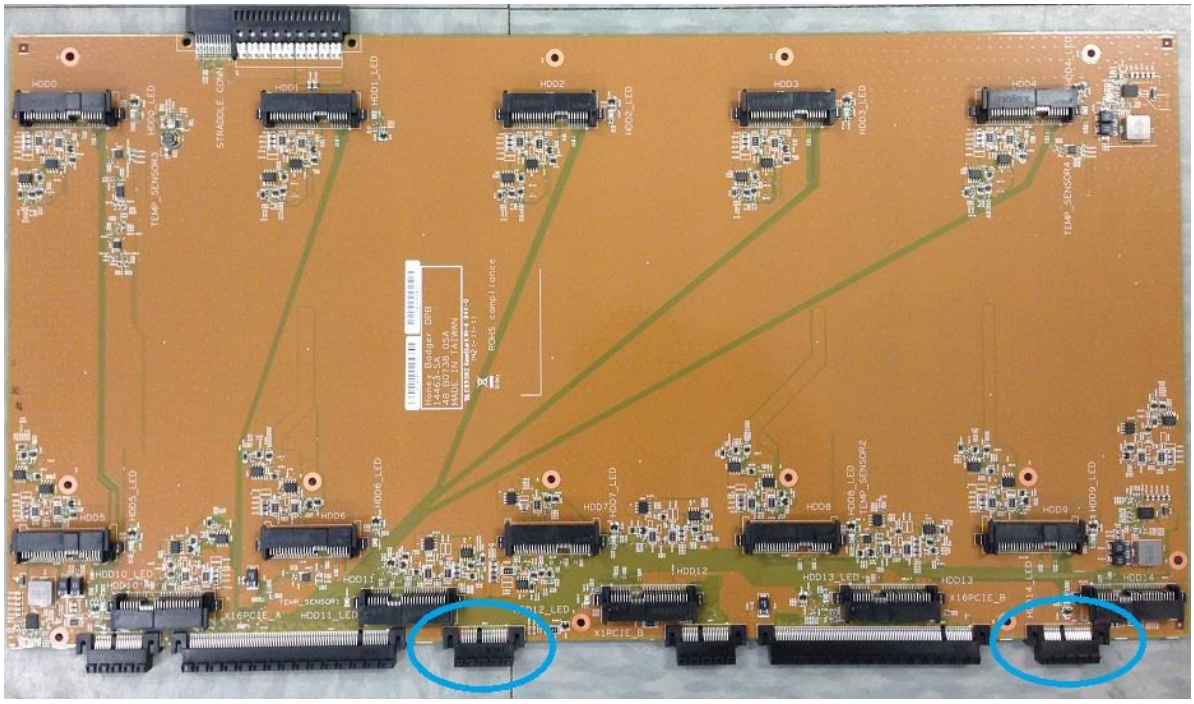

Figure 14 New Honey Badger DPB

6 Panther+ Card for Honey Badger

6.1 Micro-Server Card Specification

Honey Badger adopts Panther+ Micro-Server card as compute node, but it also accepts any other Micro-Server card that meets the requirements in Section 4.1. The general design specification for a standard Micro-Server card can be found on the Open Compute Project website:

- Open_Compute_Project_Micro-Server_Card_Specification_v0.7.pdf
- From: http://www.opencompute.org/projects/motherboard-design/
- Or: http://www.opencompute.org/wiki/Motherboard/SpecsAndDesigns

6.2 Panther+ Design Specifications

Panther+ is a Micro-Server card based on Intel Avoton SoC. It has been, and also will be applied to different platforms other than Honey Badger. The following sections highlight the high level design concepts of the Panther+ card in the Honey Badger compute module. For full design details, please refer to the specification for Panther+ on Open Compute Project website:

- Open_Compute_Project_Panther+_Specification_v0.7.pdf.
- From: http://www.opencompute.org/projects/motherboard-design/
- Or: http://www.opencompute.org/wiki/Motherboard/SpecsAndDesigns

6.3 Panther+ Block Diagram

Figure 15 illustrates the functional block diagram of the Panther+ card. The dot-lined features are not used in Honey Badger.

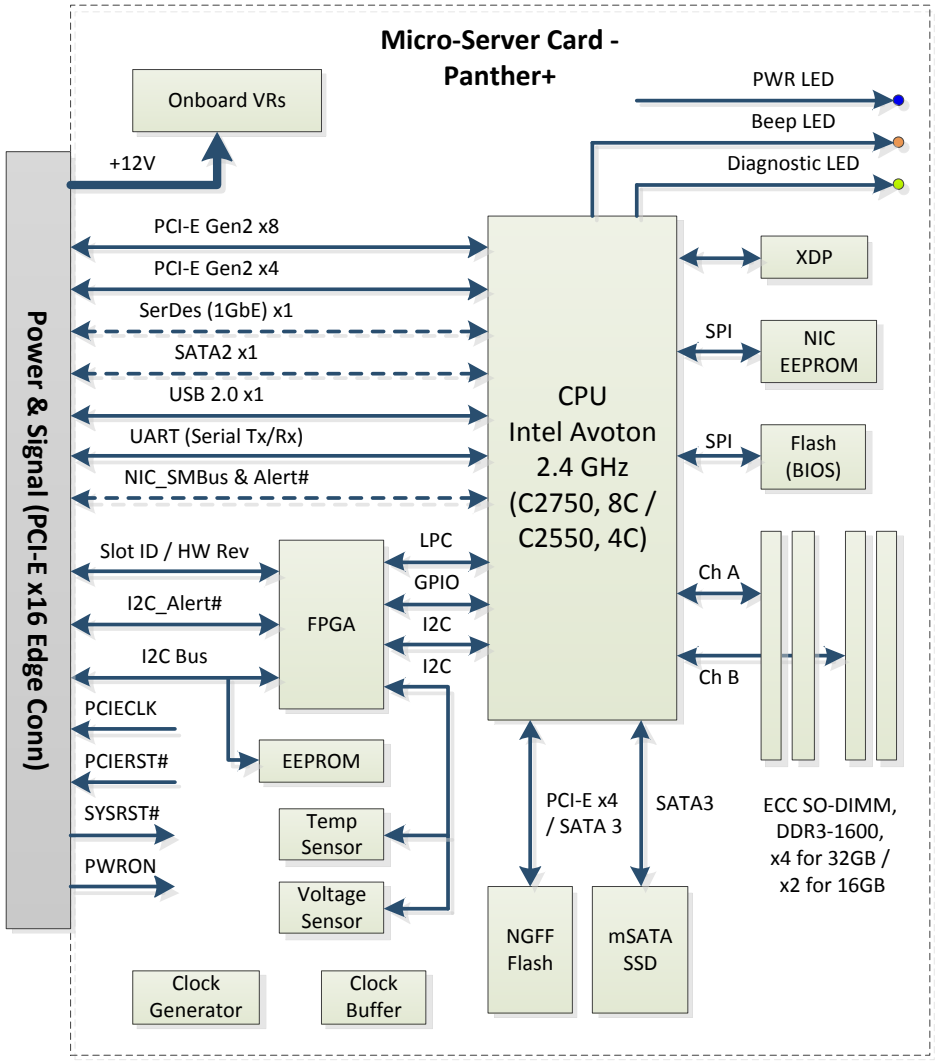

Figure 15 Block Diagram of the Panther+ Card

6.4 Panther+ Feature List

The main Panther+ card feature list for the Honey Badger compute module includes:

- One Intel Avoton CPU / SoC, 2.4GHz
  - 8 cores for Feature Model
  - 4 cores for Entry Model
- Up to four DDR3-1600 SO-DIMM slot, ECC enabled
  - 4 DIMM modules for Feature Model, 32 GB max
  - 2 DIMM modules for Entry Model, 16 GB max
  - Panther+ only support DDR3L (low-voltage)
- One mSATA SSD module, SATA3
  - 256 GB POR

- One NGFF Flash module, SATA3 or PCI-E x4 (BOM Option), 2280 form factor
  - 256 GB POR
  - Available only on Feature Model
- Three Status LEDs
  - One Blue LED for power
  - One Amber / Orange LED for beep
  - One Yellow-Green LED for diagnostic
- One JTAG connector reserved for OCP test on Micro-Server card

6.5 Panther+ PCB Dimension

Figure 16 to Figure 18 shows the details of the Panther+ PCB dimension. The A-side is also referred as the top side, while the B-side is referred to as the bottom side.

Instead of a flexible length for the generic Micro-Server card specification, Panther+ adopts the fixed length at the maximum (210mm). Its dimensions are as below:

- Width: 73.8mm
- Length: 210mm

Because Panther+ will be used in different platforms and systems, Figure 16 and Figure 17 show the two possible airflow options for cooling. Honey Badger adopts the Airflow Option 2.

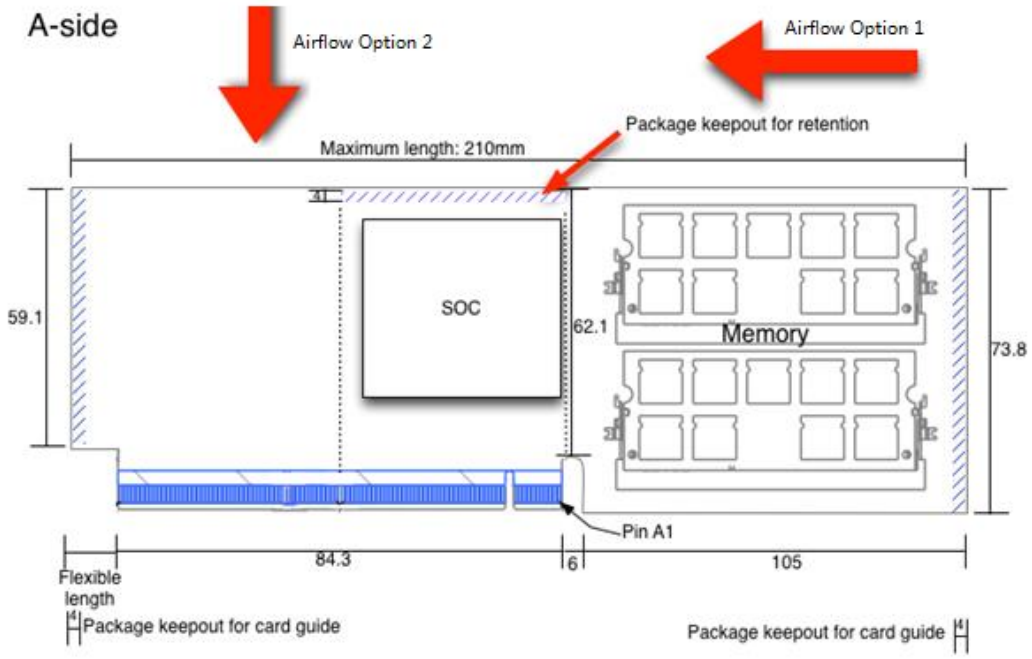

Figure 16 Panther+ Card Dimension, A side

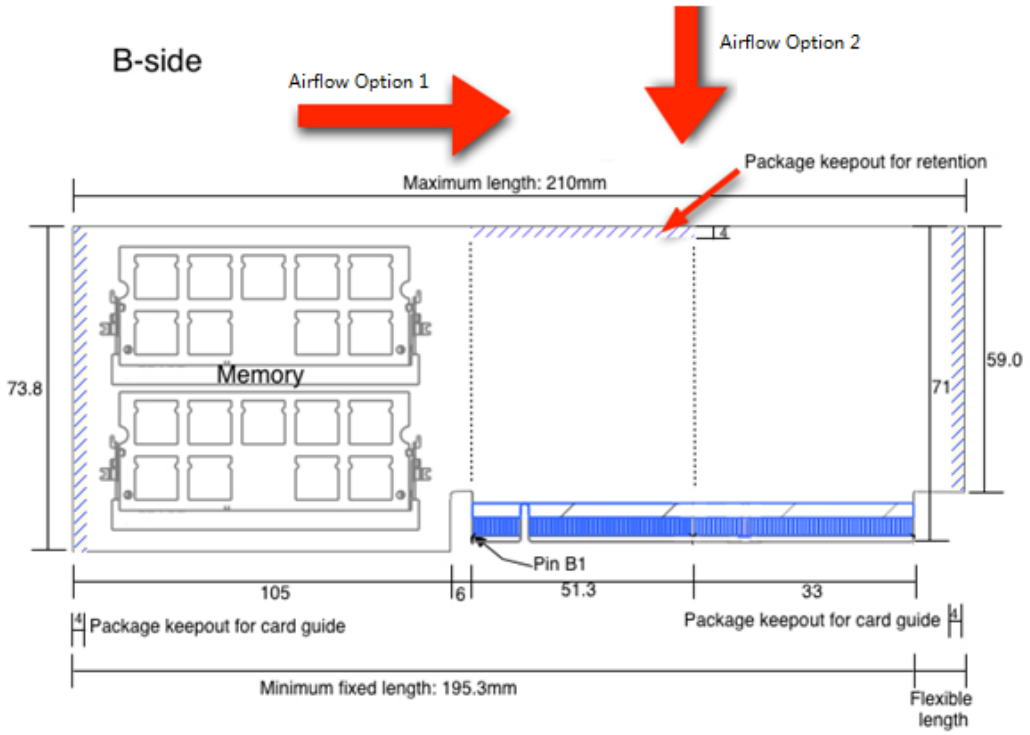

Figure 17 Panther+ Card Dimension, B side

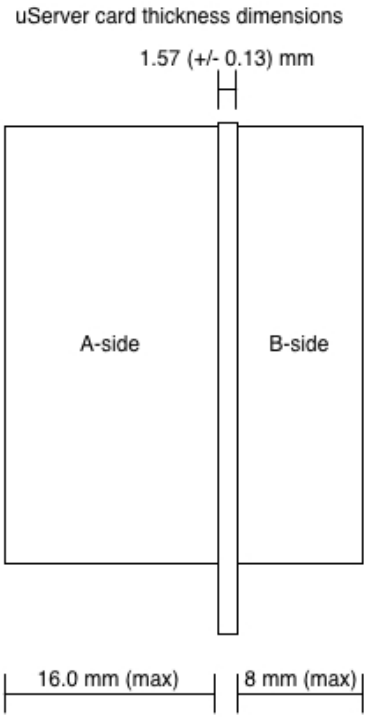

Figure 18 Panther+ Card Height Limitation

7 Honey Badger Baseboard

7.1 Baseboard Feature List

The Honey Badger baseboard functions as a storage HBA card. It also contains a server management module. The main feature list of the Honey Badger baseboard appears below:

- One 12G SAS controller with one 12G SAS expander, to provide non-blocking throughput and IOPS from CPU to 15 or 30 NL-SAS HDDs or Cloud SATA HDDs
  - SAS expander is responsible for storage enclosure management services (in-band)
- One BMC is responsible for system enclosure management services (out-band), such as fan control and all standard IPMI related functions
  - One or two I2C buses are necessary between the SAS expander and the BMC to exchange related information
- A hardware approach is reserved for future exploration of "BMC as Virtual SEP," with a BOM option
  - Reserve path for BMC as storage enclosure management services: BOM option to connect a drive's GPIO to the BMC
  - Reserve I2C bus between a SAS controller and the BMC (one or two as needed): for "BMC as Virtual SEP" software investigation
- One Mini-SAS connector in SFF-8088 form factor
  - From SAS controller, to connect Knox SEB in the another tray within the same Honey Badger system
- One reserved Mini-SAS connector in SFF-8087 form factor
  - From SAS expander, for cascading purpose (to connect Knox SEB in another Knox system)
- One 10GbE mezzanine card to support one 10GbE port (SFP+)
  - Shared NIC feature support on the 10GbE mezzanine card for in-band management. This will occur by connecting both the NC-SI/RMII and the I2C between the 10GbE card and the BMC
  - Compatible for future 40GbE mezzanine card, single port (QSFP) only
- One USB port for on-site management/service/debug
- One debug header to accept an existing OCP debug card
  - With a slide switch to select either the CPU sub-system or the storage sub-system to be debugged
  - With a Red LED to indicate when storage sub-system is being debugged
- Two Switch Buttons
  - Power
  - Reset
- Four Status LEDs:
  - One for power and system identify
  - One for enclosure fault status
  - Two 10GbE SFP+ port link status LEDs on the 10GbE Mezz Card
- Manufacturing Test Requirements
  - One JTAG connector reserved for OCP test on baseboard

- JTAG scan chain is available for key ICs on board: BMC, SAS controller, SAS expander
- Enable BIST for manufacturing test

7.2 Baseboard Block Diagram

Figure 19 illustrates the functional block diagram of the Honey Badger baseboard with an LSI solution.

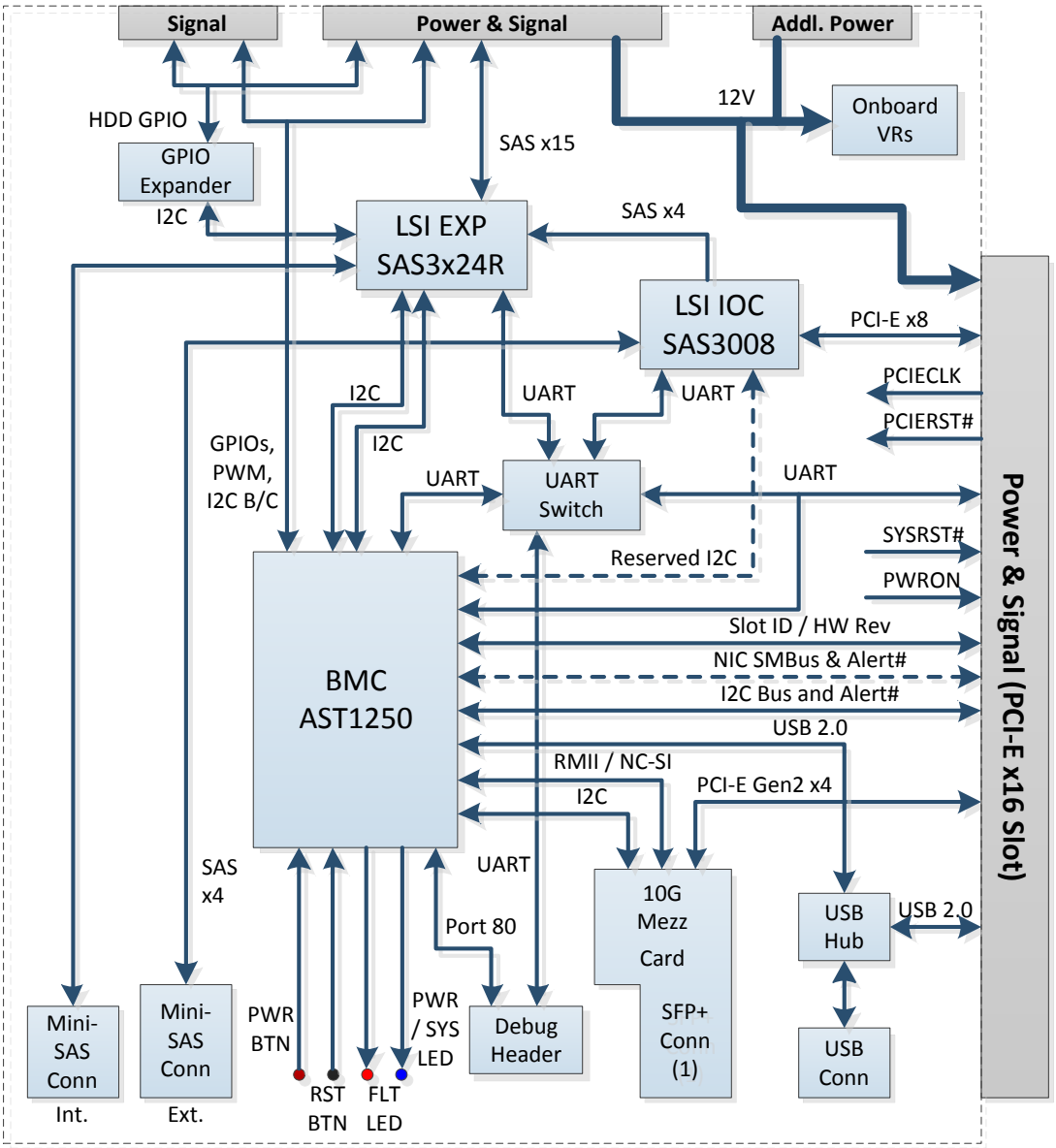

Figure 19 Honey Badger baseboard Block Diagram – LSI solution

Figure 20 shows the functional block diagram of the Honey Badger baseboard with a PMC-Sierra solution.

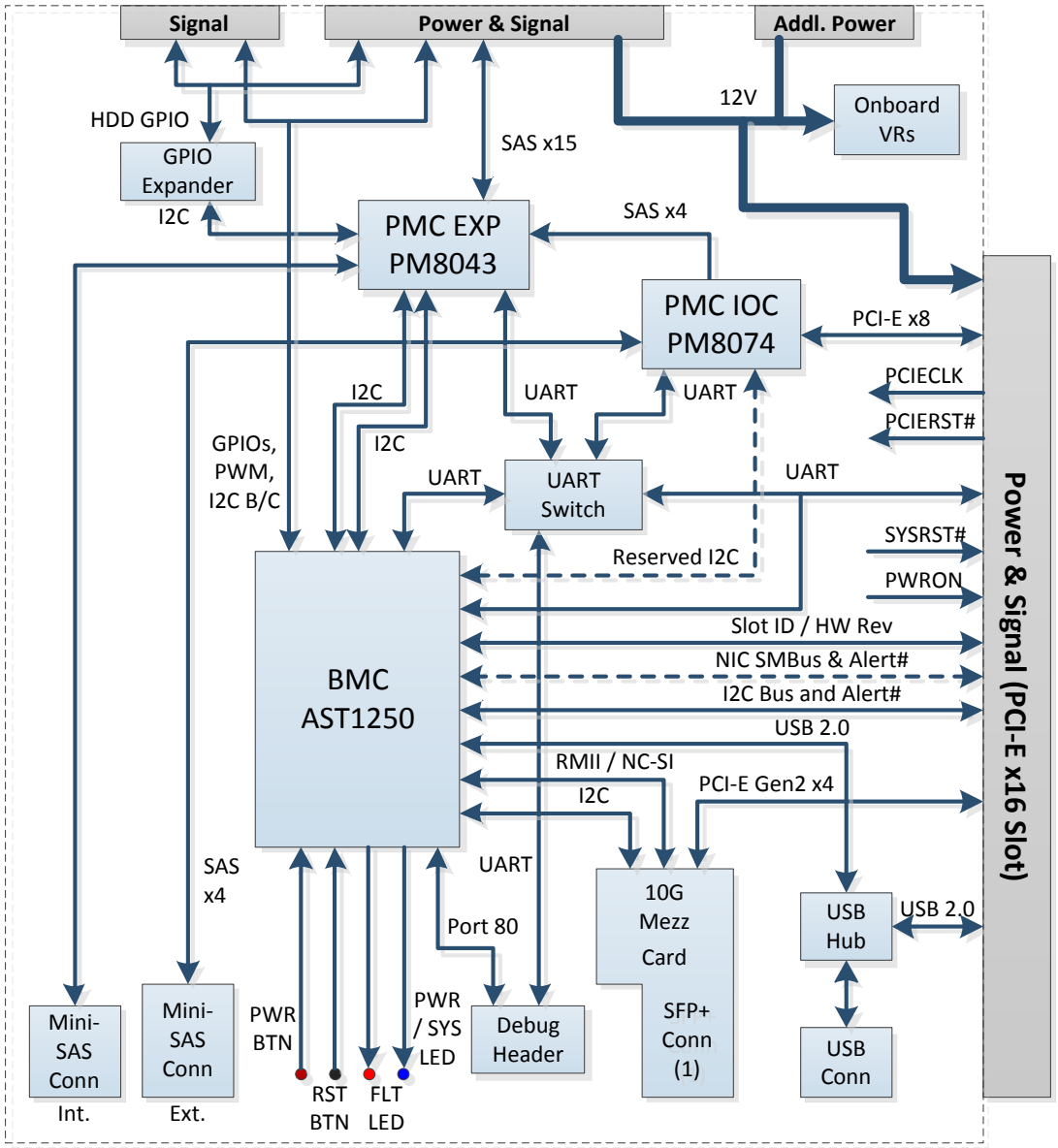

Figure 20 Honey Badger baseboard Block Diagram – PMC solution

7.3 Mechanical Requirements for the Baseboard

Figure 21 illustrates the Baseboard PCB dimensions of the Honey Badger compute module.

- Extended width to 354 mm, and a maximum depth not to exceed 251 mm.
- The dotted line shows the original Knox SEB dimension (start from the top left corner).
- The notch on the top right area is to engage with the shortened center card guide on new Honey Badger tray, as shown in Figure 13.

- The height limitation area on the top side is marked with an "X". It only allows components less than 2 mm in height.
- The component height limitation for the entire bottom side is 1.6 mm.
- The Keep out area is also marked with an "X" as labeled in the figure below. It is suggested that the vendor cut out this area to keep free space for the Honey Badger tray latch / handle.

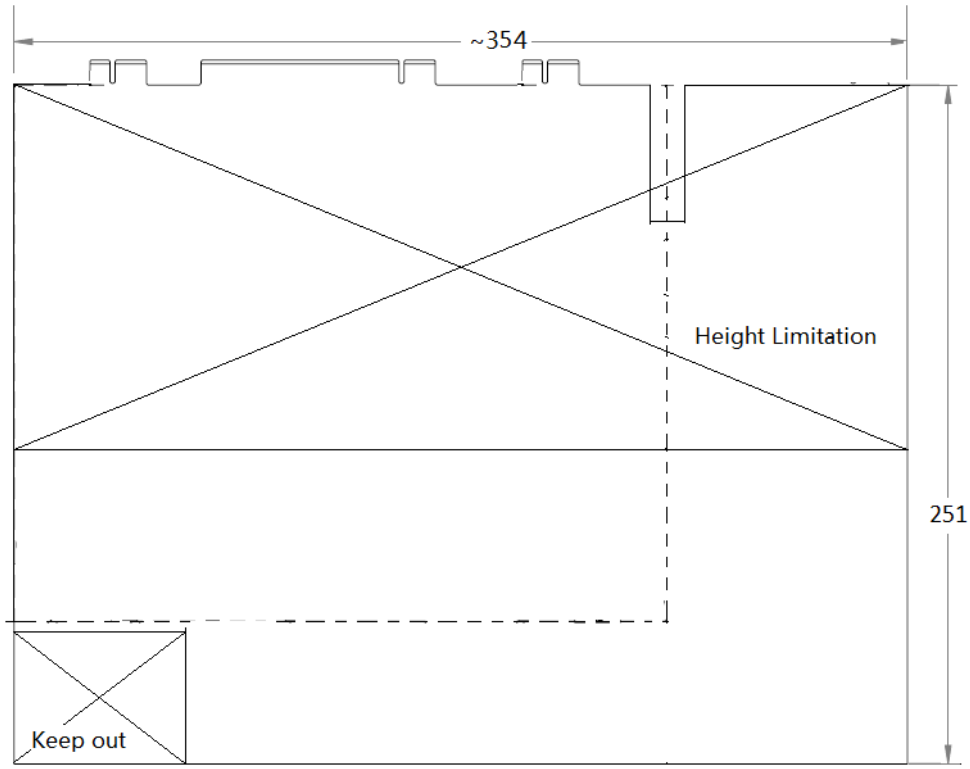

Figure 21 Honey Badger Baseboard PCB Dimension

- Latches on the left and right side of the Panther+ PCB shall restrain it. These latches, shown below in Figure 22, will rotate horizontally, and will not be spring-loaded. If a latch is opened it will stay open until it is manually closed. These latches will have features that will impart a tactile feedback ("click") when in the fully open and fully closed positions. They must pass transportation shock and vibration testing in the closed position, without additional parts or packing material. There will be a hard stop to restrain the latch from opening wider than necessary to allow the card to pass by, thus eliminating difficulty in retrieving a latch that has over-rotated into the chassis. The design of the latches shall copy as closely as space allows, the shape and size of the example. The pivot features are TBD by the vendor.

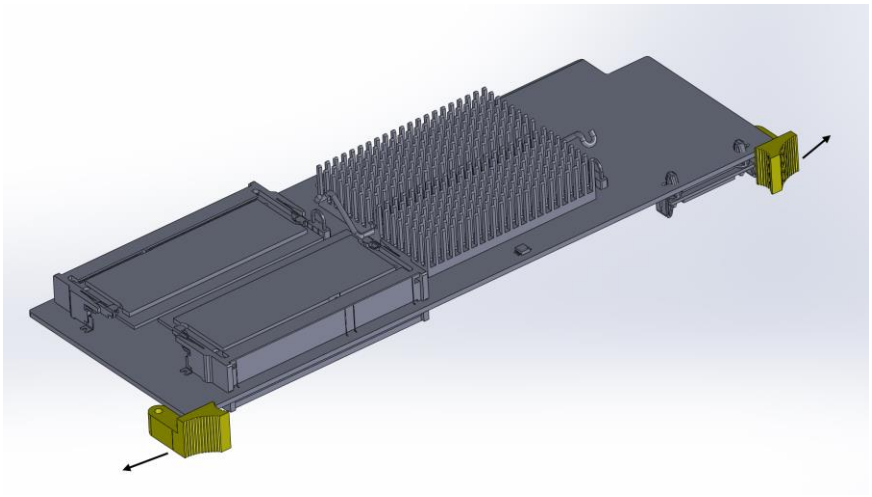

Figure 22 Concept of Latch Mechanism for Panther+

- The lower HDD tray's HDD latches shall be confirmed to clear all cables, connectors, features and components.
- Facebook shall define the mechanical fixturing to the chassis. The company will share CAD files.
- Baseboard to chassis fasteners: "quarter turn" thumbscrew fasteners shall be used. Facebook shall supply a specific Southco brand part number and drawing so the vendor can supply their own mating thumbscrew. Facebook will also supply a reference part number for the thumbscrew. Facebook must also approve any deviations from this size and form factor. If a quarter turn fastener part number is not available in time, a standard M3 thumbscrew shall be used.

7.4 Baseboard Key Component Placement

Figure 23 below illustrates the key component placement of the Honey Badger baseboard.

- For rack level cable routing, it is preferred that the Mini-SAS connector (and cable) is to the left side of the Panther+ card
- For rack level cable routing, it is preferred that the 10GbE Mezz Card (and cable) is to the right side of the Panther+ card
- It is preferred that the Mini-SAS connector is recessed a certain distance from the front edge, so that when a Mini-SAS cable with a long connector head is plugged in, it won't stretch out too far in the front. The goal should be keep the cable (with bent radius) at a similar depth (to the front) between the Mini-SAS cable and 10G Ethernet cable.
- Try to put the SAS expander in the suggested location or as close as possible. The main purpose is to shorten the total SAS trace length (similar to the Knox SEB and DPB).
- To keep the Honey Badger baseboard width as small as possible, it is suggested to stack the 10GbE mezzanine card under the Panther+ Micro-Server card.
- The placement is for reference only. The vendor can adjust it accordingly for better design implementation.

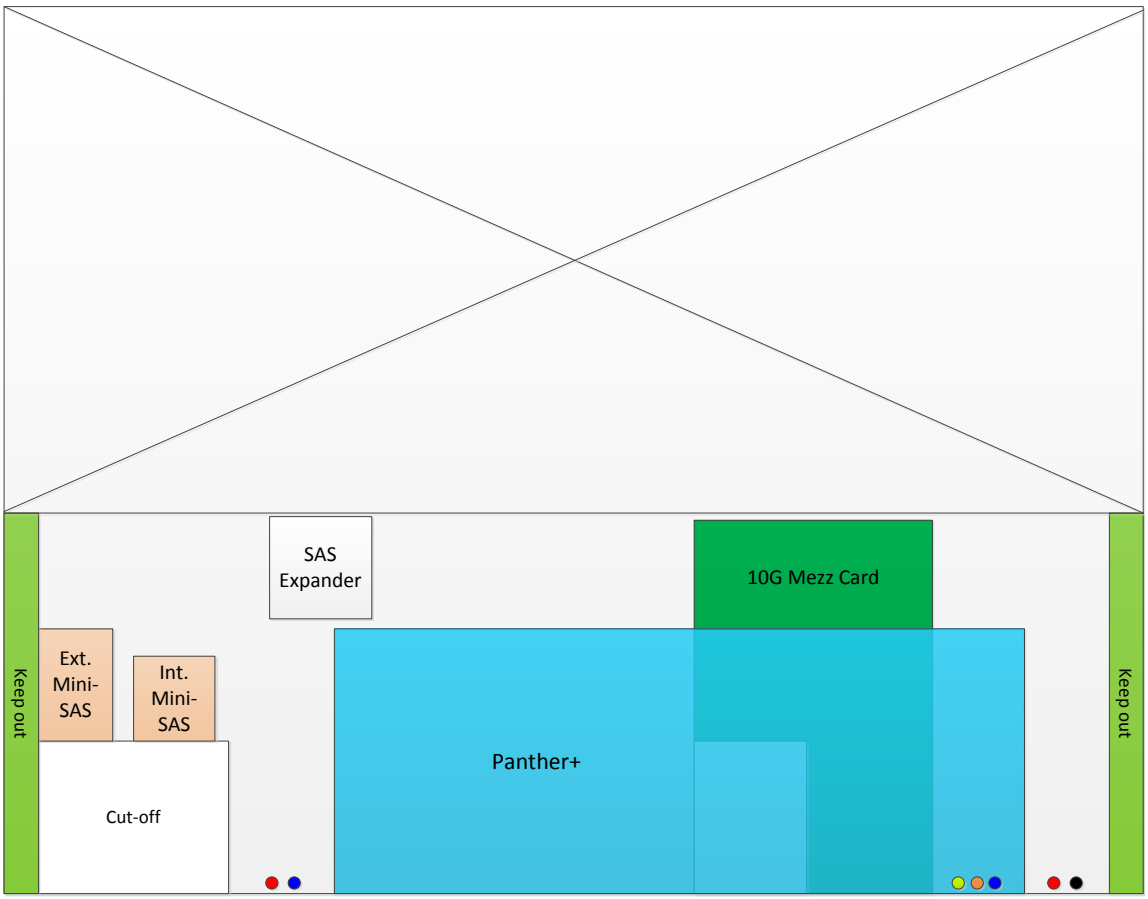

Figure 23 Honey Badger baseboard Key Component Placement

7.5 SAS Controller and SAS Expander

The Honey Badger baseboard has two solutions for a storage sub-system. Both are 12G SAS solutions, with one 8-port SAS controller and one 24-port SAS expander. One solution is from Avago / LSI, the other solution is from PMC-Sierra.

7.5.1 LSI SAS Controller and Expander Solution

The Avago / LSI 12G SAS solution includes an 8-port SAS controller and a 24-port SAS expander.

LSISAS3008 is a 12G SAS / 6G SATA controller with a PCI-E Gen3 interface. It's based on Avago / LSI Fusion-MPT architecture, and provides a full-featured host bus adapter solution for SAS and SATA devices. It also comes with a hardware-based RAID solution that supports RAID levels 0, 1, 1E, and 10. The main features implemented in Honey Badger are:

- Eight-lane 8 Gt/s PCI-E Gen3 host interface
- Eight-port 12 Gb/s SAS and 6 Gb/s SATA interface
- 896 pin, 25 mm x 25 mm FPBGA package, 0.8mm ball pitch

LSISAS3x24R is a 24-port, 12G SAS expander device that can connect up to 24 directly attached SAS or SATA devices. It supports both initiator and target connections on any link. All of the

expander ports contain the DataBolt technology feature used to match the bandwidth between fast hosts and slower SAS or SATA devices. *LSISAS3x24R* also provides an ARM-core-based CPU complex with sufficient memory capacity to implement full enclosure management functionality within the expander. The main features are listed below:

- 51 I/O pins for Link Status LEDs or GPIO
- 16 dedicated GPIO
- 5 I2C buses for master or slave operation
- 2 UART ports
- Drive spin-up and sequencing control
- DataBolt technology for End Device Frame Buffering
- Low power version selected (*LSISAS3x24RLC1*)
- 672 pin, 27 mm x 27 mm FPBGA package, 1.0 mm ball pitch

7.5.2 PMC SAS Controller and Expander Solution

The PMC 12G SAS solution also includes an 8 port SAS controller and a 24 port SAS expander.

The *PM8074* is a high-performance 8-port, 12 Gb/s SAS protocol controller intended for the server and data center solutions market. The *PM8074* complies with the PCI-E Gen3 standard and supports up to 8 Gt/s per lane. It comes with proven system performance, availability and manageability, as well as a turnkey solution for production host software drivers. The main features implemented in Honey Badger are:

- Eight-lane PCI-E Gen3 interface
- Eight SAS-3 compliant PHYs
- Independent per-channel selectable high-speed outputs support multiple programmable levels of pre-emphasis and output swing
- Multiple programmable levels of receive equalization
- Decision Feedback Equalizer provides robust recovery of 12 Gb/s SAS signals over lossy channels
- Integrated resistive termination
- 1071 pin, 27 mm x 27 mm FCBGA package, 0.8 mm ball pitch

PM8043 is a 24-port SAS expander that features SAS 3 T10 zoning, self-configuration, table-to-table routing, and an integrated MIPS processor for SES and enclosure management support. It has a small footprint that enables space-constrained designs. It also has ultra-low switching latency for improved system performance. *PM8043* provides SAS and SATA edge-buffering functionality to improve performance with existing 3G and 6G drives. It also has an integrated MIPS processor for enclosure management. Its main features are:

- Up to 62 GPIO pins
- 8 dedicated I2C buses (up to 12 total) for master or slave operation
- Up to 4 UART ports
- Disk spin-up control and disk qualification API
- Edge-buffering functionality
- 896 pin, 25 mm x 25 mm FCBGA package, 0.8 mm ball pitch

7.6 BMC Chip

Aspeed AST1250 is a new Integrated Remote Management Processor (IRMP), functioning as a BMC on the Honey Badger baseboard. It's a vastly integrated SoC device playing as a service processor to support various functions required for highly manageable server platforms. Its highlighted features are:

- Embedded an *ARM926EJ* 32-bit RISC CPU, and a ColdFire V1 CPU
- Internal SRAM and external DDR2 / DDR3 ECC SDRAM
- 14 sets Multi-Function I2C/SMBus bus controllers
- 5 sets UART I/O interface, 4 sets with full flow control
- Up to 216 GPIO pins
- Support 8 PWM outputs, with 3 types of frequency mode PWM for fan speed control
- Up to 16 fan tachometer inputs
- PECI controller, Intel PECI 3.0/2.0/1.1 compliant
- Up to 16 integrated 10-bit ADCs, low-leakage inputs to measure voltage rails
- Adopt full-scan-chain design methodology for testing internal logic by Automatic Test Pattern Generation (ATPG)
- Support Built-In-Self-Test (BIST) and JTAG-compliant boundary scan
- 408 pin, 19 mm x 19 mm TFBGA package, 0.8 mm ball pitch

7.6.1 Voltage Monitor by BMC ADC

To ensure proper operation of all power rails at all times, Honey Badger baseboard adopts the ADC integrated in BMC for voltage monitor. Voltages are reported as part of the system enclosure status. The voltage rails to be monitored are shown as below, Table 1 for the LSI solution, and Table 2 for the PMC solution.

Table 1 Monitored Voltage Rails on Honey Badger baseboard, LSI Solution

Power Rail	**Voltage**
P0V9 Controller	0.9V
P0V9 Expander	0.9V
P1V5 Controller	1.5V
P1V5 Expander	1.5V
P1V8 Standby	1.8V
P3V3 Standby	3.3V
P5V Standby	5.0V
Input 12V	12.5V

Table 2 Monitored Voltage Rails on Honey Badger baseboard, PMC Solution

Power Rail	**Voltage**
P0V925 Controller	0.925V
P0V925 Expander	0.925V
P1V0 Controller	1.0V
P1V0 Expander	1.0V
P1V8 Standby	1.8V

P3V3 Standby	3.3V
P5V Standby	5.0V
Input 12V	12.5V

7.7 10GbE Mezz Card

Honey Badger adopts the existing OCP 10GbE Mezz Card as its primary data network interface at I/O side. There is an option to select a single port or dual port card as per the OCP standard. But for Honey Badger, due to mechanical interference between the 2nd port (both the SFP+ connector and the cable) with the HDD cover on the lower tray when pulled out for service, only a single port 10GbE Mezz Card will be supported.

P/N of single port 10GbE Mezz cards:

- Mellanox – *MCX341A-XCGN*
- Intel – *FBKX520DA1OCP4*

Both of the above Mezz cards have the NC-SI connection to BMC to support OOB function (or "shared-NIC" function).

The Honey Badger baseboard has one PCI-E x8 Mezzanine Card connector that holds x4 PCI-E signal from the Panther+ card (from the Avoton CPU). The Mezzanine connector on the baseboard should use P/N *FCI 61082-121402LF* or its equivalent, with mating P/N *FCI 61083-124402LF* or its equivalent on the Mezzanine card. Pin definitions are in Table 3.

There are two single color LEDs for each SFP+ port. Their definitions follow the standard Ethernet port status LED behaviors.

Table 3 Pin Definition of 10GbE Mezz Card Connector

Signal	Description	Pin	Pin	Signal	Description
P12V_AUX	Aux Power	61	1	MEZZ_PRSNT1_N	Present pin1, short to Pin120 on Mezz card
P12V_AUX	Aux Power	62	2	P5V_AUX	Aux Power
P12V_AUX	Aux Power	63	3	P5V_AUX	Aux Power
GND	Ground	64	4	P5V_AUX	Aux Power
GND	Ground	65	5	GND	Ground
P3V3_AUX	Aux Power	66	6	GND	Ground
GND	Ground	67	7	P3V3_AUX	Aux Power
GND	Ground	68	8	GND	Ground
P3V3	Power	69	9	GND	Ground
P3V3	Power	70	10	P3V3	Power
P3V3	Power	71	11	P3V3	Power
P3V3	Power	72	12	P3V3	Power
GND	Ground	73	13	P3V3	Power
LAN_3V3STB_ALERT_N	SMBus Alert for OOB	74	14	NC-SI_RCSDV	BMC NC-SI
SMB_LAN_3V3STB_CLK	SMBus Clock for OOB	75	15	NC-SI_RCLK	BMC NC-SI
SMB_LAN_3V3STB_DAT	SMBus Data for OOB	76	16	NC-SI_TXEN	BMC NC-SI

PCIE_WAKE_N	PCI-E wake up	77	17	RST_PLT_MEZZ_N	PCI-E reset signal
NC-SI_RXER	BMC NC-SI	78	18	RSVD (MEZZ_SMCLK)	RSVD(PCI-E slot SMBus Clock)
GND	Ground	79	19	RSVD (MEZZ_SMDATA)	RSVD(PCI-E slot SMBus Data)
NC-SI_TXD0	BMC NC-SI	80	20	GND	Ground
NC-SI_TXD1	BMC NC-SI	81	21	GND	Ground
GND	Ground	82	22	NC-SI_RXD0	BMC NC-SI
GND	Ground	83	23	NC-SI_RXD1	BMC NC-SI
CLK_100M_MEZZ1_DP	100MHz PCI-E clock	84	24	GND	Ground
CLK_100M_MEZZ1_DN	100MHz PCI-E clock	85	25	GND	Ground
GND	Ground	86	26	RSVD(CLK_100M_MEZZ 2_DP)	RSVD(2nd set of 100MHz PCI-E clock)
GND	Ground	87	27	RSVD(CLK_100M_MEZZ 2_DN)	RSVD(2nd set of 100MHz PCI-E clock)
MEZZ_TX_DP_C<0>	PCI-E TX signal	88	28	GND	Ground
MEZZ_TX_DN_C<0>	PCI-E TX signal	89	29	GND	Ground
GND	Ground	90	30	MEZZ_RX_DP<0>	PCI-E RX signal
GND	Ground	91	31	MEZZ_RX_DN<0>	PCI-E RX signal
MEZZ_TX_DP_C<1>	PCI-E TX signal	92	32	GND	Ground
MEZZ_TX_DN_C<1>	PCI-E TX signal	93	33	GND	Ground
GND	Ground	94	34	MEZZ_RX_DP<1>	PCI-E RX signal
GND	Ground	95	35	MEZZ_RX_DN<1>	PCI-E RX signal
MEZZ_TX_DP_C<2>	PCI-E TX signal	96	36	GND	Ground
MEZZ_TX_DN_C<2>	PCI-E TX signal	97	37	GND	Ground
GND	Ground	98	38	MEZZ_RX_DP<2>	PCI-E RX signal
GND	Ground	99	39	MEZZ_RX_DN<2>	PCI-E RX signal
MEZZ_TX_DP_C<3>	PCI-E TX signal	100	40	GND	Ground
MEZZ_TX_DN_C<3>	PCI-E TX signal	101	41	GND	Ground
GND	Ground	102	42	MEZZ_RX_DP<3>	PCI-E RX signal
GND	Ground	103	43	MEZZ_RX_DN<3>	PCI-E RX signal
MEZZ_TX_DP_C<4>	PCI-E TX signal	104	44	GND	Ground
MEZZ_TX_DN_C<4>	PCI-E TX signal	105	45	GND	Ground
GND	Ground	106	46	MEZZ_RX_DP<4>	PCI-E RX signal
GND	Ground	107	47	MEZZ_RX_DN<4>	PCI-E RX signal
MEZZ_TX_DP_C<5>	PCI-E TX signal	108	48	GND	Ground
MEZZ_TX_DN_C<5>	PCI-E TX signal	109	49	GND	Ground
GND	Ground	110	50	MEZZ_RX_DP<5>	PCI-E RX signal
GND	Ground	111	51	MEZZ_RX_DN<5>	PCI-E RX signal
MEZZ_TX_DP_C<6>	PCI-E TX signal	112	52	GND	Ground
MEZZ_TX_DN_C<6>	PCI-E TX signal	113	53	GND	Ground
GND	Ground	114	54	MEZZ_RX_DP<6>	PCI-E RX signal
GND	Ground	115	55	MEZZ_RX_DN<6>	PCI-E RX signal
MEZZ_TX_DP_C<7>	PCI-E TX signal	116	56	GND	Ground
MEZZ_TX_DN_C<7>	PCI-E TX signal	117	57	GND	Ground
GND	Ground	118	58	MEZZ_RX_DP<7>	PCI-E RX signal
GND	Ground	119	59	MEZZ_RX_DN<7>	PCI-E RX signal

MEZZ_PRSNT2_N	Present pin2, short to Pin1 on Mezz card	120	60	GND	Ground

7.8 I/O Connectors

Sections 7.8.1 through 7.8.5 describe the I/O connectors that reside on the Honey Badger baseboard.

7.8.1 Power and Signal Connectors to Knox DPB

The new Honey Badger DPB has six PCI-E connectors, three on the A-side are adopted to interface with the system through the Honey Badger baseboard. Three on the B-side are reserved for future use. These straddle-type connectors are mated with 1mm pitch gold finger contacts and are PCI-E Gen3 capable. From left to right, the connectors are:

- A-side: An x1 connector (36 pin from Amphenol, P/N *G630H3612248EU*), mainly for low speed signals and ground pins.
- A-side: An x16 connector (164 pin from Amphenol, P/N *G630HAA12248EU*), for the rest of the low speed signals, all high speed signals, power and ground pins.
- A-side: An x1 connector (36 pin from Amphenol, P/N *G630H3612248EU*), only for power and ground pins.
- B-side: An x1 connector, an x16 connector, and an x1 connector.

Due to the large number of signals, the full connector pin definition is provided in Section 15.1. The following pin assignments are fixed for Honey Badger DPB and FCB:

- DPB Hardware Revision = 0
- FCB Hardware Revision = 0

7.8.2 PCI-E x16 Connector to Panther+

A standard PCI-E x16 card edge connector on the Honey Badger baseboard provides the interface to and from the Panther+ Micro-Server card. Depending on the architecture and board layout, it can be a vertical type connector, such as *AAA-PCI-006-G05* from Lotes; or a right-angled connector, such as *ASP-177154-01* from Samtec.

Panther+ follows the x16 version of Micro-Server card specification, which can support two configurations.

1. Supports 3x PCI-E x4 + 1x Eth + 1x SATA + 80W cards
2. Supports 1x PCI-E x4 + 1x PCI-E x8 + 1x Eth + 1x SATA + 80W cards

Panther+ for Honey Badger (and later on storage projects) follows the 2nd configuration, but Honey Badger doesn't utilize the Ethernet port and the SATA port. Table 4 shows the draft pin assignments for this configuration.

The following pin assignments are applied to the Honey Badger baseboard for different storage solutions:

- Slot ID 12 (SVR_ID = 0x1100) for Honey Badger baseboard, LSI solution
- Slot ID 13 (SVR_ID = 0x1101) for Honey Badger baseboard, PMC solution

Table 4 Pin Assignments for Panther+ PCI-E Golden Finger

Pin Name	Side B	Side A	Pin Name
P12V	1	1	PRSNT#
P12V	2	2	P12V
P12V	3	3	P12V
GND	4	4	GND
I2C_SCL	5	5	SVR_ID0/GPIO0
I2C_DATA	6	6	SVR_ID1/GPIO1
GND	7	7	COM_TX
PWR_BTN#	8	8	COM_RX
USB_P	9	9	SVR_ID2/GPIO2
USB_N	10	10	SVR_ID3/GPIO3
SYS_RESET#	11	11	PCIE_RESET#
I2C_ALERT#	12	12	GND
GND	13	13	PCIE0_REFCLK_P
GND	14	14	PCIE0_REFCLK_N
PCIE0_TX0_P	15	15	GND
PCIE0_TX0_N	16	16	GND
GND	17	17	PCIE0_RX0_P
GND	18	18	PCIE0_RX0_N
PCIE0_TX1_P	19	19	GND
PCIE0_TX1_N	20	20	GND
GND	21	21	PCIE0_RX1_P
GND	22	22	PCIE0_RX1_N
PCIE0_TX2_P	23	23	GND
PCIE0_TX2_N	24	24	GND
GND	25	25	PCIE0_RX2_P
GND	26	26	PCIE0_RX2_N
PCIE0_TX3_P	27	27	GND
PCIE0_TX3_N	28	28	GND
GND	29	29	PCIE0_RX3_P
GND	30	30	PCIE0_RX3_N
SATA0_TX_P	31	31	GND
SATA0_TX_N	32	32	GND
GND	33	33	SATA0_RX_P
GND	34	34	SATA0_RX_N
PCIE1_REFCLK_P	35	35	GND
PCIE1_REFCLK_N	36	36	GND
GND	37	37	RSVD
GND	38	38	RSVD
PCIE1_RESET#	39	39	GND
RSVD	40	40	GND
GND	41	41	RSVD
GND	42	42	RSVD
RSVD	43	43	GND
RSVD	44	44	GND

GND	45	45	RSVD
GND	46	46	RSVD
RSVD	47	47	GND
RSVD	48	48	GND
GND	49	49	PCIE0_RX4_P
GND	50	50	PCIE0_RX4_N
PCIE0_TX4_P	51	51	GND
PCIE0_TX4_N	52	52	GND
GND	53	53	PCIE0_RX5_P
GND	54	54	PCIE0_RX5_N
PCIE0_TX5_P	55	55	GND
PCIE0_TX5_N	56	56	GND
GND	57	57	PCIE0_RX6_P
GND	58	58	PCIE0_R6_N
PCIE0_TX6_P	59	59	GND
PCIE0_TX6_N	60	60	GND
GND	61	61	PCIE0_RX7_P
GND	62	62	PCIE0_RX7_N
PCIE0_TX7_P	63	63	GND
PCIE0_TX7_N	64	64	GND
GND	65	65	PCIE1_RX0_P
GND	66	66	PCIE1_RX0_N
PCIE1_TX0_P	67	67	GND
PCIE1_TX0_N	68	68	GND
GND	69	69	PCIE1_RX1_P
GND	70	70	PCIE1_RX1_N
PCIE1_TX1_P	71	71	GND
PCIE1_TX1_N	72	72	GND
GND	73	73	PCIE1_RX2_P
GND	74	74	PCIE1_RX2_N
PCIE1_TX2_P	75	75	GND
PCIE1_TX2_N	76	76	GND
GND	77	77	PCIE1_RX3_P
GND	78	78	PCIE1_RX3_N
PCIE1_TX3_P	79	79	GND
PCIE1_TX3_N	80	80	GND
GND	81	81	P12V
GND	82	82	P12V

7.8.3 Debug Header

The Honey Badger baseboard includes a debug header on the front side. It supports hot plugging for an existing debug card. The debug card has been used in Open Compute servers and Open Vault storage system (Knox). It contains the following functionalities:

- Two 7-segment LED displays. Shows BIOS POST information and CPU system error codes, or storage system error codes.

- One RS-232 serial connector. Provides console redirection.
- One reset button. When pressed, triggers either a CPU system reset or a storage system (expander) reset.
- One UART channel selection button. Sends a positive pulse to the Honey Badger baseboard to select and rotate the UART console in a loop of:
  - Host console -> BMC debug console -> SAS controller console -> SAS expander console.

The connector for the debug header is a 14-pin, shrouded, right-angled, 2 mm pitch connector. Figure 24 shows an illustration. The debug card has a key to match with the notch to avoid pin shift when plugging it in.

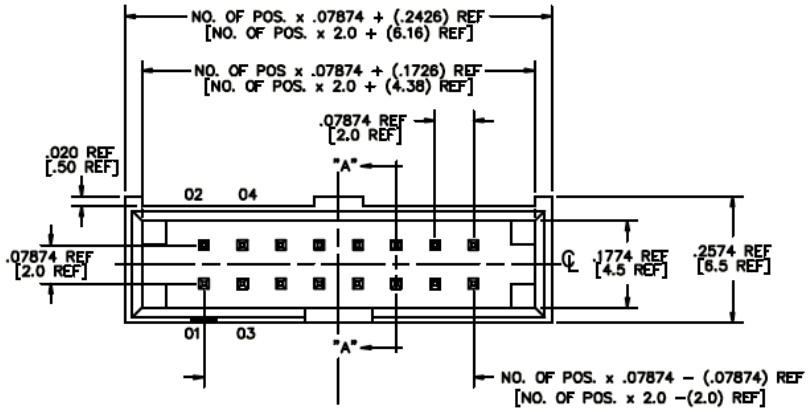

Figure 24 Debug Header Illustration

Table 5 lists the pin definition of the debug header.

Table 5 Debug Header Pin-out

Pin (CKT)	Function
1	Low HEX character [0] least significant bit
2	Low HEX character [1]
3	Low HEX character [2]
4	Low HEX character [3] most significant bit
5	High HEX character [0] least significant bit
6	High HEX character [1]
7	High HEX character [2]
8	High HEX character [3] most significant bit
9	Serial Transmit
10	Serial Receive
11	System Reset
12	UART Channel Selection
13	GND
14	VCC (5VDC)

7.8.4 External Mini-SAS Connector

The external Mini-SAS connector is to connect Knox SEB in another tray within the same Honey Badger system, so that to support the use case of 1:30 compute to HDD ratio. The Mini-SAS connector is in SFF-8088 standard form factor, and it's referred to as a Mini-SAS-4x connector. Its part number is *G40BR261BEU* from AMPHENOL, or equivalent. The connector pin-out is shown in Table 6.

Table 6 External Mini-SAS-4x Connector Pin-out

Pin	Assignment	Pin	Assignment
A1	GND	B1	GND
A2	Rx0P	B2	Tx0P
A3	Rx0N	B3	Tx0N
A4	GND	B4	GND
A5	Rx1P	B5	Tx1P
A6	Rx1N	B6	Tx1N
A7	GND	B7	GND
A8	Rx2P	B8	Tx2P
A9	Rx2N	B9	Tx2N
A10	GND	B10	GND
A11	Rx3P	B11	Tx3P
A12	Rx3N	B12	Tx3N
A13	GND	B13	GND

The part number of EMI cage for Mini-SAS connector is Molex *74548-0211*, or equivalent.

7.8.5 Internal Mini-SAS Connector

The internal Mini-SAS connector is reserved for cascading purpose (to connect Knox SEB in another system). This connector is in SFF-8087 standard form factor, or referred to as Mini-SAS-4i connectors. The part number is 75783-0012 from Molex, or equivalent. The connector pin-out is shown in Table 7.

Table 7 Internal Mini-SAS-4x Connector Pin-out

Pin	Assignment	Pin	Assignment
A1	GND	B1	GND
A2	Rx0P	B2	Tx0P
A3	Rx0N	B3	Tx0N
A4	GND	B4	GND
A5	Rx1P	B5	Tx1P
A6	Rx1N	B6	Tx1N
A7	GND	B7	GND
A8	NC	B8	NC
A9	NC	B9	NC

A10	NC	B10	NC
A11	NC	B11	NC
A12	GND	B12	GND
A13	Rx2P	B13	Tx2P
A14	Rx2N	B14	Tx2N
A15	GND	B15	GND
A16	Rx3P	B16	Tx3P
A17	Rx3N	B17	Tx3N
A18	GND	B18	GND

7.8.6 USB Hub and Connector

The Honey Badger baseboard requires one external USB port located in the front. It should be a standard Type-A USB connector, to support the following devices.

- USB keyboard and mouse
- USB flash drive (bootable)
- USB hard drive (bootable)
- USB optical drive (bootable)

The Honey Badger baseboard also requests an USB hub, which routes the USB port from the Panther+ to both the USB connector and the BMC chip. This was shown in the block diagrams of Figure 19 and Figure 20, in Section 7.2.

7.9 Switch and Buttons

7.9.1 Sub-System Selection for Debug Card

As a storage server, Honey Badger contains two sub-systems. One is the CPU system, the other is the storage system. Each sub-system has both of the debug features mentioned in Section 7.8.3: two digit error codes displayed on a 7-Segment LED, and the reset switch to trigger a sub-system reset.

On a Honey Badger baseboard, there is a slide switch located besides the debug header. It will be used to select which sub-system is to be debugged.

- When the CPU sub-system is selected (default setting):
  - The debug card displays a POST 80 code from the Panther+ card (through I2C to BMC), driven by the BMC
  - The reset button on the debug card will trigger a CPU system reset
- When the storage sub-system is selected:
  - The debug card displays the storage system error code as defined in Knox (Open Vault Storage), driven by SAS expander
  - The reset button on debug card will trigger a SAS expander reset

A red LED is located close to the slide switch, to indicate when storage sub-system is selected and debugged.

7.9.2 UART Switch Button

Also, as mentioned in Section 7.8.3, the debug card has a push button that's used for UART channel selection. A related functional diagram is shown in Figure 25.

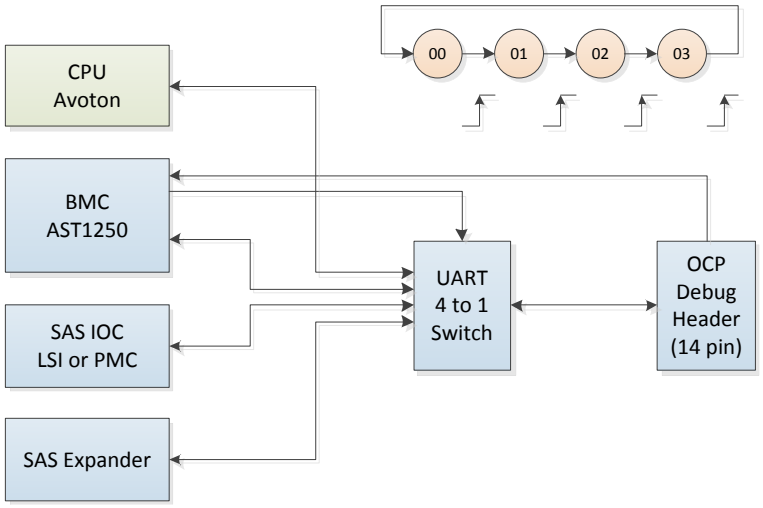

Figure 25 Concept of UART Channel Selection

7.9.3 Power and Reset Buttons

On the Honey Badger baseboard, there are two switch buttons for the whole compute module:

- Power switch (red)
- System reset switch (black)

The vertical tactile switch buttons must be placed in an easy accessible area. The push button actuator must have a minimum 2.5 mm diameter and must protrude 7 mm to 9 mm from top of the actuator to the PCB surface.

- When only one button can be placed to the front edge, the power switch is the outer one, and the systems reset switch is the inner one.
- If the power switch is depressed for durations less than four seconds, a power management event will occur. This event indicates that the power switch has been triggered.
- If the power switch is depressed for longer than four seconds, the Honey Badger baseboard and Panther+ card shall perform a hard power off.
- If the reset switch is depressed for any duration of time, the Honey Badger baseboard and Panther+ card shall perform a hard reset and begin executing BIOS initialization code.

The functionality of each switch shall be indicated by a label on the Honey Badger baseboard's silk screen. The labels PWR and RST are acceptable.

7.10 LEDs

The Honey Badger baseboard has two LEDs on its front edge, to display various types of information:

- One single color in blue, for power and system identify
- One single color in red, for enclosure fault status

Table 8 summarizes the power and system identify LED behaviors.

Table 8 Power and System Identify LED

Power and System Identify	Blue LED
Power off, System Identify off	Consistently off
Power off, System Identify on	On 0.1sec, off 0.9sec, and loop
Power on, System Identify off	Consistently on
Power on, System Identify on	On 0.9sec, off 0.1sec, and loop

Table 9 summarizes the enclosure fault status LED behaviors.

Table 9: Enclosure Fault Status LED

Enclosure Fault Status	Red LED
Normal system operation	Off
Any fault in whole enclosure	On
Reserved for future use	Blinking

7.11 PCB Stack-up

PCB thickness of Honey Badger baseboard is 1.6mm. For a typical 8 layers' PCB stack-up, Table 10 shows one example with details. Table 11 shows the impedance control accordingly. Based on different PCB material, placement and routing strategies, vendor may adjust the stack-up slightly. But it should be communicated with Facebook and get approval in advance.

Table 10 PCB Stack-up for Honey Badger Baseboard

Layer	Plane Description		Copper Weight (oz)	Thickness (mil)	Dielectric (er)
		Solder Mask		0.5	3.7
L1	TOP	Signal	0.5 + 1.0	1.9	
		PrePreg		2.7	3.5
L2	GND1	Ground	1.0	1.3	
		Core		4.0	3.6
L3	IN1	Signal	1.0	1.3	
		PrePreg		17.0	4.5
L4	VCC1	Power	1.0	1.3	
		Core		3.0	3.5
L5	VCC2	Power	1.0	1.3	
		PrePreg		17.0	4.5
L6	IN2	Signal	1.0	1.3	
		Core		4.0	3.6
L7	GND2	Ground	1.0	1.3	

		PrePreg		2.7	3.5
L8	BOT	Signal	0.5 + 1.0	1.9	
		Solder Mask		0.5	3.7
		Total Thickness and Tolerance:		63.0	+/-6mil

Table 11: PCB Impedance Control for Honey Badger Baseboard

Trace Width (mil)	Air Gap Spacing (mil)	Impedance Type	Layer	Impedance Target (ohm)	Tolerance (+/-)
4.5		Single	1, 8	50	5 ohm
5.5	8.0	Differential	1, 8	85	10%
4.0	9.5	Differential	1, 8	100	10%
5.0		Single	3, 6	50	5 ohm
5.0	6.0	Differential	3, 6	85	10%
4.0	9.0	Differential	3, 6	100	10%

8 Board Level Power Budget

This section lists the PCBA level power budget for Honey Badger, both the feature and the entry models.

8.1 Feature Model Power Budget

Board level power budget of Honey Badger feature model is about 75W. Table 12 shows the details of calculation estimated as of now.

Table 12 Honey Badger Power Budget for Feature Model

Major Device	TDP max (W)	Qty	Utilization (%)	Power (W)
Processor (Avoton) 8 core	20	1	90%	18
DDR3 U-DIMM / SO-DIMM	5	4	70%	14
M-SATA SSD	2.3	1	70%	1.61
PCI-E NGFF Flash	3	1	70%	2.1
Other uServer Card Logic/IC	2	1	80%	1.6
Power Buidget for Panther+ Card, High Configuration				37.31
12G 8 port SAS Controller	17	1	80%	13.60
12G 24 port SAS Expander	12.5	1	80%	10.00
10G Card (Ethernet controller)	10	1	80%	8
BMC AST1250	2	1	80%	1.6
Other Baseboard Logic/IC	4	1	90%	3.6
USB2.0	2.5	1	50%	1.25
Board Power Buidget for X86 Feature Model, Baseboard				38.05
Total Power Buidget for X86 Feature Model				75.36

8.2 Entry Model Power Budget

The board level power budget of Honey Badger X86 entry model is about 59W. Table 13 shows the details of calculation estimated as of now.

Table 13 Honey Badger Power Budget for X86 Entry Model

Major Device	TDP max (W)	Qty	Utilization (%)	Power (W)
Processor (Avoton) 4 core	14	1	90%	12.6
DDR3 U-DIMM / SO-DIMM	5	2	70%	7
M-SATA SSD	2.3	1	70%	1.61
PCI-E NGFF Flash	3	0	70%	0
Other uServer Card Logic/IC	2	1	80%	1.6
Power Buidget for Panther+ Card, Medium Configuration				22.81
12G 8 port SAS Controller	17	1	70%	11.90
12G 24 port SAS Expander	12.5	1	80%	10.00
10G Card (Ethernet controller)	10	1	80%	8
BMC AST1250	2	1	80%	1.6
Other Baseboard Logic/IC	4	1	90%	3.6
USB2.0	2.5	1	50%	1.25
Board Power Buidget for X86 Entry Model, Baseboard				36.35
Total Power Buidget for X86 Entry Model				59.16

9 BIOS Feature List

The Honey Badger BIOS design will follow the same requirements as the Panther+, or the generic Micro-Server card. Please refer to the documents as described in Section 6.1 or Section 6.2. Highlighted key items as below:

- UEFI compatible
- Configuration and features
  - Disable unused devices
  - BIOS setup menu
  - SoC settings to allow tuning to achieve the optimal combination of performance and power consumption
- BIOS settings tools
- Default boot device priority
  - Network / PXE -> mSATA SSD module -> NGFF flash card -> Other removable devices
- PXE boot
  - Supports PXE boot and provide the ability to modify the boot sequence. When PXE booting, the card first attempts to boot from the first Ethernet device (etho). If this fails, the PXE boot will attempt on the next Ethernet device.
  - PXE timeout timer set to 10 seconds (only for booting from OCP Mezz Card)
- iSCSI network boot
- Other boot options
  - Also supports booting from SATA/SAS and USB interfaces
  - Provides the capability to select boot options

- Remote BIOS update
  - Scenario 1: Sample/audit BIOS settings
  - Scenario 2: Update BIOS with pre-configured set of BIOS settings
  - Scenario 3: BIOS/firmware update with a new revision
  - Update from the operating system over the LAN
  - Can complete BIOS update or setup change with a single reboot (no PXE boot, no multiple reboots)
  - No user interaction (e.g., prompts)
  - BIOS updates and option changes do not take longer than five minutes to complete
  - Can be scripted and propagated to multiple machines
- Event log
  - Implement SMBIOS type 15 per SMBIOS specification Rev 2.6
  - Hold more than 500 event records (assuming the maximum event record length is 24 bytes, then the size will be larger than 12KB)
  - Each event record includes enhanced information identifying the error source device's vendor ID, card slot ID, and device ID
  - A system access interface and application software to retrieve and clear the event log from the BIOS
- Logged errors
  - CPU/memory errors
  - PCI-E errors
  - POST errors
  - SATA errors
  - System reboot events
  - Sensor values exceeding warning or critical thresholds
- Error thresholds
  - Setting must be enabled for both correctable and uncorrectable errors
  - Threshold for Memory Correctable ECC is TBD
  - PCI-E error, follow chipset vendor's suggestion
- POST codes
  - To be displayed on debug card
  - To be provided on the serial console

10 BMC and System Enclosure Management

The Honey Badger baseboard has a BMC for various platform management services and interfaces. Storage sub-system is on the baseboard. The compute module is on the Panther+ Micro-Server card.

The BMC should be a standalone system operating in parallel to host (Honey Badger baseboard and Panther+ card). The health status of the host system should not affect the normal operation and network connectivity of the BMC. The BMC cannot share memory with the host system. Management connectivity for the BMC should work independently from the host, and have no NIC driver dependency for Out-Of-Band (OOB) communication while using a shared-NIC.

The BMC firmware must support IPMI 2.0 compliant features. All features must be remotely accessible.

10.1 Management Network Interface

The BMC should have both an I2C port and a RMII/NC-SI port for OOB access.

The BMC firmware needs to be flexible about which interface and device to activate by either hardware strapping or via a preset priority policy. The BMC firmware needs to make sure the unused interfaces and devices are disabled and do not interfere with the activated management interface and device.

The BMC management network firmware and utilities need to support all features defined in this specification in both an IPv4 and IPv6 network environment.

10.2 Local Serial Console and SoL

The BMC needs to support two paths to access the serial console. It is preferred that both interfaces are functional at all stages of system operation.

- A local serial console on debug header/debug card, as described in Section 7.8.3 and Section 7.9.2
- A remote console, also known as Serial-over-LAN (SoL) through management network described in Section 10.1.

The BMC firmware and baseboard circuitry design should enable the Local console and remote SoL in the same time, which includes both input and output, bidirectional.

When the system boots, POST codes are sent to Port 80 and decoded by the BMC to drive the LED display on the debug card. POST codes should be displayed in the SoL console during system POST. Before the system displays the first screen, POST codes are dumped to and displayed in the SoL console in sequence. After the system shows the first screen in the SoL console, the last POST code received on Port 80 is displayed in the lower right corner of the SoL console screen.

A serial console buffer feature is required. The buffer needs to save at least last five screens of local and five screens of remote console output; 80 columns x 24 rows for each screen. OOB raw command is used to extract and display the buffer. The buffer has to be stored in volatile media such as internal or external SDRAM of the BMC. Buffer data is cleared within five seconds of the removal of standby power. Buffer should NOT be stored in any non-volatile media.

10.3 Remote Power Control and Power Policy

The vendor should implement BMC firmware to support remote system power on/off/cycle and warm reboot through the In-Band or Out-Of-Band IPMI command.

The vendor should implement BMC firmware to support the power on policy to be last-state, always-on, and always-off. The default setting is last-state. The change of power policy should be supported by IPMI command and take effect without BMC firmware cold reset or a system reboot.

It should take less than 3 seconds from AC on for the BMC to process the power button signal and power up the system for POST. A long waiting period from AC on, for BMC firmware to get ready before allowing system POST start is NOT allowed.

10.4 Port 80 POST Code

The vendor should implement BMC to support Port 80 POST code display to drive 8 bit HEX GPIO to debug header. The BMC post function need to be ready before system BIOS starts to send 1st POST code to Port 80. POST code should also be sent to SoL as well.

BMC should have access to POST code and record up to 20x POST codes. OOB raw command can be used to retrieve last 20x POST code from BMC.

10.5 BMC Firmware Update

Vendors should provide tool(s) to implement a remote BMC firmware update. The firmware update should not require any physical input at the system. Remote update means either by OOB by the management network or by logging into the local OS (CentOS) through the data network. Tool(s) shall support CentOS 5.2 / CentOS 6.4 and the updated Facebook Kernel (FBK).

A remote BMC firmware update may take a maximum of five minutes to complete. The BMC firmware update process and the BMC reset process require that the host system neither reboot nor power down. The reset should have no impact to host system's normal operation. The BMC needs to be fully functional with updated firmware after the update. It must reset without further configuration.

The default update should recover the BMC to the factory default settings. There must be an option to preserve SEL and configuration. The MAC address should not be cleared with any BMC firmware update.

10.6 System Sensors

The BMC has access to all analog sensors, discrete sensors and event only sensors on the Honey Badger baseboard, Panther+ card (through the I2C management interface from FPGA), and the Knox system (DPB and FCB). All connected sensors need to be displayed in the sensor data record (SDR) repository.

The sensors required are below. The related lower and upper critical thresholds are listed for system event logging purposes.

- Analog sensors
    - CPU Temp sensor(s)
    - CPU Package Power (PECI)
    - DIMM Temperature(s)
    - Panther+ on-board Temp sensor(s)
    - Panther+ on-board Voltage(s)
    - SAS Controller Temp sensor
    - SAS Expander Temp sensor
    - Baseboard on-board Temp sensor(s)
    - Baseboard on-board Voltage(s)

  - Knox FCB HSC Input Voltage
  - Knox FCB HSC Output Voltage
  - Knox FCB HSC Output Current
  - Knox FCB HSC Output Power
  - Knox FCB BJT Temp sensor(s)
  - Knox DPB Voltage(s)
  - Knox DPB on-board Tem sensor(s)
  - Knox Fan Speed(s)

- Discrete sensors
  - System Status: Thermal trip, CATERR, System throttle
  - SEL Status: Clear, Rollover
  - DCMI Watchdog
  - Processor Fail
  - Chassis Power Status
  - System Booting Status
  - Thermal Limit 1
  - VR HOT
  - CPU / DIMM HOT
  - CPU Error
  - PMBus Status Word: High, Low
  - DIMM UCE

- Event only sensors
  - POST Error
  - Proc Hot Ext
  - Mem Hot Ext
  - Machine Check Error
  - PCI-E Error
  - Voltage Error
  - Memory ECC Error

10.7 System Event Log

The vendor should implement BMC to support the System Event Log (SEL).

- Errors to be logged
  - I2C bus status error
  - Power error
  - Fan failure
  - Voltage failure
  - Thermal events
  - HDD fault
  - Mini-SAS link error
  - Tray pulled out
  - System reboot events

- Critical SEL filter

- OEM commands are required to set and display two different level of SEL filtering. The default is to log all errors during EVT/DVT/PVT with the option to log only critical SELs that need service or indicate power cycle state change, and SEL clear and overflow
- The scope of the critical SEL list is TBD

10.8 Fan Speed Control

The Honey Badger baseboard BMC is responsible for fan speed control. The control algorithm should be based on all temperature sensors' information and thermal profile. Temperature sensors' location are shown in Figure 26 below.

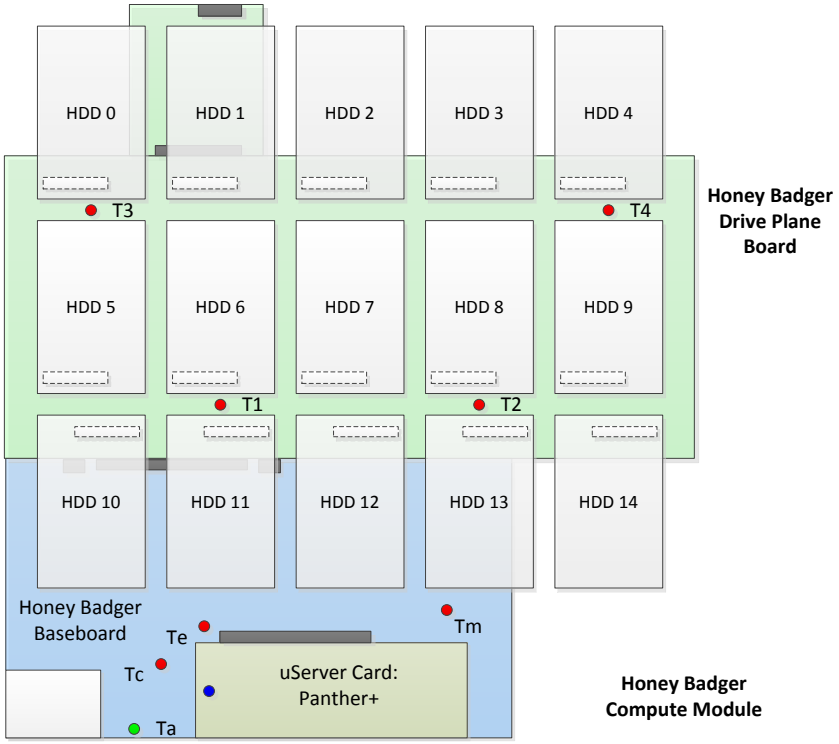

Figure 26 Honey Badger System Thermal Sensor Locations

Consider these key sensors for the fan speed control algorithm:

- Honey Badger compute module
  - CPU core temperature from PECI
  - One ambient temperature sensor on the Panther+ card
  - One ambient temperature sensor on the Honey Badger baseboard, for inlet temperature
    - Ta is the ambient temperature sensor for inlet.
  - Three ambient temperature sensors on the Honey Badger baseboard, for hot spot temperatures
    - Please refer to Tc, Te and Tm respectively
- Knox storage system enclosure
  - Four ambient temperature sensors on the drive plane board

- Please refer to T_1, T_2, T_3 and T_4 respectively

The Honey Badger thermal design should meet these two targets at the same time:

- Ensure all Honey Badger on-board key component temperatures meet thermal requirements with enough margin in all operating environment temperature ranges (e.g., Avoton CPU, SAS controller, SAS expander, etc.)
- Ensure all Knox system component temperatures meet thermal requirements with enough margin in all operating environment temperature ranges. For example, all hard disk drives.

The ODM should be responsible to provide a detailed implementation of the fan speed control requirements. Figure 27 shows the high-level strategy of the fan speed control for Knox systems with Honey Badger, executed by firmware in the existing Knox SEB (SAS expander), and the new Honey Badger baseboard (BMC).

The fan control tables must be upgradeable on the fly (i.e., no system reboot required). Or, an override mechanism must be provided to set fan speed manually without requiring a system reboot.

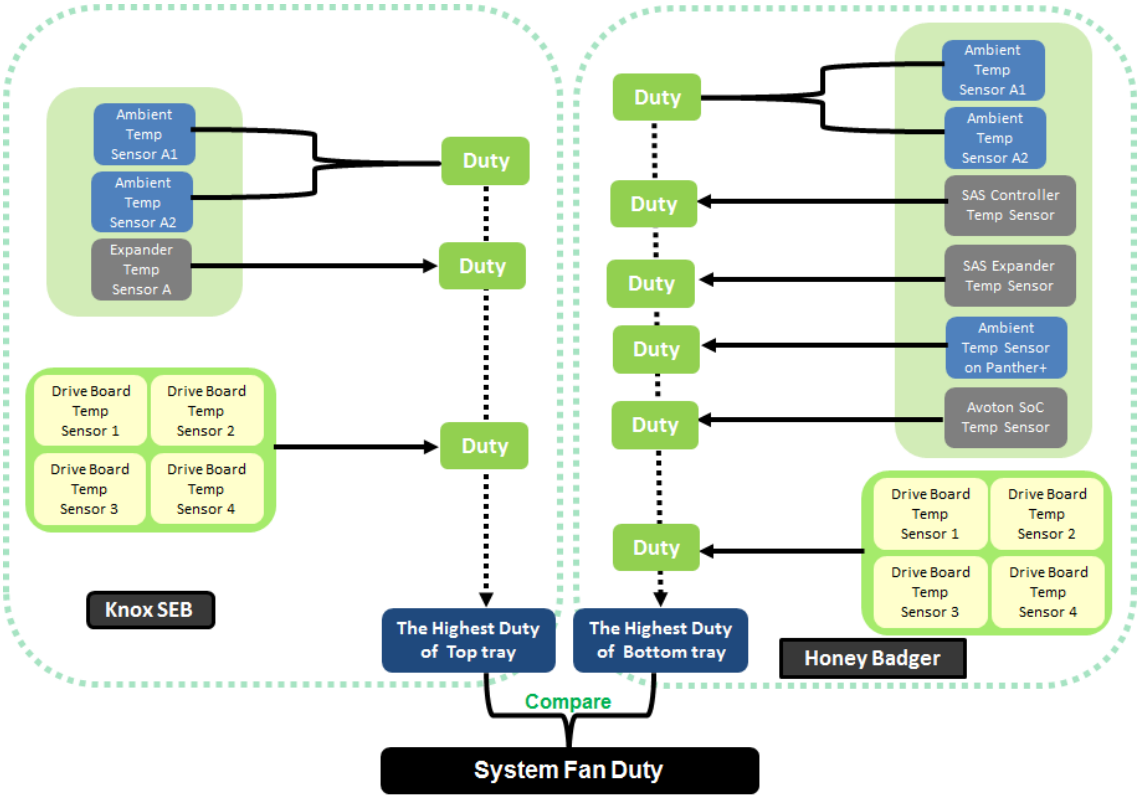

Figure 27 Honey Badger System Fan Speed Control Strategy

10.9 Thermal Protection

There are different levels of consideration for software and hardware thermal protection for the Honey Badger system. They include:

- Setting a **Warning** level for each monitored parameter (including all temperatures,

voltages and input power). When any one of the parameters reaches its warning value, the firmware should report an alarm status to the host server. The host server can predictively perform some actions to avoid actual (both hardware and software) protection in advance.

- Setting a **Software Protection** level for each monitored parameter. When one parameter reaches this level, the related fault LED will light, an error code will be generated, and the firmware should report a critical status to the host server. The host server takes suitable actions to protect the system, such as setting the fan to maximum speed or powering off the related HDDs.
- Setting a **Hardware Protection** level. When some parameters reach this level or meet a set of pre-defined conditions, hardware protection actions will be taken to prevent system damage or to reduce the cost of more power and airflow.

11 Storage Enclosure Management

The ODM is responsible for creating and supporting the firmware to run all storage enclosure management features described in the following sections. The ODM is also responsible for creating a set of diagnostic commands capable of providing status summary and device information to a user terminal.

The Honey Badger design should have the SAS expander as the SEP (Storage Enclosure Processor). Expander firmware design should follow the requirements below for the SES and SCSI buffer specifications.

11.1 Supported Information

Honey Badger's SAS expander firmware should support the functionality described in Table 14.

Table 14 Overview of Honey Badger SAS Expander Firmware Functionality

Name	Comments
SES Standard	
Enclosure Descriptor	
Array Device Slot	
Connector	
Cooling (Fan)	With fine-grained PWM control, details in Section 11.4.2
Current Sensor	Section 11.2.2
Voltage Sensor	
Temperature Sensor	
Enclosure	
SAS Expander	
Extension of SES Standard	
HDD Temperature Reading	Populated as temperature sensors, details in Section 11.4.1
SCSI Buffer	
HDD Temp Polling Interval	
Fan PWM Control	Fine-grained PWM control in percentage.

SN/PN/Tag	Set/retrieve serial number, part number, asset tag,
Power Reading	(Optional) Report power if power monitor is available
GPIO Reading and Control	Read GPIO values
LED Reading and Control	Read/control LEDs
Error Code Report	Report status of all predefined error codes
Heartbeat Control	Control heartbeat generation of the expander
SMP	
PHY Information Reading	Report PHY error counters
Others	
Event Log	SCSI buffer is the preferred backend for event log

11.2 SES Standard

For items listed in "SES Standard" (part of Table 14 above) the Honey Badger SAS expander firmware follows the SES-3 standard (Revision 05, 20 November 2012). Table 15 below summarizes the required SES elements for the SES pages.

Table 15 Required SES Elements

Element	**Pages**
Enclosure Descriptor	01h
Array Device Slot	01h, 02h, 05h, 07h
Connector	01h, 02h, 05h, 07h
Cooling	01h, 02h, 05h, 07h
Temperature Sensor	01h, 02h, 05h, 07h
Current Sensor	01h, 02h, 05h, 07h
Voltage Sensor	01h, 02h, 05h, 07h
Enclosure	01h, 02h, 05h, 07h
SAS Expander	01h, 02h, 05h, 07h, 0Ah
Additional Element Status, Array Device Slot	0Ah
Additional Element status, SAS Expander	0Ah
Download Microcode	0Eh

To be compatible with upper layer management tools, the Honey Badger SAS expander firmware should also take into consideration the items listed in the following subsections.

11.2.1 Array Device Slot

Each expander reports 15 array device slots (not all 30 HDDs are in the chassis), where slot ID equals 0 - 14. The array device slots should be named as "ArrayDevice00" through "ArrayDevice14". The order of the array device element should be the same as its physical slot (0 to 14).

11.2.2 Current Sensor and Voltage Sensor

A current sensor on the 12V power supply is required for power monitoring. The current sensor for the 12V power supply should be the ***first*** current sensor element on the enclosure status diagnostic page (02h).

A voltage sensor is required for all 12V and every key internal power rail.

11.3 Extension to SES Standard

11.3.1 Hard Drive Temperature Polling

The Honey Badger SAS expander firmware should poll the HDD SMART periodically. The interval between HDD temperature polls should be configurable from 1 minute to 60 minutes (details in Section 11.4.1). The firmware should report HDD temperature readings as temperature sensor element in the enclosure status diagnostic page (02h) in the order of slot 0 to slot 14. The Honey Badger SAS expander firmware should also use keyword "HDD" in for HDD temperature readings in the element descriptor page (07h). Other temperature sensors should avoid using keyword "HDD" in the element descriptor page.

Honey Badger SAS expander firmware should log events when the HDD temperature reaches given thresholds. When the HDD temperature sensor's parent drive is not installed, the HDD temperature sensor element should report as "Not Installed" (ELEMENT STATUS CODE = 5h). When HDD temperature reading is not available to firmware, the HDD temperature sensor element should report as "Unknown" (ELEMENT STATUS CODE = 6h).

11.4 SCSI Buffer Definitions

For diagnostic information that does not match standard SES elements, Honey Badger SAS expander firmware should report through SCSI buffer.

11.4.1 HDD Temperature Polling Interval

15 HDDs in the same sub-enclosure share a configurable polling interval, from 1 minute to 60 minutes. The HDD temperature polling interval should be non-volatile.

Table 16 HDD Temperature Polling Interval Control / Status Buffer Layout

Bytes	**Information**	
0000 - 0002h	Reserved	
0003 - 0003h	Polling Interval	00h: disable polling;
		01h – 3Ch: 1 – 60 minutes;
		> 3Ch: 60 minutes.

11.4.2 Fan PWM Control (Optional)

The Honey Badger SAS expander firmware should provide fine-grained fan PWM control through an SCSI buffer. The first byte of the buffer indicates the number of independent PWM in the system. The following bytes report/control each individual PWM with 1 byte. The buffer supports up to 15 PWMs. When fewer PWMs are available, the firmware should fill the buffer with reserved bytes (00h).

Table 17 shows details of PWM control / status buffer. Writing non-zero PWM will force the fans to run at given PWM. Writing zero (00h) PWM will return PWM control to firmware (based on thermal sensor readings). PWM configuration is volatile. When both sub-enclosures boot, the system should use firmware controlled PWM (00h). When only one sub-enclosure reboots, it uses PWM setting in its peer sub-enclosure.

The firmware should ignore REQUESTED SPEED CODE in SES cooling control element.

Table 17 Fan PWM Control / Status Buffer Layout

Bytes	Information	
0000 - 0000h	Number of independent PWM (read only)	
0001 - 0001h	1st PWM	00h: firmware controlled PWM;
		01h – 64h: fan PWM in percentage;
		> 64h: 100% PWM.
0002 - 0002h	2nd PWM (if any)	
…	…	
000F - 000Fh	Reserved.	

11.4.3 PN / SN / Tag

The Honey Badger SAS expander firmware should report part numbers (PN) and serial numbers (SN) for all major components. In addition, the firmware should also remember / report the PN and the Asset Tag.

11.4.4 Power Reading (Optional)

If a power monitor is equipped, the Honey Badger SAS expander firmware should report power readings through the SCSI buffer. The firmware should report the root mean square (RMS) of all power readings in a time window. The window size should be configurable (1 to 255 second) through byte (01h) of the SCSI buffer.

Table 18 Power Reading Buffer Layout

Bytes	Information
0000 - 0000h	Reserved
0001 - 0001h	RMS window size in seconds (01h to FFh)
0002 - 0003h	RMS power reading in Watts (reserved for write)

11.4.5 GPIO Reading

The GPIO buffer should report the status of each GPIO with 1 byte data (00h for low and 01h for high).

Honey Badger SAS expander firmware should report the following GPIO readings.

Table 19 Required GPIO

Name	Direction	Comments
Expander ID	IN	Differentiate different expanders in the same chassis.

Sub-enclosure ID	IN	Differentiate different sub-enclosure in the same chassis.
Debug Card Detection	IN	
Peer Expander Detection	IN	Hardware based detection or heartbeat based detection.
		Report multiple GPIOs if there is more than one peer.
Hardware Revision	IN	(Optional) In case for different version (for cold storage).
Pull Out Detection	IN	Indicate the chassis is pulled out for service.

11.4.6 LED Reading and Control

The LED buffer should report/control the status of LEDs **not** covered by SES, including the 7 segment LED. Each LED should use one byte. By default, the firmware should control LEDs according to system status (warning, error, etc.). The host utility can overwrite LED behavior by writing to the SCSI buffer. Writing FFh to the SCSI buffer returns control to the firmware.

Table 20 LED Control / Status Value and Behavior

Device	**Value and Behavior**
7 Seg LED	00 - FEh;
	FFh: return control to firmware (only for control)
Single Color LED	00h: off;
	01h: on;
	02h: blink;
	03h: unknown;
	FFh: return control to firmware (only for control)
	other: reserved
Duo Color LED	00h: off;
	01h: red;
	02h; red blink;
	10h: blue;
	20h blue blink;
	22h: blink between red and blue;
	33h: unknown;
	FFh: return control to firmware (only for control)
	other: reserved

11.4.7 Fan Speed Control Profile Selection (Optional)

To achieve optimal power consumption, the firmware may apply different fan speed control (FSC) profiles for different HDDs. The firmware should report the FSC profiles in the SCSI buffer with 1 byte (00h for first profile, 01h for second profile, etc.). The host should be able to select different FSC profiles by writing to the same SCSI buffer.

11.4.8 Error Status Array

The Honey Badger SAS expander firmware should report the status of each error code in a buffer. Each error code should be reported with 1 byte, 00h for error code off, and 01h for error code on.

The firmware should support error codes described in Table 21.

The error status array is in addition to SES error status bits. For error conditions covered by SES, the firmware should report in both SES pages and the error status array.

Table 21 Honey Badger SAS Expander Error Code and Event Log

Error Description	Condition
Expander Fault	Expander heartbeat stop
I2C bus crash	Cannot query I2C device
Fan fault	Cannot query fan speed
Temperature sensor warning	Temperature over critical threshold
Voltage sensor warning	Voltage over or under critical threshold
Current sensor warning	Current over or under critical threshold
HDD fault	HDD array device slot status element fault
SAS link error	Loss SAS links
Sub-enclosure pulled out	Firmware detect enclosure is pulled out
Sub-enclosure pushed in	Firmware detect enclosure is pushed in (event log only, no error code)
FW HW not match	FW should log the event and then hang
Component Remove/Attach	
HDD Remove/Attach	

11.4.9 Heartbeat Control (Optional)

To test heartbeat related GPIOs, the firmware should support the ability to disable/enable the heartbeat. The firmware should trigger (start/stop) the heartbeat when the host writes 00h to the heartbeat control buffer.

11.4.10 Event Log

Honey Badger SAS expander firmware should support system event log. It is preferred to implement event log reading through SCSI READ BUFFER command (3Ch). The system event log should report time stamp for each event (if available).

Table 21 in Section 11.4.8 shows the event log requirements.

11.5 HDD Spin-up Control

When an HDD spins up after power on, it draws excessive current on both 12V and 5 V. Especially for the 12V rail, the peak current may reach 1.5A ~ 2A range, which is 2 ~ 3 times the maximum current during normal operation. To minimize the impact on the system power budget, the hardware design supports a staggered power-on feature, and the enclosure management firmware implements a grouped spin-up control mechanism.

- The group definition of hard disk drives follows the SAS expander chip vendor's strategy.
- The ODM vendor defines the quantity of hard disk drives in each group.
- The ODM vendor defines the delay interval between each group.

11.6 HDD Spin-down Control Support

To be aligned with a power saving strategy in future data center operations, the Honey Badger design also supports a spin-down control. Both the hardware design and enclosure management firmware implementation support such a feature.

11.7 Storage System Error Code

As mentioned in Section 7.9.1, one of the two options for error codes displayed on the debug card is for storage system error code. High level categories of related error codes are defined in Table 22 below. Detailed error codes are listed in Section 16.

Table 22 Storage System Error Codes for Honey Badger

00	**No Error**
01-02	Critical Crash - Expander
03-06	Critical Crash - I2C Bus
07-10	*Reserved*
11-22	Fan Fault Critical
23-30	*Reserved*
31-42	Temperature Sensor Critical
43-44	*Reserved*
45-48	Voltage & Current Sensor Critical
49	*Reserved*
50-64	HDD SMART Temp Critical
65-66	Expander Internal Temp Critical
67-69	*Reserved*
70-84	HDD Fault
85-89	*Reserved*
90-92	Mini-SAS Link Error
93-94	Tray Pulled-out
93-98	*Reserved*
99	Firmware and Hardware Mismatch

12 Environmental Requirements and Reliability

12.1 Environmental Requirements

The Honey Badger compute module should support the Knox system to meet the following environmental requirements:

- Gaseous contamination: Severity Level G1 per ANSI/ISA 71.04-1985
- Ambient operating temperature range for system without HDD: -5°C to +45°C
- Ambient operating temperature range for system with HDD: +5°C to +35°C
- Operating and storage relative humidity: 10% to 90% (non-condensing)
- Storage temperature range: -40°C to +70°C
- Transportation temperature range: -55°C to +85°C (short-term storage)

In addition, the full Honey Badger and Knox storage system has an operating altitude with no de-ratings of 1,000 meters (3,300 feet).

12.2 Vibration and Shock

The Honey Badger compute module should support the Knox system to meet shock and vibration requirements according to the following IEC specifications: IEC78-2-(*) & IEC721-3-(*) Standard & Levels. The testing requirements are listed in Table 23.

Table 23 Vibration and Shock Requirements

	Operating	**Non-Operating**
Vibration	0.4g acceleration, 5 to 500 Hz, 10 sweeps at 1 octave/minute per each of the three axes (one sweep is 5 to 500 to 5 Hz)	1g acceleration, 5 to 500 Hz, 10 sweeps at 1 octave/minute per each of the three axes (one sweep is 5 to 500 to 5 Hz)
Shock	6g, half-sine 11mS, 5 shocks per each of the three axes	12g, half-sine 11mS, 10 shocks per each of the three axes

Shock and vibration tests need to take place while the Honey Badger is installed in a Knox and an Open Rack for different type of shipping conditions.

12.3 Mean Time Between Failures (MTBF) Requirements

The system shall have a minimum calculated MTBF of 300,000 hours at 95% confidence level at 25°C ambient temperature while running at full load.

The system shall meet a demonstrated MTBF of minimum 300,000 hours at 95% confidence level prior to the mass production ramp.

The system shall have a minimum service life of 3 years (24 hours/day, full load, at 35°C ambient temperature).

12.4 Regulations

The vendor needs to provide CB reports of Honey Badger (both Panther+ card and baseboard) at the component level. Facebook will need these documents to have rack level CE.

13 Labels and Markings

13.1 PCBA Labels and Markings

All Honey Badger PCBAs shall include the following labels on the component side of the boards. The labels shall not be placed in such a way that may cause them to disrupt the functionality or the airflow path of the system.

Table 24 PCBA Label Requirements

Description	**Type**	**Barcode Required?**
Safety markings	Silkscreen	No
Vendor P/N, S/N, REV (revision would increment for any approved changes)	Adhesive label	Yes
Vendor logo, name & country of origin	Silkscreen	No
PCB vendor logo, name	Silkscreen	No
Facebook P/N	Adhesive label	Yes
Date code (industry standard: WEEK/YEAR)	Adhesive label	Yes
DC input ratings	Silkscreen	No
RoHS compliance	Silkscreen	No
WEEE symbol:  The motherboard will have the crossed out wheeled bin symbol to indicate that it will be taken back by the manufacturer for recycling at the end of its useful life. This is defined in the European Union Directive 2002/96/EC of January 27, 2003 on Waste Electrical and Electronic Equipment (WEEE) and any subsequent amendments.	Silkscreen	No

13.2 Chassis Labels and Markings

With Honey Badger, the new Knox chassis and trays shall carry the following adhesive barcoded labels in visible locations where they can be easily scanned during integration.

Vendor and Facebook will have an agreement for the label locations.

Table 25 Chassis Label Requirements

Description
Vendor P/N, S/N, REV (revision would increment for any approved changes)
Facebook P/N (or OCP customer P/N)
Date code (industry standard: WEEK/YEAR)
The assembly shall be marked "THIS SIDE UP", "TOP SIDE", "UP ^" or other approved marking in bright, large characters in a color to be defined by ODM and Facebook (or OCP customer). This printing may be on the PCB itself, or on an installed component such as an air baffle. The label should be clear and easy to read in low light conditions, when viewed from above or below from 2 feet away and at an angle of approximately 60 degrees off horizontal.

14 Prescribed Materials

14.1 Sustainable Materials

Materials and finishes that reduce the life cycle impact of servers should be used where cost and performance are not compromised. This includes the use of non-hexavalent metal finishes, recycled and recyclable base materials and materials made from renewable resources, with associated material certifications.

Facebook identified plastic alternatives including polypropylene plus natural fiber (PP+NF) compounds that meet functionality requirements while reducing cradle to gate environmental impact when compared to PC/ABS. GreenGranF023T is one acceptable alternate material. JPSECO also offers a PP+NF material that is acceptable; the model number will be available at a later date. It is strongly preferred that such alternatives are identified and used. If vendor is unable to use this, or a similar alternate material, vendor will provide a list of materials that were considered and why they were not successfully incorporated.

14.2 Disallowed Components

The following components shall not be used in the design of the motherboard:

- Components disallowed by the European Union's Restriction of Hazardous Substances Directive (RoHS)
- Trimmers and/or potentiometers
- Dip switches

14.3 Capacitors and Inductors

The following limitations shall be applied to the use of capacitors:

- Only aluminum organic polymer capacitors from high-quality manufacturers are used; they must be rated 105°C
- All capacitors have a predicted life of at least 50,000 hours at 45°C inlet air temperature, under worst conditions
- Tantalum capacitors are forbidden
- SMT ceramic capacitors with case size > 1206 are forbidden (size 1206 still allowed when installed far from PCB edge, and with a correct orientation that minimizes risks of cracks)
- Ceramics material for SMT capacitors must be X7R or better material (COG or NP0 type should be used in critical portions of the design)

Only SMT inductors may be used. The use of through-hole inductors is disallowed.

14.4 Component De-Rating

For inductors, capacitors, and FETs, de-rating analysis should be based on at least 20% de-rating.

15 Honey Badger Interconnect Pin Definitions

Below are the full interconnected-pin definitions between the Honey Badger baseboard and the drive plane board. The connectors are placed such that Pin1 is towards the right side of the chassis.

15.1 Drive Plane Board Pin Definitions

This section lists the pin definitions on the Honey Badger DPB one A-side PCI-E connectors that the Honey Badger baseboard will interface with. Table 26 to Table 28 are for the three connectors, respectively.

Table 26 Honey Badger DPB Connector Pin Definition – Side A, Part I

A1	SAS_PRE0	SAS_PWR0	B1
A2	SAS_PRE1	SAS_PWR1	B2
A3	SAS_PRE2	SAS_PWR2	B3
A4	SAS_PRE3	SAS_PWR3	B4
A5	SAS_PRE4	SAS_PWR4	B5
A6	SAS_PRE5	SAS_PWR5	B6
A7	SAS_PRE6	SAS_PWR6	B7
A8	SAS_PRE7	SAS_PWR7	B8
A9	SAS_PRE8	SAS_PWR8	B9
A10	SAS_PRE9	SAS_PWR9	B10
A11	SAS_PRE10	SAS_PWR10	B11
Key	Key	Key	Key
A12	SAS_PRE11	SAS_PWR11	B12
A13	SAS_PRE12	SAS_PWR12	B13
A14	SAS_PRE13	SAS_PWR13	B14
A15	SAS_PRE14	SAS_PWR14	B15
A16	SELF_TRAY_IN	SAS_PWR15	B16
A17	PEER_TRAY_IN	PCI-E_MATED_A	B17
A18	**GND**	PEER_SEB_IN	B18

Table 27 Honey Badger DPB Connector Pin Definition – Side A, Part II

A1	GND	SAS_PRE15	B1
A2	SAS0_RX+	FCB_HW_REV	B2
A3	SAS0_RX-	GND	B3
A4	GND	SAS0_TX+	B4
A5	GND	SAS0_TX-	B5
A6	SAS1_RX+	GND	B6
A7	SAS1_RX-	GND	B7
A8	GND	SAS1_TX+	B8

A9	GND	SAS1_TX-	B9
A10	SAS2_RX+	GND	B10
A11	SAS2_RX-	DPB_HW_REV	B11
Key	Key	Key	Key
A12	Tray_ID	SAS2_TX+	B12
A13	GND	SAS2_TX-	B13
A14	SAS3_RX+	GND	B14
A15	SAS3_RX-	GND	B15
A16	GND	SAS3_TX+	B16
A17	GND	SAS3_TX-	B17
A18	SAS4_RX+	GND	B18
A19	SAS4_RX-	GND	B19
A20	GND	SAS4_TX+	B20
A21	GND	SAS4_TX-	B21
A22	SAS5_RX+	GND	B22
A23	SAS5_RX-	GND	B23
A24	GND	SAS5_TX+	B24
A25	GND	SAS5_TX-	B25
A26	SAS6_RX+	GND	B26
A27	SAS6_RX-	GND	B27
A28	GND	SAS6_TX+	B28
A29	GND	SAS6_TX-	B29
A30	SAS7_RX+	GND	B30
A31	SAS7_RX-	GND	B31
A32	GND	SAS7_TX+	B32
A33	**GND**	**SAS7_TX-**	B33
A34	**SAS8_RX+**	**GND**	B34
A35	**SAS8_RX-**	**GND**	B35
A36	**GND**	**SAS8_TX+**	B36
A37	**GND**	**SAS8_TX-**	B37
A38	**SAS9_RX+**	**GND**	B38
A39	**SAS9_RX-**	**GND**	B39
A40	**GND**	**SAS9_TX+**	B40
A41	Shutdown_Release	**SAS9_TX-**	B41
A42	SAS1_FLT	**GND**	B42
A43	SAS0_FLT	SAS9_FLT	B43
A44	SAS2_FLT	SAS10_FLT	B44
A45	SAS3_FLT	SAS11_FLT	B45
A46	SAS4_FLT	SAS12_FLT	B46
A47	SAS5_FLT	SAS13_FLT	B47

A48	SAS6_FLT	**GND**	B48
A49	SAS7_FLT	**SAS10_TX+**	B49
A50	SAS8_FLT	**SAS10_TX-**	B50
A51	**GND**	**GND**	B51
A52	**SAS10_RX+**	SAS14_FLT	B52
A53	**SAS10_RX-**	SAS15_FLT	B53
A54	**GND**	SEB_HTBT_OUT	B54
A55	SCL_C	SEB_HTBT_IN	B55
A56	SDA_C	SCL_B	B56
A57	SCL_D	SDA_B	B57
A58	SDA_D	SEB_ID	B58
A59	**GND**	PWM_OUT	B59
A60	**SAS11_RX+**	PEER_SEBA_HB	B60
A61	**SAS11_RX-**	**GND**	B61
A62	**GND**	**SAS11_TX+**	B62
A63	**GND**	**SAS11_TX-**	B63
A64	**SAS12_RX+**	**GND**	B64
A65	**SAS12_RX-**	**GND**	B65
A66	**GND**	**SAS12_TX+**	B66
A67	**GND**	**SAS12_TX-**	B67
A68	**SAS13_RX+**	**GND**	B68
A69	**SAS13_RX-**	**GND**	B69
A70	**GND**	**SAS13_TX+**	B70
A71	**GND**	**SAS13_TX-**	B71
A72	**SAS14_RX+**	**GND**	B72
A73	**SAS14_RX-**	**GND**	B73
A74	**GND**	**SAS14_TX+**	B74
A75	**GND**	**SAS14_TX-**	B75
A76	**SAS15_RX+**	**GND**	B76
A77	**SAS15_RX-**	**GND**	B77
A78	**GND**	**SAS15_TX+**	B78
A79	PEER_SEBB_HB	**SAS15_TX-**	B79
A80	**12V**	**GND**	B80
A81	**12V**	**GND**	B81
A82	**12V**	**GND**	B82

Table 28 Honey Badger DPB Connector Pin Definition – Side A, Part III

A1	PCI-E_MATED_B	**GND**	B1
A2	**12V**	**GND**	B2

A3	**12V**	**GND**	B3
A4	**12V**	**GND**	B4
A5	**12V**	**GND**	B5
A6	**12V**	**GND**	B6
A7	**12V**	**GND**	B7
A8	**12V**	N/C	B8
A9	N/C	N/C	B9
A10	N/C	N/C	B10
A11	N/C	N/C	B11
Key	Key	Key	Key
A12	N/C	GND	B12
A13	GND	N/C	B13
A14	N/C	N/C	B14
A15	N/C	GND	B15
A16	GND	N/C	B16
A17	N/C	N/C	B17
A18	GND	GND	B18

16 Honey Badger Storage System Error Code Definitions

This section lists the full definitions of Honey Badger storage system error codes. These codes are displayed on the debug card when switch button selected, and are stored in the storage system event log.

Table 29 Storage Enclosure Error Code Definition

Error Code	Description	Error Code	Description
00	No error	50	HDD0 SMART temp critical
01	Expander A fault	51	HDD1 SMART temp critical
02	Expander B fault	52	HDD2 SMART temp critical
03	I2C bus A crash	53	HDD3 SMART temp critical
04	I2C bus B crash	54	HDD4 SMART temp critical
05	I2C bus C crash	55	HDD5 SMART temp critical
06	I2C bus D crash	56	HDD6 SMART temp critical
07	Reserved	57	HDD7 SMART temp critical
08	Reserved	58	HDD8 SMART temp critical
09	Reserved	59	HDD9 SMART temp critical
10	Reserved	60	HDD10 SMART temp critical
11	Fan 1 front fault	61	HDD11 SMART temp critical
12	Fan 1 rear fault	62	HDD12 SMART temp critical
13	Fan 2 front fault	63	HDD13 SMART temp critical

14	Fan 2 rear fault	64	HDD14 SMART temp critical
15	Fan 3 front fault	65	Expander A Internal temp critical
16	Fan 3 rear fault	66	Expander B Internal temp critical
17	Fan 4 front fault	67	Reserved
18	Fan 4 rear fault	68	Reserved
19	Fan 5 front fault	69	Reserved
20	Fan 5 rear fault	70	HDD0 fault
21	Fan 6 front fault	71	HDD1 fault
22	Fan 6 rear fault	72	HDD2 fault
23	Reserved	73	HDD3 fault
24	Reserved	74	HDD4 fault
25	Reserved	75	HDD5 fault
26	Reserved	76	HDD6 fault
27	Reserved	77	HDD7 fault
28	Reserved	78	HDD8 fault
29	Reserved	79	HDD9 fault
30	Reserved	80	HDD10 fault
31	Drive board temp sensor 1 critical	81	HDD11 fault
32	Drive board temp sensor 2 critical	82	HDD12 fault
33	Drive board temp sensor 3 critical	83	HDD13 fault
34	Drive board temp sensor 4 critical	84	HDD14 fault
35	Expander temp sensor A critical	85	Reserved
36	Expander temp sensor B critical	86	Reserved
37	Ambient temp sensor A1 critical	87	Reserved
38	Ambient temp sensor A2 critical	88	Reserved
39	Ambient temp sensor B1 critical	89	Reserved
40	Ambient temp sensor B2 critical	90	External Mini-SAS Link Error
41	BJT temp sensor 1 critical	91	Internal Mini-SAS 1 Link Error
42	BJT temp sensor 2 critical	92	Internal Mini-SAS 2 Link Error
43	Reserved	93	Self Tray Pulled-out
44	Reserved	94	Peer Tray Pulled-out
45	Expander voltage sensor critical	95	Reserved
46	Drive plane board voltage sensor critical	96	Reserved
47	Fan Control Board voltage sensor critical	97	Reserved
48	Fan Control Board current sensor critical	98	Reserved
49	Reserved	99	Firmware and Hardware Mismatch

17 Revision History

Version	Date	Changes
0.7	12/3/2014	Initial version submitted for OCP review.