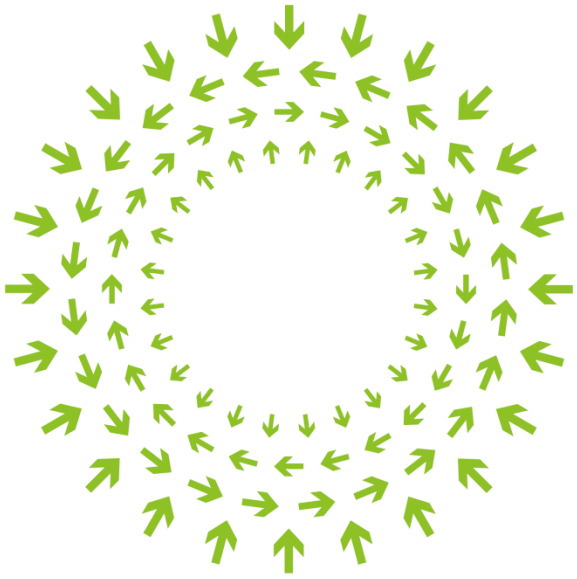

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Project Olympus
Cavium ThunderX2™ ARMx64
Motherboard Specification

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Revision History

Table 1. Revision History

Date	Description
11/1/2017	Version 1.0

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1 Project Olympus Specifications List

Table 2 lists the Project Olympus system specifications.

Table 2. List of Specification

Specification Title	Description
Project Olympus Server Rack Specification	Describes the mechanical rack hardware used in the system
Project Olympus Server Mechanical Specification	Describes the mechanical structure for the server used in the system.
Project Olympus Universal Motherboard Specification	Describes the server motherboard general requirements.
Project Olympus Server Power Supply	Describes the Power Supply Unit (PSU) used in the server
Project Olympus Power Management Distribution Unit Specification	Describes the Power Management Distribution Unit (PMDU).
Project Olympus Rack Manager Specification	Describes the Rack Manager PCBA used in the PMDU.

This document is intended for designers and engineers who will be building servers for Project Olympus systems.

2 Overview

This specification focuses on the Project Olympus Cavium ThunderX2™ ARMx64 Motherboard. This is an implementation specific specification under the Project Olympus Universal Motherboard Specification.

Refer to respective specifications for other elements of the Project Olympus system such as Power Supply Unit (PSU), Rack Manager (RM), Power and Management Distribution Unit (PMDU), and Server Rack.

This specification covers block diagram, management sub-system, power management, FPGA Card support, IO connectors, and physical specifications of the Server Motherboard.

3 Background

The server motherboard is the computational element of the server. The motherboard includes a full server management solution and supports interfaces to integrated or rear-access 12V Power Supply Units (PSUs).

The server optionally interfaces to a rack-level Power and Management Distribution Unit (PMDU).

The PMDU provides power to the Server and interfaces to the Rack Manager (RM).

The motherboard design provides optimum front-cable access (cold aisle) for external IO such as networking and storage as well as standard PCIe cards. This enables flexibility to support many configurations.

4 Block Diagram

Figure 1 shows the baseline block diagram describing general features for the server motherboard.

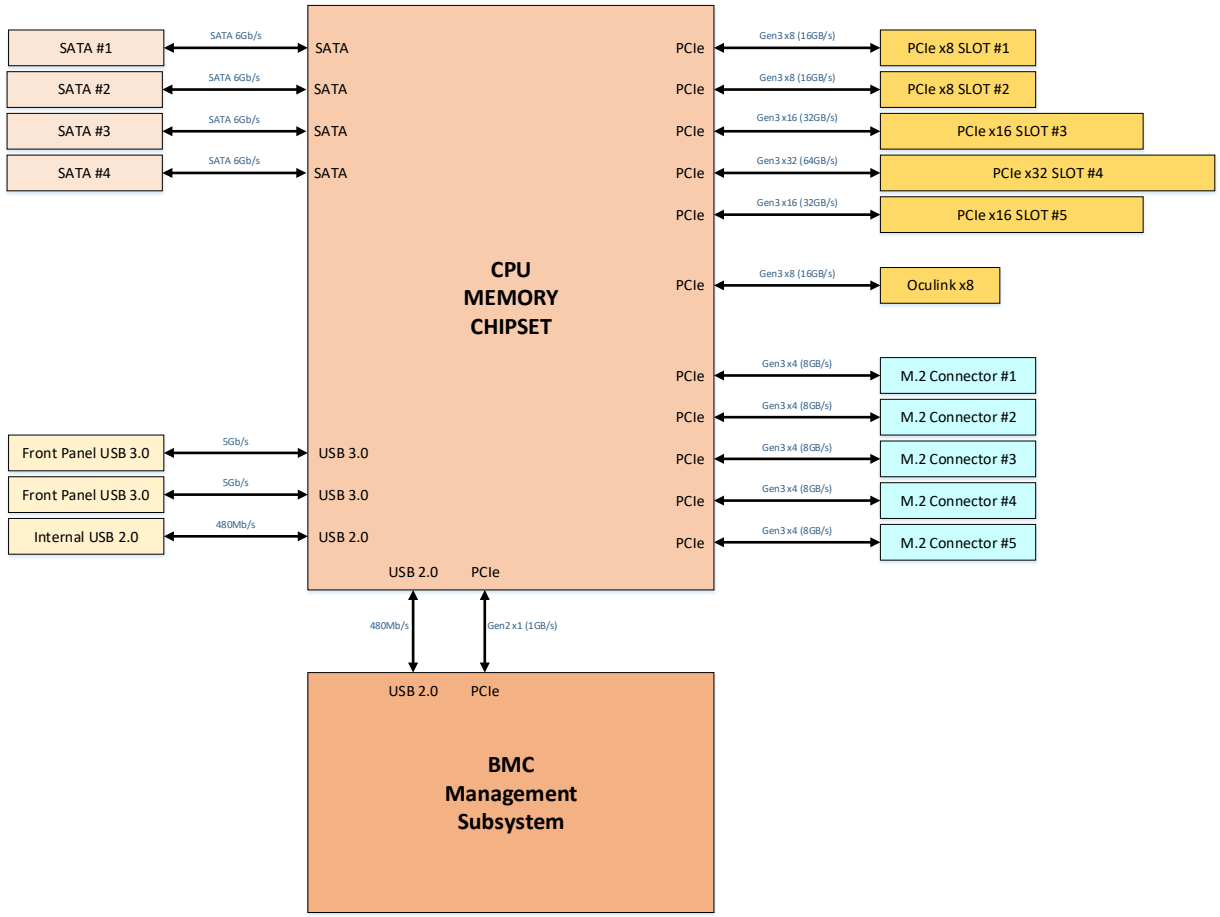


Figure 1. Top Level Block Diagram

5 Features

The motherboard includes support for the following features:

Table 3: Motherboard Features

Processor	
Platform	Cavium ThunderX2™ Platform
CPU	Cavium ThunderX2™ processors
Sockets	Dual socket operation
TDP Wattage	Up to 195W (Support for all server class SKUs)
Memory	
DIMM Slots	24 total DIMM slots on 16 memory channels (8 per CPU)
DIMM Type	Double data rate fourth generation (DDR4) Registered DIMM (RDIMM) with Error-Correcting Code (ECC)
DIMM Speed	DDR4-2400 (2DPC), DDR4-2666 (1DPC)
DIMM Size	16GB, 32GB, 64GB
Capacities Supported	128GB, 256GB, 512GB, 756GB, 1TB
Storage	
SATA	4 local ports @ 6.0 Gb/s
Server Management	
Chipset	BMC ASPEED AST2500 series
Interface	Representational State Transfer (REST) API Windows Management Instrumentation (WMI) Open Management Interface (OMI) Command-Line Interface (CLI)
System Firmware	
BIOS	Unified Extensible Firmware Interface (UEFI)

BMC	AMI
Security	Trusted Platform Module (TPM 2.0) Secure Boot
PCI-Express Expansion	
2 PCIe x8 Slots	Supports PCIe M.2 Riser Cards
2 PCIe x16 Slots	Supports standard PCIe x16 cards
1 PCIe x32 Slot	Supports standard PCIe x16, butterfly PCIe 2x16
5 M.2 Slots	Supports 60mm, 80mm, and 110mm M.2 Cards
1 PCIe x8 Expansion	1 Oculink x8
Networking	
LOM	N/A
MGMT	1x 1GbE from BMC to RJ45 Connector

5.1 CPU

The server supports two Cavium ThunderX2™ CPUs for all server class SKUs. The maximum TDP to be supported is 195W.

5.2 DIMMs

The motherboard supports 24 DDR4 RDIMMs on 16 memory channels. 8 channels with two DIMMs slots per channel and 8 channels with one DIMM slot per channel. It supports all available configurations for single, dual, and quad rank RDIMMs supported by Cavium ThunderX2™ Platform. The DIMM sockets shall also support NVDIMM as described in this document.

The following is supported on all DIMM slots:

- 8-Gbit DRAM
- 16-Gbit DRAM (Not Validated)
- RDIMMs
- DDR4 NVDIMM – 12V support through the NVDIMM connector
- 3DS RDIMM (Not Validated)

Though the DIMM technology are supported, it should be noted that not all have been validated and tested. Example includes: 16-Gbit DRAM, and 3DS RDIMMs.

5.3 PCIe Support

5.3.1 PCIe x8 Slots

The motherboard supports two PCIe x8 slots as shown in Figure 2, PCIe Slot #1 and Slot #2. Each slot supports 1x8 and 2x4 bifurcation. 2x4 bifurcation is supported at the connector with the addition of a 2nd PCIe clock to the standard PCIe pinout. The primary purpose of the slots is to support M.2 Modules with each slot capable of supporting two modules. Use of the modules requires a PCIe riser edge card to connect the modules to the PCIe bus. The riser can support 60mm, 80mm, and 110mm M.2 Modules.

5.3.2 PCIe x16 Slots

The motherboard supports two PCIe x16 slots as shown in Figure 2, PCIe Slot #3 and Slot #5. Each slot supports a standard PCIe form factor card using a riser card to interface to the PCIe connector. The size of the card supported is dependent on the height of the tray assembly. 1U trays can support FHHL PCIe cards. 2U trays can support FHFL cards.

All slots support bifurcation below 1x16 but utilize the standard PCIe connector pinout and do not contain additional clocks. Additional clocks required for bifurcation below 1x16 is handled with buffer circuitry on the PCIe card.

5.3.3 PCIe x32 Slot

The motherboard supports one PCIe x32 slot as shown in Figure 2, PCIe Slot #4. The x32 slot can support standard PCIe form factor card(s) using a riser card that interfaces to the PCIe connector in a 1U configuration. This slot can be configured with two types of riser cards:

- A Butter riser card with x16 connector on each side of the PCB. This riser will allow two x16 FH/HL cards to be installed.
- A single-sided riser card with a x16 connector. The riser will allow one x16 FH/HL card to be installed.

The size of the card supported is dependent on the height of the tray assembly. Table 4 describes the type of riser cards and the sized card supported for each tray assembly height.

Table 4. PCIe x32 Slot Card Support

	Riser Card	1U	2U
SLOT #4	Butterfly Riser	FH/HL	FH/HL or FH/FL
	x16 Riser	FH/HL	FH/HL or FH/FL

5.3.3.1 Three PCIe Card Example

Figure 2 shows a front view of the server demonstrating the orientation of 3 standard PCIe cards.

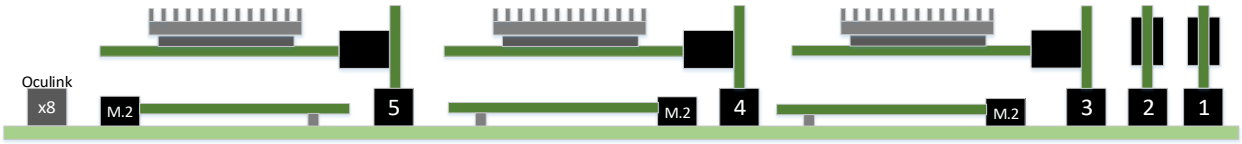


Figure 2. Three standard PCIe Cards

5.3.3.2 Four PCIe Card Example

Figure 3 shows a front view of the server demonstrating the orientation of two standard FH/FL PCIe cards and two 2 standard FH/HL PCIe cards.

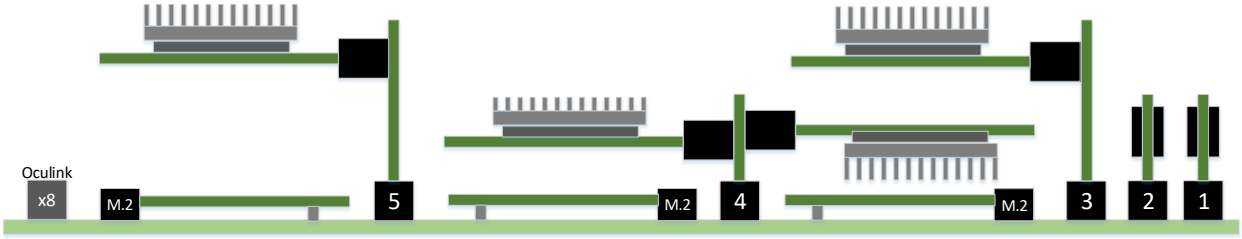


Figure 3. Four Standard PCIe Cards

To enable full height, full length cards in the 2U space, the PCIe riser cards is tall enough allowing cards to sit above the CPU heatsinks.

5.3.4 PCIe Cables

The motherboard supports an OCulink x8 connector. PCIe clock and control signals are driven through this cabling.

5.3.5 M.2 Modules

The M.2 devices are x4 PCIe Gen-3 interfaces (M.2 connector with M Key). These cards can be supported through any of the following methods:

- Standard M.2 connector mounted directly on the motherboard. The motherboard supports five on-board M.2 modules.
- Dual M.2 Interposer Module: PCIe card with two M.2. modules.
- Quad M.2 Carrier Card.: FHHL PCIe Card in standard PCIe format with four M.2. modules.

For both motherboard and PCIe Card applications, the supported M.2 modules are 60mm, 80mm, and 110mm dual sided form factors (Type 2260, 2280, and 22110).

5.3.6 CPU PCIe Mapping

Table 5 describes the PCIe port mapping between the CPUs and the PCIe endpoints.

Table 5. PCIe Slot to CPU Mapping

CPU	PCIe Bus	Destination

CPU0	*PCIE M*	M.2. Module #5
CPU0	*PCIE E-H*	PCIe Slot #3
CPU0	*PCIE I-L*	PCIe Slot #4a
CPU0	*PCIE A-B*	PCIe Slot #1
CPU0	*PCIE C-D*	PCIe Slot #2
CPU0	*PCIE N*	BMC
CPU1	*PCIE A-D*	PCIe Slot #4b
CPU1	*PCIE F*	M.2. Module #1
CPU1	*PCIE E*	M.2. Module #2
CPU1	*PCIE G*	M.2 Module #3
CPU1	*PCIE H*	M.2 Module #4
CPU1	*PCIE M-N*	OCulink x8
CPU1	*PCIE I-L*	PCIe Slot #5

5.4 SATA Storage

The motherboard provides support for cabling up to four SATA3.0 storage drives. This is accomplished with four x1 SATA connectors connected to CPU; two from CPU0 and two from of CPU1.

5.5 TPM Module

The motherboard includes a connector to support a TPM 2.0 module connected to CPU0 SPI bus.

5.6 FPGA Card Support

The motherboard supports an FHHL x16 or x32 PCIe form factor FPGA card in Slot #4. The motherboard supports an x8 OCulink connector for cabling an additional x8 PCIe Link from the motherboard or the Riser to the FPGA card as well as an internal USB connector to support FPGA debug.

6 Management Subsystem

The Management Controller circuitry for the motherboard uses the ASPEED AST2500 Baseboard Management Controller (BMC). This section describes the management features of the motherboard. Primary features include:

- BMC - ASPEED AST2500; optional AST2520 support
- BMC dedicated 1GbE LAN for communication with Rack Manager
- SSIF and IPMB connection between BMC and CPU
- CPU to support system management and monitoring capabilities

- Out of band environmental controls for power and thermal management
- FRUID EEPROM for storage of manufacturing data and events (I^2C)
- Thermal sensors for inlet and exhaust temperature monitoring (I^2C)
- Power monitoring through the 12V Hot Swap Controller circuitry (I^2C)
- Service LEDs

Figure 4 shows the management block diagram.

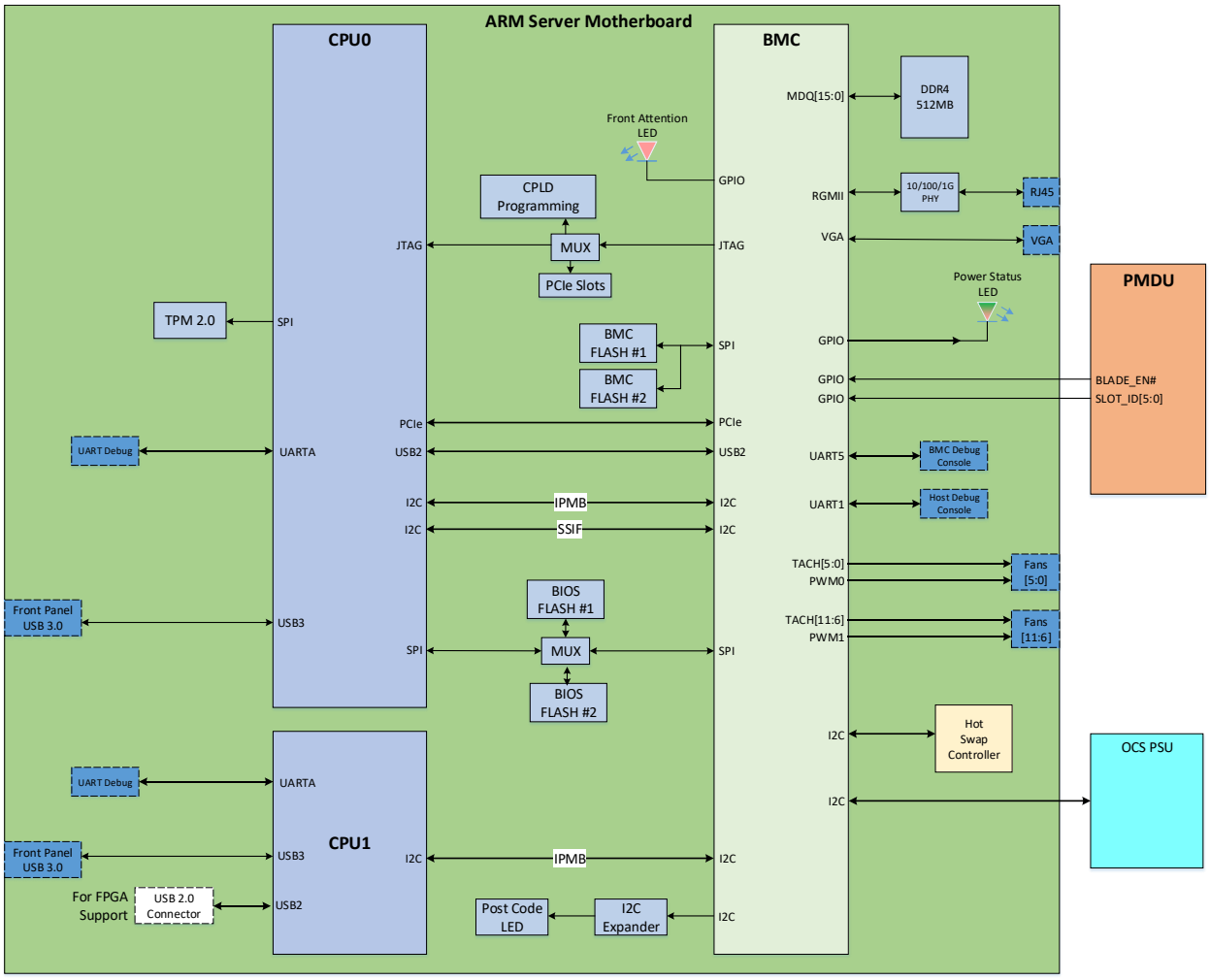


Figure 4: ARM Management Block Diagram

6.1 BMC

The design for the BMC is based on the ASPEED 2500 family and supports either the AST2500 or the AST2520. Primary features include:

- Embedded ARM Processor (ARM1176JZF-S 32-bit RISC CPU)
- Embedded 16KB/16KB Cache

- DDR4 Memory 512MB (supports up to 1GB)
- 8-bit ECC with error counter
- Redundant NOR/NAND/SPI flash memory
- 14 I2C/SMBus
- 5 UART Controllers
- LPC Bus Interface
- 228 GPIO Pins
- VGA port (AST2500 only)
- A single lane of PCIe (AST2500 only)

6.1.1 DRAM

The BMC supports of 512MB of DDR4 memory.

6.1.2 BMC Boot Flash

The BMC boots from a flash memory device located on the SPI bus. The device size is 256Mb (32MB) and support storing of FPGA and CPLD recovery images. Winbond W25Q256 or equivalent is supported. A secondary device is supported to provide BMC recovery.

6.1.3 BMC GPIO Mapping

BMC GPIO mapping is described in Project Olympus GPIO Guide documentation.

6.1.4 BIOS Flash

The BIOS utilizes one 256Mb (32MB) Flash BIOS device located on the CPU SPI bus. MXIC MPN MX25L25673GM2I or equivalent is supported. The BIOS is recoverable from the BMC in the event the chipset is inaccessible. It operates at 104MHz. The design also includes a BIOS Recover Jumper.

6.1.5 1GbE PHY

The server is managed through a 1GbE PHY connected to the BMC. An RJ45 connector located at the front of the server provides 1GbE connectivity to an external management switch. The PHY is from a Broadcom BCM54610 controller.

6.1.6 UARTS

The motherboard supports two debug UARTS connected to the BMC as follows:

- UART5 (Header 4) BMC Debug Console
- UART1 (Header 3) Host Debug Console

In addition, the motherboard supports two additional debug UARTS connected to the CPLD and CPU

- UART (Header 1) Boot Processor KD Serial Debugging
- UART (Header 2) Non-Boot Processor KD Serial Debugging

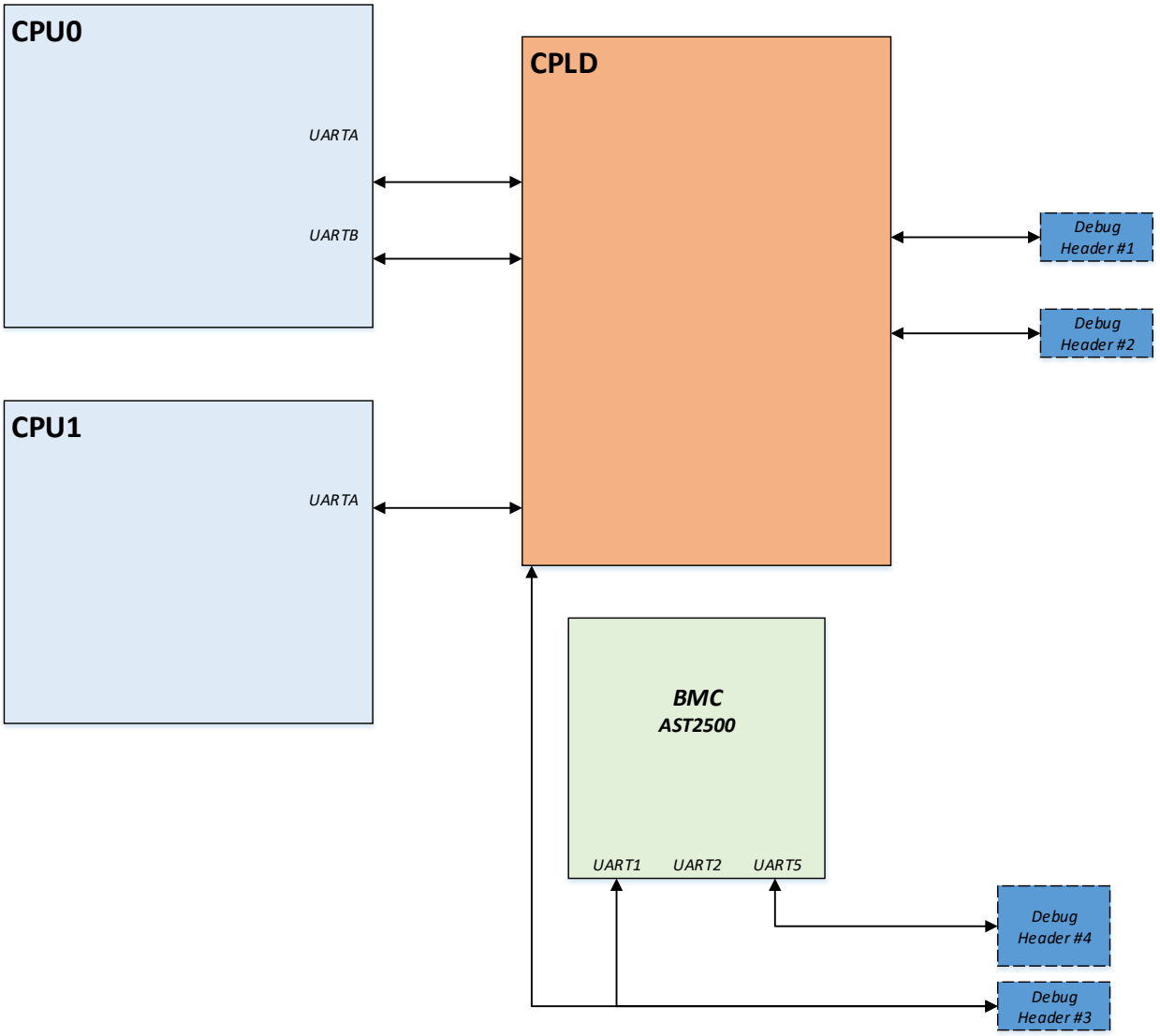


Figure 5. UART Debug Headers

6.2 CPU Thermal Monitoring

The BMC supports mechanisms to query CPU, Memory, and server thermal information to provide optimized fan speed control.

The CPU core includes integrated temperature sensors, and the CPU has five more sensors spread around it's die. The sensors can be reported external to the BMC via the IPMB. There are two IPMB connection made to the BMC. CPU0 IPMB is connected to I2C5 on the BMC. CPU1 IPMB is connected to I2C11 on the BMC. The system management can provide minimum, maximum, and average temperatures to the BMC.

The BMC also read sensor values for DIMMs, VRMs, and the inlet and outlet motherboard TMP75 sensors.

6.3 VGA

The motherboard includes optional support for VGA assuming the AST2500 processor. To support VGA, PCIe is provided from the PCIEN_[RX/TX]0_[N/P] PCIe port of CPU0.

6.4 I^2C

To optimize telemetry gathering for power and thermal management as well as general management of the server assembly, the following functions supports I^2C access from the BMC.

- All PCIe slots
- All M.2 modules
- Local hot swap controllers
- Management connector and Expansion management connector
- Key voltage regulators
- Temperature sensors
- FRUID PROM

The design shall include several I2C devices/functions available to the BMC. A brief description of the entities is included below I2C Mapping Diagram. Some of the blocks are specific with respect to the requirements of the device and its slave address.

Electrical isolation of components was taken into consideration. Ex: Devices that were required to be powered from separate power domains, but also located on the same I2C bus.

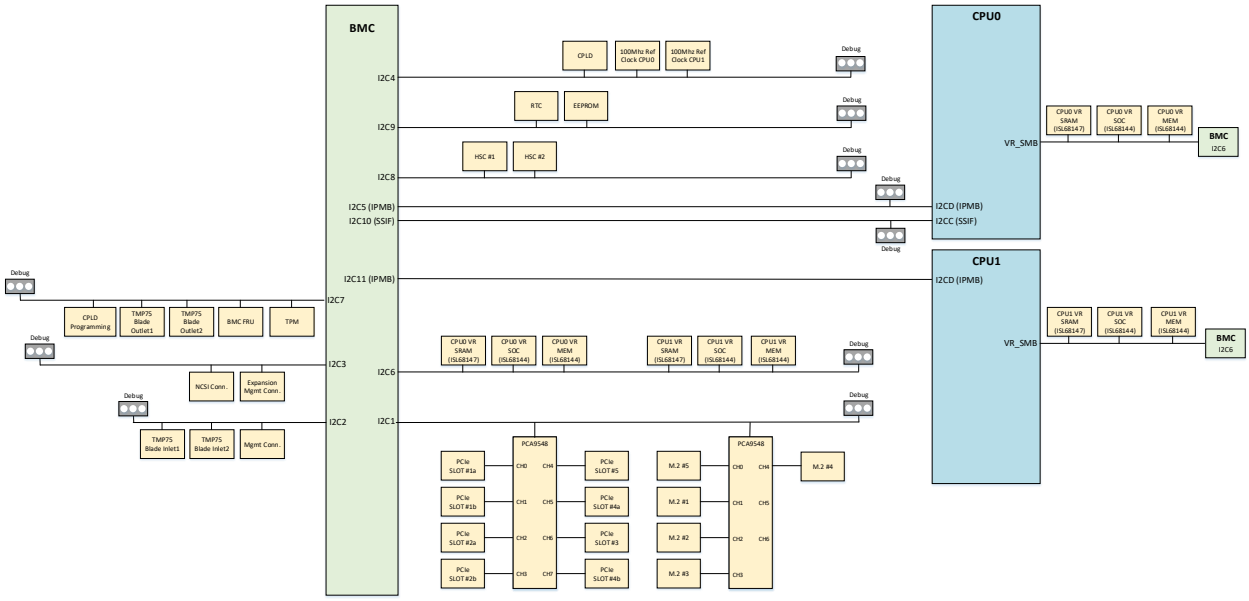


Figure 6: BMC I2C Mapping

6.4.1 FRUID PROM

The motherboard includes I2C support for a 64Kb serial EEPROM MPN AT24C64 or equivalent for storing manufacturing data.

6.4.2 Voltage Regulators

The motherboard includes I2C support for all CPU and Memory Subsystem voltage regulators enabling the BMC to monitor health of the individual power rails.

6.4.3 Temperature Sensors

The motherboard includes I^2C support for four temperature sensors, MPN TMP75, for monitoring the inlet and outlet air temperatures of the motherboard. The motherboard also includes provisions to support temperature monitoring of all DIMMs (SPD) and all PCIe slots including M.2s. The DIMM I2C interfaces with the CPU. The CPU reports the temperature to the BMC through the IPMB interface.

6.5 JTAG Master

The motherboard supports JTAG programming of programmable logic devices using the BMC's JTAG master controller. The JTAG programming is supported to any required CPLDs and PCIe slots designated for FPGA Cards, PCIe Slot 3, Slot 4, Slot 5. In addition, a JTAG Header hangs off of CPU0 and CPU1

enabling addition debug capability to the CPUs. The board contains mux circuitry controlled by the BMC to switch between the two programming paths. A block diagram is shown below.

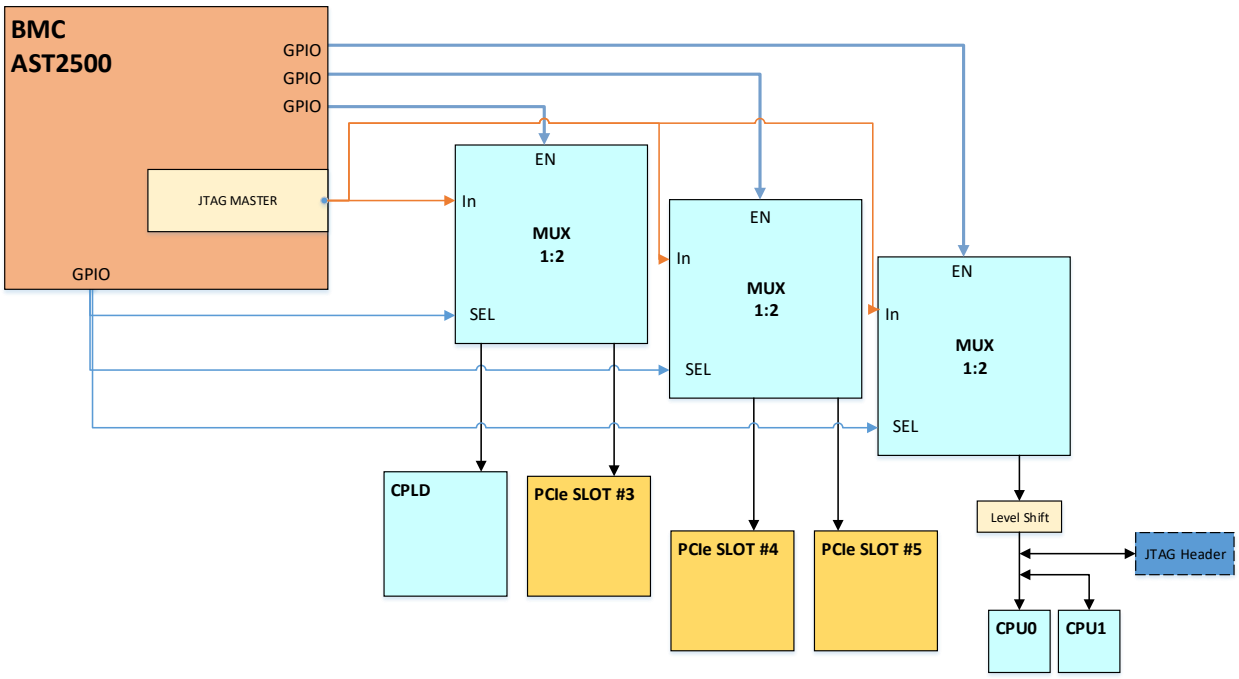


Figure 7. JTAG Programming

6.6 Jumpers

The design includes appropriate debug jumpers.

Table 6. Jumpers

Jumper Name	Default Position	Detected By	Function
BMC Disable (default)	High (not installed)	BMC	Disables BMC (sets all pins to High impedance)
BMC FRU Write Protect	Low (1,2)	BMC	Enable BMC FRU Write Protect
BIOS SPI CTRL	CPU (1,2)	BIOS	Select CPU or BMC SPI control for BIOS flash
BIOS Backup SEL	BIOS0 (1,2)	BIOS	Select BIOS backup – BIOS0 (1,2) or BIOS1 (2,3)
BIOS USB Recovery	Low (1,2 short)	BIOS	Enables BIOS recovery via USB image update

6.7 LEDs

The following sections describe the light-emitting diodes (LEDs) used as indicators on the motherboard. Table 7 lists the LEDs and provides a brief description. Greater detail for some LEDs is included in subsequent sections below. All LEDs are made visible at the front of the motherboard (cold aisle).

Table 7. LEDs

LED Name	Color	Description
UID LED	Blue	Unit Identification LED
Attention LED	Red	Indicates that Server requires servicing

Power Status LED	Amber/Green	Indicates Power Status of the Server
SATA HDD Activity	Green	Indicates R/W activity to HDDs
Post Code	Green	Indicates the Boot status of the Server
Catastrophic Error	Red	Indicates that a CPU catastrophic error has occurred
BMC Heartbeat	Green	Blinks to indicate BMC is alive
GbE Port 0 Activity	Green	Indicates activity on 1GbE Port 0 (not supported for production)
GbE Port 0 Speed	Green/Orange	Green=high speed, Orange=Low speed (not supported for production)
PSU1 Status LED1 (P2010)	Green	Status LED for PSU1 • Solid Green = AC and DC Power Good • Blinking Green = Battery Power Good
PSU1 Status LED2 (P2010)	Amber	Status LED for PSU1 • Solid Amber = Failure of PSU Phase • Blinking Amber = Failure of 2 PSU Phases
PSU2 Status LED1 (P2010)	Green	Status LED for PSU2 (optional) • Solid Green = AC and DC Power Good • Blinking Green = Battery Power Good
PSU2 Status LED2 (P2010)	Amber	Status LED for PSU2 (optional) • Solid Amber = Failure of PSU Phase • Blinking Amber = Failure of 2 PSU Phases

6.7.1 UID LED

The motherboard supports a blue UID (unit ID) LED used to help visually locate a specific server within a datacenter.

6.7.2 Power Status LED

When a server is initially inserted, the Power Status LED turns amber if 12V is present at the output of the Hot Swap Controller. This assures that the 12V power is connected and present at the motherboard and that the Hot-swap Controller (HSC) is enabled.

When the server management software turns on the system power (CPU/Memory/PCIe), the Power Status LED turns green. Note that the power status LED may be driven by an analog resistor network tied directly to a power rail and is not an indication of the health of the server. Table 8 describes the operation of the Power Status LED.

Table 8. Power Status LED Description

LED status	Condition
Off	12V power is absent or PWR_EN# is de-asserted
Solid Amber ON	PWR_EN# is asserted and 12V power output of the Hot Swap Controller is present.
Solid Green ON	Indicates that the management (BMC or IE) is booted and system power is enabled (CPU/Memory/PCIe).

6.7.3 Attention LED

The Attention LED directs the service technicians to the server that requires service. When possible, server diagnostics are used to direct repairs. Alternately, the Microsoft scale-out management software can be used. In both cases, event logs of the repair work are available.

The LED is driven by a single BMC GPIO. Table 9 describes the operation of the Attention LED.

Table 9. Attention LED Description

LED status	Condition
Off	No attention indicated
Solid RED	System needs attention

6.7.3.1 PSU Status LEDs

The motherboard supports four PSU status LEDs (2 per PSU). Each PSU is comprised of 2 individual status LEDs indicating the PSU status. These LEDs support the WCS P2010 PSU. Standard PSUs may not support external LEDs.

6.8 Fan Control

The motherboard supports control of twelve fans located at the rear of the server assembly. Fan control is divided between two connectors enabling two separate fan zones. Each connector supports 12V power, a single PWM, and six TACH signals for controlling up to 6 fans in a single zone. The motherboard supports two separate fan zones.

6.9 SPD Block Diagram

Figure 8 below details the SPD I2C bus for the DDR4 memory. The SPD bus is set to CPU access by default. The CPU controls the SPD bus.

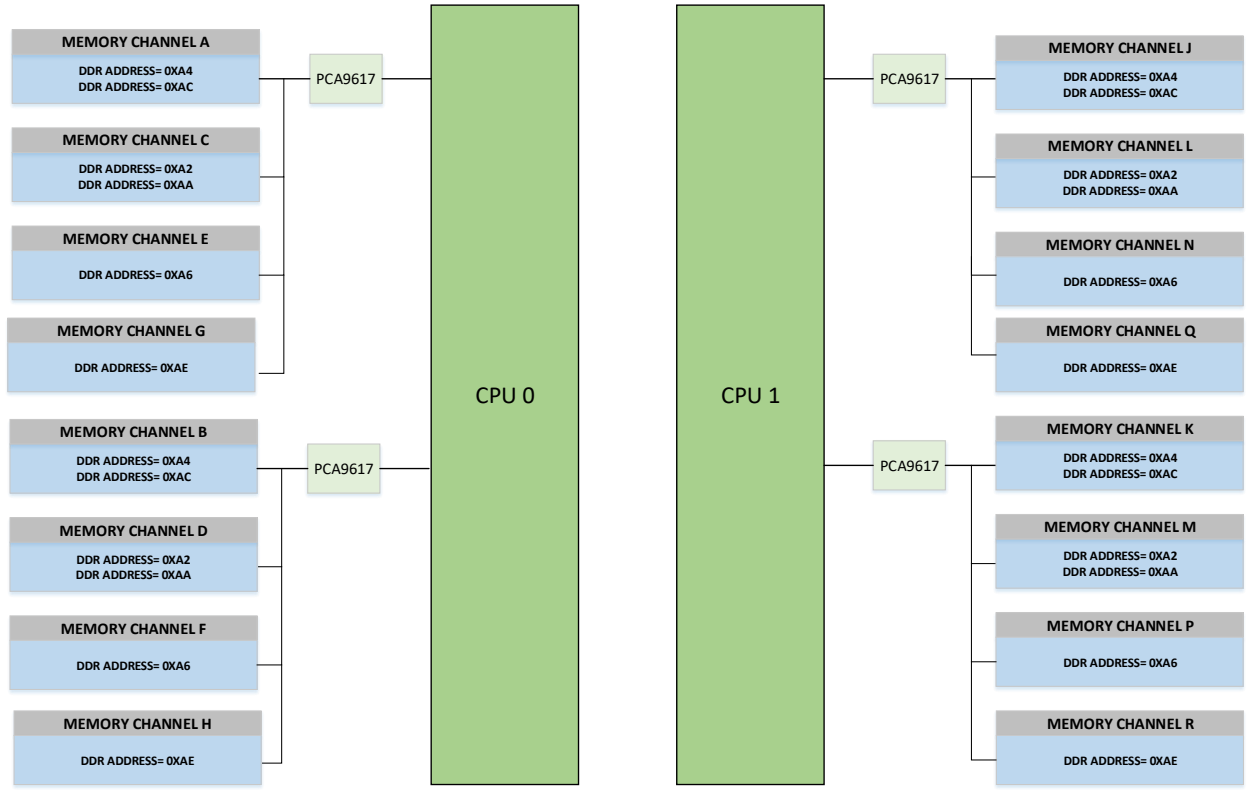


Figure 8. SPD Block Diagram

7 Power Management

The motherboard provides a rear connector for interfacing the motherboard to a 12V PSU. The motherboard also provides a rear management connector for enabling external control of server power. A block diagram of the interface is shown Figure 9.

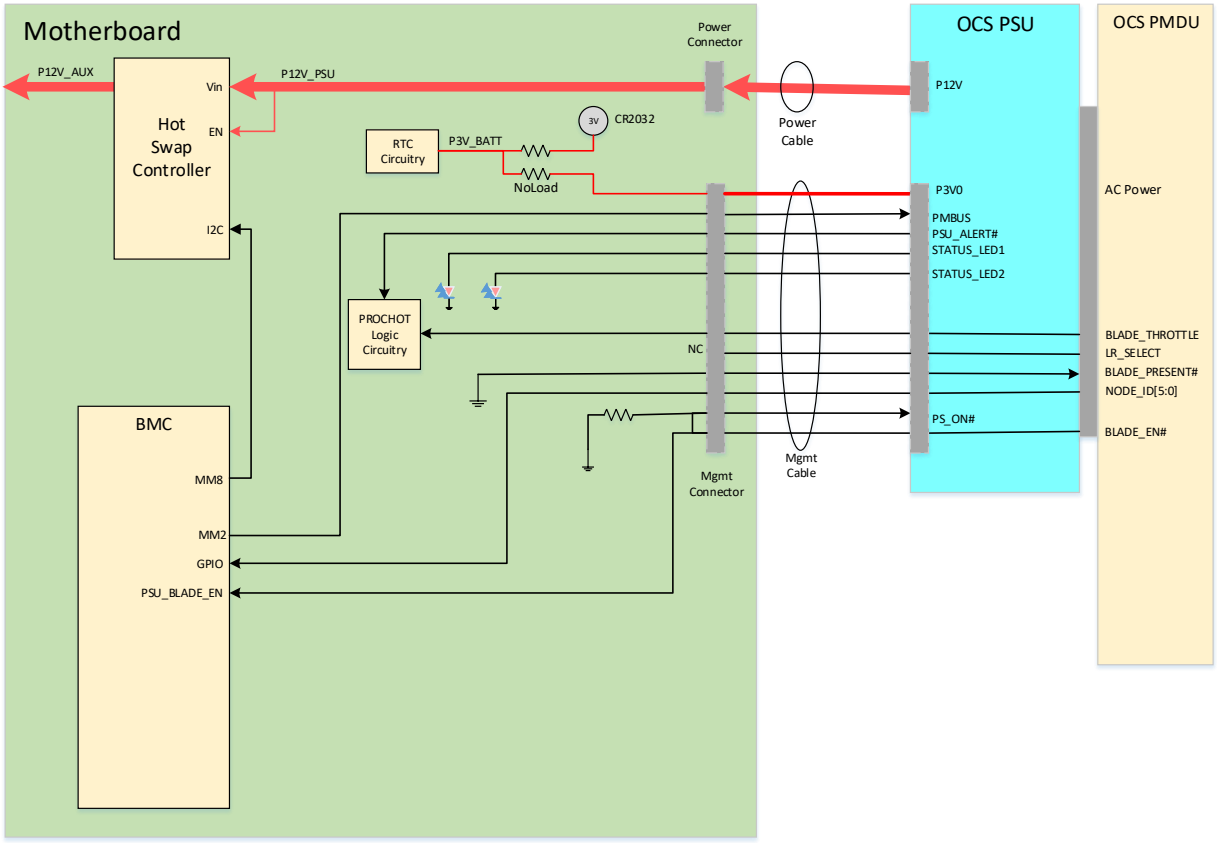


Figure 9. Power Management Block Diagram

7.1 Rack Management

The Rack Manager communicates with the server motherboard through the PMDU. The following describes the management interfaces.

- BLADE_EN# - Active low signal used to enable/disable power to the P2010 PSU. A 1K ohm pulldown resistor is used on the motherboard to ensure a default low state (active) if the Rack Manager is not present. This signal connects to the PS_ON# signal of the PSU. When in high state (inactive), this signal disables output power from the P2010 PSU. This signal also connects to the BMC so that the BMC can disable logging as soon as power is disabled.
- SERVER_PRESENT# - Active low signal used to communicate physical presence of the server to the Rack Manager. This signal should be tied to GND on the motherboard.
- SERVER_THROTTLE - Active high signal used to put the motherboard into a low power (power cap) state. This signal should default low (inactive) if the Rack Manager is not present. This signal

is fanned out from the Rack Manager to multiple servers and therefore the circuit design supports electrical isolation of this signal from the motherboard power planes.

- SLOT_ID[5:0] – Identifies the physical rack slot in which the server is installed. ID is hard set by the PMDU.
- LR_SELECT – Spare signal. Used to differentiate between left and right slots for a dual-node implementation.

Table 10. Slot ID Decode

Slot	SLOT_ID[5:0]	Slot	SLOT_ID[5:0]
Slot 1	000000	Slot 25	100000
Slot 2	000001	Slot 26	100001
Slot 3	000010	Slot 27	100010
Slot 4	000011	Slot 28	100011
Slot 5	000100	Slot 29	100100
Slot 6	000101	Slot 30	100101
Slot 7	001000	Slot 31	101000
Slot 8	001001	Slot 32	101001
Slot 9	001010	Slot 33	101010
Slot 10	001011	Slot 34	101011
Slot 11	001100	Slot 35	101100
Slot 12	001101	Slot 36	101101
Slot 13	010000	Slot 37	110000
Slot 14	010001	Slot 38	110001
Slot 15	010010	Slot 39	110010
Slot 16	010011	Slot 40	110011
Slot 17	010100	Slot 41	110100
Slot 18	010101	Slot 42	110101
Slot 19	011000	Slot 43	111000
Slot 20	011001	Slot 44	111001
Slot 21	011010	Slot 45	111010
Slot 22	011011	Slot 46	111011
Slot 23	011100	Slot 47	111100
Slot 24	011101	Slot 48	111101

7.2 PSU Management

The motherboard supports management of the P2010 PSU. Below is a description of the signals supported by the PMDU.

- PS_ON# - Active low signal used to enable/disable power to the PSU. This signal is driven by the PWR_EN# signal from the Rack Manager. A 1K ohm pulldown resistor is used on the motherboard to ensure a default low state if the RM is not present.
- PSU_ALERT# - Active low signal used to alert the motherboard that a fault has occurred in the PSU. Assertion of this signal by the PSU puts the motherboard into a low power (PROCHOT) state. This signal is also connected to the BMC for monitoring of PSU status.
- PMBUS – I^2C interface to the PSU. The BMC uses this signal is used by the BMC to read the status of the PSU.
- STATUS_LED – Controls LED to provide visual indication of a PSU fault.

7.3 Hot Swap Controller

For in-rush current protection on the motherboard, a hot swap controller (HSC) that includes support for the PMBUS interface is used on the motherboard. The ADM1278 HSC is made available to BMC I2C and provides its ALERT# signal to the BMC. The signals are dedicated to the HSC to provide fast response time to power excursions. In the case of future expansions, a 2nd HSC made available on BMC I2C as well.

7.4 Power Capping

The motherboard supports throttling of the processors using the Fast PROCHOT mechanism based on monitoring of the motherboards input voltage and power. A block diagram detailing these triggers is shown in Figure 10.

The following triggers are monitored by the BMC can directly generate PROCHOT# events. Each trigger is filtered by the CPLD and the CPLD ensure that any trigger event generates a minimum 100mS PROCHOT# pulse.

- Undervoltage – A comparator monitors the 12V output of the HSC and asserts if this voltage falls below 11.5V.
- Overcurrent Alert – The HSC monitors the input current and asserts the trigger if the input current exceeds 93A.
- Overcurrent Protect – The HSC monitors the input current and disables power to the motherboard if the current exceeds 95A.
- HSC ALERT #1 and #2 – The HSC provides two programmable alerts. These alerts are spare inputs and are disabled by default.

Note that the CPU voltage regulators also can generate PROCHOT triggers to the CPUs.

The motherboard enables power capping of the server from different trigger sources. Assertion of either of the following causes the motherboard to assert PROCHOT and the BMC to initiate power capping of the server. Each of these triggers can be disabled by the BMC. In addition, the BMC can trigger these events for debugging.

- RM THROTTLE# - Throttle signal driven by the Rack Manager indicating that the rack has exceeded its power limit.
- PSU ALERT# - Alert signal driven by the PSU. Assertion indicates an over-current event or that the Olympus PSU has transitioned its power source from AC to battery backup.
- SPARE - Test signal that allows BMC to assert power cap

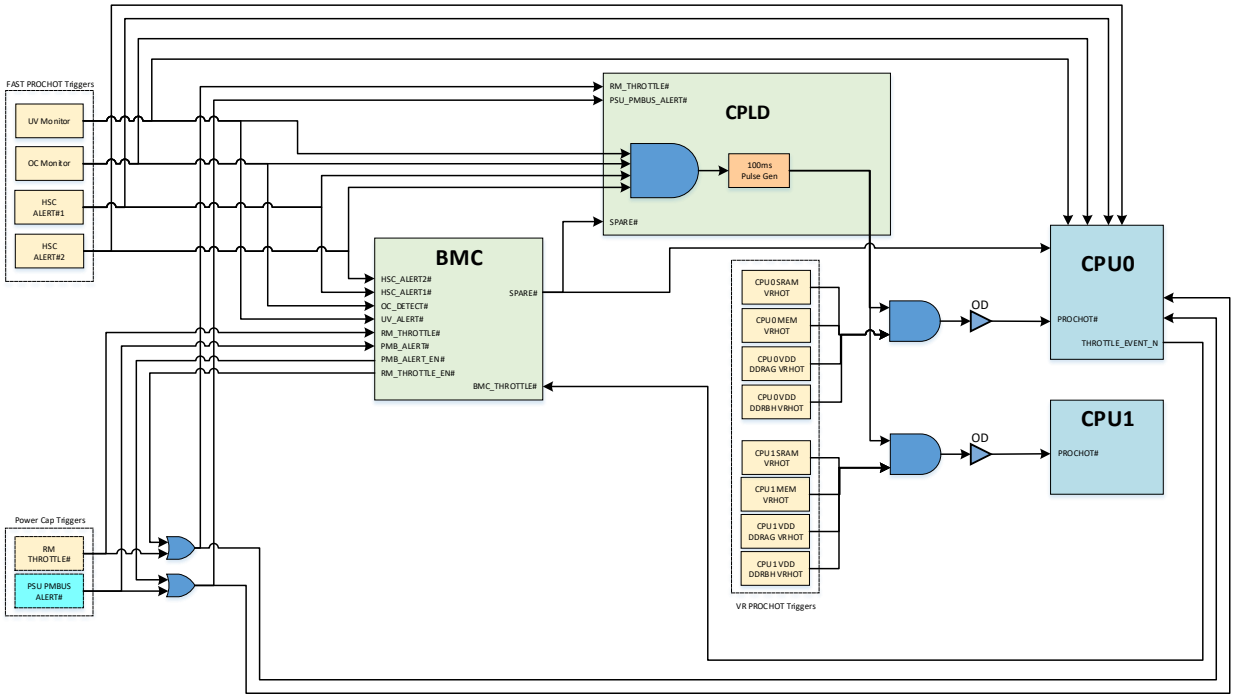


Figure 10. Power Capping

All triggers can also inform CPU0 of an asserted event. The CPU can also determine what additional actions are needed during a power event.

7.5 PWRBRK#

The motherboard supports Emergency Power Reduction mechanism (PWRBRK#) for the x16 and x32 PCIe slots. The primary purpose is to provide a power reduction mechanism for PCIe cards as part of the throttle and power capping strategy. Figure 11 shows the block diagram for PWRBRK#. PWRBRK# can be triggered by either the RM_THROTTLE# or PSU2_ALERT#. The BMC controls enable/disable monitoring of the two triggers and can also force an event.

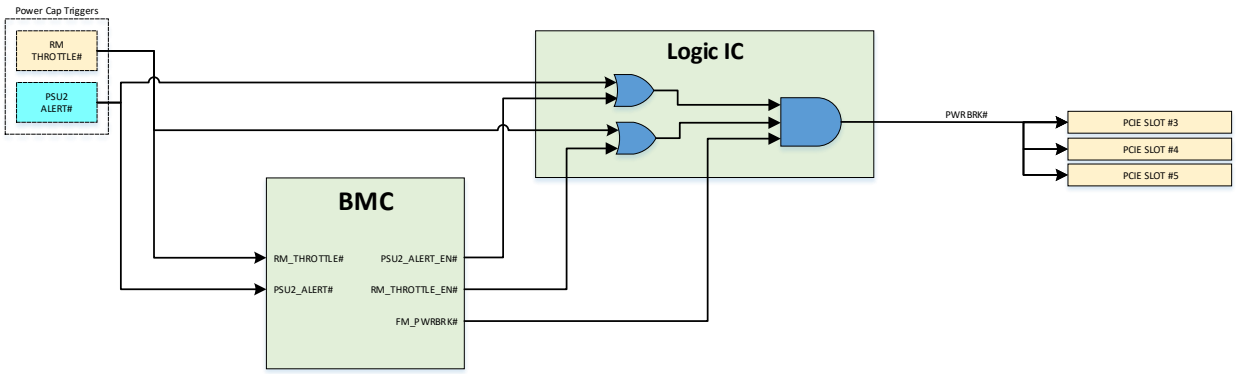


Figure 11. PWRBRK#

7.6 Overcurrent Protection

The hot swap controller (HSC) is responsible for detecting a current level that indicates a catastrophic failure of the server. In this event, the HSC should disable 12V to the motherboard typically by disabling the HSC's input FETS.

7.7 Datasafe Storage

The design supports datasafe storage solutions. A datasafe storage device is a device that contains nonvolatile storage backup for volatile memory. Backup power for these devices can be supplied by a device local energy source such as a lithium battery (RAID), Pfail circuit (M.2), or Supercap (NVDIMM), or it can be supplied by a PSU battery backup. Supported datasafe devices include:

- **RAID Controller**
  Uses device local battery solution or PSU battery. Save initiated by PERST#.
- **M.2**
  Uses device local Pfail circuit or PSU battery. Save initiated by PERST#.
- **NVDIMM**
  Uses Supercap solution or PSU battery. Save initiated by SAVE#.

7.7.1 M.2

The design supports up to 9 M.2 modules. Four modules are supported through Slots 1-2 and five are supported through M.2 connectors on the motherboard. If the M.2 contains a local PFAIL solution, the solution shall reside within the volume space designated for the M.2 module. It is intended that the PFAIL solution would be used in servers that are not supported by the PSU battery backup solution. If the server contains a PSU battery solution, the design properly initiate a SAVE event and meet the power state requirements for backup.

8 Clock Generator

The motherboard supports multiple clock generators. The clock circuitry supports I2C and is made available to the BMC.

Reference clock for motherboard interface are shown below:

- Core: 33.33 MHz
- SOC: 33.33 MHz
- DDR: 33.33 MHz
- CCPI2™: 125 MHz
- PCIe: 100 MHz
- SATA: 100 MHz
- USB: 100 MHz

Figure 12 provides an overview of the motherboard clock circuitry.

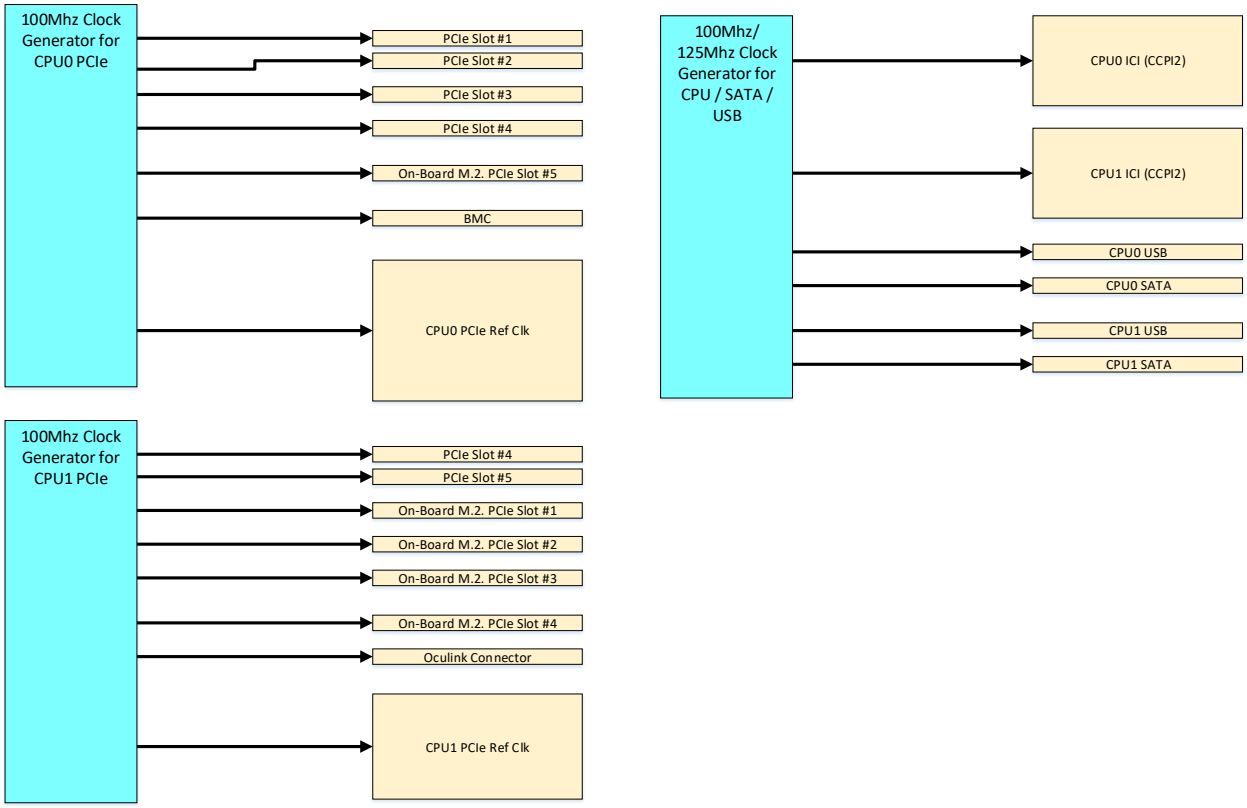


Figure 12. Clock Generator

9 Motherboard Layout

Figure 13 shows an example layout and the approximate location of critical components and connectors. The bottom of the diagram represents the location of the cold aisle.

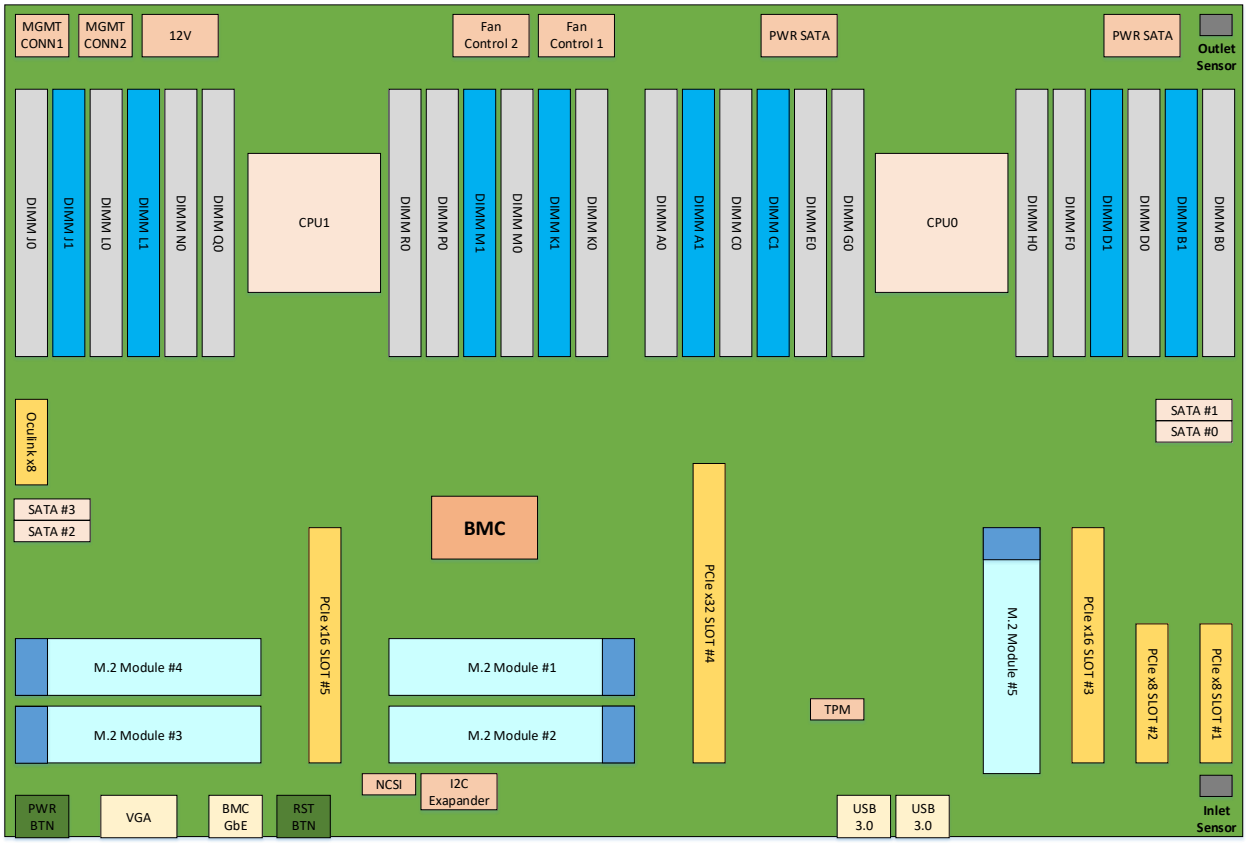


Figure 13. Motherboard Layout

10 Serviceability

10.1 Debug Features

The motherboard supports the following debug features:

- I2C Debug headers on all I2C ports. Headers are compatible with standard I2C Protocol Analyzers such as Beagle or Aardvark.
- Debug connector on all UARTS. 4-pin 2.54mm headers.
- POST LEDs.
- BIOS Debug Support Including:
    - Two socketed BIOS Flash (socket to be removed for production)

  - BIOS recovery jumper connected to GPIO
- Two USB 3.0 debug ports connected to CPU0 USB Port 2 and CPU1 USB Port 1 available at the front of motherboard (cold aisle)

The motherboard provides two USB 3.0 Type A connectors at the front of the server to enable cold aisle servicing.

10.2 LED Visibility

Motherboard LEDs determined to be important for communicating status to service personnel are visible at the front (cold aisle) of the motherboard.

- UID LED
- Power Status LED
- Attention LED

11 Motherboard Interfaces

This section describes the connector interfaces to the motherboard.

11.1 PCIe x8 Connectors

All standard PCIe x8 connectors (slot #1 and #2) on the motherboard supports the dual M.2 riser card. The interface is designed to support a standard PCIe x8 card as well as the M.2 Interposer Module. The M.2 Interposer Module is a custom edge card PCA that supports two M.2 SSD Modules (NGFF form factor cards) in the connectorized SSD Socket 3 format per the PCI Express M.2 Specification. To support two M.2 modules, the PCIe connector interface is altered to support two x4 PCIe Gen3 interfaces as well as the SSD specific signals per the PCIE M.2 specification. Table 11 describes the connector pinout. All signals satisfy the electrical requirements of the PCIe Card Electromechanical Specification. The following is a list of pin assignment deviations from that specification needed to support two M.2 modules. These signals are highlighted in red.

- SUSCLK is assigned to pin A6 replacing JTAG TDI pin. Support for SUSCLK is optional.
- LINKWIDTH is assigned to pin B17 replacing PRSNT#2. Enables auto-detection of 2x4 M.2 Interposer or 1x8 standard PCIe card. The design is not required to support PCIe x1 cards.
- REFCLK2+/- is assigned to pins A32/A33 replacing two Reserved pins.
- SMBCLK2 and SMBDAT2 are assigned to pins A7/A8 replacing TDO and TMS pins.

Table 11. PCIe x8 connector pinout

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	+12v	+12 volt power	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK1	SMBus clock	JTAG2	TCK
6	SMDAT1	SMBus data	SUSCLK	Suspend Clk
7	GND	Ground	SMCLK2	SMBus clock
8	+3.3v	+3.3 volt power	SMDAT2	SMBus data
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PGOOD	Powergood
Mechanical Key				
12	CLKREQ#	Request Running Clock	GND	Ground
13	GND	Ground	REFCLK1+	Reference Clock
14	PETP(0)	Transmitter Lane 0,	REFCLK1-	Differential pair
15	PETN(0)	Differential pair	GND	Ground
16	GND	Ground	PERP(0)	Receiver Lane 0,
17	LINKWIDTH	0= 2 x4 1= 1 x8	PERN(0)	Differential pair
18	GND	Ground	GND	Ground
19	PETP(1)	Transmitter Lane 1,	RSVD	Reserved
20	PETN(1)	Differential pair	GND	Ground
21	GND	Ground	PERP(1)	Receiver Lane 1,
22	GND	Ground	PERN(1)	Differential pair
23	PETP(2)	Transmitter Lane 2,	GND	Ground
24	PETN(2)	Differential pair	GND	Ground
25	GND	Ground	PERP(2)	Receiver Lane 2,
26	GND	Ground	PERN(2)	Differential pair
27	PETP(3)	Transmitter Lane 3,	GND	Ground
28	PETN(3)	Differential pair	GND	Ground
29	GND	Ground	PERP(3)	Receiver Lane 3,
30	RSVD	Reserved	PERN(3)	Differential pair
31	PRSNT#2	Presence Detect	GND	Ground

32	GND	Ground	REFCLK2+	Reference Clock Differential pair
33	PETP(4)	Transmitter Lane 4, Differential pair	REFCLK2-	
34	PETN(4)		GND	Ground
35	GND	Ground	PERP(4)	Receiver Lane 4, Differential pair
36	GND	Ground	PERN(4)	
37	PETP(5)	Transmitter Lane 5, Differential pair	GND	Ground
38	PETN(5)		GND	Ground
39	GND	Ground	PERP(5)	Receiver Lane 5, Differential pair
40	GND	Ground	PERN(5)	
41	PETP(6)	Transmitter Lane 6, Differential pair	GND	Ground
42	PETN(6)		GND	Ground
43	GND	Ground	PERP(6)	Receiver Lane 6, Differential pair
44	GND	Ground	PERN(6)	
45	PETP(7)	Transmitter Lane 7, Differential pair	GND	Ground
46	PETN(7)		GND	Ground
47	GND	Ground	PERP(7)	Receiver Lane 7, Differential pair
48	PRSNT#2	Presence detect	PERN(7)	
49	GND	Ground	GND	Ground

11.2 PCIe x16 Connectors

The PCIe x16 connector interface is designed to support a standard PCIe x16 full-height card. The pinout for supporting PCIe x16 described in Table 12. This interface also supports the PWRBRK# power reduction feature. Note that this signal is declared on pins B12 and B30. This enables support for the feature on existing platforms (B12) and meets the latest PCI SIG definition (B30). For further information, refer to the PCI Express® Card Electromechanical Specification.

Table 12. PCIe x16 connector pinout

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	+12v	+12 volt power	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO

8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PWRGD	Power Good
Mechanical Key				
12	PWRBRK#	Power Reduction	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock
14	PETP(0)	Transmitter Lane 0,	REFCLK-	Differential pair
15	PETN(0)	Differential pair	GND	Ground
16	GND	Ground	PERP(0)	Receiver Lane 0,
17	PRSNT#2	Presence detect	PERN(0)	Differential pair
18	GND	Ground	GND	Ground
19	PETP(1)	Transmitter Lane 1,	RSVD	Reserved
20	PETN(1)	Differential pair	GND	Ground
21	GND	Ground	PERP(1)	Receiver Lane 1,
22	GND	Ground	PERN(1)	Differential pair
23	PETP(2)	Transmitter Lane 2,	GND	Ground
24	PETN(2)	Differential pair	GND	Ground
25	GND	Ground	PERP(2)	Receiver Lane 2,
26	GND	Ground	PERN(2)	Differential pair
27	PETP(3)	Transmitter Lane 3,	GND	Ground
28	PETN(3)	Differential pair	GND	Ground
29	GND	Ground	PERP(3)	Receiver Lane 3,
30	PWRBRK#	Power Reduction	PERN(3)	Differential pair
31	PRSNT#2	Hot plug detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETP(4)	Transmitter Lane 4,	RSVD	Reserved
34	PETN(4)	Differential pair	GND	Ground
35	GND	Ground	PERP(4)	Receiver Lane 4,
36	GND	Ground	PERN(4)	Differential pair
37	PETP(5)	Transmitter Lane 5,	GND	Ground
38	PETN(5)	Differential pair	GND	Ground
39	GND	Ground	PERP(5)	Receiver Lane 5,
40	GND	Ground	PERN(5)	Differential pair
41	PETP(6)	Transmitter Lane 6,	GND	Ground
42	PETN(6)	Differential pair	GND	Ground

43	GND	Ground	PERP(6)	Receiver Lane 6,
44	GND	Ground	PERN(6)	Differential pair
45	PETP(7)	Transmitter Lane 7,	GND	Ground
46	PETN(7)	Differential pair	GND	Ground
47	GND	Ground	PERP(7)	Receiver Lane 7,
48	PRSNT#2	Hot plug detect	PERN(7)	Differential pair
49	GND	Ground	GND	Ground
50	PETP(8)	Transmitter Lane 8,	RSVD	Reserved
51	PETN(8)	Differential pair	GND	Ground
52	GND	Ground	PERP(8)	Receiver Lane 8,
53	GND	Ground	PERN(8)	Differential pair
54	PETP(9)	Transmitter Lane 9,	GND	Ground
55	PETN(9)	Differential pair	GND	Ground
56	GND	Ground	PERP(9)	Receiver Lane 9,
57	GND	Ground	PERN(9)	Differential pair
58	PETP(10)	Transmitter Lane 10,	GND	Ground
59	PETN(10)	Differential pair	GND	Ground
60	GND	Ground	PERP(10)	Receiver Lane 10,
61	GND	Ground	PERN(10)	Differential pair
62	PETP(11)	Transmitter Lane 11,	GND	Ground
63	PETN(11)	Differential pair	GND	Ground
64	GND	Ground	PERP(11)	Receiver Lane 11,
65	GND	Ground	PERN(11)	Differential pair
66	PETP(12)	Transmitter Lane 12,	GND	Ground
67	PETN(12)	Differential pair	GND	Ground
68	GND	Ground	PERP(12)	Receiver Lane 12,
69	GND	Ground	PERN(12)	Differential pair
70	PETP(13)	Transmitter Lane 13,	GND	Ground
71	PETN(13)	Differential pair	GND	Ground
72	GND	Ground	PERP(13)	Receiver Lane 13,
73	GND	Ground	PERN(13)	Differential pair
74	PETP(14)	Transmitter Lane 14,	GND	Ground
75	PETN(14)	Differential pair	GND	Ground
76	GND	Ground	PERP(14)	Receiver Lane 14,
77	GND	Ground	PERN(14)	Differential pair
78	PETP(15)	Transmitter Lane 15,	GND	Ground

79	PETN(15)	Differential pair	GND	Ground
80	GND	Ground	PERP(15)	Receiver Lane 15,
81	PRSNT#2	Hot plug present detect	PERN(15)	Differential pair
82	RSVD#2	Hot Plug Detect	GND	Ground

11.3 PCIe x32 Connector

The PCIe x32 connector interface is designed to support a PCIe x32 full-height card. Use of PCIe x32 is optional for the front I/O slot, and is primarily intended as a future growth targeting slot #4. The interface is comprised of two Samtec HSEC8 connectors: 200 pin MPN DFHSK0FS015 and 60 pin MPN DFHS60FS042. The pinouts for the 200 pin and 60 pin connectors are shown in Table 13 and Table 14 respectively. Key features for this interface includes:

- Supports two PCIe x16 interfaces
- Supports auto-bifurcation (Config ID)
- Supports up to 6 PCIe Clocks
- Supports two SMBus interfaces
- Supports JTAG Interface
- Supports USB 2.0 Interface

Table 13. PCIe x32 Connector Pinout - 200 Pin

Pin	Side A Connector		Side B Connector		Pin
#	Name	Description	Name	Description	#
1	P12V	+12 volt power	P12V	+12 volt power	2
3	P12V	+12 volt power	P12V	+12 volt power	4
5	P12V	+12 volt power	P12V	+12 volt power	6
7	P12V	+12 volt power	P12V	+12 volt power	8
9	P12V	+12 volt power	P12V	+12 volt power	10
11	P12V	+12 volt power	P12V	+12 volt power	12
13	GND	Ground	GND	Ground	14
15	I2C1_SMBDAT	SMBus1 to BMC	BMC_ALERT#	SMBus Alert to BMC	16
17	I2C1_SMCLK	SMBus1 to BMC	SLT_CFG1	Slot Configuration Bit1	18
19	SLT_CFG0	Slot Configuration Bit0	PWRBREAK#	Power Break	20
21	P3V3	+3.3 volt power	P3V3	+3.3 volt power	22
23	P3V3	+3.3 volt power	P3V3	+3.3 volt power	24
25	P3V3_STBY	+3.3 volt stby power	GND	Ground	26
27	BMC_ALERT#	SMBus Alert to BMC	WAKE#	Wake	28
29	PERST#	PCIe Reset	I2C2_SMDAT	SMBus2 to BMC	30
31	GND	Ground	I2C2_SMCLK	SMBus2 to BMC	32
33	CLK_100M_DP<0>	Reference Clock	GND	Ground	34
35	CLK_100M_DN<0>	Differential pair	CLK_100M_DP<1>	Reference Clock	36

37	GND	Ground	CLK_100M_DN<1>	Differential pair	38
39	CLK_100M_DP<2>	Reference Clock	GND	Ground	40
41	CLK_100M_DN<2>	Differential pair	CLK_100M_DP<3>	Reference Clock	42
43	GND	Ground	CLK_100M_DN<3>	Differential pair	44
45	CLK_100M_DP<4>	Reference Clock	GND	Ground	46
47	CLK_100M_DN<4>	Differential pair	CLK_100M_DP<5>	Reference Clock	48
49	GND	Ground	CLK_100M_DN<5>	Differential pair	50
51	P3E_P0_TXP<15>	Transmitter Lane 15,	GND	Ground	52
53	P3E_P0_TXN<15>	Differential pair	P3E_P0_RXP<15>	Receiver Lane 15,	54
55	GND	Ground	P3E_P0_RXN<15>	Differential pair	56
57	P3E_P0_TXP<14>	Transmitter Lane 14,	GND	Ground	58
59	P3E_P0_TXN<14>	Differential pair	P3E_P0_RXN<14>	Receiver Lane 14,	60
61	GND	Ground	P3E_P0_RXP<14>	Differential pair	62
63	RSVD1	Reserved	GND	Ground	64
65	GND	Ground	RSVD2	Reserved	66
67	P3E_P0_TXN<13>	Transmitter Lane 13,	GND	Ground	68
69	P3E_P0_TXP<13>	Differential pair	P3E_P0_RXP<13>	Receiver Lane 13,	70
71	GND	Ground	P3E_P0_RXN<13>	Differential pair	72
73	P3E_P0_TXN<12>	Transmitter Lane 12,	GND	Ground	74
75	P3E_P0_TXP<12>	Differential pair	P3E_P0_RXP<12>	Receiver Lane 12,	76
77	GND	Ground	P3E_P0_RXN<12>	Differential pair	78
79	P3E_P0_TXN<11>	Transmitter Lane 11,	GND	Ground	80
81	P3E_P0_TXP<11>	Differential pair	P3E_P0_RXP<11>	Receiver Lane 11,	82
83	GND	Ground	P3E_P0_RXN<11>	Differential pair	84
85	P3E_P0_TXN<10>	Transmitter Lane 10,	GND	Ground	86
87	P3E_P0_TXP<10>	Differential pair	P3E_P0_RXP<10>	Receiver Lane 10,	88
89	GND	Ground	P3E_P0_RXN<10>	Differential pair	90
91	P3E_P0_TXP<9>	Transmitter Lane 9,	GND	Ground	92
93	P3E_P0_TXN<9>	Differential pair	P3E_P0_RXP<9>	Receiver Lane 9,	94
95	GND	Ground	P3E_P0_RXN<9>	Differential pair	96
97	P3E_P0_TXP<8>	Transmitter Lane 8,	GND	Ground	98
99	P3E_P0_TXN<8>	Differential pair	P3E_P0_RXP<8>	Receiver Lane 8,	100
101	GND	Ground	P3E_P0_RXN<8>	Differential pair	102
103	P3E_P0_TXP<7>	Transmitter Lane 7,	GND	Ground	104
105	P3E_P0_TXN<7>	Differential pair	P3E_P0_RXP<7>	Receiver Lane 7,	106
107	GND	Ground	P3E_P0_RXN<7>	Differential pair	108
109	P3E_P0_TXP<6>	Transmitter Lane 6,	GND	Ground	110
111	P3E_P0_TXN<6>	Differential pair	P3E_P0_RXP<6>	Receiver Lane 6,	112
113	GND	Ground	P3E_P0_RXN<6>	Differential pair	114
115	P3E_P0_TXP<5>	Transmitter Lane 5,	GND	Ground	116
117	P3E_P0_TXN<5>	Differential pair	P3E_P0_RXP<5>	Receiver Lane 5,	118
119	GND	Ground	P3E_P0_RXN<5>	Differential pair	120
121	P3E_P0_TXP<4>	Transmitter Lane 4,	GND	Ground	122
123	P3E_P0_TXN<4>	Differential pair	P3E_P0_RXP<4>	Receiver Lane 4,	124
125	GND	Ground	P3E_P0_RXN<4>	Differential pair	126

127	P3E_P0_TXP<3>	Transmitter Lane 3,	GND	Ground	128
129	P3E_P0_TXN<3>	Differential pair	P3E_P0_RXP<3>	Receiver Lane 3,	130
131	GND	Ground	P3E_P0_RXN<3>	Differential pair	132
133	P3E_P0_TXP<2>	Transmitter Lane 2,	GND	Ground	134
135	P3E_P0_TXN<2>	Differential pair	P3E_P0_RXP<2>	Receiver Lane 2,	136
137	GND	Ground	P3E_P0_RXN<2>	Differential pair	138
139	P3E_P0_TXP<1>	Transmitter Lane 1,	GND	Ground	140
141	P3E_P0_TXN<1>	Differential pair	P3E_P0_RXP<1>	Receiver Lane 1,	142
143	GND	Ground	P3E_P0_RXN<1>	Differential pair	144
145	P3E_P0_TXP<0>	Transmitter Lane 0,	GND	Ground	146
147	P3E_P0_TXN<0>	Differential pair	P3E_P0_RXP<0>	Receiver Lane 0,	148
149	GND	Ground	P3E_P0_RXN<0>	Differential pair	150
151	P3E_P1_TXP<15>	Transmitter Lane 15,	GND	Ground	152
153	P3E_P1_TXP<15>	Differential pair	P3E_P1_RXP<15>	Receiver Lane 15,	154
155	GND	Ground	P3E_P1_RXP<15>	Differential pair	156
157	P3E_P1_TXP<14>	Transmitter Lane 14,	GND	Ground	158
159	P3E_P1_TXN<14>	Differential pair	P3E_P1_RXP<14>	Receiver Lane 14,	160
161	GND	Ground	P3E_P1_RXN<14>	Differential pair	162
163	P3E_P1_TXP<13>	Transmitter Lane 13,	GND	Ground	164
165	P3E_P1_TXN<13>	Differential pair	P3E_P1_RXP<13>	Receiver Lane 13,	166
167	GND	Ground	P3E_P1_RXN<13>	Differential pair	168
169	P3E_P1_TXP<12>	Transmitter Lane 12,	GND	Ground	170
171	P3E_P1_TXN<12>	Differential pair	P3E_P1_RXP<12>	Receiver Lane 12,	172
173	GND	Ground	P3E_P1_RXN<12>	Differential pair	174
175	P3E_P1_TXP<11>	Transmitter Lane 11,	GND	Ground	176
177	P3E_P1_TXN<11>	Differential pair	P3E_P1_RXP<11>	Receiver Lane 11,	178
179	GND	Ground	P3E_P1_RXN<11>	Differential pair	180
181	P3E_P1_TXP<10>	Transmitter Lane 10,	GND	Ground	182
183	P3E_P1_TXN<10>	Differential pair	P3E_P1_RXP<10>	Receiver Lane 10,	184
185	GND	Ground	P3E_P1_RXN<10>	Differential pair	186
187	P3E_P1_TXP<9>	Transmitter Lane 9,	GND	Ground	188
189	P3E_P1_TXN<9>	Differential pair	P3E_P1_RXP<9>	Receiver Lane 9,	190
191	GND	Ground	P3E_P1_RXN<9>	Differential pair	192
193	P3E_P1_TXP<8>	Transmitter Lane 8,	GND	Ground	194
195	P3E_P1_TXN<8>	Differential pair	P3E_P1_RXP<8>	Receiver Lane 8,	196
197	GND	Ground	P3E_P1_RXN<8>	Differential pair	198
199	PRESENT#	Present signal	GND	Ground	200

Table 14. PCIe x32 Connector Pinout - 60 Pin

Pin	Side A Golden Finger		Side B Golden Finger		Pin
#	Name	Description	Name	Description	#
1	GND	Ground	P5V	USB Power	2
3	P3E_P1_TXP<7>	Transmitter Lane 7,	GND	Ground	4
5	P3E_P1_TXN<7>	Differential pair	P3E_P1_RXP<7>	Receiver Lane 7,	6
7	GND	Ground	P3E_P1_RXN<7>	Differential pair	8

9	P3E_P1_TXP<6>	Transmitter Lane 6,	GND	Ground	10
11	P3E_P1_TXN<6>	Differential pair	P3E_P1_RXP<6>	Receiver Lane 6,	12
13	GND	Ground	P3E_P1_RXN<6>	Differential pair	14
15	P3E_P1_TXP<5>	Transmitter Lane 5,	GND	Ground	16
17	P3E_P1_TXN<5>	Differential pair	P3E_P1_RXP<5>	Receiver Lane 5,	18
19	GND	Ground	P3E_P1_RXN<5>	Differential pair	20
21	P3E_P1_TXP<4>	Transmitter Lane 4,	GND	Ground	22
23	P3E_P1_TXN<4>	Differential pair	P3E_P1_RXP<4>	Receiver Lane 4,	24
25	GND	Ground	P3E_P1_RXN<4>	Differential pair	26
27	P3E_P1_TXP<3>	Transmitter Lane 3,	GND	Ground	28
29	P3E_P1_TXN<3>	Differential pair	P3E_P1_RXP<3>	Receiver Lane 3,	30
31	GND	Ground	P3E_P1_RXN<3>	Differential pair	32
33	P3E_P1_TXP<2>	Transmitter Lane 2,	GND	Ground	34
35	P3E_P1_TXN<2>	Differential pair	P3E_P1_RXP<2>	Receiver Lane 2,	36
37	GND	Ground	P3E_P1_RXN<2>	Differential pair	38
39	P3E_P1_TXP<1>	Transmitter Lane 1,	GND	Ground	40
41	P3E_P1_TXN<1>	Differential pair	P3E_P1_RXP<1>	Receiver Lane 1,	42
43	GND	Ground	P3E_P1_RXN<1>	Differential pair	44
45	P3E_P1_TXP<0>	Transmitter Lane 0,	GND	Ground	46
47	P3E_P1_TXN<0>	Differential pair	P3E_P1_RXP<0>	Receiver Lane 0,	48
49	GND	Ground	P3E_P1_RXN<0>	Differential pair	50
51	JTAG_TDI	JTAG TDI	GND	Ground	52
53	JTAG_TDO	JTAG TDO	JTAG_TMS	JTAG TMS	54
55	GND	Ground	JTAG_TCK	JTAG TCK	56
57	USB2_DP	USB 2.0	GND	Ground	58
59	USB2_DN	USB 2.0	JTAG_TRST	JTAG Reset	60

11.4 M.2 Connectors

The board support five on-board M.2. PCIe connectors for expansion flash memory. The M.2 connector pinout is shown in Table 15. For more information about the M.2 interface, refer to the PCI Express M.2 Specification.

Table 15. M.2 connector pinout

M.2 Module Standard Pinout					
Pin	**Signal**	**Description**	**Pin**	**Signal**	**Description**
74	3.3V	3.3V Power	75	GND	Ground
72	3.3V	3.3V Power	73	GND	Ground
70	3.3V	3.3V Power	71	GND	Ground
68	SUSCLK(32KHz)	Reduce Power Clock	69	NC	Reserved
66	KEY	Module Key	67	GND	Ground
64	KEY	Module Key	65	KEY	Module Key

62	KEY	Module Key	63	KEY	Module Key
60	KEY	Module Key	61	KEY	Module Key
58	NC	Reserved	59	KEY	Module Key
56	NC	Reserved	57	GND	Ground
54	PEWAKE#	PCIe PME Wake (Open Drain)	55	REFLKCP	PCIe Reference Clock
52	CLKREQ#	Reference Clock Request	53	REFLKCN	PCIe Reference Clock
50	PERST#	PCIe Reset	51	GND	Ground
48	NC	Reserved	49	PETP0	PCIe Transmit Lane 0
46	NC	Reserved	47	PETN0	PCIe Transmit Lane 0
44	ALERT#	SMBus ALERT	45	GND	Ground
42	SMB_DATA	SMBus Data	43	PERP0	PCIe Receive Lane 0
40	SMB_CLK	SMBus Clock	41	PERN0	PCIe Receive Lane 0
38	DEVSLP	Device Sleep	39	GND	Ground
36	NC	Reserved	37	PETP1	PCIe Transmit Lane 1
34	NC	Reserved	35	PETN1	PCIe Transmit Lane 1
32	NC	Reserved	33	GND	Ground
30	NC	Reserved	31	PERP1	PCIe Receive Lane 1
28	NC	Reserved	29	PERN1	PCIe Receive Lane 1
26	NC	Reserved	27	GND	Ground
24	NC	Reserved	25	PETP2	PCIe Transmit Lane 2
22	NC	Reserved	23	PETN2	PCIe Transmit Lane 2
20	NC	Reserved	21	GND	Ground
18	3.3V	3.3V Power	19	PERP2	PCIe Receive Lane 2
16	3.3V	3.3V Power	17	PERN2	PCIe Receive Lane 2
14	3.3V	3.3V Power	15	GND	Ground
12	3.3V	3.3V Power	13	PETP3	PCIe Transmit Lane 3
10	DAS/DSS#	Drive Active Signal (Open Drain)	11	PETN3	PCIe Transmit Lane 3
8	NC	Reserved	9	GND	Ground
6	NC	Reserved	7	PERP3	PCIe Receive Lane 3
4	3.3V	3.3V Power	5	PERN3	PCIe Receive Lane 3
2	3.3V	3.3V Power	3	GND	Ground
			1	GND	Ground

11.5 SATA Cable Ports

The motherboard includes support for four x1 SATA standard 7-pin connectors.

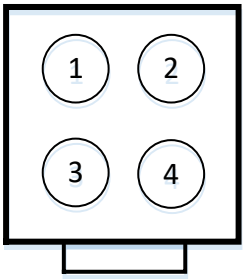
11.6 SATA Power Connector

The motherboard optionally includes up to two 4-pin Mini-Fit® Jr™ 5566 series power connectors, Molex P/N 39-28-1043 or equivalent for supplying power to up to 4 SATA devices. The motherboard optionally supports additional connectors to provide power to up to an additional 8 SATA devices (12 total). Each connector pin has a maximum 13A current capacity. Table 16 describes the connector pinout. Figure 14 shows a top view of the physical pin numbering.

Table 16. SATA Power Connector

Pin	Signal name	Capacity (in A)
Pin 1 & 2	GND	13A (Black)
Pin 3	12V	9A (Yellow)
Pin 4	5V	9A (Red)

Figure 14. SATA Power Connector Pin Numbering



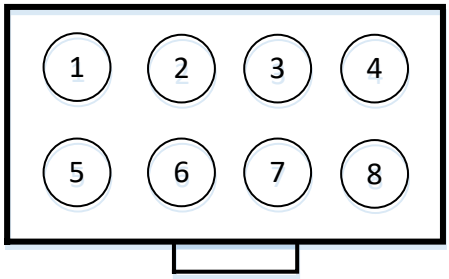
11.7 SATA Power Expansion Connector

The motherboard optionally includes up to two 8-pin Mini-Fit® Jr™ 5566 series power connectors, Molex P/N 39-28-1083 or equivalent for supplying power to up to 8 additional SATA devices. Each connector has a maximum 13A current capacity. Table 17 describes the connector pinout. Figure 15 shows a top view of the physical pin numbering.

Table 17. SATA Power Expansion Connector Pinout

Pin	Signal name	Capacity (in A)
Pin 1-4	GND	13A (Black)
Pin 5,6	12V	9A (Yellow)
Pin 7,8	5V	9A (Red)

Figure 15. SATA Power Expansion Connector Pin Numbering



11.8 12V Power Connector

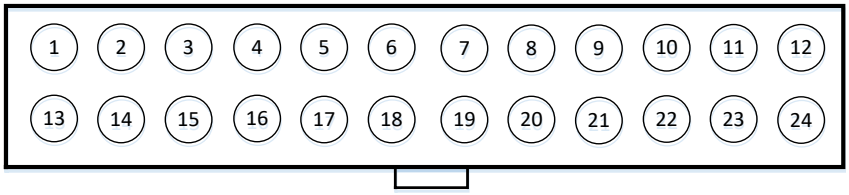
The motherboard includes a 24-pin Mini-Fit® Jr™ 5569 series power connector, Molex P/N 3930-0240 or equivalent to support 12V cabling from the motherboard to the PSU. The connector supports 800W. Table 18 describes the connector pinout. Figure 16 shows a top view of the physical pin numbering. For further information, refer to the Project Olympus PSU Specification.

Table 18. 12V Power Connector

Management Connector				
Pin	**Signal**	**I/O**	**Voltage**	**Description**
1	GND	I	0V	GND from PSU
2	GND	I	0V	GND from PSU
3	GND	I	0V	GND from PSU
4	GND	I	0V	GND from PSU
5	GND	I	0V	GND from PSU
6	GND	I	0V	GND from PSU
7	P12V_PSU	I	12V	12V Power from PSU
8	P12V_PSU	I	12V	12V Power from PSU
9	P12V_PSU	I	12V	12V Power from PSU
10	P12V_PSU	I	12V	12V Power from PSU
11	P12V_PSU	I	12V	12V Power from PSU
12	P12V_PSU	I	12V	12V Power from PSU
13	GND	I	0V	GND from PSU

14	GND	I	0V	GND from PSU
15	GND	I	0V	GND from PSU
16	GND	I	0V	GND from PSU
17	GND	I	0V	GND from PSU
18	GND	I	0V	GND from PSU
19	P12V_PSU	I	12V	12V Power from PSU
20	P12V_PSU	I	12V	12V Power from PSU
21	P12V_PSU	I	12V	12V Power from PSU
22	P12V_PSU	I	12V	12V Power from PSU
23	P12V_PSU	I	12V	12V Power from PSU
24	P12V_PSU	I	12V	12V Power from PSU

Figure 16. Mini-Fit Connector Pin Numbering



11.9 Management Connector

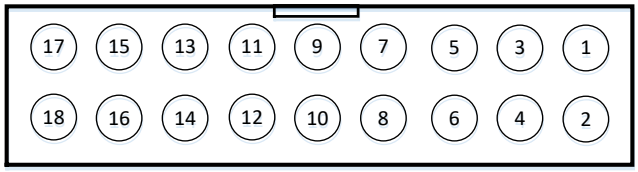
The motherboard includes a connector for interfacing management signals from the motherboard to the Rack Manager through a cable to a rear panel connector on the server assembly. The connector for supporting the cable is an 18 pin Molex Picoblade™ series connector, Molex part number 87832-5823 or equivalent. Table 19 describes the connector pinout. Figure 17 shows a top view of the physical pin numbering.

Table 19. Management Connector

1U Management Connector				
Pin	**Signal**	**I/O**	**Voltage**	**Description**
1	BLADE_EN#	I	3.3V	Enable signal from Rack Manager to PS_ON and BMC
2	LR_SELECT	I	RS232	Left/Right Node Select
3	SLOT_ID0	I	3.3V	SLOT ID from PMDU to the Server
4	SLOT_ID1	I	3.3V	SLOT ID from PMDU to Server
5	SERVER_THROTTLE#	I	3.3V	Server Throttle control from Rack Manager
6	SERVER_PRESENT#	O	3.3V	Indicates Server presence to the Rack Manager
7	I2C _SCL	O	3.3V	I2C Clock to PSU (PMBus)
8	I2C_SDA	I/O	3.3V	I2C Data to PSU (PMBus)
9	I2C_GND	I	0V	GND reference for I^2C bus
10	PS_ON#	O	3.3V	Turns on PSU. Connector to BLADE_EN#

11	PSU_ALERT#	I	3.3V	I²C Alert from the PSU
12	PSU_LED0	I	3.3V	PSU LED 0(Green)
13	PSU_LED1	I	3.3V	PSU LED 1(Yellow)
14	SLOT_ID2	I	3.3V	SLOT ID from PMDU to Server
15	SLOT_ID3	I	3.3V	SLOT ID from PMDU to Server
16	SLOT_ID4	I	3.3V	SLOT ID from PMDU to Server
17	SLOT_ID5	I	3.3V	SLOT ID from PMDU to Server
18	P3V_BAT_SOURCE	I	3V	Optional 3V RTC Source (if no onboard 3V battery is present)

Figure 17. 1U Management Connector Pin Numbering



11.10 Management Expansion Connector

The motherboard includes a connector for enabling management and power control of expansion hardware, such as a 2U server. The connector for supporting the cable shall be an 18 pin Molex Picoblade™ series connector, Molex part number 87832-5823 or equivalent. This is the same connector as used for the 1U Server Management Connector. Table 20 describes the connector pinout.

Table 20. Expansion Server Management Connector

Server Management Connector				
Pin	**Signal**	**I/O**	**Voltage**	**Description**
1	NC	NA	NA	No Connect
2	I2C1_SDA	O	3.3V	I2C Data (expansion)
3	I2C1_SDL	I/O	3.3V	I2C Clock (expansion)
4	GND	I	0V	GND Reference
5	NC	NA	NA	No Connect
6	PRESENT#	I	3.3V	Indicate expansion server presence to the rack manager
7	I2C2_SCL	O	3.3V	I2C Clock to expansion PSU (PMBus)
8	I2C2_SDA	I/O	3.3V	I2C Data to expansion PSU (PMBus)
9	I2C_GND	I	0V	GND reference for I2Cbus
10	PS_ON#	O	3.3V	Turns on expansion PSU. Driven by BMC or CPLD
11	PSU_ALERT#	I	3.3V	I2C Alert from the expansion PSU
12	PSU_LED0	I	3.3V	Expansion PSU LED 0(Green)
13	PSU_LED1	I	3.3V	Expansion PSU LED 1(Yellow)
14	NC	NA	NA	No Connect
15	PSU1_PWROK	I	3.3V	PSU Power OK signal to BMC

16	PSU2_PWROK	I	3.3V	PSU2 Power OK Signal to BMC
17	PSU1_PRESENT	I	3.3V	PSU Present Signal
18	PSU2_PRESENT	I	3.3V	PSU2 Present Signal

11.11 OCuLink x8 Connector

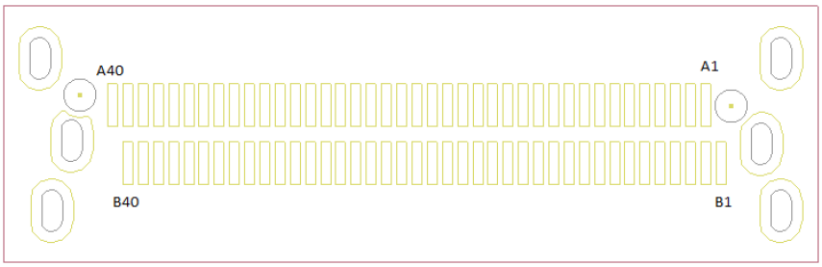
The motherboard includes a connector for cabling PCIe x8 from the motherboard to the FPGA Card. The connector for supporting the cable is an 80-pin vertical Molex Nanopitch™ series connector or equivalent (Molex part number 173162-0338). Table 21 describes the connector pinout. Figure 18 shows a top view of the physical pin numbering.

Table 21. Oculink x8 Connector

Row A			Row B		
Pin	**Signal Name**	**Description**	**Pin**	**Signal Name**	**Description**
A1	GND	Ground	B1	GND	Ground
A2	PERp0	PCIe Receive Data to CPU	B2	PETp0	PCIe Transmit Data from CPU
A3	PERn0	PCIe Receive Data to CPU	B3	PETn0	PCIe Transmit Data from CPU
A4	GND	Ground	B4	GND	Ground
A5	PERp1	PCIe Receive Data to CPU	B5	PETp1	PCIe Transmit Data from CPU
A6	PERn1	PCIe Receive Data to CPU	B6	PETn1	PCIe Transmit Data from CPU
A7	GND	Ground	B7	GND	Ground
A8	NC	No Connect	B8	NC	No Connect
A9	NC	No Connect	B9	NC	No Connect
A10	GND	Ground	B10	GND	Ground
A11	NC	No Connect	B11	NC	No Connect
A12	NC	No Connect	B12	CPRSNT#	Cable Present
A13	GND	Ground	B13	GND	Ground
A14	PERp2	PCIe Receive Data to CPU	B14	PETp2	PCIe Transmit Data from CPU
A15	PERn2	PCIe Receive Data to CPU	B15	PETn2	PCIe Transmit Data from CPU
A16	GND	Ground	B16	GND	Ground
A17	PERp3	PCIe Receive Data to CPU	B17	PETp3	PCIe Transmit Data from CPU
A18	PERn3	PCIe Receive Data to CPU	B18	PETn3	PCIe Transmit Data from CPU
A19	GND	Ground	B19	GND	Ground
A20	RSVD	Reserved	B20	RSVD	Reserved
A21	RSVD	Reserved	B21	RSVD	Reserved
A22	GND	Ground	B22	GND	Ground
A23	PERp4	PCIe Receive Data to CPU	B23	PETp4	PCIe Transmit Data from CPU
A24	PERn4	PCIe Receive Data to CPU	B24	PETn4	PCIe Transmit Data from CPU
A25	GND	Ground	B25	GND	Ground
A26	PERp5	PCIe Receive Data to CPU	B26	PETp5	PCIe Transmit Data from CPU

A27	PERn5	PCIe Receive Data to CPU	B27	PETn5	PCIe Transmit Data from CPU
A28	GND	Ground	B28	GND	Ground
A29	NC	No Connect	B29	NC	No Connect
A30	NC	No Connect	B30	NC	No Connect
A31	GND	Ground	B31	GND	Ground
A32	NC	No Connect	B32	NC	No Connect
A33	NC	No Connect	B33	NC	No Connect
A34	GND	Ground	B34	GND	Ground
A35	PERp6	PCIe Receive Data to CPU	B35	PETp6	PCIe Transmit Data from CPU
A36	PERn6	PCIe Receive Data to CPU	B36	PETn6	PCIe Transmit Data from CPU
A37	GND	Ground	B37	GND	Ground
A38	PERp7	PCIe Receive Data to CPU	B38	PETp7	PCIe Transmit Data from CPU
A39	PERn7	PCIe Receive Data to CPU	B39	PETn7	PCIe Transmit Data from CPU
A40	GND	Ground	B40	GND	Ground

Figure 18. OCuLink x8 Pin Numbering



11.12 NCSI Connector

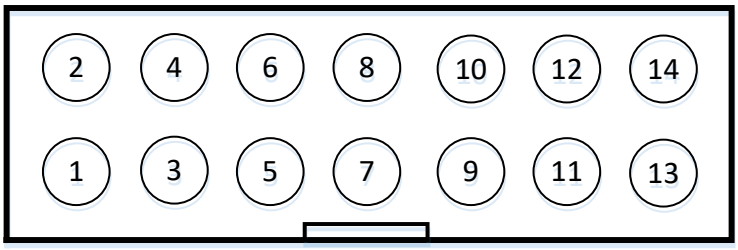
The motherboard optionally includes a connector for cabling NCSI signals from the motherboard to a NIC. The connector for supporting the cable is a 14-pin header connector, Molex part number 87832-1420 or equivalent. Table 22 describes the connector pinout. Figure 19 shows a top view of the physical pin numbering.

Table 22. NCSI Connector

NCSI Connector				
Pin	**Signal**	**I/O**	**Voltage**	**Description**
1	RXER	O	3.3V	Enable signal from Rack Manager to HSC on the motherboard
2	GND	I	0V	Ground
3	TXD1	I	3.3V	Transmit Data from BMC to NIC
4	CLK_50M	I	0V	50Mhz Clock
5	TXD0	I	3.3V	Transmit Data from BMC to NIC
6	GND	I	0V	Ground
7	TXEN	I	3.3V	Transmit Enable from BMC to NIC

8	GND	I	0V	Ground
9	CRSDV	O	3.3V	Receive carrier sense and data valid from NIC to BMC
10	GND	I	0V	Ground
11	RXD1	O	3.3V	Receive Data from NIC to BMC
12	GND	I	0V	Ground
13	RXD0	O	3.3V	Receive Data from NIC to BMC
14	GND	I	0V	Ground

Figure 19. NCSI Connector Pin Numbering



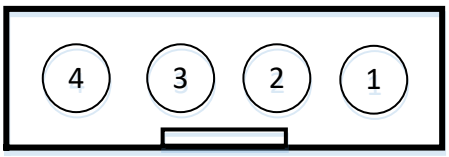
11.13 USB 2.0 Internal Header

USB2.0 is routed to PCIe Slot #4 – x32 connector. That slot allows for a 260pin riser to be used. A USB header connector is located on the riser for enabling USB 2.0 communication with the FPGA card. The connector is TE 440054-4 or equivalent. Table 23 describes the connector pinout. Figure 20 shows a top view of the physical pin numbering.

Table 23. Internal USB Connector

Pin	Signal Name	I/O	Logic	Name/Description
1	P5_USB			5V (500mA max)
2	USB_N	I/O		USB Data
3	USB_P	I/O		USB Data
4	GND			Ground

Figure 20. Internal USB Connector Pinout



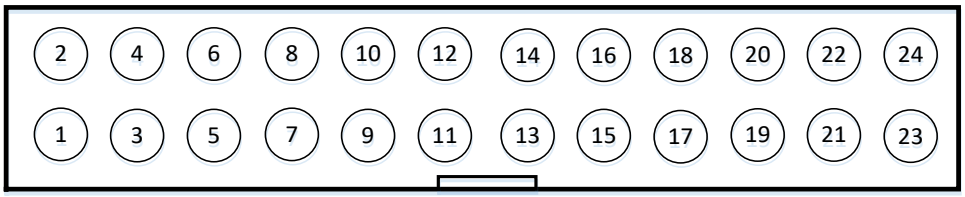
11.14 Fan Control Connector

The motherboard supports two header connectors for enabling fan control. The connector is Molex 87831-2435 or equivalent. Table 24 describes the connector pinout. Figure 21 shows a top view of the physical pin numbering.

Table 24. Fan Control Connector

Management Connector				
Pin	**Signal**	**I/O**	**Voltage**	**Description**
1	FAN5_PWM	O	5V	Fan #5 PWM
2	FAN4_PWM	O	5V	Fan #4 PWM
3	FAN5_TACH	I	5V	Fan #5 Tachometer
4	FAN4_TACH	I	5V	Fan #4 Tachometer
5	P12V	O	12V	12V Fan Power
6	P12V	O	12V	12V Fan Power
7	GND	O	0V	Ground
8	GND	O	0V	Ground
9	FAN3_PWM	O	5V	Fan #3 PWM
10	FAN2_PWM	O	5V	Fan #2 PWM
11	FAN3_TACH	I	0V	Fan #3 Tachometer
12	FAN2_TACH	I	3.3V	Fan #2 Tachometer
13	P12V	I	3.3V	12V Fan Power
14	P12V	I	3.3V	12V Fan Power
15	GND	O	0V	Ground
16	GND	O	0V	Ground
17	FAN1_PWM	O	5V	Fan #1 PWM
18	FAN0_PWM	O	5V	Fan #0 PWM
19	FAN1_TACH	I	5V	Fan #1 Tachometer
20	FAN0_TACH	I	5V	Fan #0 Tachometer
21	P12V	O	12V	12V Fan Power
22	P12V	O	12V	12V Fan Power
23	GND	O	0V	Ground
24	GND	O	0V	Ground

Figure 21. Fan Control Connector Pin Numbering



11.15 TPM Connector

The motherboard supports a header connector for interfacing to a TPM Module. The connector is FCI 91932-32111L or equivalent. Table 25 describes the connector pinout. Figure 22 shows a top view of the physical pin numbering. The TPM 2.0 module is connected to the CPU0 SPI bus.

Table 25. TPM Connector Pinout

TPM Connector				
Pin	**Signal**	**I/O**	**Voltage**	**Description**
1	SPI_CLK	O	3.3V	SPI Clock
2	RESET#	O	3.3V	Reset
3	SPI_MOSI	O	3.3V	SPI Data Out
4	SPI_MISO	I	3.3V	SPI Data In
5	SPI_CS#	O	3.3V	SPI Chip Select
6	I2C_SDA	I/O	3.3V	I2C Data
7	P3V3_STBY	O	3.3V	3.3V Standby Power
8	TPM_PRESENT#	I	3.3V	Indicates physical presence of TPM
9	SPI_IRQ#	I	3.3V	Interrupt
10	I2C_SCL	O	3.3V	I2C Clock
11	GND	O	0V	Ground

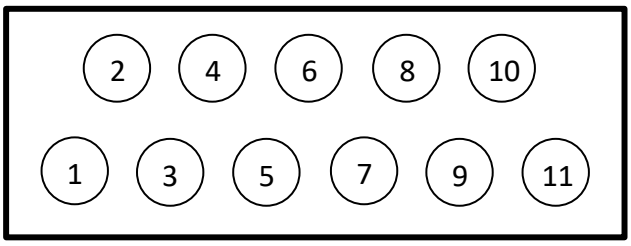


Figure 22. TPM Connector

11.16 Connector Quality

The Project Olympus system is designed for use in datacenters with a wide range of humidity. The connectors for these deployments is capable of withstanding high humidity during shipping and installation. The baseline for plating DIMMs and PCIe connectors will be 30µ”-thick gold. DIMM connectors include lubricant/sealant applied by the connector manufacturer that can remain intact after soldering and other manufacturing processes. The sealant is required to displace any voids in the connector gold plating.

12 Electrical Specifications

The following sections provide specifications for the server input voltage and current, as well as the primary motherboard signals.

12.1 Input Voltage, Power, and Current

Table 26 lists the nominal, maximum, and minimum values for the server input voltage. The maximum and minimum voltages include the effects of connector temperature, age, noise/ripple, and dynamic loading.

Table 26. Input Power Requirements

	Minimum	Nominal	Max
Input voltage	11V DC	12.3V DC	14V DC
Input Power	n/a	n/a	750W
Inrush Rise Time	5ms	n/a	200ms

12V power to the motherboard is supplied through a 24 pin Mini-Fit Jr or equivalent connector. The server provides inrush current control through the 12V bus rail; return-side inrush control is not used. The inrush current rises linearly from 0A to the load current over a minimum 5 millisecond (ms) period (this time period is no longer than 200ms).

12.2 Current Interrupt Protection and Power, Voltage, and Current Monitoring

The motherboard provides a cost-effective way to measure and report server voltage and current consumption, and to make instance reporting available to the system. The motherboard includes power consumption measurements at the inrush controller. (Accuracy of the measurement is +/- 2%)

The motherboard also provides a way to interrupt current flow within 1 microsecond (µs) of exceeding the maximum current load.

12.3 Filtering and Capacitance

The motherboard should provide sufficient input filtering and capacitance to support operation with the power supply as specified in the P2010 PSU Specification.

12.4 Grounding and Return

The server chassis grounding/return is provided to the motherboard from the tray assembly through the alignment and mounting holes that secure the motherboard to the tray. The motherboard is also tied to

the PSU ground through the 12V power connector. Chassis ground and Logic ground are tied together on the motherboard.

13 Physical Specification

The motherboard is nearly compatible with the mechanical requirements of the Project Olympus Universal Motherboard Specification. The motherboard is intended to be deployable in a variety of server mechanical configurations. Figure 23 depicts a 3D drawing of the motherboard with its dimensions. The bottom right sides show the PCIe I/O brackets. The top left side shows the CPU and Memory DIMMs. Shown are locations of two PCIe x16 and one PCIe x32 slots on the motherboard as a reference. Figure 24 is a top view of the motherboard outline.

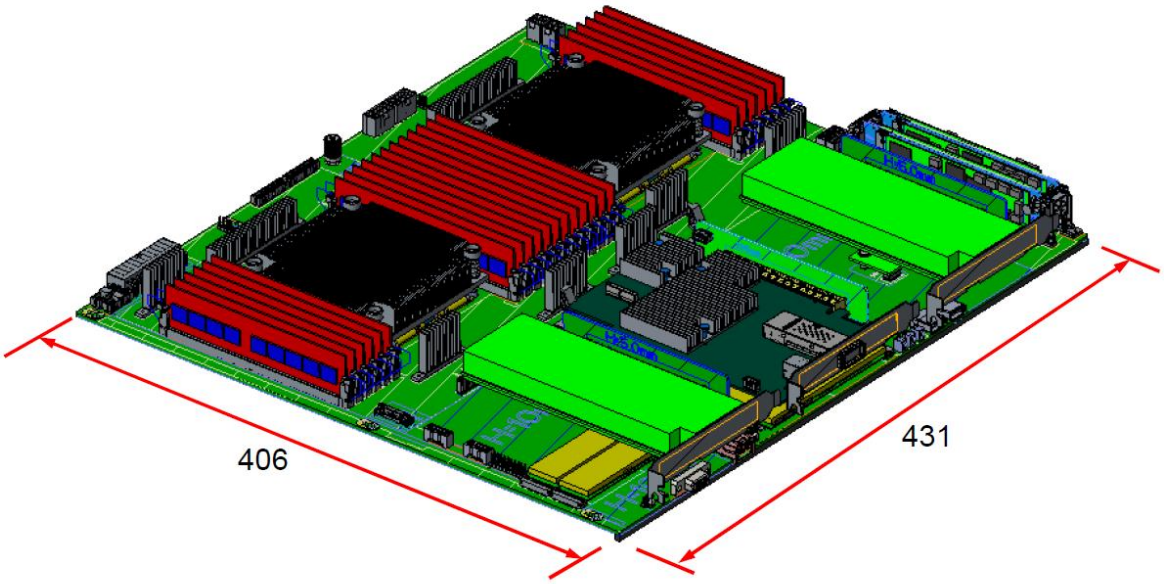


Figure 23. 3D Drawing of Motherboard

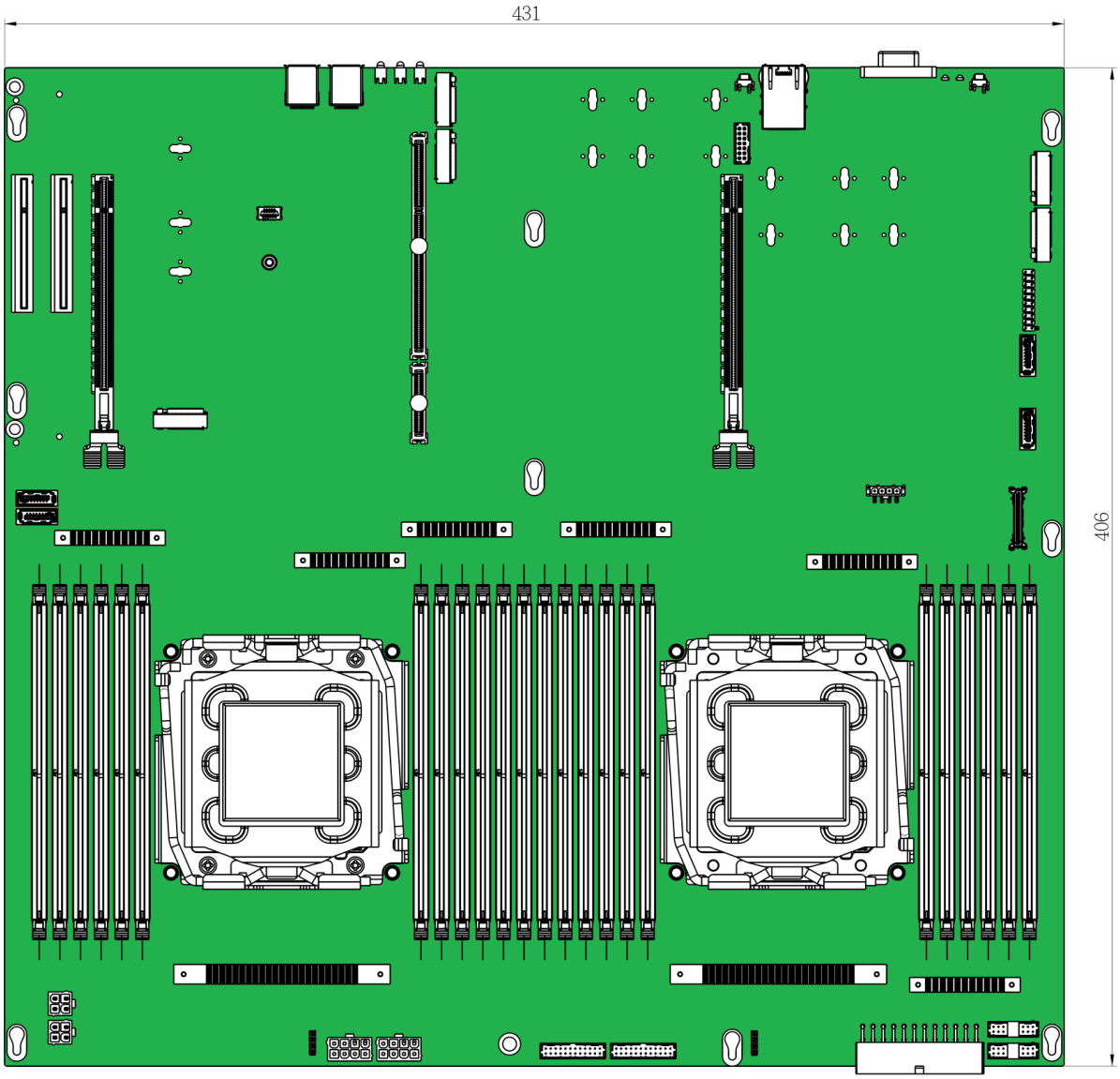


Figure 24. ARMx64 Motherboard Outline

The Project Olympus Cavium ThunderX2™ ARMx64 motherboard is nearly 100% identical to the Project Olympus Universal Motherboard in physical specification. The deviation is the motherboard thickness. Figure 25 shows a side view of the board showing the thickness of ARMx64 motherboard. Figure 26 shows a side view of the Project Olympus Universal Motherboard.

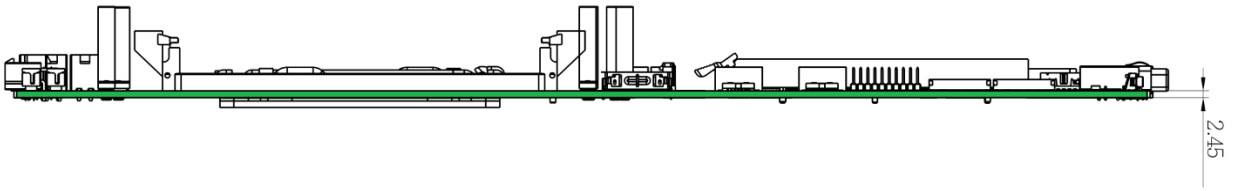


Figure 25. ARMx64 Motherboard Thickness

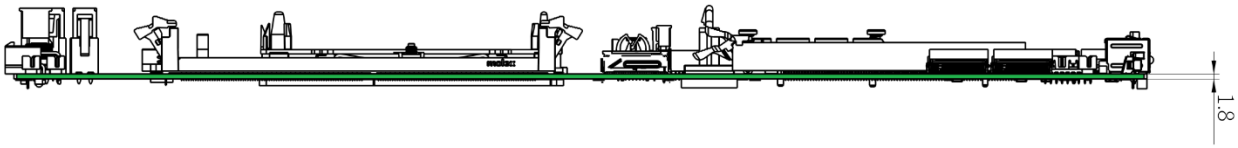


Figure 26. Project Olympus Universal Motherboard Thickness

The difference in the motherboard and CPU socket backplate thickness could lead to impacts to the board standoff design, front I/O hole locations on the mechanical chassis, and PCIe riser design. Figure 27 shows the motherboard thickness differences between this ARMx64 motherboard (bottom image) and the Project Olympus Universal Motherboard. In this example, the board standoff design is shown to be different due to the board thickness and the required spacing between the bottom of the motherboard and the chassis bottom.

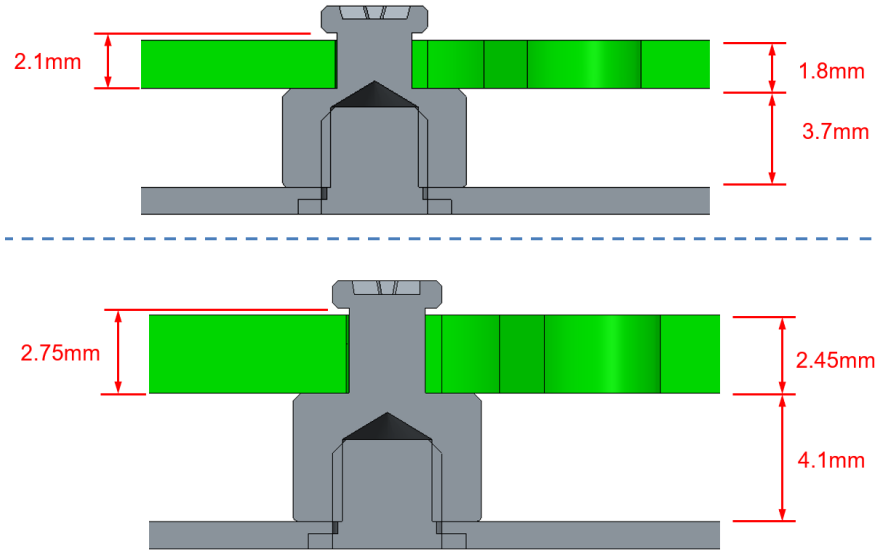


Figure 27. Motherboard Thickness Difference

14 Environmental

The motherboard is designed to be deployed in an environmentally controlled location meeting the environmental requirements. The server has the capability to provide full functional operation under the conditions given.

Table 27. Environmental Requirement

Specification		Requirement
Inlet temperature	Operating	• 50°F to 95°F (10°C to 35°C) • Maximum rate of change: 18°F (10°C)/hour • Allowable derating guideline of 1.6°F/1000ft (0.9°C/304m) above 3000 ft.
	Non-operating	• -40°F to 140°F (-40°C to 60°C) • Rate of change less than 36°F (20°C)/hour

The server is required to use on-board fans to cool the electrical components. A maximum of twelve fans may be used to cool the components on the motherboard and in the chassis assembly. The maximum airflow allowed in a server cannot exceed 158 CFM/kW. The server also operates at its maximum power configuration without performance degradation with 2 failed fans.

Variable fan speed capability allows the rack to minimize energy consumption of the air movers and facilities in conditions that permit it. The speed of airflow is based on component temperature requirements within the server.

15 Electromagnetic Interference Mitigation

For electromagnetic interference (EMI) containment, EMI shielding, and grounding must be accounted for at the server assembly level.