Partial Width, Density Optimized HPM Form (M-DNO) Factor Base Specification

Part of the

Datacenter – Modular Hardware Systems (DC-MHS) Rev 1.0 Family

Version 0.8

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Table of Contents

1. License ... 6
1.1. Open Web Foundation (OWF) CLA ... 6
1.2. Acknowledgements ... 7
2. Version Table ... 8
3. Scope ... 9
3.1. Items Not In Scope of Specification ... 9
3.2. Typical OCP Sections Not Applicable ... 9
4. Specification Compliance Table ... 10
5. Overview ... 11
6. References ... 12
7. Terminology ... 14
8. Background & Assumptions ... 16
8.1. Common Industry Platform Features Considered ... 16
8.2. Architecture Specific Assumptions ... 17
9. HPM Layout Concepts & Definitions ... 18
10. Mechanical ... 21
10.1. HPM Outlines ... 21
10.2. Board Datum and Mounting Holes ... 24
10.3. Board and Assembly Thickness ... 28
10.4. Chassis-to-Board Bracket and Secondary Side Keep Outs ... 30
10.5. HPM to Chassis Retention Mounting ... 36
10.6. Board Handling ... 36
10.7. Common Peripheral Location Requirements ... 37
10.8. Platform Infrastructure Connector Placement ... 38
10.9. Near IO Connector Placement ... 40
10.9.1. Cabled Near IO Connectors ... 40
10.9.2. Fixed Riser Connectors ... 40
10.10. Far Side IO Connector Placement ... 42
10.11. Mounting Hole Requirements for IO Module Retention ... 42
10.12. Primary Side Component Height Restrictions and KOZs ... 43
10.13. Cabling Enablement Keep Out Zones ... 44
11. Power ... 45

11.1. HPM Power Zones 45
11.1.1. Near and Far Bi-Directional (Ingress / Egress) Power Zones 45
11.1.2. Fixed I/O Riser Location Power 47
11.1.3. DC-SCM 2.0 48
11.1.4. OCP NIC 3.0 48
11.1.5. Platform Custom Zone (Type 4 Only) 49
11.1.6. Ingress / Egress Power Connector Locations 49
11.2. HPM Power Planes 50
12. I/O System (Electrical Interfaces) 51
12.1. High Speed IO (HSIO) Connectors 51
12.2. Internal USB 51
12.3. Intrusion Switch 51
12.4. Boot Storage Peripheral 52
12.5. Control Panel 52
12.6. PDB Management Connector 52
13. Supplemental Material: M-DNO Conceptual Implementation Examples 53
14. Supplemental Material: M-DNO Power Zone Usage Examples 64
15. Appendix A - Checklist for IC approval of this specification (to be completed by contributor(s) of this Spec) 68
16. Appendix B-__ <supplier name> - OCP Supplier Information and Hardware Product Recognition Checklist 69

Table of Figures

Figure 1: M-DNO Board Type Layout Overview 19
Figure 2: Near and Far Terminology Example 19
Figure 3: M-DNO Type Interop Goals 20
Figure 4: Type 1 HPM Outline 21
Figure 5: Type 2 HPM Outline 22
Figure 6: Type 3 HPM Outline 23
Figure 7: Type 4 HPM Outline 24
Figure 8: Hole and Pad Details 25
Figure 9: Type 1 Mounting Holes 25
Figure 10: Type 2 Mounting Holes 26
Figure 11: Type 3 Mounting Holes 27
Figure 12: Type 4 Mounting Holes 28
Figure 13: Board and Chassis Stack-up Implications 29
Figure 14: Example of consistent peripheral top surface offset relative to HPM 30
Figure 15: Example of Chassis-to-Board Bracket (Board Pan) 31
Figure 16: Type 1 HPM Secondary Side Zero-Height Keep Out Zones 32
Figure 17: Type 2 HPM Secondary Side Zero-Height Keep Out Zones 33
Figure 18: Type 3 HPM Secondary Side Zero-Height Keep Out Zones 34
Figure 19: Type 4 HPM Secondary Side Zero-Height Keep Out Zones 35
Figure 20: Secondary Side Hole Component KOZ 35
Figure 21: HPM Assembly to Chassis Retention Enablement 36
Figure 22: Example Board Handling Feature 37
Figure 23: Locations of OCP NIC 3.0 and DC-SCM 2.0 37
Figure 24: Platform Infrastructure Connector Placement 38
Figure 25: Type 1 USB Location 39
Figure 26: Platform Infrastructure Connector Placement Zones 39
Figure 27: Fixed Riser Location and Numbering 40
Figure 28: PCIe Near IO Connector Locations (Type 1/2/3) (Riser Centerlines) 42
Figure 29:PCIe Near IO Connector Locations (Type 4) (Riser Centerlines) 42
Figure 30: Primary Side Component Height Restriction Zones 44
Figure 31: Example Type 4 Cable KOZ Layout 44
Figure 32: M-DNO Power Zone Overview (Type 2 and 4 Depicted) 45
Figure 33: Bellwether UHC 2x6 + 12SB PICPWR Connector (Vertical) 46
Figure 34:M-DNO HPM with multimode interface board 47
Figure 35: Near and Far Power Zone Connector Locations 49

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1.2. Acknowledgements

The Contributors of this Specification would like to acknowledge the following companies for their feedback:

List all companies or individuals who may have assisted you with the specification by providing feedback and suggestions but did not provide any IP.

2. Version Table

Date	Version #	Description
4/21/2022	0.7	• Initial Public Release
6/22/2022	0.8	• Added Specification Compliance Table • Separated hole dimensioning to separate drawings • Added required pad size and recommended KOZs for all holes throughout document • Adjusted fixed riser connector positioning • Updated approach in Primary Side Component Height section • Added start of “zone” approach to PIC connector placement • Various text clarifications / edits • Various drawing updates and fixes

3. Scope

This document defines technical specifications for the Density Optimized Form Factors used in Open Compute Project Data Center Modular Hardware System.

Any supplier seeking OCP recognition for a hardware product based on this spec must be 100% compliant with any and all features or requirements described in this specification.

3.1. Items Not In Scope of Specification

- Compute Core (CPU/Memory/Voltage Regulators/SMP routing between CPUs)
- JTAG/Debug connectors for the Compute Core
- CPU, Memory, Heatsink, Liquid and any other thermal solutions
- Reliability requirements and design-in details
- BOM Population requirements
- Cooling System Connections (Fans, etc).

3.2. Typical OCP Sections Not Applicable

This is a Base specification, requiring other MHS specifications to fully define a design. The following typical Sections of an OCP specification are not included because they are not applicable to this specification.

- Rack Compatibility (Discussed in Section 8)
- Physical Spec
- Thermal Design
- Rear Side Power, I/O, Expansion
- Onboard Power System
- Environmental Regulations/Requirements
- Prescribed Materials
- Software Support
- System Firmware
- Hardware Management (Leverages OCP DC-SCM V2)
- Security

4. Specification Compliance Table

The following table is intended summarize the list of attributes and requirements for a design to be MHS – DNO Spec Compliant. It specifies only required attributes for compliance and does not list optional attributes.

Table 1. Specification Compliance Summary Table

Item	Requirement	Document Reference
	Mechanical	**Chapter 10**
1	Defined Board Outline	Section 10.1, Figure 4 - Figure 7
2	All required mounting holes with associated pads	Section 10.2, Figure 8- Figure 12
3	Unique alignment hole and slot	Section 10.2, Figure 8- Figure 12
4	Board Thickness <= 3.18mm	Section 10.3, Figure 13
5	Board Assembly Thickness <= 5.86mm	Section 10.3, Figure 13
6	Secondary side zero height keep out zones	Section 10.4, Figure 16 - Figure 19
7	Secondary side universal component height restriction	Section 10.4, Figure 16 - Figure 19
8	HPM to Chassis Retention hole and associated keep outs	Section 10.5, Figure 21
9	Far Side hole for board handling	Section 10.6, Figure 22
10	Specified Location for OCP NIC 3.0 Co-Planar Connector	Section 10.7, Figure 23
11	Specified Location for DC-SCM Co-Planar Connector	Section 10.7, Figure 23
12	Primary control panel connector placed within specified zone	Section 10.8, Figure 24
13	Intrusion switch header placed within specified zone	Section 10.8, Figure 24
14	Host USB connector placed within specified zone	Section 10.8, Figure 24 & Figure 25
15	PDB Management connector placed within specified zone	Section 10.8, Figure 24
16	Any implemented board to board riser connectors placed in specific defined location	Section 10.9.2, Figure 27 - Figure 29
17	2 (Type 1,2,3) or 3 (Type 4) I/O Retention Holes	Section 10.9.2, Section 10.11, Figure 27
18	All non-exempt soldered components adhere to Primary Side component height restrictions	Section 10.12, Figure 30
	Power	**Chapter 11**
19	Far side Ingress / Egress Power Zone with 1 (Type 1 & 2) or 2 (Type 3 & 4) 864W + 12SB PICPWR connectors in specified location(s)	Section 11.1.1, Section 11.1.6, Figure 35
20	If implemented, Near side Ingress / Egress Power Zone with 1 (Type 1 & 2) or 2 (Type 3 & 4) 864W + 12SB PICPWR connectors in specified zone	Section 11.1.1, Section 11.1.6, Figure 35
21	Each implemented riser location connector rated for 180W and PICPWR compliant	Section 11.1.2, M-PIC
22	HPM delivers at least 87W to each implemented riser location	Section 11.1.2
23	HPM delivers power as defined in OCP DC-SCM 2.0 specification to DC-SCM connector	Section 11.1.3, OCP DC-SCM R2.0
24	HPM delivers power as defined in OCP NIC 3.0 specification to DC-SCM connector	Section 11.1.4, OCP NIC R3.0
25	HPM power shapes have a max 30C T-rise	Section 11.2
26	At maximum load, HPM voltage drop between primary power ingress and egress connectors is <= 1%	Section 11.2
	Electrical (I/O System)	**Chapter 12**
27	All HSIO connectors (near and far) are M-XIO compliant	Section 12.1, M-XIO
28	Internal USB follows M-PIC specification	Section 12.2, M-PIC
29	Intrusion Switch follows M-PIC specification	Section 12.3, M-PIC
30	If implemented, boot storage peripheral follows M-PIC specification	Section 12.4, M-PIC
31	Primary control panel follows M-PIC specification	Section 12.5, M-PIC
32	If implemented, secondary control panel follows M-PIC specification	Section 12.5, M-PIC
33	PDB Management Connector follows M-PIC specification	Section 12.6, M-PIC

5. Overview

The objective of this specification is to outline the requirements of a family of partial width, **D**e**N**sity **O**ptimized Host Processor Module (HPM) form factors within the OCP **M**odular hardware system group of specifications (**M-DNO** for short). This M-DNO specification embodies design considerations for CPU, DIMMs, and other server processor related features commonly used by the industry today but is in not limited to only those functions. For instance, an FPGA array being placed within the Compute Area of the HPM is allowable per this specification. The HPM is designed with standard 19” rack, also known as compliant with EIA - 310-D and larger 21” racks in mind but is not limited to only those solutions. This specification considers both monolithic and multi-node / “blade” based system architectures in its definition.

The goals and successes of this specification are defined by allowing multiple generations of Compute Core (CPU/Memory) designs implemented to the specification to enable reuse of chassis and system level components over multiple generations and HPMs. Implementing to this specification and design methodology should result in reduced design investment, reduced validation investment, broader product portfolios and faster development cycle times due to enhanced reuse and leverage opportunity for each HPM designed.

This specification shall define attributes and design requirements that are common and critical to the use and deployment of Enterprise and Cloud solutions as well as EDGE optimized service provider products. Examples of these attributes are mechanical form factor, placement guidance of common subsystems and placement guidance of HPM Power and Input-Output (IO) connections.

6. References

DC-MHS Family of Specifications

The **D**ata **C**enter – **M**odular **H**ardware **S**ystem (DC-MHS) family of specifications are written to enable interoperability between key elements of datacenter and enterprise infrastructure by providing consistent interfaces and form factors among modular building blocks. At the time of this publication there are the following specification workstreams:

- **M-FLW** (**M**odular Hardware System **F**u**l**l **W**idth Specification) – Host Processor Module (HPM) form factor specification optimized for using the full width of a Standard EIA-310 Rack mountable server. The specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-DNO** (**M**odular Hardware System Partial Width **D**e**n**sity **O**ptimized Specification) – Host Processor Module (HPM) specification targeted to partial width (i.e. ½ width or ¾ width) form factors. Such form factors are often depth challenged and found not only in enterprise applications but also in Telecommunications, Cloud and Edge Deployments. While the EIA-310 Rack implementation is chosen as a key test case for use, the specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-CRPS** (**M**odular Hardware System **C**ommon **R**edundant **P**ower **S**upply Specification) – Specifies the power supply solutions and signaling expected to be utilized by DC-MHS compatible systems.
- **M-PIC** (**M**odular Hardware System **P**latform **I**nfrastructure **C**onnectivity Specification) – Specifies common elements needed to interface a Host Processor Module (HPM) to the platform/chassis infrastructure elements/subsystems. Examples include power management, control panel and cooling amongst others.
- **M-XIO** (**M**odular Hardware System E**x**tensible **I**/**O**) – Specifies the highspeed connector hardware strategy. An M-XIO source connector enables entry and exit points between sources such as Motherboards, Host Processor Modules & RAID Controllers with peripheral subsystems such as PCIe risers, backplanes, etc. M-XIO includes the connector, high speed and management signal interface details and supported pinouts.
- **M-PESTI** (**M**odular Hardware System **Pe**ripheral **S**ideband **T**unneling **I**nterface) – Specifies a standard method for discovery of subsystems, self-describing attributes, and status (e.g., versus a priori knowledge/hard coding firmware and BIOS for fixed/limited configurations). Examples: vendor/module class, physical connectivity descriptions, add-in card presence, precise source to destination cable coupling determination.

To access additional DC-MHS specifications please visit the OCP Server Project Wiki - Working

Additional References

This specification also relies on the following Open Compute Project specifications

- OCP Server Network Interface Card (NIC) 3.0 – Specifies NIC card form factors targeting a broad ecosystem of NIC solutions and system use cases. Mezz (NIC) » Open Compute Project

- OCP Datacenter Secure Control Module (DC-SCM) 2.0 – Specifies an SCM designed to interface to an HPM to enable a common management and security infrastructure across platforms within a data center. Hardware Management/Hardware Management Module - OpenCompute

7. Terminology

Standardized Term	Meaning	Alternative Terms
Shall	Indicates a requirement for spec compliance	Must
DC-SCM	Datacenter Secure Control Module v2 as defined by OCP DC-SCM 2.0 spec	SCM
PCB	Printed Circuit Board	PCBA
HPM (Host Processor Module)	PCB or PCBA form-factor being defined by this spec	Motherboard, board
Chassis-Board Bracket	Bracket that attaches to an HPM assembly, that enables a variety of board outlines and hole locations to change over time, and still fit within same chassis base.	Board Pan
Near	Board location or zone, related to section of board closer to the datum	
Far	Board location or zone, opposite of location of datum	
Platform	Complete system including HPM, power, peripherals, etc	
Compute Core	Elements of board design that are critical to processor and memory support, inclusive of CPU and Memory sockets. Examples are Voltage Regulators, High Speed IO routing, High speed trace routing between multiple processors, high speed trace routing between processors and memory, etc	
IO	Input Output, commonly referring to high speed connections to a CPU socket.	
PCIe	Peripheral Component Interconnect Express	
CXL	Compute Express Link	
HSIO	High Speed IO, commonly referring to PCIe routing, PCIe connectors, CXL routing/connectors, etc.	
OCP	Open Compute Project	
OEM	Original Equipment Manufacturer	Enterprise
CSP	Cloud Service Provider	
½ Width HPM	210mm wide HPM, enables systems with 2 HPMs side by side in 19” Rack	
¾ Width HPM	295mm wide HPM, enables systems with HPM adjacent to 2xM-CRPS PSUs	
Platform Custom Zone	Area of system board where space is allotted for Platform designers to implement custom features.	

Platform Infrastructure Connectivity Specification	Refer to Section 6 (References)	M-PIC
Full Width Specification	Refer to Section 6 (References)	M-FLW
Common Redundant Power Supply Specification	Refer to Section 6 (References)	M-CRPS, CRPS PSU
Extensible I/O Specification	Refer to Section 6 (References)	M-XIO
KOZ	Keep Out Zone, a design term for PCB designs that defines area of a board design where no components may be placed, usually to enable mechanical attachments or mechanical features.	
KIZ	Keep In Zone, a design term for PCB designs that define a zone with a height restriction (such as a volume), which the components selected for that part of the board design must comply with the height restriction of that zone.	
Compliant HPM	An HPM which meets every item listed in the M-DNO specification compliance table.	
Adapted HPM	An HPM that utilizes a Compliant HPM as a construct, with a specific set of repeatable modifications which form the adaptation.	
HPM Designer	The person or organization designing an HPM (whether compliant or adapted) which implements the M-DNO specification.	
System Designer	The person or organization designing a system which incorporates M-DNO HPMs (whether compliant or adapted) into the system design.	

8. Background & Assumptions

M-DNO targets a wide variety of 1 and 2 socket platforms including multi-node and monolithic (one HPM per chassis) systems for use in Enterprise, Cloud, and EDGE applications. In these applications the range of targeted chassis can be extremely varied, as can the location of the HPM within the chassis. Monolithic systems are typically, but not limited to, 1RU or 2RU designs. Multi-node systems on the other hand are expected to have a broad application set from 2U (e.g. 4 ½ Width HPMs) to 5U (e.g. 8-12 ½ Width HPM in vertical orientation) chassis and beyond. Rear and Front service models (including articulating chassis with removable top cover) are also considered.

When considering representative system depth targets the most common environments were distilled into the following categories:

1. **Standard Depth Rack / Solution**
   - ~1070mm+ deep with a single ½ width (210mm) or ¾ width (295mm) HPM
   - ~1070mm+ deep with two ½ width (210mm) HPMs
2. **Mid Depth Rack / Solution**
   - ~430mm to 570mm deep with a single ½ width (210mm) or ¾ width (295mm) HPM
3. **Short Depth Rack / Solution**
   - ~300mm to ~430mm deep with a single ½ width (210mm) HPM

This specification shall focus on products targeted to these primary environments. **<u>Section 13</u>** illustrates design scenarios for each of these solutions providing the reader a clearer understanding of each category. This specification does not in any way prohibit alternate environments.

8.1. Common Industry Platform Features Considered

Mechanical

- Chassis installation within minimum EIA-310-D racks (but not limited to)
- PCIe Riser Connector fixed placement
- PCIe Cable route considerations
- Any additional fixed connector placement

I/O

- PCIe (Version 3.0, 4.0, 5.0, and future) Card configurations typically offered by Enterprise OEMs/CSPs/CoSPs.
- In 1U offerings with PCIe CEM based I/O, only Half-Length PCIe cards (167.6mm) are considered. This does not prevent Three-Quarter Length (254mm) cards, but support for Three-Quarter Length cards would restrict Compute Core placement (not defined).
- Use of Open Compute peripherals connectors on the HPM
  - OCP NIC v3.0
  - DC-SCM v2.0
  - *Note: While each HPM outline requires 1 connector of each type, a system* is not limited to 1 device of each type; configurations with 0 or >1 OCP NIC v3 / DC-SCM v2.0 are possible, but outside the scope of this specification

Power

- HPM supplied power to each fixed riser locations
- HPM Power Ingress and Egress connector placement for a variety of power layouts (PSUs with Cabled PDB, blind mate to bus bar, multi-node backplane, etc.)
- Considerations for Power Delivery to important chassis subsystems.

Thermal

- Thermal Design considerations including keep-out zone to enable thermal solutions that extend beyond the CPU and Memory sockets.

8.2. Architecture Specific Assumptions

Mechanical / Systems

- M-DNO based systems
    - Do not direct plug PSUs into the HPM but instead leverage Power Distribution Boards (PDB) or other system / rack level power infrastructure
    - Use remote fan designs in air cooled platforms (there is no HPM spec provision for Fan connectors on the HPM)
    - Support riser based I/O cards, cable based I/O cards or a mix of both
    - Leverage a variety of front and rear service models of I/O, PSU, HPM, etc.
- Systems designed for larger HPM Types may support use of smaller Types in a common chassis or sled with minimal changes (e.g. cables, riser quantities)
- Multi-node chassis designs leverage static rails with overall inner chassis opening width of 443mm (in 19” rack)
- Monolithic chassis designs leverage slide rails with overall inner chassis width of 431mm (in 19” rack)
- ¾ Width HPM must accommodate 2x 60mm M-CRPS PSUs within chassis opening described above (431mm)

I/O

- All M-DNO HPM Types enable (but do not require systems to leverage) use of “off the shelf” OCP NIC V3.0
- Mid / Standard Depth systems will *typically* leverage Coplanar OCP NIC layouts
- Short Depth systems will often require alternate implementation such as “floating” the OCP NIC (or no-pop)
- PCIe CEM based I/O will be the predominant use case for consideration but alternate form factors are not prohibited

DC-SCM

- All M-DNO HPM Types enable (but do not require systems to leverage) use of “off the shelf” DC-SCM 2.0
- Mid / Standard Depth systems will *typically* leverage Coplanar DC-SCM
- Short Depth systems will often require alternate implementation such as “floating” DC-SCM

9. HPM Layout Concepts & Definitions

To achieve the goals outlined in **Section 8**, this M-DNO specification defines four different HPM board "Types" – the design goal of each type is described below. Note that the M-DNO specification does NOT mandate CPU / DIMM quantities or define a specific area for CPU and Memory, design goals are provided for *reference only*.

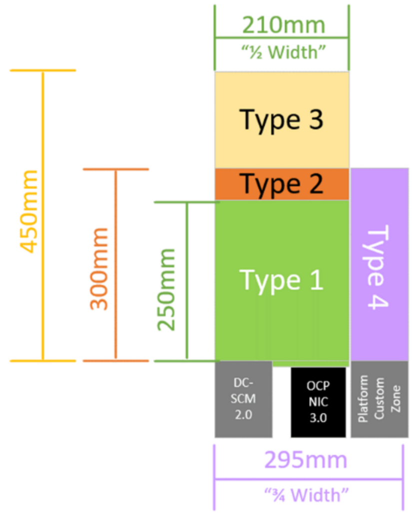
CPU Class Assumptions:

- Entry CPU => Limited Memory Capacity and Bandwidth per CPU with basic capabilities
- Mainstream CPU => Moderate Memory Capacity and Bandwidth per CPU with advanced capabilities
- Extreme CPU => Extreme Memory Capacity and Bandwidth per CPU with extreme capabilities

M-DNO HPM Type Support Goals

- Type 1: ½ Width 1 CPU Depth Optimized
  - 1 Entry or 1 Mainstream CPU
  - 1 or 2 DPC
  - Supports cable based I/O and / or 2 board to board riser locations
- Type 2: ½ Width 1 CPU Feature Optimized
  - 1 Mainstream or 1 Extreme CPU
  - 1 or 2 DPC for Mainstream CPU, 1 DPC for Extreme CPU
  - Supports cable based I/O and / or 2 board to board riser locations
- Type 3: ½ Width 2 CPU "Shadowed"
  - 2 Entry or 2 Mainstream CPUs
  - 1 or 2 DPC
  - Supports cable based I/O and / or 2 board to board riser locations
- Type 4: ¾ Width 2 CPU "Spread" or Extreme 1 CPU
  - 2 Entry or 2 Mainstream CPUs with 1 DPC **or**
  - 1 Extreme CPU with 2 DPC
  - Supports cable based I/O and / or 3 board to board riser locations

Figure 1: M-DNO Board Type Layout Overview

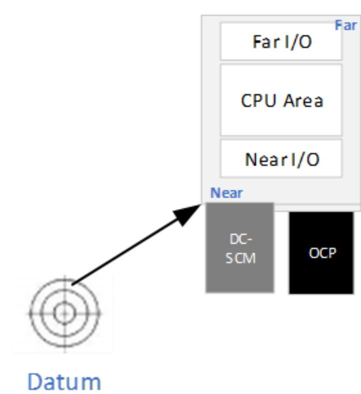


<u>Figure 1</u> provides a dimensional overview of the four board types, additional definitions and concepts are described below:

1. Due to the wide array of potential HPM and Chassis configurations, this specification defines a **Near** <<Element>> as the <<Element>> closer to the Datum (0,0 reference) and **Far** <<Element>> as the <<Element>> further from the Datum, examples for <<Element>> include:
    a. Corner
    b. Edge
    c. I/O Zone

    An example of Near and Far terminology usage is shown in **<u>Figure 2</u>**.

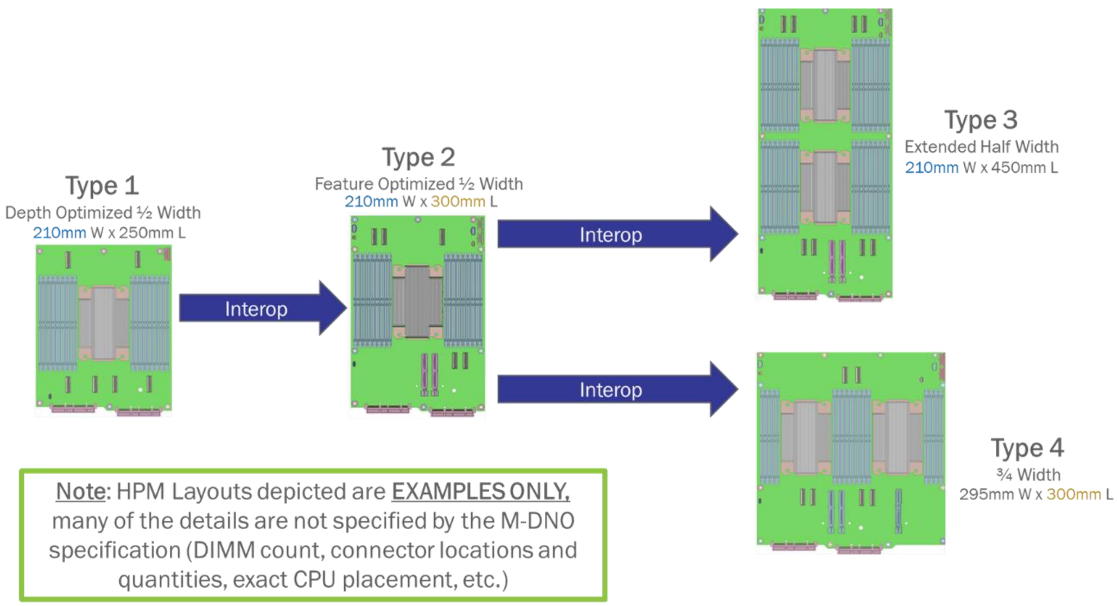
Figure 2: Near and Far Terminology Example



2. The location of the DC-SCM and OCP NIC connector on the HPM shall be common across all types relative to the Datum (0,0)
3. "½ Width" refers to the common 210mm HPM width shared by Type 1,2 and 3
4. "¾ Width" refers to the 295mm HPM width used in Type 4
5. "Full Width" HPMs are outside the scope of this specification and are defined by the M-FLW specification

6. HPMs narrower than ½ Width are also outside the scope of this specification due to the inability of supporting common DCSCM 2.0 and OCP NIC 3.0 connector locations as described in #2
7. The goal of this specification is to provide HPM Interoperability of smaller M-DNO HPM Types in systems designed for larger M-DNO HPM Types with minimal modifications (e.g. board pan or I/O cable changes), as depicted in **Figure 3**:
    a. Type 1 HPMs can be used in systems which support Type 2, 3 or 4 HPMs
    b. Type 2 HPMs can be used in systems which support Type 3 or 4 HPMs

Figure 3: M-DNO Type Interop Goals



Implementors Note: Type 1 is represented with no fixed riser location support because it is expected that most Type 1 designs will exclusively use cabled based I/O due to board depth challenges. If feasible Type 1 HPMs may elect to implement the same riser locations as Type 2 and Type 3.

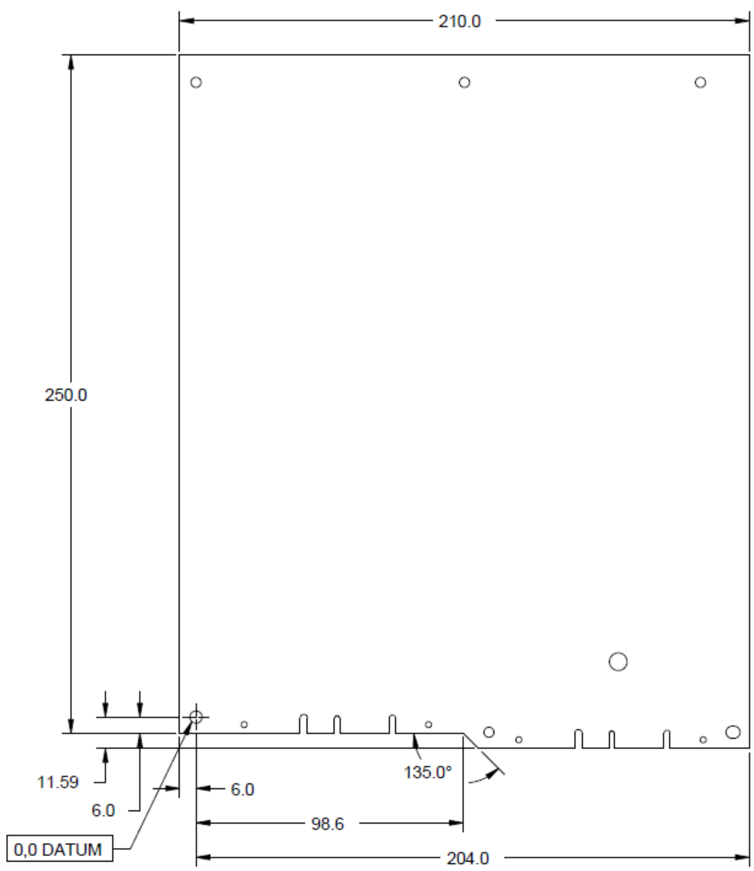
10. Mechanical

10.1. HPM Outlines

There are 4 M-DNO HPM Type Outlines defined as described in **Section 9**. High level outline dimensions are provided below. No tolerances are to be implied. DFX/CAD files will be provided for further detail.

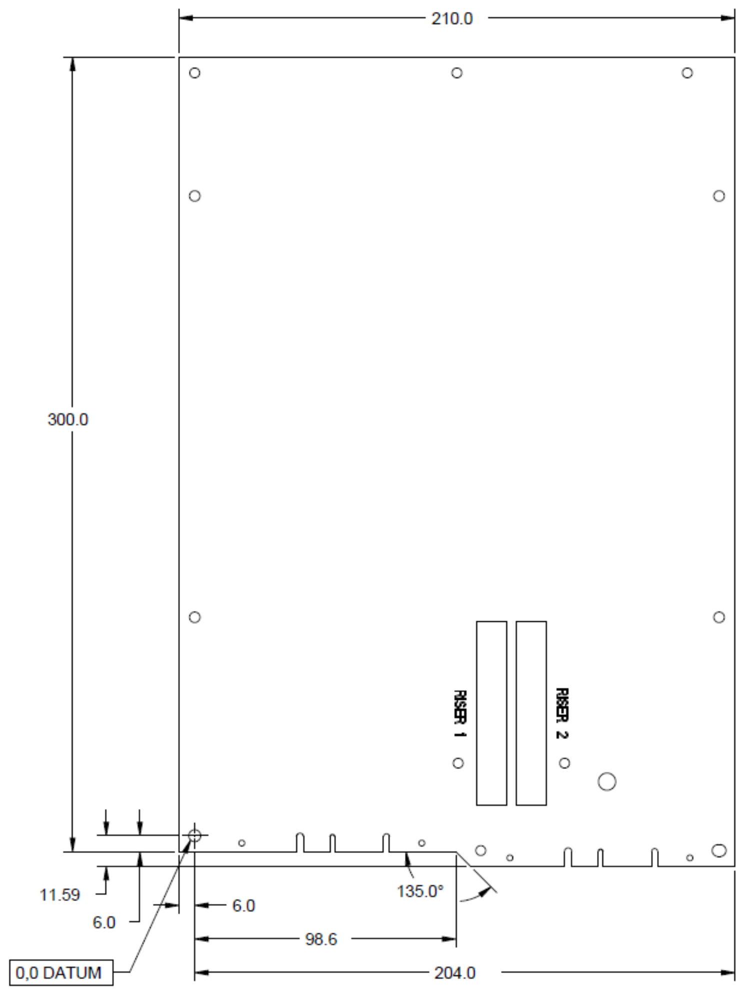
The M-DNO Type 1 Outline is defined in **Figure 4** below. Units are mm. Note: Type 1 is represented with no fixed riser locations, refer to the Implementors Note in **Section 9**.

Figure 4: Type 1 HPM Outline



The M-DNO Type 2 Outline is defined in **Figure 5** below. Units are mm.

Figure 5: Type 2 HPM Outline



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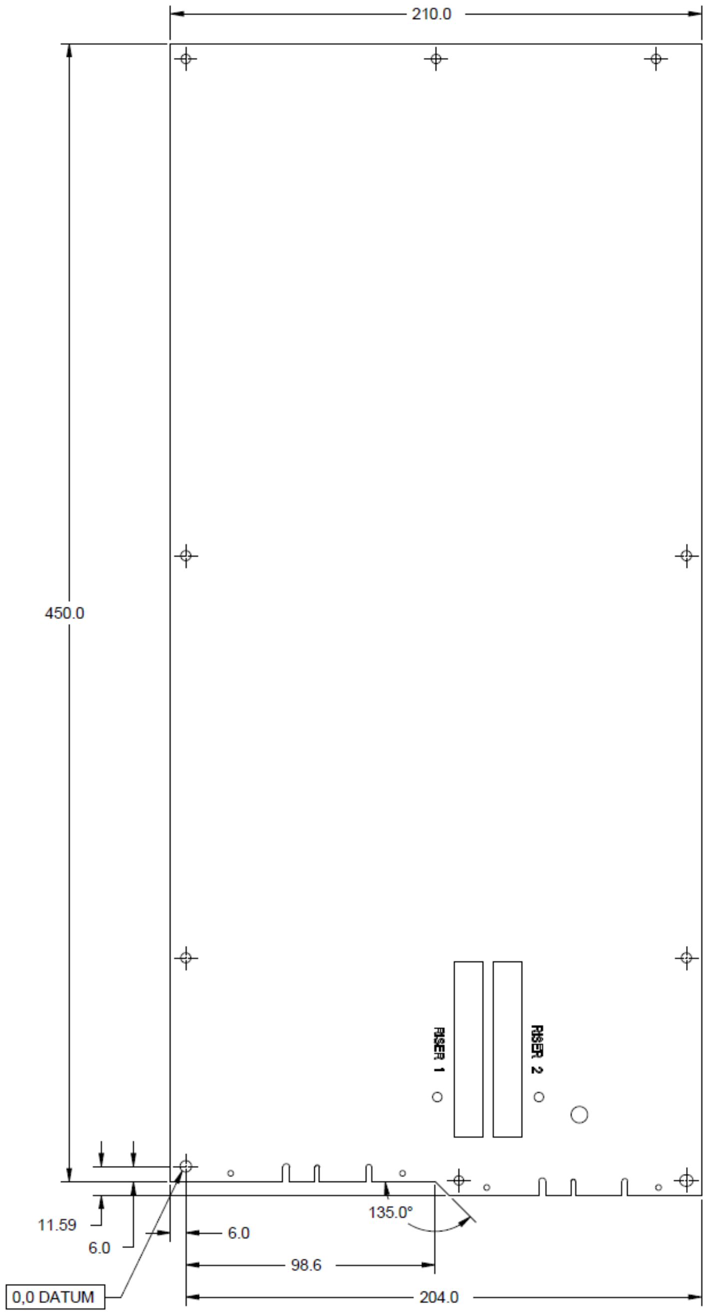
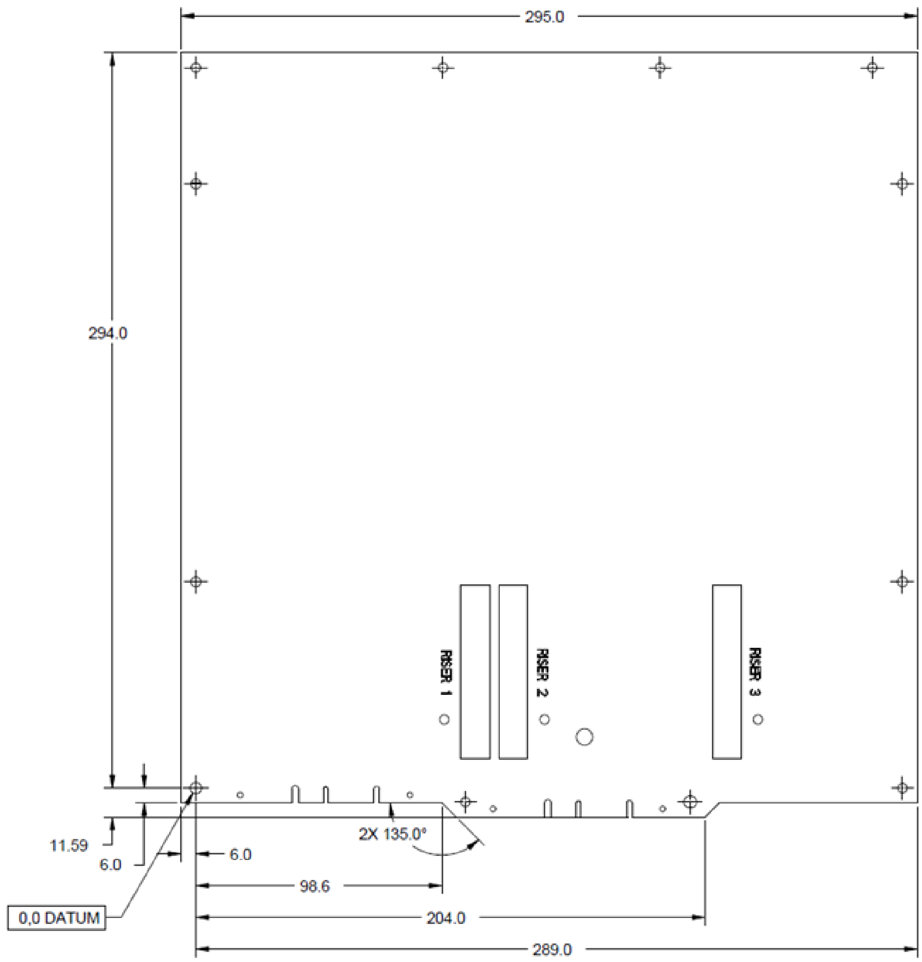
The M-DNO Type 3 Outline is defined in Figure 6 below. Units are mm.

Figure 6: Type 3 HPM Outline



The M-DNO Type 4 Outline is defined in Figure 7 below. Units are mm.

Figure 7: Type 4 HPM Outline



10.2. Board Datum and Mounting Holes

All M-DNO board types leverage a common datum location at the center of the mounting hole in the near corner of the board where the DC-SCM 2.0 connector resides. This allows for fixed elements (riser connectors, peripheral connectors, …) to have a common reference across all 4 board types.

With consideration of interoperability goals and the variety of targeted system configurations, a set of required board mounting hole locations are specified for the 4 M-DNO HPM Types in **Figure 9-Figure 12**.

Detailed hole information common to all board types is provided in **Figure 8**.

On each board type the PCB Datum hole (Detail C) is defined such that a collared standoff with tight fit can be used to control X-Y tolerances in HPM mounting. Additionally, each board type requires a slotted hole (Detail B) to control rotation around the datum, a collared standoff can be used with tight fit to the top of the slot. All other mounting holes follow standard mounting hole guidance (Detail A).

All holes shall adhere to the specified pad sizes.

Implementors may choose to add additional standard mounting holes.

A design should follow good engineering practices in consideration of Platform Shock and Vibration requirements. Shock and Vibration requirements are not in scope of this specification

Figure 8: Hole and Pad Details

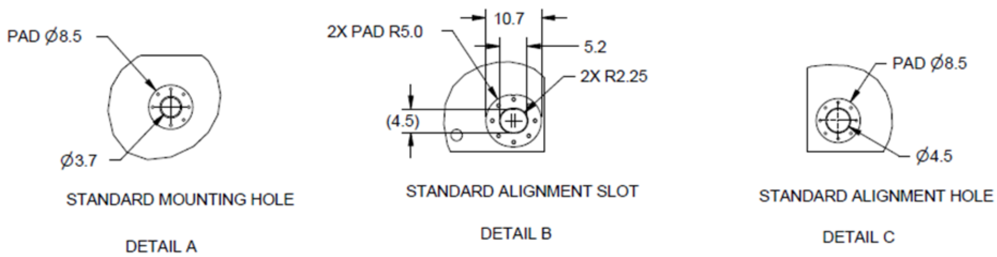


Figure 9: Type 1 Mounting Holes

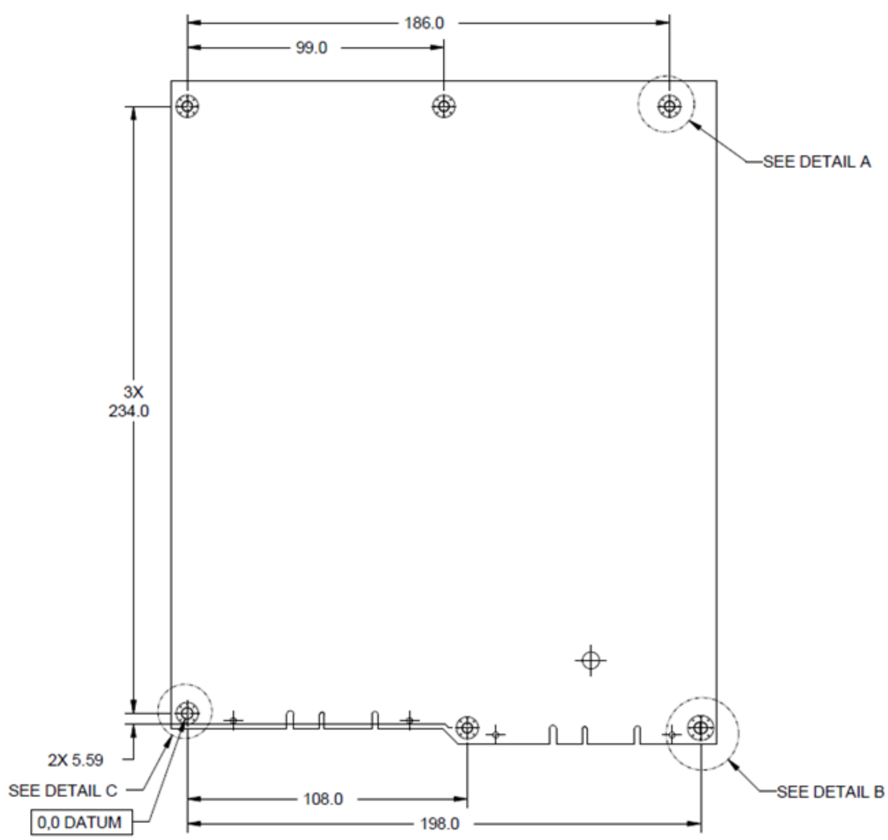
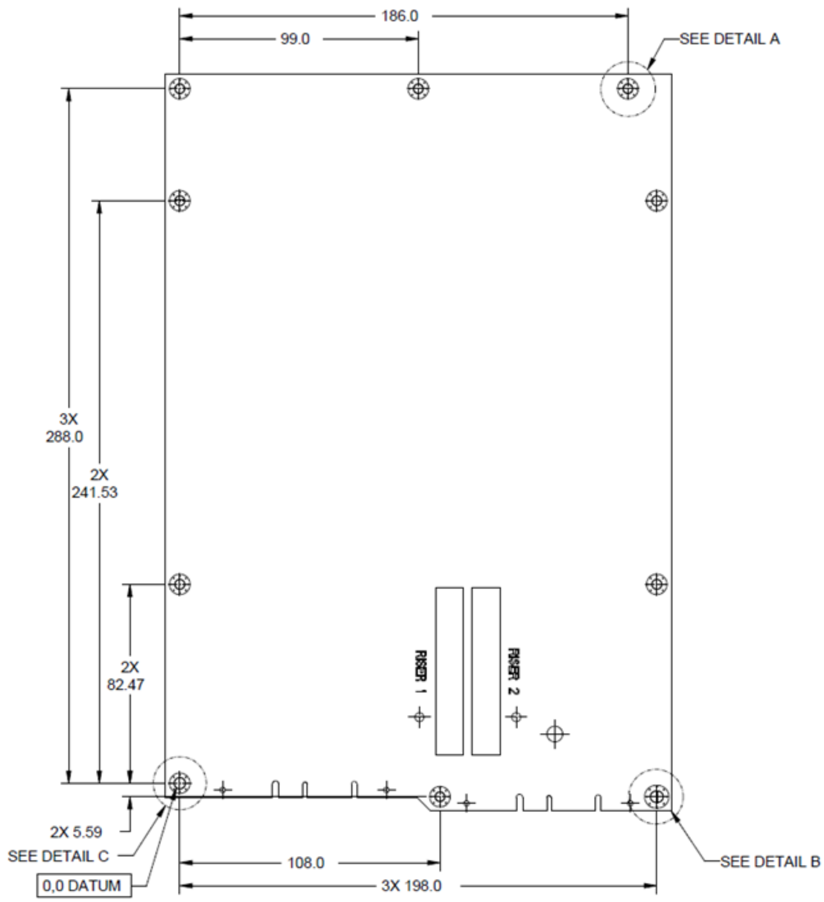


Figure 10: Type 2 Mounting Holes



495 *Figure 11: Type 3 Mounting Holes*

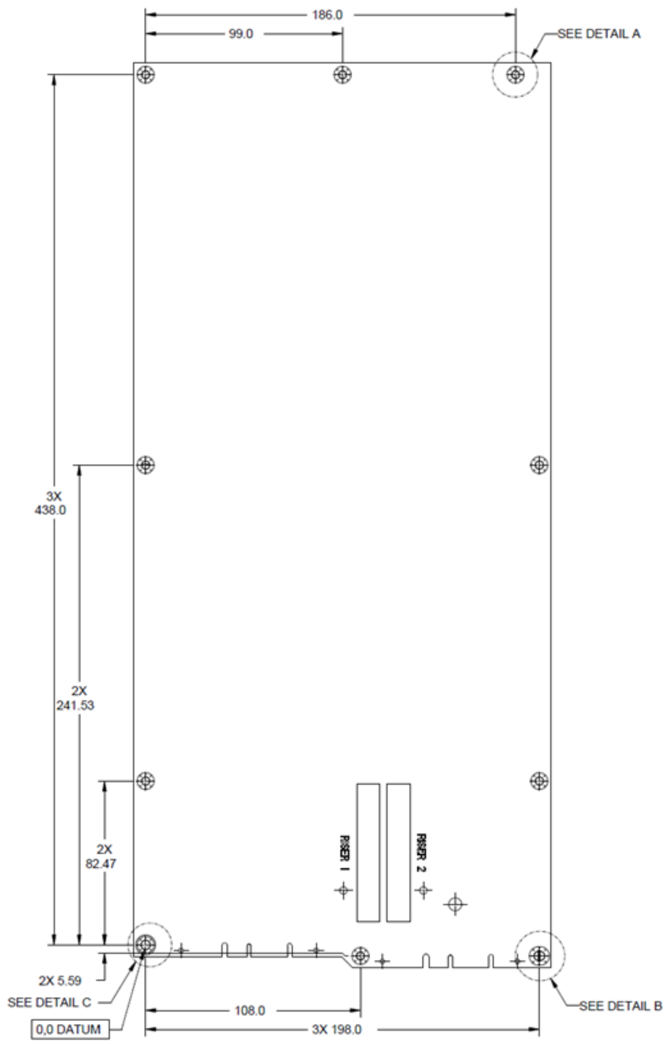
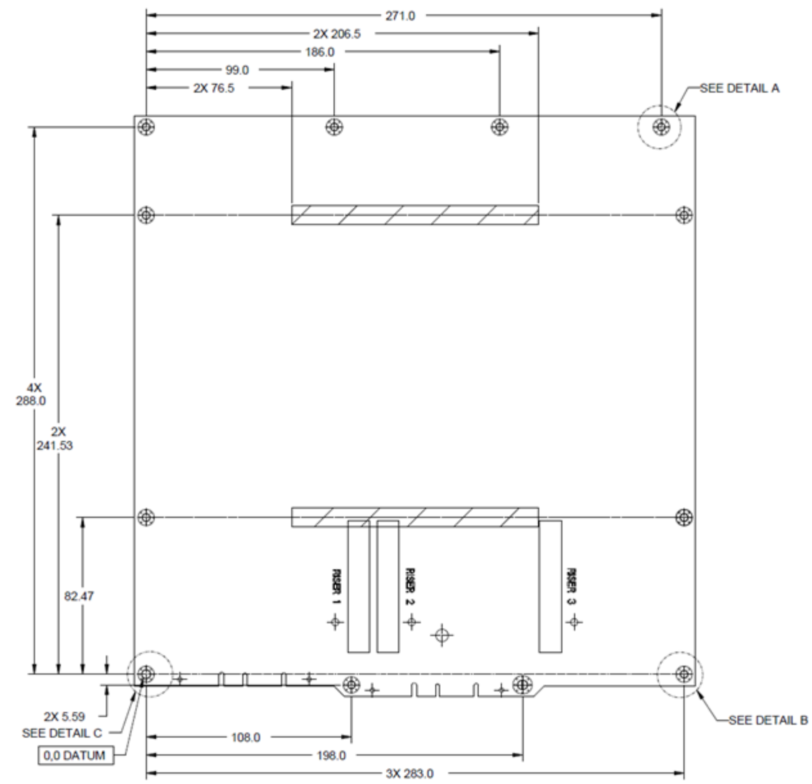


Figure 12: Type 4 Mounting Holes



Note that **Figure 12** defines two recommended zones for mid-board mounting hole locations, the quantity of holes and location of the holes within the zones are at the discretion of the HPM designer.

10.3. Board and Assembly Thickness

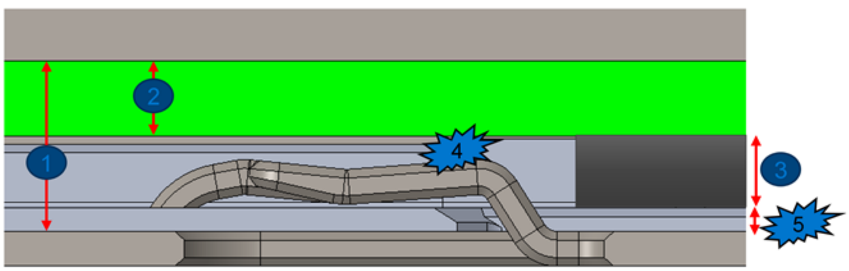
The maximum board thickness allowed is 3.18mm nominal, assuming +10% max tolerance.

The maximum overall thickness of the board assembly, including any insulators and backing plates, is 5.86mm.

Backing plates are assumed to be allowed to protrude through cuts in the Chassis-to-Board bracketry and / or HPM sled.

These thicknesses are critical to ensure a consistent maximum height for system components (e.g. Riser solutions) across M-DNO HPMs. Refer to **Figure 13** and **Table 2** for typical approaches and example scenarios. Note that while the depicted chassis supports a board pan the same maximum thicknesses apply to chassis with no board pan (e.g. a sled based solution).

Figure 13: Board and Chassis Stack-up Implications



1. HPM Top Surface Height to Chassis base
2. HPM Thickness
3. Backing Plate Thickness
4. Gap from HPM to Mounting hook
5. Gap to chassis base (may cut thru sub-pan

Table 2. Board Stackup and Thicknesses

(dimensions in mm)	1 HPM Height	2 HPM Thickness	3 Backplate	5 Gap Backplate to Base Chassis
Typical Nominal Range	5.0 - 5.86	1.57 - 3.18	2.0 – 2.6	
Scenario 1 Nominal	5.2	2.6	2.2	0.4mm
Scenario 2 Nominal	5.86	3.18	2.6	0.08mm
Worst case Gap 5 scenario	5.5	3.5	***~2.0mm***	***0***

Implementors Note:

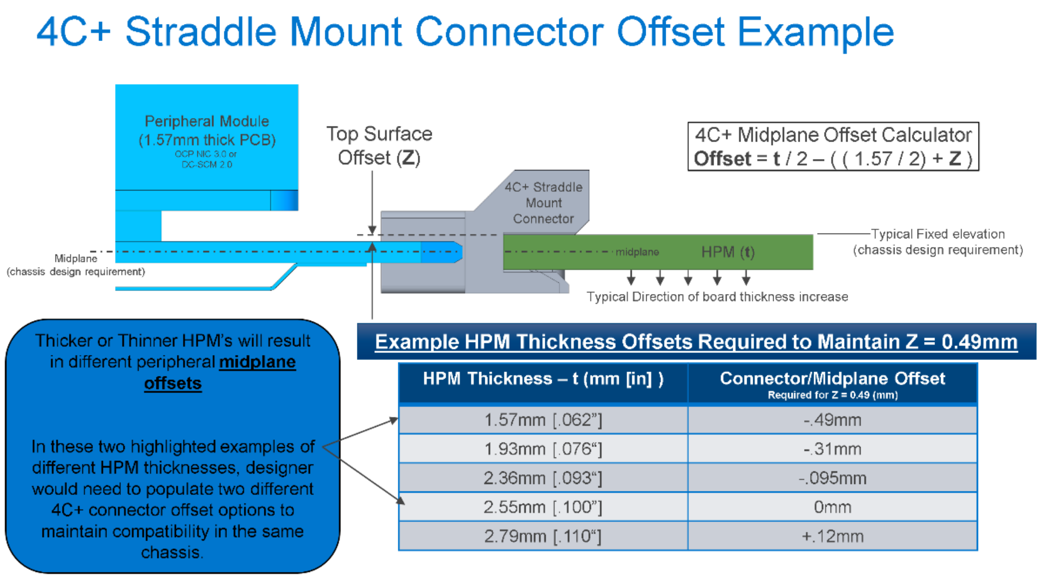
Designers should consider that variations in HPM thickness combined with 4C+ connector selection may result in variation of the vertical offset locations of OCP NIC V3 and DC SCM 2.0 peripherals relative to fixed chassis openings and the top surface of the HPM. There are common connectors in the industry which will result in varying offset locations.

Figure 14 demonstrates how selecting the variance of midplane offset within the 4C+ connector can enable a common resulting peripheral offset relative to the top surface for varying HPM thickness (example offset Z = 0.49)

Note, the host thickness examples shown are common at the time of this specification being published, however, alternate thicknesses may become common in the future.

Designers should consult with vendors of SFF-TA-1002 4C+ to determine best options for their chassis application.

Figure 14: Example of consistent peripheral top surface offset relative to HPM



HPM Thickness – t (mm [in])	Connector/Midplane Offset Required for Z = 0.49 (mm)
1.57mm [.062”]	-.49mm
1.93mm [.076“]	-.31mm
2.36mm [.093“]	-.095mm
2.55mm [.100”]	0mm
2.79mm [.110“]	+.12mm

10.4. Chassis-to-Board Bracket and Secondary Side Keep Outs

M-DNO board outlines have defined zero height secondary side keep outs driven by two key features:

1) Interoperability goals mean that larger HPMs (e.g. Type 3) could be placed in a chassis which also supports a smaller HPM (e.g. Type 2). In this instance, standoff hardware to support the smaller HPM could interfere with the larger HPM (which does not leverage all the same mid-board mounting locations). These zero-height secondary side keep outs prevent any interoperability interference.

2) M-DNO HPMs shall allow for a Chassis-to-Board Bracket (Board Pan) which enables different board layouts (and mounting hole locations) between HPM Types and Compute Core designs, while maintaining compatibility to a common chassis. An example Board Pan is shown in **Figure 15** (note**:** this example depicts an HPM defined in the M-FLW Specification).

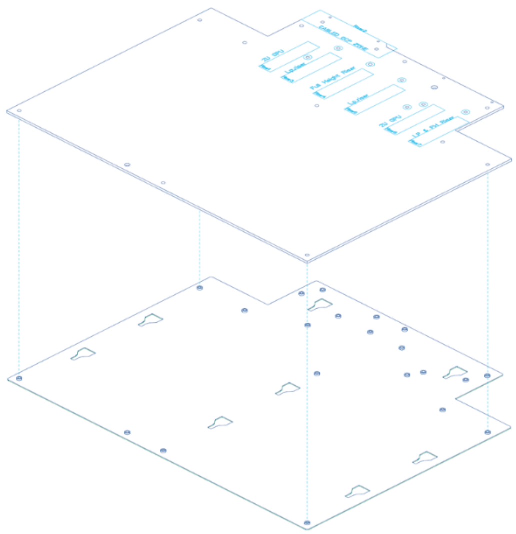
   M-DNO HPMs shall support required locations for chassis hook features that interface between the chassis base and the Chassis-to-Board Bracket. These hook locations require HPM secondary side zero-height keep out zones.

   A supporting chassis base must provide hook geometry to interface the cutouts on the Chassis to Board Bracket.

   The geometry of the Board Bracket is not specified.

Implementors Note: While most monolithic server designs benefit from a Board Pan it is NOT expected that all systems supporting M-DNO HPMs will require a Board Pan. Specifically, sled-based designs common in multi-node systems typically do not require a board pan.

Figure 15: Example of Chassis-to-Board Bracket (Board Pan)



The zero-height secondary side keep out zones reflecting both HPM Type interoperability and Board Pan support are defined in **Figure 16-Figure 19**. In addition to the zero-height secondary side keep out zones, **there is a universal secondary side component height restriction of 1.6mm** for all board types.

In some instances, an HPM or System designer may desire tall secondary side components (such as special capacitors) that **exceed** the 1.6mm Secondary Side height restriction. Although this should be avoided if possible, a designer may implement local exceptions if the following conditions can be met:

1. Exceptions are contained to small areas of the Secondary side, not to exceed $400mm^2$ area per instance.
2. No two instances of exception are closer than 10mm, as to not drive excess cutouts in Chassis-to-Board bracketry.
3. The Chassis-to-board bracketry can be cutout to accommodate the exception.
4. The HPM thickness + backside component shall never exceed 5.86mm.

Figure 16: Type 1 HPM Secondary Side Zero-Height Keep Out Zones

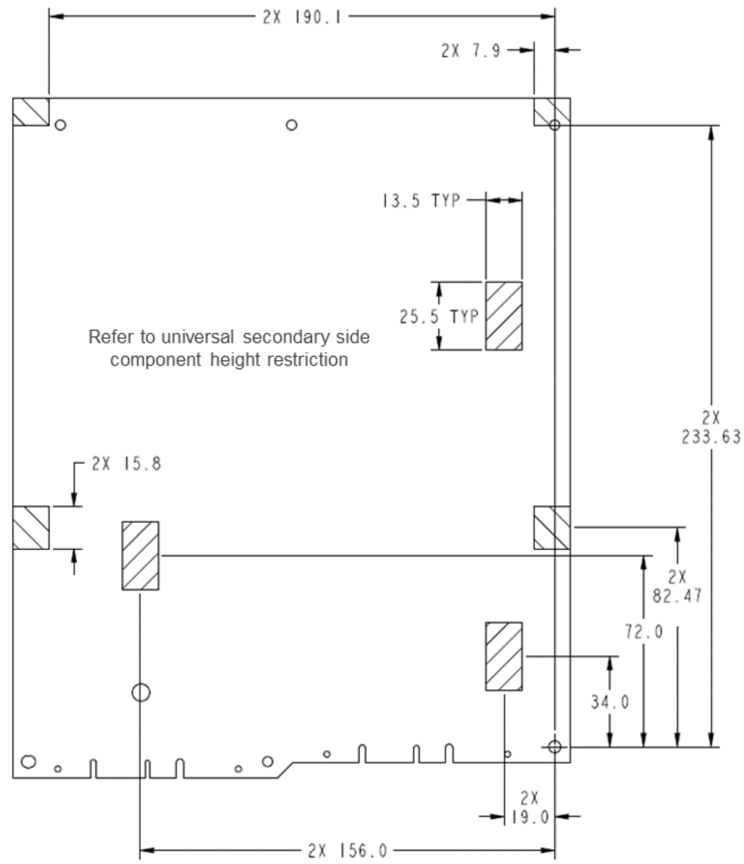
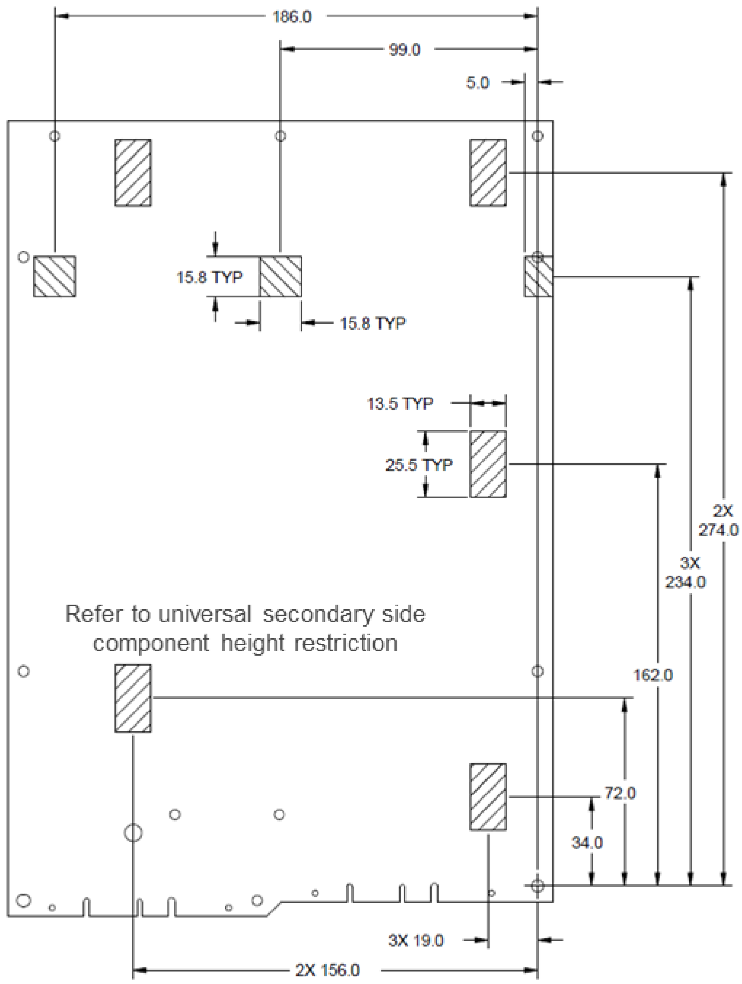


Figure 17: Type 2 HPM Secondary Side Zero-Height Keep Out Zones



ALL DIMENSIONED KOZ'S ARE ZERO HEIGHT RESTRICTION
REFER TO UNIVERSAL SECONDARY SIDE COMPONENT HEIGHT
RESTRICTION FOR MORE INFORMATION

585 ***Figure 18: Type 3 HPM Secondary Side Zero-Height Keep Out Zones***

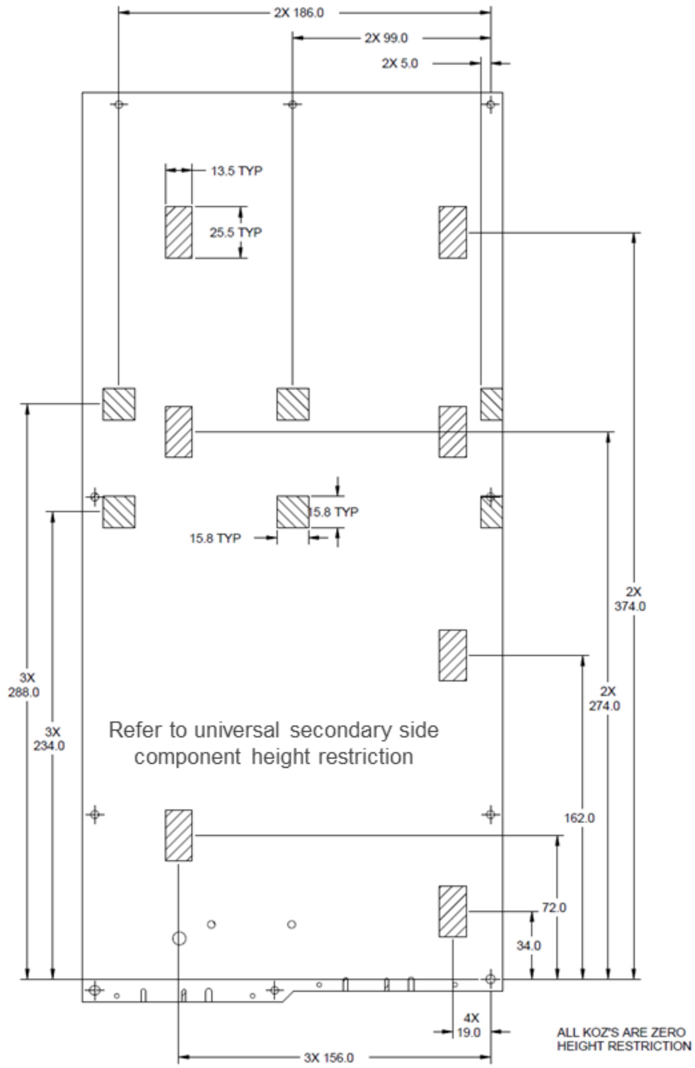
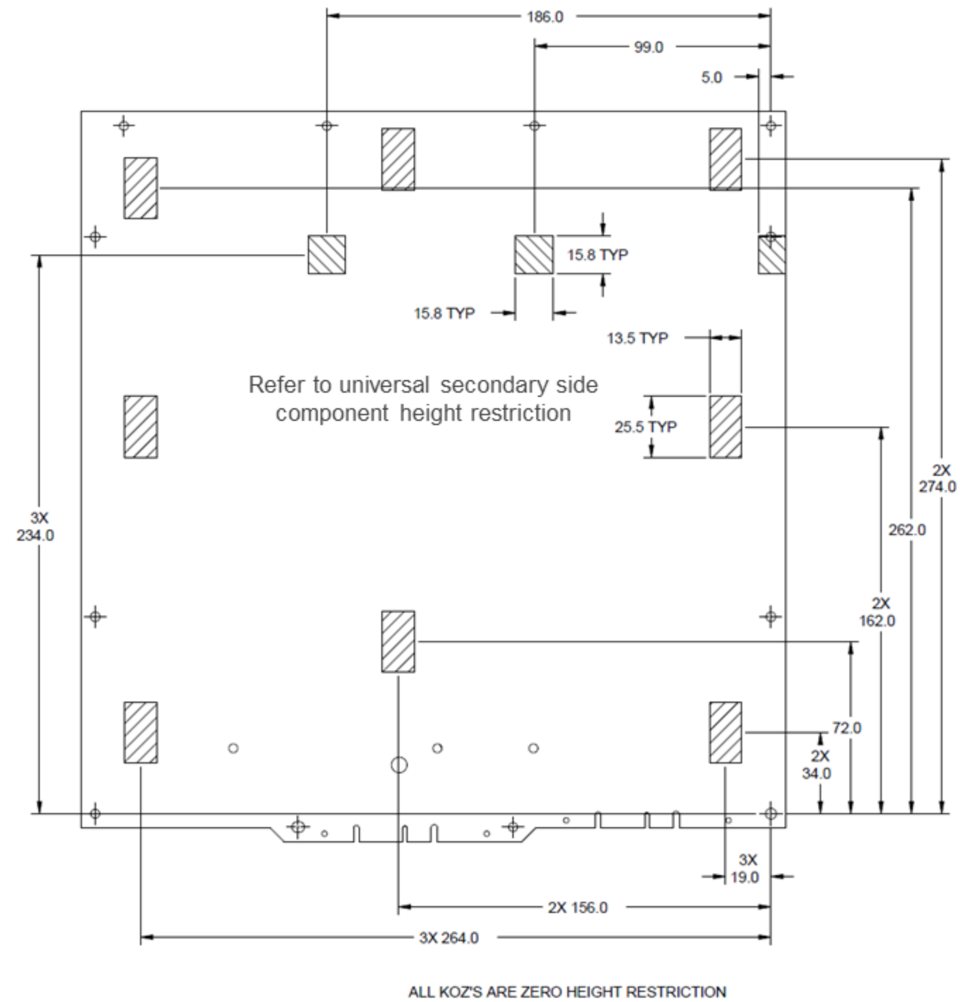
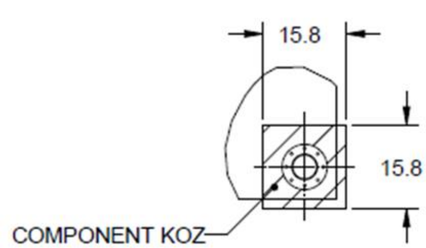


Figure 19: Type 4 HPM Secondary Side Zero-Height Keep Out Zones



590 Additionally, a recommended component KOZ for all mounting holes (including IO retention mounting holes) on all HPM types is provided in **Figure 20**.

Figure 20: Secondary Side Hole Component KOZ



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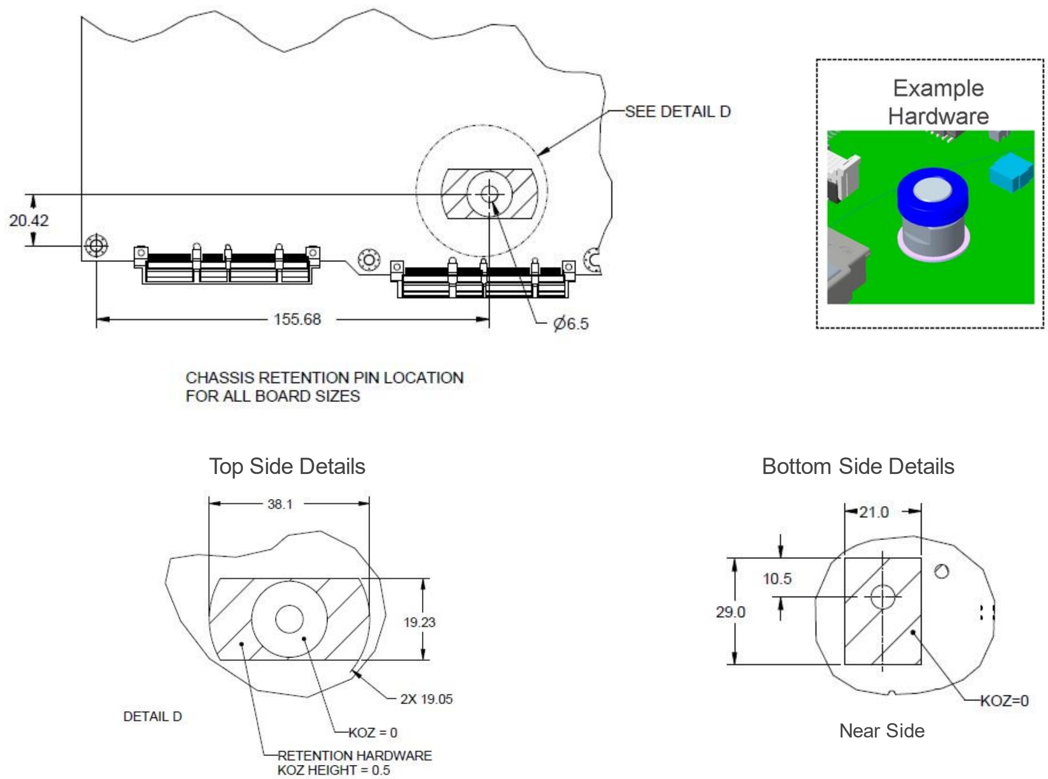
10.5. HPM to Chassis Retention Mounting

The HPM and Chassis-to-Board Bracket assembly requires retention to the chassis base. There shall be a hole required for motherboard retention to the chassis. The hole is sized for common retention methods such as plungers, thumbscrews, etc. Recommended Primary / Secondary side KOZs and height restrictions around this hole are also depicted in **Figure 21**.

Figure 21: HPM Assembly to Chassis Retention Enablement



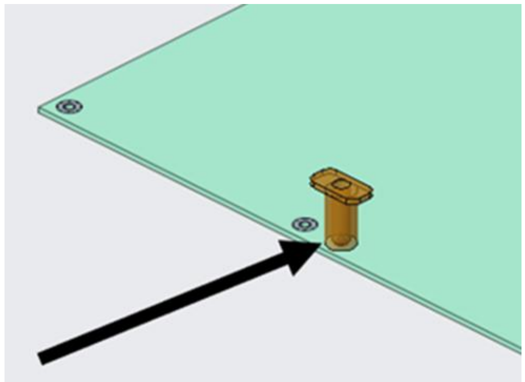
10.6. Board Handling

The HPMs shall implement a hole intended for a mechanical handle. This handle implementation is not specified, an example is shown in **Figure 22**.

The hole location shall be near the Far side edge of the Compute Core within the HPM. The specific location of the hole is not specified but should be placed considering Compute Core details, such as High-Speed IO cabling and Thermal solution keep outs.

Implementors Note: While the hole is required, HPM and / or System designers may choose to not utilize hardware in the hole location and instead provide alternate solutions to assist in board handling. As an example, if the hole location is not accessible when large thermal solutions are installed the designer may instead choose to provide a handling feature / touch point not tied to the HPM itself.

Figure 22: Example Board Handling Feature



10.7. Common Peripheral Location Requirements

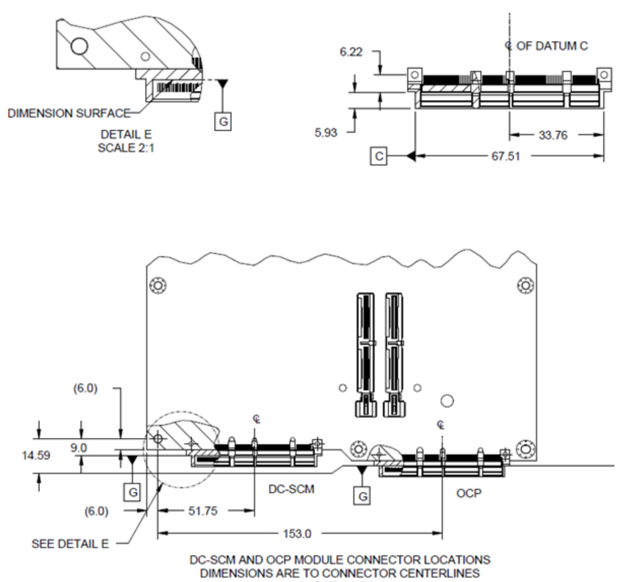
This specification defines fixed placement for certain peripheral connectors to maximize reuse across designs.

These fixed peripheral subsystem connectors are:

- OCP NIC 3.0
- DC-SCM 2.0

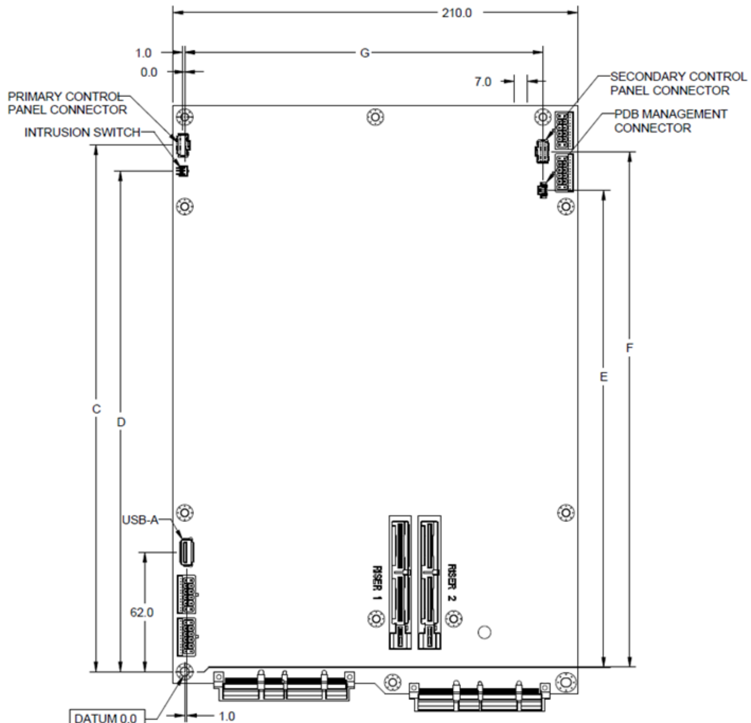
The location of each of the connectors is defined in **Figure 23**.

Figure 23: Locations of OCP NIC 3.0 and DC-SCM 2.0



10.8. Platform Infrastructure Connector Placement

Figure 24: Platform Infrastructure Connector Recommended Placements



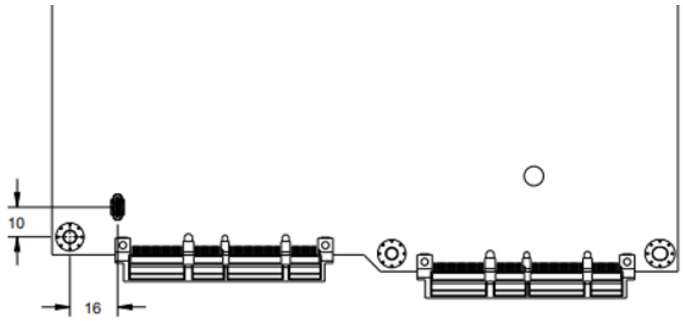
MISCELLANEOUS CONNECTORS					
	DIMENSION				
TYPE	C	D	E	F	G
1	224	210	200	220	186
2	274	260	250	270	186
3	425	410	400	431	186
4	274	260	250	270	270

Note: The M-DNO workgroup is currently investigating changes to the placement of the USB, PDB Management and Secondary control panel. Figures in this section have not been updated with the new PDB Management connector defined in M-PIC V0.75. We expect all connectors to eventually have a small placement Zone to move within as represented with the two zones in this draft Figure 26.

Figure 24 depicts the recommended location of the miscellaneous connectors defined in the M-PIC specification which are relevant to M-DNO HPMs. Additional information on these connectors is available in Section 12.2 – Section 12.6 in this document.

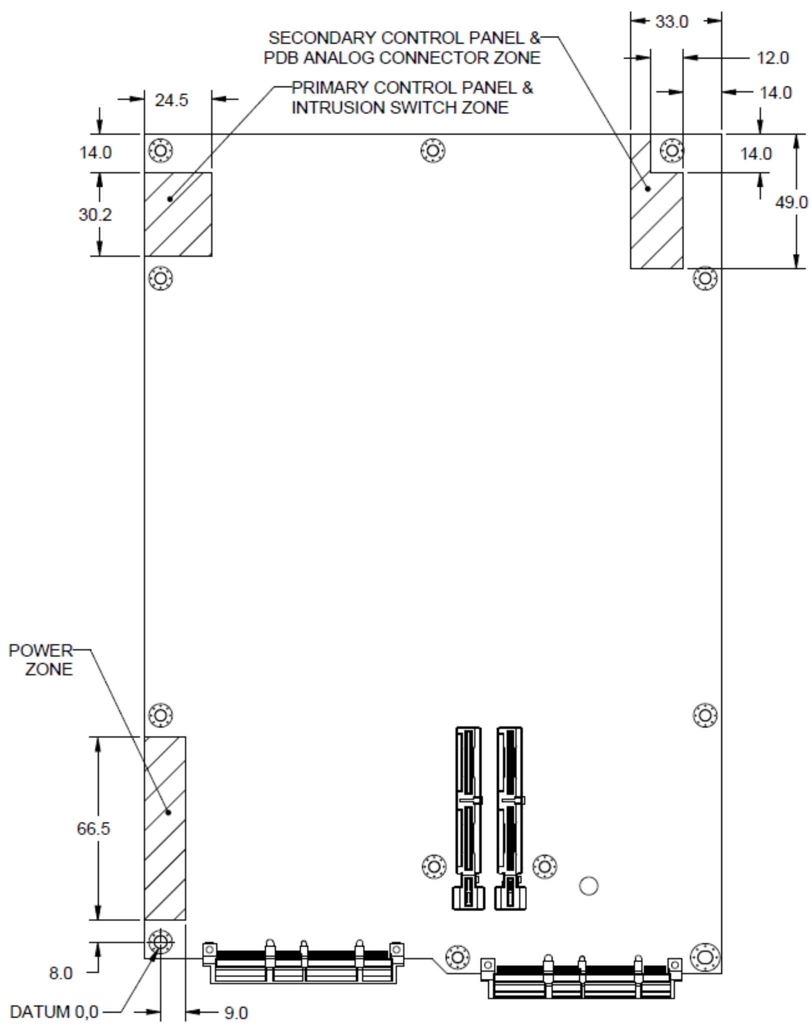
Note that a Type 2 board is represented but applicable dimensions are provided for all board types. These dimensions are intended to provide recommended connector locations that are consistent relative to the nearest board corner across all board types. The only exception to this philosophy is the USB location for Type 1 HPMs which is provided separately in **Figure 25**. Note that Type 1 depicts a USB-C style connector as type-A, while preferred, is expected to be challenging to fit.

Figure 25: Type 1 USB Location



To ease board layouts while maintaining interoperability, small placement zones are specified in **Figure 26** that connectors may move within if they cannot be placed in the recommended location. Placement of these connectors shall always be within the specified zone.

Figure 26: Platform Infrastructure Connector Placement Zones



10.9. Near IO Connector Placement

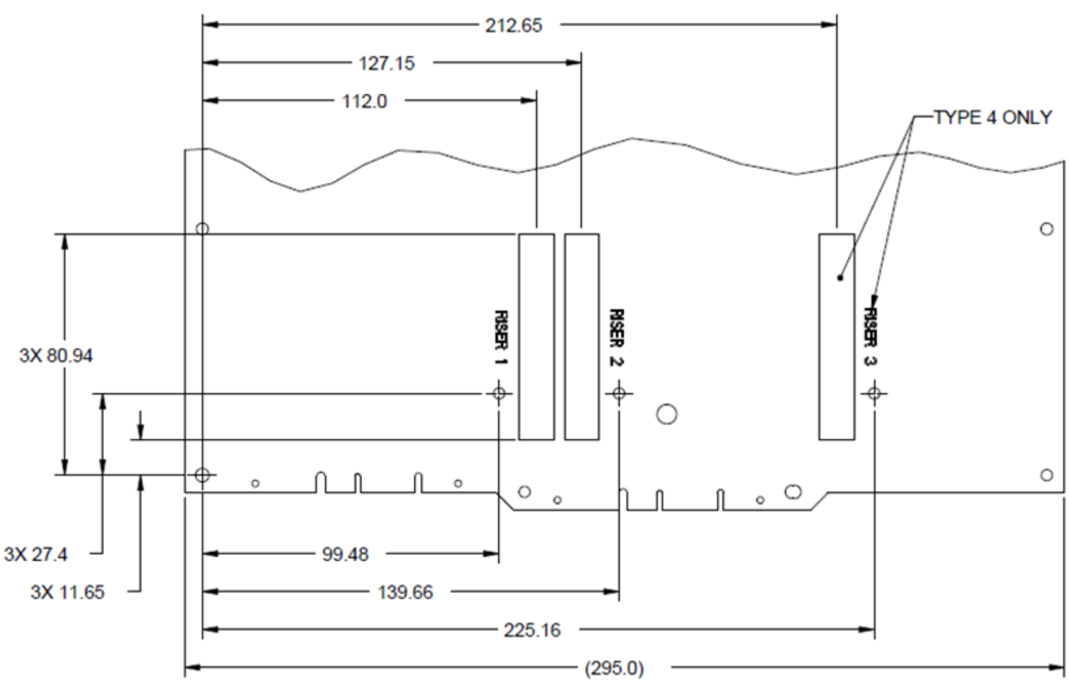
The M-DNO specification defines multiple HPM Type outlines which support different fixed riser configurations. In addition to any fixed riser implementation(s), cabled high speed I/O (HSIO) connectors may also be placed on the near side of the HPM.

10.9.1. Cabled Near IO Connectors

If cabled HSIO connectors are implemented, it is recommended to use the connector(s) defined in **Section 12.1** with signaling defined by the M-XIO specification.

10.9.2. Fixed Riser Connectors

Figure 27: Fixed Riser Location and Numbering



1. Three fixed riser locations are defined across the M-DNO HPM board Types as shown in **Figure 27**.
    a. The dimensioned locations represent riser connector keep in zones
2. Implementation of each riser location is **optional** across all M-DNO board Types.
3. M-DNO HPMs which implement fixed risers shall do so in any / all of the three specified locations.
4. **Each** fixed riser location is specified as follows (and summarized in **Table 3**):
    a. It is recommended that HPMs implement fixed risers using the connector described in **Section 12.1**.
    b. Connector locations are fixed horizontally (X – direction)
        i. The objective of this requirement is to enable Chassis and Riser Mechanical Reuse between generations of HPMs.
        ii. The dimensions indicate riser centerlines. If a chosen connector centerline is offset from the riser centerline, the designer shall adjust connector location to accomplish the Riser centerlines.

   c. Connector locations are fixed vertically (Y – direction)
      i. A keep in zone is specified to not restrict riser connector selection
      ii. Riser connectors shall fit within the specified keep in zone
      iii. The riser connector shall be oriented such that it touches the near edge within the keep in zone (11.65mm reference from datum)
   d. For information on power provided to Riser locations via the HPM refer to **Section 11.1.2**.
   e. Each riser has an associated retention hole as described in **Section 10.11**.
5. ½ Width M-DNO HPM Types (1/2/3) support two riser locations (Riser 1 and Riser 2)
   a. These locations are shown in **Figure 28** utilizing the recommended riser connector defined in **Section 12.1**.
6. ¾ Width M-DNO HPM Type 4 supports all riser locations (Riser 1, Riser 2, and Riser 3)
   a. These locations are shown in **Figure 29** utilizing the recommended riser connector defined in **Section 12.1**.

Table 3:Near IO Riser Attribute Requirements

Item	Fixed	Flexible Choice
Connector Choice		X
X-dimension location	X	
Y-dimension location	X	
Retention hole X-Y location	X	
Additional IO connector locations, beyond those specified		X

BOM Population Note:

Custom BOM Population choices are made at the discretion of a customer and are not covered by this specification. (This includes any depopulation choices for cost savings.)

Figure 28: PCIe Near IO Connector Locations (Type 1/2/3) (Riser Centerlines)

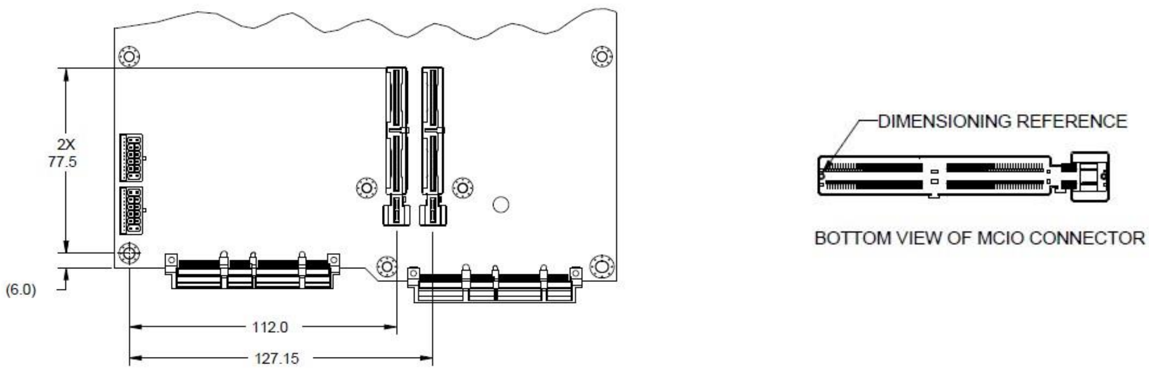
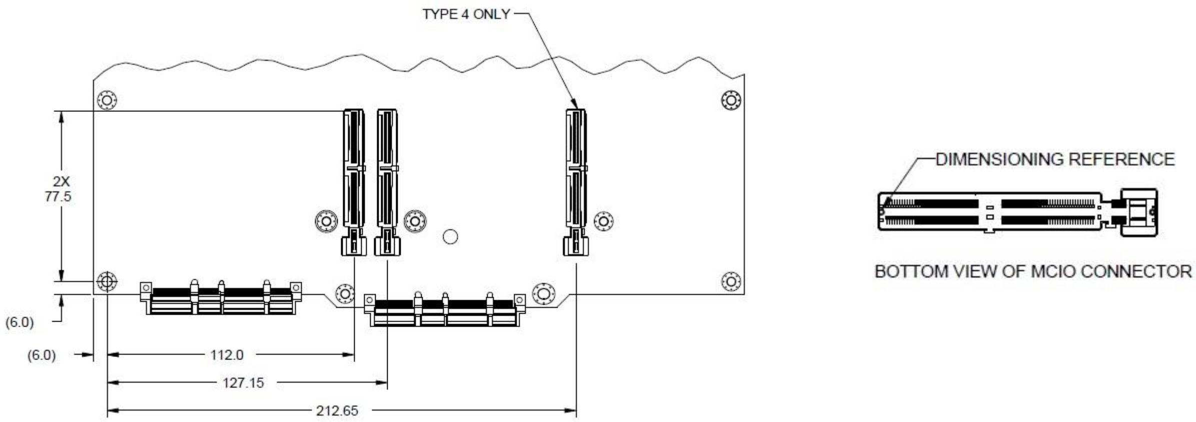


Figure 29:PCIe Near IO Connector Locations (Type 4) (Riser Centerlines)



Notes regarding **Figure 28** and **Figure 29**:

a) Reference connector choices as described in **Section 12.1**
b) All 'X' measurements are to connector slot/riser PCB centerline (regardless of chosen connector configuration)
c) 'Y' connector centerline is denoted with connectors in appropriate orientation (touching the near edge of the riser keep in zone)

10.10. Far Side IO Connector Placement

IO connector locations on the Far side of the HPM are not specified because they are all assumed to be cable-only connections and will not have major dependencies to chassis or subsystem reuse compatibility. The designer is free to choose/place these however they wish while respecting component height restrictions and other specified keep outs such as the Ingress / Egress power zone. It is recommended that high speed connectors placed on the Far Side leverage connector(s) described in **Section 12.1**.

10.11. Mounting Hole Requirements for IO Module Retention

Note: M-DNO workgroup is currently investigating changes to IO Module Retention hole locations to avoid potential conflicts with cable routing from riser connectors.

There are required holes associated with each Near IO fixed riser location **regardless of whether the riser connector is implemented**. The intent of requiring these holes is to always make retention holes available to system designers (including systems with cable based I/O).

These holes are intended to be used for mechanical module retention (such as PCIe Risers, or other modules that require mechanical retention in the HPM area). There is one associated hole per defined riser location as shown in **Figure 27**.

- The retention holes associated with Riser 1 and Riser 2 are required on all M-DNO HPMs
- The retention hole associated with Riser 3 is required on all M-DNO Type 4 HPMs

Hole dimensions follow standard mounting hole requirements as defined in Detail A of **Figure 8**.

Recommended KOZs around the holes are shown in **Figure 30**.

Chassis designers may choose the hardware and utilization method for riser retention. The hole location was selected to minimize impact of signal routing to the fixed riser locations as well as be accessible when cards are installed.

10.12. Primary Side Component Height Restrictions and KOZs

Note: M-DNO workgroup is currently investigating requirements and recommendations relative to Primary side component heights. This section is intended to provide directional guidance on current thinking – specific heights and Zone dimensions are under discussion and purposefully excluded from this draft.

All M-DNO board types shall adhere to a common approach of three different component height restriction zones as shown in **Figure 30**.

- Zone A is the most restrictive and is intended to allow for cabling while avoiding interference with PCIe CEM cards directly above the HPM and its peripherals.
- Zone B is intended to allow for extended heatsinks and other thermal solutions to extend towards the far side of the HPM while not prohibiting cabling of HSIO or other miscellaneous items (e.g. Control Panel).
- Zone C is the least restrictive to allow for areas where taller components (large capacitors, battery holders, etc.) may be placed. If the Near Ingress / Egress power zone is implemented, tall components may be placed in the area depicted, however, if any component exceeds the Zone A guidance it may restrict system I/O implementations (i.e. restrict Riser 1 to low profile CEM cards).

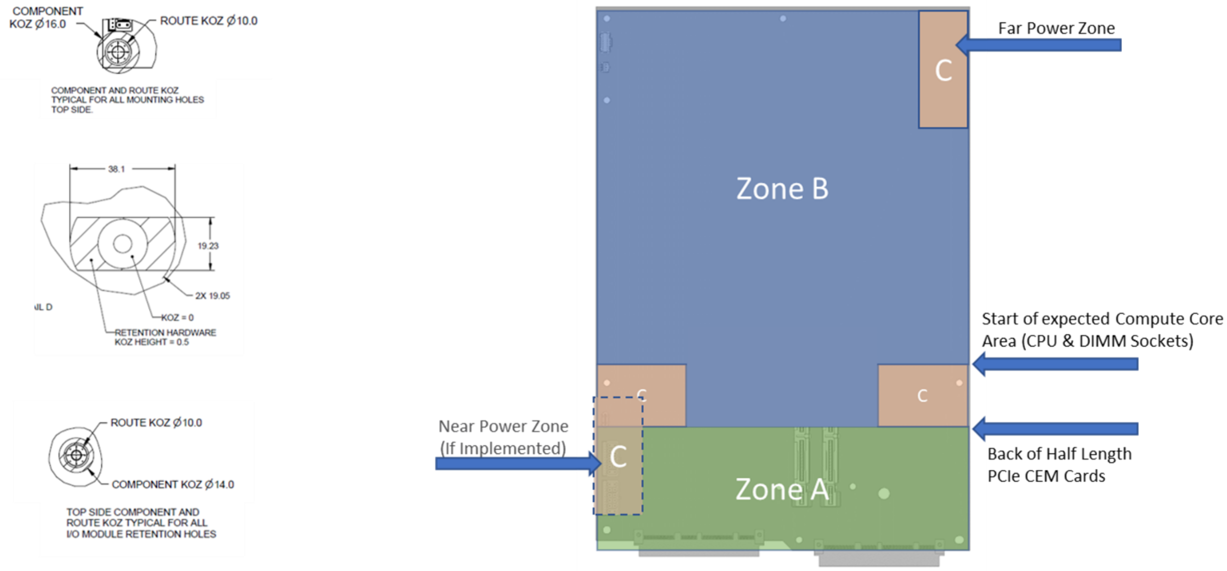
Zone height restrictions apply to soldered components only (and does not apply to heatsinks).

DIMM connectors can and will violate the Zone B restrictions.

Connectors not placed by this specification may violate these height restriction zones when mated, though HPM designers should do so with careful consideration of potential system use cases of their HPM.

Figure 30 also provides recommended component and route KOZs for all holes. Note that the component KOZ around IO Module Retention holes is different from other mounting holes. The component KOZ is intended to keep small components at risk of damage away from the hardware and assembly tools. If a component is larger than 10mm in any dimension (i.e. a DIMM connector), it is considered more robust, and may encroach on the Component KOZ's.

Figure 30: Primary Side Component Height Restriction Zones

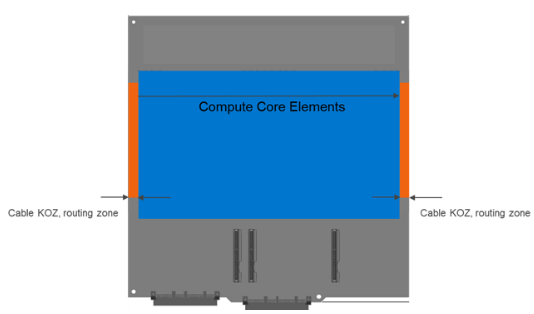


10.13. Cabling Enablement Keep Out Zones

This specification does not specify a specific Keep Out Zone for cable enablement.

When defining HPM features such as mounting hole locations and board pan keep outs, it was assumed that most HPM designs would center the Compute Core allowing for cables to be routed on either edge of the HPM in any remaining space. However, offset Compute Cores are not prohibited.

Figure 31: Example Type 4 Cable KOZ Layout



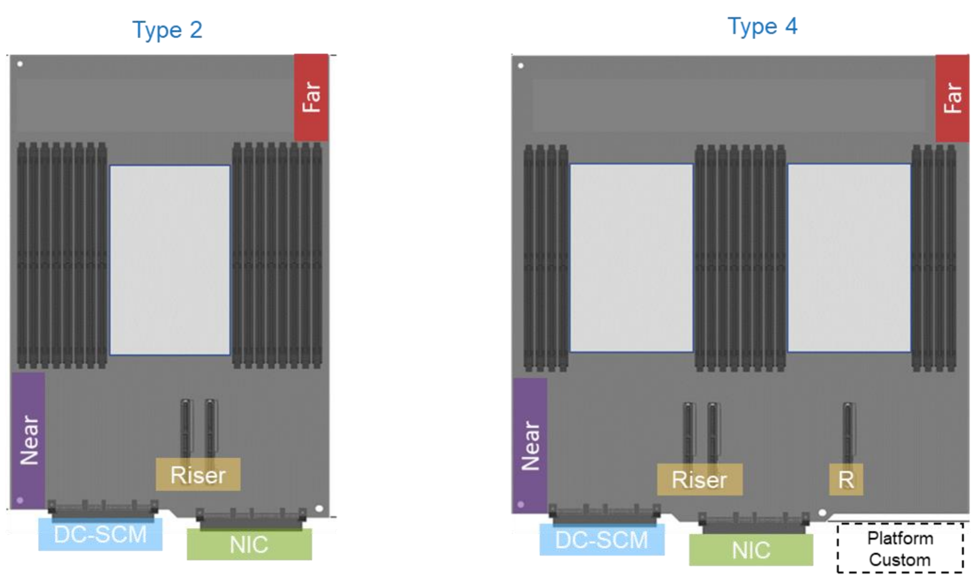
11. Power

M-DNO compliant HPMs are assumed to be powered from 12V DC. While alternate voltages are under consideration (e.g. 48V DC implementations), this specification assumes the burden for alternate power sources is placed on the system power delivery infrastructure (PDB, bus bar, etc.). For information on Power Management (including Power Gating) refer to the M-PIC specification.

11.1. HPM Power Zones

To enable a variety of system power configurations (See **Section 14**) there are two defined bi-directional power zones for each HPM type referred to as the “Near” and “Far” Ingress / Egress zones as shown in **Figure 32**. These zones are intentionally placed in opposing corners of the HPM to maximize flexibility of system orientation. Connectors placed within the Near and Far zone adhere to the “2x6 + 12 SB PICPWR” definition within the M-PIC specification and are always defined as bi-directional such that they may be used to provide power to the HPM (Ingress) or to power downstream subsystems (Egress) from the HPM. Additional power zones include power egress to DC-SCM, OCP NIC and each fixed board to board Riser location.

Figure 32: M-DNO Power Zone Overview (Type 2 and 4 Depicted)



11.1.1. Near and Far Bi-Directional (Ingress / Egress) Power Zones

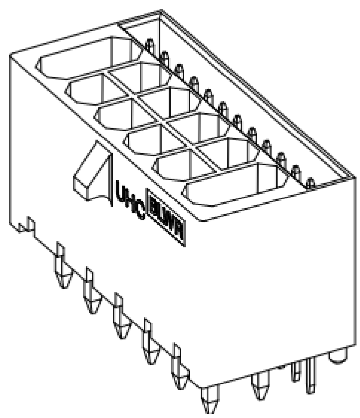
Ingress / Egress Cabled Power Connector

- **Power Connector Type**: 2x6+12SB PICPWR Vertical or Right-Angle required. Refer to M-PIC Specification for additional details.
- **Connector Power Rating**: 864W
- **Typical usage**: Power ingress to HPM and / or egress to peripheral subsystems

It is assumed that most systems will provide power to M-DNO based HPMs via a cabled solution from a Power Distribution Board (PDB). To maximize reuse of power delivery across all M-DNO HPMs the required connector for all cabled Ingress / Egress power is the 2x6 + 12S Bellwether UHC as depicted in **Figure 33**.

Each connector provides 864W of sustained power as well as 12 sideband signals enabling two sets of M-PIC PICPWR signals. When used for power Ingress this enables a single connector to interface with a power distribution board and when used for power egress this enables a single connector to fan out to two downstream subsystems. Refer to the M-PIC specification for more information on PICPWR compliant connectors.

Figure 33: Bellwether UHC 2x6 + 12SB PICPWR Connector (Vertical)



Far Power Zone

The Far Power Zone includes **required** connector location(s) such that any system capable of providing power to the Far Zone of the HPM can power all M-DNO designs. While it is required for the HPM to implement these connectors they may be depopulated in certain system configurations.

Two connector locations are defined for each board type in the Far Power Zone. Refer to **Section 11.1.6** for specific locations per board Type.

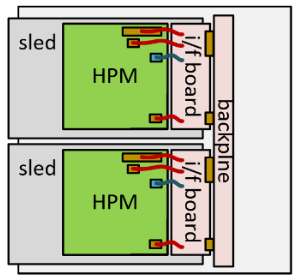
For Type 1 and 2 HPMs only a single Far connector is required to be implemented while implementation of a second connector is optional based on HPM power requirements. HPM designers electing to implement only a single connector may choose between either of the two specified locations.

For Type 3 and 4 HPMs, both far connector locations are required to be implemented.

While it is expected that many systems will implement the required connector and provide power via cable(s), another M-DNO use case involves blind mating HPM “sleds” into multi-node chassis infrastructure. HPMs intended exclusively for these use cases may deviate from the requirements above and choose to adapt a blind mate / board to board style connector along the far edge of the board. No specific connector is defined for these applications.

Implementors Note: HPMs which implement the cabled Bellwether UHC connector may still be used in multi-node systems via an interposer or interface board. Refer to **Section 13** for an example of such a system.

Figure 34:M-DNO HPM with multimode interface board



Near Power Zone

Due to the expected density of HPM designs in this area of the board the Near Power Zone **may** be implemented at the discretion of the HPM designer.

To increase the likelihood that this zone can be implemented, connectors may be placed anywhere within the designated zone area rather than having a fixed location. Refer to **Section 11.1.6** for this zone outline.

If Near zone power connectors are implemented, they are not required to be populated in all system configurations.

The near power zone does not allow for blind mate / board to board style connector adaptation.

Implementors Note: It is recommended that when the Near Power Zone is implemented that the connector count (1 or 2) matches the connector count in the Far Power Zone. This configuration enables peak flexibility for Power Ingress / egress to / from the HPM.

11.1.2. Fixed I/O Riser Location Power

- **Power Connector Type**: Amphenol G03V213X2HR Recommended
  Refer to M-PIC Specification for additional details.
- **Connector Power Rating**: 180W
- **Minimum Power Delivered to Connector by HPM**: 87W
- **Typical usage**: Power egress for 1 (required) or 2 (optional) 75W PCIe CEM Devices per Riser

For each **implemented** fixed riser location (up to three):

- DNO HPMs are required to deliver a minimum of 87W of power to the riser connector. This requirement is defined to guarantee each riser location can support a minimum of one 75W PCIe CEM card and minimize power cabling requirements in dense systems.

- HPMs may choose to deliver additional power to the riser connector to enable a second 75W PCIe CEM card at each riser location or assume additional power is provided by system infrastructure (e.g. cable from PDB).

- Additional supplemental I/O power (e.g. for a high powered GPU) is not defined and is assumed to be provided directly by system infrastructure (e.g. cable from PDB).

- I/O Risers must comply with M-PIC PICPWR sideband signaling requirements.

- Additional power must be delivered to each riser beyond PCIe CEM 5.0 specification to budget for miscellaneous logic on risers and VR conversion losses. See **Table 4** for calculation of 87W effective total power required per slot.

Table 4. Minimum HPM Power Provided to Fixed Riser Locations

Power Rail	**75 W Slot**[1]
+3.3Vaux	Generated on PCIe riser. Derived from +12V
+3.3V **(**V_{cc3_3}**)**	Generated on PCIe riser. Derived from +12V
+12V Voltage Current	 12V nominal 7.25A total: 5.5 A (CEM 5.0) + 1.0A (VR conversion to V_{cc3_3}) + 0.35A (VR conversion to +3.3Vaux) + 0.40A (misc.)

11.1.3. DC-SCM 2.0

- **Power Connector Type**: See OCP DC-SCM 2.0 specification (Refer to **Section 6**)
- **Connector Power Rating**: 50W
- **Typical usage**: Power egress for DC-SCM 2.0

11.1.4. OCP NIC 3.0

- **Power Connector Type**: See OCP NIC 3.0 spec (Refer to **Section 6**)
- **Connector Power Rating**: 80W
- **Typical usage**: Power egress for OCP NIC 3.0

11.1.5. Platform Custom Zone (Type 4 Only)

Power to the Platform Custom Zone is not defined as it is considered implementation specific.

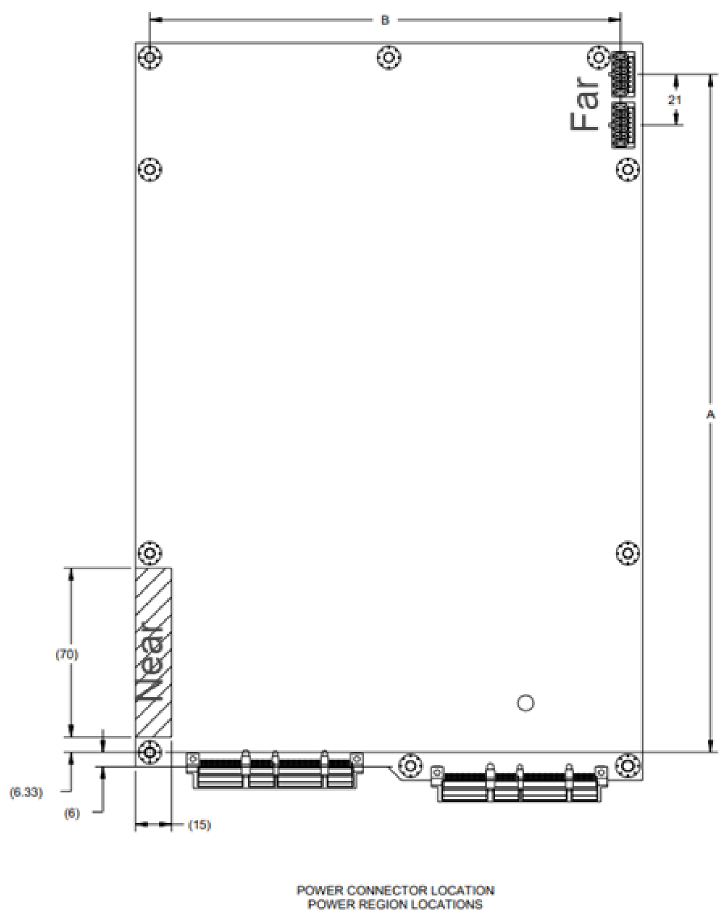
11.1.6. Ingress / Egress Power Connector Locations

Figure 35 denotes the locations of the bidirectional Near and Far power ingress / egress connectors.

As described in **Section 11.1** the two Far power connector locations are fixed for each board type with common spacing between the two locations across all board types. Refer to the drawing and table within **Figure 35** for the fixed location for each board type. Note that while for simplicity only a Type 2 board is depicted the dimensions listed are valid for other board types.

If implemented, Near connectors may be placed anywhere within the depicted zone which is common across all board types (including Type 1).

Figure 35: Near and Far Power Zone Connector Locations



	DIMENSION	
TYPE	A	B
1	231	195
2	281	195
3	431	195
4	281	280

11.2. HPM Power Planes

The HPM power planes have the following features

- At maximum load, the HPM power shapes temperatures have a maximum of 30ºC T-rise and do not exceed 100ºC absolute
- At maximum load, the maximum HPM voltage drop (IR loss) between primary power ingress connectors and associated loads or egress connectors is less than or equal to 1%
- It is not expected that all loads/connectors on the HPM will be operating at maximum power concurrently. However, it is recommended that, minimally, the power distribution be designed to allow any single load/connector to operate at max power rating.

12. I/O System (Electrical Interfaces)

The HPM shall be required to implement electrical interfaces that must be in compliance with the DC-MHS family of specifications. Refer to **Section 6** for additional details.

This section provides additional guidance for specific connectors on M-DNO HPMs.

12.1. High Speed IO (HSIO) Connectors

HSIO connector selections are strongly suggested, but not required for compliance. Use of the suggested HSIO connectors will ensure broader compatibility with chassis, riser, and cable interfaces in the future. The selection is intentionally not stated as "required" so the specification allows for future selection of new connector technologies, as may be required by IO speeds and bandwidth changes in future generations of HPM.

Requirement: Connector Choices must be compliant with M-XIO specification.

Table 5: M-DNO Connector Recommendations

	Recommended Connector	Note
Fixed Riser	Amphenol G03V213X2HR	Compatible with 1016 cabled solutions
Near HSIO	SFF-TA-1016	Common interconnect for cabled connections and Riser solutions
Far HSIO	SFF – TA – 1026	Appropriate due to low profile and ability to fit under thermal solutions

The Near HSIO location and flexibility is further described in **Section 10.9**.

12.2. Internal USB

- **M-PIC Section Reference:** "Internal USB3 Connector"
- **Connector Requirement:** Required (may be de-populated)
- **Connector Placement:** Specified
- **Connector:** Refer to the DC-MHS M-PIC Specification

Electrical implementation for an internal USB3 connector follows the M-PIC specification. It is strongly recommended that HPMs implement a Type A connector. For M-DNO HPMs the connector shall be placed as defined in **Section 10.7**.

12.3. Intrusion Switch

- **M-PIC Section Reference:** "Intrusion Switch"
- **Connector Requirement:** Required (may be de-populated)
- **Connector Placement:** Fixed Location
- **Connector:** Refer to the DC-MHS M-PIC Specification

Electrical implementation for the intrusion switch follows the M-PIC specification. For M-DNO HPMs the connector shall be placed at the location defined in **Section 10.7**.

12.4. Boot Storage Peripheral

- **M-PIC Section Reference:** "Boot Storage Peripheral"
- **Connector Requirement:** Recommended
- **Connector Placement:** TBD
- **Connector:** Refer to the DC-MHS M-PIC Specification

Electrical implementation for the boot storage peripheral follows the M-PIC specification. For M-DNO HPMs the connector placement is TBD.

12.5. Control Panel

- **M-PIC Section Reference:** "Control Panel Interfacing"
- **Connector Requirement:** Primary: Required (may be de-populated), Secondary: Optional
- **Connector Placement:** Fixed Location
- **Connector:** Refer to the DC-MHS M-PIC Specification

Electrical implementation for the Control Panel(s) follows the M-PIC specification. For M-DNO HPMs the Primary Control Panel is required while the Secondary Control Panel is optional, the location of both control panel connectors is defined in **Section 10.7**.

12.6. PDB Management Connector

- **M-PIC Section Reference:** "PDB Management Connector"
- **Connector Requirement:** Required (may be de-populated)
- **Connector Placement:** Fixed Location (optional secondary placement)
- **Connector:** Refer to the DC-MHS M-PIC Specification

Electrical implementation for the PDB Management Connector follows the M-PIC specification. For M-DNO HPMs implementation of this connector within the Far Ingress / Egress Power Zone is required as defined in **Section 10.7**. Additionally, it is recommended that M-DNO HPMs which implement the Near Ingress / Egress Power Zone provide a BOM population option for a PDB Management Connector within or directly adjacent to the Near Ingress / Egress Power Zone.

Implementors Note: It is recommended that if the Near Power Zone is implemented that the HPM provide an additional option for the PDB Management Connector to be populated in the Near Power Zone. Care should be taken in providing a BOM population option which minimizes trace stub between the two connector locations due to the analog signals on this connector.

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13. Supplemental Material: M-DNO Conceptual Implementation Examples

The M-DNO specification has multiple form factor types to address various product types and sizes. In this section some of the possible configurations and usages for the different Types will be shown.

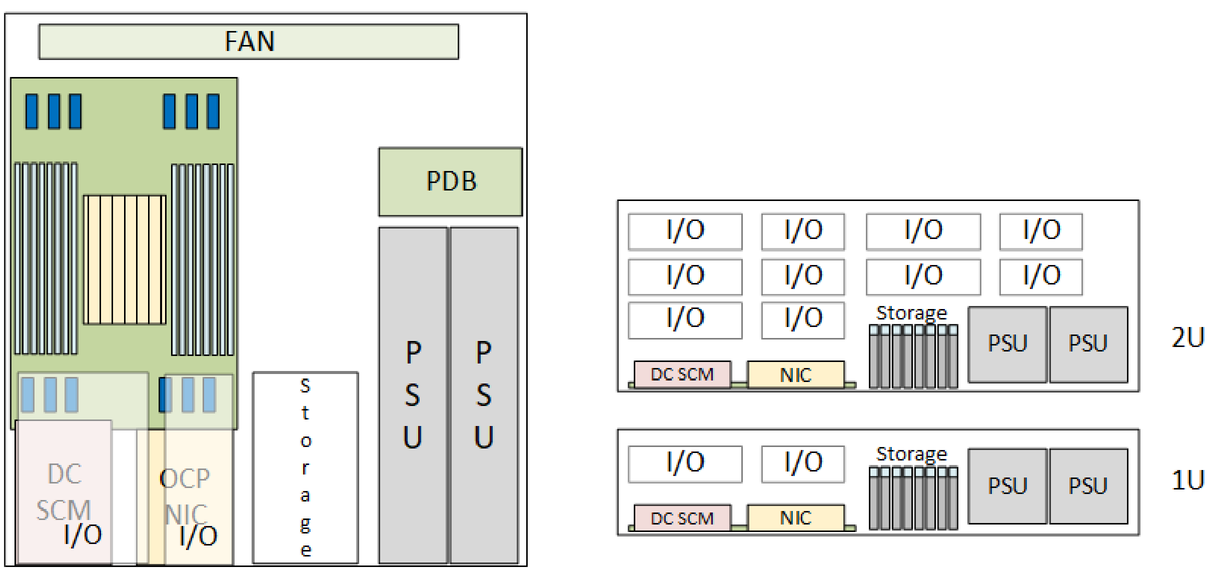
Note: Image representation of elements may not be to scale, and is subject to change

It is understood that the configurations shown represents a small sample of what could be possible. This section also conveys the reasoning behind the different sizes of HPM associated with the four types.

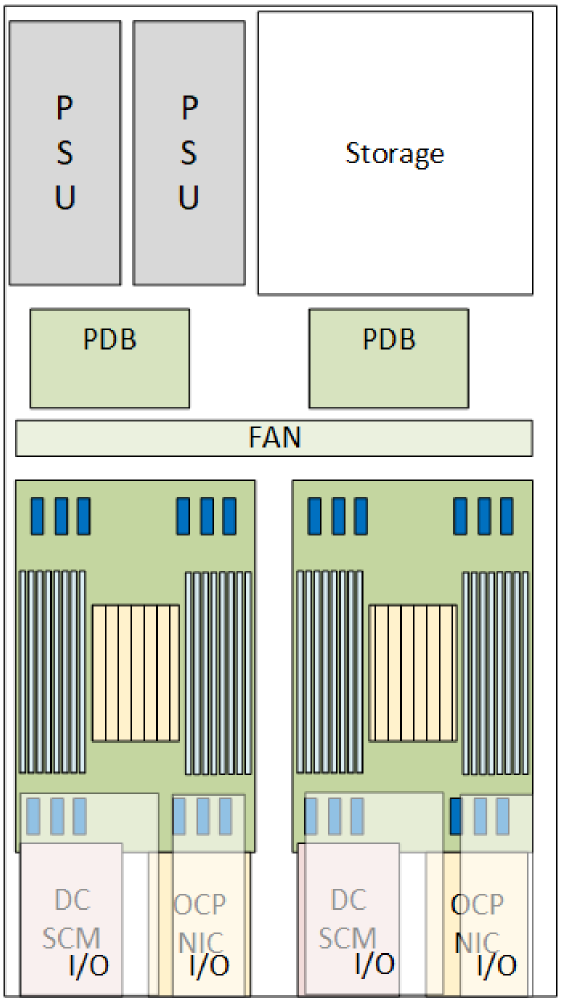
Type 1

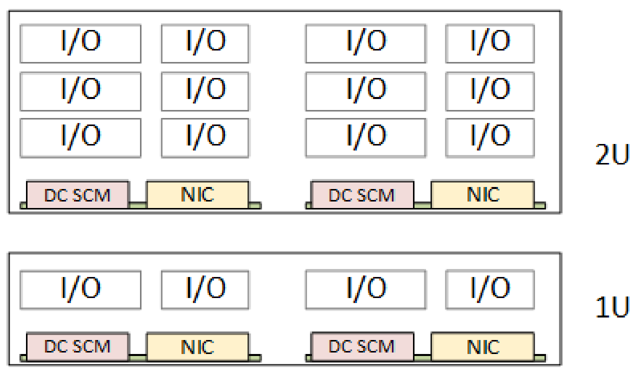
The application for Type 1 is the densest product size, that would be able to trade-off PCIe lane access and CPU cooling for the smallest size. Type 1 designs are intended to accommodate ~430mm overall product depth. These products are typically target for EDGE applications and mounting, where I/O, Storage, and Power are all accessed from the same end of the chassis. Type 1 designs are also optimized for embedded systems leveraging smaller core compute elements such as SOCs and FPGAs.

Type 1 configuration example – 1 Node



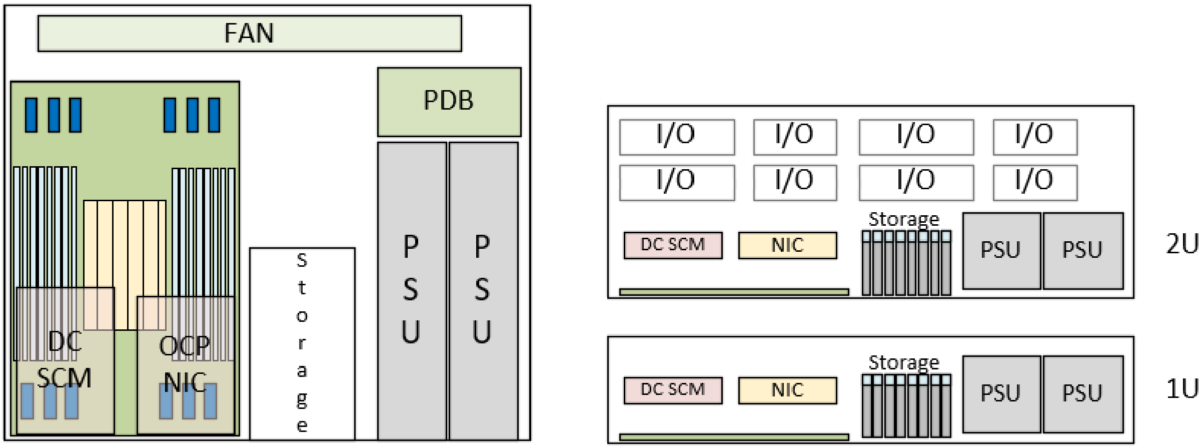
Type 1 Configuration Example – 2 Node





Type 1 designs are also the most likely to locate the DCSCM and NIC elsewhere in the design (via cable) or to no-pop them entirely and potentially leverage the connectors only. An example Type 1 system layout is shown below that enables 300-350mm chassis solutions

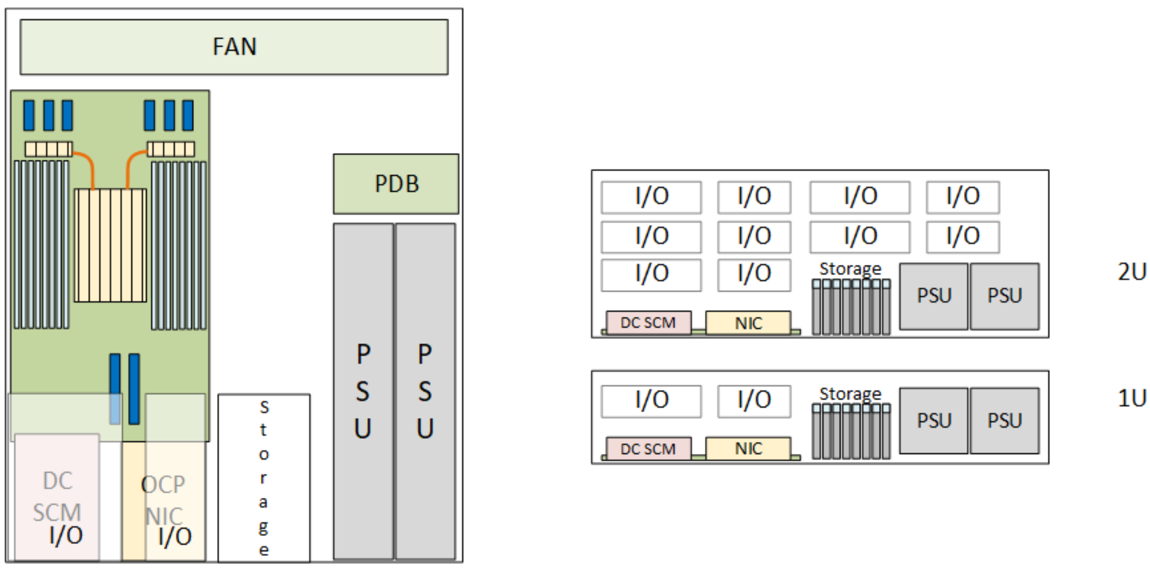
Type 1 Configuration Example – Short Chassis



Type 2

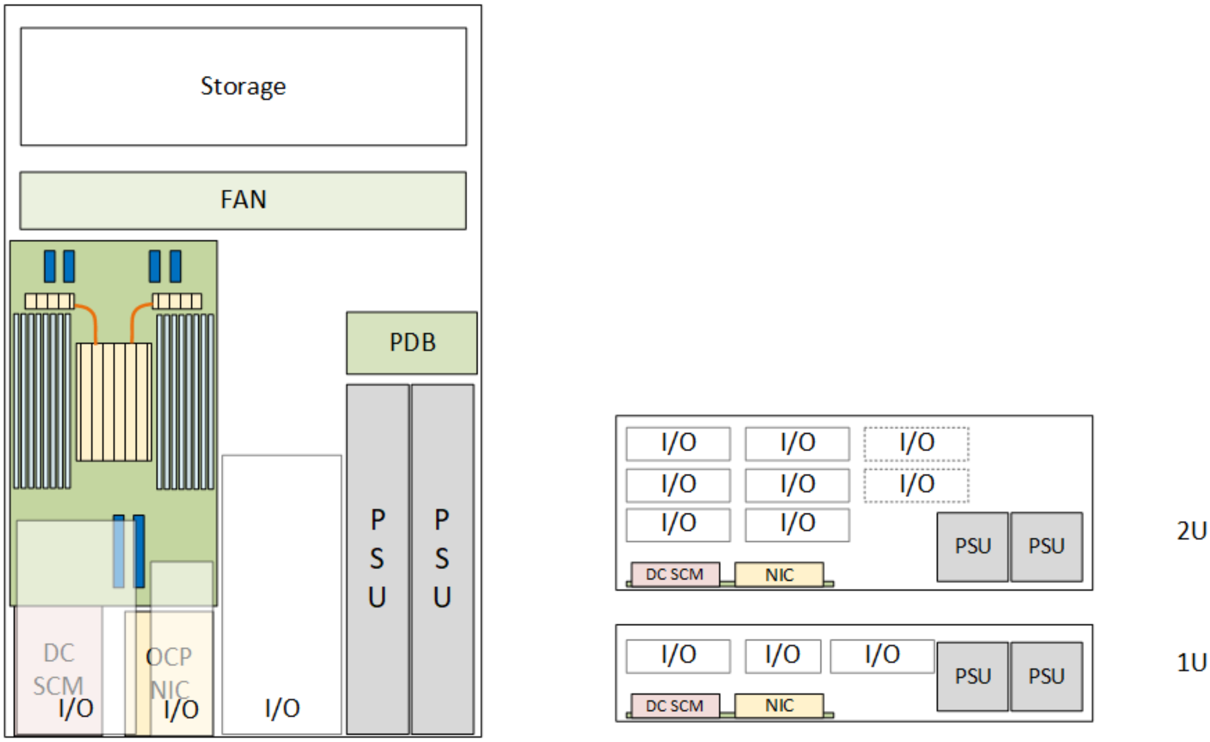
The Type 2 HPM increases the depth and maintains the same board width as Type 1. The increase in depth is done to support PCIe direct attach risers and EVAC thermal solutions as well as larger CPU sockets.

Type 2 Configuration Example – 1 Node Edge



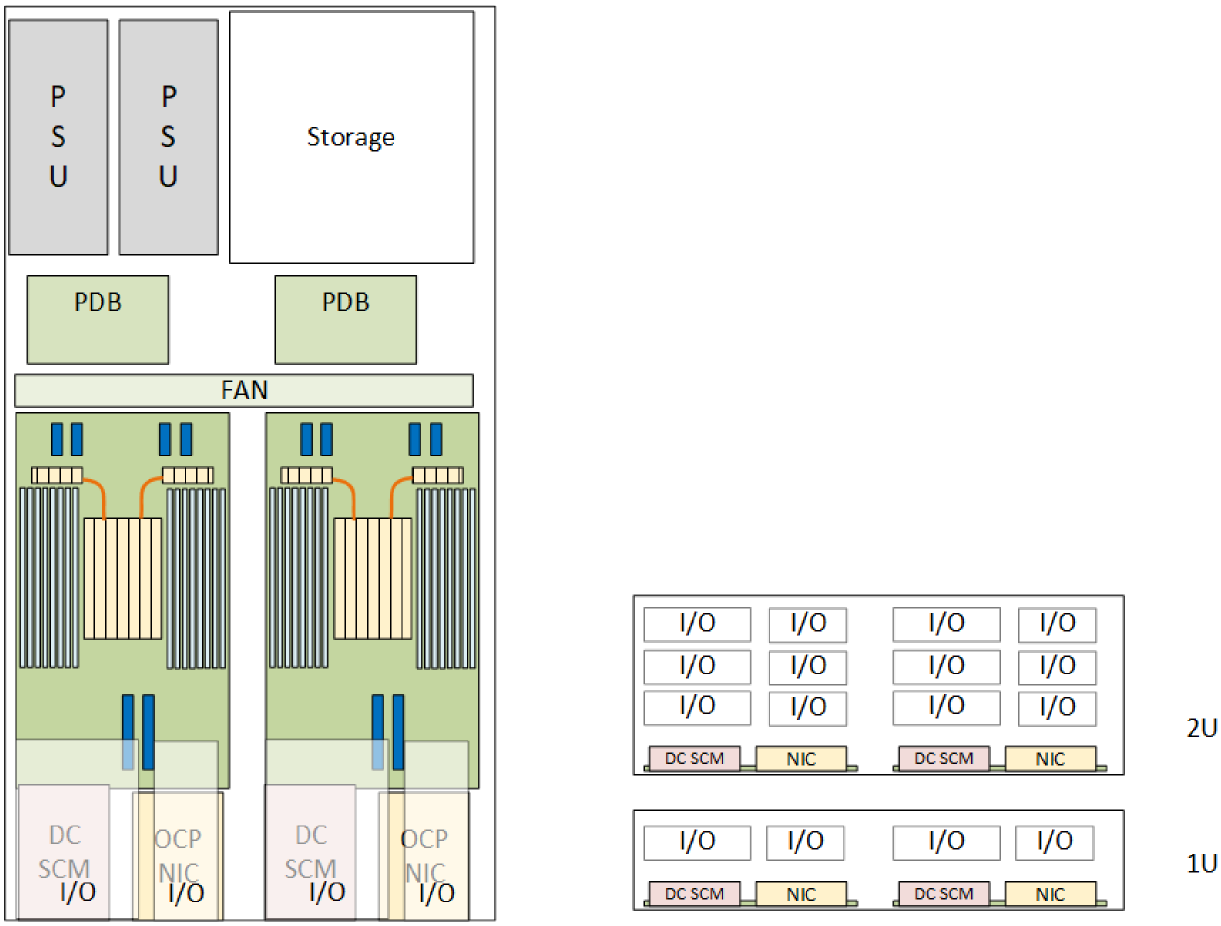
The Type 2 HPM would also be applicable for traditional enterprise server applications in or 1U or 2U heights. The variability of capabilities for I/O and Storage would be plentiful and facilitated by different riser, cable, and mid-plane configurations.

Type 2 Configuration Example – Enterprise Server



The Type 2 HPM would also be suitable for 2 Node products.

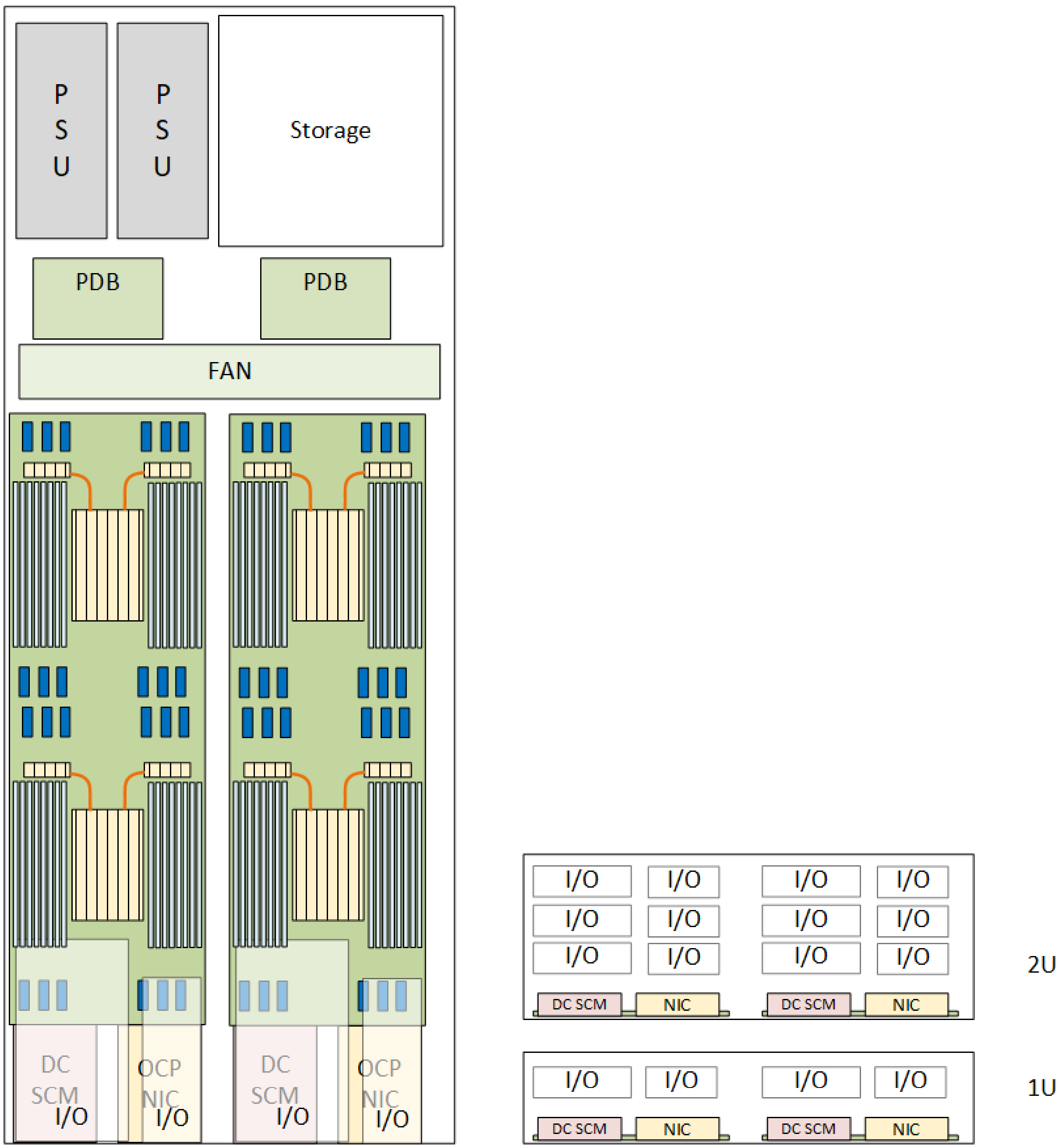
Type 2 Configuration Example – 2 Node



Type 3

The Type 3 HPM grows in depth to allow 2 socket “shadow core” designs, specifically to support 2 Nodes across a chassis. In this configuration the ability to utilize the full PCIe resources is de-prioritized. The ability to support EVAC thermal solutions would be applicable.

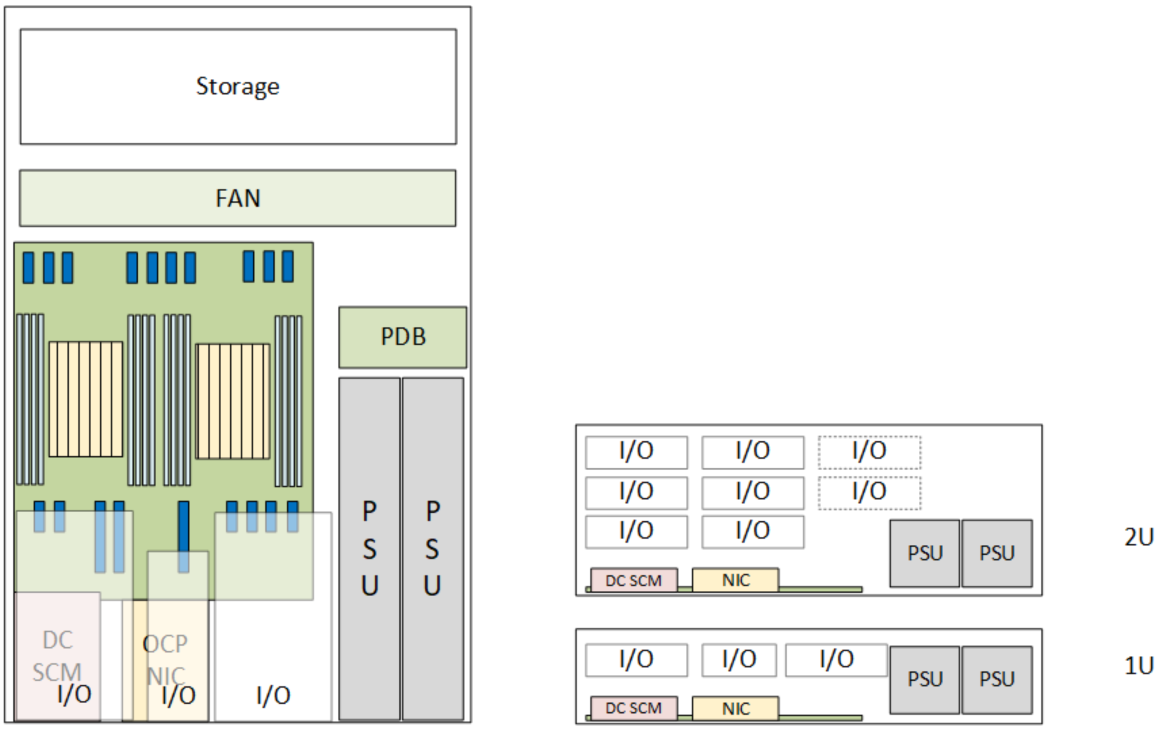
Type 3 Configuration Example – 4 Node



Type 4

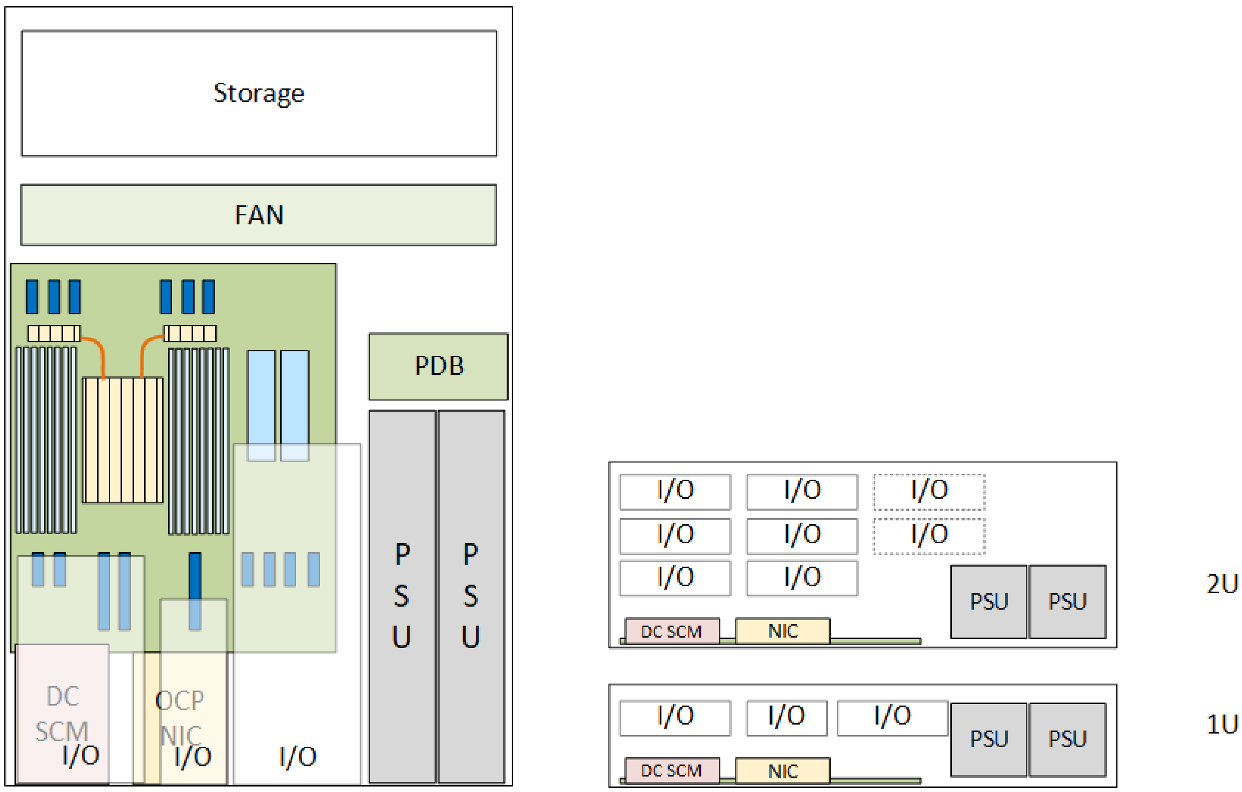
The Type 4 HPM is the only Type to grow in width. The primary driver for the Type 4 form factor is ability to support a dual socket "spread core" 2 Node product with adjacent PSUs in a 19" (or larger) rack. To achieve this 2 socket design a concession is made on memory socket support so that only one DIMM per channel is expected on a 8 channel per socket architecture. The other features intended to be supported on a Type 4 HPM would be full PCIe lane count, and EVAC thermal solutions.

Type 4 Configuration Example – 2 Socket Spread Core



Another possible Type 4 HPM would be a 8 memory channel CPU with 2 DIMMS per channel as in Type 2, but with more on board peripherals than the other ½ width Types.

Type 4 Configuration Example – Expanded Features 1 Node



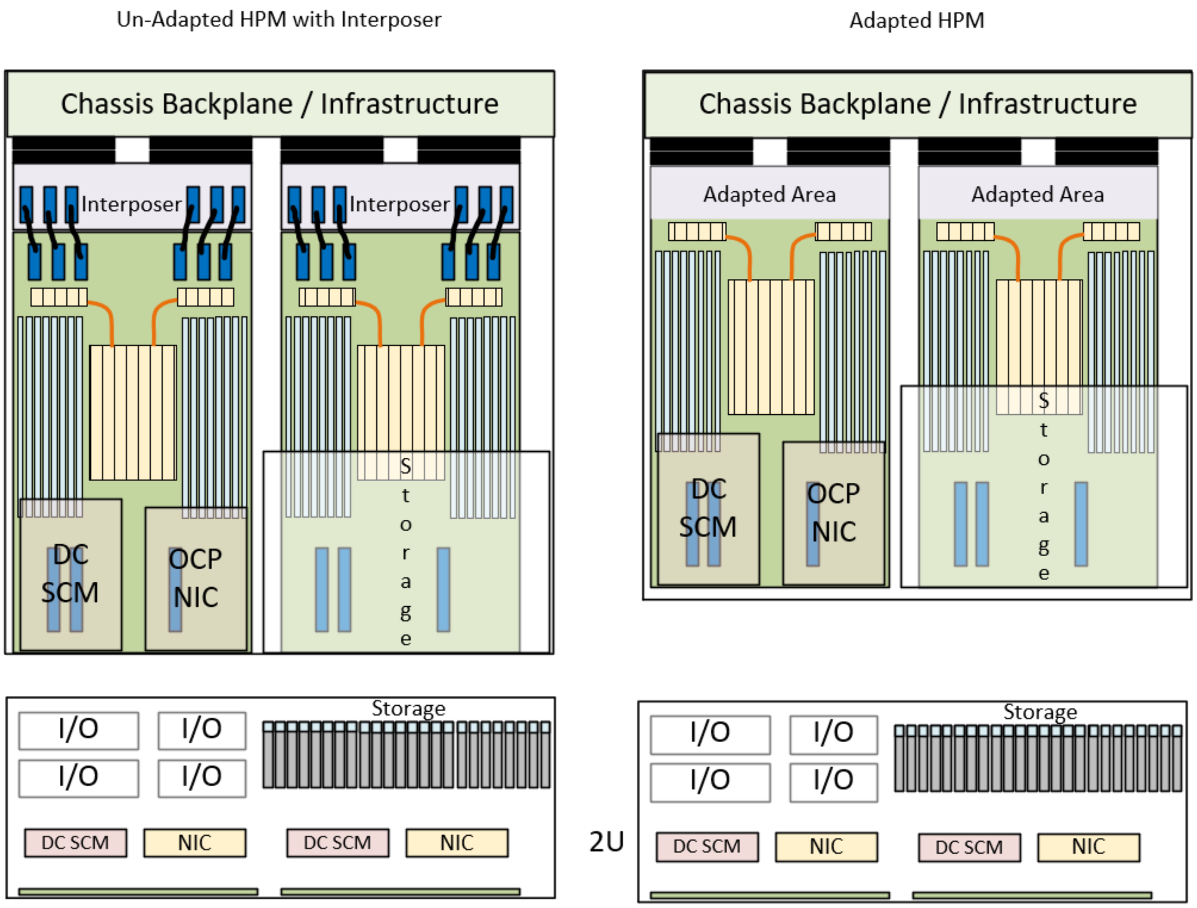
Multi-Node Specific

Multi-Node Adaptation

As described in the Power Zone **Section 11.1,** multi-node HPMs may choose to adapt the HPM to add board to board connectors on the Far board edge intended to directly mate into chassis power infrastructure (mid-plane, PDB, bus bar etc.).

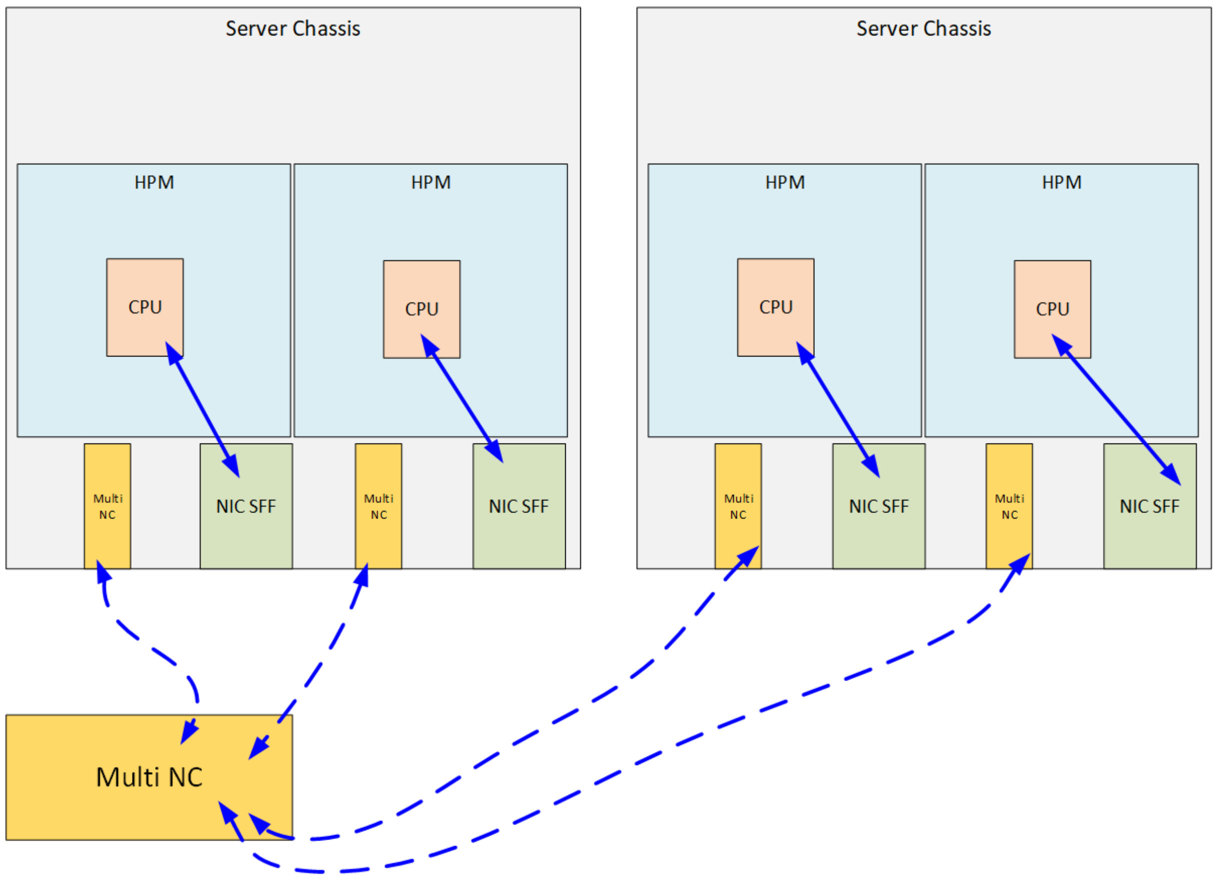
Un-adapted HPMs can also be leveraged with this type of chassis infrastructure by leveraging an interposer board between the HPM and the chassis infrastructure.

The example below depicts using an un-adapted HPM on the left and an adapted HPM on the right in a similar system. For this example, shown is a Type 2 node opting to “float” the DC-SCM and NIC cards as opposed to placing them Co-Planar. Additionally, a 21” chassis is depicted.



Multi-Node Management

How to deploy a multi-node management infrastructure using base specification complaint HPMs is outside of the scope of this specification. However, various common methodologies were evaluated to ensure that M-DNO compliant HPMs could be leveraged into these infrastructures. As an example, a small low-cost local node controller could be connected to the DC-SCM 4C+ connector and then connected to a chassis manager or multi-node controller.



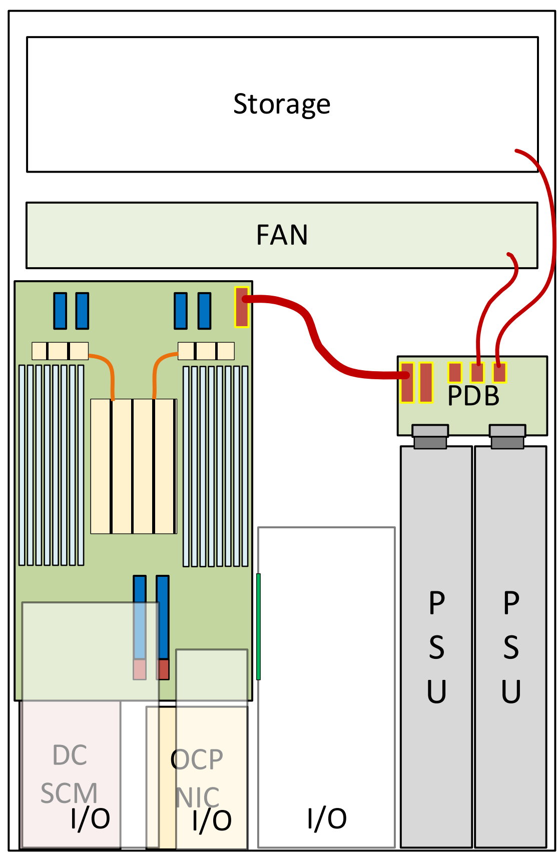
14. Supplemental Material: M-DNO Power Zone Usage Examples

The M-DNO specification provides some flexibility to HPM implementors and system designers when it comes to Power Zone Usage. In this section, demonstration of some expected configurations leveraging these various options are conveyed. For simplicity's sake, the different power flows are demonstrated using the same HPM board Type (Type 2), however the power zone use case flexibility is common across all board types.

The first example listed below shows a simple monolithic (one HPM) system where PSUs feed power to the system PDB, the HPM power zones are utilized in the minimum required model:

- Far Side Ingress: Power from PDB to HPM
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: None
- Supplemental Power to I/O: None

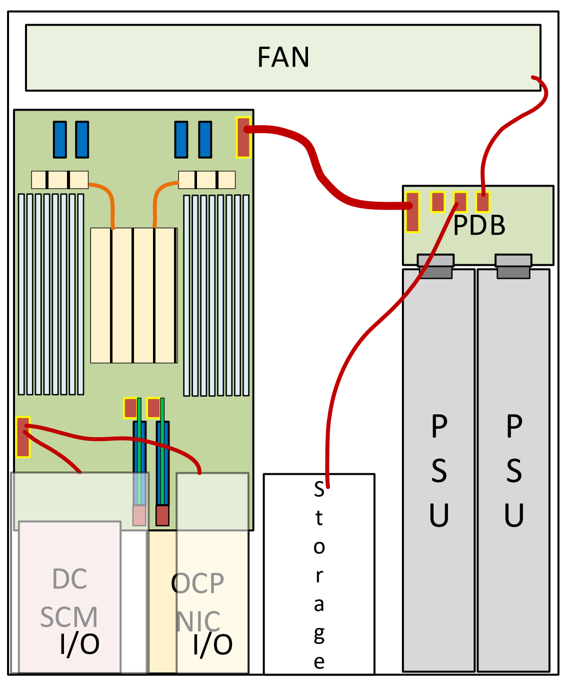
Example 1: Monolithic Basic One Zone Ingress



In the second example below, a monolithic (one HPM) system where PSUs feed power to the system PDB is shown. However, in this example, the optional Near Side power zone is leveraged:

- Far Side Ingress: Power from PDB to HPM
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: Supplemental power cable to CEM card aux (Note that the PICPWR definition requires a control “puck” to power gate these cables)
- Supplemental Power to I/O: From Near Zone (These cables could also be sourced from the PDB directly and would not require a “puck” as control logic could be based on the PDB.)
- Note that because the HPM depicted supports both power Ingress / Egress zones the same HPM could be used in systems which leverage the far side for ingress power

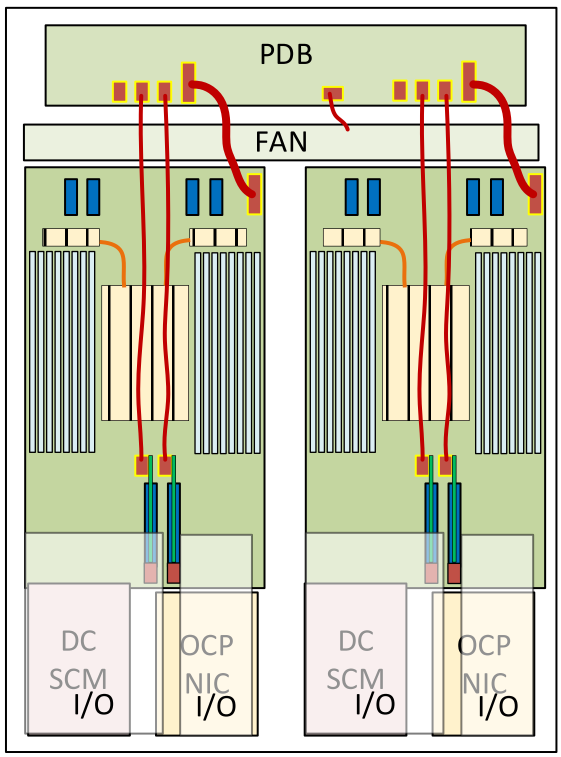
Example 2: Monolithic Leveraging Both Zones



The third example below illustrates a multi-node (>1 HPM) system with a Far Side PDB that could be supplied via PSUs, system level bus bars, or even rack level power distribution.

- Far Side Ingress: Power from PDB to HPM (while these connections are depicted with cables the HPM could also be adapted to support a board-to-board connector to chassis power infrastructure like a PDB as noted in **Section 11.1**)
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: None
- Supplemental Power to I/O: From the PDB directly (do not require a "puck" as control logic could be based on the PDB)

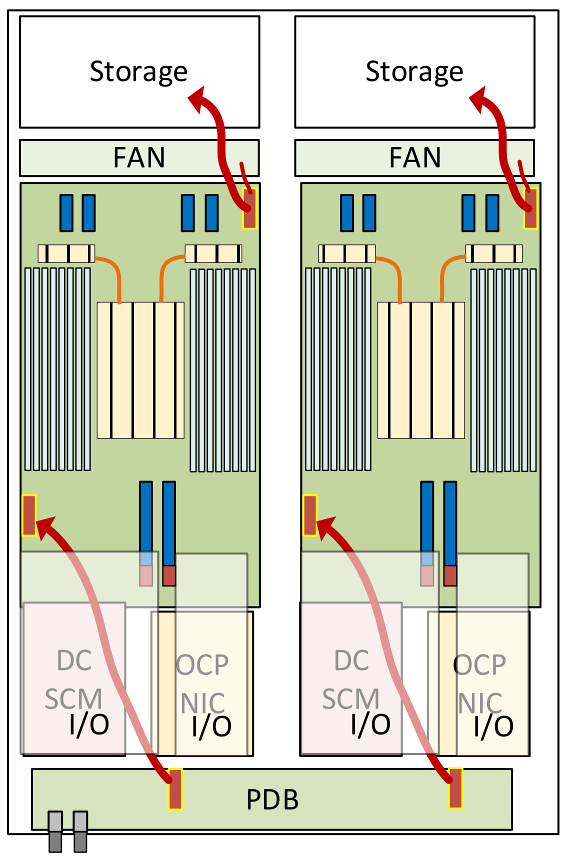
Example 3: Multi-node with Far Side PDB



The fourth example below demonstrates a multi-node (>1 HPM) system with a Near Side PDB that could be supplied via PSUs, system level bus bars or even rack level power distribution.

- Far Side Ingress: None
- Far Side Egress: Used to power Storage peripheral subsystem,
- Near Side Ingress: Power from PDB to HPM (cabled)
- Near Side Egress: None
- Supplemental Power to I/O: None
- Note that because the HPM depicted supports both power Ingress / Egress zones the same HPM could be used in systems which use to leverage the far side for ingress power

Example 4 : Multi-node with Near Side PDB



15. Appendix A - Checklist for IC approval of this specification (to be completed by contributor(s) of this Spec)

Complete all the checklist items in the table with links to the section where it is described in this spec or an external document.

This will be filled out at V1.0

16. Appendix B-__ <supplier name> - OCP Supplier Information and Hardware Product Recognition Checklist

This is a Base Specification and no specific designs can be derived from this specification. Future Design Specifications will be established based on DC-MHS Rev 1.0 specifications, and supplier information and HW checklist will be applicable and filled by future contributors