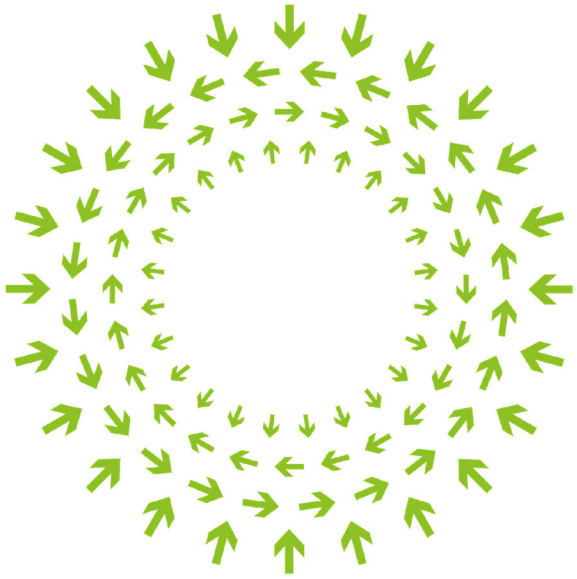

OPEN

Compute Project

Platform Infrastructure Connectivity (M-PIC) Base Specification

Part of the

Datacenter – Modular Hardware Systems (DC-MHS) Rev 1.0 Family

Version 0.90

August 23, 2022

M-PIC Authors/Contributors:

Advanced Micro Devices, Inc: Greg Sellman

Dell, Inc.: Tim Lambert, Sanjiv Sinha, Shawn Dube, Will Smith, Michael Gregoire

Google LLC: Michael Leung, Mike Branch, Siamak Tavallaei

Hewlett Packard Enterprise Company: Daniel Humphrey, Vincent Nguyen

Intel Corporation: Clifford DuBay, Brian Aspnes, Eduardo Estrada, Todd Langley, Aurelio Rodriguez-Echevarria

Meta Platforms, Inc.: Michael Garner, Damien Chong, Todd Westhauser

Microsoft Corporation: Priya Raghu, Shane Kavanagh, Priscilla Lam

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1.2. Acknowledgements

The Contributors of this Specification would like to acknowledge the following companies for their feedback:

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Molex, Amphenol

2. Version Table

Date	Version #	Description
April 22nd 2022	0.70	• Initial public release.
June 8th 2022	0.71	• Added a note about PICPWR signal naming and updated document for consistency in section 8.1.2. • Added notes to allow fusing to protect connectors, cables, and traces and requiring back-feed prevention on modules docking into M-CRPS connectors in section 8.1.4. and section 8.1.5. • Added clarification and guidance allowing peripherals to consume initial power in section 8.1.6. • Added a note about PESTI and recommended usages for PICPWR_A/B_SB1 and PICPWR_A/B_SB4 in *Table 2*, *Table 14*, and *Table 16*. • Added ratings for power connectors in section 8.1.7. • Added a power only riser connector and pinout in section 8.1.7.5. • Updated the connector in section **Error! Reference source not found.** from 12S to 16S to include analog signals, and +12VStby pins. • Removed "Analog" and prepared for the new connector with +12VStby and PDB management signals in section 8.1.9. • Updated the Internal USB connector to recommend type A but allow type C in section 8.4. • Added a note to *Table 14* and *Table 16* recommending overcurrent protection for 12V_CP be added. • Updated control panel pin numbering in *Table 15* and *Table 17*. • Referred to M-XIO for USB2 usage Smart NIC interface in section 8.8. • Added Imon and Vmon signaling requirements in section 8.11. • Added physical connector pin numbering figures for multiple connectors.
June14th 2022	0.72	• Added a note about PESTI giving recommended usages for PICPWR_A/B_SB1 and PICPWR_A/B_SB4 missed in V0.71 for *Table 16*. • Updated control panel USB connectivity in *Figure 25*, *Table 14*, and *Table 16*. • Added a requirement for silkscreen labeling for PICPWR sideband channel positions in sections 8.1.2. • Updated part numbers in sections 8.1.7.1, 8.1.7.2, and 8.1.7.5 • Updated *Figure 1* to use the near side riser connector. • Updated the SPI signaling voltage requirement note.

		• Updated *Figure 2*, *Figure 3*, *Figure 5*, and *Figure 19* to show +12VStby. • Updated to use “shall” for consistency. • Added section 8.11.3 for PMBus and section 8.11.6 for SGPIO. • Added trademark information for PMBus.
June16th 2022	0.73	• Corrected PESTI note from PICPWR_A/B in *Table 14* and *Table 16* for PCP and SCP. • Updated *Figure 17* PCIe AUX Signals. • Updated sections 8.1.8.3 and 8.1.9 defining the PDB management connector. • Added AMD in Section 1.1.
June 17th	0.74	• Updated from AMD to use the official legal name. • Updated PDB management connector to allow for different packaging, different tail lengths, and use the plug that provides a mated height of 8 mm.
June 24th	0.75	• Aligned PDB and PIB terms with definitions in *Table 1*. • 2nd public release
August 23, 2022	0.90	• General cleanup • Added a specification compliance table in Section 4. • Simplified the definition of 12V_PRIMARY and figures in Section 8.1. • Updated PDB management connector and near riser PN(s). • Updated PICPWR, PCP, and SCP SB definitions. • Updated boot storage in section □. • Removed 48V content for v0.9 • Updated SGPIO definition • Added 2x3+6SB 12V PICPWR connectors • Updated 2x6+12SB channel definition to match *Figure 1*. • Specified contact plating for 2x6+12SB and 2x3+6SB headers. • Updated contributor list; grammatical errors • Moved ”12V 3+16S+3 PICPWR Blind-mate Right Angle Connector Pinout” to Supplemental backup section per core team agreements • Added SFF-TA-1033 term to the PICPWR variant associated with the data combo connector defined in M-XIO and SNIA. • Section 1.2 Added some companies that assisted with connector investigationsUpdated 8.2.1 with connector rendering and definition of FLEX pin • Removed connector p/n’s with pointers to main XLSRemoved the blink mate 3+16+3 from main body since it was duplicated with the agreed supplemental until >1.0 • Fixed PICPWR 3+16+3 back into main body and clarified that supplemental section is a placeholder for 48V and UBB 2.0 related investigations.

3. Scope

This document defines technical specifications for the Platform Infrastructure Connectivity Specification used in Open Compute Project. This document shall comprise the hardware product types complete technical specification.

Any supplier seeking OCP recognition for a hardware product based on this spec must be 100% compliant with any and all features or requirements described in this specification.

3.1. Typical OCP Sections Not Applicable

This is a Base specification, requiring other MHS specifications to fully define a design. The following typical Sections of an OCP specification are not included because they are not applicable to this specification.

Rack Compatibility
Physical Spec
Rear Side Power, I/O, Expansion
Mechanical
Onboard Power System
Environmental Regulations/Requirements
Prescribed Materials
Software Support
System Firmware
Hardware Management
Security

4. Specification Compliance Table

#	Technical Specification	Document Reference
1	12V PICPWR connector minimum requirements shall be implemented.	Section 8.1.1
2	12V PICPWR labeling requirements shall be implemented.	Section 8.1.2
3	If HPM supports PSU or power subsystem with 12V output directly docking into the HPM, HPM power distribution architecture requirements shall be Implemented	Section 8.1.4
4	If HPM supports remote PSU or power subsystems (PDB) with 12V output, HPM power distribution architecture requirements shall be implemented.	Section 8.1.5
5	12V PICPWR connector pin definitions, electrical requirements, and topologies shall be implemented.	Section 8.1.7
6	12V PICPWR parts specified (or equivalent) and pinouts shall be implemented.	Sections 8.1.7.1 thru **Error! Reference source not found.**

7	If the HPM supports remote PSU or power subsystems (PDB), PDB Management Connector part (or equivalent), pin definitions, electrical requirements, and pinout shall be implemented.	Section 8.1.9
8	If a cable optimized boot storage subsystem is implemented, the required connector part (or equivalent), pin definitions, electrical requirements, and pinout shall be implemented.	Section 8.2.1
9	If a direct dock boot storage subsystem is implemented, the requirements for M.2 or E1.S connector type and pinout shall be implemented.	Sections 8.2.2.1 and 8.2.2.2
10	Intrusion header part (or equivalent), pin definitions, connectivity, electrical requirements, and pinout shall be implemented.	Section 8.3
11	If the form factor specification for the form factor selected specifies an internal USB connector, internal USB connector generation and type requirements shall be implemented.	Section 8.4
12	If the form factor specification for the form factor selected specifies a single control panel connector, the primary control panel connector part (or equivalent), pin definitions, electrical requirements, and pinout shall be implemented.	Section 8.5.1
13	If the form factor specification for the form factor selected specifies a second control panel connector, the secondary control panel connector part (or equivalent), pin definitions, electrical requirements, and pinout shall be implemented.	Section 8.5.2
14	Coin cell battery requirements shall be implemented	Section 8.9
15	DC-SCM 2.0 shall be implemented.	Section 8.10
16	Electrical requirements shall be implemented.	Section 8.11

5. Overview

This specification defines and standardizes common elements needed to interface a Host Processor Module (HPM) to the platform/chassis infrastructure elements/subsystems within the DC-MHS 10 family of OCP servers. Standardization of the common interfaces and connectors enables hardware compatibility between DC-MHS HPMs and various DC-MHS system components.

The standardized common elements defined in this specification can be utilized by DC-MHS form-factor specifications and/or DC-MHS peripherals. The elements defined within this specification are not inherently required with a DC-MHS form-factor. The form-factor specifications call out which of these elements are required or optional, the physical placement, and any additional details specific to that form-factor.

This specification defines connectors, signals, and electrical interface requirements to enable connectivity and hardware compatibility to the following types of platform/chassis infrastructure:

1. Cooling infrastructure including:
    a. **Cooling modules** with one or more intelligent fan controllers, interfaced to air-movers
    b. Monitoring and control of **liquid-cooling infrastructure**, handled as intelligent cooling modules

2. **Power distribution/management:** Connectors for input power from source or PDB (power distribution board) and connectors to output power to peripheral subsystems.
3. **Boot storage peripheral**: small modules that provide minimal storage for a hypervisor or OS, typically using USB or 1 to 4 lanes of PCIe, typically a monolithic storage device or a controller with RAID1 using two media devices.
4. **Intrusion switch** to detect physical access to the internals of a platform.
5. **Internal Host USB** for Internal Key functions, debug, or as an additional source for control panel USB.
6. **Control panels** for human interaction beyond what is offered on DC-SCM. This includes options for indirect support for buttons, LEDs, more complex displays, and external peripheral ports like USB.
7. **Smart NIC Management Interface:** for Smart NICs connected via M-XIO.
8. **Coin Cell Battery** to supply battery back-up power for features like RTC.
9. **DC-SCM** – Data Center Secure Control Module Revision 2.0 is used with DC-MHS.

5.1. Items Not Included

- Designs or specific implementation requirements on platform infrastructure including those referenced above.
- Elements specified by DC-SCM
- Elements specified by DC-MHS XIO Specifications
- Elements supporting rack-level infrastructure
- NVMe Hot plug: attention and LEDs
- Edge/Telco: time-sync requirements

6. Terminology

Table 1: Terminology

Standardized Term	Meaning	Alternative Terms
DC-SCM	Data Center Secure Control Module	
DC-MHS	Data center - Modular Hardware System	
M-FLW	Modular Hardware System Full Width HPM Form Factor	FLW
M-DNO	Modular Hardware System Partial Width Density Optimized HPM Form Factor	DNO
M-XIO	Modular Hardware System eXtensible I/O	XIO
M-CRPS	Modular Hardware System Common Redundant Power Supply	PSU, CRPS
HPM	Host Processor Module PCB or PCBA form factor defined in M-FLW or M-DNO	

Smart NIC	A programmable network device used to improve data center networking performance, security, features, and flexibility.	IPU or DPU
MCU	A microcontroller unit	uC
CEM	Card Electromechanical specification	
ACPI	Advanced Configuration and Power Interface	
PIB	Power Interface Board	
PDB	Power Distribution Board	
SMBus	System Management Bus	SMB
PMBus	Power Management Bus	PMB
+12VStby	12V Standby from CRPS	
+12V	12V Main Power from CRPS	
PICPWR	Platform Infrastructure Connectivity Power distribution connector	
SGPIO	Serial GPIO	

7. Thermal Design

Systems have variable cooling requirements ranging from air movers to liquid cooling or hybrid solutions. This section describes the power and management interface for cooling systems which play a vital role in the overall thermal solution. The HPM interface covered for cooling addresses only cooling subsystems connected to HPM via separate cooling subsystem boards because the HPM formfactors standardized on off-HPM cooling solutions. The adoption of DC-SCM caused the change in air mover cooling system architecture from discrete fan controls via BMC to cooling system being controlled over SMBus or I3C. The choice to use off HPM cooling solutions provides greater flexibility and applicability of an HPM to different platforms and cooling solutions. The method chosen for DC-MHS utilizes the managed power distribution connection (namely PICPWR) from the HPM or power distribution board for power and all remote cooling control management. The PICPWR connector includes an SMB/I3C interface and 4 additional sideband signals (per channel) that can be used to manage the cooling subsystem board. (See section **8.1** for the 12V PICPWR definition).

There is no intent to provide a dedicated remote cooling connector /interface definition.

In some cases, the cooling system may be managed and/or powered at a chassis or rack level so the HPM may play no role in the cooling system.

8. Power Delivery

8.1. 12V Power Distribution and Management

This section covers the minimum power distribution architecture requirements for a 12V HPM, and peripheral subsystems attached to the HPM. Example peripheral subsystems include, but not limited to, risers, backplanes, cooling, battery power, ingress from PSU or higher-level power source (e.g., multimodal). PICPWR stands for Platform Infrastructure Connectivity Power distribution connector. The goal is for HPM and Power Distribution boards to provide a homogeneous power + sideband interface for powering remote peripherals (like backplanes, risers, PCIe CEM AUX connections, etc.). Peripheral subsystems that do not require HPM to supply or manage their ingress power source are outside the scope of this specification. If an HPM contains 12V PICPWR connectors, the use of those connectors is optional.

8.1.1. 12V PICPWR Power Connector Form Factor

Distribution of power within the HPM and to/from Peripheral Subsystems can be implemented in any connector form factor that meets minimum requirements:

- Connectors shall have power pins with equal capability for 12V_PRIMARY power supply and return.
- Connectors shall have 6 sideband pins dedicated for power delivery management.

Power connectors that meet the minimum requirements are referred to as 12V PICPWR connectors

A 12V PICPWR connector can include an implementation that has additional function/signals (for example, high-speed IO) shared in a common connector housing. Additionally, a PICPWR connector can support multiple channels of sideband signals, where each channel shall contain the 6 sideband pins dedicated for power delivery management.

Figure 1 shows an example of a stand-alone 12V PICPWR connector as well as a 12V PICPWR implementation as part of a larger connector with additional functions/signals.

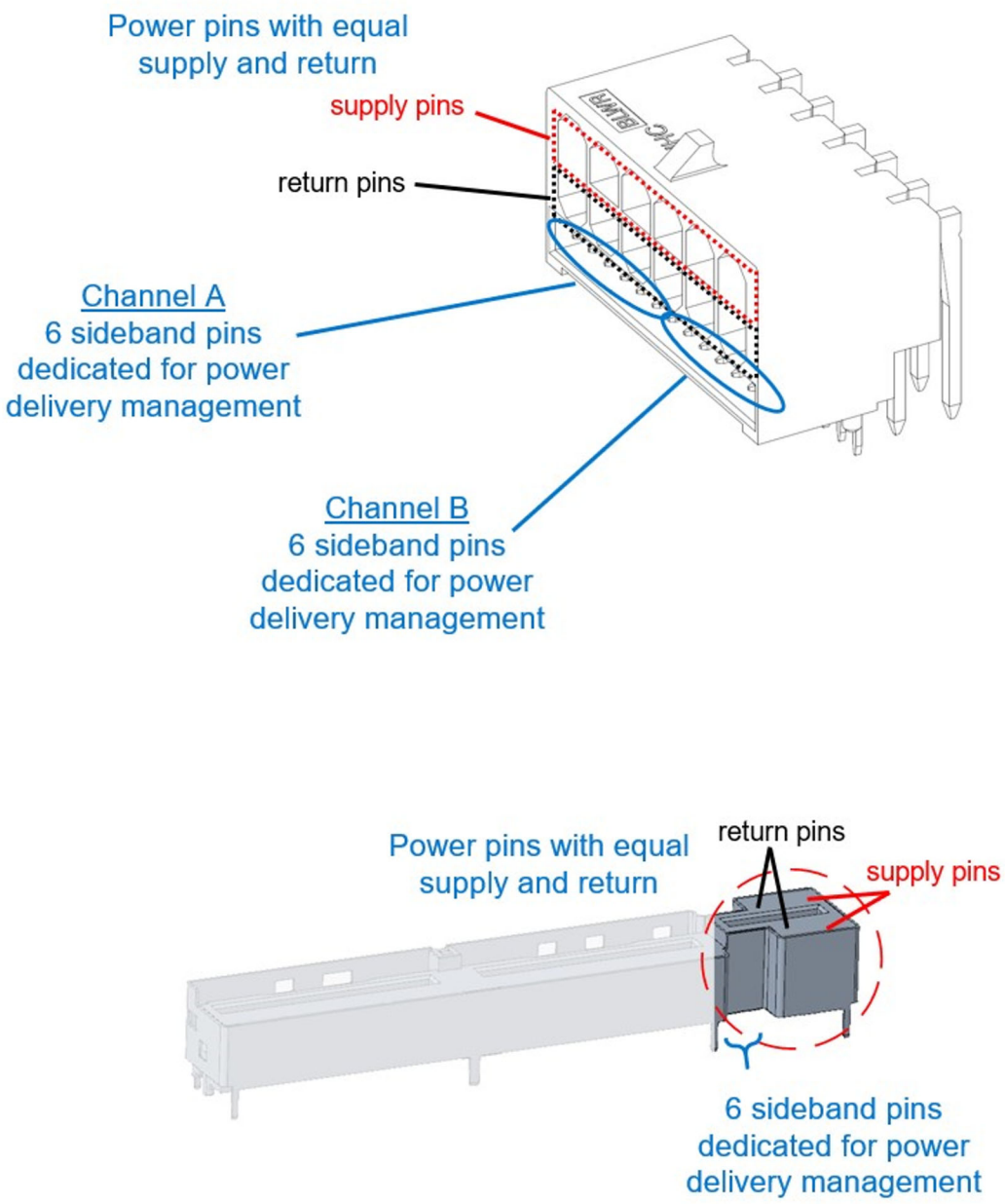


Figure 1: Examples of 12V PICPWR Connectors

8.1.2. 12V PICPWR Connector Power Labeling Requirements

PICPWR connector contains two or more sideband channels, a visible silkscreen shall be placed near each 12V PICPWR connector to indicate the position for each channel. Example: “A” on the right side and “B” on the left side.Since each 12V PICPWR connector power rating will depend on the ampacity and number of supply and return pins in the connector, as well as the size of copper planes attached to the connector, a visible silkscreen shall be placed near the

PICPWR connector to indicate the maximum TDP (Thermal Design Point) capability of the PICPWR implementation. Example “PWR*n*_12V_600W”, where *n* is a unique identifier/number for each PICPWR connector instantiation per board. If any 12V

8.1.3. 12V Management Signal Naming

The 12V PICPWR and PDB connector signal naming shown in the rest of this specification is represented as “*location*_PICPWRn_A/B_***” where; *location* is the destination board on which the connector will be located (*location* is blank since most are expected to be on HPM), n is the unique identifier per board, A/B is the sideband channel (if more than one channel exists in the connector), and *** is the signal function (SB[4:1], SCL, or SDA). Example: PDB_PICPWR3_A_SCL.

8.1.4. 12V HPM Power Distribution Architecture

This section describes implementations of the HPM where the PSU or power subsystem is directly docking into the HPM.

Referring to *Figure 2*, the HPM power distribution architecture has the following attributes:

- “12V_PRIMARY” shall be sourced by +12V in ACPI Power states from ACPI-S5 and higher (i.e., in ACPI-S5 to ACPI-S0).
- The 12V power MGMT switching circuit shall be located on the HPM.
- 12V PICPWR connectors shall only connect to 12V_PRIMARY.
- 12V PICPWR connectors shall be bi-directional: can be either power source (power egress) or power sink (power ingress).
- Other than the power capability of the power connector, each 12V PICPWR connector on the HPM shall be logically equivalent.
- It is strongly recommended that HPM designs balance current flow through adjacent 12V PICPWR connectors to enable source or load sharing and without overloading one of the two current paths.
- **There shall not be power gating to 12V PICPWR connectors on 12V_PRIMARY**. However, the HPM may implement fusing to prevent damage to connectors, cables, and traces.
- Any module docking into the M-CRPS connector shall have an ORing circuit or an HSC circuit on +12V to prevent reverse current going into the module.
- In implementations where the PSU is directly docking into the HPM, HPM and/or the PSU shall implement gating for the voltage output of the PSU to prevent the wrong voltage from being distributed through the 12V_PRIMARY rail (e.g., 48V instead of 12V).

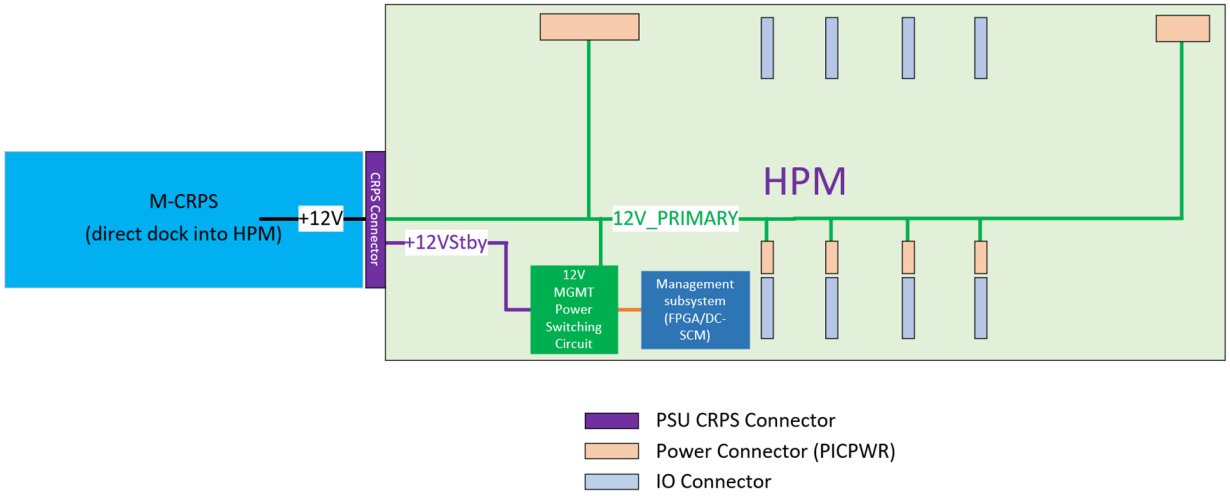


Figure 2: HPM 12V Power Distribution Architecture (PSU Direct mate to HPM variant)

8.1.5. 12V Remote Power Distribution Architecture

This section describes requirements of a Remote Power Distribution implementation where the PSU or power subsystem is docking into the Remote Power Distribution or PDB/PIB (Power Distribution Board / Power Interface Board) and powering the HPM via a 12V PICPWR connector on the HPM.

Referring to *Figure 3*, the Remote Power Distribution architecture has the following attributes:

- "12V_PRIMARY" shall be sourced by +12V in ACPI Power states from ACPI-S5 and higher (i.e., in ACPI-S5 to ACPI-S0).
- The 12V power MGMT switching circuit shall be located on the HPM.
- Any module docking into the M-CRPS connector shall have an ORing circuit or an HSC circuit on +12V to prevent reverse current going into the module.
- In implementations where the PSU is directly docking into a PDB, PDB and/or the PSU shall implement gating for the voltage output of the PSU to prevent the wrong voltage from being distributed through the 12V_PRIMARY rail (e.g., 48V instead of 12V).
- If configurations with power subsystems directly docking into the HPM and connected to the HPM through a PDB exist, requirements for each attachment method shall be met, even though they may share power.

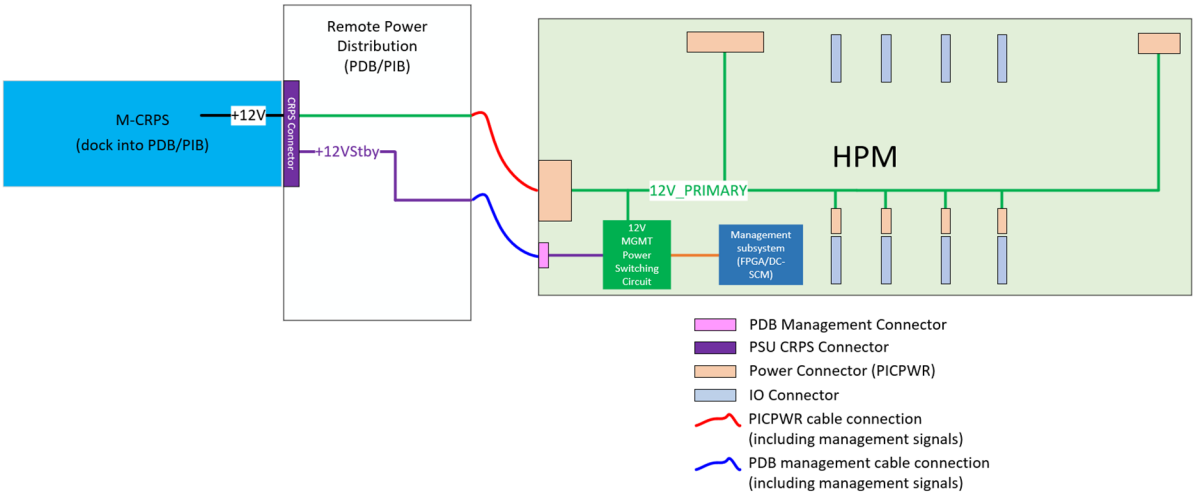


Figure 3: Remote 12V Power Distribution Architecture (PSUs mate to PDB/PIB variant)

8.1.6. 12V Peripheral Subsystem Power Distribution Architecture

Referring to *Figure 4*, the Peripheral Subsystem power architecture has the following attributes:

- Peripheral subsystems can attach to any 12V PICPWR connector on the HPM that has the power capability to support loads of the peripheral subsystem.
- 12V PICPWR connectivity methods are dependent on system needs and connection type(s) supported at each 12V PICPWR location (e.g., card edge or a compatible cable).
- For cable applications with 12V PICPWR connectors, the pinouts shall both meet M-PIC pinout requirements.
- A peripheral subsystem consists of a management subsystem, a power gating subsystem, and a power load.
- The peripheral subsystem shall assume that the power rail supplied from the HPM will be operational in the ACPI-S5 power state. If the load on the peripheral subsystem is not intended to operate in the S5 domain, then the peripheral subsystem shall implement appropriate power gating for the load.
- Loads shall not be directly attached to 12V PICPWR connectors (e.g., PCIe AUX power cable attaching from 12V PICPWR to PCIe AIC (Add In Card) is NOT supported). Minimally, a power delivery management subsystem shall be implemented on the peripheral subsystem or the load that is compatible with the PICPWR sidebands.
- Peripherals may consume a small amount of power for inventory and sideband initialization prior to being transitioned to higher power states by the HPM. It is strongly recommended that peripheral designs minimize the initial power consumed. It is also recommended that system designers verify that the total system power consumed is within the total initial power available.

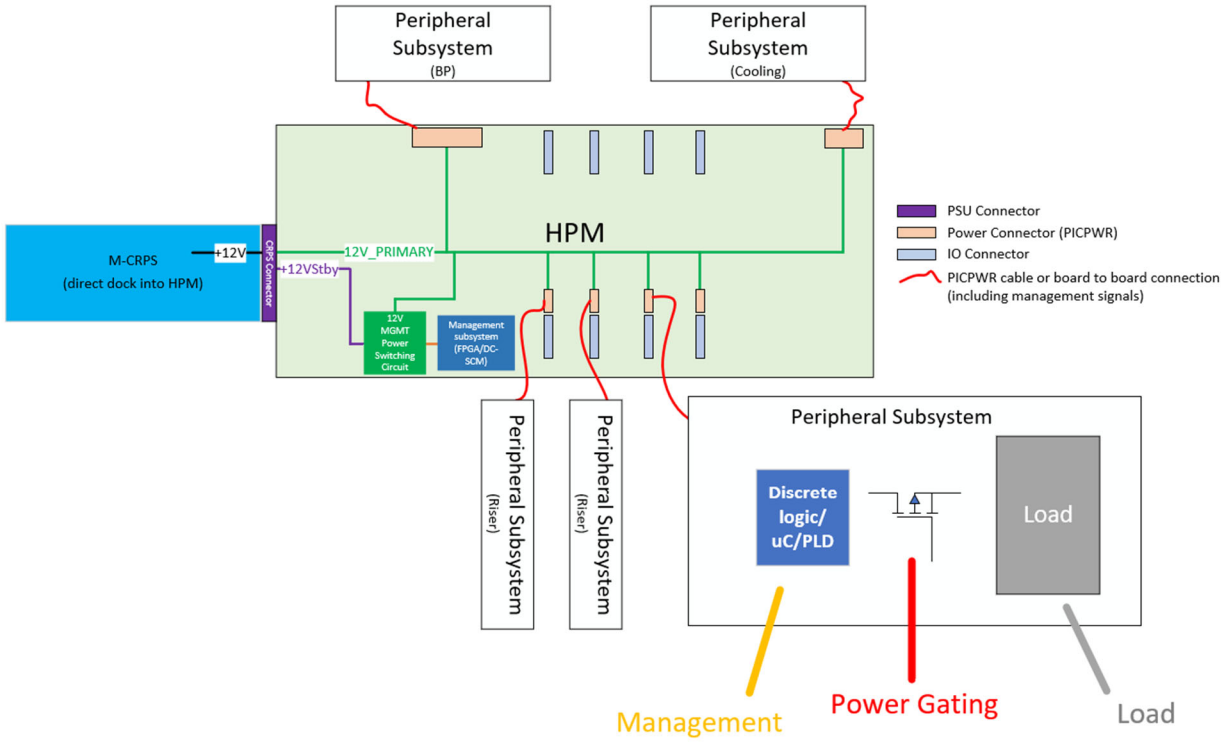


Figure 4: Peripheral Subsystem 12V Power Distribution Architecture

Figure 5 shows additional details of the power architecture of a Peripheral Subsystem.

- Power gating in the Peripheral Subsystem is needed if loads are not intended to operate in ACPI-S5 state. Power gating can be implemented in a variety of forms including, but not limited to, load switches, hot-swap controller, voltage regulators. System implementors shall design a Peripheral Subsystem that does not cause back-feeding, over current, or over voltage events to propagate back into the HPM and Power Supply subsystem.
- 4 Sideband GPIOs and an SMBus interface shall be provided to the peripheral subsystem to enable the HPM to perform status, control, and inventory.
- It is strongly recommended that Peripheral designs balance current flow through PICPWR connectors in applications that source power through more than one 12V PICPWR connector (on HPM or on the peripheral) to prevent overloading one of the two current paths.

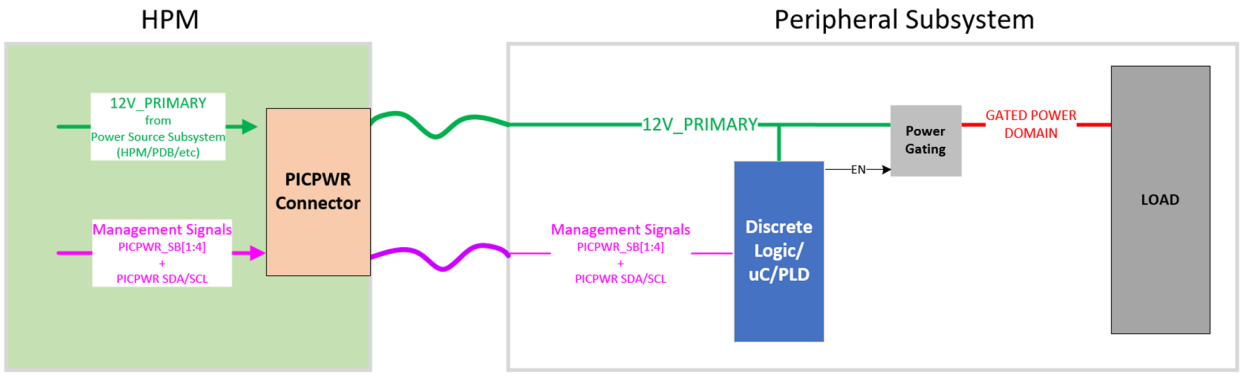


Figure 5: Peripheral Subsystem 12V Power Distribution Architecture Details

8.1.7. 12V PICPWR Connector Pin Definition

Table 2: 12V PICPWR Pin Definition

Pin(s)	Signal Name	Signal Requirements
PWR	12V_PRIMARY	Primary power rail from the power source subsystem used to power downstream loads & logic on peripheral subsystem 12V_PRIMARY shall be sourced by +12V in ACPI Power states from ACPI-S5 and higher (i.e., in ACPI-S5 to ACPI-S0).
PWR	GND	Ground return for 12V_PRIMARY and side-band signals
SB1:4	PICPWR*n*_SB[1:4]	Sideband GPIOs for status, control, and inventory of peripheral subsystem; shall be connected to HPM FPGA with prescribed terminations for “Plug-N-Code” specific usages. For electrical requirements see section **8.11.1**, Table 3, and *Figure 6*. The Plug-N-Code connectivity also enables the PESTI interface described in the M-PESTI specification. To maximize commonality between peripherals, it is recommended to use PICPWR_A/B_SB1 for PRES_N or PESTI functionality and use PICPWR_A/B_SB2 as active high power enable or for PWREN (power enable) functionality. SB[3:4] terminations and connections are optional and may be omitted if not used.
SB5	PICPWR*n*_SCL	See section **8.11.2**. for SMBus and I3C electrical requirements.
SB6	PICPWR*n*_SDA	

Each instantiation of a PICPWR connector shall implement a unique set of 6 sidebands. Additionally, *Table 3* describes how the sideband signals on the HPM shall be implemented.

Table 3: Required HPM implementation for each 12V PICPWR connector

Pin	Signal Name	HPM Implementation Requirements		
		HPM Connections	**Termination**	**HPM GPIO Buffer Type**
SB1	PICPWR*n*_SB1	connect to HPM FPGA GPIO	22Ω Series + 127kΩ pullup to +3.3Vaux	Configurable as both open-drain AND push-pull
SB2	PICPWR*n*_SB2	connect to HPM FPGA GPIO	22Ω Series + 127kΩ pulldown to GND	Configurable as both open-drain AND push-pull
*SB3	*PICPWR*n*_SB3	*connect to HPM FPGA GPIO	*22Ω Series + *127kΩ pullup to +3.3Vaux	*Configurable as both open-drain AND push-pull
*SB4	*PICPWR*n*_SB4	*connect to HPM FPGA GPIO	*22Ω Series + *127kΩ pullup to +3.3Vaux	*Configurable as both open-drain AND push-pull
SB5	PICPWR*n*_SCL	connect to DC-SCM SMBus subsystem	See section **8.11.2** for SMBus and I3C electrical requirements.	SMBus or I3C Basic compliant
SB6	PICPWR*n*_SDA	connect to DC-SCM SMBus subsystem		SMBus or I3C Basic compliant

*These components and connections are optional and may be omitted if not used.

Figure 6 shows the required HPM implementation with the example of two 12V PICPWR connector instantiations. Pullups on SCL and SDA are shown for reference, see *Table 3* for details.

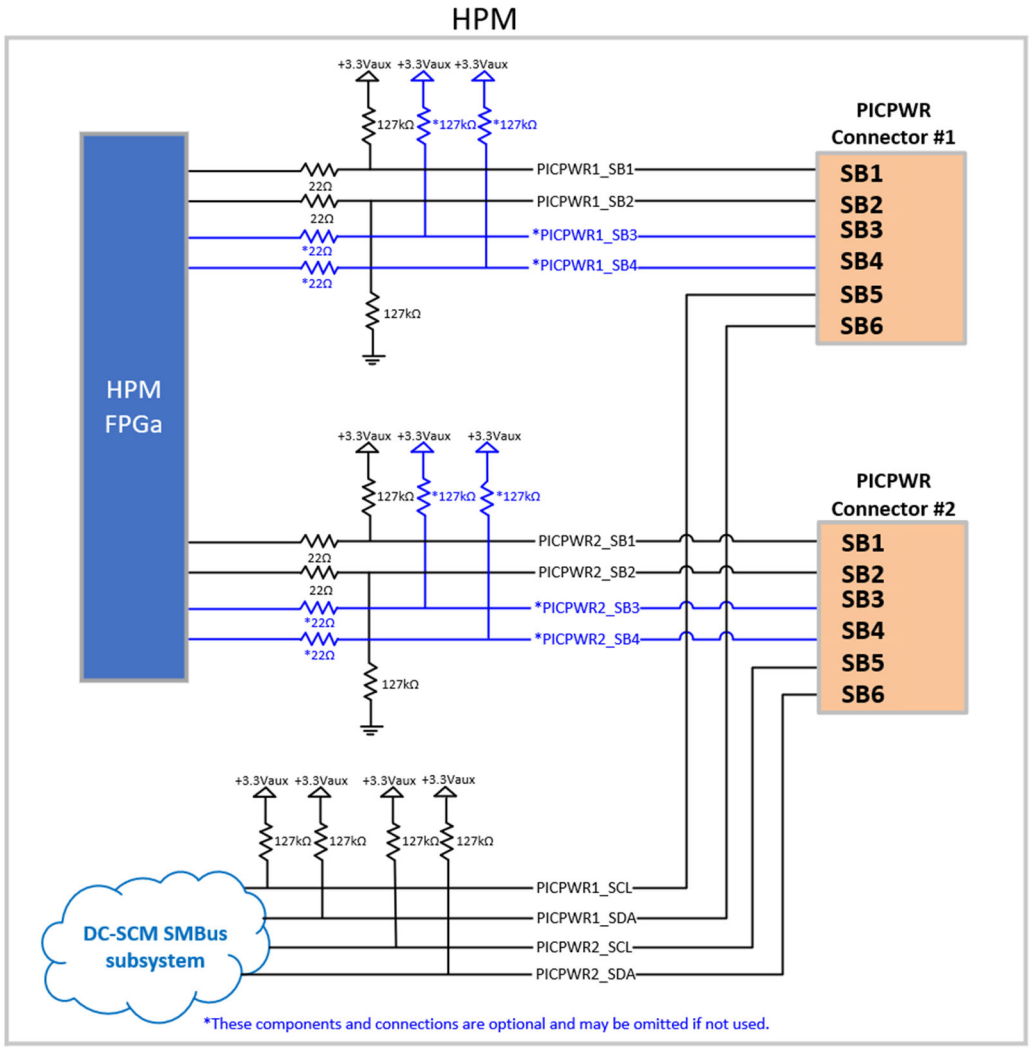


Figure 6: HPM implementation with two 12V PICPWR connectors

8.1.7.1. 12V 2x6+12SB PICPWR Right Angle Header Pinout

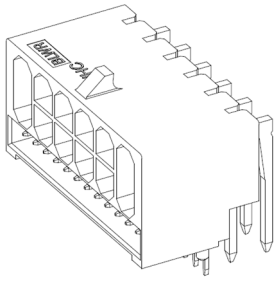


Figure 7: 12V 2x6+12SB Right Angle Header

Notes:

- Connector power rating: 864W (12A per power pin)
- This connector has two independent channels (A & B) of PICPWR sideband management signals.
- Refer to documentation of connector vendors and part numbers located at: DC-MHS Connector Information @ https://drive.google.com/drive/folders/1sURGb6UQ7pzr48_0RnXanBGqgC2a4EA4
-
-

Table 4: 12V 2x6+12SB PICPWR Right Angle Header Pinout

Pin(s)	Signal Name
Circuits [1:6]	GND
Circuits [7:12]	12V_PRIMARY
SB1	PICPWR*n*_B_SB1
SB2	PICPWR*n*_B_SB2
SB3	PICPWR*n*_B_SB3
SB4	PICPWR*n*_B_SB4
SB5	PICPWR*n*_B_SCL
SB6	PICPWR*n*_B_SDA
SB7	PICPWR*n*_A_SB1
SB8	PICPWR*n*_A_SB2
SB9	PICPWR*n*_A_SB3
SB10	PICPWR*n*_A_SB4
SB11	PICPWR*n*_A_SCL
SB12	PICPWR*n*_A_SDA

Refer to *Figure 8* for 2x6+12SB physical connector pin numbering.

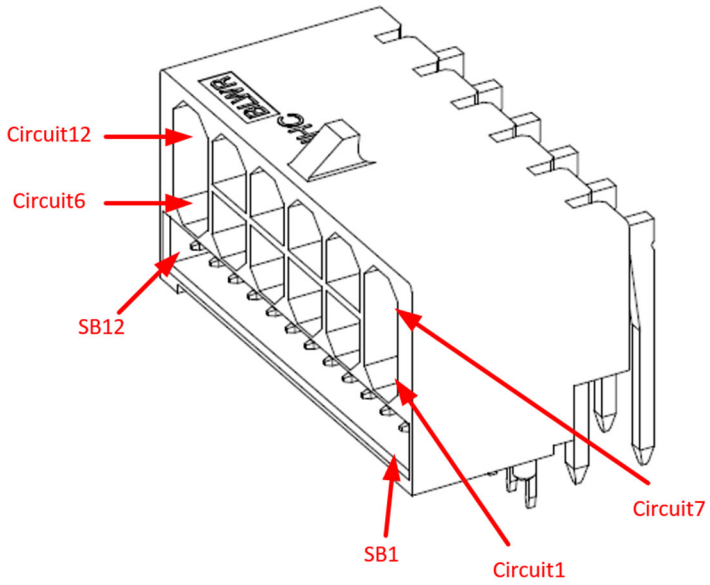


Figure 8: 2x6+12SB Physical Pin Numbering

8.1.7.2. 12V 2x6+12SB PICPWR Vertical Header Pinout

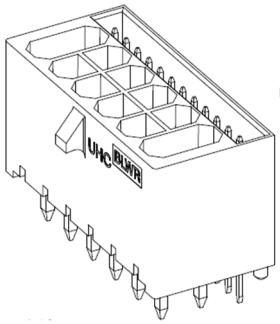


Figure 9: 12V 2x6+12SB Vertical Header

Notes:

- Connector power rating: 864W (12A per power pin)
- This connector has two independent channels (A & B) of PICPWR sideband management signals.
- Refer to documentation of connector vendors and part numbers located at: DC-MHS Connector Information @ https://drive.google.com/drive/folders/1sURGb6UQ7pzr48_0RnXanBGqgC2a4EA4

Table 5: 12V 2x6+12SB PICPWR Vertical Header Pinout

Pin(s)	Signal Name

Circuits [1:6]	GND
Circuits [7:12]	12V_PRIMARY
SB1	PICPWR*n*_B_SB1
SB2	PICPWR*n*_B_SB2
SB3	PICPWR*n*_B_SB3
SB4	PICPWR*n*_B_SB4
SB5	PICPWR*n*_B_SCL
SB6	PICPWR*n*_B_SDA
SB7	PICPWR*n*_A_SB1
SB8	PICPWR*n*_A_SB2
SB9	PICPWR*n*_A_SB3
SB10	PICPWR*n*_A_SB4
SB11	PICPWR*n*_A_SCL
SB12	PICPWR*n*_A_SDA

Refer to *Figure 8* for 2x6+12SB physical connector pin numbering.

8.1.7.3. 12V 2x3+6SB PICPWR Right Angle Header Pinout

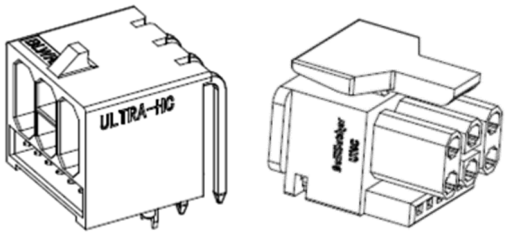


Figure 10: 12V 2x3+6SB Right Angle Header and associated plug

Notes:

- Connector power rating: 486W (13.5A per power pin)
- This connector has one channel of PICPWR sideband management signals.
- Refer to documentation of connector vendors and part numbers located at: DC-MHS Connector Information @ https://drive.google.com/drive/folders/1sURGb6UQ7pzr48_0RnXanBGqgC2a4EA4
-

Table 6: 12V 2x3+6SB Right Angle Header Pinout

Pin(s)	Signal Name
Circuits [1:3]	GND
Circuits [4:6]	12V_PRIMARY
SB1	PICPWR*n*_SB1
SB2	PICPWR*n*_SB2
SB3	PICPWR*n*_SB3
SB4	PICPWR*n*_SB4
SB5	PICPWR*n*_SCL
SB6	PICPWR*n*_SDA

Refer to *Figure 11* for 2x3+6SB physical connector pin numbering.

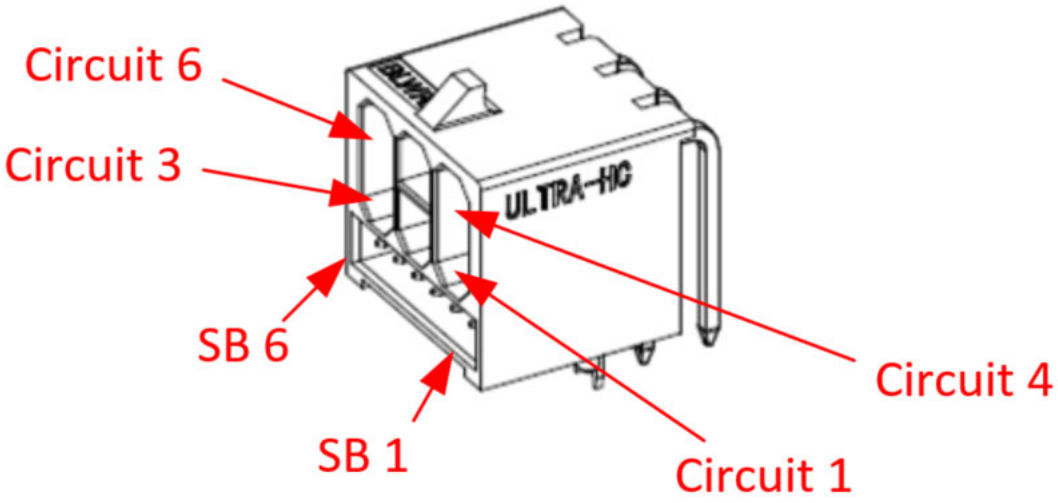


Figure 11: 2x3+6SB Physical Pin Numbering

8.1.7.4. 12V 2x3+6SB PICPWR Vertical Header Pinout

OBJ

Figure 12: 12V 2x3+6SB Vertical Header

Notes:

- Connector power rating: 486W (13.5A per power pin)
- This connector has one channel of PICPWR sideband management signals.

- Refer to documentation of connector vendors and part numbers located at: DC-MHS Connector Information @ https://drive.google.com/drive/folders/1sURGb6UQ7pzr48_0RnXanBGqgC2a4EA4
-

Table 7: 12V 2x6+12SB PICPWR Vertical Header Pinout

Pin(s)	Signal Name
Circuits [1:3]	GND
Circuits [4:6]	12V_PRIMARY
SB1	PICPWR*n*_SB1
SB2	PICPWR*n*_SB2
SB3	PICPWR*n*_SB3
SB4	PICPWR*n*_SB4
SB5	PICPWR*n*_SCL
SB6	PICPWR*n*_SDA

Refer to *Figure 11* for 2x3+6SB physical connector pin numbering.

8.1.7.5. 12V Near Side Riser PICPWR Pinout

The M-XIO specification defines the SFF-TA-1033 connector including the PICPWR section as shown here.

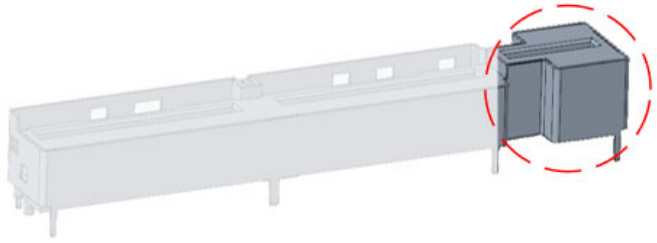


Figure 13: 12V I/O Plus Power Near Side Riser PICPWR Egress

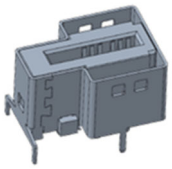


Figure 14: SFF-1033 (power only)

Notes:

- Connector power rating: 225W (9.375A per power pin)
- Part Number: G03V213**HR has M-XIO and PICPWR pins all within the same housing. *Table 8* only covers the pinout of the power section of this connector (circled in *Figure 13*). Refer to M-XIO specification for additional pinout details.
- Part Number: G03VP13**HR includes only the power section of this connector (shown in *Figure 14*).
- Both connector part numbers have two independent channels (A & B) of 12V PICPWR sideband management signals.
- Refer to documentation of connector vendors and part numbers located at: DC-MHS Connector Information @ https://drive.google.com/drive/folders/1sURGb6UQ7pzr48_0RnXanBGqgC2a4EA4
-

Table 8: 12V Near Side Riser PICPWR Pinout

Pin	Signal Name	Signal Name	Pin
SA1	PICPWR*n*_A_SB1	PICPWR*n*_B_SB1	SB1
SA2	PICPWR*n*_A_SB2	PICPWR*n*_B_SB2	SB2
SA3	PICPWR*n*_A_SB3	PICPWR*n*_B_SB3	SB3
SA4	PICPWR*n*_A_SB4	PICPWR*n*_B_SB4	SB4
SA5	PICPWR*n*_A_SCL	PICPWR*n*_B_SCL	SB5
SA6	PICPWR*n*_A_SDA	PICPWR*n*_B_SDA	SB6
PA1	GND	GND	PB1
PA2	12V_PRIMARY	12V_PRIMARY	PB2

Refer to *Figure 15* for 12V near side riser PICPWR physical connector pin numbering.

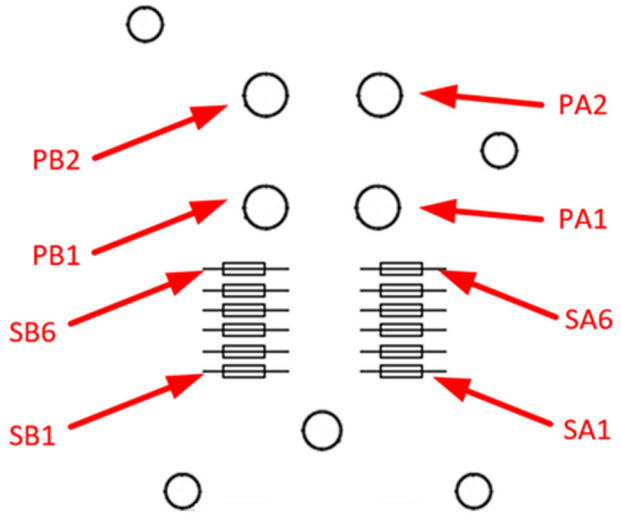


Figure 15: SFF-1033 (power only) Physical Pinout

8.1.7.6. 12V 3+16S+3 PICPWR Blind-mate Right Angle Connector Pinout

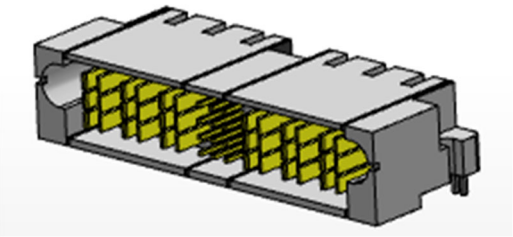


Figure 16: 12V 3+16S+3 PICPWR Blind-mate connector

Notes:

- Connector power rating 1080W (30A per high power contact, 3A per signal contact)
- Refer to documentation of connector vendors and part numbers located at: DC-MHS Connector @ https://drive.google.com/drive/folders/1sURGb6UQ7pzr48_0RnXanBGqgC2a4EA4
-

Table 9: 12V 3+12S+3 PICPWR Blind-mate Right Angle Connector Pinout

Pin(s)	**Signal Name**
P[1:3]_ [1:8]	GND
A1	PICPWR*n*_A_SCL
A2	PICPWR*n*_A_SDA
A3	PICPWR*n*_A_SB1
A4	IMON
B1	PICPWR*n*_A_SB2
B2	PICPWR*n*_A_SB3
B3	PICPWR*n*_A_SB4
B4	+12VStby
C1	PICPWR*n*_B_SCL
C2	PICPWR*n*_B_SDA
C3	PICPWR*n*_B_SB1
C4	VMON
D1	PICPWR*n*_B_SB2
D2	PICPWR*n*_B_SB3
D3	PICPWR*n*_B_SB4
D4	+12VStby
P[4:6]_ [1:8]	12V_PRIMARY

Refer to *Figure 16* for 12V 3+12S+3 PICPWR blind-mate right angle connector physical pinout.

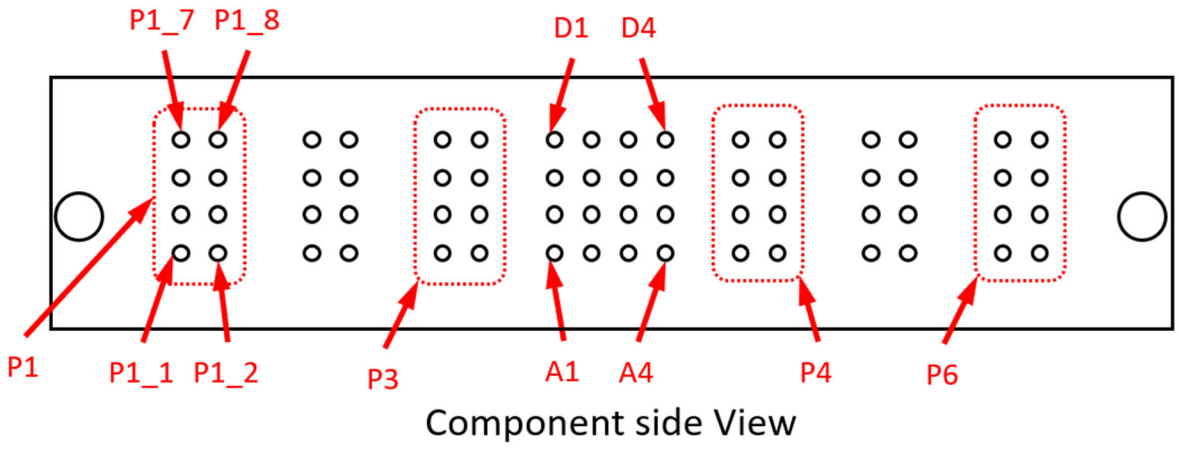
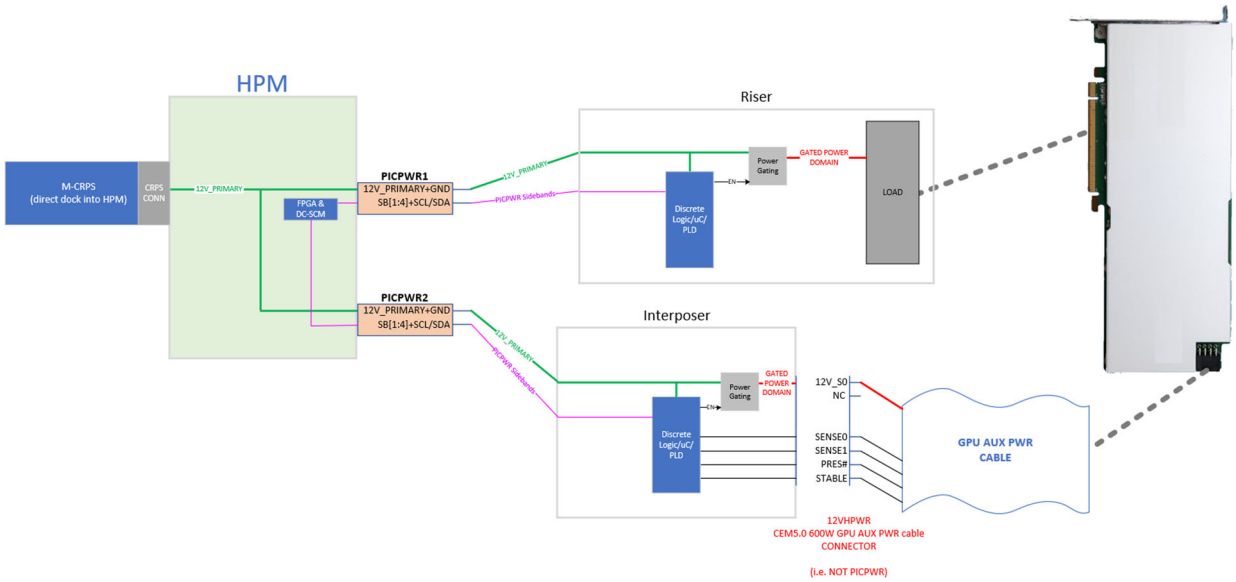


Figure 16: 12V 3+12S+3 PICPWR Blind-mate Right Angle Connector Physical Pinout

8.1.8. Example 12V Topologies

8.1.8.1. Powering a 12V PCIe Device with AUX Power Cable

Figure 17 shows a couple of example implementations of how to use 12V PICPWR to power a PCIe device with an AUX cable. Note that the PCIe AUX power cable is not directly attached to the HPM's 12V PICPWR connector. Instead, the AUX power cable comes from a PDB or a peripheral subsystem with management and power gating capability.



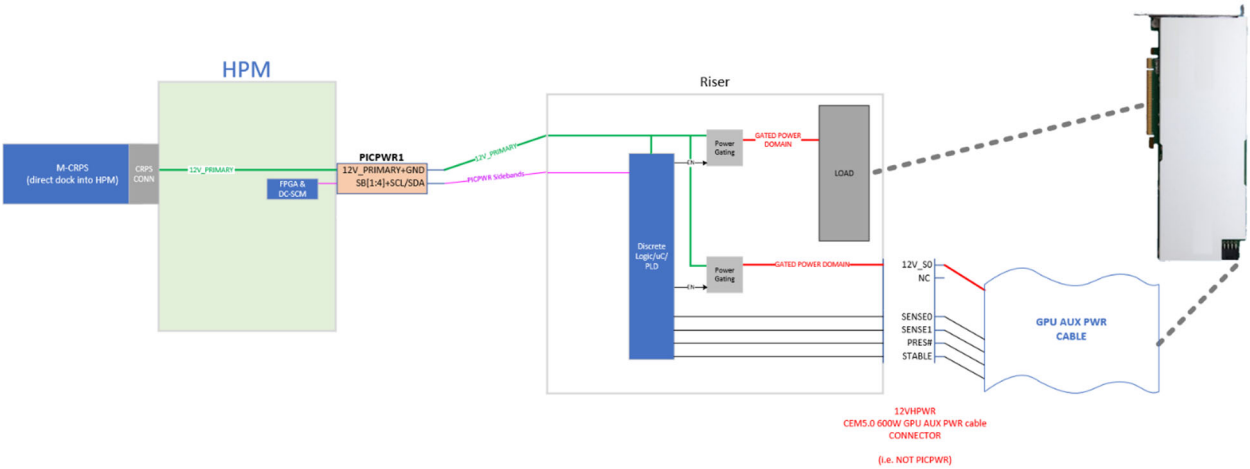


Figure 17: Powering a 12V CEM Riser & 12V PCIe Device 's AUX Power Cable

8.1.8.2. Multiple 12V PICPWR Connectors Powering a Peripheral Subsystem

Figure 18 shows two 12V PICPWR connectors on the HPM powering a single peripheral subsystem to support the large power requirements of a single peripheral subsystem. It is strongly recommended that HPM, cable, and peripheral designs balance current flow through both PICPWR connectors in applications with shared sources or loads to prevent overloading one of the two current paths.

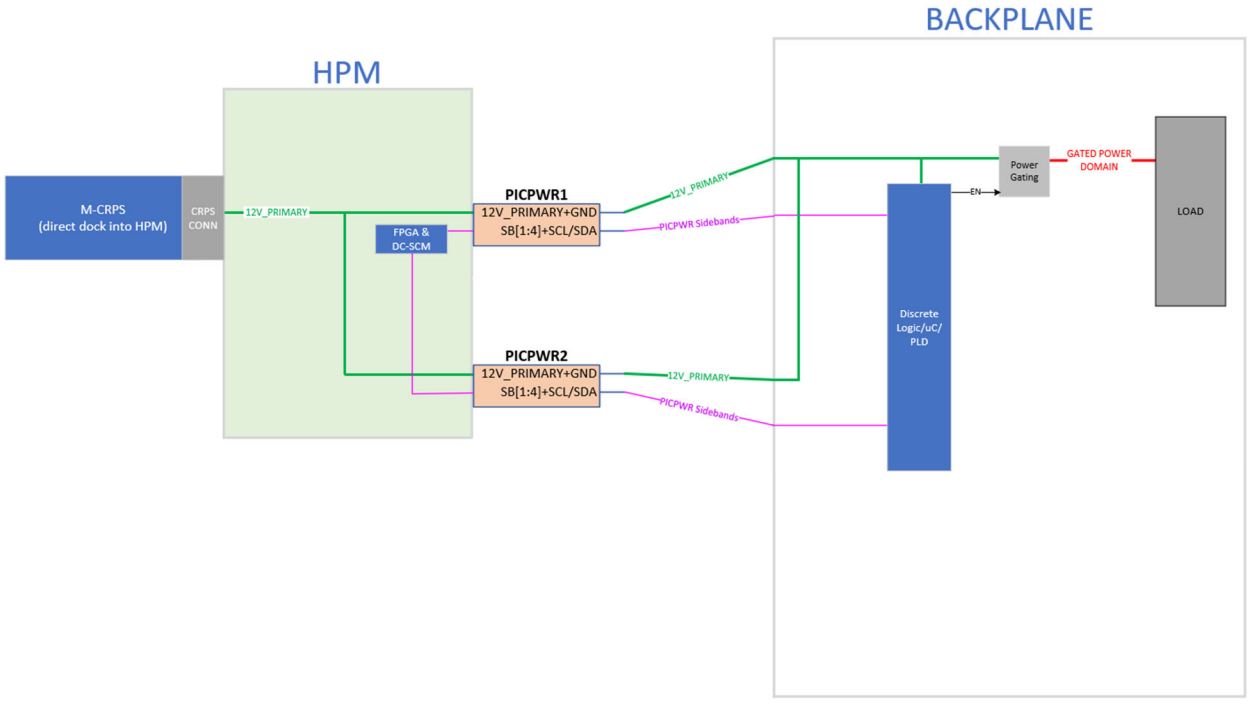


Figure 18: Multiple 12V PICPWR Connectors Powering a Single Peripheral Subsystem

8.1.8.3. 12V PICPWR Implementation in a PSU PDB Topology

In *Figure 19*, PSUs on a PDB provide power to the HPM through 12V PICPWR connectors. The HPM and the PSUs communicate all real-time control and status through the 12V PICPWR sideband and/or PDB management pins described in section **8.1.9**. PDB Management PMBus pins provide a mechanism for PMBus messages between the HPM and PSUs.

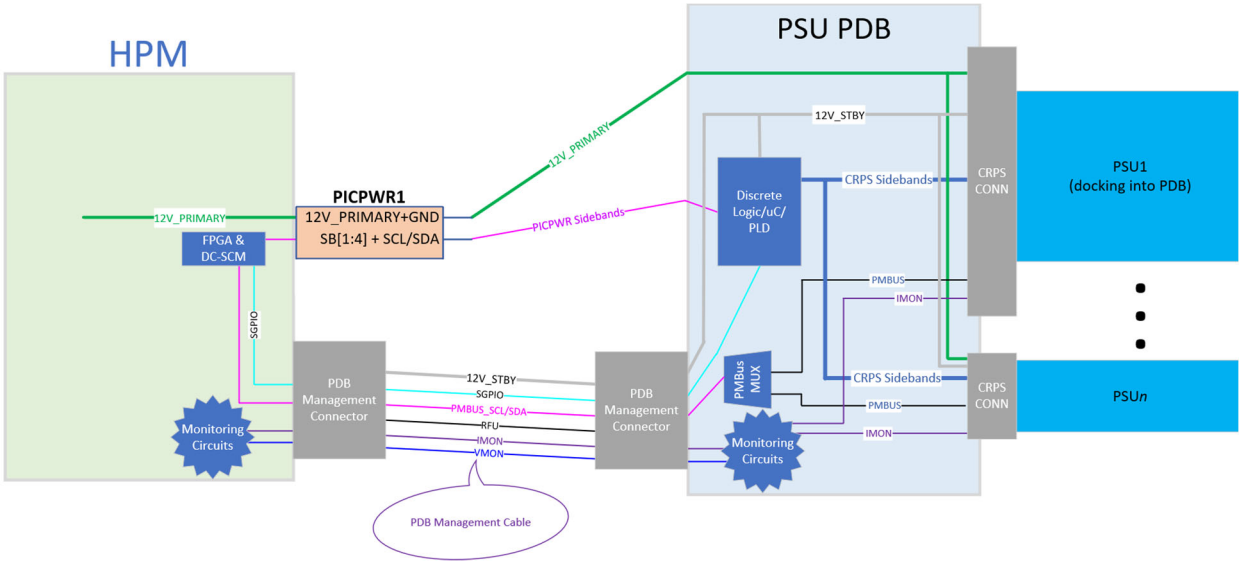


Figure 19: Power Supplies through a PDB

8.1.9. PDB Management Connector

This section defines a connection for HPMs used with a PDB. This connector provides +12VStby to the HPM, analog connections used to monitor current and voltage from the M-CRPS modules on the PDB, and management signals for PDB.

Table 10: PDB Management Connector Pin Definition

Signal Name	Description	Spec	Notes
12V_STBY	12V Standby Management Power	12V +/-5% Up to 6 Amps	
IMON	Shared current monitor signal that represents the total output current for all shared power supplies.	Refer to *Table 19*	
VMON	Voltage Monitor output signal from PDB circuit.		
GND	Ground return for 12V_PRIMARY and side-band signals	Up to 6 Amps	
SLoad	SGPIO Load Signal to PDB	Refer to section **8.11.6** for SGPIO electrical requirements and protocol.	The SGPIO interface provides a low latency path from HPM to PDB for IO expansion on PDB.
SDataOut	SGPIO Data signal from HPM to PDB		
SDataIn	SGPIO Data signal from PDB to HPM		
SClock	SGPIO Clock to PDB		

PMBUS_SCL PMBUS_SDA	PMBus from DC-SCM BMC for PSU Management/updates.	See section **8.11.3** for PMBus electrical requirements.	The PMBus interface does not support I3C.
RFU	Reserved for Future Use – do not connect		

Table 11: PDB Management Connector Pinout

Pin	Signal Name	Signal Name	Pin
A01	+12V_STBY	+12V_STBY	B01
A02	IMON	VMON	B02
A03	+12V_STBY	+12V_STBY	B03
A04	GND	GND	B04
A05	SLoad	SClock	B05
A06	SDataOut	GND	B06
A07	GND	SDataIn	B07
A08	PMBUS_SCL	GND	B08
A09	PMBUS_SDA	RFU	B09

Refer to *Figure 20* for 2x9 vertical PDB Management Connector physical pinout.

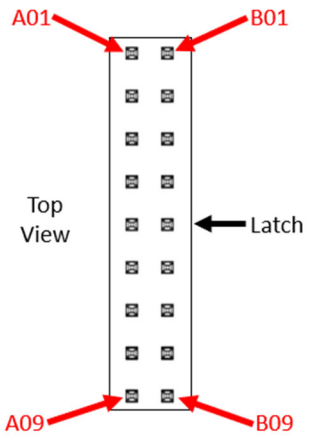


Figure 20: 2x9 Vertical PDB Management Connector Physical Pinout

2x9 Vertical Header

Notes:

- Connector current rating: 2A per contact
- Refer to documentation of connector vendors and part numbers located at: DC-MHS Connector Information @ https://drive.google.com/drive/folders/1sURGb6UQ7pzr48_0RnXanBGqgC2a4EA4
-

8.2. Boot Storage

This section defines an optional cable optimized interface for a boot/storage peripheral and two options for direct attach boot storage. This subsystem is typically implemented as 1 or 2 M.2 media devices or similar, and often with a RAID 1 controller. PCIe generational/speed requirements are not provided.

8.2.1. Cable Optimized Boot Peripheral

If present, the cable optimized peripheral interface is comprised of a dedicated connector with optimized power, signals, and connector form factor to work in FLW and DNO form factors. The interface does not include the PICPWR signals because the power is switched on the HPM. Multiple HPMs sharing a single boot storage peripheral is outside the scope of this specification.

Refer to *Table 12* for the boot optimized connector pin definitions.

Table 12: Boot Optimized HPM Connector Pin Definition

Signal Name	Description	Spec	Notes
12V	12V (HPM controlled)	12V +/-5% Up to 25W	The power switch shall be located on the HPM.
GND	Ground return for 12V and signals		
3p3_AUX_MGMT	3.3V Aux powered. Available from S5.	Up to 200 mA (if provided)	This connection is optional. EDSFF devices are limited to 25 mA.
PETp0, PETn0 PETp1, PETn1 PETp2, PETn2 PETp3, PETn3	Root Port TX signals	Defined by the PCI Express Card Electromechanical Specification.	Support x1, x2, or x4 configurations
PERp0, PERn0 PERp1, PERn1 PERp2, PERn2 PERp3, PERn3	Root Port RX signals	Defined by the PCI Express Card Electromechanical Specification.	Support x1, x2, or x4 configurations
REFCLK_Dp0, REFCLK_Dn0	100 MHz PCIe reference clock	Defined by PCIe Base Specification.	
PERST0_N	PCIe fundamental reset to the device.	Defined as PERST# by the PCI Express Base Specification.	
REFCLK_Dp1, REFCLK_Dn1	100 MHz PCIe reference clock	Defined by PCIe Base Specification.	Used only if DUALPORTEN_N IS LOW
PERST1_N	PCIe fundamental reset to the device.	Defined as PERST# by the PCI Express Base Specification.	Used only if DUALPORTEN_N IS LOW
PESTI_PRES_N / PRSNT0_N	Peripheral Presence detection signal with the option for PESTI	This signal shall be connected to HPM FPGA with the	

	communication with the peripheral.	prescribed terminations for PICPWR_SB1. For electrical requirements see section **8.11.1**, Table 3, and *Figure 6*.	
SMB_SCL, SMB_SDA	SMBus management interface	See section **8.11.2**. for SMBus electrical requirements.	
SMBRST_N	SMBus reset	Defined by the SFF-TA-1009 Rev 3.0 Specification.	Reset for the management interface.
DUALPORTEN_N	Dual port enable signal	Defined by the SFF-TA-1009 Rev 3.0 Specification.	
LED	LED signal	Defined by the SFF-TA-1009 Rev 3.0 Specification.	
PWRDIS (Power Disable)	Power Disable Signal	Defined by the SFF-TA-1009 Rev 3.0 Specification.	
FLEXIO	Non-EDSFF device flexible use signal	Shall be connected to HPM FPGA without external PU or PD and in a no bias state till after discovery is complete and use is negotiated. WARNING: Recommend to *not* wire this signal directly to an EDSFF device signal MFG, pin #B7. See SFF TA-1009 Rev 3.0 Specification for Device's MFG use.	Instead of making this pin a 'No Connect', it is connected to the HPM FPGA for proprietary use as desired by implementor Discovery and the mechanism of negotiation is out of the scope of this specification but could be done by either 2 wire management bus or 1 wire management bus.
RFU	Reserved for Future Use	Defined by the SFF-TA-1009 Rev 3.0 Specification.	

Figure 21: Rendering of Boot Optimized Connector

Notes:

- Connector current rating: >3ATBD per 3 power contact pins, 0.65A per differential pair contact, and 0.30A per single ended contact.
- Refer to documentation of connector vendors and part numbers located at: DC-MHS Connector Information @ https://drive.google.com/drive/folders/1sURGb6UQ7pzr48_0RnXanBGqgC2a4EA4
-

Table 13: Boot Optimized Connector Pinout

Pin	Signal Name	Signal Name	Pin
26	12V	GND	25
27	12V	GND	24
28	12V	GND	23
29	FLEXIO	SMB_SCL	22
30	RFU	SMB_SDA	21
31	DUALPORTEN_N	SMBRST_N	20
32	PERST0_N	LED	19
33	3.3V AUX	PERST1_N	18
34	PWRDIS	PESTI_PRES_N / PRSNT0_N	17
35	GND	GND	16
36	REFCLKn0	REFCLKn1	15
37	REFCLKp0	REFCLKp1	14
38	GND	GND	13
39	PETn0	PERn0	12
40	PETp0	PERp0	11
41	GND	GND	10
42	PETn1	PERn1	9
43	PETp1	PERp1	8

44	GND	GND	7
45	PETn2	PERn2	6
46	PETp2	PERp2	5
47	GND	GND	4
48	PETn3	PERn3	3
49	PETp3	PERp3	2
50	GND	GND	1

Refer to *Figure 22* for boot optimized connector physical pin numbering.

<<<PLACEHOLDER >>>

Figure 22: Boot Optimized Connector Physical Pin Numbering

8.2.2. Direct Attach Boot Storage

HPMs may implement an integrated boot storage subsystem directly on the HPM.

8.2.2.1. M.2 Direct Attach Boot Storage

If M.2 direct connect storage media is implemented on HPM, it shall be a right-angle Socket 3 (Mechanical Key M) connector following the PCI Express M.2 Specification Revision 4.0, Version 1.0 pinout. HPMs may optionally connect from HPM FPGA to M.2 connector pin 1 with a pull-up to 3.3V Aux (Available from S5) for M.2 device presence detection.

8.2.2.2. E1.S Direct Attach Boot Storage

If E1.S direct connect storage media is implemented on HPM, it shall be a right-angle SFF-TA-1002 connector following SFF-TA_1009 Rev 3.0 pinout.

8.3. Intrusion Switch

HPM form-factors supporting an intrusion switch shall be implemented as follows:

1. 1x3 Vertical header
   - Refer to documentation of connector vendors and part numbers located at: DC-MHS Connector Information @ https://drive.google.com/drive/folders/1sURGb6UQ7pzr48_0RnXanBGqgC2a4EA4

2. The signal HPM_SCM_INTRUSION_N is routed directly between header and DC-SCM without other circuit connectivity. Polarity of the HPM_SCM_INTRUSION_N has an active low indicating intrusion.
3. Presence-detect signal routed to HPM's FPGA
4. Electrical details of HPM_SCM_INTRUSION_N are defined in the DC-SCM 2.0 specification.

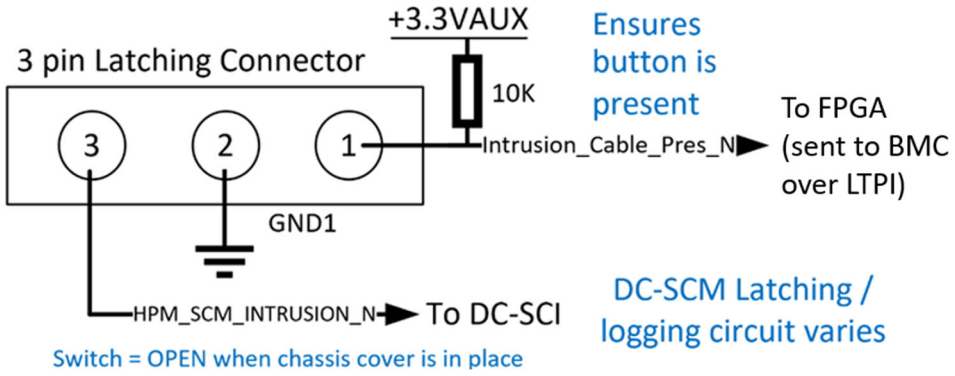


Figure 23: Intrusion Switch Pinout and Connectivity

Refer to *Figure 24* for intrusion switch header physical pin numbering.

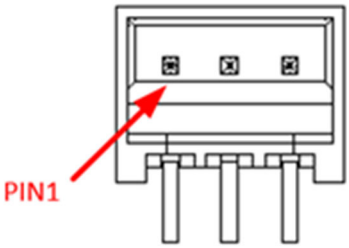


Figure 24: Intrusion Switch Header Physical Pin Numbering

8.4. Internal Host USB3 Connector

If the HPM includes only one internal host USB3.1 connector (Internal port), it shall be either a vertical type A or vertical type C connector. Type A is strongly recommended to achieve maximum modularity. Refer to *Figure 25* for an example of Host and BMC managed USB connectivity.
Usage examples include Control Panel expansion, debug, or an Internal key. Physical presence, location, and envelope / keep out of the attached device or cable exit are to be defined by individual HPM form factor specifications. Additional USB connectors located on the HPM are outside the scope of this specification.

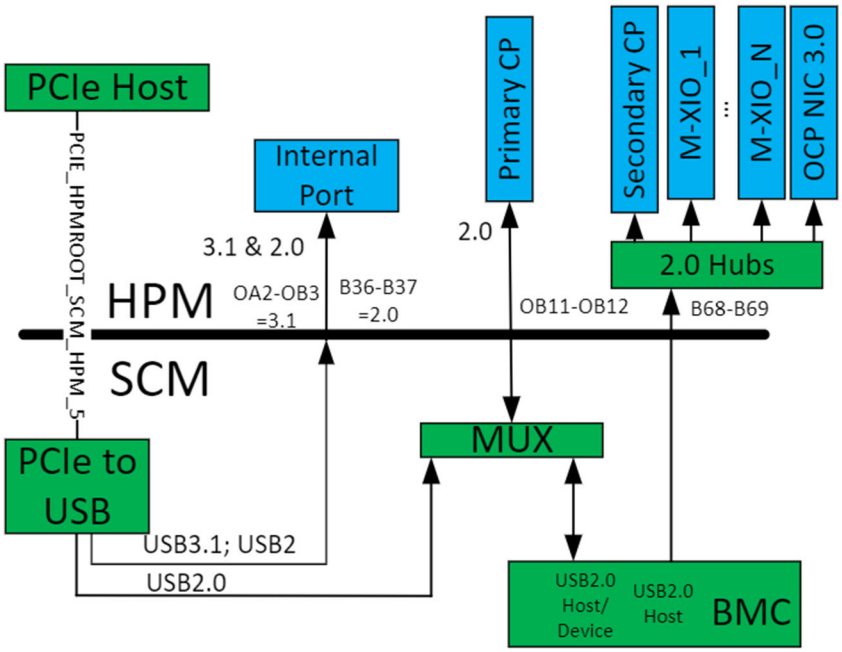


Figure 25: Example High Level USB Diagram

8.5. Control Panel Interfacing

The primary function of a control panel is to enable users to interact with the system while they are physically present in front of the chassis. If the HPM form-factor includes a single control, then it shall be the primary control panel (PCP) connector. If an HPM form-factor includes two control panels, the additional control panel shall be the secondary control panel (SCP) connector. Connecting multiple HPMs to a single control panel is outside the scope of this specification.

Additional buses or signals may be sourced from DC-SCM hosted connectors. For example, if front VGA or display port feature is added to the system, it could be sourced from the DC-SCM.

If USB3 is required in one or more control panels, it may be cabled from the Internal USB3 connector on the HPM described in section **8.4**.

Table 14: Primary HPM Control Panel Pin Definition

Signal Name	Description	Spec	Notes
12V_CP GND	Control Panel Power S5 available power distribution	12V +/-8%, Up to 200mA before 12V_PRIMARY is sourced by +12V. Up to 1.4A after 12V_PRIMARY is sourced by +12V.	12V_CP shall be derived from raw CRPS +12VStby but switched to +12V when it's available. It could also be shared with other subsystems. Overcurrent protection for 12V_CP is recommended to prevent shorts from being passed to

			+12VStby and management subsystems.
[SMB/I3C]_BMC_SDA/SCL	From DC-SCM BMC	3.3V Aux powered. Available from S5. See section **8.11.2** for SMBus and I3C electrical requirements.	Used for Temp sensor, and/or other SMBus devices
PCP_SB[4:1]	From HPM FPGA for GPIO expansion on Control Panel	Use the same HPM topology, termination, and values as PICPWRn_SB[4:1] See section **8.11.1** for electrical requirements See *Figure 6* for topology	Sideband GPIOs for status, control, inventory, and/or other control panel functions shall be connected to HPM FPGA with prescribed terminations for “Plug-N-Code” specific usages. The Plug-N-Code connectivity also enables the PESTI interface described in the M-PESTI specification. To maximize commonality between peripherals, it is recommended to use PCP_SB1 for PRES_N or PESTI functionality and use PCP_SB2 as active high PWREN (power enable) functionality.
USB_PCP_DP/DN	One USB 2.0 combo (SCMOTG/HPM HOST) connection from DC-SCM (pins OB11, OB12).	See section **8.11.4** for electrical requirements Refer to *Figure 25* for Host USB high level DC-SCM to HPM USB connectivity.	Potential use cases: boot key, service port, keyboard, or mouse. Expect a USB Hub on control panel for richer features. Video or USB3.0 would be fly over from enabled HPM
SPI	SPI bus from DS-SCM	≥33 MHz See section **8.11.1** for electrical requirements 3.3V_VAUX signaling (in S5)	Higher speed bus for devices such as SPI flash HPM shall be the SPI controller source where: MOSI is an output from HPM. MISO is an input to HPM.

8.5.1. Primary HPM to Control Panel connector

2x10 Vertical Header Notes:

- Connector current rating: 1A per contact
- Refer to documentation of connector vendors and part numbers located at: DC-MHS Connector Information @ https://drive.google.com/drive/folders/1sURGb6UQ7pzr48_0RnXanBGqgC2a4EA4
-

Table 15: Primary HPM Control Panel Pinout

Pin	Signal Name
1	12V_CP
3	12V_CP
5	NC
7	GND
9	USB2_PCP_DP
11	USB2_PCP_DN
13	GND
15	MISO
17	CS
19	MOSI

Signal Name	PIN
GND	2
[SMB/I3C]_BMC_SDA	4
[SMB/I3C]_BMC_SCL	6
GND	8
PCP_SB4	10
PCP_SB3	12
PCP_SB2	14
PCP_SB1	16
GND	18
CK	20

Refer to *Figure 26* for control panel header physical pin numbering.

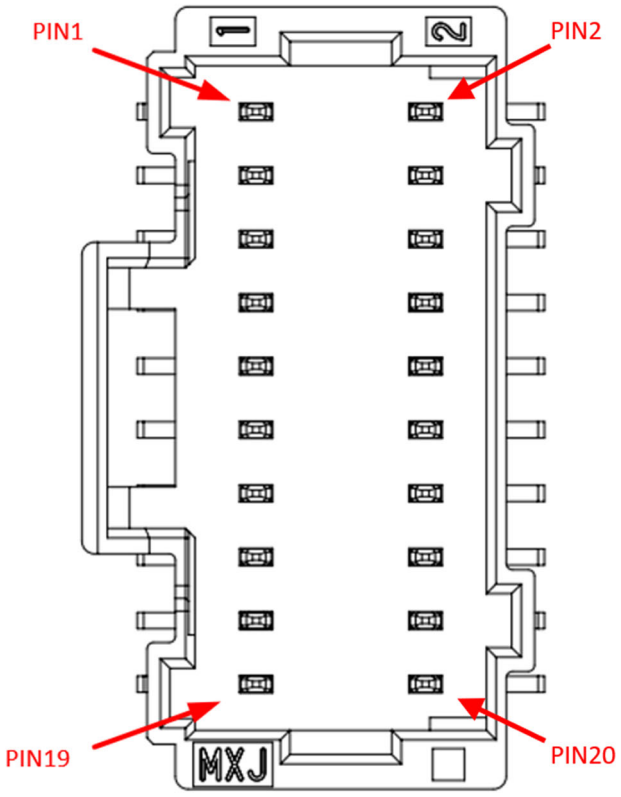


Figure 26: Control Panel Header Physical Pin Numbering

Table 16: Secondary HPM Control Panel Pin Definition

Signal Name	Description	Spec	Notes
P12V_CP GND	Control Panel Power S5 available power distribution	12V +/-8%, Up to 200mA before 12V_PRIMARY is sourced by +12V. Up to 1.4A after 12V_PRIMARY is sourced by +12V.	12V_CP shall be derived from raw CRPS +12VStby but switched to +12V when it's available. It could also be shared with other subsystems. Overcurrent protection for 12V_CP is recommended to prevent shorts from being passed to +12VStby and management subsystems.
[SMB/I3C]_BMC_SCP_SDA/SCL	From DC-SCM BMC	3.3V powered. Available from S5. See section **8.11.2** for SMBus and I3C electrical requirements.	Used for Temp sensor, and/or other SMBus devices

SCP_SB[4:1]	From HPM FPGA for GPIO expansion on Control Panel	Use the same HPM topology, termination, and values as PICPWRn_SB[4:1] See section **8.11.1** for electrical requirements See *Figure 6* for topology	Sideband GPIOs for status, control, inventory, and/or other control panel functions shall be connected to HPM FPGA with prescribed terminations for "Plug-N-Code" specific usages. The Plug-N-Code connectivity also enables the PESTI interface described in the M-PESTI specification. To maximize commonality between peripherals, it is recommended to use SCP_SB1 for PRES_N or PESTI functionality and use SCP_SB2 as active high PWREN (power enable) functionality.
USB_SCP_DP/DN	One BMC USB2.0 host connection from DC-SCM (pins OB11, OB12) through USB2.0 hubs(s).	See section **8.11.4** for electrical requirements Refer to *Figure 25* for Host USB high level DC-SCM to HPM USB connectivity.	Potential use cases: boot key, service port, keyboard, or mouse. Expect a USB Hub on control panel for richer features. Video or USB3.0 would be fly over from enabled HPM
RFU_[1:4]	RFU pins	Shall not be Connected	Reserved for Future Use

8.5.2. Secondary HPM to Control Panel Connector

2x10 Vertical Header

Notes:

- Connector current rating: 1A per contact
- Refer to documentation of connector vendors and part numbers located at: DC-MHS Connector Information @ https://drive.google.com/drive/folders/1sURGb6UQ7pzr48_0RnXanBGqgC2a4EA4
-

Table 17: Secondary HPM Control Panel Pinout

Pin	Signal Name
1	12V_CP
3	12V_CP

Signal Name	Pin
GND	2
[SMB/I3C]_BMC_SDA	4

5	NC	[SMB/I3C]_BMC_SCL	6
7	GND	GND	8
9	USB2_SCP_DP	SCP_SB4	10
11	USB2_SCP_DN	SCP_SB3	12
13	GND	SCP_SB2	14
15	RFU_1	SCP_SB1	16
17	RFU_2	GND	18
19	RFU_3	RFU_4	20

Refer to *Figure 26* for control panel header pin numbering.

8.6. TPM

If using a single node configuration with a single DC-SCM, then the TPM used shall be located on the DC-SCM. Other configurations are outside the scope of this specification because the DC-SCI (Data Center ready Secure Control Interface) lacks the interface for more than one TPM. Placement or mechanical aspects are outside the scope of this specification.

8.7. OCP NIC 3.0

See HPM form factor specifications for guidance on explicit OCP NIC variations supported (SFF, LFF, hot plug supported, etc.).

8.8. Smart NIC Management Interface

DC-MHS supports the option to interface with DPU/Smart NIC/IPU devices using BMC USB2.0 host controller signals through the M-XIO. See *Figure 25* for USB high level DC-SCM to M-XIO USB connectivity. Refer to the M-XIO base specification for details.

8.9. Coin Cell Battery

A CR2032 system coin cell battery shall reside on the HPM. The coin cell battery holder shall be compatible with a CR2032 battery. Orientation of the connector coin cell battery holder is outside the scope of this specification.

8.10. DC-SCM Revision

DC-MHS is defined using the features and the form factor of DC-SCM revision 2.0. Use of DC-SCM revision 1.0 is outside the scope of this specification.

Note: Even though DC-SCM doesn’t require a new interface for HPM discovery, it is important for HPM designers to consult the DC-SCM revision 2.0 specification for HPM discovery logic requirements.

8.11. Electrical Requirements

The destination subsystem is responsible for 1) electrical protection of local circuitry if the peripheral/subsystem is unpowered, 2) any cross-power domain isolation (such as when connecting MAIN powered only targets to the upstream AUX powered bus) and 3) any necessary voltage level translation in SMBus mode.

8.11.1. 3.3V Signaling Requirements

The 3.3V single-ended digital signals (PICPWRn_B/A_SB[4:1], [P/S]CP_SB[4:1] , INTRUSION_CABLE_PRES_N, PESTI_PRES_N / PRSNT0_N, and SPI) are defined in *Table 18*.

Table 18: 3.3V Logic Signal Requirements

Parameter	Symbol	Min	Max	Unit	Notes
High level input voltage	V_{IH}	2.0	3.465	V	
Low level input voltage	V_{IL}	-0.3	0.8	V	
High level output voltage	V_{OH}	2.3	3.465	V	
Low level output voltage	V_{OL}		0.2	V	
SPI High level input voltage	SPI V_{IH}	0.7 x VCC	VCC + 0.4	V	Care must be taken because SPI device VCC will have different sources.
SPI Low level input voltage	SPI V_{IL}	-0.3	0.8	V	
SPI High level output voltage	SPI V_{OH}	VCC – 0.2		V	
SPI Low level output voltage	SPI V_{OL}		0.4	V	Care must be taken because SPI device VCC will have different sources.

8.11.2. SMBus and I3C Signaling Requirements

SMBus, 3.3V, up to 400KHz or I3C Basic 1.1.1 mode, 1.8V, at higher speeds (I3C speeds vary based on overall topology and loading).

For SMBus signals (named with SCL or SDA) logic levels, refer to the System Management Bus (SMBus) Specification, Version 3.1.

For SMBus operation, a pullup to 3.3V shall be enabled. For I3C mode, the pullup shall be integrated in the I3C device upstream of the M-PIC defined connector, configurable (start at 3.3V then go to 1.8v), and transaction based.

For I3C signals (named with SCL or SDA) logic levels, refer to the I3C Basic 1.1.1 Specification.

8.11.3. PMBus Signaling Requirements

PMBus, 3.3V, up to 400KHz.

For PMBus signals (named with SCL or SDA) logic levels, refer to the System Management Bus (SMBus) Specification, Version 3.2.

For PMBus operation, a pullup to 3.3V shall be provided.

PMBus does not support I3C mode.

8.11.4. USB Signaling Requirements

For USB, reference Universal Serial Bus Specification. Inputs and outputs are referenced from the signal destination's standpoint.

8.11.5. Imon and Vmon Signaling Requirements

Refer to *Table 19* for Imon and Vmon analog signaling requirements.

Table 19: Imon and Vmon Voltage Signaling Requirements

Parameter	Min	Max (compliance mode)	Max (open circuit)	Unit	Notes
Analog Voltage Range	0	10.5	12.6	V	

8.11.6. SGPIO Requirements

This section describes signaling requirements for the low latency SGPIO interface between the HPM FPGA (initiator) and the PDB FPGA (target) if the HPM supports a PDB. The SGPIO interface is used for IO expansion on PDB.

8.11.6.1. SGPIO Protocol

The SGPIO interface has dedicated push-pull data signals going to (SDataOut) and from (SDataIn) the PDB. Both data paths transmit data at the same time.

SLoad shall be a push-pull signal used to select the SGPIO target device and signal the start of the data transfer (starting with the first bit). When this signal is low, the SGPIO initiator and target shall clock out data. If the SLoad signal goes high before the data transfer is completed, then the transfer shall be aborted. When SLoad is high, the target data output shall be high impedance. If the data transfer is complete and the SLoad signal is still low, the data sent shall all be "1b". Data is clocked in on the falling edge of SClock.

SClock shall be a push-pull signal used as the reference clock for the SGPIO interface. Because the latency between transactions depends on the total number of bits per transaction and the clock frequency, the SClock frequency shall be 25 MHz to provide flexibility for PDB designs.

Refer to *Figure 27* for an example SGPIO transaction waveform.

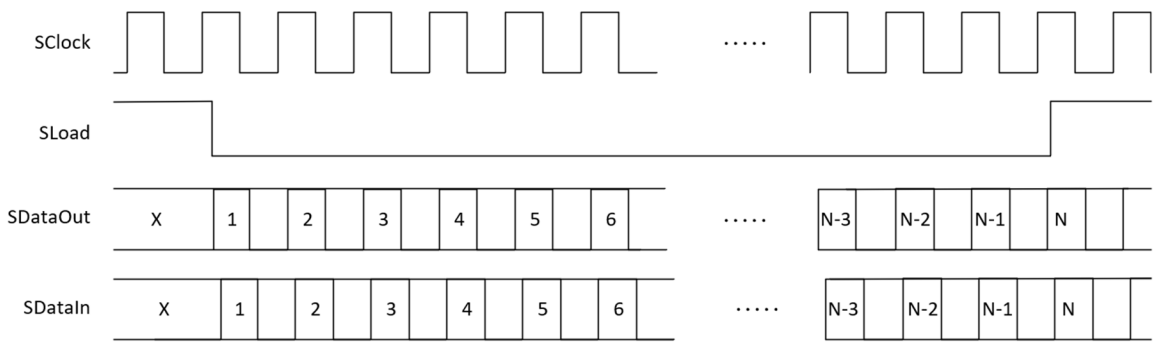


Figure 27: Example SGPIO Transaction Waveform

Refer to *Table 20* for HPM passive interconnect requirements.

Table 20: HPM Passive Interconnect Requirements

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Skew between SClock and SLoad, SDataOut, and SDataIn signal lines on HPM	T_{SKEW}	-	10	ps	

SGPIO signaling levels shall be compatible with 3.3V LVCMOS technology. Refer to *Table 21* for electrical characteristics of the SGPIO transmitters and receivers.

Table 21: Transmitter and Receiver Electrical Requirements

Parameter	Symbol	Minimum	Maximum	Unit	Notes
IO Voltage	$V_{CC\ IO}$	3.135	3.465	V	
High level input voltage	V_{IH}	1.7	3.465	V	
Low level input voltage	V_{IL}	-0.3	0.8	V	
High level output voltage	V_{OH}	$V_{CC\ IO}$ -0.4	-	V	
Low level output voltage	V_{OL}	-	0.4	V	
IO Capacitance	$C_{I/O}$	-	8	pF	

Refer to *Table 22* for SGPIO timing requirements.

Table 22: SGPIO Timing Requirements

Parameter	Symbol	Minimum	Maximum	Unit	Notes
SClock Frequency	f_{CK}	5	25	MHz	HPM should designed to support $f_{CK\ MAX}$ but the system may operate at lower frequencies because of cable and PDB loading.

SClock Duty Cycle	t_{DUTY}	45	55	%	Measured at the midpoint between $V_{IH\ MIN}$ and $V_{IL\ MAX}$ of SClock
Rise time	t_R	-	6	ns	Measured from $V_{IL\ MAX}$ to $V_{IH\ MIN}$.
Fall time	t_F	-	6	ns	Measured from $V_{IH\ MIN}$ to $V_{IL\ MAX}$.
Setup time	t_{SU}	0	-	ns	Measured from $V_{IL\ MAX}$ for SLoad, SDataOut, and SDataIn to the midpoint between $V_{IH\ MIN}$ and $V_{IL\ MAX}$ (on the falling edge) of SClock
Hold time	t_H	2	-	ns	Measured from the midpoint between $V_{IH\ MIN}$ and $V_{IL\ MAX}$ (on the falling edge) of SClock to $V_{IL\ MAX}$ for SLoad, SDataOut, and SDataIn

9. References

DC-MHS Family of Specifications

The Data Center – Modular Hardware System (DC-MHS) family of specifications are written to enable interoperability between key elements of datacenter and enterprise infrastructure by providing consistent interfaces and form factors among modular building blocks. At the time of this publication there are the following specification workstreams:

- **M-FLW** (**M**odular Hardware System **F**ull **W**idth Specification) – Host Processor Module (HPM) form factor specification optimized for using the full width of a Standard EIA-310 Rack mountable server. The specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-DNO** (**M**odular Hardware System Partial Width **De**n**s**ity **O**ptimized Specification) – Host Processor Module (HPM) specification targeted to partial width (i.e., ½ width or ¾ width) form factors. Such form factors are often depth challenged and found not only in enterprise applications but also in Telecommunications, Cloud and Edge Deployments. While the EIA-310 Rack implementation is chosen as a key test case for use, the specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-CRPS** (**M**odular Hardware System **C**ommon **R**edundant **P**ower **S**upply Specification) – Specifies the power supply solutions and signaling expected to be utilized by DC-MHS compatible systems.

- **M-PIC** (**M**odular Hardware System **P**latform **I**nfrastructure **C**onnectivity Specification) – Specifies common elements needed to interface a Host Processor Module (HPM) to the platform/chassis infrastructure elements/subsystems. Examples include power management, control panel and cooling amongst others.
- **M-XIO** (**M**odular Hardware System E**x**tensible **I**/**O**) – Specifies the high-speed connector hardware strategy. An M-XIO source connector enables entry and exit points between sources such as Motherboards, Host Processor Modules & RAID Controllers with peripheral subsystems such as PCIe risers, backplanes, etc. M-XIO includes the connector, high speed and management signal interface details and supported pinouts.
- **M**-**PESTI** (**M**odular Hardware System **Pe**ripheral **S**ideband **T**unneling **I**nterface) – Specifies a standard method for discovery of subsystems, self-describing attributes, and status (e.g., versus a priori knowledge/hard coding firmware and BIOS for fixed/limited configurations). Examples: vendor/module class, physical connectivity descriptions, add-in card presence, precise source to destination cable coupling determination.

To access additional DC-MHS specification please visit the OCP Server WIKI.

Additional References

This specification also relies on the following specifications

- OCP Server Network Interface Card (NIC) 3.0 – Specifies NIC card form factors targeting a broad ecosystem of NIC solutions and system use cases.
  Mezz (NIC) » Open Compute Project
- OCP Datacenter Secure Control Module (DC-SCM) Revision 2.0 – Specifies a DC-SCM designed to interface to an HPM to enable a common management and security infrastructure across platforms within a data center.
  Hardware Management/Hardware Management Module – Open Compute
- SMBus Management Interface Forum. System Management Bus (SMBus) Specification. System. Management Interface Forum, Inc, Version 3.1, 19 Mar 2018
- USB Implementers Forum. Universal Serial Bus Specification, Revision 2.0, April 27th, 2000
- MIPI alliance Specification for I3C Basic℠ v1.1.1 (9-Jun-2021)
- PCI-SIG®. PCI Express® Base Specification, Revision 5.0 May 28th, 2019
- PCI-SIG®. PCI Express® Card Electromechanical Specification, Revision 4.0, September 2nd, 2019
- SFF-TA-1009 specification for Enterprise and Datacenter Standard Form Factor Pin and Signal Specification Rev 3.0, March 19th, 2021.

10. Trademarks

Names and brands may be claimed as trademarks by their respective companies. I3C is a trademark of MIPI Alliance. PMBus name and logo are trademarks of SMIF, Incorporated. PCIe® and PCI Express® are the registered trademarks of PCI-SIG.

11. Supplement Material

Note: This section intends to move in the main document body when further refined by the workgroups after Release 1.0. The implementation is highly subject to change.

Placeholder for 48V PICPWR variant(s) and interconnects related to UBB 2.0

Appendix A - Checklist for IC approval of this specification (to be completed by contributor(s) of this Spec)

This will be filled out at v1.0

Complete all the checklist items in the table with links to the section where it is described in this spec or an external document.

Appendix B - OCP Supplier Information and Hardware Product Recognition Checklist

This is a base specification, and no specific designs can be derived from this specification. Future Design specs will be established based on MHS specifications, and supplier information and HW checklist will be applicable and filled in by future contributors