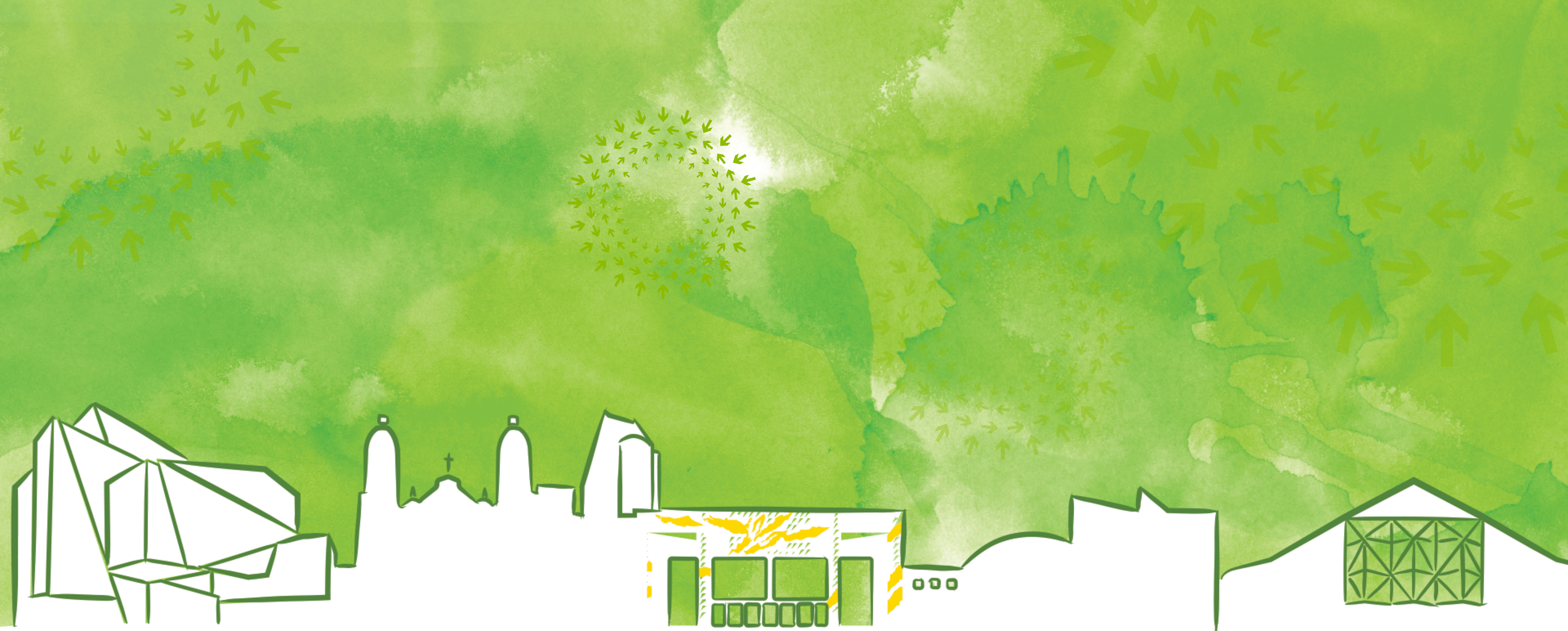




OCP U.S. SUMMIT 2016

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M.2 PCIe Carrier Card

Chris Petersen

HARDWARE SYSTEMS ENGINEER, FACEBOOK

Dominic Cheng

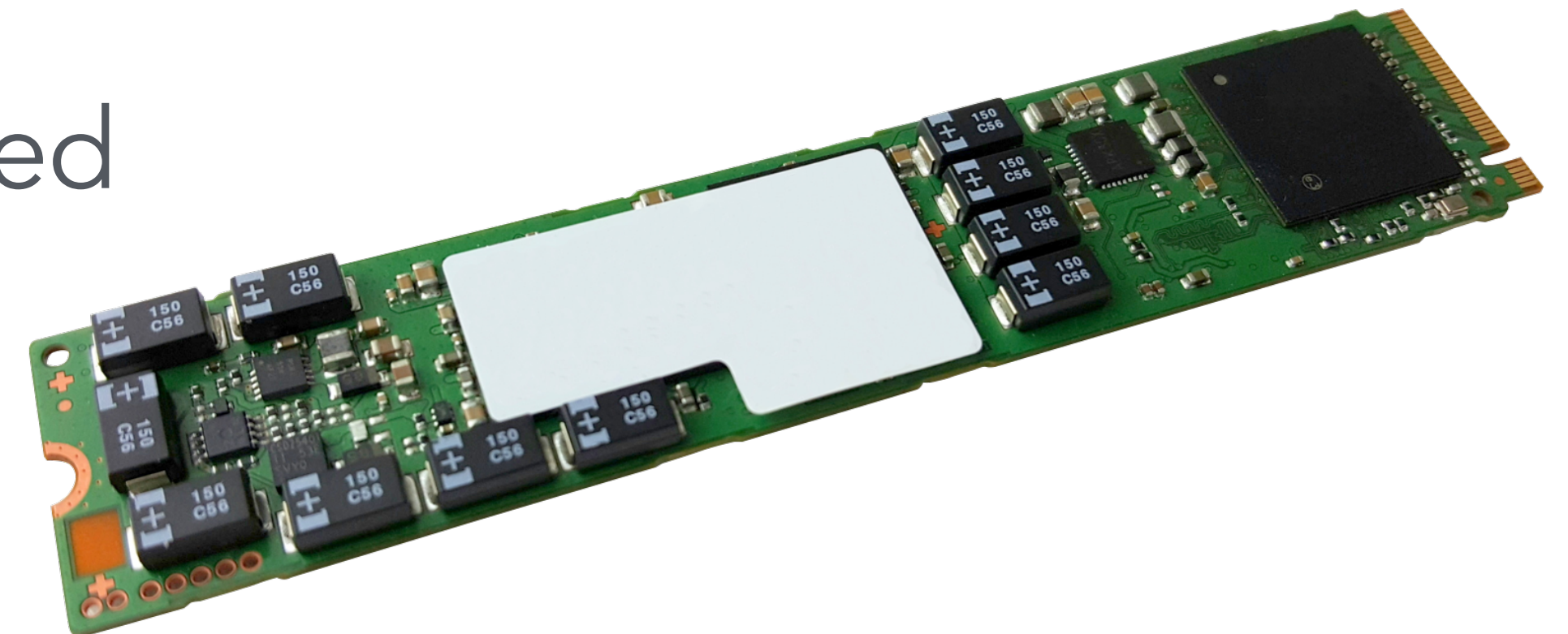
HARDWARE ENGINEER, FACEBOOK

Mark Shaw

HARDWARE ENGINEER, MICROSOFT

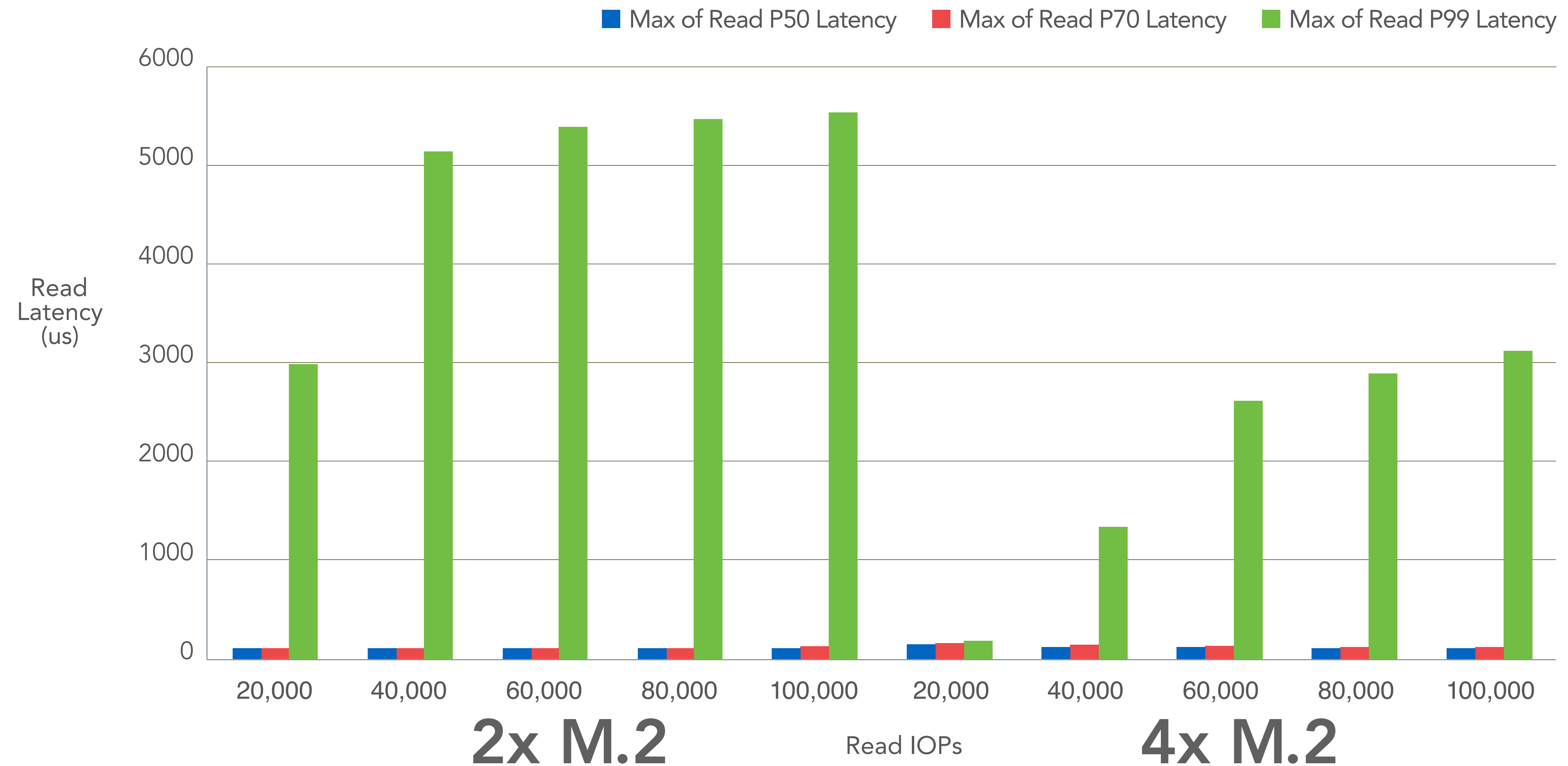
Why M.2?

- It is compatible with our storage and compute platforms
- M.2 is a commodity
- M.2 scales
- M.2 maximum capacity and power is limited



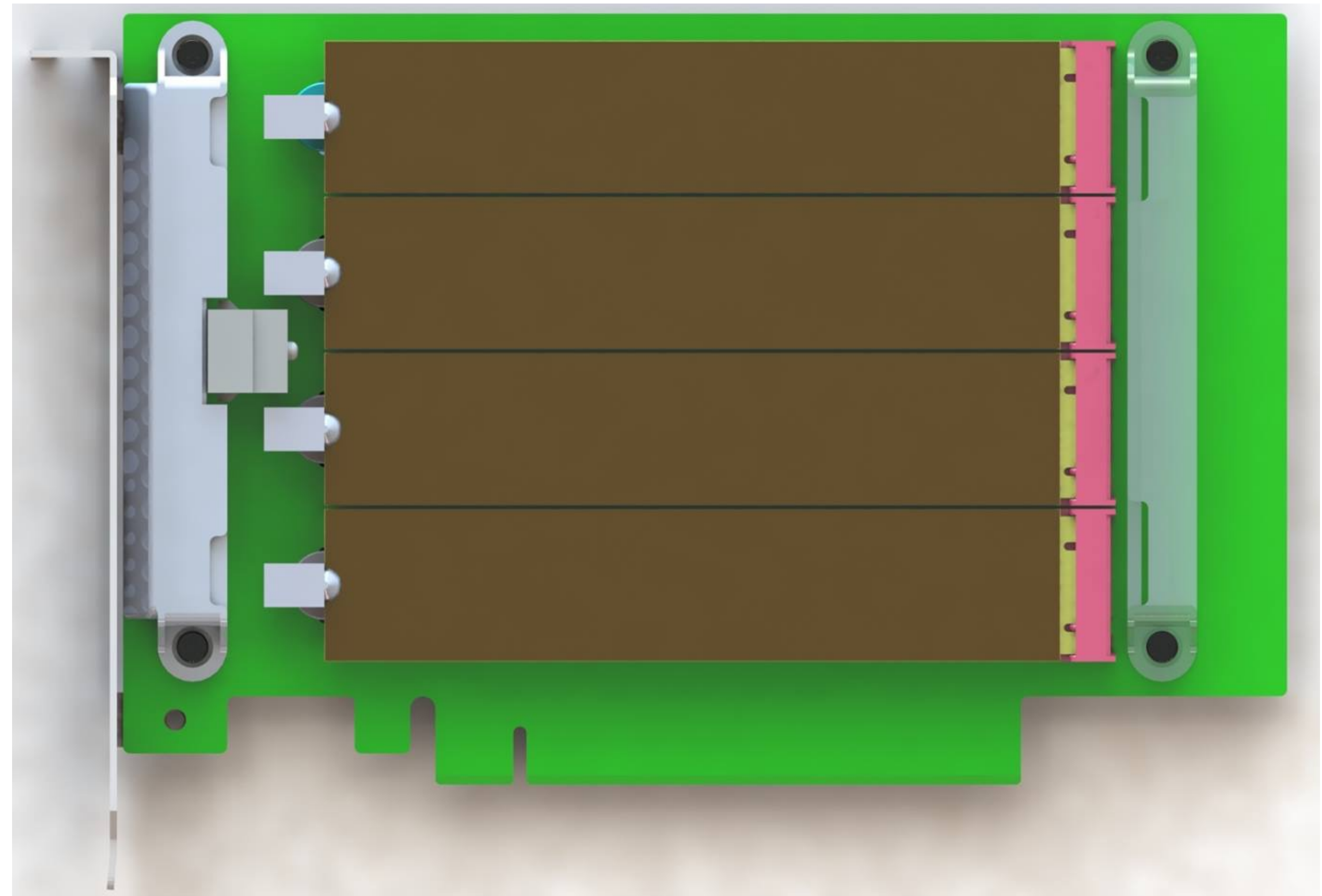
Performance

Preliminary



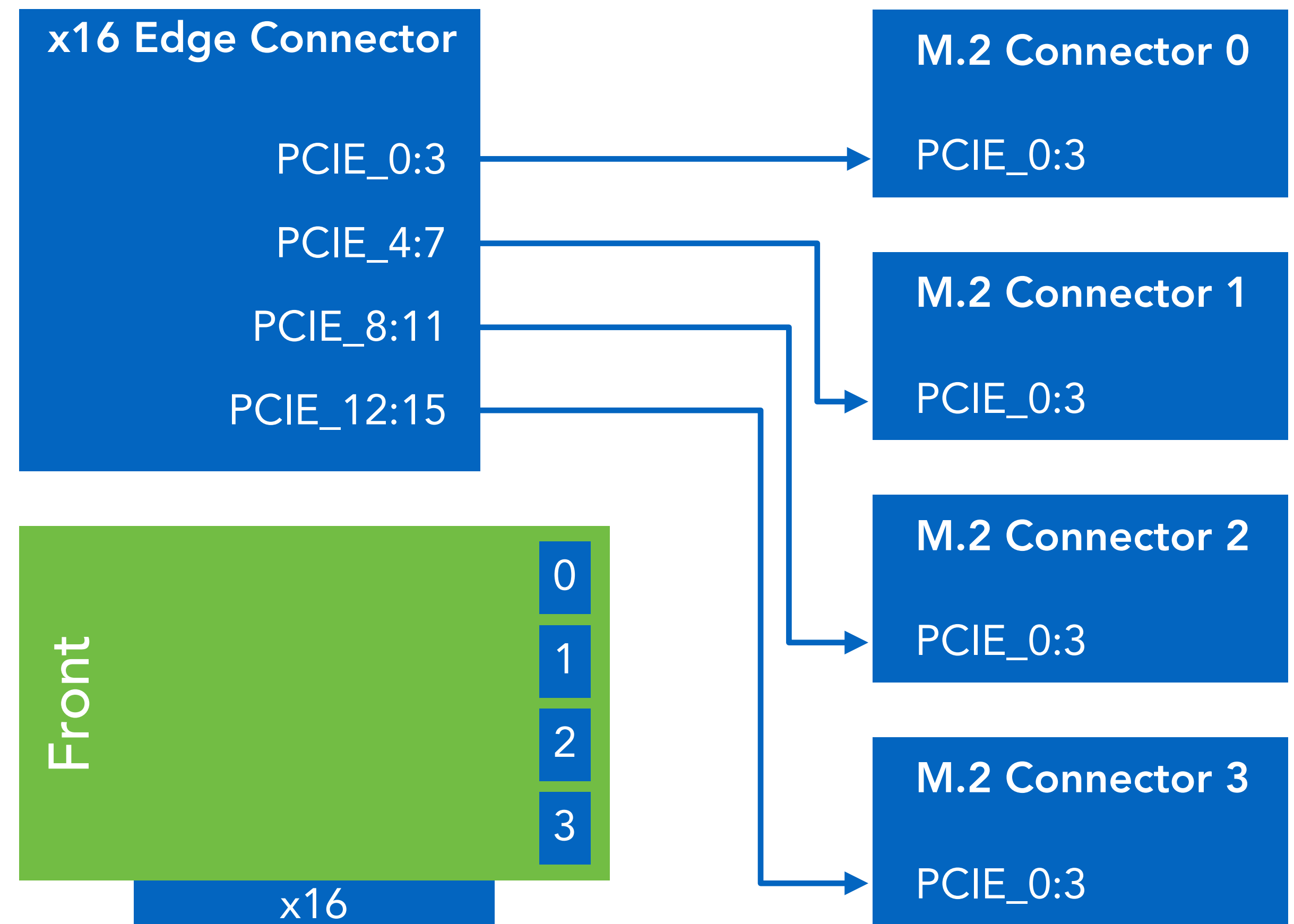
Design objectives

- No PCIe switches or re-drivers
- Future-proof
- Low cost
- PCIe FHHL CEM compliant



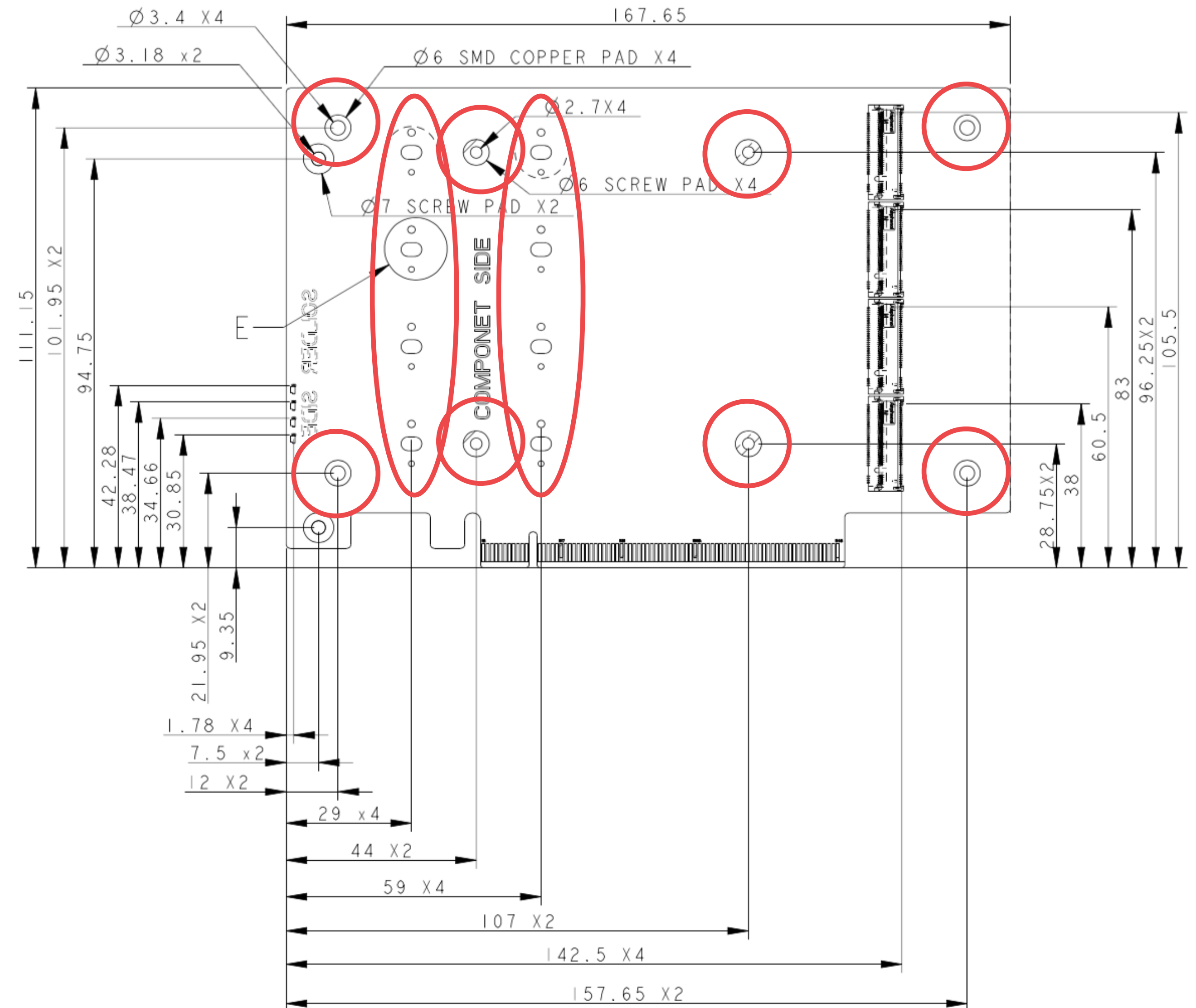
M.2 Carrier overview

- M.2 connector M-key and 5.8mm height
- Standard "Socket 3" pin-out plus SMBus ECN



Mechanical

- Mounting holes for top thermal solution
- Mounting holes for bottom thermal solution
- Mounting holes for M.2 2280
- Mounting holes for M.2 22110



M.2 device support

Attribute	Option 1	Option 2
Length	80mm	110mm
Top-side maximum thickness	3.1mm	3.1mm
Bottom-side maximum thickness	1.5mm	1.5mm
Power consumption	8.25W	14.85W

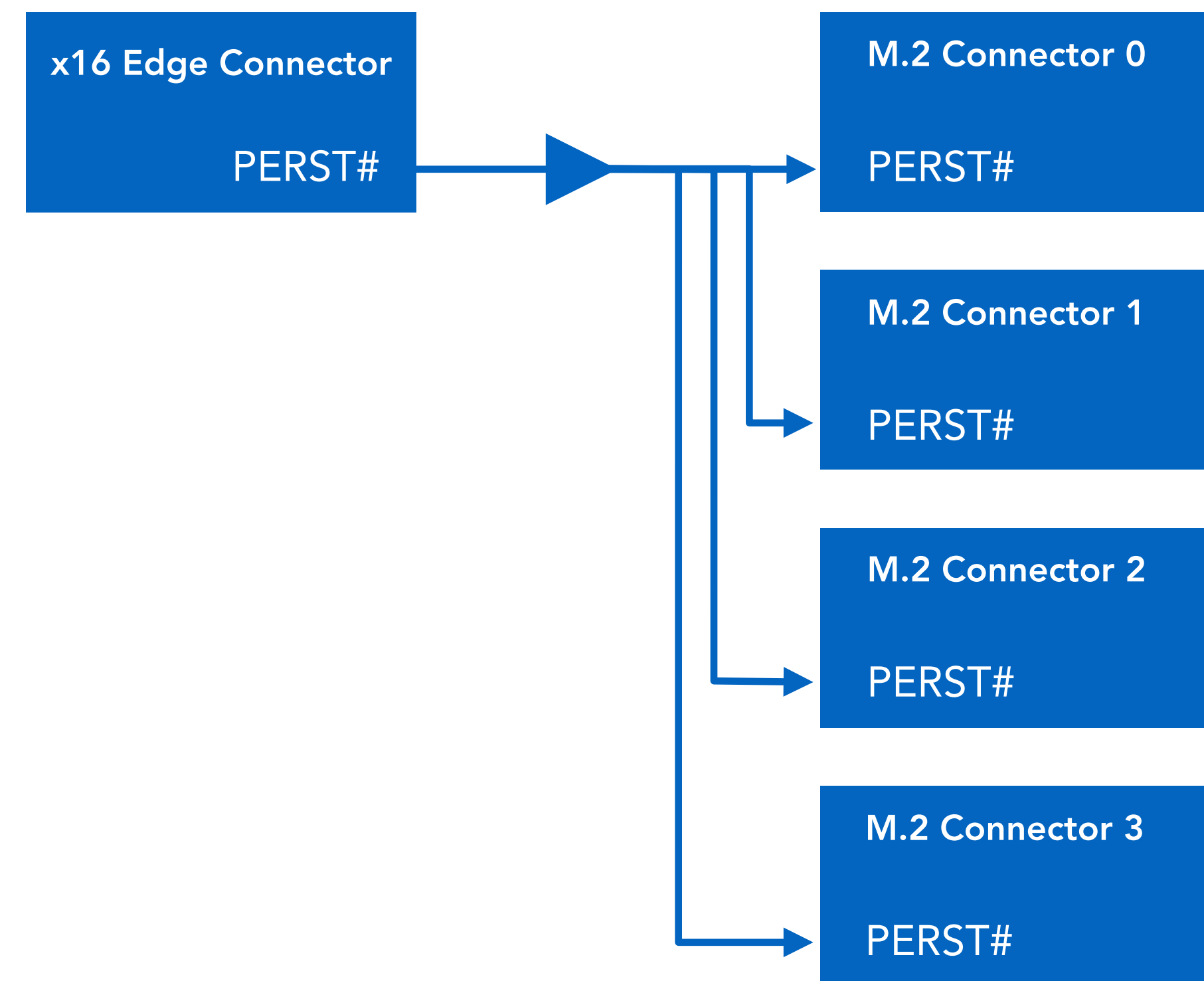
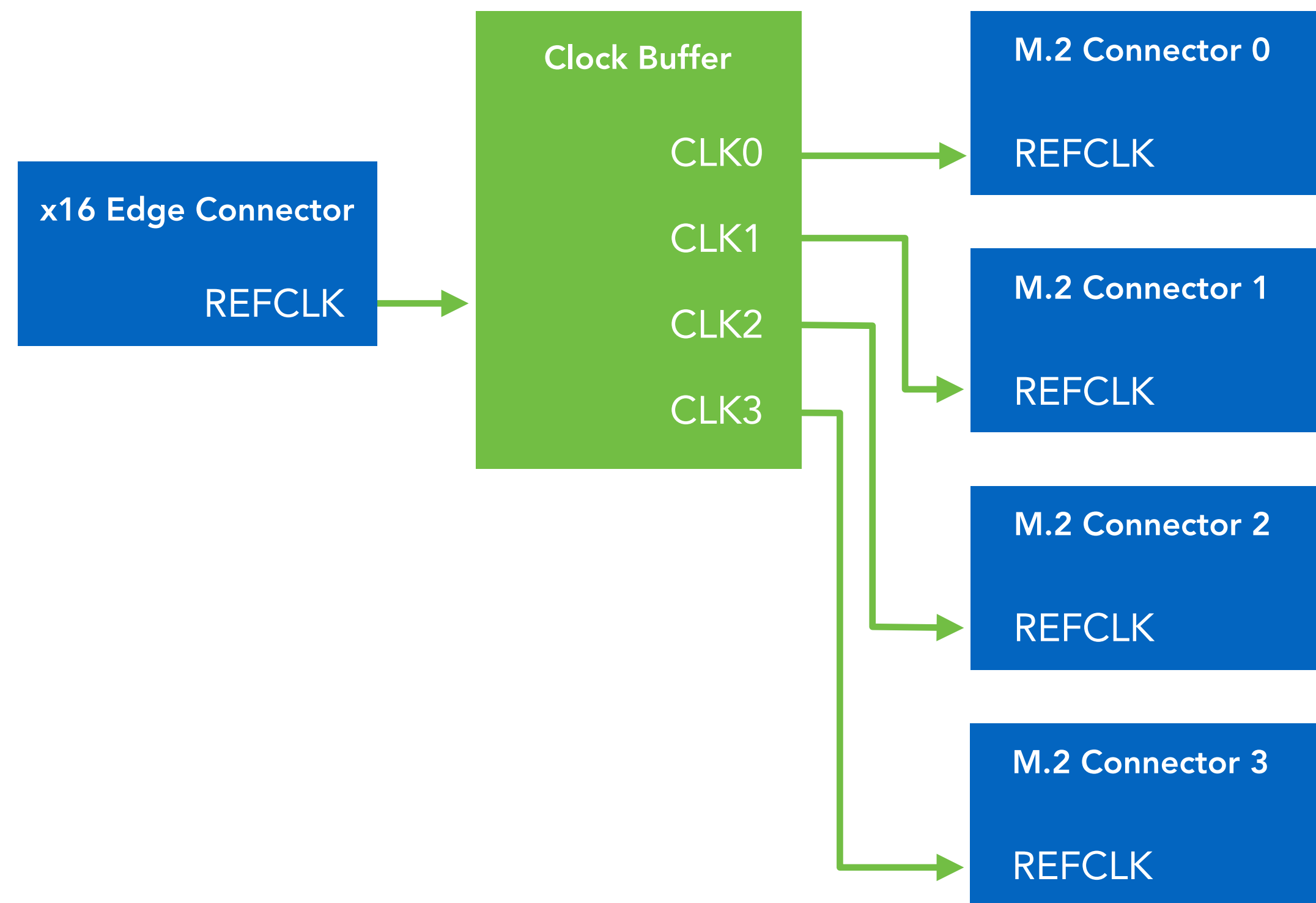
PCIe Bi-furcation

Four x4 configuration

- Pin B31 is pulled low on the card
- Pin B81 is connected to pin A1 on the card for presence detection
- All PRSNT#2 pins are routed to the PCH
- BIOS auto-detects if B31 + B81 is low

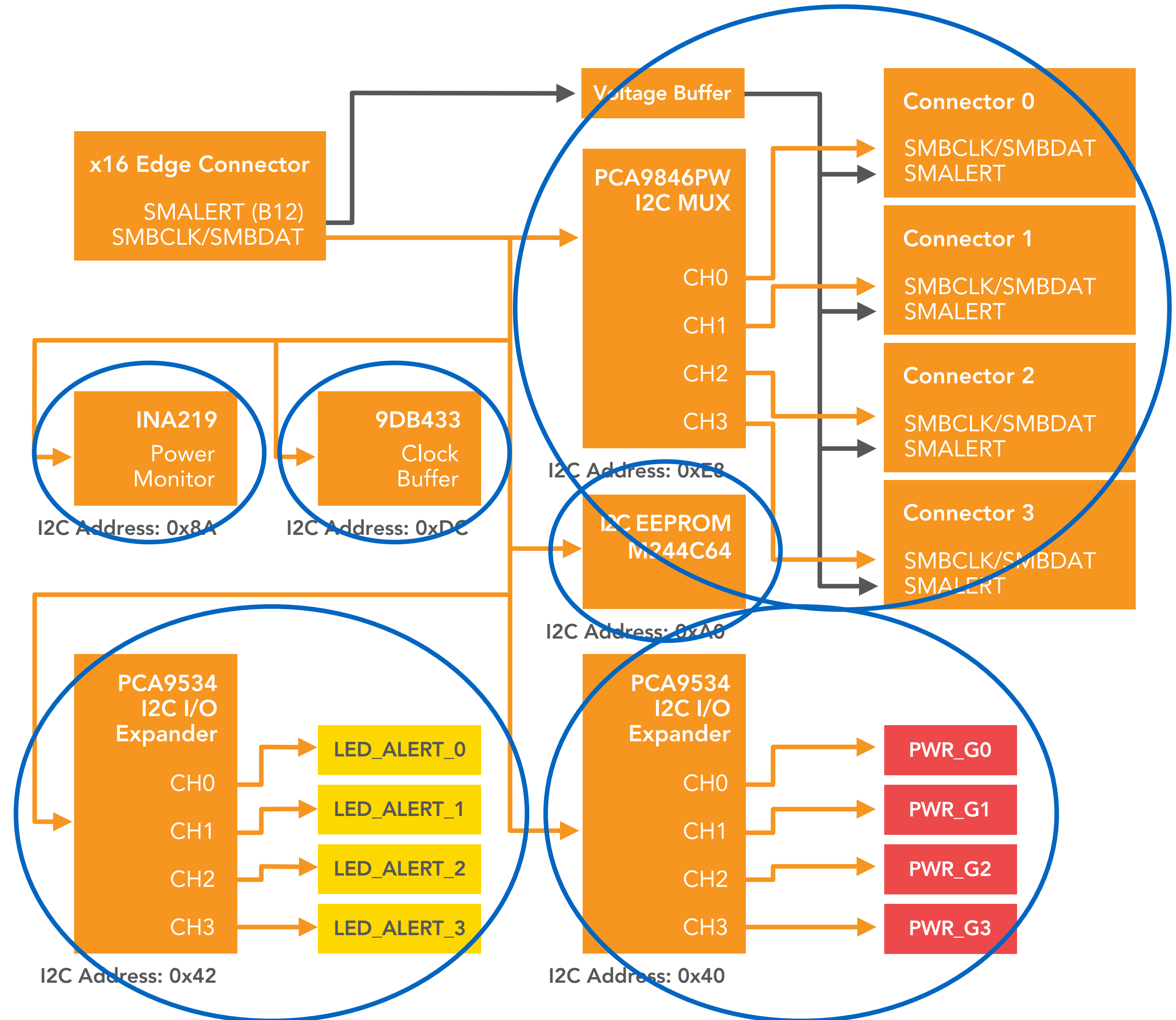
Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot-plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	+12v	+12 volt power	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	+3.3 volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PWRGD	Power Good
Mechanical Key				
12	SMBALERT#	Power Reduction	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock
14	PETP(0)	Transmitter Lane 0,	REFCLK-	Differential pair
15	PETN(0)	Differential pair	GND	Ground
16	GND	Ground	PERP(0)	Receiver Lane 0,
17	PRSNT#2	Presence detect	PERN(0)	Differential pair
18	GND	Ground	GND	Ground
19	PETP(1)	Transmitter Lane 1,	RSVD	Reserved
20	PETN(1)	Differential pair	GND	Ground
21	GND	Ground	PERP(1)	Receiver Lane 1,
22	GND	Ground	PERN(1)	Differential pair
23	PETP(2)	Transmitter Lane 2,	GND	Ground
24	PETN(2)	Differential pair	GND	Ground
25	GND	Ground	PERP(2)	Receiver Lane 2,
26	GND	Ground	PERN(2)	Differential pair
27	PETP(3)	Transmitter Lane 3,	GND	Ground
28	PETN(3)	Differential pair	GND	Ground
29	GND	Ground	PERP(3)	Receiver Lane 3,
30	PWRBRK#	Power Reduction	PERN(3)	Differential pair
31	BIFURx4	0 = PCIe x4 Bifurcation	GND	Ground

Clocks and reset



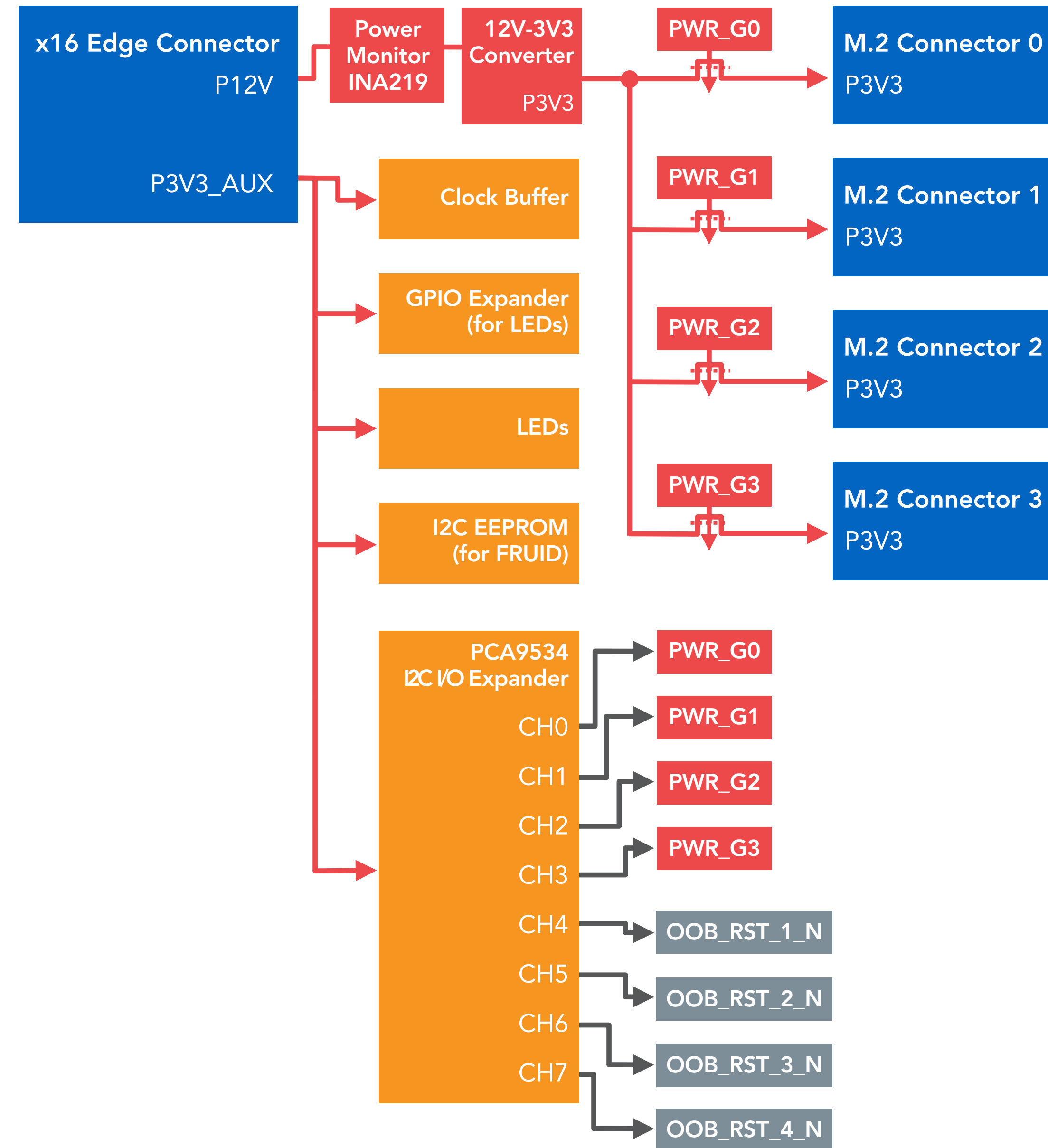
I2C/SMBus

- SMBus connection to each M.2
- FRU EEPROM
- Status LED control
- M.2 power/reset control
- Power monitor
- Clock buffer



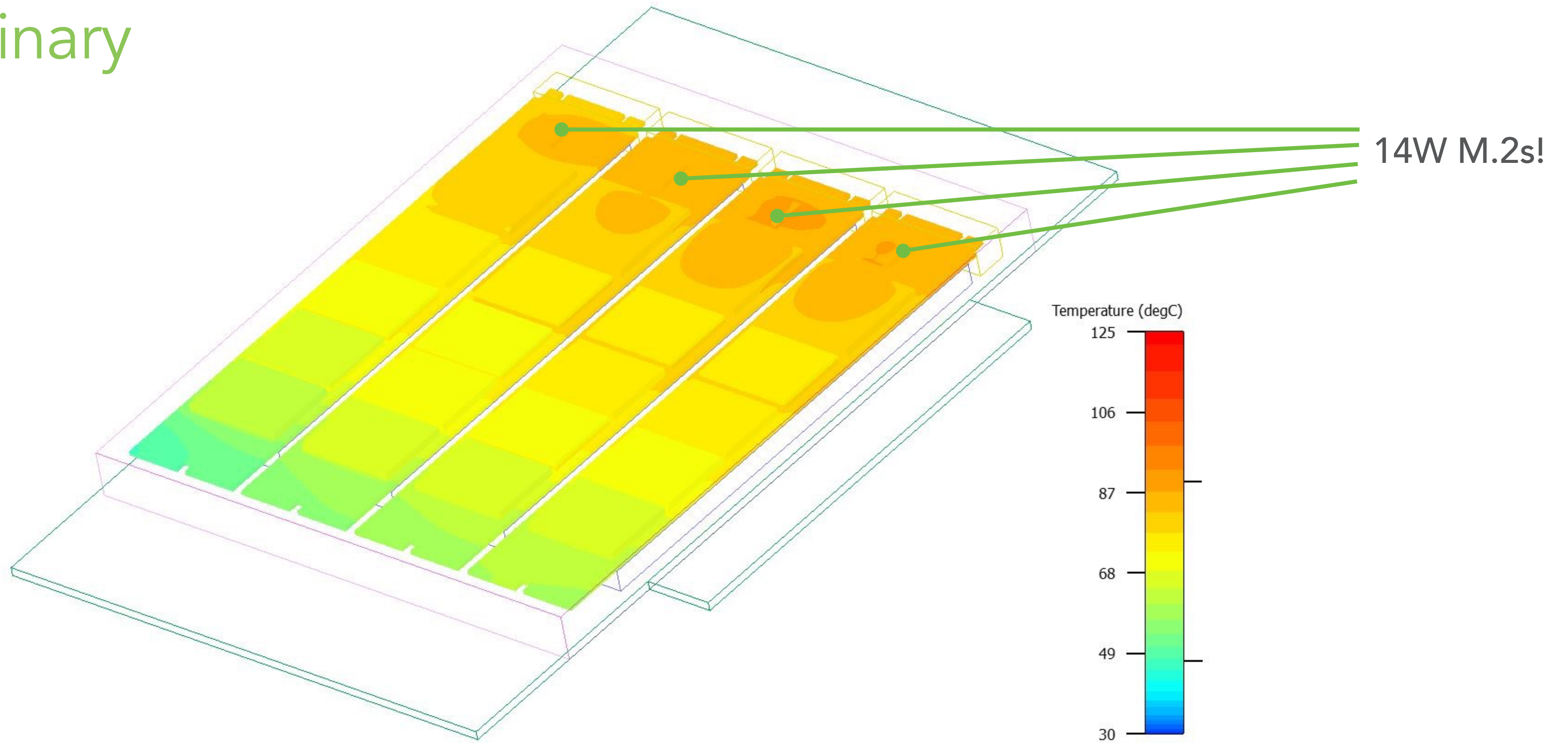
Power

- 3.3V VR supports up to 18A of continuous current
- Up to 4x 14.85W M.2s supported
- All I2C/SMBus devices are powered off of 3.3VAux



Thermal

Preliminary



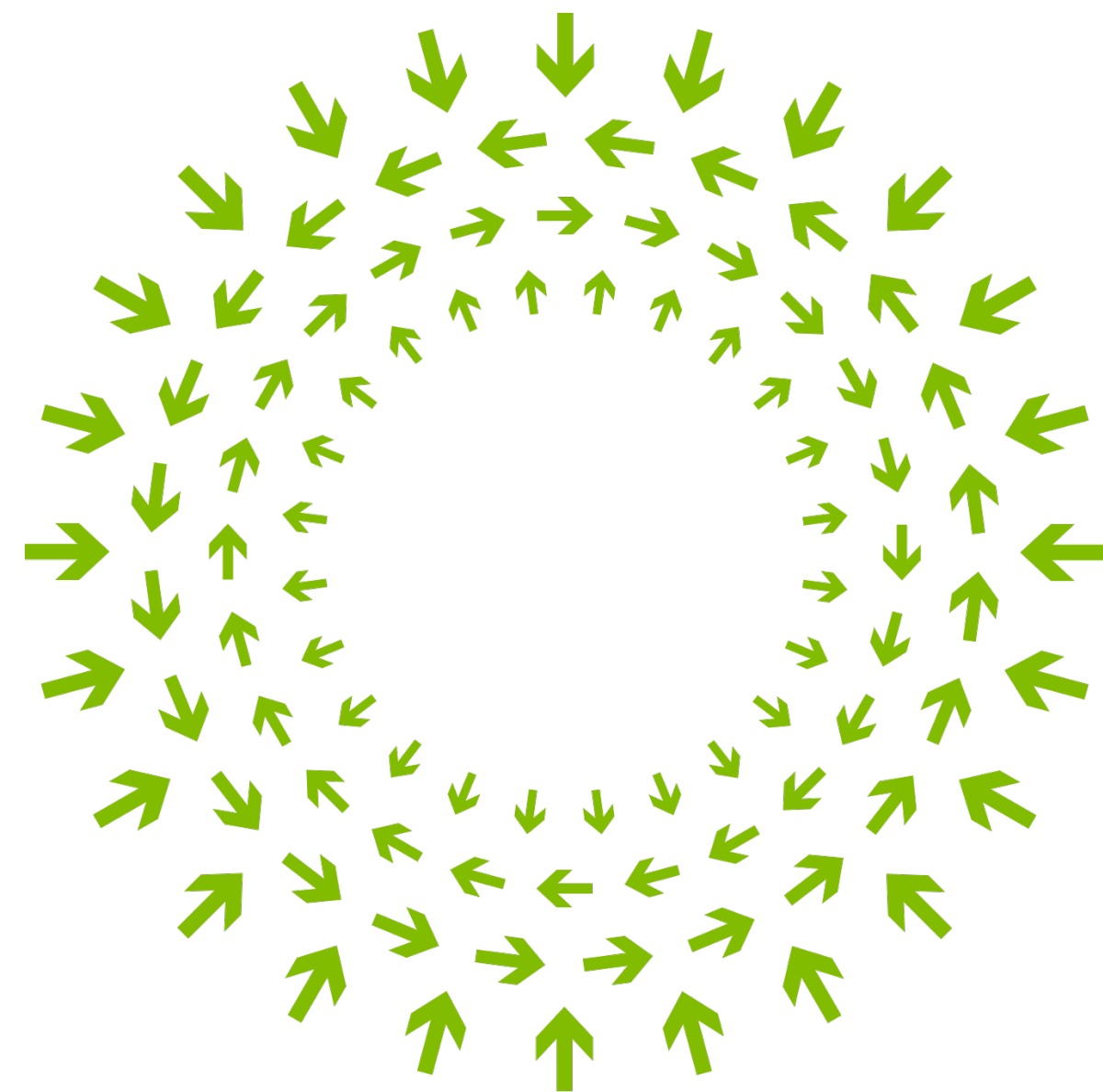
More information

- See the OCP spec in the server working group!
- Come see the Facebook booth!



**A special THANK YOU to the Facebook,
and Quanta teams!**





OPEN

Compute Project