

**GIGABYTE Server**

**Intel Motherboard**

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# 1 Scope

This document defines the technical specifications for the Intel motherboard used in Open Compute Project servers.

# 2 Overview

When data center design and hardware design move in concert, they can improve efficiency and reduce power consumption. To this end, the Open Compute Project is a set of technologies that reduces energy consumption and cost, increases reliability and choice in the marketplace, and simplifies operations and maintenance. One key objective is openness—the project is starting with the opening of the specifications and mechanical designs for the major components of a data center, and the efficiency results achieved at facilities using Open Compute technologies.

One component of this project is a custom motherboard. This document describes the Open Compute Project Efficient Performance Intel motherboard. The motherboard is power­ optimized and bare bones, designed to provide the lowest capital and operating costs. Many features found in traditional motherboards have been removed from the design.

## 2.1 License

As of April 7, 2011, the following persons or entities have made this Specification available under the Open Web Foundation Final Specification Agreement (OWFa 1.0), which is available at http://www.openwebfoundation.org/legal/the­owf­1­0­agreements/owfa­1­0:

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# 3 Efficient Performance Motherboard Features

## 3.1 Block Diagram

The figure below illustrates the functional block diagram of the Efficient Performance Motherboard.

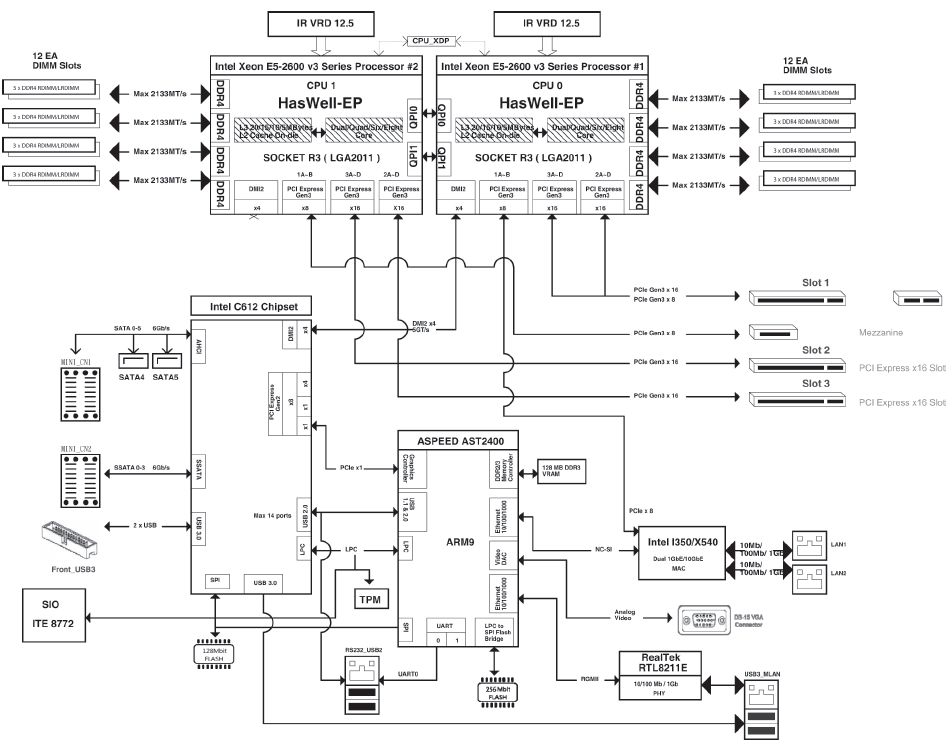


Figure 1: Efficient Performance Motherboard Functional Block Diagram

## 3.2 Placement and Form Factor

The motherboard's form factor is 16.6 inches x 15.2 inches. Figure 2 illustrates board placement. The placement shows the relative positions of key components. Exact dimension and position information is available in the mechanical drawing interchange file (DXF). Strictly follow the form factor, CPU, and DIMM socket location, PCI­E slot position, front I/O ports’ position, Power and Reset buttons, PCI­E Mezzanine Card connector position, and mounting hole locations.

**Internal connector:**

* 14-pin ATX power connector for HDD BP
* 3 x 8-pin ATX 12V power connectors
* 3 x 4-pin ATX 12V power connectors
* 2 x hot-plug CRPS power supply connectors
* 2 x Mini-SAS connectors (SATA3 6Gb/s signal)
* 2 x SATA3 6Gb/s connectors
* 2 x CPU fan headers
* 5 x System fan headers
* 1 x Front panel header
* 1 x HDD Back plane board header
* 1 x TPM module connector
* 1 x Software RAID key connector
* 1 x IPMB connector
* 1 x PCIE x24 connector
* 2x PCIE x16 connector
* 1 x PCIE x16 slot (Mezzanine slot)

**Rear Panel I/O:**

* 2 x USB 3.0 ports
* 2 x USB 2.0 ports
* 1 x RJ11 COM port
* 3 x RJ-45 ports (1 x 10/100/1000 dedicated management LAN port)
* 1 x VGA port
* 1 x ID button

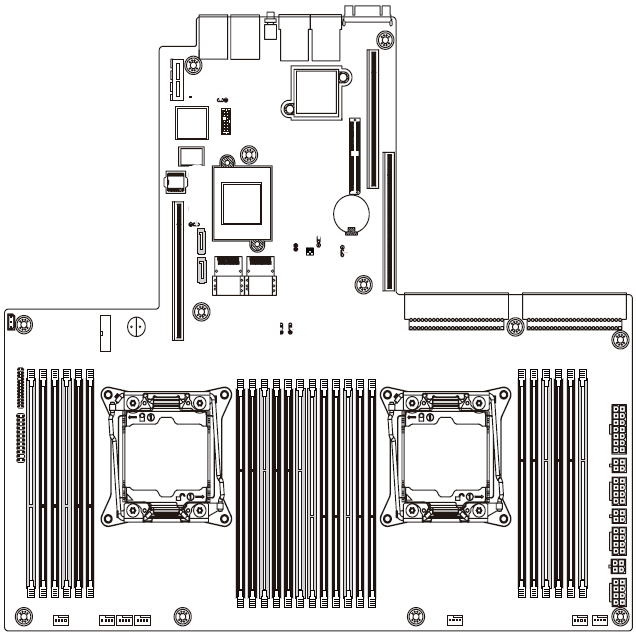


Figure 2: Efficient Performance Board Placement

## 3.3 CPU and Memory

### 3.3.1 CPU

The motherboard uses next generation Intel® Xeon® CPUs with a TDP (thermal design power) up to 145W. The motherboard supports these features:

* Intel**®** Xeon® E5-2600 v3 series processors
* Single Processor Mode
* DDR4 direct attached memory support on cpu0 and cpu1

### 3.3.2 Non-Volatile DIMM (NVDIMM)

Besides traditional DDR4 DIMM, the motherboard needs to support NVDIMM on all DIMM slots. A power failure detection circuit must be implemented to initiate three actions related to data transferring:

1. CPU cache flush

2. Memory controller write pending queue flush

3. Joint Electron Device Engineering Council (JEDEC) standard DIMM support

to store DRAM memory into flash (non­volatile) memory

Due to system energy storing and timing requirement limitations, the logic of action 1) is disabled by default with the resistor option set to Enable. The logic of action 2) and 3) is enabled by default with the resistor option set to Disable. The original design manufacturer (ODM) will work with an NVDIMM vendor to implement a BIOS design.

Action 2) and 3) should be supported and validated in a DDR4 SKU board.

The under­voltage based power failure detection circuit should also trigger separate CPU/DIMM/FAN throttling with separate resistor options for Enable and Disable. The default is set to Enable. This reduces power consumption and slows down voltage decay on P12V.

## 3.4 Platform Controller Hub

The Efficient Performance board uses the Intel® platform controller hub C612 (PCH), which supports the following features:

* USB ports
* SATA ports connected to standard SATA port and mini SAS ports
* SPI interface, connect to BMC to enable BMC the capability to perform BIOS upgrade and recovery
* SMBUS interface (master and slave)

## 3.5 Printed Circuit Board Stackup (PCB)

The Efficient Performance board's PCB stack­up and impedance control are defined in the table below.

Table 1: Efficient Performance Board PCB Stackup

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Layer** | **Plane Description** | | **Copper (oz)** | **Thickness (mil)** | **Dielectric (er)** |
|  |  | SolderMask |  | 0.7 | 4.2 |
| L1 | TOP | Signal | 0.5 | 1.6 |  |
|  |  | PrePreg |  | 2.7 | 4 |
| L2 | GND1 | Ground | 1.0 | 1.2 |  |
|  |  | Core |  | 4.0 | 4.1 |
| L3 | IN1 | Signal | 1.0 | 1.2 |  |
|  |  | PrePreg |  | 19.9 | 4.4 |
| L4 | GND2 | Power | 2.0 | 2.4 |  |
|  |  | Core |  | 4.0 | 4.1 |
| L5 | IN2 | Power | 2.0 | 2.4 |  |
|  |  | PrePreg |  | 19.9 | 4.4 |
| L6 | VCC1 | Power | 1.0 | 1.2 |  |
|  |  | Core |  | 4.0 | 4.2 |
| L7 | VCC2 | Power | 1.0 | 1.2 |  |
|  |  | PrePreg |  | 2.7 | 4.1 |
| L8 | IN3 | Signal | 1.0 | 1.6 |  |
|  |  | SolderMask |  | 0.7 | 4.2 |
|  |  | Total |  | 71.4 | Tolerance:+/-10% |

Table 2; Efficient Performance Board PCB Impedance Control

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Trace** **Width** **(mil)** | **Air** **Gap** **Spacing** **(mil)** | **Impedance** **Type** | **Layer** | **Impedance** **Target** **(ohm)** | **Tolerance** **(+/­** **%)** |
| 6.5 |  | Single | 1,8 | 40 | 10.0 |
| 7.5 |  | Single | 3,6 | 40 | 10.0 |
| 4.0 |  | Single | 1,8 | 50 | 10.0 |
| 4.5 |  | Single | 3,6 | 50 | 10.0 |
| 4.0 | 4.5 | Differential | 1,3,6,8 | 85 | 10.0 |
| 4.0 | 9.0 | Differential | 8 | 95 | 10.0 |
| 4.0 | 12.0 | Differential | 1,5 | 100 | 10.0 |

# 4 Basic Input Output System (BIOS)

The ODM is responsible for supplying and customizing BIOS for the motherboard. This section outlines the specific BIOS requirements.

## 4.1 BIOS Chip

The BIOS chip should use PCH’s SPI interface through a baseboard management controller (BMC) controlled multiplexer (MUX) for the BMC to perform offline BIOS updates or recovery. The vendor is responsible for selecting a specific BIOS chip. The chip should fit the required functionality and be able to support potential additional features that may be required in the future. Considering the space needed for both BIOS and PCH, we recommend a 16MByte size. The vendor should provide a flash region plan for different code and current used size for each region to justify the sizing of the serial peripheral interface (SPI) flash.

A socket on the motherboard should be used to hold the BIOS chip, so the chip can be manually replaced. The BIOS socket must be easily accessible. Other components on the motherboard or in the system must not interfere with the insertion or removal of the BIOS chip. The BIOS socket needs to fit the JEDEC specification package considering tolerance, and fit major available SPI flash vendors’ package drawing.

## 4.2 BIOS Source Code

The BIOS source code comes from the American Megatrends Inc. (AMI) extensible firmware interface (EFI). The ODM is responsible for maintaining the BIOS source code to make sure it has the latest version from AMI and Intel.

## 4.3 BIOS Feature Requirements

### 4.3.1 Optimization

The BIOS should be tuned to minimize system power consumption and maximize performance. This includes:

* Disabling unused devices, including PCI­E lanes, USB ports, SATA/SAS ports, clock generator and buffer ports
* Tuning CPU/chipset settings to reach minimized power consumption and best performance
* Open Turbo Mode tuning option for power limits, short and long time duration
* Using SPEC Power guidelines as guidance for the ODM to validate BIOS tuning results

### 4.3.2 Setup Menu

The ODM must provide a BIOS specification, which includes the complete BIOS, setup menu, and default settings. The setup menu allows its options to be configured before the operating system loads. The configuration options available through the boot menu include the following:

* Setting for enable different Turbo Mode tuning settings based on CPU SKU and Memory configuration. The default is Turbo enable with the CPU vendor’s POR unless otherwise mentioned.
* Setting for power feature after AC power failure. The default is set to Restore Last Power State.
* Setting for Console redirection. There are three selectable options:
  + “Serial over LAN” with baud rate 57600, no flow control, and terminal type VT100
  + “Local Console” with baud rate 57600, no flow control, and terminal type VT100
  + “Auto”, means that Serial­‐Over­‐LAN port is enabled by default, and BIOS will switch to local console automatically depending on hardware strapping. The default option is “Auto”.
* Event log clearing.
* Setting for the error correcting code (ECC) memory error threshold on correctable error. The default setting for mass production is 10.
* Setting of the unified extensible firmware interface (UEFI) and Legacy boot options. The default is UEFI.

### 4.3.3 PXE Boot

The BIOS must support PXE Boot capability in both the IPv4 and the IPv6 environment at the same time.

Boot mode and boot order can be displayed and changed from the BMC.

### 4.3.4 Remote BIOS Update

Vendors should provide tool(s) to implement remote BIOS update function. Vendors must validate update tools on each BIOS release during development and production. Any tool(s) provided should support three update scenarios:

* Scenario 1: Sample/Audit BIOS settings
* Return current BIOS settings, or
* Save/export BIOS settings in a human­‐readable form that can be restored/imported (as in Scenario 2). Output must include a detailed value­‐meaning description for each setting. Settings must include pre­‐production setup menus/options too.
* Scenario 2: Update BIOS with pre­‐configured set of BIOS settings
* Update/change multiple BIOS settings. Settings must include pre­‐production setup menus/options. Tool(s) should provide detailed value­‐meaning descriptions for each setting.
* Reboot.
* Scenario 3: BIOS/firmware update with a new revision
* Load new BIOS/firmware on machine and update, retaining the current BIOS settings.
* Reboot.
* Scenario 4: Use BMC to update BIOS in PCH flash (also described in Section 5.13)
* Update BIOS flash from BMC. The update time should be less than five minutes including uploading the BIOS binary and updating/verifying flash.
* Update with a command line script in the Linux environment from a remote server. A graphical user interface (GUI) is not acceptable.

Additionally, the update tools must have the following capabilities:

* Ability to update from the operating system (OS) through ssh; the current OS is CentOS 5.2 (64­‐bit)
* Require no more than one reset cycle to the system to complete the BIOS update or the BIOS setup option change
* No user interaction (e.g. prompts)
* Can be scripted and propagated to multiple machines

### 4.3.5 Event Log

The BIOS should do event logging through BMC system event logs (SEL). The combination of BIOS and BMC should meet the SEL log requirements in Section 5.10.

### 4.3.6 BIOS Error Codes

BIOS fatal error codes listed in following table should be enabled for POST­‐code output. The major and minor codes alternately display.

# 5 Baseboard Management Controller (BMC)

The motherboard uses a BMC for various platform management services and interfaces with hardware, BIOS, PCH.

The BMC should be a standalone system in parallel to the host. The health status of the host system should not affect the normal operation and network connectivity of the BMC. The BMC cannot share memory with the host system. BMC management connectivity should work independently from the host. If using a shared NIC, there should be no NIC driver dependency for out­‐of­‐band (OOB) communication.

## 5.1 Management Network Interface

The BMC should have RMII/NCSI port for OOB access.

BMC management network firmware and utilities need to support all features defined in this specification in both the IPv4 and IPv6 network environment.

## 5.2 Local Serial Console and Serial-Over-LAN (SOL)

The BMC needs to support two access paths to the serial console:

* A local serial console on debug header
* A remote console, also known as Serial­‐Over­‐LAN (SOL) through the management network described in section 5.1.

It is preferred that both interfaces are functional at all stages of system operation.

The BMC has the control of switching the console input and output between SOL and the local serial console on the fly. When there is a legacy limitation that only one interface is functional, the default is set to Local.

## 5.3 Remote Power Control and Power Policy

The vendor should implement BMC firmware to support remote system power on/off/cycle and warm reboot through the In­‐Band or Out­‐of­‐Band IPMI command.

The vendor should implement BMC firmware to support power on policy to be last­‐state, always­‐on, and always­‐off. The default setting is Last­‐State. The change of power policy should be supported by IPMI command and take effect without a BMC firmware cold reset or a system reboot.

## 5.4 Port 80 POST

The vendor should implement BMC to support a port 80 POST code display to drive the 8­‐bit HEX GPIO to debug header. The BMC post function must be ready before the system BIOS starts to send the first POST code to port 80. The POST code should also be sent to SOL as mentioned in section 5.2.

## 5.5 Platform Environment Control Interface (PECI)

The BMC should access the platform environment control interface (PECI) through PCH by default. The PECI connection implementation should follow Intel guidelines. The BMC should be able to execute PECI raw commands.

The vendor should implement the board design to connect the CPU PECI interface to the PCH PECI. It should be accessed by PCH directly by default. As an option it should reserve the ability to establish a direct connection from the BMC to the CPU PECI interface.

## 5.6 Power and Thermal Monitoring and Power Limiting

The vendor should implement BMC firmware to support platform power monitoring. Power limiting for processor, memory, and platform, PCH is required. Access to this function must be available through In­‐Band and Out­‐of­‐Band.

## 5.7 Sensors

### 5.7.1 Analog Sensors

The BMC has access to all analog sensors on the motherboard either directly or through the PCH. All analog sensors need to be displayed in the sensor data record (SDR) repository.

The analog sensors required are listed in the table below. The lower and upper critical threshold is listed for system event logging purpose.

Table 3: Analog Sensor Table with Lower and Upper Critical Values

|  |  |  |
| --- | --- | --- |
| **Sensor Name** | **Lower Critical** | **Upper Critical** |
| CPU0\_TEMP |  | 94 |
| CPU1\_TEMP |  | 93 |
| SIO |  | 80 |
| SIO |  | 96 |
| PCH\_TEMP |  | 116 |
| DIMM\_P0\_A0 |  | 80 |
| DIMM\_P0\_A1 |  | 80 |
| DIMM\_P0\_B0 |  | 80 |
| DIMM\_P0\_B1 |  | 80 |
| DIMM\_P0\_C0 |  | 80 |
| DIMM\_P0\_C1 |  | 80 |
| DIMM\_P0\_D0 |  | 80 |
| DIMM\_P0\_D1 |  | 80 |
| DIMM\_P1\_E0 |  | 80 |
| DIMM\_P1\_E1 |  | 80 |
| DIMM\_P1\_F0 |  | 80 |
| DIMM\_P1\_F1 |  | 80 |
| DIMM\_P1\_G0 |  | 80 |
| DIMM\_P1\_G1 |  | 80 |
| DIMM\_P1\_H0 |  | 80 |
| DIMM\_P1\_H1 |  | 80 |
| VR\_P0\_TEMP |  | 93 |
| VR\_D\_AB\_TEMP |  | 93 |
| VR\_D\_CD\_TEMP |  | 93 |
| VR\_P1\_TEMP |  | 93 |
| VR\_D\_EF\_TEMP |  | 93 |
| VR\_D\_GH\_TEMP |  | 93 |
| P12V |  | 13.688 |
| P5V |  | 5.688 |
| P3V3 |  | 3.76 |
| P5V\_STBY |  | 5.688 |
| P\_1V05\_PCH |  | 1.196 |
| P\_VBAT | 2.581 |  |
| P\_VCCIN\_P0 |  | 2.127 |
| P\_VCCIN\_P1 |  | 2.127 |
| P\_VDDQ\_AB |  | 1.372 |
| P\_VDDQ\_CD |  | 1.372 |
| P\_VDDQ\_EF |  | 1.372 |
| P\_VDDQ\_GH |  | 1.372 |
| P\_VCCIO\_PCH |  | 1.196 |
| P\_1V5\_PCH |  | 1.705 |
| P\_1V05\_STBY\_PCH |  | 1.196 |
| P\_1V0\_AUX\_LAN |  | 1.137 |
| P\_1V8\_LAN |  | 2.052 |
| P\_1V538\_AUX |  | 1.752 |
| P\_1V26\_AUX |  | 1.44 |
| VR\_P0\_VIN |  | 13.625 |
| VR\_P0\_VOUT |  | 2.128 |
| VR\_D\_AB\_P12V |  | 13.625 |
| VR\_D\_AB\_P3V3 |  | 3.764 |
| VR\_D\_AB\_VOUT |  | 1.373 |
| VR\_D\_CD\_P12V |  | 13.625 |
| VR\_D\_CD\_P3V3 |  | 3.764 |
| VR\_D\_CD\_VOUT |  | 1.373 |
| VR\_P1\_VIN |  | 13.625 |
| VR\_P1\_VOUT |  | 2.128 |
| VR\_D\_EF\_P12V |  | 13.625 |
| VR\_D\_EF\_P3V3 |  | 3.764 |
| VR\_D\_EF\_VOUT |  | 1.373 |
| VR\_D\_GH\_P12V |  | 13.625 |
| VR\_D\_GH\_P3V3 |  | 3.764 |
| VR\_D\_GH\_VOUT |  | 1.373 |
| VR\_P0\_IOUT |  | 248 |
| VR\_D\_AB\_IOUT |  | 248 |
| VR\_D\_CD\_IOUT |  | 248 |
| VR\_P1\_IOUT |  | 248 |
| VR\_D\_EF\_IOUT |  | 248 |
| VR\_D\_GH\_IOUT |  | 248 |
| CPU0\_FAN | 600 |  |
| CPU1\_FAN | 600 |  |
| SYS\_FAN1 | 600 |  |
| SYS\_FAN2 | 600 |  |
| SYS\_FAN3 | 600 |  |
| SYS\_FAN4 | 600 |  |
| SYS\_FAN5 | 600 |  |

### 5.7.2 Discrete Sensors

The vendor should implement BMC firmware access and display discrete sensors in SDR. The BMC should log abnormal sensor readings to SEL.

The discrete sensors required and the SEL format is listed in the table below.

Table 4: SEL format

|  |  |
| --- | --- |
| **Sensor Name** | **Event data** |
| CPU0 | 00: IERR 01: Thermal Trip 07: Processor Presence Detected |
| CPU1 | 00: IERR 01: Thermal Trip 07: Processor Presence Detected |
| BIOS\_POST | display post code |
| SEL | 04: SEL Full 05: SEL Almost Full |

## 5.8 System Event Log (SEL)

The vendor should implement BMC to support the SEL.

### 5.8.1 Errors to be logged

**CPU error**

Both correctable ECC and uncorrectable ECC errors should be logged in the event log. Error categories include Link and L3 Cache.

**Memory error**

Both correctable ECC and uncorrectable ECC errors should be logged in the event log. The error log should indicate the location of DIMM, CPU socket#, channel # and slot #. Memory error reporting needs to be tested by both debug tool error injection and the reworked ECC DIMM.

**PCI­‐E error**

All errors that have status, register, should be logged in the Event Log. This includes root complex, endpoint device, and any switch upstream/downstream ports if available. Link disable on errors should also be logged. The error classifications (fatal, non­‐fatal, or correctable) follow the chipset vendor’s recommendation.

**POST error**

All POST errors, which are detected by BIOS during POST, should be logged in the Event Log.

**Power error**

Two kinds of power errors should be logged. One is a 12.5V DC input power failure that causes all power rails on the motherboard to lose power, including standby power. The other is an unexpected system shutdown during system S0/S1 while 12.5V DC input is still valid.

**FAN Failure**

FAN failure error should be logged if the fan speed is out of expected ranges between the lower and upper critical threshold. The Error log should also identify which fan fails.

**PMBus status error**

The PMBus status sensors check PMBus controller health status and log errors if an abnormal value is detected. The PMBus controller can be a DC Hot Swap Controller (HSC) or a PMBus AC to DC power supply unit (PSU).

## 5.9 Fan Speed Control in BMC

The vendor should enable fan speed control (FSC) on BMC. The BMC samples thermal related analog sensors in real time. The FSC algorism processes these inputs and drives two pulse width modulation (PWM) outputs in optimized speed.

## 5.10 BMC Firmware Update

Vendors should provide tool(s) to implement a remote BMC firmware update that will not require any physical input at the system level. We define a remote update as an update either through OOB by management network or through logging into the local OS (CentOS) by the data network.

A remote BMC firmware update may take a maximum of 10 minutes to complete. The BMC firmware update process and BMC reset process should require no reboot or power down of the host system. It should also have no impact on the normal operations of the host system. The BMC needs to be fully functional, with updated firmware after the update and it must reset without further configuration.

By default, the update should recovery the BMC to its factory default settings. There must also be options to preserve SEL and configuration. The MAC address should not be cleared with the BMC firmware update.

# 6 Thermal Design Requirements

To meet thermal reliability requirements, the thermal and cooling solution should dissipate heat from the components when the system is operating at its maximum thermal power. Find the thermal solution by setting a high power target for the initial design in order to avoid redesigning the cooling solution. The final thermal solution of the system delivered should be the most optimized and energy efficient with the lowest capital and operating costs. The thermal solution should not allow components in the motherboard to overheat. Under following environmental conditions, neither the CPU nor the memory should throttle due to any thermal issue:

 Inlet temperature lower than or equal to 35**°**C, and 0 inch H2O data center pressure with all fans functioning in each thermal zone

 Inlet temperature lower than or equal to 35**°**C, and 0.01 inch H2O data center pressure with one fan (or one rotor) failure in each thermal zone

## 6.1 Data Center Environmental Conditions

The thermal design for the motherboard needs to satisfy the operational conditions at data centers. Conditions listed below use in the Data Center as reference.

### 6.1.1 Location of Data Center/Altitude

Data centers may be located 1000m above sea level (at maximum). Any variation of air properties or environmental difference due to the high altitude needs to be accounted for in the thermal design.

### 6.1.2 Cold Aisle Temperature

Data centers keep cold aisle temperatures between 18°C and 30°C (65°F to 85°F). The mean temperature in the cold aisle is 24°C with 3°C standard deviation. The cold aisle temperature may fluctuate minutely depending on the outside air temperature. Every component must be cooled and maintained below its maximum specification temperature in any cold aisle temperature.

### 6.1.3 Cold Aisle Pressurization

Data centers maintain cold aisle pressure between 0inches H2O and 0.05 inches H2O. The thermal design should factor in the worst operational pressurization in the data center, which is 0 inches H2O and 0.01 inches H2O with a single fan (or rotor) failure.

### 6.1.4 Relative Humidity

Data centers maintain relative humidity between 20% and 85%.Environmental condition changes due to the high altitude may not need to be considered if the thermal design can meet the requirement with maximum relative humidity (85%).

## 6.2 Server Operational Conditions

### 6.2.1 System Loading

The power consumption of individual components in the motherboard vary with the application the server is running or the motherboard’s SKU. The total power consumption of the system may also vary with the usage or with the number of PCI­‐E cards on the system. Please see the summary below:

 System loading: idle to 100%

 Number of PCI­‐E full height or half height cards installed: 0 ­‐ 2

 Number of PCI­‐E Mezzanine card installed: 0 ­‐ 1

 Number of 2.5” HDD: 0 ­‐ 8

The power can consume up to 800W per system. The plan of record (worst­‐case configuration) for the thermal and power delivery design is two CPUs with 24x 8GB DIMMs.

A unified thermal solution is preferred to cover up to 100% of system loading. However, an ODM can propose a non­‐unified thermal solution if there is alternative way to provide cost benefits. At minimum, the air­‐duct design should be unified for all SKUs.

### 6.2.2 DDR DIMM DRAM Operation

The thermal design should meet DIMM maximum operating temperatures (85°C) with a single refresh rate. A thermal test should be done based on DIMM module approved vendor list (AVL). The BIOS and memory subsystem should have an optimized refresh rate. It should use the optional DIMM auto­‐self­‐refresh (ASR) based on the DIMM’s temperature. The implementation should follow the updated DDR4 memory controller and the DIMM vendor’s specification.

### 6.2.3 Inlet Temperature

Inlet air temperatures will vary. The cooling system should cover the following inlet temperatures (20°C, 25°C, 30°C, and 35°C). Cooling above 30°C is beyond the system’s operating specification. It is used during validation, however, to demonstrate design margin. CPU throttling is not allowed to activate over the validation range of 0°C – 35°C.

### 6.2.4 Pressurization

The thermal solution should not consider the availability of extra airflow from data center cooling fans. If (and only if) one rotor in server fan fails, the negative or positive data center pressurization can be considered in the thermal solution in the hot aisle or in the cold aisle.

### 6.2.5 Thermal Margin

The thermal margin is the difference between the maximum theoretical safe temperature and the actual temperature. The board design operates at an inlet temperature of 35°C (95°F) outside of the system with a minimum 2% thermal margin for every component on the card. Otherwise, the thermal margin for every component in the system is at least 7% for temperatures up to 30°C.

## 6.3 Thermal Kit Requirements

Thermal testing must be performed up to a 35°C (95°F) inlet temperature to guarantee high­‐ temperature reliability.

### 6.3.1 Heat Sink

(Vapor chamber base + CU fin) x 2Pcs

### 6.3.2 System Fan

40mm x 40mm x 28mm Fan x 4Pcs

40mm x 40mm x 56mm Fan x 4Pcs

### 6.3.3 Air Duct

The air duct must be part of the motherboard tray cover. The design must be energy efficient, simple, and easily serviceable. It should also be unified for all system SKUs. It is preferred that the manufacturer uses highly green materials or reusable materials for the air duct.

### 6.3.4 Thermal Sensor

The maximum allowable tolerance of the thermal sensors in the system is ±3°C.

# 7 Motherboard Power system

## 7.1 Replacing the Power Supply

1. Disconnect the three power cables.
2. Remove the four screws securing on the power supply.
3. Lift the power supply out of the chassis in the direction of the arrow.
4. Insert the replacement power supply firmly into the chassis. Connect the AC power cord to the replacement power supply.

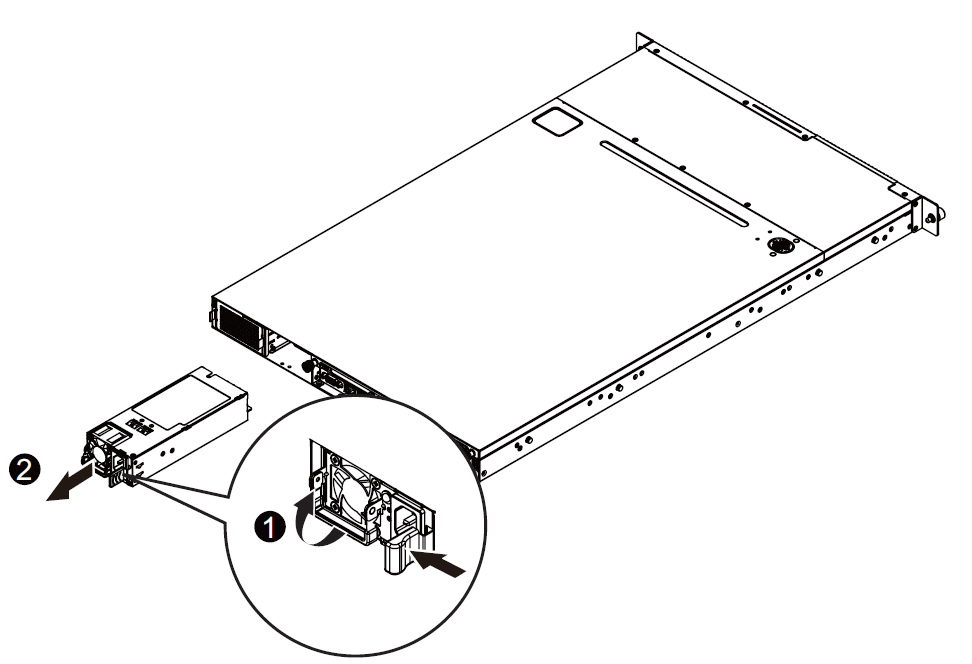


Figure 3: instruction for replacing the power supply

## 7.2 Input Voltage

### 7.2.1 Input Voltage Level

The nominal input voltage delivered by the CRPS power supply is +12.0 volts and +12Vsb volts. The motherboard shall accept and operate normally with input voltage tolerance range between 11.4V and 12.6V.

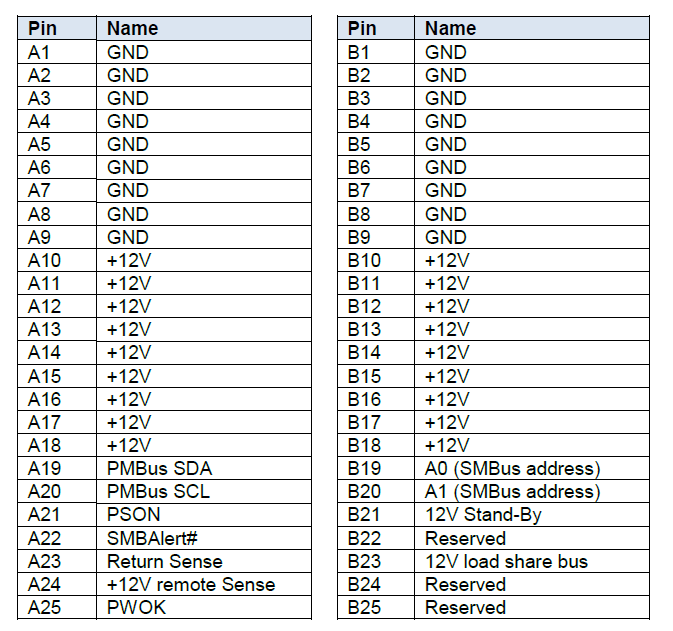
### 7.2.2 Capacitive Load

To ensure compatibility with the system power supply, the motherboard may not have a capacitive load greater than 20000µF with +12V and 3000µF with +12Vsb.

### 7.2.3 Power Card Edge connector

The MB shall use 2x25 Power Card Edge connector equivalent FCI 10035388-102LF.

Table 5: Power Card Edge connector pin description



## 7.3 CPU Voltage Regulator (VR)

### 7.3.1 CPU Maximum Power

The motherboard shall be designed to handle a processor with a maximum TDP of 145W CPU. Support for processors of higher TDP is not required. As a result, the vendor shall optimize the CPU voltage regulator (VR) accordingly.

### 7.3.2 CPU VR Optimizations

CPU VR optimizations shall be implemented to reduce cost and increase the efficiency of the power conversion system. The CPU VR should have an auto­‐ phase­‐dropping feature, and run at optimized phase count among 1, 2, 3,… and maximum phase count. The CPU VR should support all power states to allow the VRM to operate at its peak efficiency at light loading.

The CPU VR should be compliant to the latest Intel VR specification and validation method and pass test with margin.

### 7.3.3 CPU VRM Efficiency

The minimum efficiency for the CPU VRM efficiency is 91% over the 30% to 90% load range and 93% over the 50% to 70% load range for TDP power of CPU, measured from the 12V input to the VRM output. Vendors are encouraged to exceed the above efficiency requirement and may propose higher efficiency VRMs that may come at additional cost. The power efficiency measured from 12V input to the CPU socket should also be analyzed and improved.

## 7.4 DIMM Voltage Regulator

### 7.4.1 DIMM Power Rails

The motherboard design should have a DIMM Power Rails option for DDR4 on DDR4 SKU.

### 7.4.2 DIMM Maximum Power

The motherboard has a DIMM configuration for 24x slots of two CPU sockets. The vendor should follow the memory controller vendor’s guideline to design and validate the DIMM power rail to support the maximum power needed for this configuration, and support a 1.2V DDR4 DIMM.

### 7.4.3 DIMM VR Optimizations

The DIMM VR should be compliant to the latest Intel VR specification, the memory controller vendor’s updated validation guideline, and pass the test with margin.

## 7.5 Hard Drive Power

The motherboard shall supply power to HDD backplane board (2.5” 24 bays or 3.5” 12 bays maximum). Hard drives require 12 volt DC, 5 volt DC and 3.3 volt DC power sources. Power will be delivered through a 2x7 pins power connector (LOTES ABA-POW-008-P32 or equivalent). The pin assignment shall follow the described in the table below.

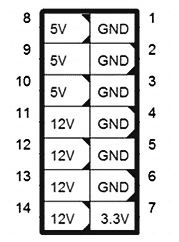


Figure 4:2x13 pins HDD BP power connector

Table 6: Pin Description

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Pin No.** | **Definition** | **Pin No.** | **Definition** | **Pin No.** | **Definition** |
| 1 | GND | 2 | GND | 3 | GND |
| 4 | GND | 5 | GND | 6 | GND |
| 7 | 3.3V | 8 | 5V | 9 | 5V |
| 10 | 5V | 11 | 12V | 12 | 12V |
| 13 | 12V | 14 | 12V |

### 7.5.1 HDD Power Requirements

The motherboard must provide enough power delivery on 12.0volts DC and 5 volts DC to support up to 12 x 3.5” or 24 x 2”5 HDDs. This means enough power to support 1A continuous per HDD on a 12.0 VOLT DC power rail, and 0.75A continuous per HDD on a 5 volt DC power rail. The in­rush current required to spin up the drive must also be considered in the power delivery design.

### 7.5.2 Output Protection

Both 12V and 5V disk output power rails shall protect against short circuits and overload conditions.

### 7.5.3 Spin-up Delay

When a hard drive spins up, it draws excessive current on both 12V and 5V. The peak current may reach the 1.5A ~ 2A range in 12V. The system may have up to nine hard drives installed, so there is a need to spin up the hard drives in sequence. The BIOS should implement a five­ second delay between spinning up each hard drive. In order to do this, the SATA hard drive’s power cable should set pin 11 as NC or PU (No Connection or Pull high) to enable the delayed hard drive spin­ up function.

## 7.6 System VRM Efficiency

Vendors shall supply high­ efficiency VRMs for all other voltage regulators over 20W not defined in this specification. All other voltage regulation modules shall be 91% efficiency over the 30% to 90% load range. Vendors are encouraged to deliver systems with higher efficiencies.

## 7.7 Power On

The motherboard should be set to restore the last power state during AC on/off. This means when the AC cycles on/off, the motherboard should power on automatically without someone pressing the power button. When the motherboard is powered off on purpose, it should be kept off through AC on/off.

# 8 I/O System

This section describes the motherboard's I/O features.

## 8.1 PCIe\* x24 Slot Connector and PCIE x16 connector/Riser Card

The motherboard has one PCI­E x24 slot and one connector PCI­E x16 slots to support PCI­E Gen 3 signals. The slot location must follow the mechanical requirement delivered in DXF format.

The system vendor should also provide a PCI­E riser card so two full ­height PCI­E cards could be plugged in horizontally and locked in position. The top slot has x16 PCI­E connector and supports a full­ height, half ­length PCI­E card. The bottom slot has x8 PCI­E connector.

Table 7.8 contains information PCI­E x24 slot and PCI-E x16 slot connector on the motherboard.

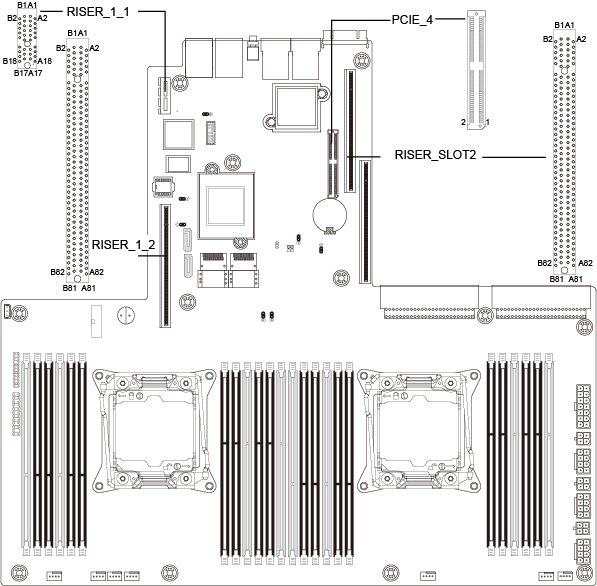


Figure 5: Riser1\_1 & Riser1\_2

Table 7: Pin Description

**⚫ RISER\_1\_1**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin No.** | **Definition** | **Pin No.** | **Definition** | **Pin No.** | **Definition** | **Pin No.** | **Definition** |
| B1 | 12V | B10 | PCIE2\_TXP0 | A1 | 12V | A10 | PCIE2\_RXP0 |
| B2 | 12V | B11 | PCIE2\_TXN0 | A2 | 12V | A11 | PCIE2\_RXN0 |
| B3 | 12V | B12 | WAKE# | A3 | 12V | A12 | RESET# |
| B4 | GND | B13 | GND | A4 | 12V | A13 | GND |
| B5 | 3.3V\_EN | B14 | PCIE2\_TXP1 | A5 | GND | A14 | PCIE2\_RXP1 |
| B6 | SMBCLK | B15 | PCIE2\_TXN1 | A6 | CLK\_100M\_P | A15 | PCIE2\_RXN1 |
| B7 | SMBDAT | B16 | GND | A7 | CLK\_100M\_N | A16 | GND |
| B8 | 3.3V\_AUX | B17 | PCIE2\_TXP2 | A8 | GND | A17 | PCIE2\_RXP2 |
| B9 | GND | B18 | PCIE2\_TXN2 | A9 | GND | A18 | PCIE2\_RXN2 |

**⚫ RISER\_1\_2**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin No.** | **Definition** | **Pin No.** | **Definition** | **Pin No.** | **Definition** | **Pin No.** | **Definition** |
| B1 | PCIE2\_TXP3 | B42 | GND | A1 | PCIE2\_RXP3 | A42 | GND |
| B2 | PCIE2\_TXN3 | B43 | GND | A2 | PCIE2\_RXN3 | A43 | GND |
| B3 | GND | B44 | PCIE1\_TXP6 | A3 | GND | A44 | PCIE1\_RXP6 |
| B4 | GND | B45 | PCIE1\_TXN6 | A4 | GND | A45 | PCIE1\_RXN6 |
| B5 | PCIE2\_TXP4 | B46 | GND | A5 | PCIE2\_RXP4 | A46 | GND |
| B6 | PCIE2\_TXN4 | B47 | GND | A6 | PCIE2\_RXN4 | A47 | GND |
| B7 | GND | B48 | PCIE1\_TXP7 | A7 | GND | A48 | PCIE1\_RXP7 |
| B8 | GND | B49 | PCIE1\_TXN7 | A8 | GND | A49 | PCIE1\_RXN7 |
| B9 | PCIE2\_TXP5 | B50 | GND | A9 | PCIE2\_RXP5 | A50 | GND |
| B10 | PCIE2\_TXN5 | B51 | GND | A10 | PCIE2\_RXN5 | A51 | GND |
| B11 | GND | B52 | PCIE1\_TXP8 | A11 | GND | A52 | PCIE1\_RXP8 |
| B12 | PCIE2\_TXP6 | B53 | PCIE1\_TXN8 | A12 | PCIE2\_RXP6 | A53 | PCIE1\_RXN8 |
| B13 | PCIE2\_TXN6 | B54 | GND | A13 | PCIE2\_RXN6 | A54 | GND |
| B14 | GND | B55 | GND | A14 | GND | A55 | GND |
| B15 | GND | B56 | PCIE1\_TXP9 | A15 | GND | A56 | PCIE1\_RXP9 |
| B16 | PCIE2\_TXP7 | B57 | PCIE1\_TXN9 | A16 | PCIE2\_RXP7 | A57 | PCIE1\_RXN9 |
| B17 | PCIE2\_TXN7 | B58 | GND | A17 | PCIE2\_RXN7 | A58 | GND |
| B18 | GND | B59 | GND | A18 | GND | A59 | GND |
| B19 | GND | B60 | PCIE1\_TXP10 | A19 | GND | A60 | PCIE1\_RXP10 |
| B20 | PCIE1\_TXP0 | B61 | PCIE1\_TXN10 | A20 | PCIE1\_RXP0 | A61 | PCIE1\_RXN10 |
| B21 | PCIE1\_TXN0 | B62 | GND | A21 | PCIE1\_RXN0 | A62 | GND |
| B22 | GND | B63 | GND | A22 | GND | A63 | GND |
| B23 | GND | B64 | PCIE1\_TXP11 | A23 | GND | A64 | PCIE1\_RXP11 |
| B24 | PCIE1\_TXP1 | B65 | PCIE1\_TXN11 | A24 | PCIE1\_RXP1 | A65 | PCIE1\_RXN11 |
| B25 | PCIE1\_TXN1 | B66 | GND | A25 | PCIE1\_RXN1 | A66 | GND |
| B26 | GND | B67 | GND | A26 | GND | A67 | GND |
| B27 | GND | B68 | PCIE1\_TXP12 | A27 | GND | A68 | PCIE1\_RXP12 |
| B28 | PCIE1\_TXP2 | B69 | PCIE1\_TXN12 | A28 | PCIE1\_RXP2 | A69 | PCIE1\_RXN12 |
| B29 | PCIE1\_TXN2 | B70 | GND | A29 | PCIE1\_RXN2 | A70 | GND |
| B30 | GND | B71 | GND | A30 | GND | A71 | GND |
| B31 | GND | B72 | PCIE1\_TXP13 | A31 | GND | A72 | PCIE1\_RXP13 |
| B32 | PCIE1\_TXP3 | B73 | PCIE1\_TXN13 | A32 | PCIE1\_RXP3 | A73 | PCIE1\_RXN13 |
| B33 | PCIE1\_TXN3 | B74 | GND | A33 | PCIE1\_RXN3 | A74 | GND |
| B34 | GND | B75 | GND | A34 | GND | A75 | GND |
| B35 | GND | B76 | PCIE1\_TXP14 | A35 | GND | A76 | PCIE1\_RXP14 |
| B36 | PCIE1\_TXP4 | B77 | PCIE1\_TXN14 | A36 | PCIE1\_RXP4 | A77 | PCIE1\_RXN14 |
| B37 | PCIE1\_TXN4 | B78 | GND | A37 | PCIE1\_RXN4 | A78 | GND |
| B38 | GND | B79 | GND | A38 | GND | A79 | GND |
| B39 | GND | B80 | PCIE1\_TXP15 | A39 | GND | A80 | PCIE1\_RXP15 |
| B40 | PCIE1\_TXP5 | B81 | PCIE1\_TXN15 | A40 | PCIE1\_RXP5 | A81 | PCIE1\_RXN15 |
| B41 | PCIE1\_TXN5 | B82 | ID0 | A41 | PCIE1\_RXN5 | A82 | ID1 |

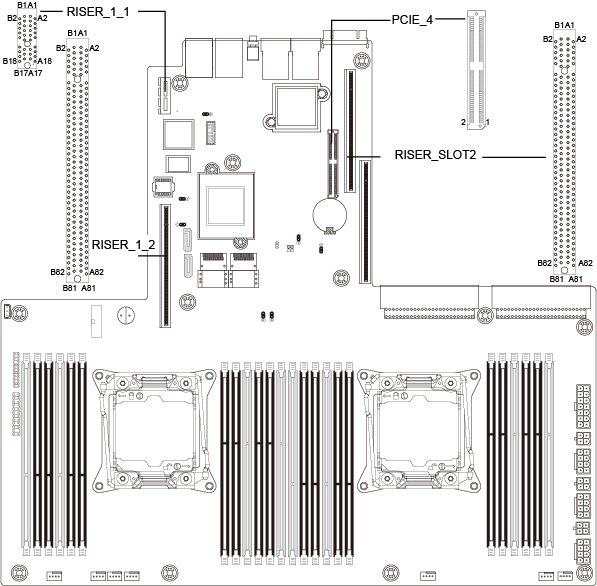


Figure 6: Riser2

Table 8: Pin Description

**⚫ RISER\_2**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin No.** | **Definition** | **Pin No.** | **Definition** | **Pin No.** | **Definition** | **Pin No.** | **Definition** |
| B1 | 12V | B42 | PCIE\_TXN6 | A1 | GND | A42 | GND |
| B2 | 12V | B43 | GND | A2 | 12V | A43 | PCIE\_RXP6 |
| B3 | 12V | B44 | GND | A3 | 12V | A44 | PCIE\_RXN6 |
| B4 | GND | B45 | PCIE\_TXP7 | A4 | GND | A45 | GND |
| B5 | SMBCLK | B46 | PCIE\_TXN7 | A5 | NC | A46 | GND |
| B6 | SMBDAT | B47 | GND | A6 | CLK\_100M\_2ND\_P | A47 | PCIE\_RXP7 |
| B7 | GND | B48 | NC | A7 | CLK\_100M\_2ND\_N | A48 | PCIE\_RXN7 |
| B8 | 3.3V | B49 | GND | A8 | NC | A49 | GND |
| B9 | NC | B50 | PCIE\_TXP8 | A9 | 3.3V | A50 | ID1 |
| B10 | 3.3V\_AUX | B51 | PCIE\_TXN8 | A10 | 3.3V | A51 | GND |
| B11 | WAKE# | B52 | GND | A11 | RESET# | A52 | PCIE\_RXP8 |
| B12 | NC | B53 | GND | A12 | GND | A53 | PCIE\_RXN8 |
| B13 | GND | B54 | PCIE\_TXP9 | A13 | CLK\_100M\_P | A54 | GND |
| B14 | PCIE\_TXP0 | B55 | PCIE\_TXN9 | A14 | CLK\_100M\_N | A55 | GND |
| B15 | PCIE\_TXN0 | B56 | GND | A15 | GND | A56 | PCIE\_RXP9 |
| B16 | GND | B57 | GND | A16 | PCIE\_RXP0 | A57 | PCIE\_RXN9 |
| B17 | NC | B58 | PCIE\_TXP10 | A17 | PCIE\_RXN0 | A58 | GND |
| B18 | GND | B59 | PCIE\_TXN10 | A18 | GND | A59 | GND |
| B19 | PCIE\_TXP1 | B60 | GND | A19 | GND | A60 | PCIE\_RXP10 |
| B20 | PCIE\_TXN1 | B61 | GND | A20 | GND | A61 | PCIE\_RXN10 |
| B21 | GND | B62 | PCIE\_TXP11 | A21 | PCIE\_RXP1 | A62 | GND |
| B22 | GND | B63 | PCIE\_TXN11 | A22 | PCIE\_RXN1 | A63 | GND |
| B23 | PCIE\_TXP2 | B64 | GND | A23 | GND | A64 | PCIE\_RXP11 |
| B24 | PCIE\_TXN2 | B65 | GND | A24 | GND | A65 | PCIE\_RXN11 |
| B25 | GND | B66 | PCIE\_TXP12 | A25 | PCIE\_RXP2 | A66 | GND |
| B26 | GND | B67 | PCIE\_TXN12 | A26 | PCIE\_RXN2 | A67 | GND |
| B27 | PCIE\_TXP3 | B68 | GND | A27 | GND | A68 | PCIE\_RXP12 |
| B28 | PCIE\_TXN3 | B69 | GND | A28 | GND | A69 | PCIE\_RXN12 |
| B29 | GND | B70 | PCIE\_TXP13 | A29 | PCIE\_RXP3 | A70 | GND |
| B30 | IBUTT3 | B71 | PCIE\_TXN13 | A30 | PCIE\_RXN3 | A71 | GND |
| B31 | NC | B72 | GND | A31 | GND | A72 | PCIE\_RXP13 |
| B32 | GND | B73 | GND | A32 | CLK\_100M\_3RD\_P | A73 | PCIE\_RXN13 |
| B33 | PCIE\_TXP4 | B74 | PCIE\_TXP14 | A33 | CLK\_100M\_3RD\_N | A74 | GND |
| B34 | PCIE\_TXN4 | B75 | PCIE\_TXN14 | A34 | GND | A75 | GND |
| B35 | GND | B76 | GND | A35 | PCIE\_RXP4 | A76 | PCIE\_RXP14 |
| B36 | GND | B77 | GND | A36 | PCIE\_RXN4 | A77 | PCIE\_RXN14 |
| B37 | PCIE\_TXP5 | B78 | PCIE\_TXP15 | A37 | GND | A78 | GND |
| B38 | PCIE\_TXN5 | B79 | PCIE\_TXN15 | A38 | GND | A79 | GND |
| B39 | GND | B80 | GND | A39 | PCIE\_RXP5 | A80 | PCIE\_RXP15 |
| B40 | GND | B81 | NC | A40 | PCIE\_RXN5 | A81 | PCIE\_RXN15 |
| B41 | PCIE\_TXP6 | B82 | ID0 | A41 | GND | A82 | GND |

## 8.2 DIMM Connector

This motherboard provides 24 DDR4 memory sockets and supports Four Channel Technology. After the memory is installed, the BIOS will automatically detect the specifications and capacity of the memory. Enabling Four Channel memory mode will be four times of the original memory bandwidth. The four DDR4 memory sockets are divided into four channels each channel has two memory sockets as following:

Channel 1: DIMM\_P0\_A0/DIMM\_P0\_A1/DIMM\_P0\_A2 (For primary CPU);

DIMM\_P1\_E0/DIMM\_P1\_E1/DIMM\_P1\_E2 (For secondary CPU)

Channel 2: DIMM\_P0\_B0/DIMM\_P0\_B1/DIMM\_P0\_B2 (For primary CPU);

DIMM\_P1\_F0/DIMM\_P1\_F1/DIMM\_P1\_F (For secondary CPU)

Channel 3: DIMM\_P0\_C0/DIMM\_P0\_C1/DIMM\_P0\_C2 (For primary CPU);

DIMM\_P1\_G0/DIMM\_P1\_G1/DIMM\_P1\_G2 (For secondary CPU)

Channel 4: DIMM\_P0\_D0/DIMM\_P0\_D1/DIMM\_P0\_D2 (For primary CPU);

DIMM\_P1\_H0/DIMM\_P1\_H1/DIMM\_P1\_H2 (For secondary CPU)

## 8.3 PCI-E Mezzanine Card

The motherboard has one PCI­E x8 Mezzanine card connector that holds x8 PCI­E Gen 3 signals. The Mezzanine card connector on the motherboard should use (SAMTEC HSEC8-150-01-L-DV-A-K-TR) or an equivalent connector, with mating (SAMTEC HSEC8-150-01-L-DV-A-K-TR) or an equivalent connector on the Mezzanine card.

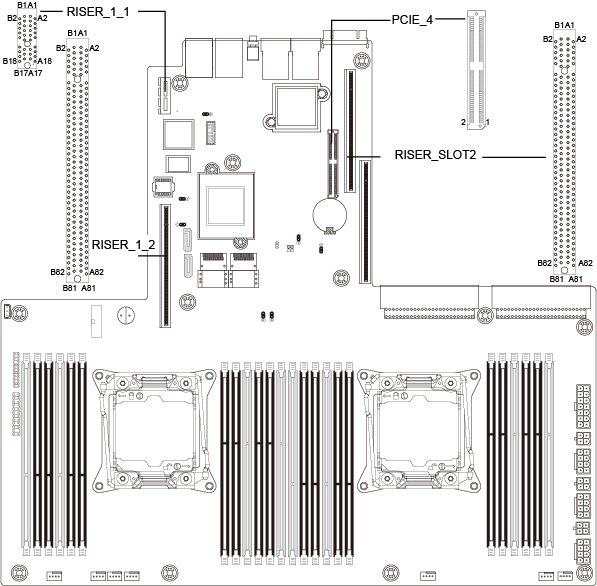


Figure 7: Mezzanine card connector

Table 9: Pin Description

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin No.** | **Definition** | **Pin No.** | **Definition** | **Pin No.** | **Definition** | **Pin No.** | **Definition** |
| 1 | GND | 2 | GND | 3 | 12V | 4 | 12V |
| 5 | 12V | 6 | 12V | 7 | GND | 8 | GND |
| 9 | 3.3V | 10 | 3.3V | 11 | 3.3V | 12 | 3.3V |
| 13 | 3.3V | 14 | 3.3V | 15 | 3.3V | 16 | 3.3V |
| 17 | 3.3V\_AUX | 18 | GND | 19 | GND | 20 | NC |
| 21 | PCIE\_TXP7 | 22 | GND | 23 | PCIE\_TXN7 | 24 | GND |
| 25 | GND | 26 | PCIE\_RXP7 | 27 | GND | 28 | PCIE\_RXN7 |
| 29 | PCIE\_TXP6 | 30 | GND | 31 | PCIE\_TXN6 | 32 | GND |
| 33 | GND | 34 | PCIE\_RXP6 | 35 | GND | 36 | PCIE\_RXN6 |
| 37 | PCIE\_TXP5 | 38 | GND | 39 | PCIE\_TXN5 | 40 | GND |
| 41 | GND | 42 | PCIE\_RXP5 | 43 | GND | 44 | PCIE\_RXN5 |
| 45 | PCIE\_TXP4 | 46 | GND | 47 | PCIE\_TXN4 | 48 | GND |
| 49 | GND | 50 | PCIE\_RXP4 | 51 | GND | 52 | PCIE\_RXN4 |
| 53 | NC | 54 | GND | 55 | GND | 56 | NC |
| 57 | PCIE\_TXP3 | 58 | GND | 59 | PCIE\_TXN3 | 60 | GND |
| 61 | GND | 62 | PCIE\_RXP3 | 63 | GND | 64 | PCIE\_RXN3 |
| 65 | PCIE\_TXP2 | 66 | GND | 67 | PCIE\_TXN2 | 68 | GND |
| 69 | GND | 70 | PCIE\_RXP2 | 71 | GND | 72 | PCIE\_RXN2 |
| 73 | PCIE\_TXP1 | 74 | GND | 75 | PCIE\_TXN1 | 76 | GND |
| 77 | GND | 78 | PCIE\_RXP1 | 79 | GND | 80 | PCIE\_RXN1 |
| 81 | PCIE\_TXP0 | 82 | GND | 83 | PCIE\_TXN0 | 84 | GND |
| 85 | GND | 86 | PCIE\_RXP0 | 87 | GND | 88 | PCIE\_RXN0 |
| 89 | CLK\_100M\_P | 90 | GND | 91 | CLK\_100M\_N | 92 | GND |
| 93 | GND | 94 | NC | 95 | RESET# | 96 | GND |
| 97 | SMBCLK | 98 | WAKE# | 99 | SMBDAT | 100 | ID0 |

## 8.4 Network

### 8.4.1 Data Network

The motherboard uses two RJ-45 LAN ports as its primary data network interface at the I/O side.

One I350-BT2 is on board to provide two optional 10/100/1000 data connection.

### 8.4.2 Management Network

The motherboard has two management network interface options for the BMC’s connection.

* 10/100/1000 MDI shared­ NIC connected to RJ45 from I350, driven by the BMC through the RMII/NCSI.
* The MLAN port provides Internet connection with data transfer speeds of 10/100/1000Mbps. This port is the dedicated LAN port for server management.

### 8.4.3 IPv4/IPv6 Support

The motherboard needs to be deployed in both IPv4 and IPv6 network environments. All data networks and management networks should have this capability. This includes, but is not limited to:

* DHCP and static IP settings
* PXE booting capability
* NIC and BMC firmware support
* OS drivers
* Utilities in both IPv4 and IPv6.

## 8.5 USB

The motherboard requires one external USB port at the front and two at rear. The BIOS should support the following devices on the motherboard’s USB ports:

* USB Keyboard and mouse
* USB flash drive (bootable)
* USB hard drive (bootable)
* USB optical drive (bootable)

## 8.6 SATA

The motherboard has PCH on board. PCH has a SATA controller support for SATA3 ports, and an sSATA controller to support SATA3 ports.

The HDDs are attached to all SATA connectors and must follow the spin­up delay requirement described in section 7.5.3.

## 8.7 Debug Header

The motherboard has one header alternative support TPM or port 80 debug.

Connector on the motherboard should use PINREX 52S-90-14GB10 or an equivalent connector.

### 8.7.1 Post Codes

The post codes reach the debug header in hexadecimal format via two hexadecimal codes. The hexadecimal codes can be driven by either the legacy parallel port (port 80) on SIO, or by 8 GPIO pins. A debug card with two seven segments displays two hexadecimal- to­ seven segment converters and a logic level to RS­232 shifter. A RS­232 connector shall interface with the debug header.

During POST, the BIOS should also output POST codes to BMC SOL. When a SOL session is available during POST, a remote console should show the POST codes as mentioned in Section 5.2.

During the boot sequence, the BIOS shall initialize and test each DIMM module. If a module does not initialize or does not pass the BIOS test, post codes should flash on the debug card to indicate which DIMM has failed. The first hexadecimal character indicates which CPU interfaces with the DIMM module. The second hexadecimal character indicates the number of the DIMM module. The POST code will also display the error major code and error minor code from the Intel memory reference code. The display sequence will be “00”, DIMM location, error major code and error minor code with a one second delay between every code displayed. The BIOS shall repeat the display sequence indefinitely to allow time for a technician to service the system. The DIMM location code table is TBD. The DIMM number count starts from the furthest DIMM from the CPU.

### 8.7.2 Serial Console

The debug card shall contain the output stage of the system’s serial console. The TX and RX signals from the system UART shall be brought to the debug header at the chip's logic levels (+3.3V). The debug card will contain 4pin (2.54mm pin pitch) connector with the pin definition shown in the table below. A separate convertor is needed to provide a RS­232 transceiver and a DB9 connector.

Table 10: Debug Card Mini-USB UART Pins

|  |  |
| --- | --- |
| **Pin** | **Function** |
| 1 | VCC (+3.3V) |
| 2 | RX |
| 3 | TX |
| 4 | GND |

### 8.7.3 Other Debug Use Design Requirements on the Motherboard

An XDP header is required for BIOS debug and should be populated in both EVT and DVT samples. Access to the XDP header should not be mechanically blocked by the CPU heat sink or other components.

The SMBUS debug header should be inserted for the SMBUS on the motherboard based on SMBUS topology vendor designs. SMBUS debug headers for PCH host bus and CPU/DIMM VR PMBus are required.

If any other testing/debugging header is needed based on Intel platform development requirements, it should be added and populated in both EVT and DVT samples.

## 8.8 Pin headers and LEDs

The motherboard shall include a pin header for Front IO panel board. A pin header for HDD back plane board.

### 8.8.1 FP\_1 pin header

Connect the power switch, reset switch, chassis intrusion switch/sensor and system status indicator on the chassis to this header according to the pin assignments below. Note the positive and negative pins before connecting the cables.



Figure 8: Front IO panel connector

Table 11: Pin Description

**⚫ FP\_1**

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin No.** | **Definition** | **Pin No.** | **Definition** |
| 1 | Power LED+ | 2 | 5V Standby |
| 3 | No Pin | 4 | ID\_LED+ |
| 5 | Power LED- | 6 | LD\_LED- |
| 7 | HDD\_LED+ | 8 | System Front Board LED+ |
| 9 | HDD\_LED | 10 | System LED- |
| 11 | Power Button | 12 | LAN1 Active LED+ |
| 13 | GND | 14 | LAN1 Link LED- |
| 15 | Reset Button+ | 16 | SMBus Data |
| 17 | GND | 18 | SMBus Clock |
| 19 | ID Switch+ | 20 | Case Open |
| 21 | ID Switch- | 22 | LAN2 Active LED+ |
| 23 | NMI Switch- | 24 | LAN2 Link LED- |

### 8.8.2 BP\_1 pin header

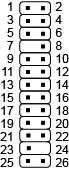


Figure 9: HDD back plane connector

Table 12: Pin Description

**⚫ BP\_1**

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin No.** | **Definition** | **Pin No.** | **Definition** |
| 1 | BP\_SGP\_CLK | 2 | NC |
| 3 | BP\_SGP\_GLD | 4 | FAN\_GATE\_N |
| 5 | BP\_SGP\_DOUT | 6 | GND |
| 7 | KEY | 8 | RESET |
| 9 | GND | 10 | BP\_LED\_A\_N |
| 11 | BP\_LED\_G\_N | 12 | GND |
| 13 | BP\_SGP\_DIN | 14 | NC |
| 15 | GND | 16 | SMB\_BP\_DATA |
| 17 | GND | 18 | SMB\_BP\_CLK |
| 19 | P\_3V3\_AUX | 20 | BMC\_ACK |
| 21 | P\_3V3\_AUX | 22 | BMC\_REQ |
| 23 | GND | 24 | KEY |
| 26 | BP\_PRESENSE | 26 | GND |

### 8.8.3 Front Panel LED and Buttons

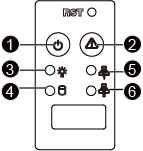
****

Figure 10: Front Panel LED and Button

Table 13: Function Description

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **No.** | **Name** | **Color** | **Status** | **Description** |
| 1 | Reset Button |  |  | Press the button to reset the system. |
| 2 | ID Button |  |  | Press the button to activate system identification. |
| 3 | Power LED | Green | Solid On | System is powered on |
| Green | Blink | System is in ACPI S1 state (sleep mode) |
| N/A | Off | * System is not powered on or in ACPI S5 state (power off) * System is in ACPI S4 state (hibernate mode) |
| 4 | HDD Status LED | Green | Solid On | HDD locate |
| Blink | HDD access |
| Amber | On | HDD fault |
| Green/Amber | Blink | HDD rebuilding |
| N/A | Off | * No HDD access * No HDD fault |
| 5 | LAN1 Active/  Link LED | Green | Solid On | Link between system and network or no access |
| Green | Blink | Data transmission or receiving is occurring |
| N/A | Off | No data transmission or receiving is occurring |
| 6 | LAN2 Active/  Link LED | Green | Solid On | Link between system and network or no access |
| Green | Blink | Data transmission or receiving is occurring |
| N/A | Off | No data transmission or receiving is occurring |

### 8.8.4 Rear System LAN LEDs

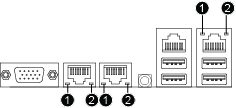


Figure 11: Rear System LAN LED

Table 14: LED Description

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **No.** | **Name** | **Color** | **Status** | **Description** |
| 1 | 1GbE Speed LED | Yellow | On | Link between system and network or no access |
| Green | On | Data transmission or receiving is occurring |
| N/A | Off | No data transmission or receiving is occurring |
| 2 | 1GbE Link/  Activity LED | Green | On | Link between system and network or no access |
| Blink | Data transmission or receiving is occurring |
| N/A | Off | No data transmission or receiving is occurring |

### 8.8.5 Hard Disk Drive LEDs



Figure 12: HDD LEDs

Table 15: LED Description

|  |  |  |  |
| --- | --- | --- | --- |
| **No.** | **Description** | **Multi-Color LEDs** | |
|  |  | LED Active  Green | LED Active  Amber |
| 1. | HDD Access | Blink | Off |
| HDD Locate | On | Off |
| HDD Failure | Off | On |
| HDD connected and rebuilding data | Blink | Blink  (Alternative) |
| 2. | Reserved |  | |

## 8.9 Fan Connector

The system back plane board has twelve system fan connectors, .Most fan Connector possess a foolproof insertion design. When connecting a fan cable, be sure to connect it in the correct orientation (the black connector wire is the ground wire). For optimum heat dissipation, it is recommended that a system fan be installed.



Figure 13: Fan Connector

Table 16: Pin Description

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin No.** | **Definition** | **Pin No.** | **Definition** |
| 1 | GND | 2 | +12V |
| 3 | Sense | 4 | Speed Control |

## 8.10 TPM Connector and Module

A 14pin vertical receptacle connector is defined on the motherboard for the LPC TPM module. The connector pin definition on the motherboard side is shown in the table below. Use a PINREX 52S-90-14GB10 receptacle or its equivalent on the motherboard.



Figure 14: TPM connector

Table 17: Pin Description

**⚫ TPM**

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin No.** | **Definition** | **Pin No.** | **Definition** |
| 1 | GND | 2 | P3V3\_AUX |
| 3 | LPC\_RST | 4 | P3V3 |
| 5 | LPC\_LAD0 | 6 | IRQ\_SERIAL |
| 7 | LPC\_LAD1 | 8 | TPM\_DET\_N |
| 9 | LPC\_LAD2 | 10 | NC |
| 11 | LPC\_LAD3 | 12 | GND |
| 13 | LPC\_FRAME\_N | 14 | GND |

# 9 Mechanical

Mechanically, The Chassis follow SSI Rack spec. EIA-310D Standard cabinet Dimensions and Volumetric.

## 9.1 Chassis

For Rack request, Chassis design follow EIA-310D dimensions and volumetric. Chassis Widths 430mm (SSI spec: under 450mm) and Chassis height keep under 43.5mm (SSI 1U spec: 44.45mm). and Chassis length support 900mm Cabinet enclosure.

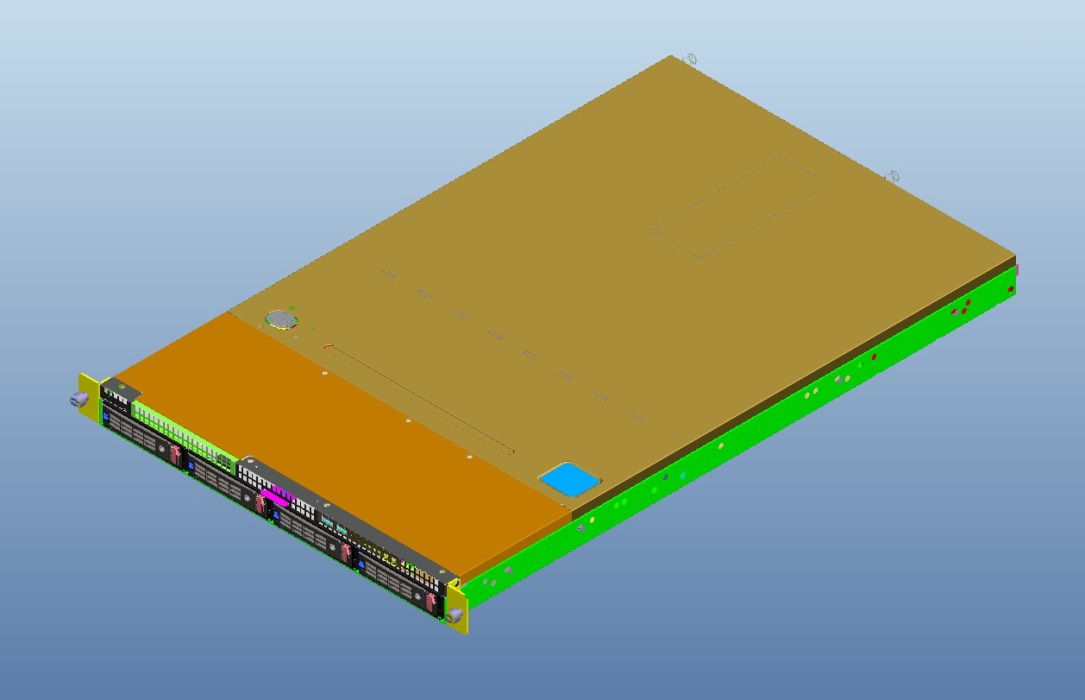
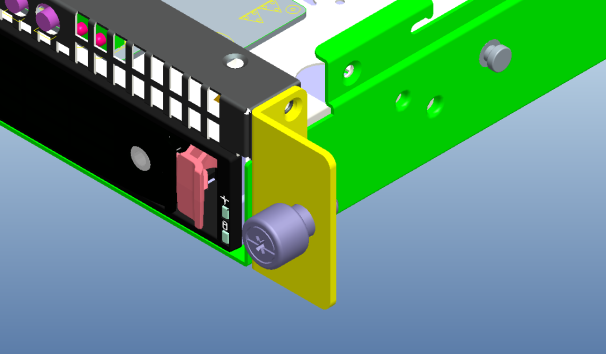


Figure 15: Chassis

## 9.2 Rail kits

Our Chassis ear bracket design support EIA-310D standard mounting flange and hole. Rail kits design follow EIA-310D specifications.



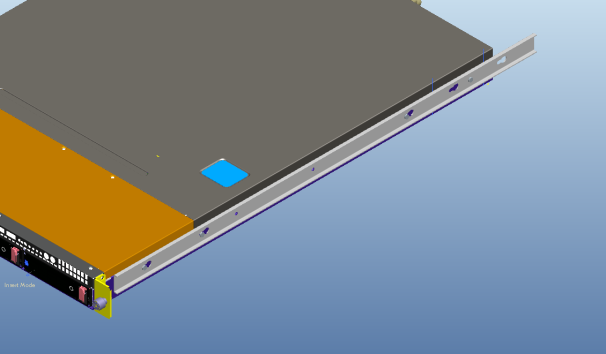


Figure 16: Rail kits

## 9.3 PCIe and HDD bracket

There is a metal bracket near the I/O side of the tray to provide mechanical support for two full­ height PCIe cards, a Low-profile PCIe or Gigabyte universal Mezzanine card and 3.5" hard drive module.

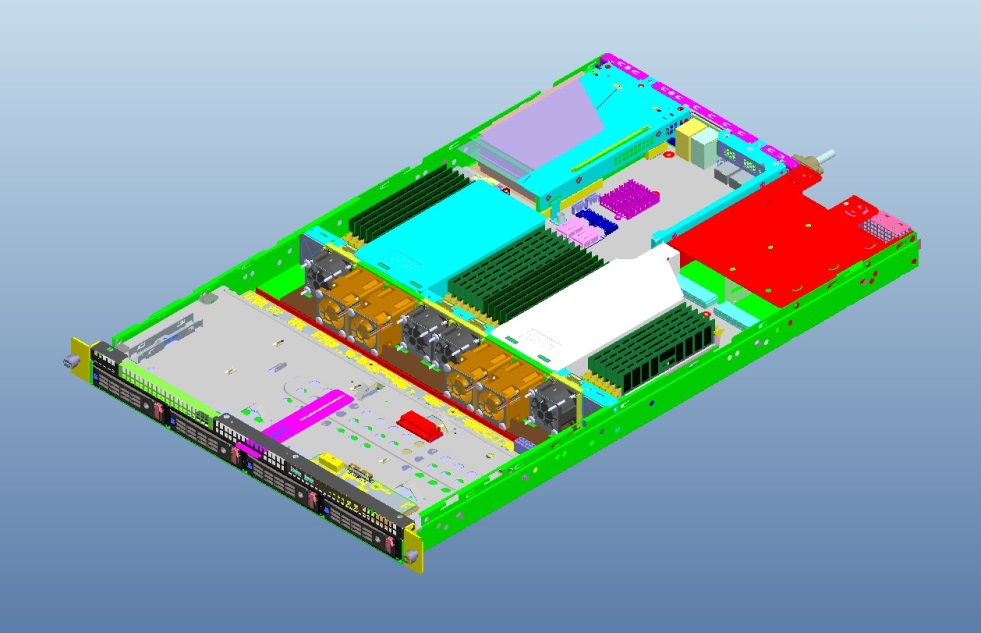


Figure 17: Overview

## 9.4 Fixed Locations

Refer to the mechanical DXF file for the fixed locations of the mounting holes, the 24/16 PCI­E slots and the CRPS power connector.

## 9.5 PCB Thickness

To ensure proper alignment of the motherboard and the midplane interface within mechanical enclosure, the motherboard should follow PCB stack up in Table 1 to have 71.4 mil (1.81mm) PCB thickness. Mezzanine card, interposer card and riser card PCB thickness should be 62 mil (≈1.6mm).

## 9.6 Heat Sinks and Independent Loading Mechanism (ILM)

The motherboard shall support heat sinks that are mounted according to the Intel CPU thermal mechanical specification and design guide. The vendor shall comply with all keep out zones defined by Intel in the above referenced specification. A standard heat sink and square independent loading mechanism (ILM) solution is preferred.

## 9.7 DIMM Connector Color

Colored DIMM connectors shall be used to indicate the first DIMM of each memory channel. The first DIMM on each channel is defined as the DIMM placed physically furthest from its associated CPU. This DIMM connector shall be populated first when the memory is only partially populated. The First DIMM connector shall be Blue, remains are black.

## 9.8 PCB Color

PCB colors shall be blue.

# 10 Environmental Requirements

The motherboard must meet the following environmental requirements:

* Ambient operating temperature range: 0°C to +35°C
* Operating and storage relative humidity: 20% to 95% (non­‐condensing)
* Storage temperature range: ­‐40°C to +60°C
* Transportation temperature range: ­‐40°C to +60°C

## 10.1 Vibration and Shock

The motherboard meets shock and vibration requirements according to the following IEC specifications: IEC78­2­(\*) and IEC721­3­(\*) Standard & Levels. The testing requirements are listed in Table below.

Table 18: Vibration and Shock Requirements

|  |  |  |
| --- | --- | --- |
|  | Operating | Non-operating |
| Vibration | 0.25g acceleration, 5 to 250 Hz, 2 sweeps at 0.5 octave / minute for each of the three axes | 2.2g acceleration, 0.001g2/Hz~0.01g2/Hz from 5~20 Hz , 0.01g2/Hz from 20~500 Hz 10 minutes for each of the three axes |
| Shock | 2g, half­‐sine 11mS, 1 shocks for each of the three axes | 35g, half­‐sine 11mS, 1 shocks for each of the three axes |

# 11 Compliance and interoperability

Describe the areas for test for the platform/system.

OS requirement on Ubuntu

1. Motherboard Specification

 CPU / Memory

- CPU Information

- Processor Topology

- Memory Information

 Platform Controller Hub

- SATA Port

- USB Port

 BIOS Setup Menu

- Scenario 3: BIOS/firmware update

- Scenario 4: Use BMC to update BIOS

 Sensors Monitoring

- In-band Sensors Monitoring

- OOB Sensors Monitoring

- Thermal Monitoring

- Power Monitoring

 Baseboard Management Controller (BMC)

- Fan Speed Control from in-band access

- Fan Speed Control from out-of-band access

- BMC Firmware Update

 Power Policy

- Power Policy/last-state

- Power Policy/always-on

- Power Policy/always-¬off

2. Hardware Management

 Initial Machine Provisioning

- DHCP Lease Information

- Monitor Attachment

 Rights and Credentials

- BMC Default Credential Validation

- BMC Default Credential Change

 Boot Order / PXE

- Boot Order / PXE

 Remote Serial Console

- Enable SOL

- SOL Operation

 Remotely Power Control

- Remotely Power Off and ON

- Remotely Hard Reset

- Remotely Warm Reboot

 Temperature

- Temp Sampling Increment

 User Levels

- Verify BMC Account Privilege : User

- Verify BMC Account Privilege : Operator

- Verify BMC Account Privilege : Administrator

 Inventory

- FRU

 System Log

- System Log Entries

- System Log Hardware Error

- System Log PET Format

3. System Information and Interoperability

 System Information

- Disk Information

- BIOS Information

- NIC Information

- RAID Card Information

 Network Interface Controller

- Network performance

 Hard Disk Drive

- Bad Block Test

 System Idle and Stress Test

- 24 Hours Idle

- System Stress

 JBOD Testing

- Get All HDDs

- Build RAID 5

- Build RAID 0

- RAID 5 Availability Test

- RAID 0 Availability Test

- Rebuild RAID 5