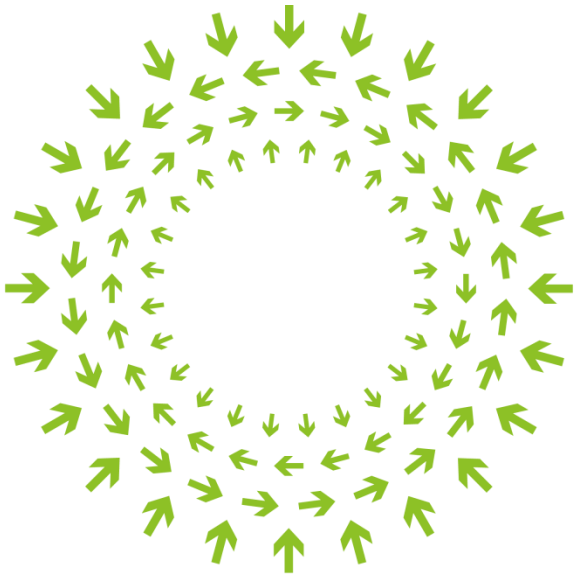

OPEN

Compute Project

Facebook – Backpack

128 x 100GE Modular Switch

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1. Revision History

Date/Version	Name	Description
11/07/2016, v0.92	Zhiping Yao	The first public draft of Backpack system specification
02/14/2017, v1.00	Zhiping Yao	Update specification to include new diagram and pictures, add LED behavior content
02/18/2017, v1.10	Zhiping Yao	Add CPLD register map for CMM, SCM, LC, FAB and FCB

2. Scope

This document outlines the technical specifications for Facebook's Backpack Open Modular Switch Platform submitted to the Open Compute Foundation

3. Contents

4. Overview

4.1. Scope

The purpose of this document is to provide a high level description of the Backpack modular switch platform, its software accessible interfaces, and required software actions to properly manage the hardware at the system level. Refer to the individual module functional specifications for additional detail.

The Backpack system uses Broadcom BCM56960 (a.k.a Tomahawk) Switch Chip which can support 32 x 100GE ports.

4.2. System Description

Backpack is Facebook's next generation datacenter modular switching platform. The main attributes are:

- Chassis Size
  - G4: 4 line cards Chassis
- Line card(LC)
  - 32 QSFP28 100G port blade
- Fabric Card(FAB)
  - G4 FAB: 1 tomahawk
- Control plane
  - intel based CPU, it is 1 to 1 mapping to switch ASIC
  - industrial standard COM-E CPU module
  - System Control Module (SCM) can have two COM-E CPU module.
- Data plane Switching ASIC
  - Broadcom: BCM56960 a.k.a Tomahawk
  - 2nd ASIC: TBD
- Management Plane
  - Chassis Management Module
    - OOB GbE Switch for all COM-e and BMC inside Backpack Chassis
    - UART mux
    - I2C chassis management bus
  - Each SWE (Switch Element) has one AST1250 BMC
  - CMM has AST2520 BMC for chassis level management
  - Two CMM for 1:1 redundancy
- Power Plane
  - 2+2 PSU redundant
  - 90VAC to 300VAC input
  - 12V output

4.3. Common terms

The following terms are used in Backpack project:

- 10GE – 10 Gigabit Ethernet
- 40GE – 40 Gigabit Ethernet
- 100GE – 100 Gigabit Ethernet
- Tomahawk – Broadcom BCM56960 3.2T TOR switch ASIC
- G4 - four slot chassis, 128x QSFP28 100G ports
- G8 - eight slot chassis, 256x QSFP28 100G ports
- LC - Line Card
- FAB – Fabric Module
- FCC – Fabric Cross-connect Card
- SCM – System Controller Module
- CMM – Chassis Management Module
- VCP – Vertical Control Plane
- HCP – Horizontal Control Plane
- BBA – Bus Bar Assembly. Consists of HBAR, HPD, and VBAR
- VBAR – Vertical Power Bus Bar
- HBAR – Horizontal Power Bus Bar.
- HPD – Horizontal Power Distribution, Part of copper Bus Bar
- COM-E – COM-Express CPU module
- PDB – Power Distribution Board
- FCB – Fan-tray Control Board
- PCIe – PCI express
- SIM – System Information Module
- PSU – Power Supply Unit. Converts 48V DC or AC line voltage to system 12V

4.4. Chassis

In the initial deployment we focus on G4. In principle the design can be extended to G8 and G16.

- G4: 13.85” (H) x 17.44”(W) x 29.5”” (D)

Figure 1: Backpack Chassis front ISO View

Figure 2: Backpack Rear ISO View

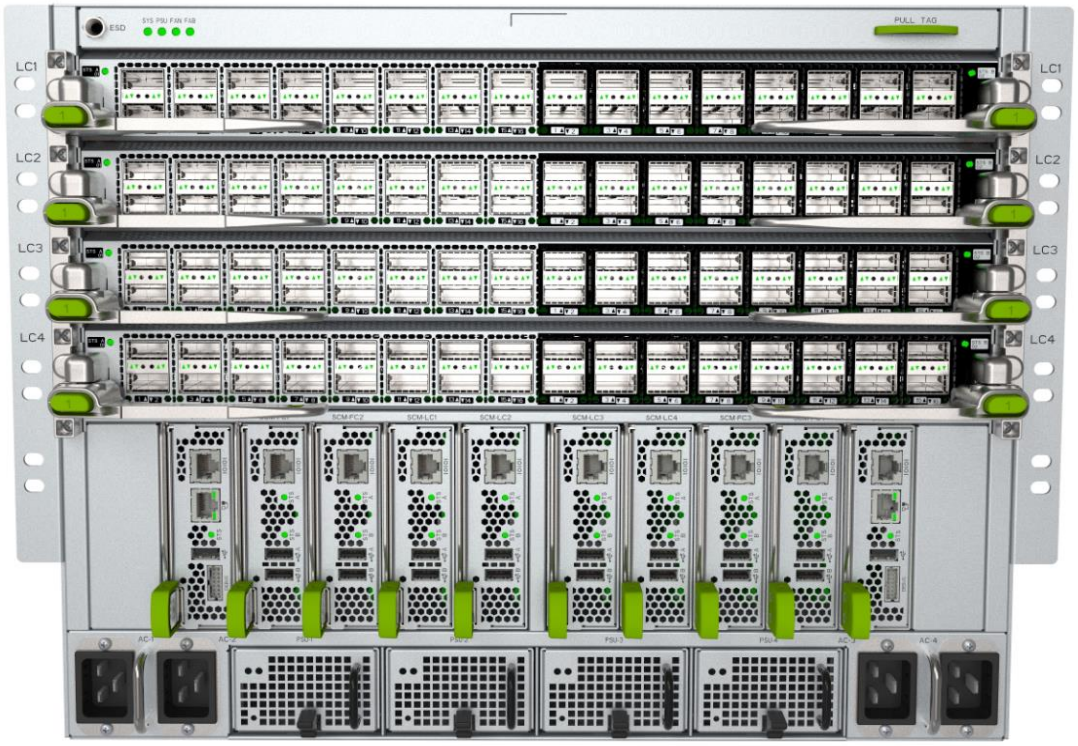

Figure 3: Backpack Front View

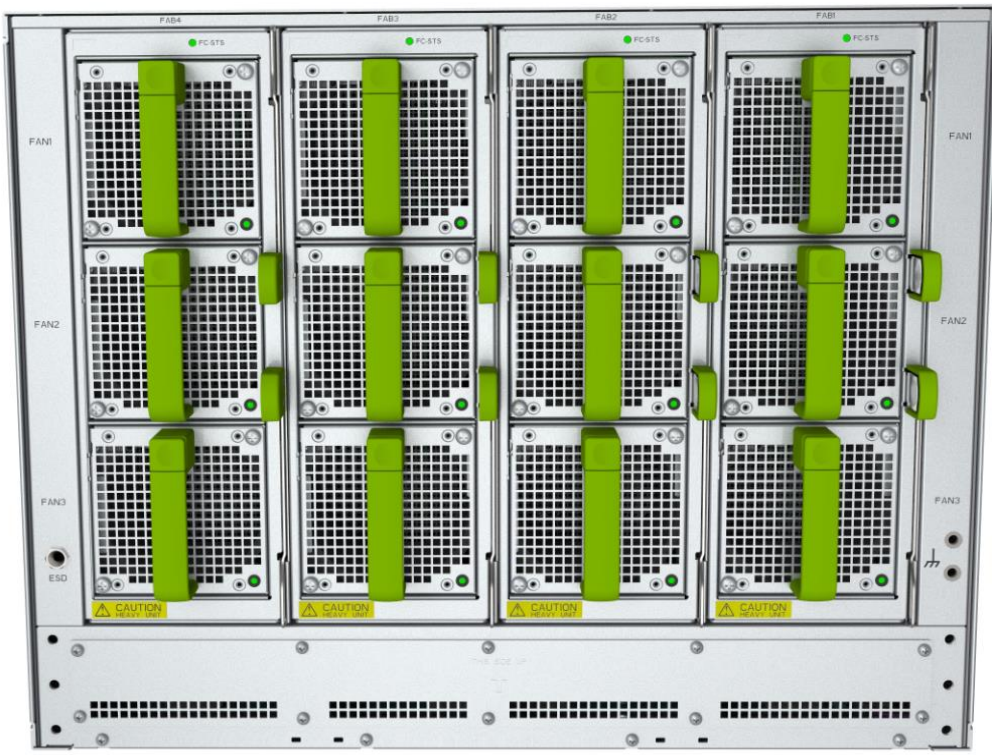

Figure 4: Backpack Rear View With Fantray

5. System Components

Backpack chassis consists of the following components:

- Chassis Management Module (CMM)
- System Controller Module (SCM)
  - SCM for LC (SCM-LC)
  - SCM for FAB (SCM-FAB)
- Line Cards (LC)
- Fabric Card (FAB)
- Bus Bar Assembly (BBA)
  - Horizontal Bus Bar (HBAR)
  - Vertical Bus Bar (VBAR)
  - Horizontal Power Distribution Board (HPD)
- Horizontal Control Plane (HCP)
- Vertical Control Plane (VCP)
  - VCP Left (VCP-L)
  - VCP Right (VCP-R)
- Fan Control Board (FCB)
- Power Supply Unit (PSU)
- Power Distribution Board (PDB)

The line card (LC), System Controller Module (SCM), Chassis Management Module (CMM) and power supply (PSU) plug into the front side of the chassis. The switch fabric (FAB), fan FRU are accessed from the rear side of the chassis.

FRU Type	Name	Quantity
Line Card	LC	4
Fabric Card	FAB	4
System Controller Module	SCM	8
Chassis Management Module	CMM	2
FAN Module	FAN	12
PSU	PSU	4

Table 1: FRU Type

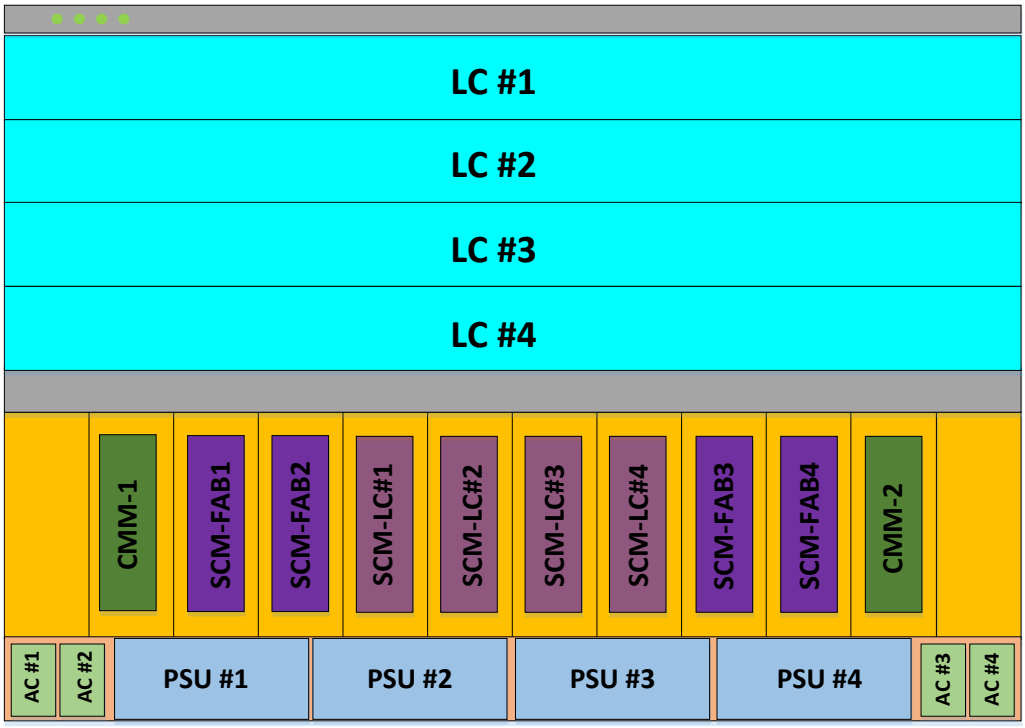

Figure 5: Backpack front View with FRU numbering

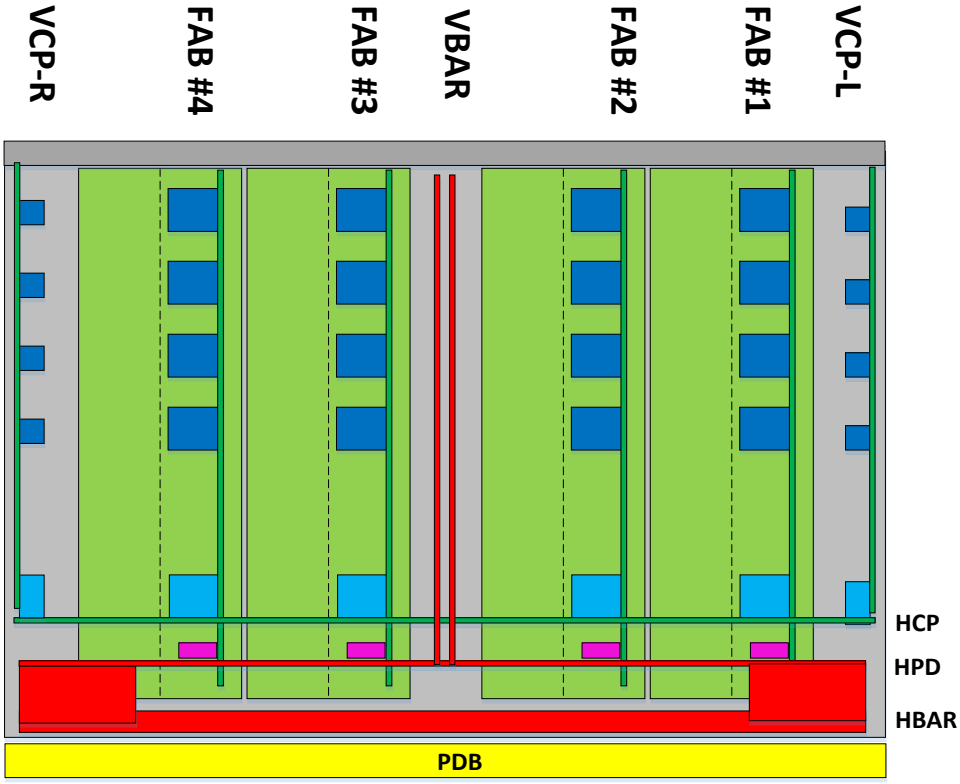

Figure 6: Backpack Rear View with FRU Numbering

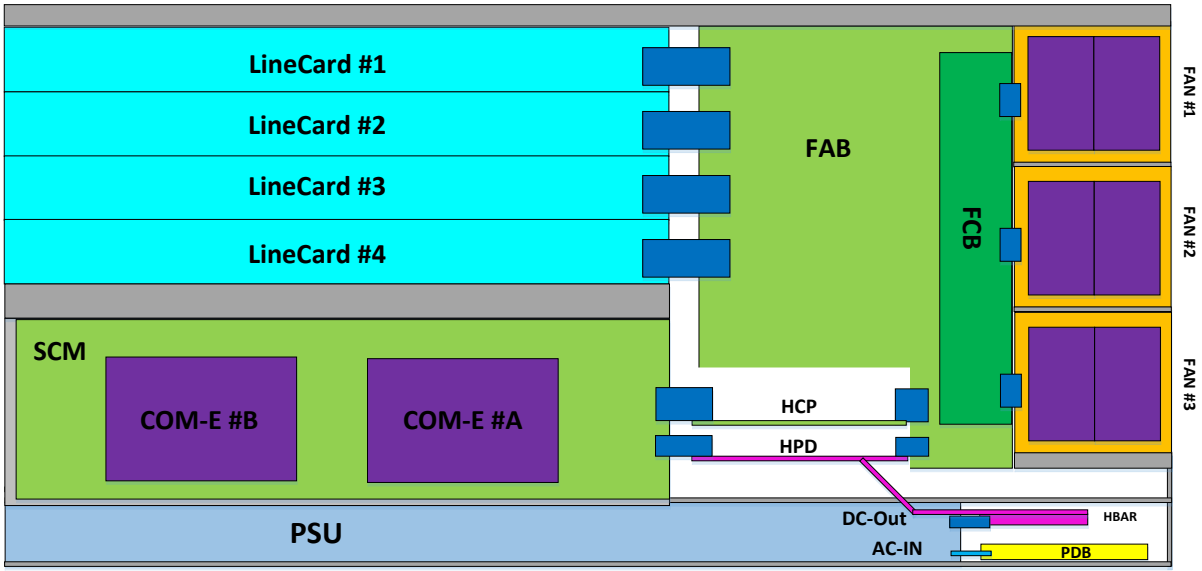

Figure 7: G4 Chassis Side View

5.1. Line Card

The line card (LC) provide network interface for Backpack. 32 port of 100G QSFP28 ports are supported on front panel. Each QSFP28 port can be configured as 100G mode, 2x50G mode, 4x25G mode, 40G mode, or 4x10G mode. 100G and 40G mode are the most common used port mode in Backpack platform.

5.1.1. Block Diagram of LC

Each line card has the following components:

- Two Switch Element (SWE) on LC
- Two tomahawk Switch ASIC, each Switch ASIC is part of one Switch Element (SWE).
- 32 x 100G QSFP28 ports on front panel
- 32 x 100G interface (32x4x25G SERDES) to four Orthogonal Fabric Cards
- BMC AST1250 is used for Board Management. One BMC per one switch Element.
- A eight port SGMII GBE Switch BCM5389 is used for OOB switch to connect to CMM1, CMM2, BMC, SCM-COM-E, Tomahawk Management port(configured as SGMII), on board debug RJ45 port, 2 ports are unused.
- Control signals connect to VCP
- Power is provided by VBAR, part of BBA
- Multiple temperature sensors can be accessed by CMM

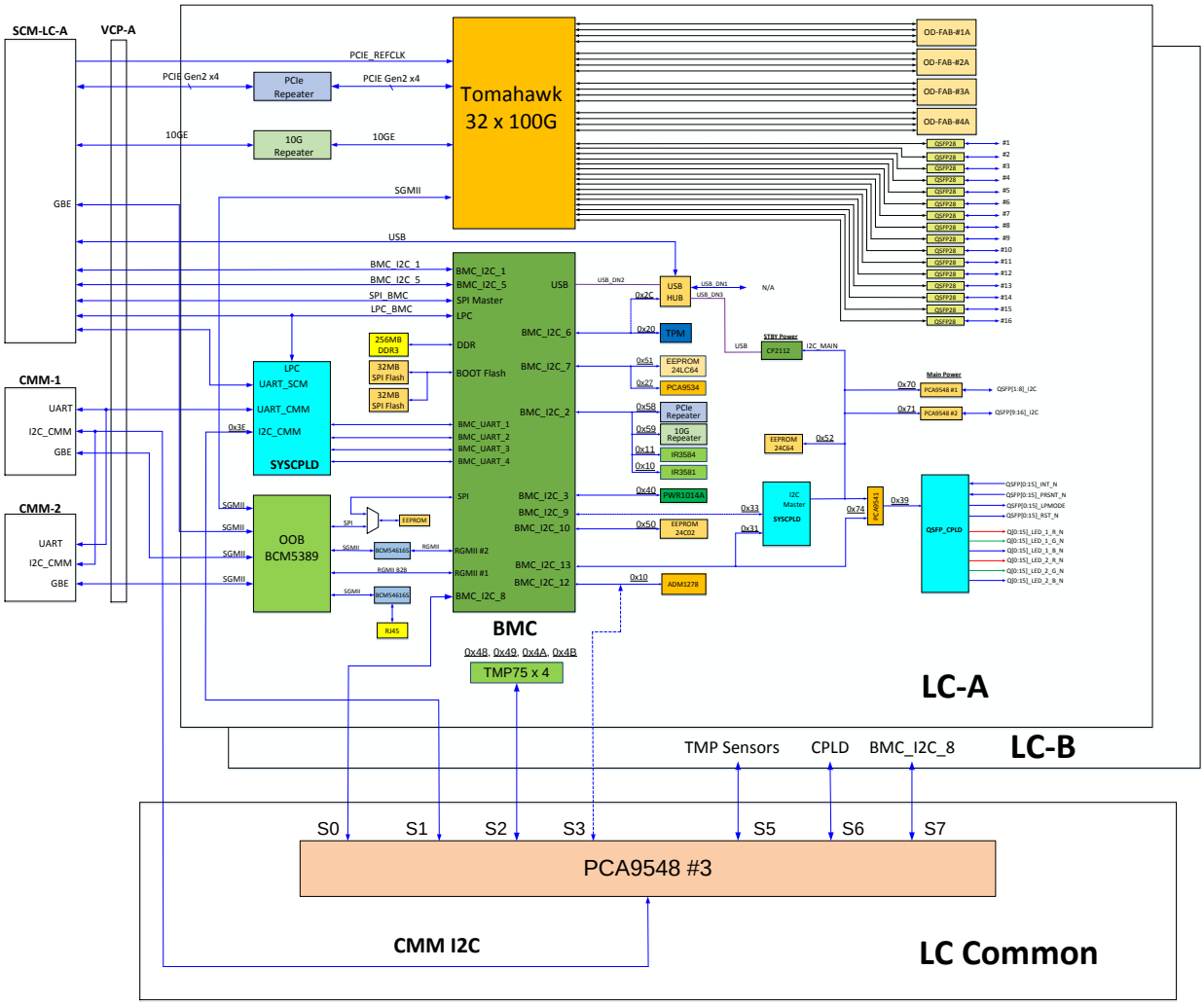

Figure 8: Line Card Block Diagram

5.1.2. Line Card QSFP28 ports

The following diagram shows the front panel QSFP28 port mapping of Line Card. the left 16 ports connect to tomahawk A, and the right 16 ports connect to tomahawk B.

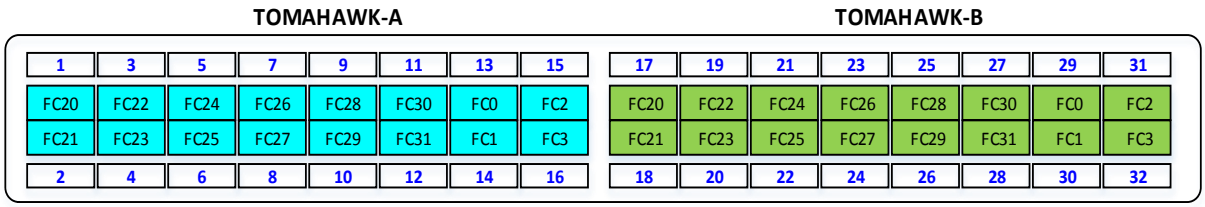

Figure 9: Backpack LC QSFP28 Port Mapping

Figure 10: LC front Panel

5.1.3. Line Card QSFP28 Control

Each one of the two SWE of LC has one dedicated CPLD to control QSFP28 interface. The QSFP CPLD can be accessed by both BMC and COM-e in order for software to control or check status of QSFP28 modules.

The following functions are supported by QSFP CPLD:

- QSFP28 port LED control
- QSFP28 Reset Control (QSFP_RESET_N[16:1])
- QSFP28 LPMODE control (QSFP_LPMODE[16:1])
- QSFP28 Interrupt status (QSFP_INT_N[16:1])
- QSFP28 module present status (QSFP_ABS[16:1])

5.1.4. Line Card Port Mapping

The following table shows the port mapping for QSFP ports of Tomahawk-A, the switch ASIC of left SWE.

TOMAHAWK-A								
SDK Port No.	Port No.	TD/RD Lane	FalconCore		TD Lane	RD Lane	TD P/N reversal	RD P/N reversal
CE0	zQSFP1	Lane 0	FalconCore 20	Lane	1	1	N	N
		Lane 1		Lane	3	3	Y	N
		Lane 2		Lane	0	0	N	N
		Lane 3		Lane	2	2	N	N
CE1	zQSFP2	Lane 0	FalconCore 21	Lane	2	2	Y	N
		Lane 1		Lane	0	0	Y	N
		Lane 2		Lane	3	3	N	N
		Lane 3		Lane	1	1	N	N
CE2	zQSFP3	Lane 0	FalconCore 22	Lane	1	1	N	N
		Lane 1		Lane	3	3	Y	N
		Lane 2		Lane	0	0	N	N
		Lane 3		Lane	2	2	N	N
CE3	zQSFP4	Lane 0	FalconCore 23	Lane	2	2	N	Y
		Lane 1		Lane	0	0	N	Y
		Lane 2		Lane	3	3	Y	Y
		Lane 3		Lane	1	1	Y	Y
CE4	zQSFP5	Lane 0	FalconCore 24	Lane	1	1	Y	Y
		Lane 1		Lane	3	3	N	Y
		Lane 2		Lane	0	0	Y	Y
		Lane 3		Lane	2	2	Y	Y
CE5	zQSFP6	Lane 0	FalconCore 25	Lane	2	2	N	N
		Lane 1		Lane	0	0	N	N
		Lane 2		Lane	3	3	Y	N
		Lane 3		Lane	1	1	Y	N
CE6	zQSFP7	Lane 0	FalconCore 26	Lane	1	1	Y	Y
		Lane 1		Lane	3	3	N	Y
		Lane 2		Lane	0	0	Y	Y
		Lane 3		Lane	2	2	Y	Y
CE7	zQSFP8	Lane 0	FalconCore 27	Lane	2	2	Y	N
		Lane 1		Lane	0	0	Y	N
		Lane 2		Lane	3	3	N	N
		Lane 3		Lane	1	1	N	N
CE8	zQSFP9	Lane 0	FalconCore 28	Lane	1	2	Y	Y
		Lane 1		Lane	2	1	N	Y
		Lane 2		Lane	3	0	Y	Y
		Lane 3		Lane	0	3	Y	Y

CE9	**zQSFP10**	Lane 0	**FalconCore 29**	**Lane**	2	0	N	Y
		Lane 1		**Lane**	0	2	N	Y
		Lane 2		**Lane**	3	1	Y	Y
		Lane 3		**Lane**	1	3	Y	Y
CE10	**zQSFP11**	Lane 0	**FalconCore 30**	**Lane**	2	0	N	Y
		Lane 1		**Lane**	0	2	Y	Y
		Lane 2		**Lane**	3	1	N	Y
		Lane 3		**Lane**	1	3	N	Y
CE11	**zQSFP12**	Lane 0	**FalconCore 31**	**Lane**	1	3	N	Y
		Lane 1		**Lane**	3	1	N	Y
		Lane 2		**Lane**	0	2	Y	Y
		Lane 3		**Lane**	2	0	Y	Y
CE12	**zQSFP13**	Lane 0	**FalconCore 0**	**Lane**	2	0	Y	Y
		Lane 1		**Lane**	0	2	N	Y
		Lane 2		**Lane**	3	1	Y	Y
		Lane 3		**Lane**	1	3	Y	Y
CE13	**zQSFP14**	Lane 0	**FalconCore 1**	**Lane**	2	0	N	Y
		Lane 1		**Lane**	0	2	N	Y
		Lane 2		**Lane**	3	1	Y	Y
		Lane 3		**Lane**	1	3	Y	Y
CE14	**zQSFP15**	Lane 0	**FalconCore 2**	**Lane**	2	0	Y	Y
		Lane 1		**Lane**	0	2	N	Y
		Lane 2		**Lane**	3	1	Y	Y
		Lane 3		**Lane**	1	3	Y	Y
CE15	**zQSFP16**	Lane 0	**FalconCore 3**	**Lane**	2	0	N	Y
		Lane 1		**Lane**	0	2	N	Y
		Lane 2		**Lane**	3	1	Y	Y
		Lane 3		**Lane**	1	3	Y	Y

Table 2: LC Tomahawk A Port Mapping

TOMAHAWK-B								
SDK Port No.	**Port No.**	**TD/RD Lane**	**FalconCore**		**TD Lane**	**RD Lane**	**TD P/N reversal**	**RD P/N reversal**
CE0	**zQSFP17**	Lane 0	**FalconCore 20**	Lane	1	1	N	N
		Lane 1		Lane	3	3	Y	N
		Lane 2		Lane	0	0	N	N
		Lane 3		Lane	2	2	N	N
CE1	**zQSFP18**	Lane 0	**FalconCore 21**	Lane	2	2	Y	N
		Lane 1		Lane	0	0	Y	N
		Lane 2		Lane	3	3	N	N
		Lane 3		Lane	1	1	N	N
CE2	**zQSFP19**	Lane 0	**FalconCore 22**	Lane	1	1	N	N
		Lane 1		Lane	3	3	Y	N
		Lane 2		Lane	0	0	N	N
		Lane 3		Lane	2	2	N	N
CE3	**zQSFP20**	Lane 0	**FalconCore 23**	Lane	2	2	N	Y

		Lane 1		Lane	0	0	N	Y
		Lane 2		Lane	3	3	Y	Y
		Lane 3		Lane	1	1	Y	Y
CE4	**zQSFP21**	Lane 0	**FalconCore 24**	Lane	1	1	Y	Y
		Lane 1		Lane	3	3	N	Y
		Lane 2		Lane	0	0	Y	Y
		Lane 3		Lane	2	2	Y	Y
CE5	**zQSFP22**	Lane 0	**FalconCore 25**	Lane	2	2	N	N
		Lane 1		Lane	0	0	N	N
		Lane 2		Lane	3	3	Y	N
		Lane 3		Lane	1	1	Y	N
CE6	**zQSFP23**	Lane 0	**FalconCore 26**	Lane	1	1	Y	Y
		Lane 1		Lane	3	3	N	Y
		Lane 2		Lane	0	0	Y	Y
		Lane 3		Lane	2	2	Y	Y
CE7	**zQSFP24**	Lane 0	**FalconCore 27**	Lane	2	2	Y	N
		Lane 1		Lane	0	0	Y	N
		Lane 2		Lane	3	3	N	N
		Lane 3		Lane	1	1	N	N
CE8	**zQSFP25**	Lane 0	**FalconCore 28**	Lane	1	2	Y	Y
		Lane 1		Lane	2	1	N	Y
		Lane 2		Lane	3	0	Y	Y
		Lane 3		Lane	0	3	Y	Y
CE9	**zQSFP26**	Lane 0	**FalconCore 29**	Lane	2	0	N	Y
		Lane 1		Lane	0	2	N	Y
		Lane 2		Lane	3	1	Y	Y
		Lane 3		Lane	1	3	Y	Y
CE10	**zQSFP27**	Lane 0	**FalconCore 30**	Lane	2	0	N	Y
		Lane 1		Lane	0	2	N	Y
		Lane 2		Lane	3	1	Y	Y
		Lane 3		Lane	1	3	Y	Y
CE11	**zQSFP28**	Lane 0	**FalconCore 31**	Lane	2	0	N	Y
		Lane 1		Lane	0	2	Y	Y
		Lane 2		Lane	3	1	N	Y
		Lane 3		Lane	1	3	N	Y
CE12	**zQSFP29**	Lane 0	**FalconCore 0**	Lane	2	0	Y	Y
		Lane 1		Lane	0	2	N	Y
		Lane 2		Lane	3	1	Y	Y
		Lane 3		Lane	1	3	Y	Y
CE13	**zQSFP30**	Lane 0	**FalconCore 1**	Lane	2	0	N	Y
		Lane 1		Lane	0	2	N	Y
		Lane 2		Lane	3	1	Y	Y
		Lane 3		Lane	1	3	Y	Y
CE14	**zQSFP31**	Lane 0	**FalconCore 2**	Lane	2	0	Y	Y
		Lane 1		Lane	0	2	N	Y

		Lane 2		Lane	3	1	Y	Y
		Lane 3		Lane	1	3	Y	Y
CE15	zQSFP32	Lane 0	FalconCore 3	Lane	2	0	N	Y
		Lane 1		Lane	0	2	N	Y
		Lane 2		Lane	3	1	Y	Y
		Lane 3		Lane	1	3	Y	Y

Table 3: LC Tomahawk B Port Mapping

5.1.5. Line Card Orthogonal Direct Connector Port Mapping

Each LC has four Orthogonal Direct (OD) Connector connecting highspeed signal to four FAB cards. They are numbered from left to right as OD-#1, OD-#2, OD-#3, and OD-#4, the following diagram show the OD connector numbering.

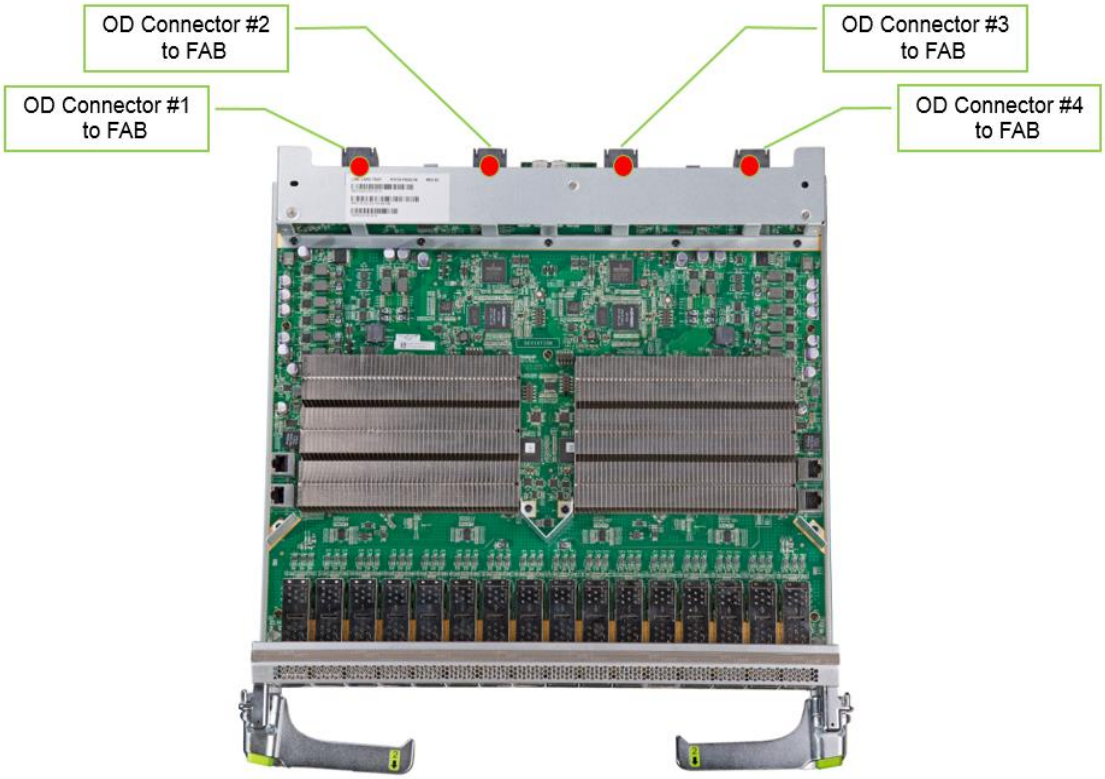

Figure 11: LC OD Connector

Each OD connector has 8 x100G signals, 4 x100G from switch ASIC A, and 4 x100G from switch ASIC B. the OD connector port mapping is shown in the following table:

	SDK Port No.	FC	TD Ln	RD Ln	TD P/N swap	RD P/N swap	Note	OD Port No.
Tomahawk 1	CE16	FC16	3	0	N	N	To FAB 1#	OD1-P0
			2	1	N	N		

			1	2	N	N		
			0	3	N	N		
	CE17	FC17	0	3	N	Y		OD1-P1
			1	2	N	Y		
			2	1	N	Y		
			3	0	N	Y		
	CE18	FC18	0	3	Y	N		OD1-P2
			1	2	Y	N		
			2	1	Y	N		
			3	0	Y	N		
	CE19	FC19	2	3	N	Y		OD1-P3
			1	0	N	Y		
			0	1	N	Y		
			3	2	Y	N		
Tomahawk 2	CE16	FC16	3	3	Y	N		OD1-P4
			0	2	N	N		
			2	0	N	N		
			1	1	N	N		
	CE17	FC17	0	3	N	N		OD1-P5
			1	2	N	N		
			2	1	N	N		
			3	0	N	N		
	CE18	FC18	0	3	Y	Y		OD1-P6
			1	2	Y	Y		
			2	1	Y	Y		
			3	0	Y	Y		
	CE19	FC19	2	3	N	N		OD1-P7
			0	1	N	N		
			1	0	N	N		
			3	2	N	N		
Tomahawk 1	CE20	FC12	0	3	N	Y	To FAB 2#	OD2-P0
			1	2	N	Y		
			2	1	N	Y		
			3	0	N	Y		
	CE21	FC13	0	3	N	Y		OD2-P1
			1	2	N	Y		
			2	1	N	Y		
			3	0	N	Y		
	CE22	FC14	0	3	Y	Y		OD2-P2
			1	2	Y	Y		
			2	1	Y	Y		
			3	0	Y	Y		
	CE23	FC15	0	3	N	Y		OD2-P3
			2	1	N	Y		

			1	2	N	Y		
			3	0	Y	N		
Tomahawk 2	CE20	FC12	0	0	Y	Y		OD2-P4
			3	1	N	Y		
			1	3	N	Y		
			2	2	N	Y		
	CE21	FC13	0	3	N	N		OD2-P5
			1	2	N	N		
			2	1	N	N		
			3	0	N	N		
	CE22	FC14	0	3	Y	N		OD2-P6
			1	2	Y	N		
			2	1	Y	N		
			3	0	Y	N		
	CE23	FC15	0	3	N	N		OD2-P7
			1	2	N	N		
			2	1	N	N		
			3	0	N	N		
Tomahawk 1	CE24	FC8	3	3	Y	N	To FAB 3#	OD3-P0
			2	2	Y	N		
			1	1	Y	N		
			0	0	Y	N		
	CE25	FC9	0	0	N	Y		OD3-P1
			1	1	N	Y		
			2	2	N	Y		
			3	3	N	Y		
	CE26	FC10	3	3	N	Y		OD3-P2
			2	2	N	Y		
			1	1	N	Y		
			0	0	N	Y		
	CE27	FC11	0	0	Y	N		OD3-P3
			2	2	Y	N		
			1	1	Y	N		
			3	3	N	Y		
Tomahawk 2	CE24	FC8	3	0	N	N		OD3-P4
			0	1	Y	N		
			2	3	Y	N		
			1	2	Y	N		
	CE25	FC9	0	0	N	N		OD3-P5
			1	1	N	N		
			2	2	N	N		
			3	3	N	N		
	CE26	FC10	3	3	N	Y		OD3-P6
			2	2	N	Y		
			1	1	N	Y		

			0	0	N	Y		
	CE27	FC11	0	0	Y	Y		OD3-P7
			1	1	Y	Y		
			2	2	Y	Y		
			3	3	Y	Y		
Tomahawk 1	CE28	FC4	3	3	Y	N	To FAB 4#	OD4-P0
			2	2	Y	N		
			1	1	Y	N		
			0	0	Y	N		
	CE29	FC5	0	0	N	Y		OD4-P1
			1	1	N	Y		
			2	2	N	Y		
			3	3	N	Y		
	CE30	FC6	3	3	N	N		OD4-P2
			2	2	N	N		
			1	1	N	N		
			0	0	N	N		
	CE31	FC7	0	0	N	N		OD4-P3
			2	2	N	N		
			1	1	N	N		
			3	3	Y	Y		
Tomahawk 2	CE28	FC4	3	0	N	N		OD4-P4
			0	1	Y	N		
			2	3	Y	N		
			1	2	Y	N		
	CE29	FC5	0	0	N	N		OD4-P5
			1	1	N	N		
			2	2	N	N		
			3	3	N	N		
	CE30	FC6	3	3	N	Y		OD4-P6
			2	2	N	Y		
			1	1	N	Y		
			0	0	N	Y		
	CE31	FC7	0	0	N	Y		OD4-P7
			1	1	N	Y		
			2	2	N	Y		
			3	3	N	Y		

Table 4: LC OD Port Mapping

5.1.6. Line Card I2C diagram

The following diagram shows the I2C architecture of LC.

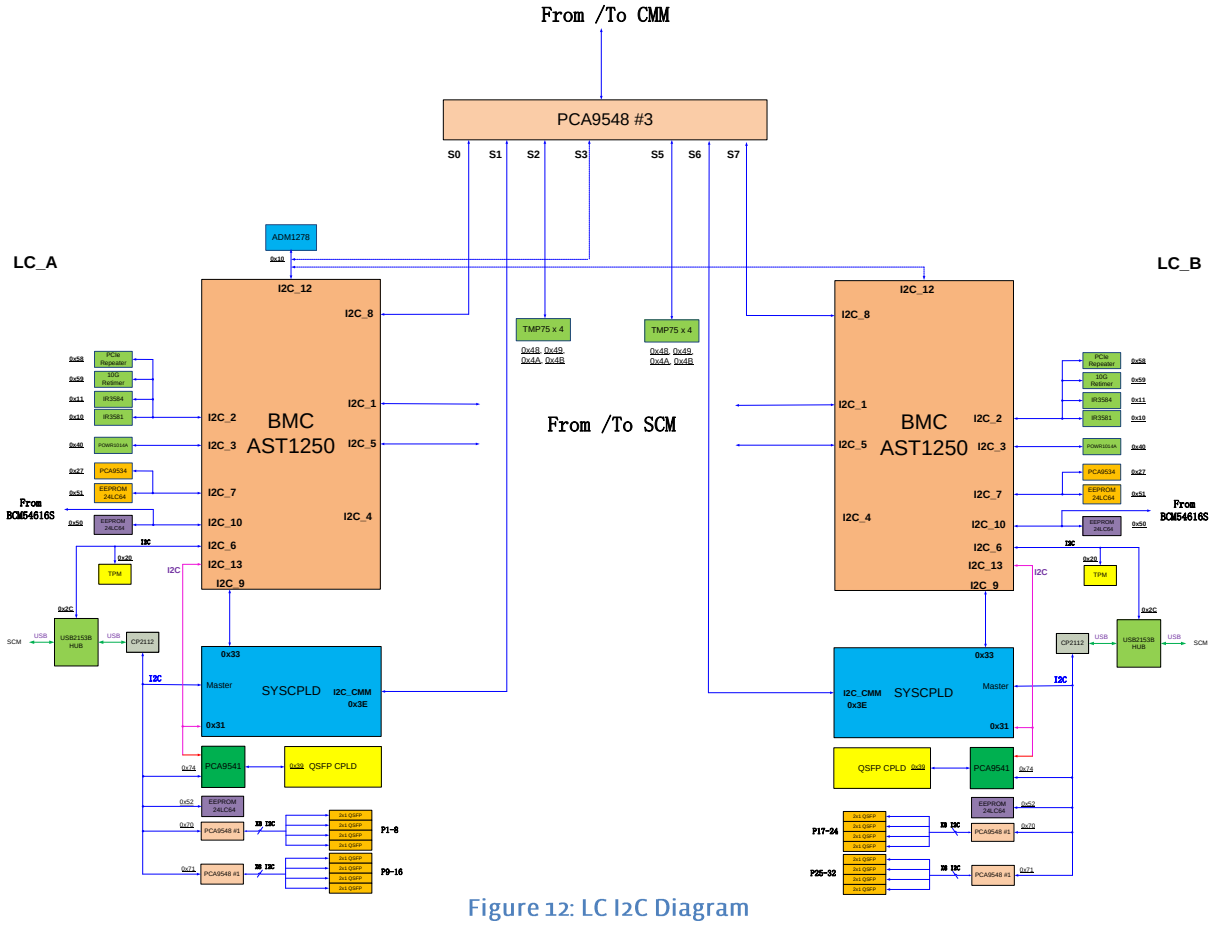

Figure 12: LC I2C Diagram

I2C Controller	I2C/SMbus Address	I2C Device
BMC_I2C_1	0x52	SYS EEPROM (SCM)
	0x54	BCM54616S EEPROM (SCM)
	0x21	PCA9534 (SCM) (LC-A access only)
	0x10	ADM1278 (SCM) (LC-A access only)
	0x58	DS80PCI402 (SCM)
	0x59	DS100BR111 (SCM)
	0x3e	SYS CPLD (SCM)
	0x33	COM-E (SCM)
SCM	TBD	BMC_I2C_5

CMM (PCA9548#3) (PCA9548#3) (PCA9548#3) (PCA9548#3) (PCA9548#3) (PCA9548#3)	0x70 S0: TBD S1: 0x3E S2: 0x48/49/4A/4B S5: 0x48/49/4A/4B S6: 0x3E S7: TBD	PCA9548 #3 BMC_I2C_8 (LC-A) SYSCPLD (LC-A) (Reserved) Thermal sensor (LC-A) Thermal sensor (LC-B) SYSCPLD (LC-B) (Reserved) BMC_I2C_8 (LC-B)
BMC_I2C_2	0x58 0x59 0x11/0x72/0x73 0x10/0x70/0x71	PCIe Repeater (Not used) 10G Repeater IR3584 IR3581
BMC_I2C_3	0x40	POWR1014
BMC_I2C_6	0x2C 0x20	USB2153B (Not used) TPM
BMC_I2C_7	0x27 0x51	PCA9534 EEPROM 24LC64
BMC_I2C_9	0x33	System CPLD (Not used)
BMC_I2C_10	0x50	BCM54616S EEPROM AT24C02
BMC_I2C_12	0x10	ADM1278
BMC_I2C_13 (PCA9541)	0x31 0x74 0x39	System CPLD PCA9541 QSFP CPLD

SYS CPLD	0x70	PCA9548 #1
(PCA9548#1)	S0: 0x50	QSFP28 P1/17 (LC-A/B)
(PCA9548#1)	S1: 0x50	QSFP28 P2/18 (LC-A/B)
(PCA9548#1)	S2: 0x50	QSFP28 P3/19 (LC-A/B)
(PCA9548#1)	S3: 0x50	QSFP28 P4/20 (LC-A/B)
(PCA9548#1)	S4: 0x50	QSFP28 P5/21 (LC-A/B)
(PCA9548#1)	S5: 0x50	QSFP28 P6/22 (LC-A/B)
(PCA9548#1)	S6: 0x50	QSFP28 P7/23 (LC-A/B)
(PCA9548#1)	S7: 0x50	QSFP28 P8/24 (LC-A/B)
	0x71	PCA9548 #2
(PCA9548#2)	S0: 0x50	QSFP28 P9/25 (LC-A/B)
(PCA9548#2)	S1: 0x50	QSFP28 P10/26 (LC-A/B)
(PCA9548#2)	S2: 0x50	QSFP28 P11/27 (LC-A/B)
(PCA9548#2)	S3: 0x50	QSFP28 P12/28 (LC-A/B)
(PCA9548#2)	S4: 0x50	QSFP28 P13/29 (LC-A/B)
(PCA9548#2)	S5: 0x50	QSFP28 P14/30 (LC-A/B)
(PCA9548#2)	S6: 0x50	QSFP28 P15/31 (LC-A/B)
(PCA9548#2)	S7: 0x50	QSFP28 P16/32 (LC-A/B)
	0x52	EEPROM 24LC64
	0x74	PCA9541
(PCA9541)	0x39	QSFP CPLD

Table 5: I2C Devices of Line Card BMC

5.1.7. LC System CPLD Register Map

LC has two CPLD: System CPLD, and QSFP CPLD.

1.1.1 System CPLD Register

BMC access those registers through I2C bus 13 of BMC, the I2C address of SYSCPLD is 0x31. In Logic support CPU & BMC read the register at same time. When write the register at same time the CPU will have higher priority.

The registers in CPLD are accessed by COM-e CPU through LPC interface. The base address in LPC is 0x0100.

Register 0x00: BOARD_VERSION – Board Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	4'b0000	MODEL_ID[4:0] 0000: Backpack LC Type-1 0100: Backpack FAB Type-1 1100: Backpack CMM Type-1	MOD_ID
[3:0]	RO	0	BRD_REV[3:0]: PCB revision	PCB_VER

Register 0x01: CPLD_VERSION – CPLD Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	0	Reserved	Reserved
[6]	RO	0	Released Bit 0= not released, 1= Released version after PVT	RELEASE_STA
[5:0]	RO	Designed	CPLD Revision[5:0]	CPLD_VER

Register 0x02: CPLD_SUB_VERSION – CPLD Sub Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:0]	RO	0x01	CPLD sub-version, HW debug only	CPLD_SUB_VER

Register 0x03: SLOT_ID – Slot ID Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved	Reserved
[3:0]	RO	None	Chassis slot information 0000 Slot-1, LC-#1 0001 Slot-2, LC-#2 0010 Slot-3, LC-#3 0011 Slot-4, LC-#4 0100 Slot-5, LC-#5 0101 Slot-6, LC-#6 0110 Slot-7, LC-#7 0111 Slot-8, LC-#8 1000 Slot-1, FAB-#1 1001 Slot-2, FAB-#2 1010 Slot-3, FAB-#3 1011 Slot-4, FAB-#4 1100 Unused ID 1101 Unused ID 1110 Unused ID 1111 Unused ID	SLOT_ID

Register 0x04: VCP_ID – VCP ID Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:2]	RO	0x0	Reserved	Reserved
[1:0]	RO	None	VCP information	VCP_ID

Register 0x05: SWE_ID – Switch Element ID Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:2]	RO	0x0	Reserved	Reserved
[1:0]	RO	None	LC Switch Element position information 00:LC Card Left Switch Element 01:LC Card Right Switch Element	SLOT_ID

Register 0x06: SYS_LED_CTRL – System LED Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved	Reserved
[3]	R/W	0b0	LED_BLINK_EN 0: LED No blink 1: LED Blink is ON	LED_BLINK
[2]	R/W	0b0	LED_BLUE 0: LED BLUE is OFF 1: LED NLUE is ON	LED_BLU
[1]	R/W	0b0	LED_GREEN 0: LED GREEN is OFF 1: LED GREEN is ON	LED_GRN
[0]	R/W	0b1	LED_RED 0: LED RED is OFF 1: LED RED is ON	LED_RED

Register 0x08: MODULE_PRESENT – Module Present Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:2]	RO	0x3F	Reserved	Reserved
[1]	RW	0b0	SCM OIR Record. Software write 0 to clear this record. 0:SCM OIR Event cleared 1:SCM OIR Event happened.	SCM_OIR_REC
[0]	RO	1b1	SCM Present 0:present 1:not present	SCM_PRESENT

Register 0x09: PEER_FAB_CON_PRESENT – Peer FAB Connector Present Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved	Reserved
[3]	RO	1b0	Peer FAB Connector4 Present 0:present 1:not present	PEER_FAB_CON4_PRESENT

[2]	RO	1b0	Peer FAB Connector3 Present 0:present 1:not present	PEER_FAB_CON3_PRESENT
[1]	RO	1b0	Peer FAB Connector2 Present 0:present 1:not present	PEER_FAB_CON2_PRESENT
[0]	RO	1b0	Peer FAB Connector1 Present 0:present 1:not present	PEER_FAB_CON1_PRESENT

Register 0x0A: HOT_SWAP_PG_STA – Hot Swap Power Good Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RO	0x7F	Reserved	Reserved
[0]	RO	1b0	The Status of HOTSWAP_PG_INV	HOTSWAP_PG_INV_STA

Register 0x0B: LM57_TOVER_STA – LM57 TOVER Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RO	0x7F	Reserved	Reserved
[0]	RO	1b0	The Status of LM57_TOVER	LM57_TOVER _STA

Register 0x10: SYS_PWR_CTRL – System Power Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:5]	RW	0x7	Reserved.	Reserved
[4]	RW	0b1	PWR_MAIN_FORCE Control	PWR_MAIN_FORCE
[3:2]	RW	0x3	Reserved.	Reserved
[1]	RW	0b1	PWR_MAIN_EN 0: Main power is OFF 1: Main Power is enabled	PWR_MAIN_EN
[0]	RW	0b1	PWR_CYC_ALL_N 0: Write 0 to this bit will trigger PWR1014A to start power cycling of all power rail 1: normal	PWR_CYC_ALL_N

Register 0x11: SYS_RST_CTRL – System Reset Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RW	0xF	Reserved	Reserved
[3]	RW	0b1	PWR_RST_REQ_N 0: write 0 to trigger power reset 1: normal	PWR_RST_REQ
[2]	RW	0b1	COLD_RST_REQ_N 0: write 0 to trigger cold reset 1: normal	COLD_RST_REQ
[1]	RW	0b1	WARM_RST_REQ_N 0: write 0 to trigger warm reset 1: normal	WARM_RST_REQ
[0]	RW	0b1	HOT_RST_REQ_N 0: write 0 to trigger hot reset 1: normal	HOT_RST_REQ

Register 0x12: TH_RST_CTRL – BCM56960 Reset Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RW	0xF	Reserved.	Reserved
[3]	RW	0b0	TH_PCIE_RST_N Mask 0: normal 1: Mask the CB_RESET_N from SCM card to TH_PCIE_RST_N	TH_PCIE_RST_MASK
[2]	RW	0b0	TH_SYS_RST_N Mask 0: normal 1: Mask the CB_RESET_N from SCM card to TH_SYS_RST_N	TH_SYS_RST_N_MASK
[1]	RW	0b1	TH_PCIE_RST_N 0: write 0 to trigger tomahawk PCIe reset 1: normal	TH_PCIE_RST_N
[0]	RW	0b1	TH_SYS_RST_N 0: write 0 to trigger tomahawk system reset 1: normal	TH_SYS_RST_N

Register 0x14: SEP_RST_CTRL – Separate Reset Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RW	0b1	Reserved.	Reserved
[6]	RW	0b1	LPC Interface Reset 0: reset 1: normal	LPC_INTF_RST
[5]	RW	0b1	SCM CPLD I2C Slave Reset 0: reset 1: normal	SCM_CPLD_I2C_SLAVE_RST
[4]	RW	0b1	BCM54616S_RST_N 0: reset 1: normal	BCM54616S_RST
[3]	RW	0b1	SWITCHPHY_RST_N 0: reset 1: normal	SWITCHPHY_RST
[2]	RW	0b1	BCM5389_RST_N 0: reset 1: normal	BCM5389_RST
[1]	RW	0b1	USB_HUB_RST_N 0: reset 1: normal	USB_HUB_RST
[0]	RW	0b1	CP2112_RST_N 0: reset 1: normal	CP2112_RST

Register 0x15: TH_RST_REC – TH Reset Reocrd Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:0]	RW	0x0	0x0: Normal status. 0x11: Hardware shutdown recorded.	HW_SHUTDN_REC

Register 0x16: TH_RST_REC – TH Reset Reocrd Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:0]	RW	0x0	0x0: Write Clear status. 0x11: Power on reset TH.	TH_RST_REC

			0x22: COMe CB_RESET_N reset TH. 0x33: Register control reset TH.	

Register 0x20: BMC_RST_EN – BMC Reset Enable Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	0b1	Reserved.	Reserved
[6]	RW	0b0	BMC_WDT2_EN	BMC_WDT2_EN
[5]	RW	0b0	BMC_WDT1_EN	BMC_WDT1_EN
[4]	RW	0b0	BMC_RESET4_EN 0: BMC reset 4 request is disabled 1: BMC reset 4 request is enabled	BMC_RST4_EN
[3]	RW	0b0	BMC_RESET3_EN 0: BMC reset 3 request is disabled 1: BMC reset 3 request is enabled	BMC_RST3_EN
[2]	RW	0b0	BMC_RESET2_EN 0: BMC reset 2 request is disabled 1: BMC reset 2 request is enabled	BMC_RST2_EN
[1]	RW	0b0	BMC_RESET1_EN 0: BMC reset 1 request is disabled 1: BMC reset 1 request is enabled	BMC_RST1_EN
[0]	RW	0b0	BMC_MAIN_RESET_N 0: BMC main reset request is disabled 1: BMC main reset request is enabled	BMC_MAIN_RST_EN

Register 0x21: BMC_RST_CTRL – BMC Reset Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RW	0x7F	Reserved.	Reserved
[0]	RW	0x1	CPLD_BMC_RST_N Control 0: write 0 to trigger BMC reset 1: normal	BMC_RST

Register 0x22: BMC_RST_TYPE – BMC Reset Type Register

Bit #	R/W	Default Value	Description	Name
[7:0]	RW	0x11	After power on this register default values set to 0x11. When BMC run, need this register to other values.	BMC_RST_TYPE

Register 0x30: UART_MUX_CTRL – UART MUX Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:3]	RO	0x0	Reserved.	Reserved
[2]	RO	0b0	0:Use BMC UART1 for sol function 1:Use BMC UART4 for sol function	SOL_UART_SEL
[1:0]	RO	2b00	TH_UART selection 00: Tomahawk UART-0 connected with BMC UART2 01: Tomahawk UART-2 connected with BMC UART2 10: Tomahawk UART-3 connected with BMC UART2 11: reserved	UART_MUX_CTRL

Register 0x40: ROV_STA – ROV Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved.	Reserved
[3:0]	RO	4b1000	TH_ROV[3:0] ROV[3:0] Voltage 4'b0000 1.2000 4'b0001 1.1750 4'b0010 1.1500 4'b0011 1.1250 4'b0100 1.1000 4'b0101 1.0750 4'b0110 1.0500 4'b0111 1.0250 4'b1000 1.0000 4'b1001 0.9750 4'b1010 0.9500 4'b1011 0.9250 4'b1100 0.9000	ROV_STA

			4'b1101 0.8750 4'b1110 0.8500 4'b1111 0.8250	

Register 0x41: BD_PWR_STA – On Board Power Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0xF	Reserved.	Reserved
[3]	RO	1b1	IR3584_1.0V_VRHOT 0: over temperature is negative 1: over temperature is active	IR3584_1.0V_VRHOT
[2]	RO	1b1	IR3584_1.0V_VRRDY1 0: power not OK 1: Power is OK	IR3584_1V_VRRDY1
[1]	RO	1b1	IR3581_VRHOT 0: over temperature is negative 1: over temperature is active	IR3581_VRHOT
[0]	RO	1b1	IR3581_VRRDY1 0: power not OK 1: Power is OK	IR3581_VRRDY1

Register 0x50: CP2112_IN – CP2112 Bridge GPIO Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	1b1	CP2112_GPIO_IN[7]	CP2112_IN7
[6]	RO	1b1	CP2112_GPIO_IN[6]	CP2112_IN6
[5]	RO	1b1	CP2112_GPIO_IN[5]	CP2112_IN5
[4]	RO	1b1	CP2112_GPIO_IN[4]	CP2112_IN4
[3]	RO	1b1	CP2112_GPIO_IN[3]	CP2112_IN3
[2]	RO	1b1	CP2112_GPIO_IN[2]	CP2112_IN2
[1]	RO	1b1	CP2112_GPIO_IN[1]	CP2112_IN1
[0]	RO	1b1	CP2112_GPIO_IN[0]	CP2112_IN0

Register 0x51: CP2112_OE – CP2112 Bridge GPIO OE Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RW	1b1	CP2112_GPIO_OE[7]	CP2112_OE7

[6]	RW	1b1	CP2112_GPIO_OE[6]	CP2112_OE6
[5]	RW	1b1	CP2112_GPIO_OE[5]	CP2112_OE5
[4]	RW	1b1	CP2112_GPIO_OE[4]	CP2112_OE4
[3]	RW	1b1	CP2112_GPIO_OE[3]	CP2112_OE3
[2]	RW	1b1	CP2112_GPIO_OE[2]	CP2112_OE2
[1]	RW	1b1	CP2112_GPIO_OE[1]	CP2112_OE1
[0]	RW	1b1	CP2112_GPIO_OE[0]	CP2112_OE0

Register 0x52: CP2112_OUT – CP2112 Bridge GPIO Output Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RW	1b1	CP2112_GPIO_OUT[7]	CP2112_OUT7
[6]	RW	1b1	CP2112_GPIO_OUT[6]	CP2112_OUT6
[5]	RW	1b1	CP2112_GPIO_OUT[5]	CP2112_OUT5
[4]	RW	1b1	CP2112_GPIO_OUT[4]	CP2112_OUT4
[3]	RW	1b1	CP2112_GPIO_OUT[3]	CP2112_OUT3
[2]	RW	1b1	CP2112_GPIO_OUT[2]	CP2112_OUT2
[1]	RW	1b1	CP2112_GPIO_OUT[1]	CP2112_OUT1
[0]	RW	1b1	CP2112_GPIO_OUT[0]	CP2112_OUT0

Register 0x60: CMM_MS_STA – CMM M/S Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0xF	Reserved	Reservd
[3]	RO	0b0	CMM2 M/S status 1:CMM2 is Slave 0:CMM2 is Master	CMM2_STA
[2]	RO	0b0	CMM1 M/S status 1:CMM1 is Slave 0:CMM1 is Master	CMM1_STA
[1:0]	RO	0x3	Reserved	Reservd

Register 0x78: QSFP_CPLD_SEP_RST_CTRL – QSPF CPLD Separate Reset Control				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:5]	RW	0xF	Reserved.	Reserved
[4]	RW	0b0	ISO_QSFP_CPLD_RST_N Mask	QSFP_CPLD_RST_MASK

			0: normal 1: Mask the CB_RESET_N from SCM card to ISO_QSFP_CPLD_RST_N	
[3]	RW	0b1	ISO_PCA9548_QSFP_2_RST_N 0: reset 1: normal	PCA9548_RST2
[2]	RW	0b1	ISO_PCA9548_QSFP_1_RST_N 0: reset 1: normal	PCA9548_RST1
[1]	RW	0b1	ISO_PCA9541_I2C_RESET 0: reset 1: normal	PCA9541_RST
[0]	RW	0b1	ISO_QSFP_CPLD_RST_N 0: reset 1: normal	QSFP_CPLD_RST

Register 0x79: QSFP_CPLD_INT_STA – QSFP CPLD Interrupt Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:2]	RO	0x3F	Reserved.	Reserved
[1]	RO	0b1	Status of ISO_CPLD_QSFP_INT_N	ISO_CPLD_QSFP_INT_N
[0]	RO	0b1	Status of ISO_CPLD_QSFP_MOD_ABS	ISO_CPLD_QSFP_MOD_ABS

Register 0x80: SYS_DEBUG_CTRL – System Debug Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	1b1	Reserved.	Reserved
[6]	RO	1b1	ISO_FORCE_MODE 0: BMC control 1: CPLD forced mode	ISO_FORCE_MODE
[5]	RO	1b1	BMC_ISO_BUF_EN Data to enable or disable isolation buffer for BMC 0: disabled 1: buffer enabled	BMC_ISO_BUF_EN
[4]	RO	1b1	ISO_BUF_EN	ISO_BUF_EN

			Data to enable or disable isolation buffer for BCM56960. 0: disable 1: buffer enabled	
[3]	RO	1b1	Reserved.	Reserved
[2]	RO	1b1	Force_2nd_Write 0: normal mode 1: always writable, debug mode	Force_2nd_Write
[1]	RO	1b1	EN_2nd_Flash_WP 0: writable 1: write protected	EN_2nd_Flash_WP
[0]	RO	1b1	DUAL_BOOT_EN 0: single boot 1: dual boot	DUAL_BOOT_EN

Register 0x90: I2C_RATE_CTRL – I2C Rate Control Register			
Bit #	**R/W**	**Default Value**	**Description**
[7]	RO	0b0	Reserved.
[6]	R/W	0b1	Baud rate setting. 0:50KHz, 1:100KHz
[5:0]	RO	0x0	Reserved.

Register 0x91: I2C_OP_CODE – I2C Operation Code Register			
Bit #	**R/W**	**Default Value**	**Description**
[7:4]	R/W	0x0	The I2C operation data byte length. Indicates 1~8byte.
[3:2]	RO	0x0	Reserved.
[1:0]	R/W	0x0	The I2C operation command byte length. Indicates 0~3 byte. When the length is 0, it means this I2C operation is a “Current Adress Read”.

Register 0x92: I2C_SLV_ADDR – I2C Slave Address Register			
Bit #	**R/W**	**Default Value**	**Description**
[7:1]	R/W	0x0	The I2C slave device address.
[0]	R/W	0b0	Read/Write indicator. 1: Read operation. 0: Write operation.

Register 0x93: I2C_CMD_BYTE0 – I2C Command Byte0 Register			
Bit #	**R/W**	**Default Value**	**Description**
[7:0]	R/W	0x0	The I2C slave's command (memory address) byte 0.

Register 0x94: I2C_CMD_BYTE1 – I2C Command Byte1 Register			
Bit #	**R/W**	**Default Value**	**Description**
[7:0]	R/W	0x0	The I2C slave's command (memory address) byte 1.

Register 0x95: I2C_CMD_BYTE2 – I2C Command Byte2 Register			
Bit #	**R/W**	**Default Value**	**Description**
[7:0]	R/W	0x0	The I2C slave's command (memory address) byte 2.

Register 0x96: I2C_STA_RST – I2C Status & Soft Reset Register			
Bit #	**R/W**	**Default Value**	**Description**
[7]	RO	0b0	I2C Master error. If the Master encounters timeout or incomplete frame, this bit will be '1'. It can only be cleared by soft reset to I2C Master.
[6]	RO	0b0	I2C busy indicator. The CPU can only start an operation when it's '0'. During a read operation, only after it is back to '0', the read data is ready.
[5]	RO	0b1	SDA Pin Status.
[4]	RO	0b1	SCL Pin Status
[3]	R/W	0b1	Control SDA Pin Status.
[2]	R/W	0b1	Control SCL Pin Status.
[1]	R/W	0b0	0:I2C Signal control by LPC-I2C Master Logic 1:I2C Signal control by register bit[2] & bit[3].
[0]	R/W	0b1	I2C Master software reset. 0: Soft reset I2C Master. This bit needs to be manually written to '1' to normal state by Soft.

Register 0xA0, 0xA1… – 0xA8: I2C_WR_DATA0/7 – I2C Write Data Byte 0 - 7 Register

Bit #	R/W	Default Value	Description
[7:0]	R/W	0x0	The data byte during I2C writing.

Register 0xB0, 0xB1… – 0xB8: I2C_RD_DATA0/7 – I2C Read Data Byte 0 - 7 Register			
Bit #	**R/W**	**Default Value**	**Description**
[7:0]	RO	0x0	The data byte got from I2C slave during I2C read.

5.1.8. LC QSFP CPLD Register Map

Both COM-e CPU and BMC can access QSFP CPLD. BMC can access QSFP CPLD registers through I2C bus 13 of BMC, the I2C address of SYSCPLD is 0x39. COM-e CPU can access the QSFP CPLD registers via LPC bus. In Logic support COM-e CPU & BMC read the register at same time. When write the register at same time the CPU will have higher priority.

Register 0x01: CPLD_VERSION – CPLD Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	0	Reserved	Reserved
[6]	RO	0	Released Bit 0= not released, 1= Released version after PVT	RELEASE_STA
[5:0]	RO	Designed	CPLD Revision[5:0]	CPLD_VER

Register 0x02: CPLD_SUB_VERSION – CPLD Sub Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:0]	RO	0x01	CPLD sub-version, HW debug only	CPLD_SUB_VER

Register 0x09: PORT_LED_OPMOD – Port LED Operating Mode Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RO	0x0	Reserved.	Reserved
[0]	R/W	0b0	Port LED Operating Mode. 0: Normal Mode, port LED are decoded from BCM56960 serial LED signals. 1: Test Mode, port LED are controlled by Port LED Test Registers.	OP_MOD

Register 0x0A: PORT_LED_TEST – Port LED Test Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:3]	RO	0b0	Reserved.	Reserved
[2]	R/W	0b1	Ports LED Blue Control. obo: All Ports LED Blue On	BLU_LED_CTRL

			ob1: All Ports LED Blue Off.	
[1]	R/W	0b1	Ports LED GreenControl. obo: All Ports LED Green On ob1: All Ports LED Green Off.	GRN_LED_CTRL
[0]	R/W	0b1	Ports LED GreenControl. obo: All Ports LED Red On ob1: All Ports LED Red Off.	RED_LED_CTRL

Note: This register is valid only when Port LED Operating Mode Register bit[0] = 0b1.

Register 0x10:QSFP_RESET_CTRL0 – QSFP Reset Control Registero				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RW	ob1	This bit control QSFP8 RESET status 0: Reset 1: not Reset	QSFP8_RST
[6]	RW	ob1	This bit control QSFP7 RESET status 0: Reset 1: not Reset	QSFP7_RST
[5]	RW	ob1	This bit control QSFP6 RESET status 0: Reset 1: not Reset	QSFP6_RST
[4]	RW	ob1	This bit control QSFP5 RESET status 0: Reset 1: not Reset	QSFP5_RST
[3]	RW	ob1	This bit control QSFP4 RESET status 0: Reset 1: not Reset	QSFP4_RST
[2]	RW	ob1	This bit control QSFP3 RESET status 0: Reset 1: not Reset	QSFP3_RST
[1]	RW	ob1	This bit control QSFP2 RESET status 0: Reset 1: not Reset	QSFP2_RST
[0]	RW	ob1	This bit control QSFP1 RESET status 0: Reset 1: not Reset	QSFP1_RST

Register 0x11:QSFP_RESET_CTRL1 – QSFP Reset Control Register1				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RW	ob1	This bit control QSFP16 RESET status 0: Reset 1: not Reset	QSFP16_RST
[6]	RW	ob1	This bit control QSFP15 RESET status 0: Reset 1: not Reset	QSFP15_RST
[5]	RW	ob1	This bit control QSFP14 RESET status 0: Reset 1: not Reset	QSFP14_RST
[4]	RW	ob1	This bit control QSFP13 RESET status 0: Reset 1: not Reset	QSFP13_RST

[3]	RW	0b1	This bit control QSFP12 RESET status 0: Reset 1: not Reset	QSFP12_RST
[2]	RW	0b1	This bit control QSFP11 RESET status 0: Reset 1: not Reset	QSFP11_RST
[1]	RW	0b1	This bit control QSFP10 RESET status 0: Reset 1: not Reset	QSFP10_RST
[0]	RW	0b1	This bit control QSFP9 RESET status 0: Reset 1: not Reset	QSFP9_RST

Register 0x12:QSFP_LPMOD_CTRL0 – QSFP LPMOD Control Register0				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RW	0b1	This bit control QSFP8 LPMOD 0:High power mode 1:Low power mode	QSFP8_LPMOD
[6]	RW	0b1	This bit control QSFP7 LPMOD 0:High power mode 1:Low power mode	QSFP7_LPMOD
[5]	RW	0b1	This bit control QSFP6 LPMOD 0:High power mode 1:Low power mode	QSFP6_LPMOD
[4]	RW	0b1	This bit control QSFP5 LPMOD 0:High power mode 1:Low power mode	QSFP5_LPMOD
[3]	RW	0b1	This bit control QSFP4 LPMOD 0:High power mode 1:Low power mode	QSFP4_LPMOD
[2]	RW	0b1	This bit control QSFP3 LPMOD 0:High power mode 1:Low power mode	QSFP3_LPMOD
[1]	RW	0b1	This bit control QSFP2 LPMOD 0:High power mode 1:Low power mode	QSFP2_LPMOD
[0]	RW	0b1	This bit control QSFP1 LPMOD 0:High power mode 1:Low power mode	QSFP1_LPMOD

Register 0x13:QSFP_LPMOD_CTRL1 – QSFP LPMOD Control Register1

Bit #	R/W	Default Value	Description	Name
[7]	RW	0b1	This bit control QSFP16 LPMOD 0:High power mode 1:Low power mode	QSFP16_LPMOD
[6]	RW	0b1	This bit control QSFP15 LPMOD 0:High power mode 1:Low power mode	QSFP15_LPMOD
[5]	RW	0b1	This bit control QSFP14 LPMOD 0:High power mode 1:Low power mode	QSFP14_LPMOD
[4]	RW	0b1	This bit control QSFP13 LPMOD 0:High power mode 1:Low power mode	QSFP13_LPMOD
[3]	RW	0b1	This bit control QSFP12 LPMOD 0:High power mode 1:Low power mode	QSFP12_LPMOD
[2]	RW	0b1	This bit control QSFP11 LPMOD 0:High power mode 1:Low power mode	QSFP11_LPMOD
[1]	RW	0b1	This bit control QSFP10 LPMOD 0:High power mode 1:Low power mode	QSFP10_LPMOD
[0]	RW	0b1	This bit control QSFP9 LPMOD 0:High power mode 1:Low power mode	QSFP9_LPMOD

Register 0x14:QSFP_INT_STA0 – QSFP INT Status Register0				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	None	Status of QSFP8 INT_N 0: Intrrupt 1:not Intrrupt	QSFP8_INT
[6]	RO	None	Status of QSFP7 INT_N 0: Intrrupt 1:not Intrrupt	QSFP7_INT
[5]	RO	None	Status of QSFP6 INT_N 0: Intrrupt 1:not Intrrupt	QSFP6_INT
[4]	RO	None	Status of QSFP5 INT_N 0: Intrrupt 1:not Intrrupt	QSFP5_INT
[3]	RO	None	Status of QSFP4 INT_N 0: Intrrupt 1:not Intrrupt	QSFP4_INT
[2]	RO	None	Status of QSFP3 INT_N 0: Intrrupt 1:not Intrrupt	QSFP3_INT
[1]	RO	None	Status of QSFP2 INT_N 0: Intrrupt 1:not Intrrupt	QSFP2_INT
[0]	RO	None	Status of QSFP1 INT_N 0: Intrrupt 1:not Intrrupt	QSFP1_INT

Register 0x15:QSFP_INT_STA1 – QSFP INT Status Register 1				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	None	Status of QSFP16 INT_N 0: Intrrupt 1:not Intrrupt	QSFP16_INT
[6]	RO	None	Status of QSFP15 INT_N 0: Intrrupt 1:not Intrrupt	QSFP15_INT
[5]	RO	None	Status of QSFP14 INT_N 0: Intrrupt 1:not Intrrupt	QSFP14_INT
[4]	RO	None	Status of QSFP13 INT_N 0: Intrrupt 1:not Intrrupt	QSFP13_INT
[3]	RO	None	Status of QSFP12 INT_N 0: Intrrupt 1:not Intrrupt	QSFP12_INT
[2]	RO	None	Status of QSFP11 INT_N 0: Intrrupt 1:not Intrrupt	QSFP11_INT
[1]	RO	None	Status of QSFP10 INT_N 0: Intrrupt 1:not Intrrupt	QSFP10_INT
[0]	RO	None	Status of QSFP9 INT_N 0: Intrrupt 1:not Intrrupt	QSFP9_INT

Register 0x16:QSFP_ABS_STA0 – QSFP ABS Status Register0				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	None	Status of QSFP8 ABS 0: Present 1:not Present	QSFP8_ABS
[6]	RO	None	Status of QSFP7 ABS 0: Present 1:not Present	QSFP7_ABS
[5]	RO	None	Status of QSFP6 ABS 0: Present 1:not Present	QSFP6_ABS
[4]	RO	None	Status of QSFP5 ABS 0: Present 1:not Present	QSFP5_ABS
[3]	RO	None	Status of QSFP4 ABS 0: Present 1:not Present	QSFP4_ABS
[2]	RO	None	Status of QSFP3 ABS 0: Present 1:not Present	QSFP3_ABS
[1]	RO	None	Status of QSFP2 ABS 0: Present 1:not Present	QSFP2_ABS
[0]	RO	None	Status of QSFP1 ABS 0: Present 1:not Present	QSFP1_ABS

Register 0x17:QSFP_ABS_STA1 – QSFP ABS Status Register 1				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	None	Status of QSFP16 ABS 0: Present 1:not Present	QSFP16_ABS
[6]	RO	None	Status of QSFP15 ABS 0: Presentz 1:not Present	QSFP15_ABS
[5]	RO	None	Status of QSFP14 ABS 0: Present 1:not Present	QSFP14_ABS
[4]	RO	None	Status of QSFP13 ABS 0: Present 1:not Present	QSFP13_ABS
[3]	RO	None	Status of QSFP12 ABS 0: Present 1:not Present	QSFP12_ABS
[2]	RO	None	Status of QSFP11 ABS 0: Present 1:not Present	QSFP11_ABS
[1]	RO	None	Status of QSFP10 ABS 0: Present 1:not Present	QSFP10_ABS
[0]	RO	None	Status of QSFP9 ABS 0: Present 1:not Present	QSFP9_ABS

Register 0x20: QSFP_COMBINE – QSFP Interrupt Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:2]	RO	0x3F	Reserved	Reserved
[1]	RO	0b1	The combined interrupt status of QSFP1-16_ABS to CPU 0: INT 1:not INT	QSFP_PRS_COMBINE
[0]	RO	0b1	The combined interrupt status of QSFP1-16_INT to CPU 0: INT 1:not INT	QSFP_INT_COMBINE

Register 0x21: QSFP_TRIG_MOD – QSFP Trig Mode Configure Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved.	Reserved
[3:2]	RW	0x2	00: Interrupt source from QSFP1-16_ABS_N trigger by falling edge 01: Interrupt source from QSFP1-16_ABS_N trigger by rising edge	QSFP_PRS_TRIG

			10: Interrupt source from QSFP1-16_ABS_N trigger by both falling edge and rising edge 11: Interrupt source from QSFP1-16_ABS_N low trigger by level	
[1:0]	RW	0x0	00: Interrupt source from QSFP1-16_INT_N trigger by falling edge 01: Interrupt source from QSFP1-16_ INT _N trigger by rising edge 10: Interrupt source from QSFP1-16_ INT _N trigger by both falling edge and rising edge 11: Interrupt source from QSFP1-16_ INT _N low trigger by level	QSFP_INT_TRIG

Register 0x22: QSFP_INT_MASK0 – QSFP INT Interrupt Mask Registero				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RW	0b1	Interrupt mask of QSFP8_INT 0:not mask 1:mask	QSFP8_INT _MASK
[6]	RW	0b1	Interrupt mask of QSFP7_INT 0:not mask 1:mask	QSFP7_INT _MASK
[5]	RW	0b1	Interrupt mask of QSFP6_INT 0:not mask 1:mask	QSFP6_INT _MASK
[4]	RW	0b1	Interrupt mask of QSFP5_INT 0:not mask 1:mask	QSFP5_INT _MASK
[3]	RW	0b1	Interrupt mask of QSFP4_INT 0:not mask 1:mask	QSFP4_INT _MASK
[2]	RW	0b1	Interrupt mask of QSFP3_INT 0:not mask 1:mask	QSFP3_INT _MASK
[1]	RW	0b1	Interrupt mask of QSFP2_INT 0:not mask 1:mask	QSFP2_INT _MASK
[0]	RW	0b1	Interrupt mask of QSFP1_INT 0:not mask 1:mask	QSFP1_INT _MASK

Register 0x23: QSFP_INT_MASK1 – QSFP INT Interrupt Mask Register1				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RW	0b1	Interrupt mask of QSFP16_INT 0:not mask 1:mask	QSFP16_INT _MASK
[6]	RW	0b1	Interrupt mask of QSFP15_INT 0:not mask 1:mask	QSFP15_INT _MASK
[5]	RW	0b1	Interrupt mask of QSFP14_INT 0:not mask 1:mask	QSFP14_INT _MASK
[4]	RW	0b1	Interrupt mask of QSFP13_INT 0:not mask 1:mask	QSFP13_INT _MASK
[3]	RW	0b1	Interrupt mask of QSFP12_INT 0:not mask 1:mask	QSFP12_INT _MASK
[2]	RW	0b1	Interrupt mask of QSFP11_INT 0:not mask 1:mask	QSFP11_INT _MASK
[1]	RW	0b1	Interrupt mask of QSFP10_INT 0:not mask 1:mask	QSFP10_INT _MASK
[0]	RW	0b1	Interrupt mask of QSFP9_INT 0:not mask 1:mask	QSFP9_INT _MASK

Register 0x24: QSFP_INT_INT0 – QSFP INT Interrupt Register0				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RC	0b0	QSFP8_INT status change interrupt 0:not INT 1:INT	QSFP8_INT _INT
[6]	RC	0b0	QSFP7_INT status change interrupt 0:not INT 1:INT	QSFP7_INT _INT
[5]	RC	0b0	QSFP6_INT status change interrupt 0:not INT 1:INT	QSFP6_INT _INT
[4]	RC	0b0	QSFP5_INT status change interrupt 0:not INT 1:INT	QSFP5_INT _INT
[3]	RC	0b0	QSFP4_INT status change interrupt 0:not INT 1:INT	QSFP4_INT _INT
[2]	RC	0b0	QSFP3_INT status change interrupt 0:not INT 1:INT	QSFP3_INT _INT
[1]	RC	0b0	QSFP2_INT status change interrupt 0:not INT 1:INT	QSFP2_INT _INT
[0]	RC	0b0	QSFP1_INT status change interrupt 0:not INT 1:INT	QSFP1_INT _INT

Register 0x25: QSFP_INT_INT1 – QSFP INT Interrupt Register1				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RC	0b0	QSFP16_INT status change interrupt 0:not INT 1:INT	QSFP16_INT _INT
[6]	RC	0b0	QSFP15_INT status change interrupt 0:not INT 1:INT	QSFP15_INT _INT
[5]	RC	0b0	QSFP14_INT status change interrupt 0:not INT 1:INT	QSFP14_INT _INT
[4]	RC	0b0	QSFP13_INT status change interrupt 0:not INT 1:INT	QSFP13_INT _INT
[3]	RC	0b0	QSFP12_INT status change interrupt 0:not INT 1:INT	QSFP12_INT _INT
[2]	RC	0b0	QSFP11_INT status change interrupt 0:not INT 1:INT	QSFP11_INT _INT
[1]	RC	0b0	QSFP10_INT status change interrupt 0:not INT 1:INT	QSFP10_INT _INT
[0]	RC	0b0	QSFP9_INT status change interrupt 0:not INT 1:INT	QSFP9_INT _INT

Register 0x26: QSFP_ABS_MASK0 – QSFP ABS Interrupt Mask Register0				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RW	0b1	Interrupt mask of QSFP8_ABS 0:not mask 1:mask	QSFP8_ABS _MASK
[6]	RW	0b1	Interrupt mask of QSFP7_ABS 0:not mask 1:mask	QSFP7_ABS _MASK
[5]	RW	0b1	Interrupt mask of QSFP6_ABS 0:not mask 1:mask	QSFP6_ABS _MASK
[4]	RW	0b1	Interrupt mask of QSFP5_ABS 0:not mask 1:mask	QSFP5_ABS _MASK
[3]	RW	0b1	Interrupt mask of QSFP4_ABS 0:not mask 1:mask	QSFP4_ABS _MASK
[2]	RW	0b1	Interrupt mask of QSFP3_ABS 0:not mask 1:mask	QSFP3_ABS _MASK
[1]	RW	0b1	Interrupt mask of QSFP2_ABS 0:not mask 1:mask	QSFP2_ABS _MASK

[0]	RW	0b1	Interrupt mask of QSFP1_ABS 0:not mask 1:mask	QSFP1_ABS _MASK

Register 0x27: QSFP_ABS_MASK1 – QSFP ABS Interrupt Mask Register1				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RW	0b1	Interrupt mask of QSFP16_ABS 0:not mask 1:mask	QSFP16_ABS _MASK
[6]	RW	0b1	Interrupt mask of QSFP15_ABS 0:not mask 1:mask	QSFP15_ABS _MASK
[5]	RW	0b1	Interrupt mask of QSFP14_ABS 0:not mask 1:mask	QSFP14_ABS _MASK
[4]	RW	0b1	Interrupt mask of QSFP13_ABS 0:not mask 1:mask	QSFP13_ABS _MASK
[3]	RW	0b1	Interrupt mask of QSFP12_ABS 0:not mask 1:mask	QSFP12_ABS _MASK
[2]	RW	0b1	Interrupt mask of QSFP11_ABS 0:not mask 1:mask	QSFP11_ABS _MASK
[1]	RW	0b1	Interrupt mask of QSFP10_ABS 0:not mask 1:mask	QSFP10_ABS _MASK
[0]	RW	0b1	Interrupt mask of QSFP9_ABS 0:not mask 1:mask	QSFP9_ABS _MASK

Register 0x28: QSFP_ABS_INT0 – QSFP ABS Interrupt Register0				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RC	0b0	QSFP8_ABS status change interrupt 0:not INT 1:INT	QSFP8_ ABS _INT
[6]	RC	0b0	QSFP7_ABS status change interrupt 0:not INT 1:INT	QSFP7_ ABS _INT
[5]	RC	0b0	QSFP6_ABS status change interrupt 0:not INT 1:INT	QSFP6_ ABS _INT
[4]	RC	0b0	QSFP5_ABS status change interrupt 0:not INT 1:INT	QSFP5_ ABS _INT
[3]	RC	0b0	QSFP4_ABS status change interrupt 0:not INT 1:INT	QSFP4_ ABS _INT
[2]	RC	0b0	QSFP3_ABS status change interrupt 0:not INT 1:INT	QSFP3_ ABS _INT
[1]	RC	0b0	QSFP2_ABS status change interrupt 0:not INT 1:INT	QSFP2_ ABS _INT

[0]	RC	0b0	QSFP1_ABS status change interrupt 0:not INT 1:INT	QSFP1_ ABS _INT

Register 0x29: QSFP_ABS_INT1 – QSFP ABS Interrupt Register1				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RC	0b0	QSFP16_ABS status change interrupt 0:not INT 1:INT	QSFP16_ ABS _INT
[6]	RC	0b0	QSFP15_ABS status change interrupt 0:not INT 1:INT	QSFP15_ ABS _INT
[5]	RC	0b0	QSFP14_ABS status change interrupt 0:not INT 1:INT	QSFP14_ ABS _INT
[4]	RC	0b0	QSFP13_ABS status change interrupt 0:not INT 1:INT	QSFP13_ ABS _INT
[3]	RC	0b0	QSFP12_ABS status change interrupt 0:not INT 1:INT	QSFP12_ ABS _INT
[2]	RC	0b0	QSFP11_ABS status change interurpt 0:not INT 1:INT	QSFP11_ ABS _INT
[1]	RC	0b0	QSFP10_ABS status change interrupt 0:not INT 1:INT	QSFP10_ ABS _INT
[0]	RC	0b0	QSFP9_ABS status change interrupt 0: not INT 1:INT	QSFP9_ ABS _INT

5.2. Fabric Module

The Fabric card (FAB) provide fabric connectivity to all line cards inside Backpack. There are four Fabric Cards altogether in the system.

5.2.1. Block Diagram of Fabric Card

Each fabric card consists of the following components:

- One tomahawk Switch ASIC, each Switch ASIC is part of one Switch Element (SWE).
- Four Orthogonal highspeed connectors, each OD connector connect to one LC
- BMC AST1250 is used for Board Management.
- A eight port SGMII GBE Switch BCM5389 is used for OOB switch to connect to CMM1, CMM2, BMC, SCM-COM-E and Tomahawk Management port (configured as SGMII)
- Fan control Board (FCB) is mezzanine card of FAB
- Control signals connect to HCP, then connect to SCM or CMM
- Power is provided by HPD, part of BBA
- Multiple temperature sensors can be accessed by CMM

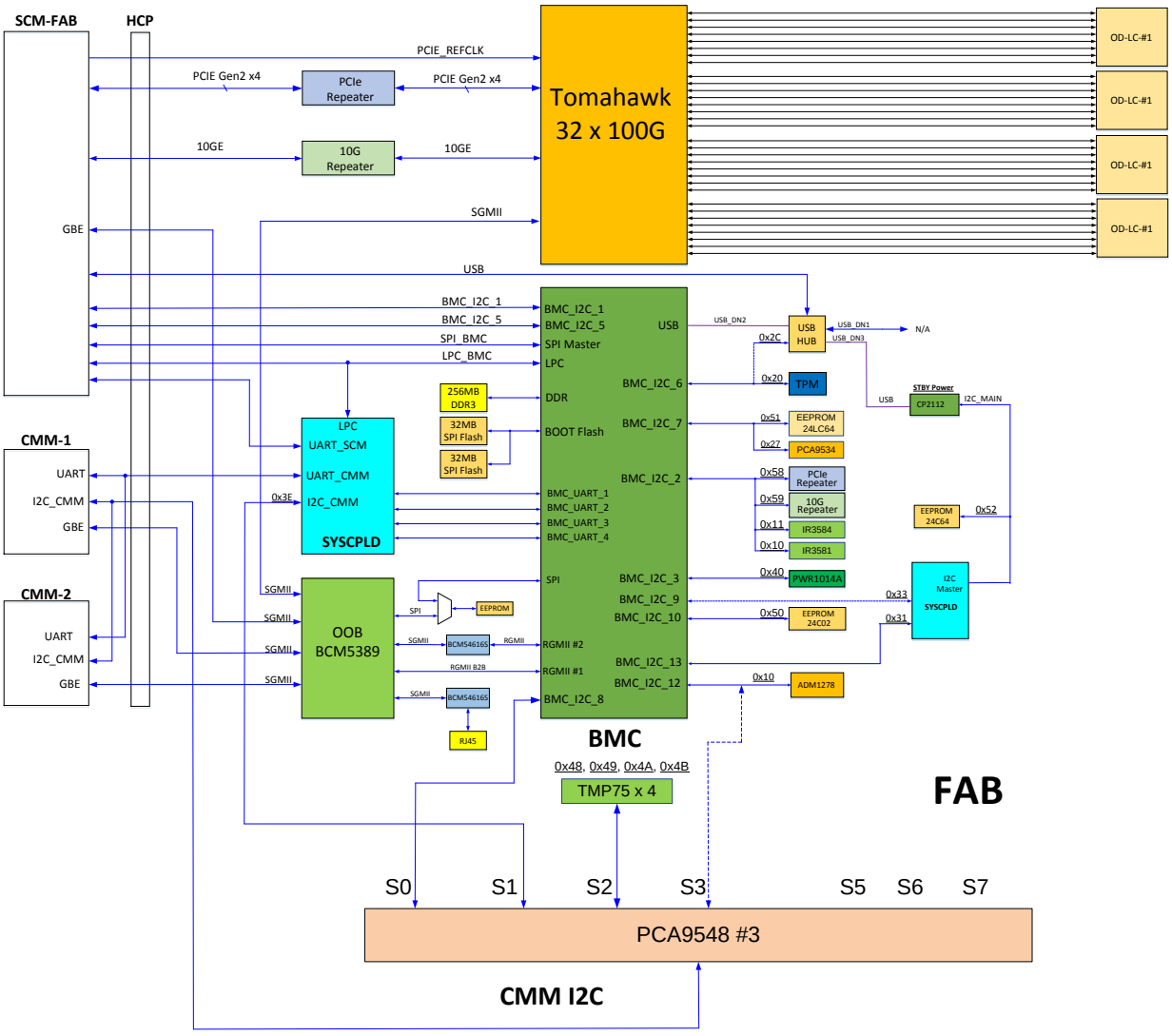

Figure 13: Fabric Module diagram

5.2.2. Fabric Card Port Mapping

FAB has four OD connector connecting to four LC, the following diagram show the OD numbering:

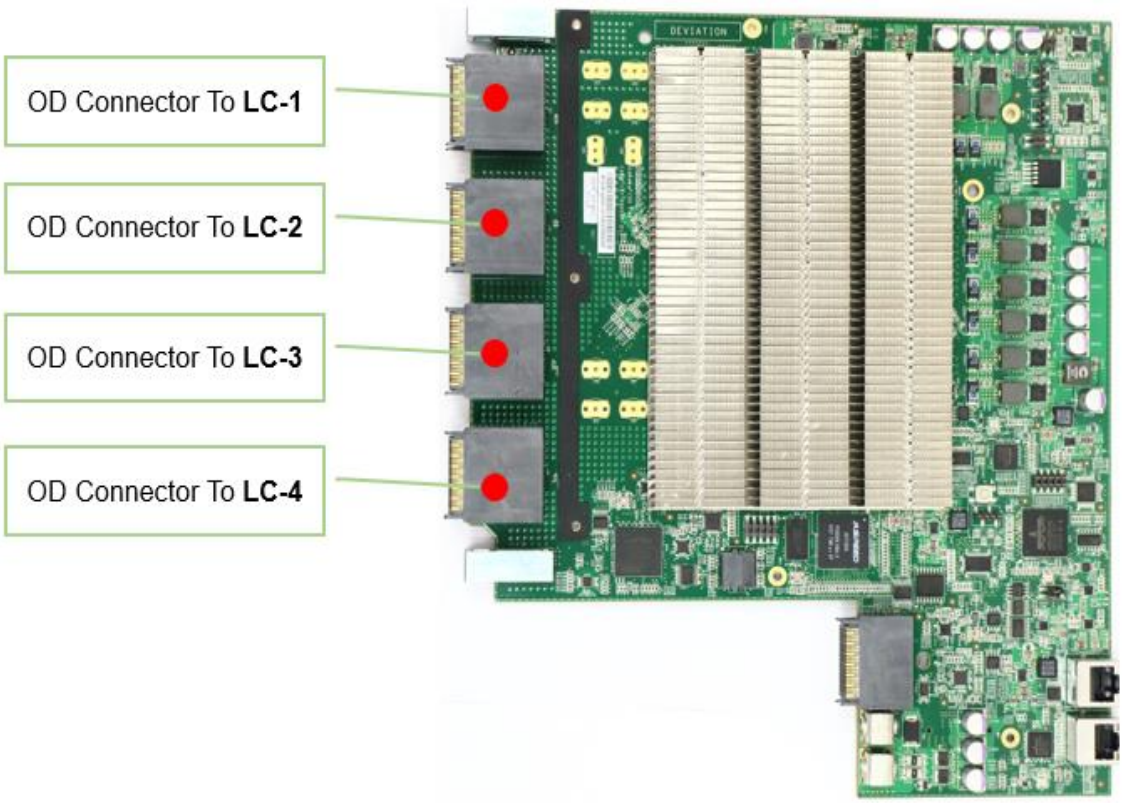

Figure 14: FAB OD connector to LC

The port mapping of FAB is shown in the following table:

Port No.	TD/RD Lane	SDK Port No.	FalconCore		TD Lane	RD Lane	TD P/N reversal	RD P/N reversal	Note
Backplane Port 1	Lane 0	CE0	FC 17	Lane	0	3	Y	N	To LC #1
	Lane 1			Lane	1	2	Y	N	
	Lane 2			Lane	2	1	Y	N	
	Lane 3			Lane	3	0	Y	N	
Backplane Port 2	Lane 0	CE1	FC 18	Lane	0	3	Y	N	
	Lane 1			Lane	1	2	Y	N	
	Lane 2			Lane	2	1	Y	N	
	Lane 3			Lane	3	0	Y	N	
	Lane 0	CE2	FC 16	Lane	3	0	N	N	

Backplane Port 3	Lane 1			**Lane**	2	1	N	N	
	Lane 2			**Lane**	1	2	N	N	
	Lane 3			**Lane**	0	3	N	N	
Backplane Port 4	Lane 0	**CE3**	**FC 19**	**Lane**	2	2	N	Y	
	Lane 1			**Lane**	0	0	N	Y	
	Lane 2			**Lane**	3	3	N	Y	
	Lane 3			**Lane**	1	1	N	Y	
Backplane Port 5	Lane 0	**CE4**	**FC15**	**Lane**	0	2	Y	N	
	Lane 1			**Lane**	1	0	Y	N	
	Lane 2			**Lane**	3	3	Y	N	
	Lane 3			**Lane**	2	1	Y	N	
Backplane Port 6	Lane 0	**CE5**	**FC 14**	**Lane**	3	0	Y	N	
	Lane 1			**Lane**	2	1	Y	N	
	Lane 2			**Lane**	1	2	Y	N	
	Lane 3			**Lane**	0	3	Y	N	
Backplane Port 7	Lane 0	**CE6**	**FC 13**	**Lane**	3	0	Y	N	
	Lane 1			**Lane**	2	1	Y	N	
	Lane 2			**Lane**	1	2	Y	N	
	Lane 3			**Lane**	0	3	Y	N	
Backplane Port 8	Lane 0	**CE7**	**FC 12**	**Lane**	3	0	Y	N	
	Lane 1			**Lane**	2	1	Y	N	
	Lane 2			**Lane**	1	2	Y	N	
	Lane 3			**Lane**	0	3	Y	N	
Backplane Port 1	Lane 0	**CE8**	**FC 26**	**Lane**	0	1	Y	N	To LC #2
	Lane 1			**Lane**	1	0	Y	N	
	Lane 2			**Lane**	2	3	Y	N	
	Lane 3			**Lane**	3	2	Y	N	
Backplane Port 2	Lane 0	**CE9**	**FC 25**	**Lane**	3	2	N	Y	
	Lane 1			**Lane**	2	3	N	Y	
	Lane 2			**Lane**	1	0	N	Y	
	Lane 3			**Lane**	0	1	N	Y	
Backplane Port 3	Lane 0	**CE10**	**FC 24**	**Lane**	0	1	Y	N	
	Lane 1			**Lane**	1	0	Y	N	
	Lane 2			**Lane**	2	3	Y	N	
	Lane 3			**Lane**	3	2	Y	N	
Backplane Port 4	Lane 0	**CE11**	**FC 27**	**Lane**	3	3	N	Y	
	Lane 1			**Lane**	2	1	N	Y	
	Lane 2			**Lane**	1	2	N	Y	
	Lane 3			**Lane**	0	0	N	Y	
Backplane Port 5	Lane 0	**CE12**	**FC23**	**Lane**	3	3	N	N	
	Lane 1			**Lane**	2	1	N	N	
	Lane 2			**Lane**	0	2	N	N	
	Lane 3			**Lane**	1	0	N	N	
Backplane Port 6	Lane 0	**CE13**	**FC 22**	**Lane**	3	2	Y	Y	
	Lane 1			**Lane**	2	3	Y	Y	

	Lane 2			**Lane**	1	0	Y	Y	
	Lane 3			**Lane**	0	1	Y	Y	
Backplane Port 7	Lane 0	**CE14**	**FC 20**	**Lane**	3	2	Y	N	
	Lane 1			**Lane**	2	3	Y	N	
	Lane 2			**Lane**	1	0	Y	N	
	Lane 3			**Lane**	0	1	Y	N	
Backplane Port 8	Lane 0	**CE15**	**FC 21**	**Lane**	0	1	N	Y	
	Lane 1			**Lane**	1	0	N	Y	
	Lane 2			**Lane**	2	3	N	Y	
	Lane 3			**Lane**	3	2	N	Y	
Backplane Port 1	Lane 0	**CE16**	**FC 1**	**Lane**	3	0	Y	N	To LC #3
	Lane 1			**Lane**	2	1	Y	N	
	Lane 2			**Lane**	1	2	Y	N	
	Lane 3			**Lane**	0	3	Y	N	
Backplane Port 2	Lane 0	**CE17**	**FC 2**	**Lane**	3	0	Y	N	
	Lane 1			**Lane**	2	1	Y	N	
	Lane 2			**Lane**	1	2	Y	N	
	Lane 3			**Lane**	0	3	Y	N	
Backplane Port 3	Lane 0	**CE18**	**FC 0**	**Lane**	3	0	Y	Y	
	Lane 1			**Lane**	2	1	Y	Y	
	Lane 2			**Lane**	1	2	Y	Y	
	Lane 3			**Lane**	0	3	Y	Y	
Backplane Port 4	Lane 0	**CE19**	**FC 3**	**Lane**	2	0	Y	N	
	Lane 1			**Lane**	0	2	Y	N	
	Lane 2			**Lane**	3	1	Y	N	
	Lane 3			**Lane**	1	3	Y	N	
Backplane Port 5	Lane 0	**CE20**	**FC 31**	**Lane**	0	1	Y	N	
	Lane 1			**Lane**	1	0	Y	N	
	Lane 2			**Lane**	3	3	Y	N	
	Lane 3			**Lane**	2	2	Y	N	
Backplane Port 6	Lane 0	**CE21**	**FC 28**	**Lane**	3	2	Y	N	
	Lane 1			**Lane**	2	3	Y	N	
	Lane 2			**Lane**	1	0	Y	N	
	Lane 3			**Lane**	0	1	Y	N	
Backplane Port 7	Lane 0	**CE22**	**FC 29**	**Lane**	0	3	Y	N	
	Lane 1			**Lane**	1	2	Y	N	
	Lane 2			**Lane**	2	1	Y	N	
	Lane 3			**Lane**	3	0	Y	N	
Backplane Port 8	Lane 0	**CE23**	**FC 30**	**Lane**	0	3	Y	N	
	Lane 1			**Lane**	1	2	Y	N	
	Lane 2			**Lane**	2	1	Y	N	
	Lane 3			**Lane**	3	0	Y	N	
Backplane Port 1	Lane 0	**CE24**	**FC 10**	**Lane**	3	3	N	Y	To LC #4
	Lane 1			**Lane**	2	2	N	Y	
	Lane 2			**Lane**	1	1	N	Y	
	Lane 3			**Lane**	0	0	N	Y	

Backplane Port 2	Lane 0	**CE25**	**FC 9**	**Lane**	0	0	Y	N	
	Lane 1			**Lane**	1	1	Y	N	
	Lane 2			**Lane**	2	2	Y	N	
	Lane 3			**Lane**	3	3	Y	N	
Backplane Port 3	Lane 0	**CE26**	**FC 7**	**Lane**	0	0	Y	N	
	Lane 1			**Lane**	1	1	Y	N	
	Lane 2			**Lane**	2	2	Y	N	
	Lane 3			**Lane**	3	3	Y	N	
Backplane Port 4	Lane 0	**CE27**	**FC 11**	**Lane**	1	1	Y	N	
	Lane 1			**Lane**	3	3	Y	N	
	Lane 2			**Lane**	0	0	Y	N	
	Lane 3			**Lane**	2	2	Y	N	
Backplane Port 5	Lane 0	**CE28**	**FC 8**	**Lane**	3	3	N	Y	
	Lane 1			**Lane**	2	1	N	Y	
	Lane 2			**Lane**	0	2	N	Y	
	Lane 3			**Lane**	1	0	N	Y	
Backplane Port 6	Lane 0	**CE29**	**FC 5**	**Lane**	3	3	Y	N	
	Lane 1			**Lane**	2	2	Y	N	
	Lane 2			**Lane**	1	1	Y	N	
	Lane 3			**Lane**	0	0	Y	N	
Backplane Port 7	Lane 0	**CE30**	**FC 6**	**Lane**	0	0	N	Y	
	Lane 1			**Lane**	1	1	N	Y	
	Lane 2			**Lane**	2	2	N	Y	
	Lane 3			**Lane**	3	3	N	Y	
Backplane Port 8	Lane 0	**CE31**	**FC 4**	**Lane**	0	0	N	Y	
	Lane 1			**Lane**	1	1	Y	Y	
	Lane 2			**Lane**	2	2	N	Y	
	Lane 3			**Lane**	3	3	N	Y	

Table 6: FAB Tomahawk Port Mapping

5.2.3. FAB I2C Diagram

The following diagram shows the I2C architecture of FAB.

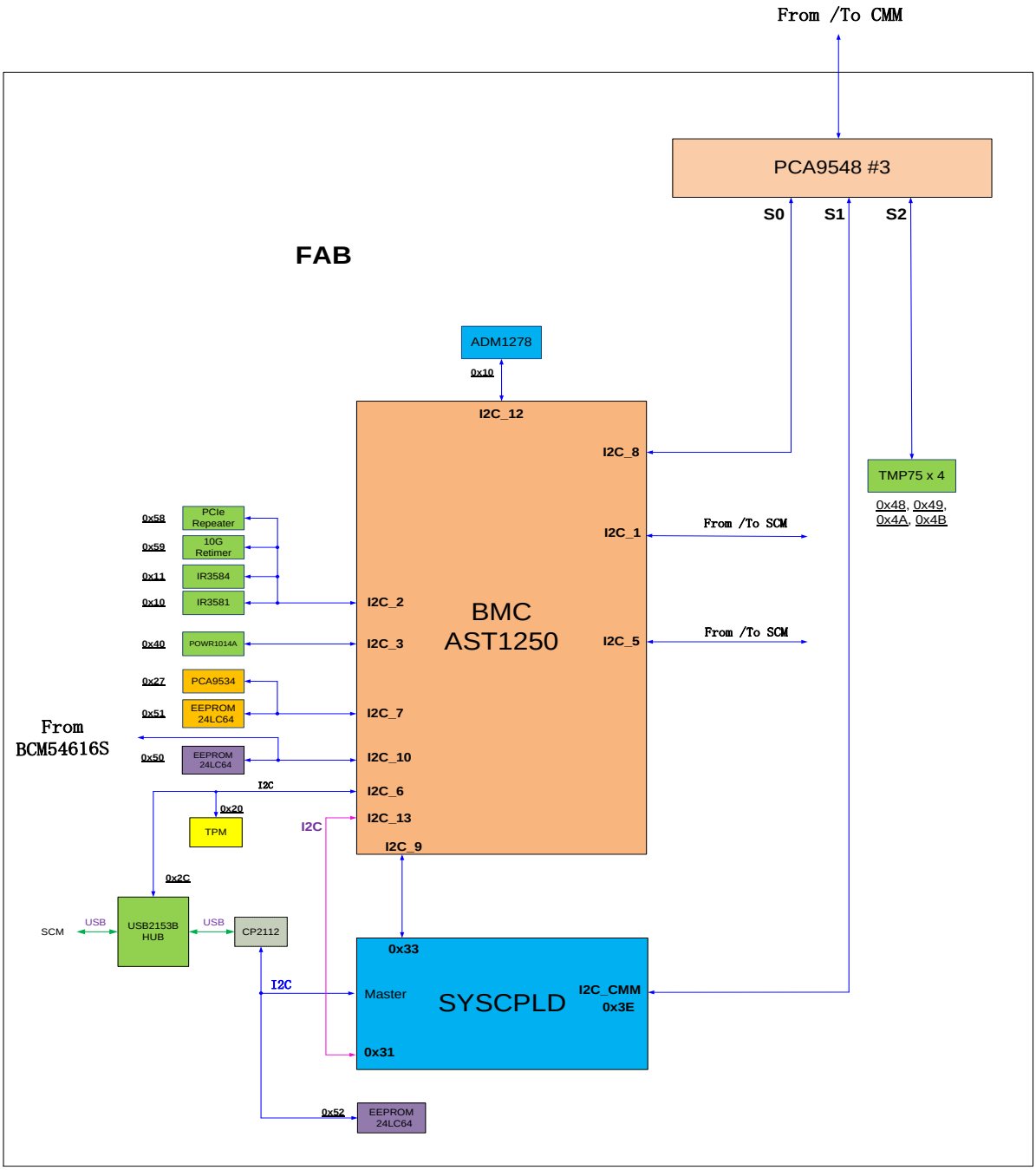

Figure 15: FAB I2C Block Diagram

I2C Controller	I2C Address	I2C Device
BMC_I2C_1	0x52	SYS EEPROM (SCM)
	0x54	BCM54616S EEPROM (SCM)
	0x21	PCA9534 (SCM)
	0x10	ADM1278 (SCM)
	0x58	DS80PCI402 (SCM)
	0x59	DS100BR111 (SCM)
	0x3e	SYS CPLD (SCM)
	0x33	COM-E (SCM)
SCM	reserved	BMC_I2C_5
CMM	0x70	PCA9548
PCA9548	S0	BMC_I2C_8
	S1	Syscpld(0x3e)
	S2	Temp sensor (0x48/49/4A/4B)
BMC_I2C_2	reserved	PCIe Repeater
	0x59	10G Repeater
	0x11/0x72/0x73	IR3584
	0x10/0x70/0x71	IR3581
BMC_I2C_3	0x40	POWR1014
BMC_I2C_6	0x2c (reserved) 0x20	USB2153B TPM
BMC_I2C_7	0x27 0x51	PCA9534 EEPROM(24LC64)
BMC_I2C_9	0x33 (reserved)	System CPLD
BMC_I2C_10	0x50	EEPROM(24LC64)
BMC_I2C_12	0x10	ADM1278
BMC_I2C_13	0x31	System CPLD

Table 7: I2C devices of FAB BMC

5.2.4. FAB System CPLD Register Map

Both COM-e CPU and BMC can access System CPLD.

BMC access those registers through I2C bus 13. The i2c address of SYS CPLD is 0x31. COM-e CPU access thise CPLD registers through LPC interface. The base address in LPC is 0x0100.

The system CPLD support CPU & BMC read the register at same time. When write the register at same time the CPU will have higher priority.

Register 0x00: BOARD_VERSION – Board Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	4'b0100	MODEL_ID[4:0] 0000: Backpack LC Type-1 0100: Backpack FAB Type-1 1100: Backpack CMM Type-1	MOD_ID
[3:0]	RO	0	BRD_REV[3:0]: PCB revision	PCB_VER

Register 0x01: CPLD_VERSION – CPLD Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	0	Reserved	Reserved
[6]	RO	0	Released Bit 0= not released, 1= Released version after PVT	RELEASE_STA
[5:0]	RO	Designed	CPLD Revision[5:0]	CPLD_VER

Register 0x02: CPLD_SUB_VERSION – CPLD Sub Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:0]	RO	0x01	CPLD sub-version, used for HW debug only	CPLD_SUB_VER

Register 0x03: SLOT_ID – Slot ID Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved	Reserved
[3:0]	RO	None	Chassis slot information 0000 Slot-1, LC-#1	SLOT_ID

			0001 Slot-2, LC-#2 0010 Slot-3, LC-#3 0011 Slot-4, LC-#4 0100 Slot-5, LC-#5 0101 Slot-6, LC-#6 0110 Slot-7, LC-#7 0111 Slot-8, LC-#8 1000 Slot-1, FAB-#1 1001 Slot-2, FAB-#2 1010 Slot-3, FAB-#3 1011 Slot-4, FAB-#4 1100 Unused ID 1101 Unused ID 1110 Unused ID 1111 Unused ID	

Register 0x04: HCP_ID – HCP ID Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved	Reserved
[1:0]	RO	None	HCP information	HCP_ID

Register 0x06: SYS_LED_CTRL – System LED Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	R/W	0xF	Reserved.	Reserved
[3]	R/W	0b0	LED_BLINK_EN 0: LED No blink 1: LED Blink is ON	LED_BLINK
[2]	R/W	0b0	LED_BLUE 0: LED BLUE is OFF 1: LED NLUE is ON	LED_BLU
[1]	R/W	0b0	LED_GREEN 0: LED GREEN is OFF 1: LED GREEN is ON	LED_GRN

[0]	R/W	0b1	LED_1_RED 0: LED 1 RED is OFF 1: LED 1 RED is ON	LED_RED

Register 0x08: MODULE_PRESENT – Module Present Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:2]	RO	0x3F	Reserved	Reserved
[1]	RW	0b0	SCM OIR Record. Software write 0 to clear this record. 0:SCM OIR Event cleared 1:SCM OIR Event happened.	SCM_OIR_REC
[0]	RO	1b1	SCM Present 0:present 1:not present	SCM_PRESENT

Register 0x09: PEER_LC_CON_PRESENT – Peer LC Connector Present Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved	Reserved
[3]	RO	1b0	Peer LC Connector4 Present 0:present 1:not present	PEER_LC_CON4_PRESENT
[2]	RO	1b0	Peer LC Connector3 Present 0:present 1:not present	PEER_LC_CON3_PRESENT
[1]	RO	1b0	Peer LC Connector2 Present 0:present 1:not present	PEER_LC_CON2_PRESENT
[0]	RO	1b0	Peer LC Connector1 Present 0:present 1:not present	PEER_LC_CON1_PRESENT

Register 0x0A: HOT_SWAP_PG_STA – Hot Swap Power Good Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RO	0x7F	Reserved	Reserved

[0]	RO	1b0	The Status of HOTSWAP_PG_INV	HOTSWAP_PG_INV_STA

Register 0x0B: LM57_TOVER_STA – LM57 TOVER Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RO	0x7F	Reserved	Reserved
[0]	RO	1b0	The Status of LM57_TOVER	LM57_TOVER_STA

Register 0x10: SYS_PWR_CTRL – System Power Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:5]	RW	0x7	Reserved.	Reserved
[4]	RW	0b1	PWR_MAIN_FORCE Control	PWR_MAIN_FORCE
[3:2]	RW	0x3	Reserved.	Reserved
[1]	RW	0b1	PWR_MAIN_EN 0: Main power is OFF 1: Main Power is enabled	PWR_MAIN_EN
[0]	RW	0b1	PWR_CYC_ALL_N 0: Write 0 to this bit will trigger PWR1014A to start power cycling of all power rail 1: normal	PWR_CYC_ALL_N

Register 0x11: SYS_RST_CTRL – System Reset Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RW	0xF	Reserved	Reserved
[3]	RW	0b1	PWR_RST_REQ_N 0: write 0 to trigger power reset 1: normal	PWR_RST_REQ
[2]	RW	0b1	COLD_RST_REQ_N 0: write 0 to trigger cold reset 1: normal	COLD_RST_REQ
[1]	RW	0b1	WARM_RST_REQ_N 0: write 0 to trigger warm reset	WARM_RST_REQ

			1: normal	
[0]	RW	0b1	HOT_RST_REQ_N 0: write 0 to trigger hot reset 1: normal	HOT_RST_REQ

Register 0x12: TH_RST_CTRL – BCM56960 Reset Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RW	0xF	Reserved.	Reserved
[3]	RW	0b0	TH_PCIE_RST_N Mask 0: normal 1: Mask the CB_RESET_N from SCM card to TH_PCIE_RST_N	TH_PCIE_RST_MASK
[2]	RW	0b0	TH_SYS_RST_N 0: normal 1: Mask the CB_RESET_N from SCM card to TH_SYS_RST_N	TH_SYS_RST_N_MASK
[1]	RW	0b1	TH_PCIE_RST_N 0: write 0 to trigger tomahawk PCIe reset 1: normal	TH_PCIE_RST_N
[0]	RW	0b1	TH_SYS_RST_N 0: write 0 to trigger tomahawk system reset 1: normal	TH_SYS_RST_N

Register 0x14: SEP_RST_CTRL – Separate Reset Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RW	0b1	Reserved.	Reserved
[6]	RW	0b1	LPC Interface Reset 0: reset 1: normal	LPC_INTF_RST
[5]	RW	0b1	SCM CPLD I2C Slave Reset 0: reset 1: normal	SCM_CPLD_I2C_SLAVE_RST
[4]	RW	0b1	BCM54616S_RST_N	BCM54616S_RST

			0: reset 1: normal	
[3]	RW	0b1	SWITCHPHY_RST_N 0: reset 1: normal	SWITCHPHY_RST
[2]	RW	0b1	BCM5389_RST_N 0: reset 1: normal	BCM5389_RST
[1]	RW	0b1	USB_HUB_RST_N 0: reset 1: normal	USB_HUB_RST
[0]	RW	0b1	CP2112_RST_N 0: reset 1: normal	CP2112_RST

Register 0x15: HW_SHUTDOWN_REC – Hardware Shutdown Reocrd Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:0]	RW	0x0	0x0: Normal status. 0x11: Hardware shutdown recorded.	HW_SHUTDOWN_REC

Register 0x16: TH_RST_REC – TH Reset Reocrd Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:0]	RW	0x0	0x0: Write Clear status. 0x11: Power on reset TH. 0x22: COMe CB_RESET_N reset TH. 0x33: Register control reset TH.	TH_RST_REC

Register 0x20: BMC_RST_EN – BMC Reset Enable Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	0b1	Reserved.	Reserved
[6]	RW	0b0	BMC_WDT2_EN	BMC_WDT2_EN
[5]	RW	0b0	BMC_WDT1_EN	BMC_WDT1_EN
[4]	RW	0b0	BMC_RESET4_EN	BMC_RST4_EN

			0: BMC reset 4 request is disabled 1: BMC reset 4 request is enabled	
[3]	RW	0b0	BMC_RESET3_EN 0: BMC reset 3 request is disabled 1: BMC reset 3 request is enabled	BMC_RST3_EN
[2]	RW	0b0	BMC_RESET2_EN 0: BMC reset 2 request is disabled 1: BMC reset 2 request is enabled	BMC_RST2_EN
[1]	RW	0b0	BMC_RESET1_EN 0: BMC reset 1 request is disabled 1: BMC reset 1 request is enabled	BMC_RST1_EN
[0]	RW	0b0	BMC_MAIN_RESET_N 0: BMC main reset request is disabled 1: BMC main reset request is enabled	BMC_MAIN_RESET_EN

Register 0x21: BMC_RST_CTRL – BMC Reset Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RW	0x7F	Reserved.	Reserved
[0]	RW	0x1	CPLD_BMC_RST_N Control 0: write 0 to trigger BMC reset 1: normal	BMC_RST

Register 0x22: BMC_RST_TYPE – BMC Reset Type Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:0]	RW	0x11	After power on this register default values set to 0x11. When BMC run, need this register to other values.	BMC_RST_TYPE

Register 0x30: UART_MUX_CTRL – UART MUX Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:3]	RO	0x0	Reserved.	Reserved
[2]	RO	0b0	0:Use BMC UART1 for sol function	SOL_UART_SEL

			1:Use BMC UART4 for sol function	
[1:0]	RO	2b00	TH_UART selection 00: Tomahawk UART-0 connected with BMC UART2 01: Tomahawk UART-2 connected with BMC UART2 10: Tomahawk UART-3 connected with BMC UART2 11: reserved	UART_MUX_CTRL

Register 0x40: ROV_STA – ROV Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved.	Reserved
[3:0]	RO	4b1000	TH_ROV[3:0] ROV[3:0] Voltage 4'b0000 1.2000 4'b0001 1.1750 4'b0010 1.1500 4'b0011 1.1250 4'b0100 1.1000 4'b0101 1.0750 4'b0110 1.0500 4'b0111 1.0250 4'b1000 1.0000 4'b1001 0.9750 4'b1010 0.9500 4'b1011 0.9250 4'b1100 0.9000 4'b1101 0.8750 4'b1110 0.8500 4'b1111 0.8250	ROV_STA

Register 0x41: BD_PWR_STA – On Board Power Status Register

Bit #	R/W	Default Value	Description	Name
[7:4]	RO	0xF	Reserved.	Reserved
[3]	RO	1b1	IR3584_1.0V_VRHOT 0: over temperature is negative 1: over temperature is active	IR3584_1V_VRHOT
[2]	RO	1b1	IR3584_1.0V_VRRDY1 0: power not OK 1: Power is OK	IR3584_1V_VRDY1
[1]	RO	1b1	IR3581_VRHOT 0: over temperature is negative 1: over temperature is active	IR3581_VRHOT
[0]	RO	1b1	IR3581_VRRDY1 0: power not OK 1: Power is OK	IR3581_VRRDY1

Register 0x50: CP2112_IN – CP2112 Bridge GPIO Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	1b1	CP2112_GPIO_IN[7]	CP2112_IN7
[6]	RO	1b1	CP2112_GPIO_IN[6]	CP2112_IN6
[5]	RO	1b1	CP2112_GPIO_IN[5]	CP2112_IN5
[4]	RO	1b1	CP2112_GPIO_IN[4]	CP2112_IN4
[3]	RO	1b1	CP2112_GPIO_IN[3]	CP2112_IN3
[2]	RO	1b1	CP2112_GPIO_IN[2]	CP2112_IN2
[1]	RO	1b1	CP2112_GPIO_IN[1]	CP2112_IN1
[0]	RO	1b1	CP2112_GPIO_IN[0]	CP2112_IN0

Register 0x51: CP2112_OE – CP2112 Bridge GPIO OE Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RW	1b1	CP2112_GPIO_OE[7]	CP2112_OE7
[6]	RW	1b1	CP2112_GPIO_OE[6]	CP2112_OE6
[5]	RW	1b1	CP2112_GPIO_OE[5]	CP2112_OE5
[4]	RW	1b1	CP2112_GPIO_OE[4]	CP2112_OE4
[3]	RW	1b1	CP2112_GPIO_OE[3]	CP2112_OE3
[2]	RW	1b1	CP2112_GPIO_OE[2]	CP2112_OE2

[1]	RW	1b1	CP2112_GPIO_OE[1]	CP2112_OE1
[0]	RW	1b1	CP2112_GPIO_OE[0]	CP2112_OE0

Register 0x52: CP2112_OUT – CP2112 Bridge GPIO Output Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RW	1b1	CP2112_GPIO_OUT[7]	CP2112_OUT7
[6]	RW	1b1	CP2112_GPIO_OUT[6]	CP2112_OUT6
[5]	RW	1b1	CP2112_GPIO_OUT[5]	CP2112_OUT5
[4]	RW	1b1	CP2112_GPIO_OUT[4]	CP2112_OUT4
[3]	RW	1b1	CP2112_GPIO_OUT[3]	CP2112_OUT3
[2]	RW	1b1	CP2112_GPIO_OUT[2]	CP2112_OUT2
[1]	RW	1b1	CP2112_GPIO_OUT[1]	CP2112_OUT1
[0]	RW	1b1	CP2112_GPIO_OUT[0]	CP2112_OUT0

Register 0x60: CMM_MS_STA – CMM M/S Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0xF	Reserved.	Reserved
[3]	RO	None	ACT_CMM2_N Status 0:CMM2 is master 1:CMM2 is slave	CMM1_STA
[2]	RO	None	ACT_CMM1_N Status 0:CMM1 is master 1:CMM1 is slave	CMM1_STA
[1:0]	RO	0x3	Reserved.	Reserved

Register 0x80: SYS_DEBUG_CTRL – System Debug Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	1b1	Reserved.	Reserved
[6]	RO	1b1	ISO_FORCE_MODE 0: BMC control 1: CPLD forced mode	ISO_FORCE_MODE
[5]	RO	1b1	BMC_ISO_BUF_EN	BMC_ISO_BUF_EN

			Data to enable or disable isolation buffer for BMC 0: disabled 1: buffer enabled	
[4]	RO	1b1	ISO_BUF_EN Data to enable or disable isolation buffer for BCM56960. 0: disable 1: buffer enabled	ISO_BUF_EN
[3]	RO	1b1	Reserved.	Reserved
[2]	RO	1b1	Force_2nd_Write 0: normal mode 1: always writable, debug mode	Force_2nd_Write
[1]	RO	1b1	EN_2nd_Flash_WP 0: writable 1: write protected	EN_2nd_Flash_WP
[0]	RO	1b1	DUAL_BOOT_EN 0: single boot 1: dual boot	DUAL_BOOT_EN

Register 0x90: I2C_RATE_CTRL – I2C Rate Control Register			
Bit #	**R/W**	**Default Value**	**Description**
[7]	RO	0b0	Reserved.
[6]	R/W	0b1	Baud rate setting. 0:50KHz, 1:100KHz
[5:0]	RO	0x0	Reserved.

Register 0x91: I2C_OP_CODE – I2C Operation Code Register			
Bit #	**R/W**	**Default Value**	**Description**
[7:4]	R/W	0x0	The I2C operation data byte length. Indicates 1~8byte.
[3:2]	RO	0x0	Reserved.
[1:0]	R/W	0x0	The I2C operation command byte length. Indicates 0~3 byte. When the length is 0, it means this I2C operation is a "Current Adress Read".

Register 0x92: I2C_SLV_ADDR – I2C Slave Address Register			
Bit #	**R/W**	**Default Value**	**Description**
[7:1]	R/W	0x0	The I2C slave device address.
[0]	R/W	0b0	Read/Write indicator. 1: Read operation. 0: Write operation.

Register 0x93: I2C_CMD_BYTE0 – I2C Command Byte0 Register			
Bit #	**R/W**	**Default Value**	**Description**
[7:0]	R/W	0x0	The I2C slave's command (memory address) byte 0.

Register 0x94: I2C_CMD_BYTE1 – I2C Command Byte1 Register			
Bit #	**R/W**	**Default Value**	**Description**
[7:0]	R/W	0x0	The I2C slave's command (memory address) byte 1.

Register 0x95: I2C_CMD_BYTE2 – I2C Command Byte2 Register

Bit #	R/W	Default Value	Description
[7:0]	R/W	0x0	The I2C slave's command (memory address) byte 2.

Register 0x96: I2C_STA_RST – I2C Status & Soft Reset Register			
Bit #	**R/W**	**Default Value**	**Description**
[7]	RO	0b0	I2C Master error. If the Master encounters timeout or incomplete frame, this bit will be '1'. It can only be cleared by soft reset to I2C Master.
[6]	RO	0b0	I2C busy indicator. The CPU can only start an operation when it's '0'. During a read operation, only after it is back to '0', the read data is ready.
[5]	RO	0b1	SDA Pin Status.
[4]	RO	0b1	SCL Pin Status
[3]	R/W	0b1	Control SDA Pin Status.
[2]	R/W	0b1	Control SCL Pin Status.
[1]	R/W	0b0	0:I2C Signal control by LPC-I2C Master Logic 1:I2C Signal control by register bit[2] & bit[3].
[0]	R/W	0b1	I2C Master software reset. 0: Soft reset I2C Master. This bit needs to be manually written to '1' to normal state by Soft.

Register 0xA0, 0xA1... – 0xA8: I2C_WR_DATA0/7 – I2C Write Data Byte 0 - 7 Register			
Bit #	**R/W**	**Default Value**	**Description**
[7:0]	R/W	0x0	The data byte during I2C writing.

Register 0xB0, 0xB1... – 0xB8: I2C_RD_DATA0/7 – I2C Read Data Byte 0 - 7 Register			
Bit #	**R/W**	**Default Value**	**Description**
[7:0]	RO	0x0	The data byte got from I2C slave during I2C read.

5.3. BMC of LC and FAB

Both LC and FAB use AST1250 BMC chip, BMC is the management plane of Switch Element (SWE). AST 1250 is a powerful BMC chip with internal ARM926EJ CPU. It is integrated with many IO interfces, including DDR2/DDR3 interface, SPI interface, SMBUS/I2C interface, UART, LPC, USB 2.0, RGMII and GPIOs.

BCM of LC and FAB is used as hardware management unit to manage the onboard DC/DC convertors, temperature thermal sensors, power sequencer, UART interfaces, management I2C bus, CPLD access, EEPROM access, etc.

The supported features are below:

- All SEL commands
- Power on/off/cycle and hardware reset, software reset commands
- I2C access to power sequencer, and DC/DC convertors
- Dual SPI boot of BMC
- Onboard OOB switch MDIO interface
- Onboard PHY MDIO interface
- CPLD or flash online upgrade

5.3.1. Dual Boot SPI Flash

Two 32MB SPI flash devices are populated with BMC to support dual boot. The first device is controlled by CS0# for the primary boot, and the second device with CS1# is used for backup.

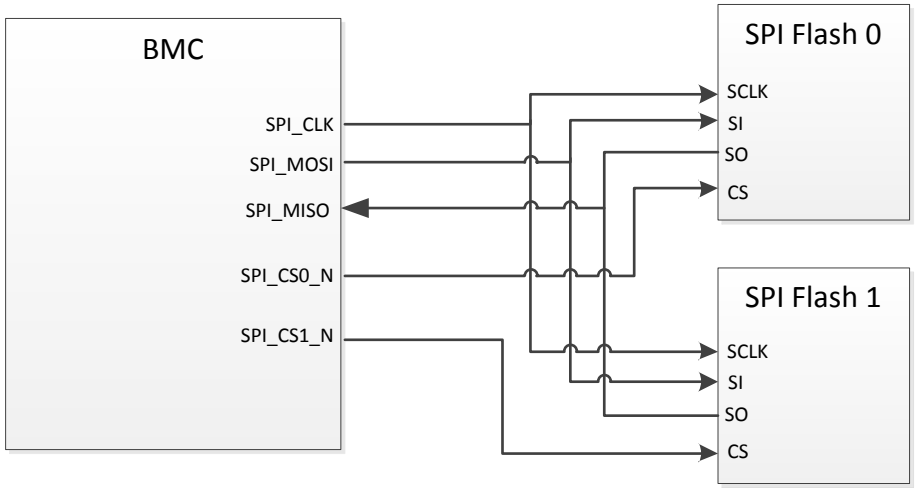

Figure 16: BMC FLash connection diagram

5.3.2. CPLD online upgrade

BMC can support online CPLD upgrade. BMC uses GPIOs to simulate the JTAG interface to upgrade CPLD. The following diagram show the connection.

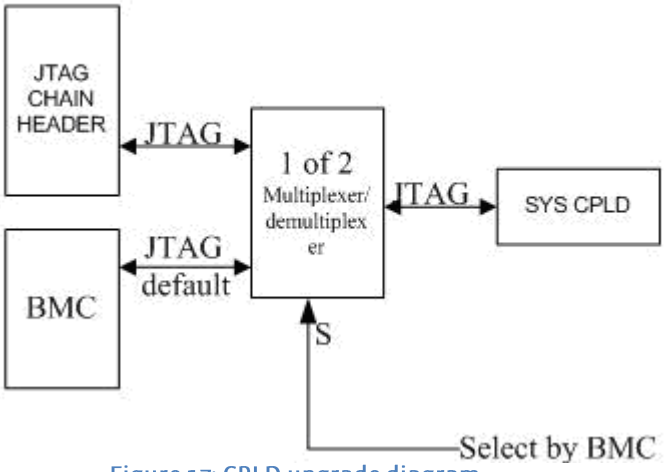

Figure 17: CPLD upgrade diagram

5.4. System Control Module

The System Control Module (SCM) has the host COM-E CPU for tomahawk ASIC. Each SCM can support two COM-E CPU module. The COM-E CPU module can be upgraded to Broadwell-DE CPU in the future if needed.

5.4.1. System Control Module Block Diagram

Each SCM has the following components:

- Two COM-E CPU modules
- RJ45 console port and USB Type-A port on front panel
- Each COM-E CPU module has one dedicated M.2 128Gbyte SSD
- CPLD is used to provide control and management function for SCM
- One dedicated I2C management bus need to be reserved for CMM access
- Control signals connect to HCP
- Power is provided by HPD

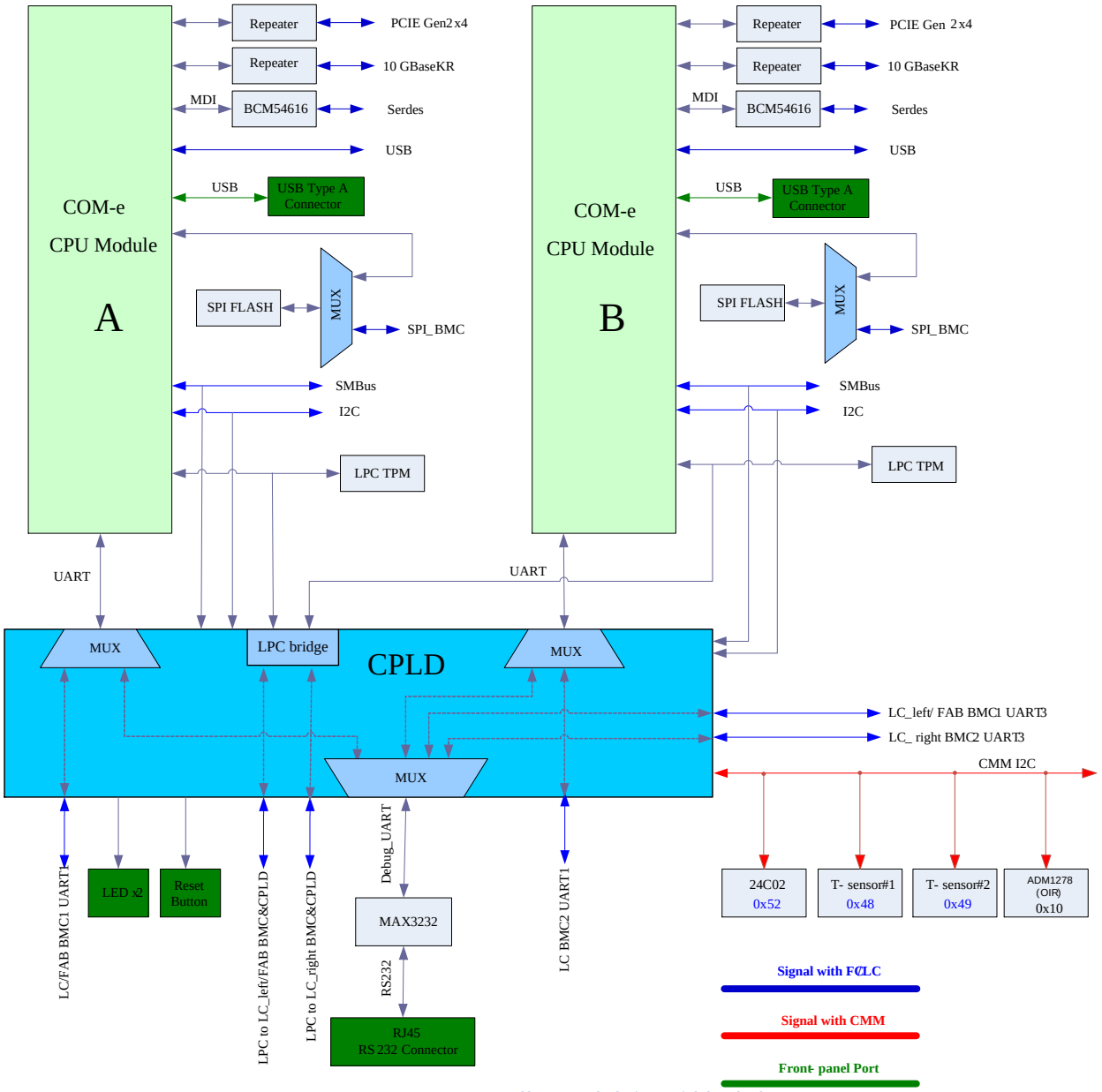

Figure 18: System Controller Module(SCM) block diagram

5.4.2. I2C of SCM

The following diagram shows the I2C diagram of SCM Board.

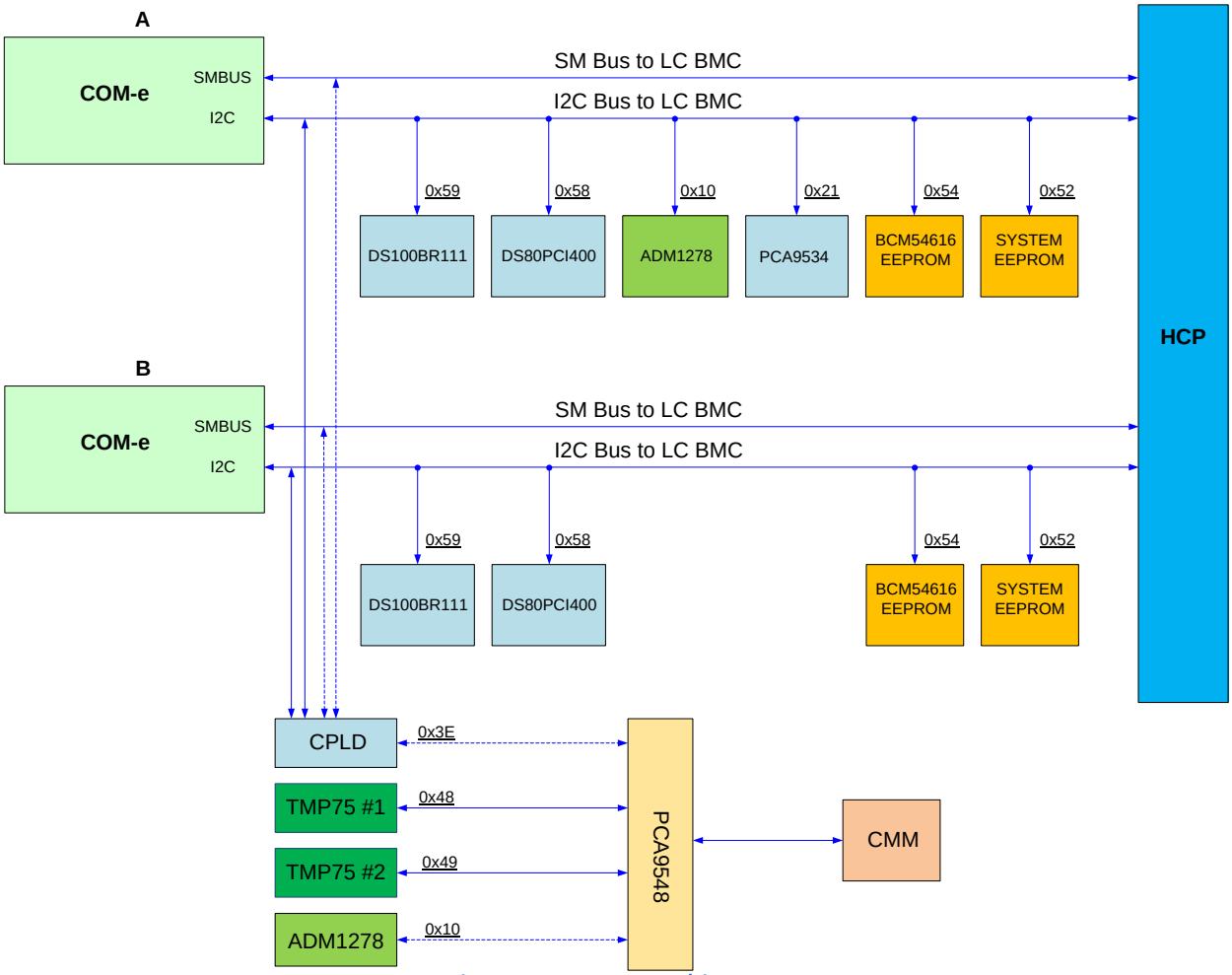

Figure 19: SCM I2C architecture

The following I2C devices can be accessed by LC left BMC, or FAB BMC.

I2C Controller	I2C/SMbus Address	I2C Device
BMC_I2C_1	0x33	COM-E EC
	0x3e	CPLD
	0x59	10GKR repeater
	0x58	PCIE repeater
	0x10	ADM1278
	0x21	PCA9534
	0x54	EEPROM for BCM54616S
	0x52	EEPROM for system

Table 8: SCM COM-e A I2C Devices

The following I2C devices can be accessed by LC right BMC.

I2C Controller	I2C/SMbus Address	I2C Device
BMC_I2C_1	0x33	COM-E EC
	0x3e	CPLD
	0x59	10GKR repeater
	0x58	PCIE repeater
	0x54	EEPROM for BCM54616S
	0x52	EEPROM for system

Table 9: SCM COM-e B I2C Devices

The devices below are on SCM board, but can be accessed by CMM BMC:

I2C Controller	I2C/SMbus Address		I2C Device
BMC_I2C_2	0x73		PCA9548
	S1	0x48	Thermal sensor in
	S2	0x49	Thermal sensor out

5.4.3. PCIe Bus

The PCIe bus of COM-e CPU module at SCM is routed across HCP, VCP backplane to tomahawk switch ASIC at LC and FAB. TI DS80PCI402SQE/NOPB is used as repeater on PCIE interface to extend the reach between SCM COM-e CPU and Switch ASIC at LC or FAB side. The DS80PCI402 is a low-power, 4-lane repeater with 4-stage input equalization, and an output de-emphasis driver to enhance the reach of PCI-Express serial links in board-to-board or cable interconnects.

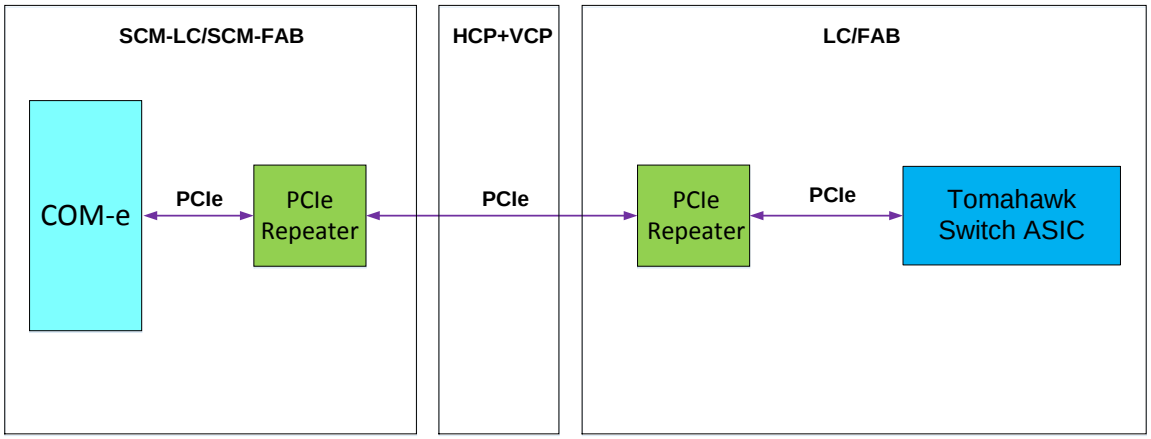

Figure 20: PCIe bus from SCM to LC/FAB

5.4.4. 10G KR interface

SCM reserves one pair of 10G KR signals across HCP, VCP to LC and FAB. current BayTrail COM-e CPU module does not support extra 10G KR ethernet interface, but it could be used in the future if Broadwell-DE COM-e express module is used. TI DS110DF111SQE/NOPB is used as repeater for 10GBase-KR interface between COM-e CPU module and LC/FAB Switch IC.

5.4.5. SCM LPC bus

The LPC bus of SCM COM-e CPU is extended across HCP and VCP to access the LPC slave devices on LC and FAB. a LPC to I2C bridge function is implemented in SYSCPLD at LC and FAB to provide LPC to I2C bridge function. The LPC-I2C bridge design is mainly to provide an alternative way for COM-e CPU to access I2C devices on LC or FAB. COM-e CPU can also access the I2C devices on main I2C bus of LC or FAB through USB-I2C CP2112 bridge control path.

Infineon SLB9660TT is the TPM with LPC interface, it is used in SCM, COM-e CPU can access it through local LPC bus.

The following diagram shows the LPC architecture of SCM and LC, SYSCPLD at LC side supports LPC to I2C bridge function, so COM-e CPU module can access the i2c devices on main I2C bus of LC, such as QSFP28, QSFP CPLD, and inventory EEPROM of LC.

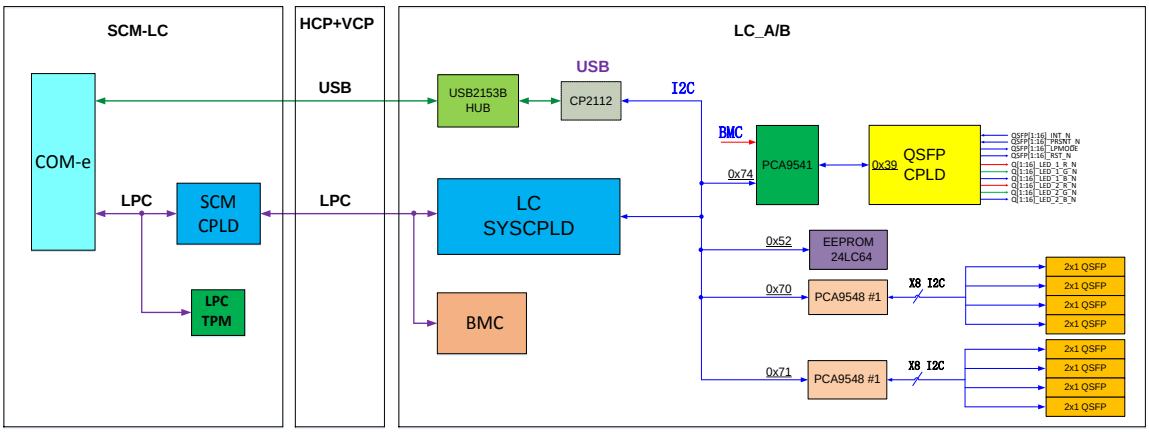

Figure 21: SCM and LC LPC bus diagram

The following diagram shows the LPC architecture of SCM and FAB, it has fewer components than LC because FAB has no QSFP ports, so there is no QSFP slaves in FAB main I2C bus. SYSCPLD at FAB side supports LPC to I2C bridge function, so COM-e CPU module can access the i2c devices on main I2C bus of FAB, FAB inventory EEPROM is the only one I2C device on main I2C bus of FAB.

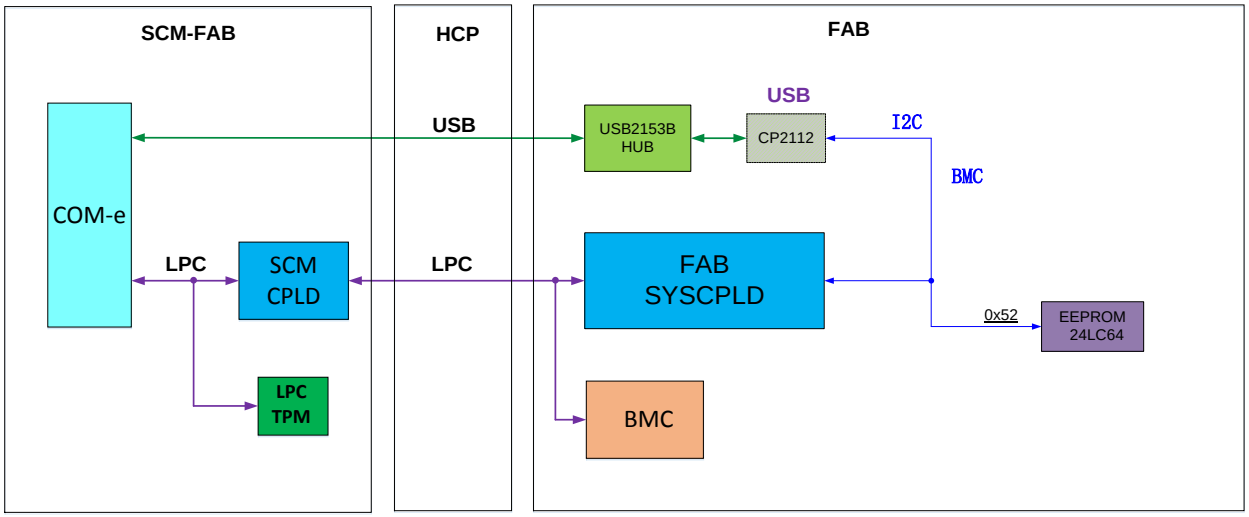

Figure 22: SCM and FAB LPC bus diagram

5.4.6. SPI bus of SCM

COM-e local SPI bus is used for the access of second booting SPI flash of CPU, the second booting SPI flash memory is on SCM main board, which can be accessed by both COM-e CPU and BMC chip on LC or FAB. if the COM-e CPU module is booting from second flash on main board, BMC has the capability to update booting SPI flash memory, it provides online upgrade capability of COM-e CPU BIOS, and is very useful in data center operation.

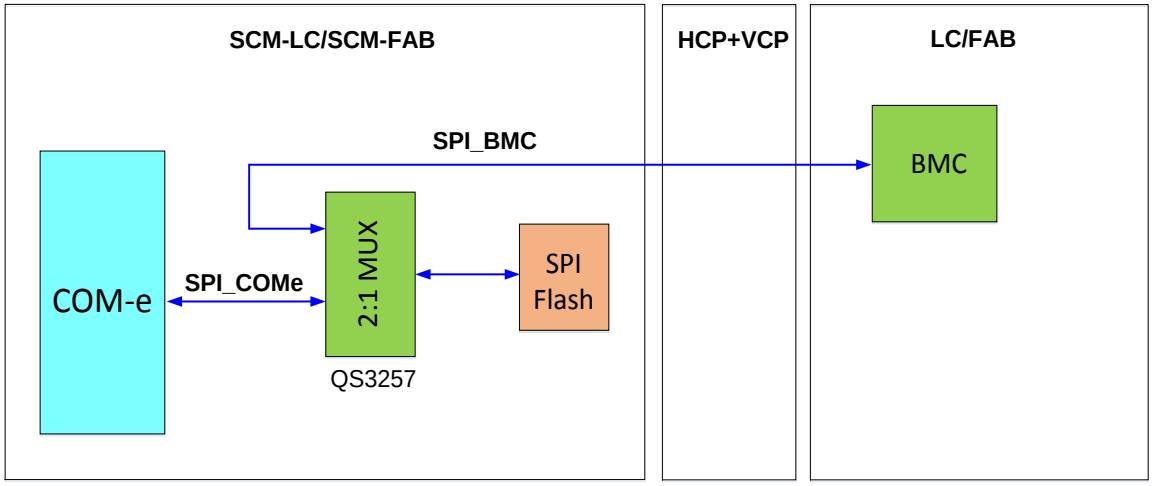

Figure 23: SPI bus of SCM and LC/FAB

5.4.7. SCM and LC/FAB USB architecture

The USB2 interface of SCM COM-e CPU is extended across HCP, and VCP to LC and FAB. A 3-port USB hub is located at LC or FAB to provide multiple USB connection to BMC, CP2112, and one unused debug port. The following diagram shows the architecture of USB interface.

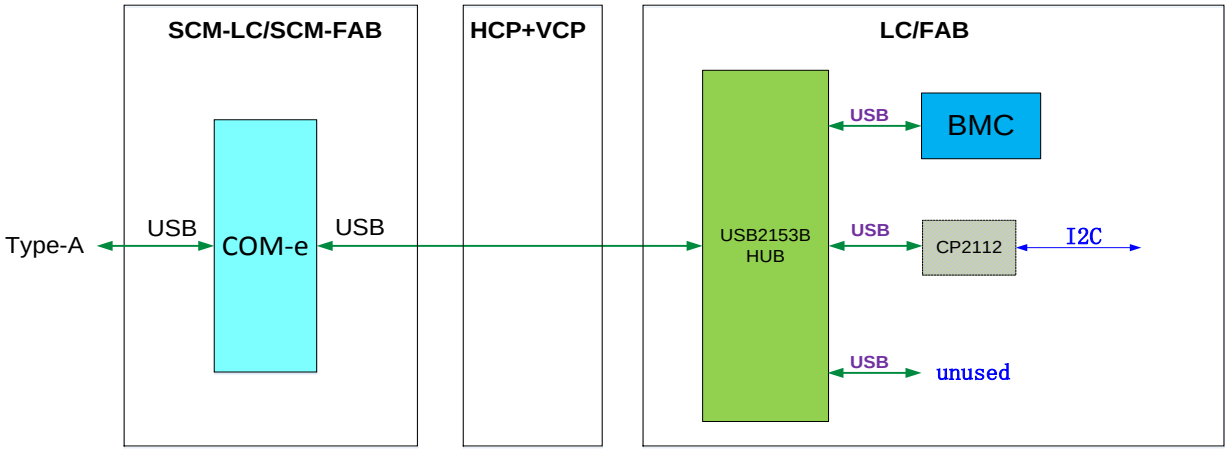

Figure 24: SCM USB Architecture

5.4.8. Hot swap design of SCM

SCM uses ADM1278 as hot swap controller, it supports current, voltage, power, temperature read back via an integrated 12bit ADC, it can be accessed using a PMBus interface.

System can read input voltage, output voltage, and measured current, measured temperature via PMbus. ADM1278 PMBus address is 0x10.

5.4.9. SCM System Control CPLD Register Map

SCM CPLD locates at LC or FAB BMC I2c Bus 0, its I2C address is 0x3E.

Register 0x00: BOARD_VERSION – Board Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved	Reserved
[3:0]	RO	0x0	BRD_REV[3:0]: PCB revision	PCB_VER

Register 0x01: CPLD_VERSION – CPLD Version **Register**				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	0	Reserved	Reserved
[6]	RO	0	Released Bit 0= not released, 1= Released version after PVT	RELEASE_STA
[5:0]	RO	Designed	CPLD Revision[5:0]	CPLD_VER

Register 0x02: CPLD_SUB_VERSION – CPLD Sub Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:0]	RO	0x01	CPLD sub-version, HW debug only	CPLD_SUB_VER

Register 0x03: SLOT_ID – Slot ID Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved	Reserved
[3:0]	RO	None	Chassis slot information 0000 Slot-1, unused in G4 0001 Slot-2, CMM0 in G4 0010 Slot-3, SCM-FAB1 0011 Slot-4, SCM-FAB2 0100 Slot-5, SCM-LC1 0101 Slot-6, SCM-LC2 0110 Slot-7, SCM-LC3	SLOT_ID

			0111 Slot-8, SCM-LC4 1000 Slot-9, SCM-FAB3 1001 Slot-10, SCM-FAB4 1010 Slot-11, CMM1 in G4 1011 Slot-12, unused in G4 1100 Unused ID 1101 Unused ID 1110 Unused ID 1111 Unused ID	

Register 0x04: HCP_ID – HCP ID Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:2]	RO	0x0	Reserved	Reserved
[1:0]	RO	None	HCP information	HCP_ID

Register 0x06: LED_TST – LED Test Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved	Reserved
[4]	R/W	0x0	LED Control 0:LED controlled by HW Logic 1:LED controlled by Bit[3:0]	LED_TST_EN
[3]	R/W	0b0	LED_BLINK_EN 0: LED No blink 1: LED Blink is ON	LED_BLINK
[2]	R/W	0b0	LED_BLUE 0: LED BLUE is OFF 1: LED NLUE is ON	LED_BLU
[1]	R/W	0b0	LED_GREEN 0: LED GREEN is OFF 1: LED GREEN is ON	LED_GRN
[0]	R/W	0b1	LED_RED 0: LED RED is OFF 1: LED RED is ON	LED_RED

Register 0x08: MODULE_PRESENT – Module Present Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RO	0x7F	Reserved	Reserved
[0]	RO	1b0	LC/FC Present 0:present 1:not present	LC_FC_PRESENT

Register 0x0A: HOT_SWAP_PG_STA – Hot Swap Power Good Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RO	0x7F	Reserved	Reserved
[0]	RO	1b0	The Status of HOTSWAP_PG_INV	HOTSWAP_PG_INV_STA

Register 0x0B: RTC_CLEAR_CTRL – RTC Clear Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RO	0x7F	Reserved	Reserved
[0]	RO	1b0	Control The Status of RTC_CLEAR	RTC_CLR_CTRL

Register 0x10: COMe_PWR_CTRL – COMe Power Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:3]	RW	0x1F	Reserved.	Reserved
[2]	RW	0b1	PWR_CYC _N Write 0 to this bit will trigger CPLD power cycling the COMe Module, This bit will automatically set to 1 after Power Cycle finish.	PWR_CYC _N
[1]	RW	0b1	PWR_COMe_FORCE Control When this bit set to 0, the CPLD will force the COMe module power off.	PWR_COME_FORCE
[0]	RW	0b0	PWR_COME_EN 0: COMe power is OFF 1: COMe power is ON	PWR_COME_EN

Register 0x11: COMe_RST_CTRL – COMe Reset Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RW	0x7F	Reserved.	Reserved
[0]	RW	0x1	COMe_RST_N 0: write 0 to trigger COMe reset 1: normal	COMe_RST_N

Register 0x12: COMe_STA – COMe Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved.	Reserved
[3]	RO	0b0	COMe Module SUS_STAT_N Status	COM_STAT
[2]	RO	0b0	COMe Module SUS_S5_N Status	COM_S5
[1]	RO	0b0	COMe Module SUS_S4_N Status	COM_S4
[0]	RO	0b0	COMe Module SUS_S3_N Status	COM_S3

Register 0x13: COMe_BIOS_DIS_CTRL – COMe BIOS DIS Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:2]	RW	0x3F	Reserved.	Reserved
[1]	RW	0b1	Control COMe BIOS DIS1	COM_BIOS_DIS1
[0]	RW	0b1	Control COMe BIOS DIS0	COM_BIOS_DIS0

Register 0x14: COMe_PWR_OFF_REC – COMe Power Off Record Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
7:0	R/W	0x0	0x0: Normal 0x11:LC/FAB remove cause CPLD control COMe to Power off. 0x22:LC/FAB BMC software control COMe to Power off. LC/FAB BMC can write any value to clear this register to 0x0.	COMe_PWR_OFF_REC

Register 0x16: SPI_FLASH_SEL_CTRL – SPI Flash Select Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RW	0x0	Reserved.	Reserved

[0]	RW	0b0	0:SPI Flash Accessed by COMe. 1:SPI Flash Accessed by BMC.	SPI_SEL

Register 0x18: BUF_ENABLE_CTRL – Buffer Enable Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:3]	RW	0x0	Reserved.	Reserved
[2]	RW	0b1	Control COM_I2C_CPLD_ISO_EN 1:Disbale 0:Enable	I2C_EN
[1]	RW	0b1	Control COM_SMB_CPLD_ISO_EN 1:Disbale 0:Enable	SMB_EN
[0]	RW	0b1	Control HOT_BUF_EN_N 1:Disbale 0:Enable	SPI_SEL

Register 0x20: BMC_INFO_EXCHANGE – Peer BMC Information Exchange Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0b0	Peer BMC Information	PEER_BMC_INFO
[3:0]	RW	0b0	Information to peer BMC	INFO_TO_PEER_BMC

Register 0x30: UART_MUX_RST – Uart Mux Reset Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	R/W	0x7F	Reserved.	Reserved
[0]	R/W	0b1	UART Mux logic reset 0: Reset UART Mux Logic. The UART connect return to default status. 1: Normal.	UART_MUX_RST

Register 0x31: LPC_BRIDGE_RST – LPC Bridge Reset Register

Bit #	R/W	Default Value	Description	Name
[7:1]	R/W	0x7F	Reserved.	Reserved
[0]	R/W	0b1	0: Reset LPC Bridge Logic. 1: Normal.	LPC_BRIDGE_RST

Register 0x60: CMM_MS_STA – CMM M/S Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:2]	RO	0x3F	Reserved.	Reserved
[1]		None	ACT_CMM2_N Status 0:CMM2 is master 1:CMM2 is slave	CMM2_STA
[0]		None	ACT_CMM1_N Status 0:CMM1 is master 1:CMM1 is slave	CMM1_STA

5.4.10.COM-Express CPU Module

COM-E CPU module is Portwell PCOM-B632VG based on Intel Atom Processor E3800 family (Code Name BayTrail) SOC, it has the following features:

- Processor
  - Intel® AtomTM processor E3800 family, 22nm process technology
  - Cache up to 2MB (for Quad Core)
  - DPM (Defect Per Million devices) <50
  - Support Intel® VT-x technology
- BIOS
  - AMI BIOS
- Memory - Support up to 8GB DDR3L 1066/1333 SDRAM on one 204-pin SODIMM
- Storage Devices
  - Two SATA 2.0
  - One Micro-SD slot
- Watchdog Timer
  - Programmable by embedded controller
- Expansion Interface
  - Supports up to four PCI Express lanes by LAN disable, four x 1 lanes can be configured to one x 4 lane (default 3x PCI-Express lanes)
  - SPI Interface
  - SM Bus interface
  - I2C interface
- I/O Interface
  - Audio - HDA controller integrated in SoC
  - Ethernet - Onboard Intel I210IT
  - Serial Port - Two series RX/TX supported from onboard EC (embedded controller)
  - USB
    - 6 ports USB2.0
    - 1 port USB3.0
  - Keyboard & Mouse - KB controller integrated in embedded controller
- Mechanic and Environment
  - Dimension - 95mm(L) x 95mm(W) x 2.0mm(H)
  - Power Supply - DC 6V~16.8V
  - Environment
    - Operation temperature: -40~80°C
    - Storage temperature: -40~80°C
    - Relative humidity : 5~95%, non-condensing
  - MTBF
    - Over 180000 hrs at 55°C

Backpack uses the following configuration:

- Boot SPI Flash: 8Mbyte, secondary on SCM main board
- M.2 SSD: 128Gbyte, physically located at SCM main board
- Memory: 8Gbyte DDR3L ECC 1600 with thermal sensor, 204-pin SODIMM
- BIOS: AMI UEFI
- Ethernet: 1000GbaseT, BCM PHY on SCM main board to provide SGMII interface
- PCIe: 3xPCIe Gen2, 2 lanes are used for Switch ASIC PCIe access
- SATA: 2x SATA 3.0Gb/s, one is used for M.2 SSD access
- USB port: USB 2.0 port is used for LC/FAB USB interface
- WDT: programmable via SW from 1s to 255min
- LPC: LPC bus at 33.33Mhz

The following is the block diagram of COM-E module:

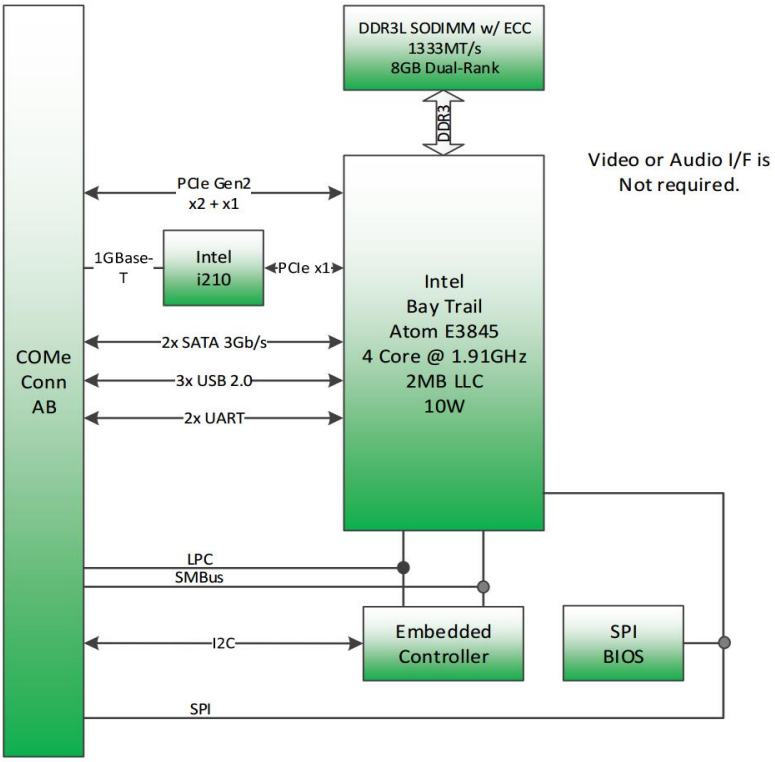

Figure 25: Portwell COM-E CPU Module Block Diagram

5.5. Chassis management Module

There are two Chassis management module in Backpack system: CMM1 and CMM2. one CMM is working as active CMM and the other one is working in standby mode. In default CMM1 will be master, the Software implementation can switch over CMM2 to be active if anything wrong in CMM1.

Each CMM has the following components:

- 16-port SGMII GBE Switch for chassis OOB ether network
  - 12 SGMII port to 12 switch element
  - 1 front panel RJ45 port
  - 1 SGMII to paired CMM OOB switch
  - 1 SGMII port to CMM AST2520 OOB ethernet interface
  - 1 SGMII port to CMM COM-E CPU Module(reserved for future use)
- 12-port UART MUX for chassis UART centralized management network
- Chassis Management I2C network
  - I2C management interface for 4 LC and 4 SCM-LC
  - I2C management interface for 4 FAB and 4 SCM-FAB
  - I2C management interface for PDB, PSU and SIM
  - I2C management interface for 4 FCB and Fan Trays
- Front port interfaces
  - RJ45 OOB ethernet port
  - RJ45 Console port
  - USB Type-A port

5.5.1. CMM and Backpack system Out-of-Band network architecture

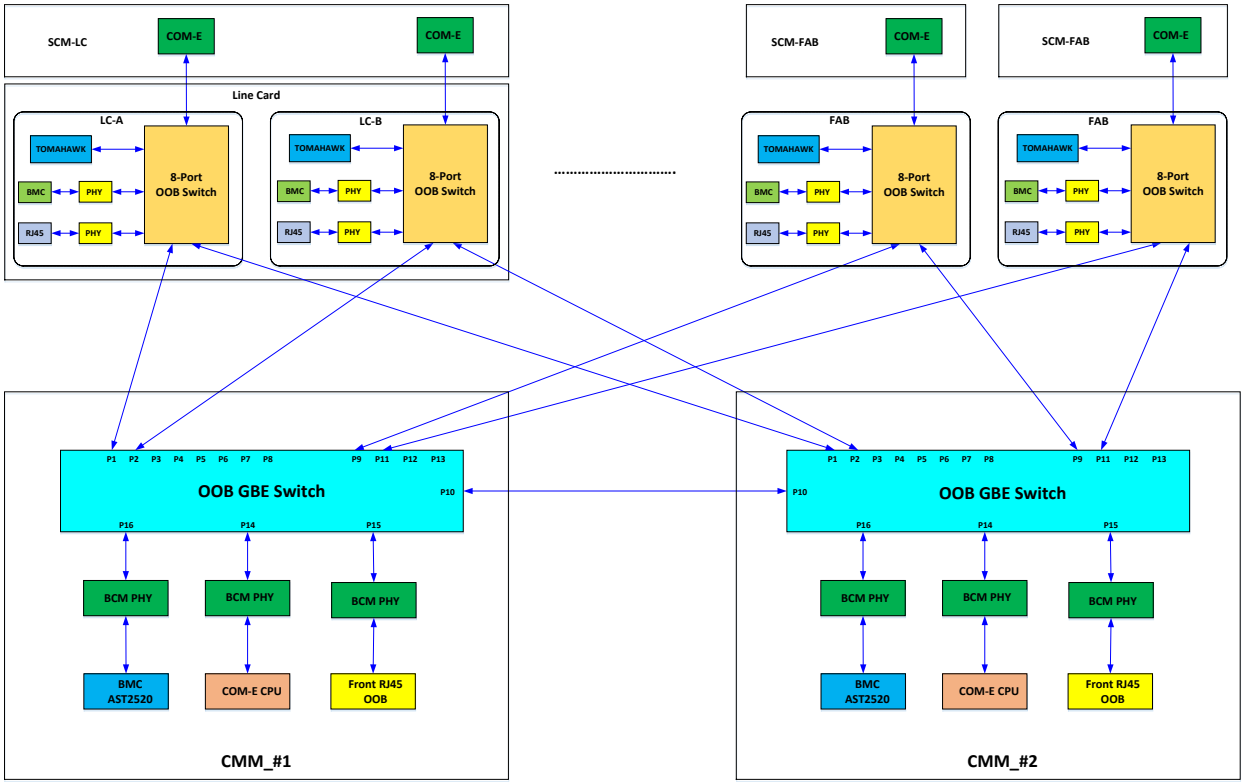

Figure 26: CMM OOB network architecture

BCM5396 Port	OOB Link Partner	Interface	Note
Port 1	LC #1A	1.25Gbs SerDes	OOB SGMII port for LC1 left SWE
Port 2	LC #1B	1.25Gbs SerDes	OOB SGMII port for LC1 right SWE
Port 3	LC #4A	1.25Gbs SerDes	OOB SGMII port for LC4 left SWE
Port 4	LC #2A	1.25Gbs SerDes	OOB SGMII port for LC2 left SWE
Port 5	LC #4B	1.25Gbs SerDes	OOB SGMII port for LC4 right SWE
Port 6	LC #3A	1.25Gbs SerDes	OOB SGMII port for LC3 left SWE
Port 7	LC #2B	1.25Gbs SerDes	OOB SGMII port for LC2 right SWE
Port 8	LC #3B	1.25Gbs SerDes	OOB SGMII port for LC3 right SWE
Port 9	FAB #4	1.25Gbs SerDes	OOB SGMII port for FAB4 SWE
Port 10	Peer CMM BCM5396 Port	1.25Gbs SerDes	CMM1 to CMM2 inter-connect
Port 11	FAB #3	1.25Gbs SerDes	OOB SGMII port for FAB3 SWE
Port 12	FAB #2	1.25Gbs SerDes	OOB SGMII port for FAB2 SWE
Port 13	FAB #1	1.25Gbs SerDes	OOB SGMII port for FAB1 SWE
Port 14	BCM54616S (PHY Addr 0x0D)	SGMII, 1.25Gbs	CMM reserved COM-e port
Port 15	BCM54616S (PHY Addr 0x0E)	SGMII, 1.25Gbs	CMM front panel RJ45 port
Port 16	BCM54616S (PHY Addr 0x0F)	SGMII, 1.25Gbs	CMM BMC AST2520 OOB
IMP Port	BMC AST2520	RGMII	

Table 10: CMM 16-Port OOB Switch Port Assignment

CMM 16-port OOB switch support dual configuration mode by using two different configuration EEPROM, if the CMM is in working mode, then all the ports are enabled, if the CMM is in standby mode, then only port 14, 15 and 16 are enabled, all other ports are disabled to prevent looping inside the chassis.

5.5.2. CMM and Backpack System UART architecture

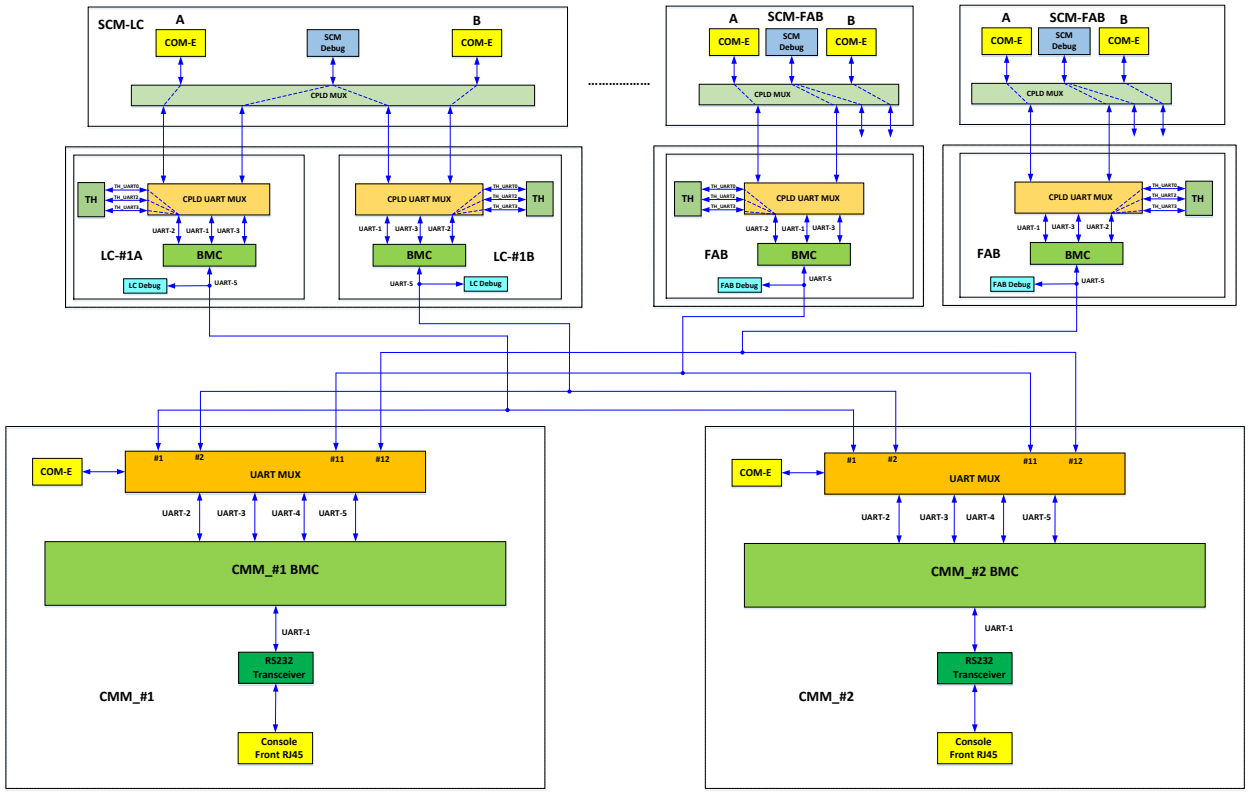

Figure 27: CMM UART architecture

5.5.3. CMM I2C Architecture

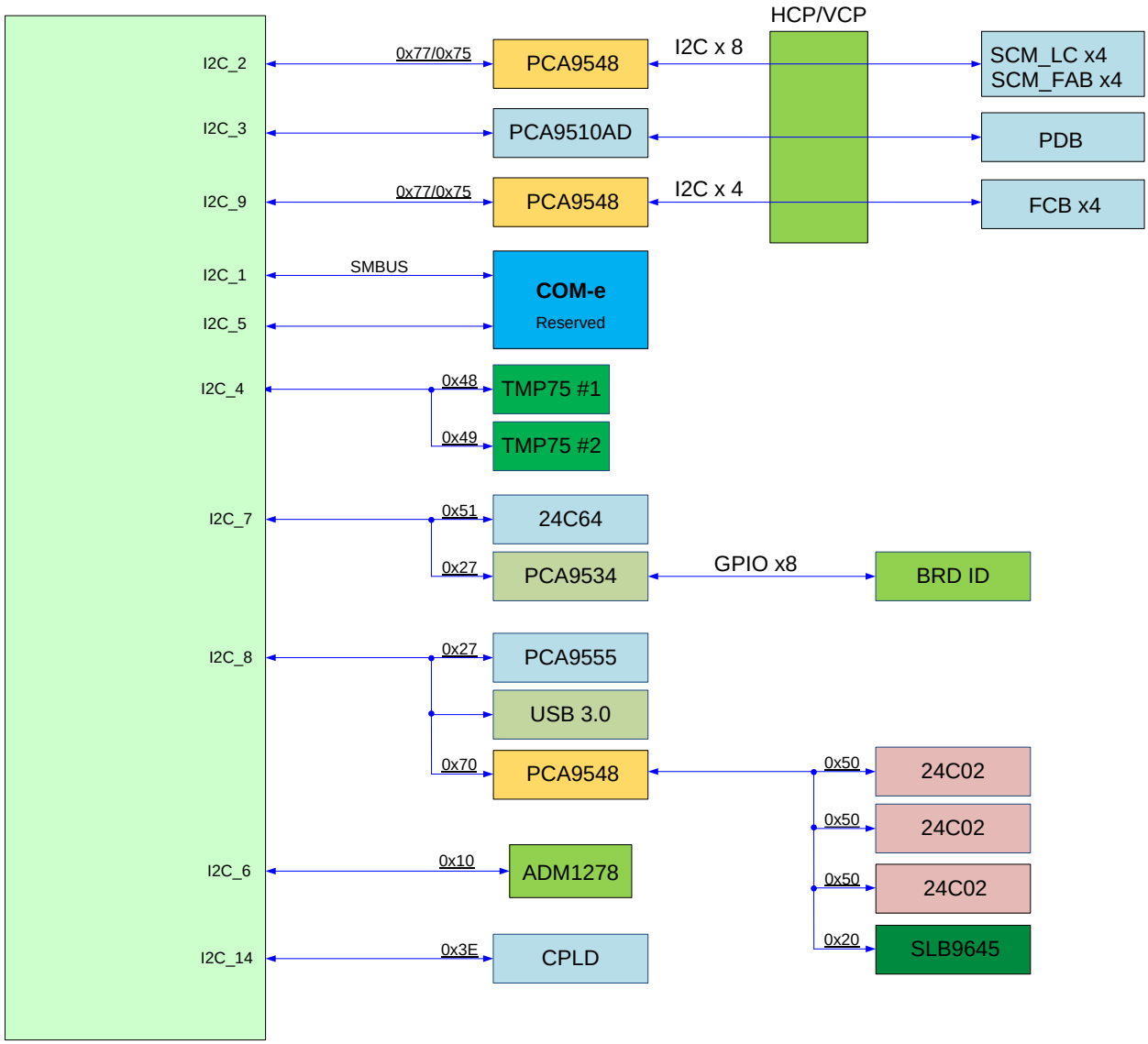

Figure 28: CMM BMC I2C architecture

AST2520 I2C Port	Level 1 Slave Device	Level 2 Slave Device	Note
I2C #1	COM E CPU SMB Bus (Reserved)	NA	CMM COM-e
I2C #2	PCA 9548 Dev Address: 0x75 or 0x77	Channel 0: FAB1 SCM Channel 1: FAB2 SCM Channel 2: LC1 SCM Channel 3: LC2 SCM Channel 4: LC3 SCM Channel 5: LC4 SCM Channel 6: FAB3 SCM Channel 7: FAB4 SCM	I2C bus to LC and FAB
I2C #3	PDB, which has PDU and SIM	Refer to PDB and SIM I2C diagram	
I2C #4	TPM75A, Dev Addr: 0x48	NA	Front
	TPM75A, Dev Addr: 0x49	NA	rear
I2C #5	COM E CPU I2C Bus (Reserved)	NA	CMM COM-e
I2C #6	ADM1278, Addr 0x10	NA	Hot swap
I2C #7	24C64, Dev Address: 0x51	NA	Inventory EE
	PCA9534, Dev Addr: 0x27	NA	BRD ID
I2C #8	PCA9548, Dev Addr: 0x70	Channel 0: 24C02, Dev Addr 0x50 Channel 1: 24C02, Dev Addr 0x50 Channel 2: 24C02, Dev Addr 0x50 Channel 3: reserved Channel 4: SLB9645 TPM Channel 5-7: reserved	
	PCA9555, Dev Addr: 0x27	NA	
	USB3 Debug	NA	FB Debug
I2C #9	PCA9548, Dev Addr: 0x71	Channel 0: FAN Control 1 Channel 1: FAN Control 2 Channel 2: FAN Control 3 Channel 3: FAN Control 4 Channal 4-7: NC	Fan Control Board
I2C #10	NA	NA	
I2C #11	NA	NA	
I2C #12	NA	NA	
I2C #13	NA	NA	
I2C #14	CMM CPLD, Dev Addr: 0x3E	NA	

Table 11: CMM BMC I2C Bus

5.5.4. CMM SYSTEM CPLD Registers

CMM has one CPLD to control the system control function of CMM. The CPLD registers can be accessed by BMC via I2C interface.

CMM CPLD register definition are shown in the following tables.

Register 0x00: BOARD_VERSION – Board Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	4'b1100	MODEL_ID[4:0] 0000: Backpack LC Type-1 0100: Backpack FAB Type-1 1100: Backpack CMM Type-1	MOD_ID
[3:0]	RO	0x0	BRD_REV[3:0]: PCB revision	PCB_VER

Register 0x01: CPLD_VERSION – CPLD Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	0	Reserved	Reserved
[6]	RO	0	Released Bit 0= not released, 1= Released version after PVT	RELEASE_STA
[5:0]	RO	Designed	CPLD Revision[5:0]	CPLD_VER

Register 0x02: CPLD_SUB_VERSION – CPLD Sub Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:0]	RO	0x01	CPLD sub-version, used for HW debug only	CPLD_SUB_VER

Register 0x03: SLOT_ID – Slot ID Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0	Reserved	Reserved
[3:0]	RO	0	Chassis slot information 0000 Slot-1, unused in G4 0001 Slot-2, CMM0 in G4 0010 Slot-3, SCM-FAB1 0011 Slot-4, SCM-FAB2	SLOT_ID[3:0]

			0100 Slot-5, SCM-LC1 0101 Slot-6, SCM-LC2 0110 Slot-7, SCM-LC3 0111 Slot-8, SCM-LC4 1000 Slot-9, SCM-FAB3 1001 Slot-10, SCM-FAB4 1010 Slot-11, CMM1 in G4 1011 Slot-12, unused in G4 1100 Unused ID 1101 Unused ID 1110 Unused ID 1111 Unused ID	

Register 0x06: SYS_LED_CTRL – System LED Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	R/W	0xF	Reserved.	Reserved
[3]	R/W	0b0	LED_BLINK_EN 0: LED No blink 1: LED Blink is ON	LED_BLINK
[2]	R/W	0b0	LED_BLUE 0: LED BLUE is OFF 1: LED BLUE is ON	LED_BLU
[1]	R/W	0b0	LED_GREEN 0: LED GREEN is OFF 1: LED GREEN is ON	LED_GRN
[0]	R/W	0b1	LED_RED 0: LED RED is OFF 1: LED RED is ON	LED_RED

Register 0x08: MODULE_PRESENT – Module Present Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	1b0	FAB4 Present 0:present 1:not present	FAB4_PRESENT
[6]	RO	1b0	FAB3 Present 0:present	FAB3_PRESENT

			1:not present	
[5]	RO	1b0	FAB2 Present 0:present 1:not present	FAB2_PRESENT
[4]	RO	1b0	FAB1 Present 0:present 1:not present	FAB1_PRESENT
[3]	RO	1b0	LC4 Present 0:present 1:not present	LC4_PRESENT
[2]	RO	1b0	LC3 Present 0:present 1:not present	LC3_PRESENT
[1]	RO	1b0	LC2 Present 0:present 1:not present	LC2_PRESENT
[0]	RO	1b0	LC1 Present 0:present 1:not present	LC1_PRESENT

Register 0x09: MODULE_PRESENT1 – Module Present Status Register1				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	1b0	SCM10 Present 0:present 1:not present	SCM10_PRESENT
[6]	RO	1b0	SCM9 Present 0:present 1:not present	SCM9_PRESENT
[5]	RO	1b0	SCM8 Present 0:present 1:not present	SCM8_PRESENT

[4]	RO	1b0	SCM7 Present 0:present 1:not present	SCM7_PRESENT
[3]	RO	1b0	SCM6 Present 0:present 1:not present	SCM6_PRESENT
[2]	RO	1b0	SCM5 Present 0:present 1:not present	SCM5_PRESENT
[1]	RO	1b0	SCM4 Present 0:present 1:not present	SCM4_PRESENT
[0]	RO	1b0	SCM3 Present 0:present 1:not present	SCM3_PRESENT

Register 0x0A: HOT_SWAP_PG_STA – Hot Swap Power Good Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RO	0x7F	Reserved	Reserved
[0]	RO	1b0	The Status of HOTSWAP_PG_INV	HOTSWAP_PG_INV_STA

Register 0x10: COMe_PWR_CTRL – COMe Power Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:3]	RW	0x1F	Reserved.	Reserved
[2]	RW	0b1	PWR_CYC _N Write 0 to this bit will trigger CPLD power cycling the COMe Module, This bit will auto set to 1 after Power Cycle finish.	PWR_CYC _N
[1]	RW	0b1	PWR_COMe_FORCE Control	PWR_COME_FORCE

			When this bit set to 0, the CPLD will force the COMe module power off.	
[0]	RW	0b0	PWR_COME_EN 0: COMe power is OFF 1: COMe power is ON	PWR_COME_EN

Register 0x11: COMe_RST_CTRL – COMe Reset Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RW	0x7F	Reserved.	Reserved
[0]	RW	0x1	COMe_RST_N 0: write 0 to trigger COMe reset 1: normal	COMe_RST_N

Register 0x12: COMe_STA – COMe Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved.	Reserved
[3]	RO	0b0	COMe Module SUS_STAT_N Status	COM_STAT
[2]	RO	0b0	COMe Module SUS_S5_N Status	COM_S5
[1]	RO	0b0	COMe Module SUS_S4_N Status	COM_S4
[0]	RO	0b0	COMe Module SUS_S3_N Status	COM_S3

Register 0x13: COMe_BIOS_DIS_CTRL – COMe BIOS DIS Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:2]	RW	0x3F	Reserved.	Reserved
[1]	RW	0b1	Control COMe BIOS DIS1	COM_BIOS_DIS1

[0]	RW	0b1	Control COMe BIOS DIS0	COM_BIOS_DIS0

Register 0x16: SPI_FLASH_SEL_CTRL – SPI Flash Select Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RW	0x0	Reserved.	Reserved
[0]	RW	0b0	0: SPI Flash Accessed by COMe. 1: SPI Flash Accessed by BMC.	SPI_SEL

Register 0x20: BMC_RST_EN – BMC Reset Enable Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	0b0	Reserved.	Reserved
[6]	RW	0b0	BMC_WDT2_EN	BMC_WDT2_EN
[5]	RW	0b0	BMC_WDT1_EN	BMC_WDT1_EN
[4]	RW	0b0	BMC_RESET4_EN 0: BMC reset 4 request is disabled 1: BMC reset 4 request is enabled	BMC_RST4_EN
[3]	RW	0b0	BMC_RESET3_EN 0: BMC reset 3 request is disabled 1: BMC reset 3 request is enabled	BMC_RST3_EN
[2]	RW	0b0	BMC_RESET2_EN 0: BMC reset 2 request is disabled 1: BMC reset 2 request is enabled	BMC_RST2_EN
[1]	RW	0b0	BMC_RESET1_EN 0: BMC reset 1 request is disabled 1: BMC reset 1 request is enabled	BMC_RST1_EN

[0]	RW	0b0	BMC_MAIN_RESET_N 0: BMC main reset request is disabled 1: BMC main reset request is enabled	BMC_MAIN_REST_EN

Register 0x21: BMC_RST_CTRL – BMC Reset Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RW	0x7F	Reserved.	Reserved
[0]	RW	0x1	CPLD_BMC_RST_N Control 0: write 0 to trigger BMC reset 1: normal	BMC_RST

Before set this register need check register 0x31 & 0x32 configure first.

Register 0x30: UART_MUX_CTRL0 – UART MUX Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:5]	RO	0x0	Reserved.	Reserved
[3:0]	RW	0x0	BMC UART2 connect selection 4'b0000:disconnect all 4'b0001:connect to FC1 BMC UART 4'b0010:connect to FC2 BMC UART 4'b0011:connect to FC3 BMC UART 4'b0100:connect to FC4 BMC UART 4'b0101:connect to LC1A BMC UART 4'b0110:connect to LC2A BMC UART 4'b0111:connect to LC3A BMC UART 4'b1000:connect to LC4A BMC UART 4'b1001:connect to LC1B BMC UART 4'b1010:connect to LC2B BMC UART 4'b1011:connect to LC3B BMC UART 4'b1100:connect to LC4B BMC UART	UART_MUX_CTRL0

			4'b1101:connect to peer BCM UART Others: disconnect all	

Before set this register need check register 0x30 & 0x32 configure first.

Register 0x31: UART_MUX_CTRL1 – UART MUX Control Register1				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved.	Reserved
[3:0]	RW	0x0	BMC UART3 connect selection 4'b0000:disconnect all 4'b0001:connect with FC1 BMC UART 4'b0010:connect with FC2 BMC UART 4'b0011:connect with FC3 BMC UART 4'b0100:connect with FC4 BMC UART 4'b0101:connect with LC1A BMC UART 4'b0110:connect with LC2A BMC UART 4'b0111:connect with LC3A BMC UART 4'b1000:connect with LC4A BMC UART 4'b1001:connect with LC1B BMC UART 4'b1010:connect with LC2B BMC UART 4'b1011:connect with LC3B BMC UART 4'b1100:connect with LC4B BMC UART 4'b1101:connect with peer BCM UART Others: disconnect all	UART_MUX_CTRL1

Before set this register need check register 0x31 & 0x32 configure first.

Register 0x32: UART_MUX_CTRL2 – UART MUX Control Register2				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved.	Reserved
[3:0]	RW	0x0	BMC UART4 connect selection	UART_MUX_CTRL2

			4'b0000:disconnect all 4'b0001:connect with FC1 BMC UART 4'b0010:connect with FC2 BMC UART 4'b0011:connect with FC3 BMC UART 4'b0100:connect with FC4 BMC UART 4'b0101:connect with LC1A BMC UART 4'b0110:connect with LC2A BMC UART 4'b0111:connect with LC3A BMC UART 4'b1000:connect with LC4A BMC UART 4'b1001:connect with LC1B BMC UART 4'b1010:connect with LC2B BMC UART 4'b1011:connect with LC3B BMC UART 4'b1100:connect with LC4B BMC UART 4'b1101:connect with peer BCM UART Others: disconnect all	

Register 0x40: BCM_RST_CTRL – BCM Devices Reset Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RW	0xF	Reserved.	Reserved
[3]	RW	0b1	BCM5396_RST_N Control 0:Reset 1:Normal	BCM5396_RST_N
[2]	RW	0b1	BMCPHY_BCM54616S_RST_N Control 0:Reset 1:Normal	BMCPHY_BCM54616S_RST_N
[1]	RW	0b1	GBEPHY_BCM54616S_RST_N Control 0:Reset 1:Normal	GBEPHY_BCM54616S_RST_N
[0]	RW	0b1	COMPHY_BCM54616S_RST_N Control 0:Reset 1:Normal	COMPHY_BCM54616S_RST_N

Register 0x41: BCM_INT_STA – BCM Devices Interrupt Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:3]	RW	0x1F	Reserved.	Reserved
[2]	RO	0b1	BMC_BCM54616S_INT_N Status 0:Interrupt 1:No Interrupt	BMCPHY_INT
[1]	RO	0b1	GBE_BCM54616S_INT_N Status 0:Interrupt 1:No Interrupt	GBEPHY_INT
[0]	RO	0b1	COM_BCM54616S_INT_N Status 0:Interrupt 1:No Interrupt	COMPHY_INT

Register 0x42: BCM_EEPROM_WP – BCM Config EEPROM WP Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:3]	RW	0x1F	Reserved.	Reserved
[2]	RW	obo	BMC_PHY_EEPROM_WP Control 0:Normal 1:EEPROM Write Protect.	BMCPHY_EEPROM_WP
[1]	RW	obo	GBE_PHY_EEPROM_WP Control 0:Normal 1:EEPROM Write Protect.	GBEPHY_EEPROM_WP
[0]	RW	obo	COM_PHY_EEPROM_WP Control 0:Normal 1:EEPROM Write Protect.	COMPHY_EEPROM_WP

Register 0x43: BCM5396_EEPROM_SEL –Config EEPROM Select Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:2]	RW	0x3F	Reserved.	Reserved
[1:0]	RW	0x0	00:BMC5396 EEPROM select through M/S logic.	BCM5396_EEPROM_SEL

			01:Force select Active EEPROM. 10:Force select Standby EEPROM. 11:Reserved.	

The register will automatically clear after reset code send out.

Register 0x50: ONE_WIRE_RST_TRIG – One Wire Reset Trig Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:0]	R/W	0x00	8'b0: Normal 8'b01000000: Send out LC1 Left device reset code. 8'b01010000: Send out LC1 Right device reset code. 8'b01000001: Send out LC2 Left device reset code. 8'b01010001: Send out LC2 Right device reset code. 8'b01000010: Send out LC3 Left device reset code. 8'b01010010: Send out LC3 Right device reset code. 8'b01000011: Send out LC4 Left device reset code. 8'b01000011: Send out LC4 Right device reset code. 8'b10001000: Send out FC1 device reset code. 8'b10001001: Send out FC2 device reset code. 8'b10001010: Send out FC3 device reset code. 8'b10001011: Send out FC4 device reset code. 8'b11000010: Send out SCM3 Left device reset code. 8'b11010010: Send out SCM3 Right device reset code.	ONE_WIRE_RST_TRIG

			8'b11000011: Send out SCM4 Left device reset code. 8'b11010011: Send out SCM4 Right device reset code. 8'b11000100: Send out SCM5 Left device reset code. 8'b11010100: Send out SCM5 Right device reset code. 8'b11000101: Send out SCM6 Left device reset code. 8'b11010101: Send out SCM6 Right device reset code. 8'b11000110: Send out SCM7 Left device reset code. 8'b11010110: Send out SCM7 Right device reset code. 8'b11000111: Send out SCM8 Left device reset code. 8'b11010111: Send out SCM8 Right device reset code. 8'b11001000: Send out SCM9 Left device reset code. 8'b11011000: Send out SCM9 Right device reset code. 8'b11001001: Send out SCM10 Left device reset code. 8'b11011001: Send out SCM10 Right device reset code. Other:Normal	

Register 0x51: ONE_WIRE_RST_DEV_SEL – One Wire Reset Device Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:0]	RO	0x1	0x1: Reset the I2C devices in LC/FAB/SCM. 0x2: Reset the COMe in SCM and BMC in LC/FAB. Other: Reserved	ONE_WIRE_RST_DEV

Register 0x52: FAN_PDB_RST – Fan & PDB Reset Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:5]	RO	0x7	Reserved	Reservd
[4]	RW	0b1	CPLD_RST_CMM_PDU_N Control 0:Reset 1:Normal	PDU_RST
[3]	RW	0b1	CPLD_RST_CMM_FAN4_N Control 0:Reset 1:Normal	FAN4_RST
[2]	RW	0b1	CPLD_RST_CMM_FAN3_N Control 0:Reset 1:Normal	FAN3_RST
[1]	RW	0b1	CPLD_RST_CMM_FAN2_N Control 0:Reset 1:Normal	FAN2_RST
[0]	Rw	0b1	CPLD_RST_CMM_FAN1_N Control 0:Reset 1:Normal	FAN1_RST

Register 0x53: FAN_PDB_ALERT – Fan & PDB Alert Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:5]	RO	0x7	Reserved	Reservd
[4]	RO	0b1	CPLD_I2C_CMM_PDU_ALRT_N Status 0:Alert 1:No Alert	PDU_ALERT
[3]	RO	0b1	CPLD_I2C_CMM_FAN4_ALRT_N Status 0:Alert 1:No Alert	FAN4_ALERT
[2]	RO	0b1	CPLD_I2C_CMM_FAN3_ALRT_N Status 0:Alert 1:No Alert	FAN3_ALERT
[1]	RO	0b1	CPLD_I2C_CMM_FAN2_ALRT_N Status	FAN2_ALERT

			0:Alert 1:No Alert	
[0]	RO	0b1	CPLD_I2C_CMM_FAN1_ALRT_N Status 0:Alert 1:No Alert	FAN1_ALERT

Register 0x54: I2C_MUX_RST – I2C Mux Reset Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:3]	RO	0x1F	Reserved	Reservd
[2]		0b1	EEPROM_I2C_MUX_RST_N Control 0:Reset 1:Normal	PHY_EEPROM_I2C_MUX_RST
[1]		0b1	PCA9548_FAN_I2C_RST_N Control 0:Reset 1:Normal	FAN_I2C_MUX_RST
[0]		0b1	PCA9548_I2C_RST_N Control 0:Reset 1:Normal	LCFC_I2C_MUX_RST

Register 0x60: MS_STA_CTRL – MS Status and Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:6]	RO	0x3	Reserved	Reservd
[5]	R/W	0b0	Force off to peer CMM 0:No force off request out 1: request peer CMM force off Notes: Only when CMM is Slave this register software can set this bit.	FORCE_OUT
[4]	RO	0b0	Peer CMM force off status 0:no force off request 1:peer CMM request force off	PER_CMM_FORCE
[3]	RO	0b1	Current CMM M/S status 1:this CMM is Slave	CUR_CMM_STA

			0:this CMM is Master	
[2]	RO	ob1	Peer CMM M/S status 1:peer CMM is Slave 0:peer CMM is Master	PER_CMM_STA
[1]	RO	obo	Current CMM present status 0:present 1:not present	CUR_CMM_PRESENT
[0]	RO	obo	Peer CMM present status 0:present 1:not present	PER_CMM_PRESENT

5.6. VCP-HCP-VCP

VCP-HCP-VCP is orthogonal passive backplane of Backpack. It is orthogonal architecture to allow better airflow and provide more flexible control signal connection among LC, FAB, SCM and CMM.

VCP-HCP-VCP has the following control signals:

- PCIe interface between COM-E CPU and Tomahawk switch ASIC
- OOB GbE SGMII interface between SCM and LC/FAB
- Console interface between SCM and LC/FAB
- SPI interface between SCM and LC/FAB
- LPC bus between SCM and LC/FAB
- USB interface between SCM and LC/FAB
- I2C interface between SCM and LC/FAB
- CMM management I2C bus to LC, FAB, FCB, and PDB/PSU
- CMM OOB ethernet interface to LC, FAB
- CMM console UART interface to LC and FAB

The following diagram is a conceptual diagram of VCP-HCP-VCP connection, it only shows the major buses in the VCP-HCP-VCP control plane.

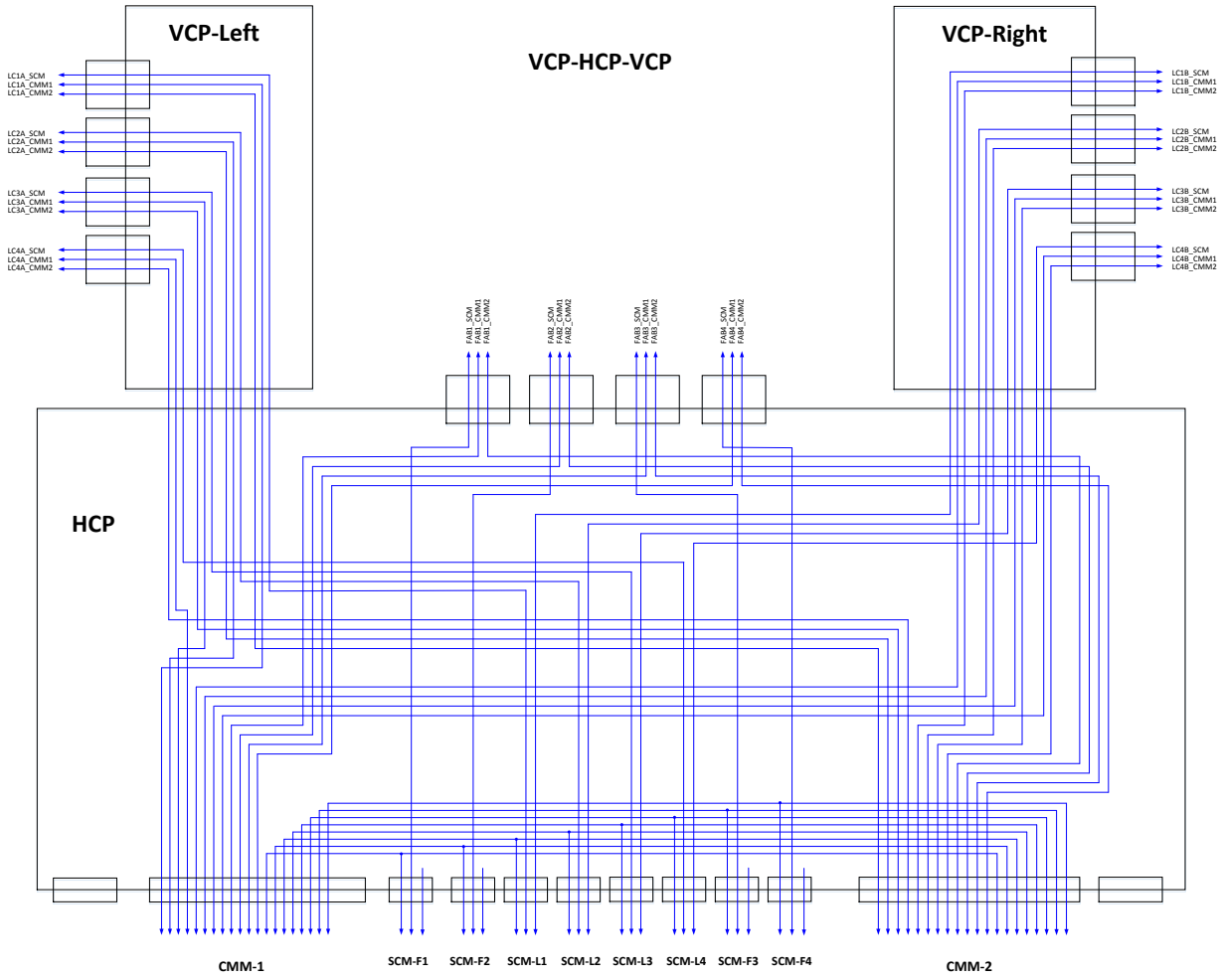

Figure 29: VCP-HCP-VCP connection

5.7. FCB and Fan-tray

Backpack uses 80mm x 80mm x 76mm CR fan to provide forced air cooling to the chassis. Each FAB carries three fan-tray, each fantray has one fan, fan-tray can be hot swappable. There are 12 fan-tray in Backpack chassis because of four FAB card. Each FAB has one fan control board (FCB), FCB has one CPLD used for fan control and fan status monitor. The CMM can access the fan control CPLD via a system management I2C bus.

The following diagram shows the functional blocks of FCB (fan control module):

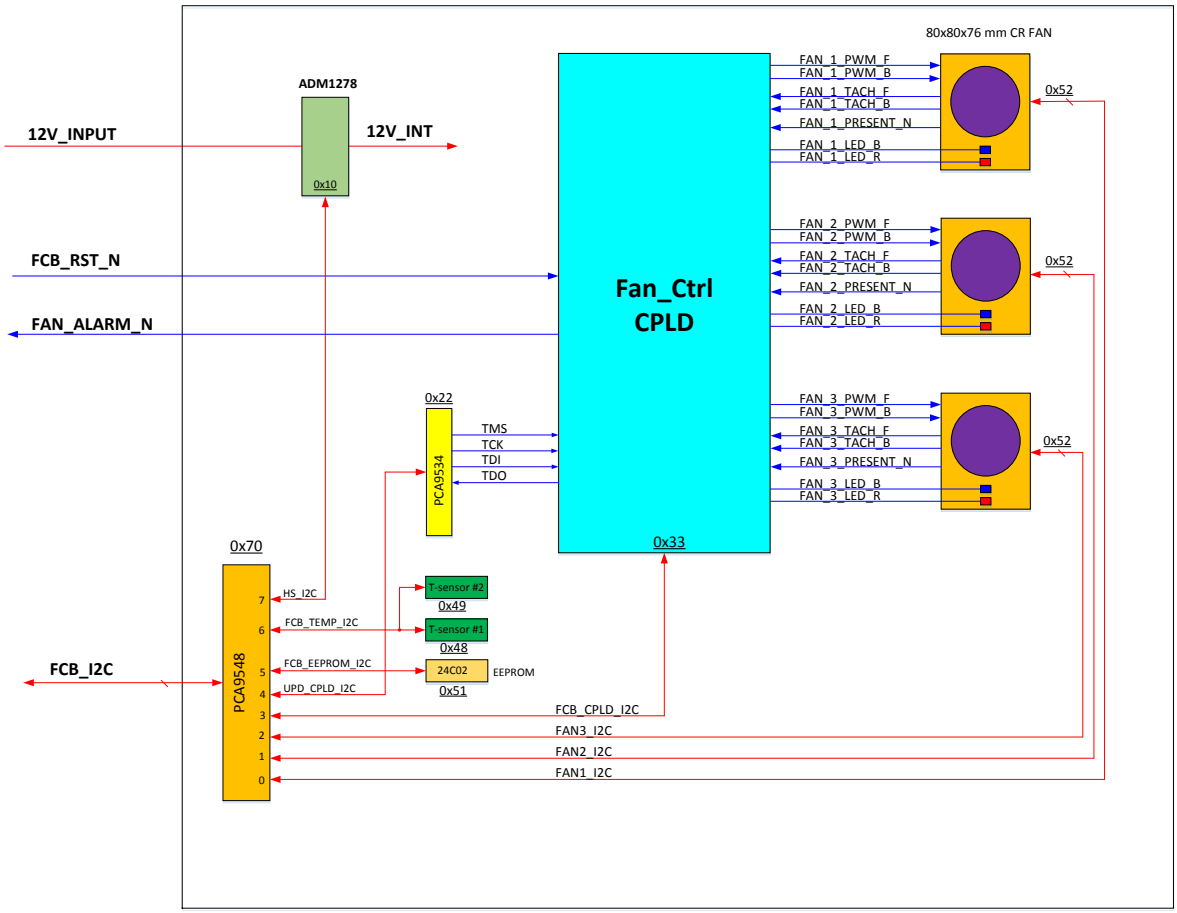

Figure 30: FAN Control Module

The following diagram shows the block diagram fo Fan Board (FB), which locates at the fan-tray and can be hot swappable from the FCB.

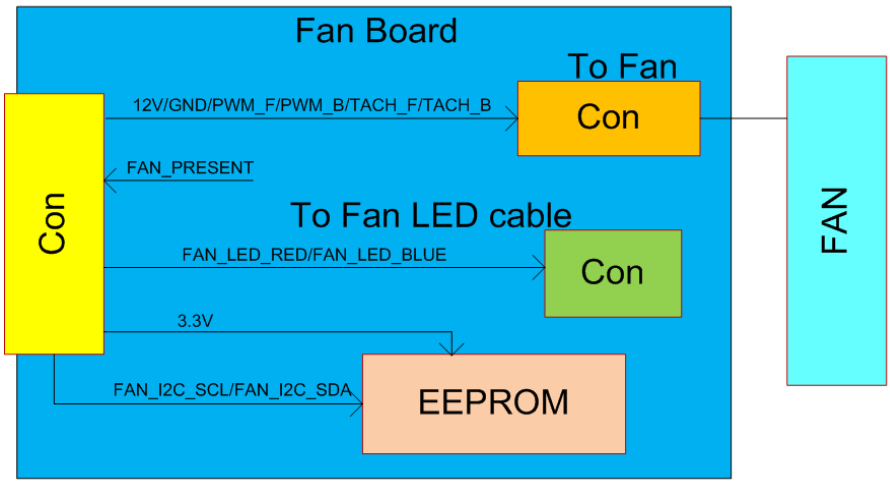

Figure 31: Fan Board (FB) Functional Diagram

5.7.1. Fan Control

Fan control CPLD controls the fan operation. For Backpack fan-tray, the maximal fan speed is about 12000 RPM. Period time is 200 ms, CPLD use

- 200ms/m = 1/2 * TS
- TS = 60/N
- N=60/TS= 60/0.4*m=150*m

SW must multiple 150 and show it as RPM(Revolutions per minute)

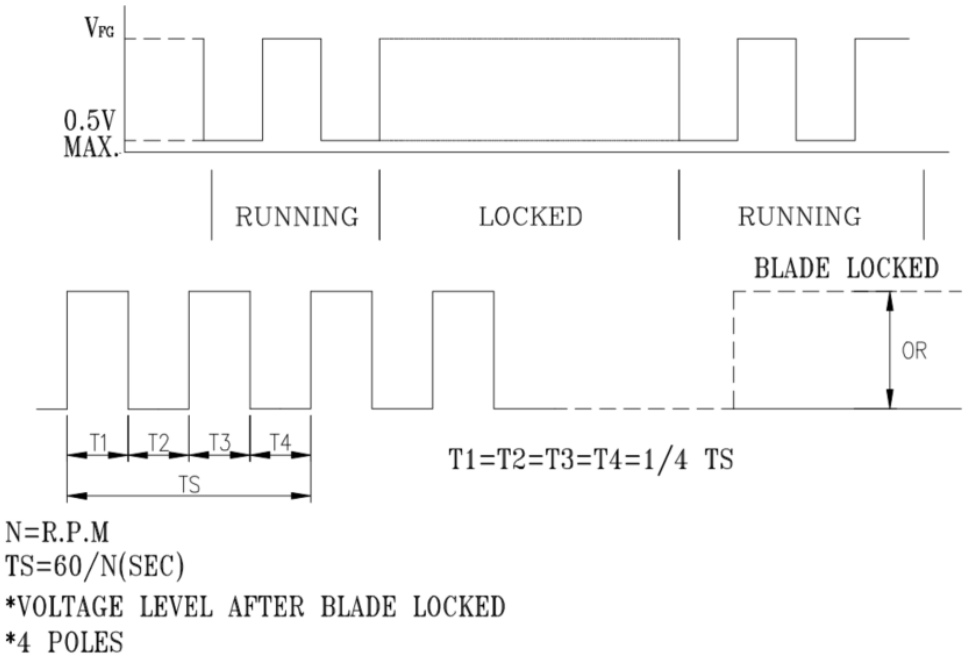

Figure 32: Fan Tachometer Output Waveform

Fan PWM set duty cycle table shown in below table

FAN_PWM[4:0]	
0_0000	0/32 or 0% duty cycle
0_0001	1/32 or 3.125% duty cycle
0_0010	2/32 or 6.25% duty cycle
0_0011	3/32 or 9.375% duty cycle
0_0100	4/32 or 12.5% duty cycle
0_0101	5/32 or 16.625% duty cycle
0_0110	6/32 or 18.725% duty cycle
0_0111	7/32 or 21.875% duty cycle
0_1000	8/32 or 25% duty cycle
0_1001	9/32 or 28.125% duty cycle
0_1010	10/32 or 31.25% duty cycle
0_1011	11/32 or 34.375% duty cycle
0_1100	12/32 or 37.5% duty cycle
0_1101	13/32 or 41.625% duty cycle
0_1110	14/32 or 43.725% duty cycle
0_1111	15/32 or 46.875% duty cycle
1_0000	16/32 or 50% duty cycle
1_0001	17/32 or 53.125% duty cycle
1_0010	18/32 or 56.25% duty cycle
1_0011	19/32 or 59.375% duty cycle
1_0100	20/32 or 62.5% duty cycle
1_0101	21/32 or 66.625% duty cycle
1_0110	22/32 or 68.725% duty cycle
1_0111	23/32 or 71.875% duty cycle
1_1000	24/32 or 75% duty cycle

1_1001	25/32 or 78.125% duty cycle
1_1010	26/32 or 81.25% duty cycle
1_1011	27/32 or 84.375% duty cycle
1_1100	28/32 or 87.5% duty cycle
1_1101	29/32 or 91.625% duty cycle
1_1110	30/32 or 93.725% duty cycle
1_1111	32/32 or 100% duty cycle

Table 12: Backpack Fan Control PWM table

In order to reduce the inrush current after Fan present, CPLD will auto control the Fan PWM value after Fan presented. By default the Fan PWM target value will set to 50%. CPLD will take 8S to increase the PWM duty cycle from 0% to 50%. Every 500mS increase a duty cycle level.

Below figure shows out the Fan present status and the PWM Duty Cycle output status.

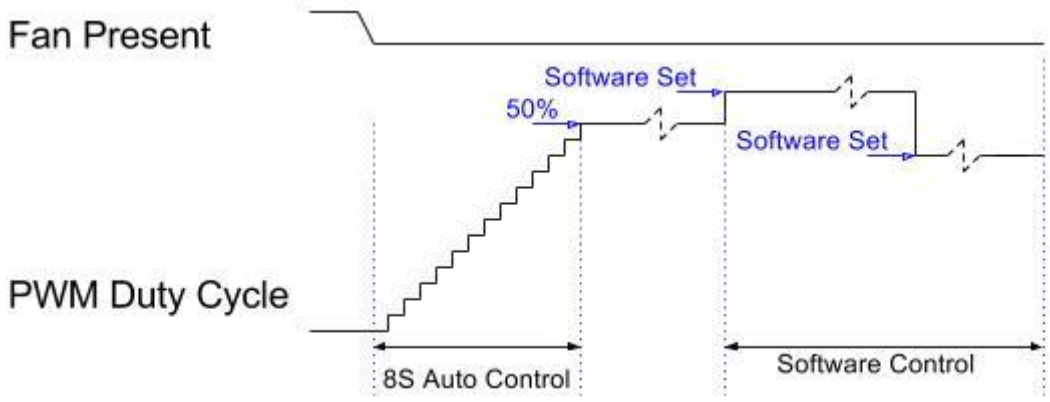

Figure 33: Inrush Current Control

Please refer to Backpack Fan Control Board CPLD Specification for more detail programming information about FCB.

5.7.2. I2C architecture of FCB

There is one I2C Mux PCA9548 on FCB, 8 sub-ports behind this I2C Mux. The following table shows the sub-bus and devices behind the buses.

PCA9548	PCA9548 I2C Mux for FCB	PCA9548 I2C Addr: 0x70	
Sub-bus and devices behind I2C Mux PCA9548			
Sub-Bus Bus	Sub-Bus function	Level 2 Slave Device	Note
I2C #0	FAN Tray #1 I2C Bus	EEPROM I2C Addr : 0x52	Access fan-tray FRU EEPROM content
I2C #1	FAN Tray #2 I2C Bus	EEPROM I2C Addr : 0x52	
I2C #2	FAN Tray #3 I2C Bus	EEPROM I2C Addr : 0x52	
I2C #3	FCB_CPLD_I2C	CPLD I2C Addr: 0x33	
I2C #4	CPLD_UPGRADE_I2C	PCA9534: 0x22	Cpld upgrade
I2C #5	EEPROM I2C	I2C Addr: 0x51	
I2C #6	TMP75 Temperature sensor I2C	TMP75 #1: 0x48	
	TMP75 Temperature sensor I2C	TMP75 #2: 0x49	
I2C #7	ADM1278 hotswap Controller	I2C Addr: 0x10	

Table 13: FCB I2C Devices

The CMM FCB I2C diagram is shown below.

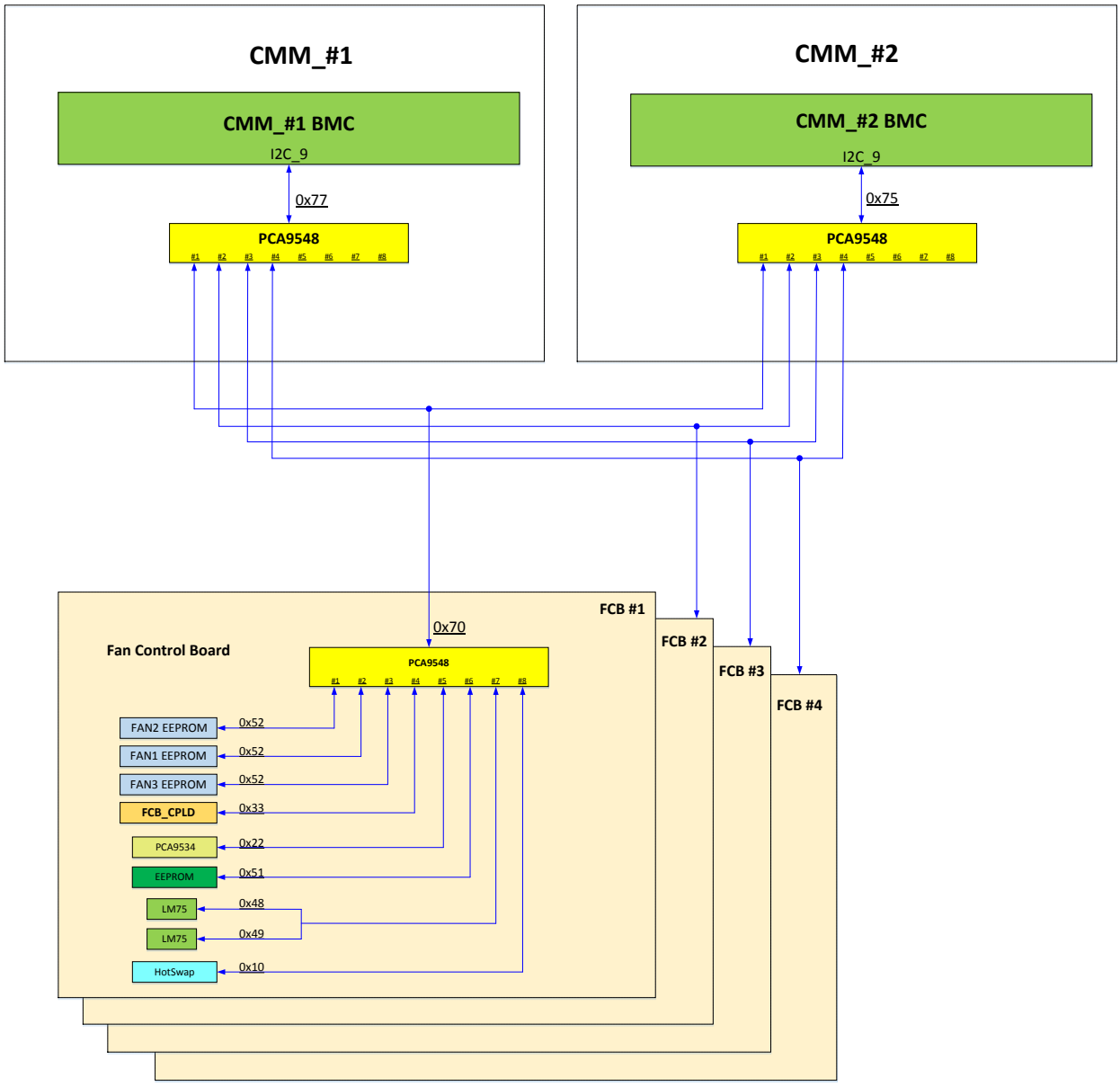

Figure 34: CMM I2C diagram to fan control board

5.7.3. FAN Control CPLD Register Map

FAN Control CPLD can be accssed by active CMM I2C bus 9, please refer to previous section for more details.

Register 0x00: BOARD_VERSION – Board Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved	Reserved
[3:0]	RO	0x0	BRD_REV[3:0]: PCB revision	PCB_VER

Register 0x01: CPLD_VERSION – CPLD Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7]	RO	0	Reserved	Reserved
[6]	RO	0	Released Bit 0= not released, 1= Released version after PVT	RELEASE_STA
[5:0]	RO	Designed	CPLD Revision[5:0]	CPLD_VER

Register 0x02: CPLD_SUB_VERSION – CPLD Sub Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:0]	RO	0x01	CPLD sub-version, HW debug only	CPLD_SUB_VER

Register 0x06: FAN_BLOCK_VERSION – Fan Block Version Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:0]	RO	0x00	Fan block definition version.	FAN_BLK_VER

Register 0x07: FAN_MISC_STA – Fan Misc Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:2]	RO	0x0	Reserved	Reserved
[1]	RO	0b1	Temp sensor 2	TMP2_STA
[0]	RO	0b1	Temp sensor 1	TMP1_STA

Register 0x08: FAN_INT_TRIG_MOD – Fan Interrupt Trig Mode Register

Table 14 – Fan Interrupt Trig Mode Register

Register 0x08: FAN_INT_TRIG_MOD – Fan Interrupt Trig Mode Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:2]	RW	0x0	Reserved	Reserved
[1:0]	RW	0x0	00: FAN interrupt trigger by falling edge 01: FAN interrupt trigger by rising edge 10: FAN interrupt trigger by both falling edge and rising edge 11: FAN interrupt trigger by low level	FAN_INT_TRIG

Register 0x09: FAN_INT_RPT – Fan Interrupt Report Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:3]	RO	0x0	Reserved	Reserved
[2]	RO	0b0	FanTray-3 Interrupt 0: No interrupt 1: Fan3 interrupt is active	FAN3_INT
[1]	RO	0b0	FanTray-2 Interrupt 0: No interrupt 1: Fan2 interrupt is active	FAN2_INT
[0]	RO	0b0	FanTray-1 Interrupt 0: No interrupt 1: Fan1 interrupt is active	FAN1_INT

Register 0x0A: CMM_BMC_HEART_BEAT – CMM BMC Heart Beat Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RO	0x0	Reserved	Reserved
[0]	R/W	0b0	CMM BMC writes this bit to 1 to clear the count in CPLD. If CMM BMC didn't set this bit over 500S. The FANx_PWM_CTRL register will set to default value. FAN will run with 50% RPM. This bit will always read back a 0 value.	CMM_BMC_HEART_BEAT

Register 0x0F: FCB_EEPROM_WP – FCB_EEPROM Write Protect Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RW	0x0	Reserved	Reserved
[0]	RW	0b0	FAN Control Board EERPOM Write Protect 1:Protect 0:Not protect	FCB_EP_WP

The following register definition is the same for all 3 fans in one fan control board.

- Fan1 control register range is 0x20-0x2F
- Fan2 control register range is 0x30-0x3F.
- Fan3 control register range is 0x40-0x4F.

Register 0x20: FAN1_FFAN_SPEED – Fan1 Front Fan Speed Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:0]	RO	0x0	Fan1 Front Fan Speed	FAN1_FFAN_SPEED

Register 0x21: FAN1_RFAN_SPEED – Fan1 Rear Fan Speed Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:0]	RO	0x0	Fan1 Rear Fan Speed	FAN1_RFAN_SPEED

Register 0x22: FAN1_PWM_CTRL – Fan1 PWM Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:5]	RO	0x0	Reserved	Reserved
[4:0]	RW	0x10	FAN1_PWM[4:0] FanTray-1 PWM control signal	FAN1_PWM

Register 0x24: FAN1_LED_CTRL – Fan1 LED Control Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:2]	RW	0x0	Reserved	Reserved
[1:0]	RW	0b00	FAN1_LED_CTRL[1:0] 00: Under HW control 01: Red OFF, Blue ON 10: Red ON, Blue OFF 11: OFF	FAN1_LED_CTRL

			If LED is under HW control Present_n=0, fan_alive_n=0, then Red OFF, Blue ON Present_n=1, fan_alive_n=x, then Red OFF, Blue OFF Present_n=0, fan_alive_n=1, then Red ON, Blue OFF	

Register 0x25: FAN1_EEPROM_WP – Fan1 EEPOM Write Protect Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:1]	RW	0x0	Reserved	Reserved
[0]	RW	0b0	FAN1 EERPOM Write Protect 1:Protect 0:Not protect	FAN1_EP_WP

Register 0x28: FAN1_STA – Fan1 Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RO	0x0	Reserved	Reserved
[3]	RO	0b0	Front Fan1 Alive Status 0: alive 1: bad	FFAN1_ALIVE
[2]	RO	0b0	Rear Fan1 Alive Status 0: alive 1: bad	RFAN1_ALIVE
[1]	RO	0b0	Fan1 Alive Status 0: alive 1: bad	FAN1_ALIVE
[0]	RO	0b0	FanTray-1 Present 0: present 1: not present	FAN1_PRE

Register 0x29: FAN1_INT_MASK – Fan1 Interrupt Mask Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RW	0xF	Reserved	Reserved
[3]	RW	0b1	Front Fan1 Alive Status Interrupt Mask 0: not mask 1: mask	FFAN1_ALIVE_MASK
[2]	RW	0b1	Rear Fan1 Alive Status Interrupt Mask 0: not mask 1: mask	RFAN1_ALIVE_MASK
[1]	RW	0b1	Fan1 Alive Status Interrupt Mask 0: not mask 1: mask	FAN1_ALIVE_MASK
[0]	RW	0b1	FanTray-1 Present Interrupt Mask 0: not mask 1: mask	FAN1_PRE_MASK

Register 0x2A: FAN1_INT_STA – Fan1 Interrupt Status Register				
Bit #	**R/W**	**Default Value**	**Description**	**Name**
[7:4]	RW	0x0	Reserved	Reserved
[3]	WC	0b0	Front Fan1 Alive Status Interrupt Status 0: not interrupt 1: interrupt happened	FFAN1_ALIVE_STA
[2]	WC	0b0	Rear Fan1 Alive Status Interrupt Status 0: not interrupt 1: interrupt happened	RFAN1_ALIVE_STA
[1]	WC	0b0	Fan1 Alive Status Interrupt Status 0: not interrupt 1: interrupt happened	FAN1_ALIVE_STA
[0]	WC	0b0	FanTray-1 Present Interrupt Status 0: not interrupt 1: interrupt happened	FAN1_PRE_STA

5.8. System LED

Backpack chassis and module cards have status LED to display the information of the system.

5.8.1. System Information LED

There are four tri-color system LED on the top left side of the chassis to display information of the system:

- STS: System Status LED
- PSU: PSU status LED
- FAN: Fan LED
- FAB: Fabric Card status

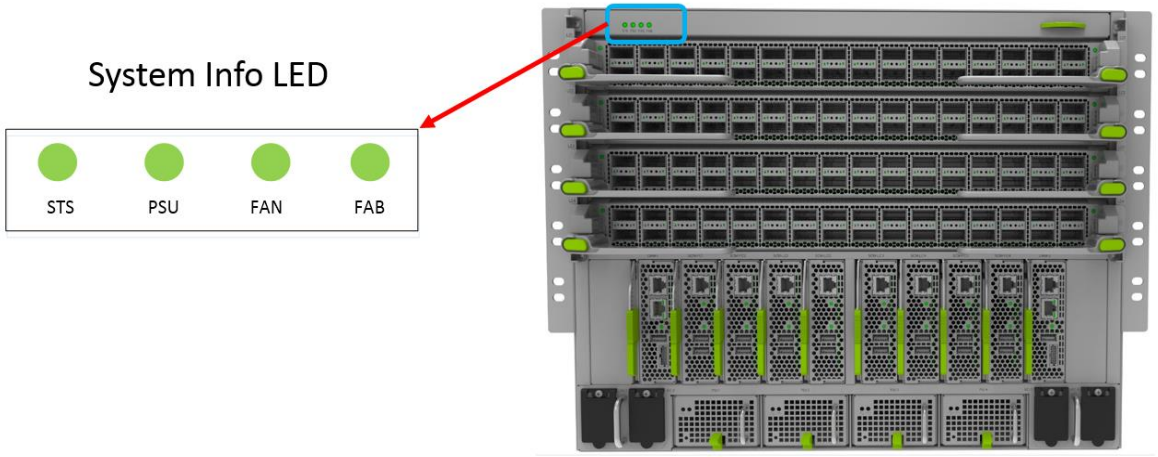

Figure 35: Backpack System LED

The following diagram shows the I2C bus structure for CMM BMC to access SIM(System Information Module). SIM is accessed by CMM I2C Bus 3, via PDB I2C MUX sub-bus 6. SIM has one I2C IO extender PCA9535, each tricolor LED has three bits to control red, green, and blue color, and totally 12 bits are used in the PCA9535. Software should poll the chassis status and control these four LED accordingly to let operation people in front to know the status of the chassis.

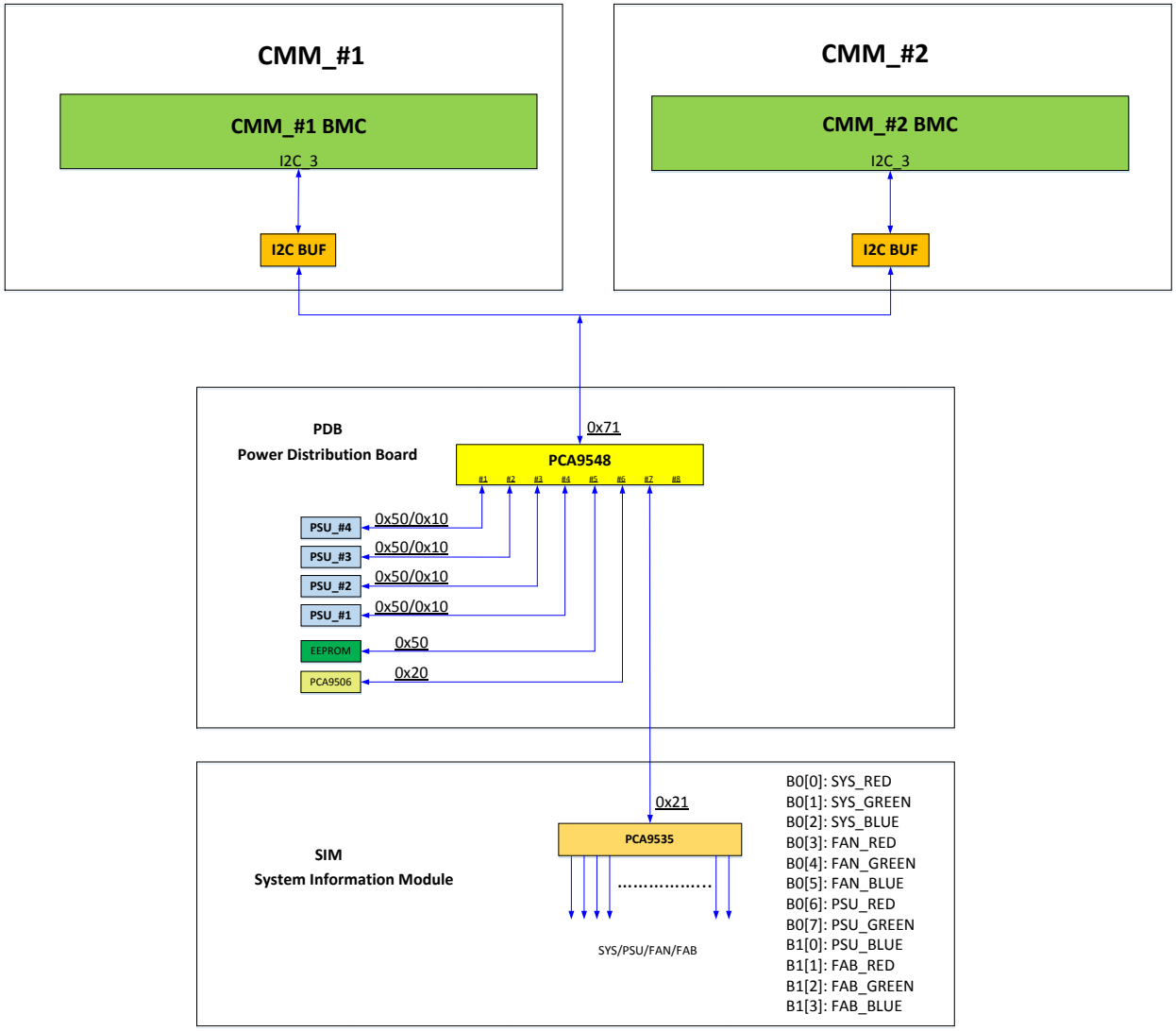

Figure 36: SIM I2C bus topology

The I2C devices of PDB and SIM card are listed in the following table:

CMM PDB and SIM I2C access			
CMM	**BMC I2C Bus #3**	**Bus #3 is used to access PDB and SIM**	
PDB			
PCA9548	PCA9548 I2C Mux for PDB	PCA9548 I2C Addr: 0x71	
Sub-bus and devices behind I2C Mux PCA9548 of PDB			
Sub-Bus	Sub-Bus function	Level 2 Slave Device	Note
I2C #0	PSU #4 I2C Bus	EEPROM I2C Addr : 0x50/0x10	
I2C #1	PSU #3 I2C Bus	EEPROM I2C Addr : 0x50/0x10	
I2C #2	PSU #2 I2C Bus	EEPROM I2C Addr : 0x50/0x10	
I2C #3	PSU #1 I2C Bus	EEPROM I2C Addr : 0x50/0x10	
I2C #4	PDB EEPROM I2C	I2C Addr: 0x50	
I2C #5	PCA9506	I2C Addr: 0x20	PDB card
I2C #6	PCA9535 at SIM card	I2C Addr: 0x21	SIM card
I2C #7	Unused		

Table 15: I2C Devices of PDB and SIM

PDB			
	Bit	Definition	Note
PCA9506	B0[0]	SMB1_ALERT_N	0: PSU #1 has alert active. 1: normal
	B0[1]	SMB2_ALERT_N	0: PSU #2 has alert active. 1: normal
	B0[2]	SMB3_ALERT_N	0: PSU #3 has alert active. 1: normal
	B0[3]	SMB4_ALERT_N	0: PSU #4 has alert active. 1: normal
	B0[4]	PS1_ON_N	Not used
	B0[5]	PS2_ON_N	Not used
	B0[6]	PS3_ON_N	Not used
	B0[7]	PS4_ON_N	Not used
	B1[0]	PSU1_PRSNT_N	0: PSU #1 is present. 1: not present
	B1[1]	PSU2_PRSNT_N	0: PSU #2 is present. 1: not present
	B1[2]	PSU3_PRSNT_N	0: PSU #3 is present. 1: not present
	B1[3]	PSU4_PRSNT_N	0: PSU #4 is present. 1: not present
	B1[4]	IN1_OK_N	0: PSU #1 AC input is OK. 1: AC input is not OK
	B1[5]	IN2_OK_N	0: PSU #2 AC input is OK. 1: AC input is not OK
	B1[6]	IN3_OK_N	0: PSU #3 AC input is OK. 1: AC input is not OK
	B1[7]	IN4_OK_N	0: PSU #4 AC input is OK. 1: AC input is not OK
	B2[0]	PWR1_OK_N	0: PSU #1 output power is OK. 1: output is bad
	B2[1]	PWR2_OK_N	0: PSU #2 output power is OK. 1: output is bad
	B2[2]	PWR3_OK_N	0: PSU #3 output power is OK. 1: output is bad
	B2[3]	PWR4_OK_N	0: PSU #4 output power is OK. 1: output is bad
	B2[4]		Not used
	B2[5]		Not used
	B2[6]		Not used
	B2[7]		Not used
	B3[0]		Not used
	B3[1]		Not used
	B3[2]		Not used
	B3[3]		Not used
	B3[4]		Not used
	B3[5]		Not used
	B3[6]		Not used
	B3[7]		Not used
	B4[0]		Not used
	B4[1]		Not used
	B4[2]	EEPROM_WP	PDB EEPROM write protect 0: Normal. 1: EEPROM write protected
	B4[3]	PSU1_EEPROM_WP	0: Normal. 1: EEPROM write protected
	B4[4]	PSU2_EEPROM_WP	0: Normal. 1: EEPROM write protected
	B4[5]	PSU3_EEPROM_WP	0: Normal. 1: EEPROM write protected
	B4[6]	PSU4_EEPROM_WP	0: Normal. 1: EEPROM write protected
	B4[7]		Not used

Table 16: PDB IO extender bit definition

SIM Card			
	Bit	Definition	Note
PCA9535	B0[0]	SYS_RED	0: SYS LED is read. 1: OFF
	B0[1]	SYS_GREEN	0: SYS LED is green. 1: OFF
	B0[2]	SYS_BLUE	0: SYS LED is blue. 1: OFF
	B0[3]	FAN_RED	0: FAN LED is read. 1: OFF
	B0[4]	FAN_GREEN	0: FAN LED is green. 1: OFF
	B0[5]	FAN_BLUE	0: FAN LED is blue. 1: OFF
	B0[6]	PSU_RED	0: PSU LED is read. 1: OFF
	B0[7]	PSU_GREEN	0: PSU LED is green. 1: OFF
	B1[0]	PSU_BLUE	0: PSU LED is blue. 1: OFF
	B1[1]	FAB_RED	0: FAB LED is read. 1: OFF
	B1[2]	FAB_GREEN	0: FAB LED is green. 1: OFF
	B1[3]	FAB_BLUE	0: FAB LED is blue. 1: OFF
	B1[4]	N/A	
	B1[5]	N/A	
	B1[6]	N/A	
	B1[7]	N/A	

Table 17: SIM IO extender Bit Definition

5.8.2. Line Card LED

LC has two Switch Element (SWE), each SWE has one tri-color status LED(SYS_LED) to display the status of that SWE.

SYSCPLD provide control register to control STS_LED, both LC BMC and SCM-LC can control this SYS_LED, this enable both BMC and COM-e to change the LED status. SYS_LED is Red in default, after LC BMC boot into OS, then software will set the SYS_LED to blue, which is the normal status.

If BMC reboot, STS_LED will blink RED, and after BMC boot into OS, BMC will set STS_LED to constant blue.

LC CPLD register 0x06 is SYS_LED_CTRL register, it is used for software to control LC SYS _LED.

Bit #	R/W	Default Value	Description	Name
[7:4]	R/W	0xF	Reserved.	Reserved
[3]	R/W	0b0	LED_BLINK_EN 0: LED No blink 1: LED Blink is ON	LED_BLINK
[2]	R/W	0b0	LED_BLUE 0: LED BLUE is OFF 1: LED NLUE is ON	LED_BLU
[1]	R/W	0b0	LED_GREEN 0: LED GREEN is OFF 1: LED GREEN is ON	LED_GRN
[0]	R/W	0b1	LED_RED	LED_RED

			0: LED RED is OFF 1: LED RED is ON	

Table 18: LC STS_LED Control Register(0x06)

5.8.3. Fabric Card LED

FAB has one Switch Element (SWE), this SWE has one tri-color status LED(STS_LED) to display the status of the SWE.

SYSCPLD provide control register to control STS_LED, both FAB BMC and SCM-FAB can control this SYS_LED, this enable both BMC and COM-e to change the LED status. SYS_LED is Red in default, after FAB BMC boot into OS, then software will set the SYS_LED to blue, which is the normal working status.

If BMC reboot, SYS_LED will blink RED, and after BMC boot into OS, BMC will set SYS_LED to constant blue.

FAB CPLD register 0x06 is SYS_LED_CTRL register, it is used for software to control FAB System LED.

Bit #	R/W	Default Value	Description	Name
[7:4]	R/W	0xF	Reserved.	Reserved
[3]	R/W	0b0	LED_BLINK_EN 0: LED No blink 1: LED Blink is ON	LED_BLINK
[2]	R/W	0b0	LED_BLUE 0: LED BLUE is OFF 1: LED NLUE is ON	LED_BLU
[1]	R/W	0b0	LED_GREEN 0: LED GREEN is OFF 1: LED GREEN is ON	LED_GRN
[0]	R/W	0b1	LED_RED 0: LED RED is OFF 1: LED RED is ON	LED_RED

Table 19: FAB STS_LED Control Register(0x06)

5.8.4. System Control Module LED

SCM (System Control Module) CPLD controls the LED status from COM-e CPU status:

- LED OFF: COM-e does not get power enable signal
- LED Red: COM-e power is on, but CPU has not entered So status yet
- LED Blue: COM-e power is on and CPU is in So state
- LED Green: BMC force COM-e power off, or paired LC/FAB is unplugged, LED will be green for about 10 seconds, and become OFF.

SCM CPLD register 0x06 is SYS_LED_CTRL register, it is used for software to control SCM System LED.

Bit #	R/W	Default Value	Description	Name
[7:5]	R/W	0xF	Reserved.	Reserved
[4]	R/W	0b0	LED_Control 0: LED controlled by hardware logic 1: LED controlled by Bit[3:0]	LED_TST_EN
[3]	R/W	0b0	LED_BLINK_EN 0: LED No blink 1: LED Blink is ON	LED_BLINK
[2]	R/W	0b0	LED_BLUE 0: LED BLUE is OFF 1: LED NLUE is ON	LED_BLU
[1]	R/W	0b0	LED_GREEN 0: LED GREEN is OFF 1: LED GREEN is ON	LED_GRN
[0]	R/W	0b1	LED_RED 0: LED RED is OFF 1: LED RED is ON	LED_RED

Table 20: SCM System LED Control Register(0x06)

LC or FAB BMC can override the SCM SYS LED status by accessing SCM CPLD register.

5.8.5. Chassis Management Module LED

CMM (Chassis Management Module) has one tri-color status LED(SYS_LED) to display the status of CMM.

CMM SYS LED:

- CMM CPLD provide register to control this LED.
- By default the LED is in RED status.
- After CMM BMC run into normal state, CMM OS will set this LED to Blue.
- BMC reboot will set SYS_LED to blinking RED until BMC fully boot up.

CMM CPLD register 0x3E is SYS_LED_CTRL register, it is used for software to control CMM System LED.

Bit #	R/W	Default Value	Description	Name
[7:4]	R/W	0xF	Reserved.	Reserved
[3]	R/W	0b1	LED_BLINK_EN 0: LED No blink 1: LED Blink is ON	LED_BLINK
[2]	R/W	0b1	LED_BLUE 0: LED BLUE is OFF	LED_BLU

			1: LED NLUE is ON	
[1]	R/W	0b1	LED_GREEN 0: LED GREEN is OFF 1: LED GREEN is ON	LED_GRN
[0]	R/W	0b0	LED_RED 0: LED RED is OFF 1: LED RED is ON	LED_RED

Table 21: CMM System LED Control Register(0x06)

The OOB RJ45 port on CMM front panel also have typical Active LED and Link status LED to indicate the status of OOB Ethernet:

- Link Speed LED, Left of OOB RJ45 port, Green/Amber
  - Solid Green: 1Gbps
  - Solid Amber: 100Mbps
  - OFF: No link/10Mbps
- Activity LED, right of OOB RJ45 port
  - Blinking Green: TX or RX activity
  - OFF: no activity

5.8.6. Chassis PSU LED

Backpack uses BelPower PFE3000 3KW PSU. The PSU has two front LEDs showing its status: LED number one is green and indicates AC power is on or off, whilre LED number two is bi-color: Yellow and green. And indicates DC power presence or fault situations. The following tables lists the different LED status.

Operating condition	**LED Signaling**
AC LED	
AC Line within range	Solid green
AC Line UV condition	OFF
DC LED	
Normal operation	Solid Green
PSON_L	Blinking Yellow (1:1)
V1 or Vsb out of regulation	Solid Yellow
Over temperature shutdown	
Output over voltage shutdown (V1 or VSB)	
Output under voltage shutdown (V1 or VSB)	
Output over current shutdown (V1 or VSB)	
Over temperature warning	Blinking Yellow/Green (2:1)
Minor fan regulation error (>5%, <15%)	Blinking Yellow/Green (1:1)

Table 22: PSU LED Status

6. System Architecture

6.1. Data Plane and Fabric Topology

Backpack uses edge-core topology for its fabric. The switch ASIC is 32 x 100G port Tomahawk ASIC from Broadcom, totally 12 switch ASICs are used in G4 chassis and 24 in the G8 chassis. Each line card has two switch ASIC. There are four fabric cards in G4 and G8 system, for G4, each fabric card has one tomahawk switch ASIC, and for G8 system, each fabric card has two tomahawk switch ASICs.

6.1.1. Switch Element

Backpack uses the Facebook unique switch elements to form the fabric. Each switch element has one BMC, one COM-EXP CPU module and one switch ASIC. This unique switch element architecture makes our data center network disaggregated, easily managed and easy to scale.

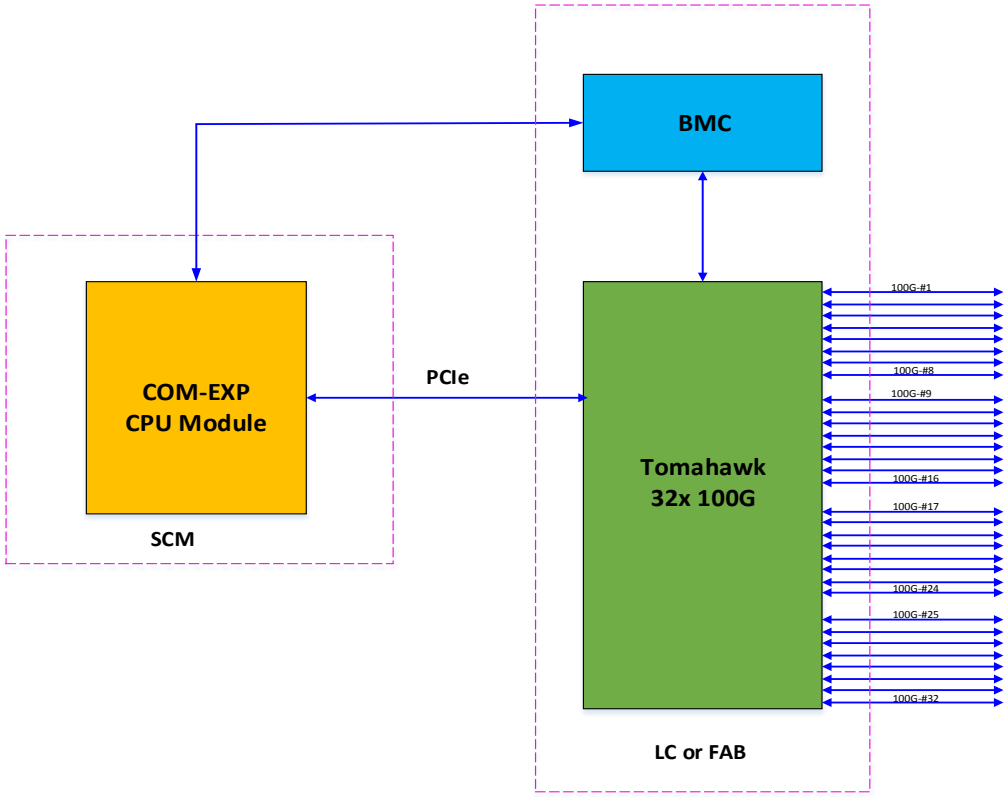

Figure 37: SWE (Switch Element)

6.1.2. Spine-leaf topology

Backpack spine-leaf fabric topology diagram is shown below:

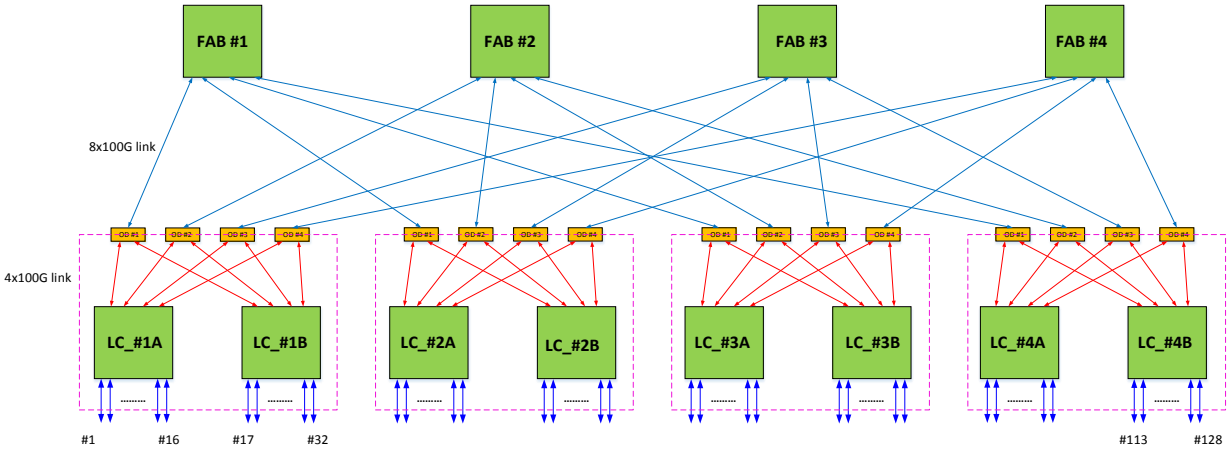

Figure 38: Backpack Data-plane topology

The following table lists the key attributes of Backpack system with spine-leaf topology.

Attributes	G4 Chassis	Notes
Line Cards	4	4 Line card, each line card has two tomahawk, 32x100G to front QSFP28 ports, and 32x100G to four fabric card
Total number of Switch Elements	12	Four LC with 2 tomahawk at each LC, four fabric card with 1 tomahawk at each FAB
SERDES Links/SWE	128	128x25G serdes port, or 32x100G
Fabric Card	4	4 FAB, each FAB has one SWE
Total number of Serdes Link per LC	128	128x25G serdes links to four FAB, each FAB has 32 links
Total number of Serdes Link per FAB	128	128x25G serdes links to four LC, each LC has 32 links
Total # of Links in chassis	512	512x25G links between 4 LC and 4 FAB
Link Speed	25G	Serdes speed is 25Gbps
Total number of QSFP28 ports	128	128 QSFP28 100G ports, each LC has 32 QSFP28 100G ports

Table 23: Backpack System Parameters for spine-leaf topology

6.2. Port mapping between LC and FAB for CLOS topology

In Backpack system, four LC and four FAB are connected orthogonally, the logic connection is shown below:

6.2.1. LC-1 port mapping to Fabric Cards

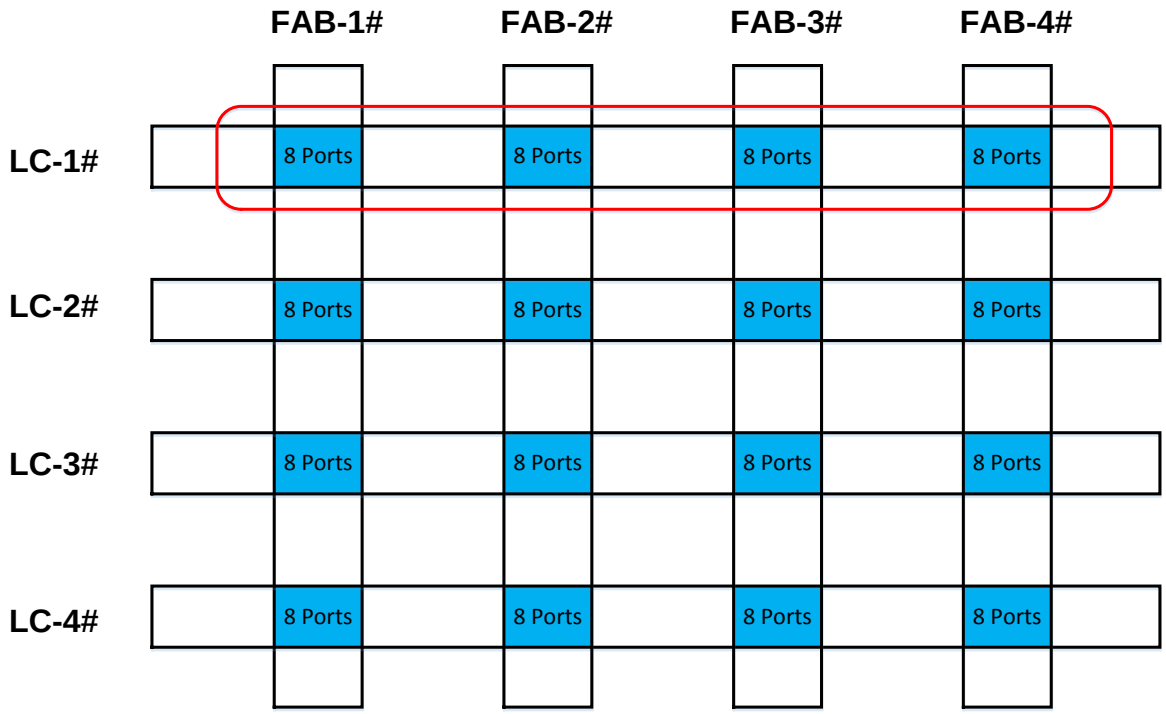

Figure 39: LC-1 Orthogonal Connection to FAB

	SDK Port No.	FC	TD Ln	RD Ln	TD P/N swap	RD P/N swap	Note	SDK Port No.	FC	TD Ln	RD Ln	TD P/N swap	RD P/N swap	Note
Tomahawk 1	CE16	FC16	3	0	N	N	To FAB 1#	CE0	FC17	0	3	Y	N	To LC 1#
			2	1	N	N				1	2	Y	N	
			1	2	N	N				2	1	Y	N	
			0	3	N	N				3	0	Y	N	
	CE17	FC17	0	3	N	Y		CE1	FC18	0	3	Y	N	
			1	2	N	Y				1	2	Y	N	
			2	1	N	Y				2	1	Y	N	
			3	0	N	Y				3	0	Y	N	
	CE18	FC18	0	3	Y	N		CE2	FC16	3	0	N	N	
			1	2	Y	N				2	1	N	N	
			2	1	Y	N				1	2	N	N	
			3	0	Y	N				0	3	N	N	
	CE19	FC19	2	3	N	Y		CE3	FC19	2	2	N	Y	
			1	0	N	Y				0	0	N	Y	
			0	1	N	Y				3	3	N	Y	
			3	2	Y	N				1	1	N	Y	
Tomahawk 2	CE16	FC16	3	3	Y	N		CE4	FC15	0	2	Y	N	
			0	2	N	N				1	0	Y	N	

			2	0	N	N				3	3	Y	N	
			1	1	N	N				2	1	Y	N	
	CE17	FC17	0	3	N	N		CE5	FC14	3	0	Y	N	
			1	2	N	N				2	1	Y	N	
			2	1	N	N				1	2	Y	N	
			3	0	N	N				0	3	Y	N	
	CE18	FC18	0	3	Y	Y		CE6	FC13	3	0	Y	N	
			1	2	Y	Y				2	1	Y	N	
			2	1	Y	Y				1	2	Y	N	
			3	0	Y	Y				0	3	Y	N	
	CE19	FC19	2	3	N	N		CE7	FC12	3	0	Y	N	
			0	1	N	N				2	1	Y	N	
			1	0	N	N				1	2	Y	N	
			3	2	N	N				0	3	Y	N	
Tomahawk 1	CE20	FC12	0	3	N	Y	To FAB 2#	CE0	FC17	0	3	Y	N	To LC 1#
			1	2	N	Y				1	2	Y	N	
			2	1	N	Y				2	1	Y	N	
			3	0	N	Y				3	0	Y	N	
	CE21	FC13	0	3	N	Y		CE1	FC18	0	3	Y	N	
			1	2	N	Y				1	2	Y	N	
			2	1	N	Y				2	1	Y	N	
			3	0	N	Y				3	0	Y	N	
	CE22	FC14	0	3	Y	Y		CE2	FC16	3	0	N	N	
			1	2	Y	Y				2	1	N	N	
			2	1	Y	Y				1	2	N	N	
			3	0	Y	Y				0	3	N	N	
	CE23	FC15	0	3	N	Y		CE3	FC19	2	2	N	Y	
			2	1	N	Y				0	0	N	Y	
			1	2	N	Y				3	3	N	Y	
			3	0	Y	N				1	1	N	Y	
Tomahawk 2	CE20	FC12	0	0	Y	Y		CE4	FC15	0	2	Y	N	
			3	1	N	Y				1	0	Y	N	
			1	3	N	Y				3	3	Y	N	
			2	2	N	Y				2	1	Y	N	
	CE21	FC13	0	3	N	N		CE5	FC14	3	0	Y	N	
			1	2	N	N				2	1	Y	N	
			2	1	N	N				1	2	Y	N	
			3	0	N	N				0	3	Y	N	
	CE22	FC14	0	3	Y	N		CE6	FC13	3	0	Y	N	
			1	2	Y	N				2	1	Y	N	
			2	1	Y	N				1	2	Y	N	
			3	0	Y	N				0	3	Y	N	
	CE23	FC15	0	3	N	N		CE7	FC12	3	0	Y	N	
			1	2	N	N				2	1	Y	N	

			2	1	N	N				1	2	Y	N	
			3	0	N	N				0	3	Y	N	
Tomahawk 1	CE24	FC8	3	3	Y	N	To FAB 3#	CE0	FC17	0	3	Y	N	To LC 1#
			2	2	Y	N				1	2	Y	N	
			1	1	Y	N				2	1	Y	N	
			0	0	Y	N				3	0	Y	N	
	CE25	FC9	0	0	N	Y		CE1	FC18	0	3	Y	N	
			1	1	N	Y				1	2	Y	N	
			2	2	N	Y				2	1	Y	N	
			3	3	N	Y				3	0	Y	N	
	CE26	FC10	3	3	N	Y		CE2	FC16	3	0	N	N	
			2	2	N	Y				2	1	N	N	
			1	1	N	Y				1	2	N	N	
			0	0	N	Y				0	3	N	N	
	CE27	FC11	0	0	Y	N		CE3	FC19	2	2	N	Y	
			2	2	Y	N				0	0	N	Y	
			1	1	Y	N				3	3	N	Y	
			3	3	N	Y				1	1	N	Y	
Tomahawk 2	CE24	FC8	3	0	N	N		CE4	FC15	0	2	Y	N	
			0	1	Y	N				1	0	Y	N	
			2	3	Y	N				3	3	Y	N	
			1	2	Y	N				2	1	Y	N	
	CE25	FC9	0	0	N	N		CE5	FC14	3	0	Y	N	
			1	1	N	N				2	1	Y	N	
			2	2	N	N				1	2	Y	N	
			3	3	N	N				0	3	Y	N	
	CE26	FC10	3	3	N	Y		CE6	FC13	3	0	Y	N	
			2	2	N	Y				2	1	Y	N	
			1	1	N	Y				1	2	Y	N	
			0	0	N	Y				0	3	Y	N	
	CE27	FC11	0	0	Y	Y		CE7	FC12	3	0	Y	N	
			1	1	Y	Y				2	1	Y	N	
			2	2	Y	Y				1	2	Y	N	
			3	3	Y	Y				0	3	Y	N	
Tomahawk 1	CE28	FC4	3	3	Y	N	To FAB 4#	CE0	FC17	0	3	Y	N	To LC 1#
			2	2	Y	N				1	2	Y	N	
			1	1	Y	N				2	1	Y	N	
			0	0	Y	N				3	0	Y	N	
	CE29	FC5	0	0	N	Y		CE1	FC18	0	3	Y	N	
			1	1	N	Y				1	2	Y	N	
			2	2	N	Y				2	1	Y	N	
			3	3	N	Y				3	0	Y	N	
	CE30	FC6	3	3	N	N		CE2	FC16	3	0	N	N	
			2	2	N	N				2	1	N	N	
			1	1	N	N				1	2	N	N	

			0	0	N	N				0	3	N	N	
	CE31	FC7	0	0	N	N		CE3	FC19	2	2	N	Y	
			2	2	N	N				0	0	N	Y	
			1	1	N	N				3	3	N	Y	
			3	3	Y	Y				1	1	N	Y	
Tomahawk 2	CE28	FC4	3	0	N	N		CE4	FC15	0	2	Y	N	
			0	1	Y	N				1	0	Y	N	
			2	3	Y	N				3	3	Y	N	
			1	2	Y	N				2	1	Y	N	
	CE29	FC5	0	0	N	N		CE5	FC14	3	0	Y	N	
			1	1	N	N				2	1	Y	N	
			2	2	N	N				1	2	Y	N	
			3	3	N	N				0	3	Y	N	
	CE30	FC6	3	3	N	Y		CE6	FC13	3	0	Y	N	
			2	2	N	Y				2	1	Y	N	
			1	1	N	Y				1	2	Y	N	
			0	0	N	Y				0	3	Y	N	
	CE31	FC7	0	0	N	Y		CE7	FC12	3	0	Y	N	
			1	1	N	Y				2	1	Y	N	
			2	2	N	Y				1	2	Y	N	
			3	3	N	Y				0	3	Y	N	

Table 24: LC-1 port mapping to FAB

6.2.2. LC-2 port mapping to Fabric Cards

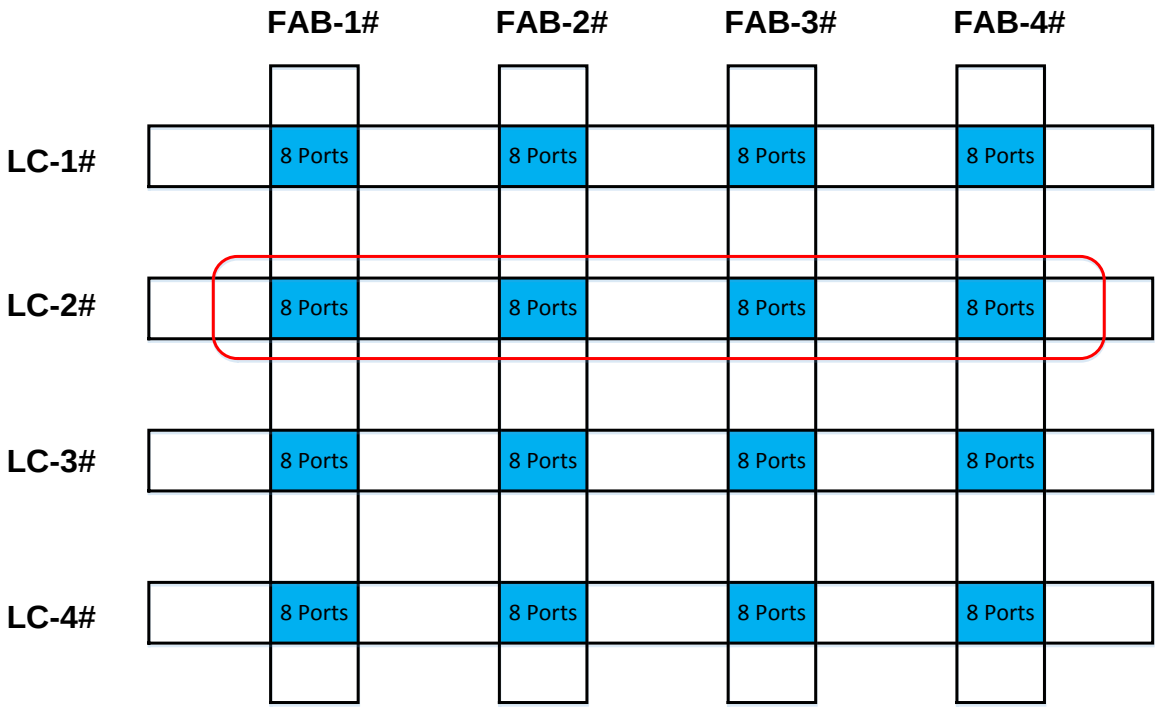

Figure 40: LC-2 Orthogonal Connection to FAB

	SDK Port No.	FC	TD Ln	RD Ln	TD P/N swap	RD P/N swap	Note	SDK Port No.	FC	TD Ln	RD Ln	TD P/N swap	RD P/N swap	Note
Tomahawk 1	CE16	FC16	3	0	N	N	To FAB 1#	CE8	FC26	0	1	Y	N	To LC 2#
			2	1	N	N				1	0	Y	N	
			1	2	N	N				2	3	Y	N	
			0	3	N	N				3	2	Y	N	
	CE17	FC17	0	3	N	Y		CE9	FC25	3	2	N	Y	
			1	2	N	Y				2	3	N	Y	
			2	1	N	Y				1	0	N	Y	
			3	0	N	Y				0	1	N	Y	
	CE18	FC18	0	3	Y	N		CE10	FC24	0	1	Y	N	
			1	2	Y	N				1	0	Y	N	
			2	1	Y	N				2	3	Y	N	

			3	0	Y	N				3	2	Y	N	
	CE19	FC19	2	3	N	Y		CE11	FC27	3	3	N	Y	
			1	0	N	Y				2	1	N	Y	
			0	1	N	Y				1	2	N	Y	
			3	2	Y	N				0	0	N	Y	
Tomahawk 2	CE16	FC16	3	3	Y	N		CE12	FC23	3	3	N	N	
			0	2	N	N				2	1	N	N	
			2	0	N	N				0	2	N	N	
			1	1	N	N				1	0	N	N	
	CE17	FC17	0	3	N	N		CE13	FC22	3	2	Y	Y	
			1	2	N	N				2	3	Y	Y	
			2	1	N	N				1	0	Y	Y	
			3	0	N	N				0	1	Y	Y	
	CE18	FC18	0	3	Y	Y		CE14	FC20	3	2	Y	N	
			1	2	Y	Y				2	3	Y	N	
			2	1	Y	Y				1	0	Y	N	
			3	0	Y	Y				0	1	Y	N	
	CE19	FC19	2	3	N	N		CE15	FC21	0	1	N	Y	
			0	1	N	N				1	0	N	Y	
			1	0	N	N				2	3	N	Y	
			3	2	N	N				3	2	N	Y	
Tomahawk 1	CE20	FC12	0	3	N	Y	To FAB 2#	CE8	FC26	0	1	Y	N	To LC 2#
			1	2	N	Y				1	0	Y	N	
			2	1	N	Y				2	3	Y	N	
			3	0	N	Y				3	2	Y	N	
	CE21	FC13	0	3	N	Y		CE9	FC25	3	2	N	Y	
			1	2	N	Y				2	3	N	Y	
			2	1	N	Y				1	0	N	Y	
			3	0	N	Y				0	1	N	Y	
	CE22	FC14	0	3	Y	Y		CE10	FC24	0	1	Y	N	
			1	2	Y	Y				1	0	Y	N	
			2	1	Y	Y				2	3	Y	N	
			3	0	Y	Y				3	2	Y	N	
	CE23	FC15	0	3	N	Y		CE11	FC27	3	3	N	Y	
			2	1	N	Y				2	1	N	Y	
			1	2	N	Y				1	2	N	Y	
			3	0	Y	N				0	0	N	Y	
Tomahawk 2	CE20	FC12	0	0	Y	Y		CE12	FC23	3	3	N	N	
			3	1	N	Y				2	1	N	N	
			1	3	N	Y				0	2	N	N	
			2	2	N	Y				1	0	N	N	
	CE21	FC13	0	3	N	N		CE13	FC22	3	2	Y	Y	
			1	2	N	N				2	3	Y	Y	
			2	1	N	N				1	0	Y	Y	

			3	0	N	N				0	1	Y	Y	
	CE22	FC14	0	3	Y	N		CE14	FC20	3	2	Y	N	
			1	2	Y	N				2	3	Y	N	
			2	1	Y	N				1	0	Y	N	
			3	0	Y	N				0	1	Y	N	
	CE23	FC15	0	3	N	N		CE15	FC21	0	1	N	Y	
			1	2	N	N				1	0	N	Y	
			2	1	N	N				2	3	N	Y	
			3	0	N	N				3	2	N	Y	
Tomahawk 1	CE24	FC8	3	3	Y	N	To FAB 3#	CE8	FC26	0	1	Y	N	To LC 2#
			2	2	Y	N				1	0	Y	N	
			1	1	Y	N				2	3	Y	N	
			0	0	Y	N				3	2	Y	N	
	CE25	FC9	0	0	N	Y		CE9	FC25	3	2	N	Y	
			1	1	N	Y				2	3	N	Y	
			2	2	N	Y				1	0	N	Y	
			3	3	N	Y				0	1	N	Y	
	CE26	FC10	3	3	N	Y		CE10	FC24	0	1	Y	N	
			2	2	N	Y				1	0	Y	N	
			1	1	N	Y				2	3	Y	N	
			0	0	N	Y				3	2	Y	N	
	CE27	FC11	0	0	Y	N		CE11	FC27	3	3	N	Y	
			2	2	Y	N				2	1	N	Y	
			1	1	Y	N				1	2	N	Y	
			3	3	N	Y				0	0	N	Y	
Tomahawk 2	CE24	FC8	3	0	N	N		CE12	FC23	3	3	N	N	
			0	1	Y	N				2	1	N	N	
			2	3	Y	N				0	2	N	N	
			1	2	Y	N				1	0	N	N	
	CE25	FC9	0	0	N	N		CE13	FC22	3	2	Y	Y	
			1	1	N	N				2	3	Y	Y	
			2	2	N	N				1	0	Y	Y	
			3	3	N	N				0	1	Y	Y	
	CE26	FC10	3	3	N	Y		CE14	FC20	3	2	Y	N	
			2	2	N	Y				2	3	Y	N	
			1	1	N	Y				1	0	Y	N	
			0	0	N	Y				0	1	Y	N	
	CE27	FC11	0	0	Y	Y		CE15	FC21	0	1	N	Y	
			1	1	Y	Y				1	0	N	Y	
			2	2	Y	Y				2	3	N	Y	
			3	3	Y	Y				3	2	N	Y	
Tomahawk 1	CE28	FC4	3	3	Y	N	To FAB 4#	CE8	FC26	0	1	Y	N	To LC 2#
			2	2	Y	N				1	0	Y	N	
			1	1	Y	N				2	3	Y	N	
			0	0	Y	N				3	2	Y	N	

	CE29	FC5	0	0	N	Y		CE9	FC25	3	2	N	Y	
			1	1	N	Y				2	3	N	Y	
			2	2	N	Y				1	0	N	Y	
			3	3	N	Y				0	1	N	Y	
	CE30	FC6	3	3	N	N		CE10	FC24	0	1	Y	N	
			2	2	N	N				1	0	Y	N	
			1	1	N	N				2	3	Y	N	
			0	0	N	N				3	2	Y	N	
	CE31	FC7	0	0	N	N		CE11	FC27	3	3	N	Y	
			2	2	N	N				2	1	N	Y	
			1	1	N	N				1	2	N	Y	
			3	3	Y	Y				0	0	N	Y	
Tomahawk 2	CE28	FC4	3	0	N	N		CE12	FC23	3	3	N	N	
			0	1	Y	N				2	1	N	N	
			2	3	Y	N				0	2	N	N	
			1	2	Y	N				1	0	N	N	
	CE29	FC5	0	0	N	N		CE13	FC22	3	2	Y	Y	
			1	1	N	N				2	3	Y	Y	
			2	2	N	N				1	0	Y	Y	
			3	3	N	N				0	1	Y	Y	
	CE30	FC6	3	3	N	Y		CE14	FC20	3	2	Y	N	
			2	2	N	Y				2	3	Y	N	
			1	1	N	Y				1	0	Y	N	
			0	0	N	Y				0	1	Y	N	
	CE31	FC7	0	0	N	Y		CE15	FC21	0	1	N	Y	
			1	1	N	Y				1	0	N	Y	
			2	2	N	Y				2	3	N	Y	
			3	3	N	Y				3	2	N	Y	

Table 25: LC-2 Port Mapping to FAB

6.2.3. LC-3 port mapping to Fabric Cards

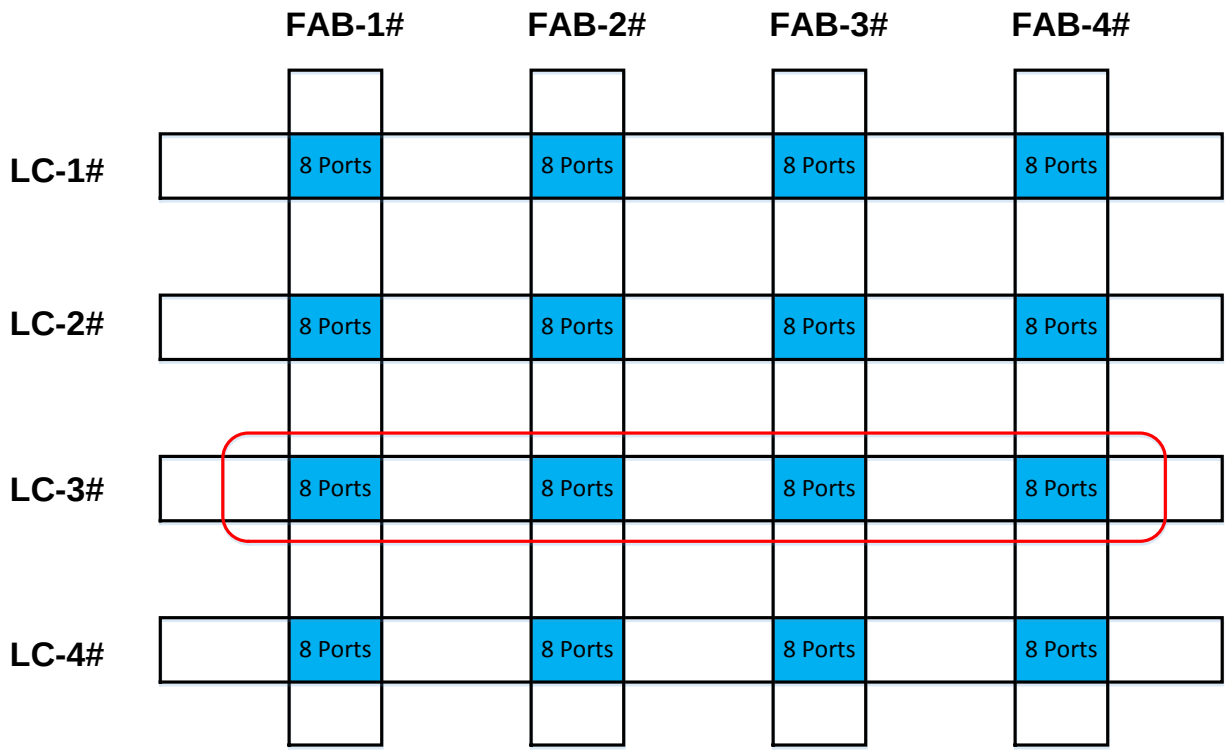

Figure 41: LC-3 Orthogonal Connection to FAB

	SDK Port No.	FC	TD Ln	RD Ln	TD P/N swap	RD P/N swap	Note	SDK Port No.	FC	TD Ln	RD Ln	TD P/N swap	RD P/N swap	Note
Tomahawk 1	CE16	FC16	3	0	N	N	To FAB 1#	CE16	FC1	3	0	Y	N	To LC 3#
			2	1	N	N				2	1	Y	N	
			1	2	N	N				1	2	Y	N	
			0	3	N	N				0	3	Y	N	
	CE17	FC17	0	3	N	Y		CE17	FC2	3	0	Y	N	
			1	2	N	Y				2	1	Y	N	
			2	1	N	Y				1	2	Y	N	
			3	0	N	Y				0	3	Y	N	
	CE18	FC18	0	3	Y	N		CE18	FC0	3	0	Y	Y	
			1	2	Y	N				2	1	Y	Y	
			2	1	Y	N				1	2	Y	Y	
			3	0	Y	N				0	3	Y	Y	

	CE19	FC19	2	3	N	Y		CE19	FC3	2	0	Y	N	
			1	0	N	Y				0	2	Y	N	
			0	1	N	Y				3	1	Y	N	
			3	2	Y	N				1	3	Y	N	
Tomahawk 2	CE16	FC16	3	3	Y	N		CE20	FC31	0	1	Y	N	
			0	2	N	N				1	0	Y	N	
			2	0	N	N				3	3	Y	N	
			1	1	N	N				2	2	Y	N	
	CE17	FC17	0	3	N	N		CE21	FC28	3	2	Y	N	
			1	2	N	N				2	3	Y	N	
			2	1	N	N				1	0	Y	N	
			3	0	N	N				0	1	Y	N	
	CE18	FC18	0	3	Y	Y		CE22	FC29	0	3	Y	N	
			1	2	Y	Y				1	2	Y	N	
			2	1	Y	Y				2	1	Y	N	
			3	0	Y	Y				3	0	Y	N	
	CE19	FC19	2	3	N	N		CE23	FC30	0	3	Y	N	
			0	1	N	N				1	2	Y	N	
			1	0	N	N				2	1	Y	N	
			3	2	N	N				3	0	Y	N	
Tomahawk 1	CE20	FC12	0	3	N	Y	To FAB 2#	CE16	FC1	3	0	Y	N	To LC 3#
			1	2	N	Y				2	1	Y	N	
			2	1	N	Y				1	2	Y	N	
			3	0	N	Y				0	3	Y	N	
	CE21	FC13	0	3	N	Y		CE17	FC2	3	0	Y	N	
			1	2	N	Y				2	1	Y	N	
			2	1	N	Y				1	2	Y	N	
			3	0	N	Y				0	3	Y	N	
	CE22	FC14	0	3	Y	Y		CE18	FC0	3	0	Y	Y	
			1	2	Y	Y				2	1	Y	Y	
			2	1	Y	Y				1	2	Y	Y	
			3	0	Y	Y				0	3	Y	Y	
	CE23	FC15	0	3	N	Y		CE19	FC3	2	0	Y	N	
			2	1	N	Y				0	2	Y	N	
			1	2	N	Y				3	1	Y	N	
			3	0	Y	N				1	3	Y	N	
Tomahawk 2	CE20	FC12	0	0	Y	Y		CE20	FC31	0	1	Y	N	
			3	1	N	Y				1	0	Y	N	
			1	3	N	Y				3	3	Y	N	
			2	2	N	Y				2	2	Y	N	
	CE21	FC13	0	3	N	N		CE21	FC28	3	2	Y	N	
			1	2	N	N				2	3	Y	N	
			2	1	N	N				1	0	Y	N	
			3	0	N	N				0	1	Y	N	

	CE22	FC14	0	3	Y	N		CE22	FC29	0	3	Y	N	
			1	2	Y	N				1	2	Y	N	
			2	1	Y	N				2	1	Y	N	
			3	0	Y	N				3	0	Y	N	
	CE23	FC15	0	3	N	N		CE23	FC30	0	3	Y	N	
			1	2	N	N				1	2	Y	N	
			2	1	N	N				2	1	Y	N	
			3	0	N	N				3	0	Y	N	
Tomahawk 1	CE24	FC8	3	3	Y	N	To FAB 3#	CE16	FC1	3	0	Y	N	To LC 3#
			2	2	Y	N				2	1	Y	N	
			1	1	Y	N				1	2	Y	N	
			0	0	Y	N				0	3	Y	N	
	CE25	FC9	0	0	N	Y		CE17	FC2	3	0	Y	N	
			1	1	N	Y				2	1	Y	N	
			2	2	N	Y				1	2	Y	N	
			3	3	N	Y				0	3	Y	N	
	CE26	FC10	3	3	N	Y		CE18	FC0	3	0	Y	Y	
			2	2	N	Y				2	1	Y	Y	
			1	1	N	Y				1	2	Y	Y	
			0	0	N	Y				0	3	Y	Y	
	CE27	FC11	0	0	Y	N		CE19	FC3	2	0	Y	N	
			2	2	Y	N				0	2	Y	N	
			1	1	Y	N				3	1	Y	N	
			3	3	N	Y				1	3	Y	N	
Tomahawk 2	CE24	FC8	3	0	N	N		CE20	FC31	0	1	Y	N	
			0	1	Y	N				1	0	Y	N	
			2	3	Y	N				3	3	Y	N	
			1	2	Y	N				2	2	Y	N	
	CE25	FC9	0	0	N	N		CE21	FC28	3	2	Y	N	
			1	1	N	N				2	3	Y	N	
			2	2	N	N				1	0	Y	N	
			3	3	N	N				0	1	Y	N	
	CE26	FC10	3	3	N	Y		CE22	FC29	0	3	Y	N	
			2	2	N	Y				1	2	Y	N	
			1	1	N	Y				2	1	Y	N	
			0	0	N	Y				3	0	Y	N	
	CE27	FC11	0	0	Y	Y		CE23	FC30	0	3	Y	N	
			1	1	Y	Y				1	2	Y	N	
			2	2	Y	Y				2	1	Y	N	
			3	3	Y	Y				3	0	Y	N	
Tomahawk 1	CE28	FC4	3	3	Y	N	To FAB 4#	CE16	FC1	3	0	Y	N	To LC 3#
			2	2	Y	N				2	1	Y	N	
			1	1	Y	N				1	2	Y	N	
			0	0	Y	N				0	3	Y	N	
	CE29	FC5	0	0	N	Y		CE17	FC2	3	0	Y	N	

			1	1	N	Y				2	1	Y	N	
			2	2	N	Y				1	2	Y	N	
			3	3	N	Y				0	3	Y	N	
	CE30	**FC6**	3	3	N	N		**CE18**	**FC0**	3	0	Y	Y	
			2	2	N	N				2	1	Y	Y	
			1	1	N	N				1	2	Y	Y	
			0	0	N	N				0	3	Y	Y	
	CE31	**FC7**	0	0	N	N		**CE19**	**FC3**	2	0	Y	N	
			2	2	N	N				0	2	Y	N	
			1	1	N	N				3	1	Y	N	
			3	3	Y	Y				1	3	Y	N	
Tomahawk 2	**CE28**	**FC4**	3	0	N	N		**CE20**	**FC31**	0	1	Y	N	
			0	1	Y	N				1	0	Y	N	
			2	3	Y	N				3	3	Y	N	
			1	2	Y	N				2	2	Y	N	
	CE29	**FC5**	0	0	N	N		**CE21**	**FC28**	3	2	Y	N	
			1	1	N	N				2	3	Y	N	
			2	2	N	N				1	0	Y	N	
			3	3	N	N				0	1	Y	N	
	CE30	**FC6**	3	3	N	Y		**CE22**	**FC29**	0	3	Y	N	
			2	2	N	Y				1	2	Y	N	
			1	1	N	Y				2	1	Y	N	
			0	0	N	Y				3	0	Y	N	
	CE31	**FC7**	0	0	N	Y		**CE23**	**FC30**	0	3	Y	N	
			1	1	N	Y				1	2	Y	N	
			2	2	N	Y				2	1	Y	N	
			3	3	N	Y				3	0	Y	N	

Table 26: LC-3 Port Mapping to FAB

6.2.4. LC-4 port mapping to Fabric Cards

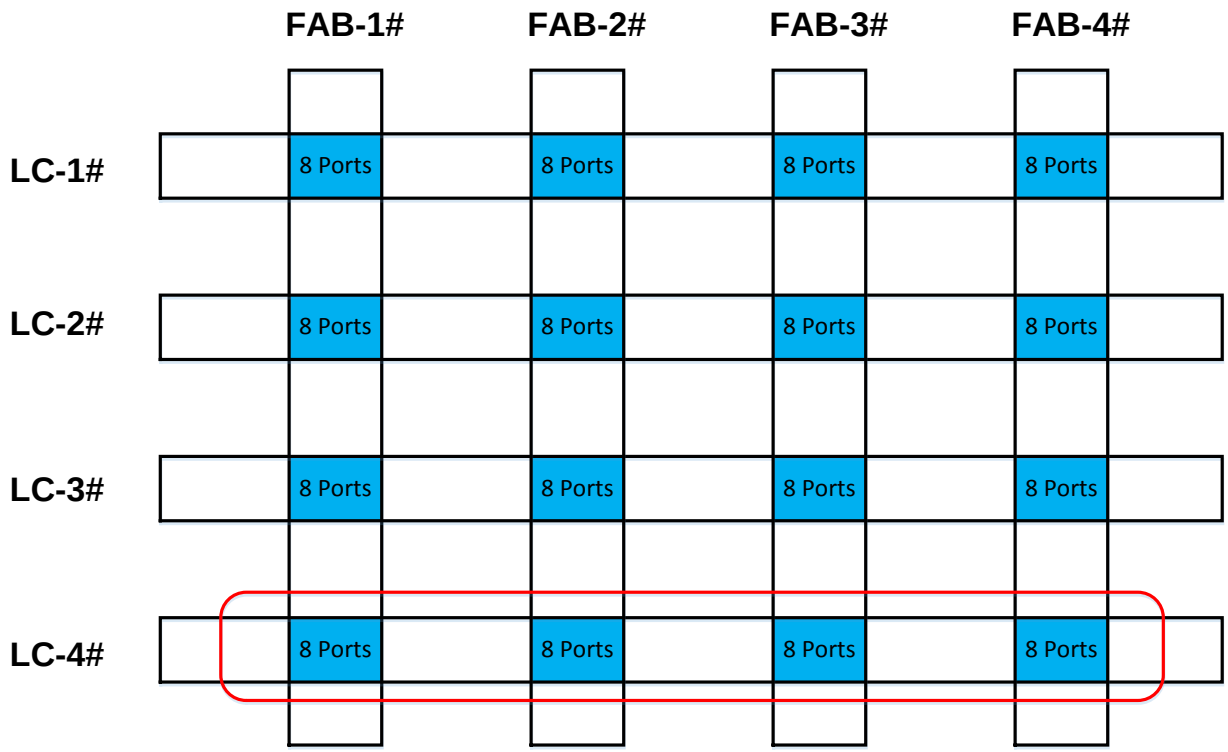

Figure 42: LC-4 Orthogonal Connection to FAB

	SDK Port No.	FC	TD Ln	RD Ln	TD P/N swap	RD P/N swap	Note	SDK Port No.	FC	TD Ln	RD Ln	TD P/N swap	RD P/N swap	Note
Tomahawk 1	CE16	FC16	3	0	N	N	To FAB 1#	CE24	FC10	3	3	N	Y	To LC 4#
			2	1	N	N				2	2	N	Y	
			1	2	N	N				1	1	N	Y	
			0	3	N	N				0	0	N	Y	
	CE17	FC17	0	3	N	Y		CE25	FC9	0	0	Y	N	
			1	2	N	Y				1	1	Y	N	
			2	1	N	Y				2	2	Y	N	
			3	0	N	Y				3	3	Y	N	
	CE18	FC18	0	3	Y	N		CE26	FC7	0	0	Y	N	
			1	2	Y	N				1	1	Y	N	
			2	1	Y	N				2	2	Y	N	

			3	0	Y	N				3	3	Y	N	
	CE19	FC19	2	3	N	Y		CE27	FC11	1	1	Y	N	
			1	0	N	Y				3	3	Y	N	
			0	1	N	Y				0	0	Y	N	
			3	2	Y	N				2	2	Y	N	
Tomahawk 2	CE16	FC16	3	3	Y	N		CE28	FC8	3	3	N	Y	
			0	2	N	N				2	1	N	Y	
			2	0	N	N				0	2	N	Y	
			1	1	N	N				1	0	N	Y	
	CE17	FC17	0	3	N	N		CE29	FC5	3	3	Y	N	
			1	2	N	N				2	2	Y	N	
			2	1	N	N				1	1	Y	N	
			3	0	N	N				0	0	Y	N	
	CE18	FC18	0	3	Y	Y		CE30	FC6	0	0	N	Y	
			1	2	Y	Y				1	1	N	Y	
			2	1	Y	Y				2	2	N	Y	
			3	0	Y	Y				3	3	N	Y	
	CE19	FC19	2	3	N	N		CE31	FC4	0	0	N	Y	
			0	1	N	N				1	1	Y	Y	
			1	0	N	N				2	2	N	Y	
			3	2	N	N				3	3	N	Y	
Tomahawk 1	CE20	FC12	0	3	N	Y	To FAB 2#	CE24	FC10	3	3	N	Y	To LC 4#
			1	2	N	Y				2	2	N	Y	
			2	1	N	Y				1	1	N	Y	
			3	0	N	Y				0	0	N	Y	
	CE21	FC13	0	3	N	Y		CE25	FC9	0	0	Y	N	
			1	2	N	Y				1	1	Y	N	
			2	1	N	Y				2	2	Y	N	
			3	0	N	Y				3	3	Y	N	
	CE22	FC14	0	3	Y	Y		CE26	FC7	0	0	Y	N	
			1	2	Y	Y				1	1	Y	N	
			2	1	Y	Y				2	2	Y	N	
			3	0	Y	Y				3	3	Y	N	
	CE23	FC15	0	3	N	Y		CE27	FC11	1	1	Y	N	
			2	1	N	Y				3	3	Y	N	
			1	2	N	Y				0	0	Y	N	
			3	0	Y	N				2	2	Y	N	
Tomahawk 2	CE20	FC12	0	0	Y	Y		CE28	FC8	3	3	N	Y	
			3	1	N	Y				2	1	N	Y	
			1	3	N	Y				0	2	N	Y	
			2	2	N	Y				1	0	N	Y	
	CE21	FC13	0	3	N	N		CE29	FC5	3	3	Y	N	
			1	2	N	N				2	2	Y	N	
			2	1	N	N				1	1	Y	N	

			3	0	N	N				0	0	Y	N	
	CE22	FC14	0	3	Y	N		CE30	FC6	0	0	N	Y	
			1	2	Y	N				1	1	N	Y	
			2	1	Y	N				2	2	N	Y	
			3	0	Y	N				3	3	N	Y	
	CE23	FC15	0	3	N	N		CE31	FC4	0	0	N	Y	
			1	2	N	N				1	1	Y	Y	
			2	1	N	N				2	2	N	Y	
			3	0	N	N				3	3	N	Y	
Tomahawk 1	CE24	FC8	3	3	Y	N	To FAB 3#	CE24	FC10	3	3	N	Y	To LC 4#
			2	2	Y	N				2	2	N	Y	
			1	1	Y	N				1	1	N	Y	
			0	0	Y	N				0	0	N	Y	
	CE25	FC9	0	0	N	Y		CE25	FC9	0	0	Y	N	
			1	1	N	Y				1	1	Y	N	
			2	2	N	Y				2	2	Y	N	
			3	3	N	Y				3	3	Y	N	
	CE26	FC10	3	3	N	Y		CE26	FC7	0	0	Y	N	
			2	2	N	Y				1	1	Y	N	
			1	1	N	Y				2	2	Y	N	
			0	0	N	Y				3	3	Y	N	
	CE27	FC11	0	0	Y	N		CE27	FC11	1	1	Y	N	
			2	2	Y	N				3	3	Y	N	
			1	1	Y	N				0	0	Y	N	
			3	3	N	Y				2	2	Y	N	
Tomahawk 2	CE24	FC8	3	0	N	N		CE28	FC8	3	3	N	Y	
			0	1	Y	N				2	1	N	Y	
			2	3	Y	N				0	2	N	Y	
			1	2	Y	N				1	0	N	Y	
	CE25	FC9	0	0	N	N		CE29	FC5	3	3	Y	N	
			1	1	N	N				2	2	Y	N	
			2	2	N	N				1	1	Y	N	
			3	3	N	N				0	0	Y	N	
	CE26	FC10	3	3	N	Y		CE30	FC6	0	0	N	Y	
			2	2	N	Y				1	1	N	Y	
			1	1	N	Y				2	2	N	Y	
			0	0	N	Y				3	3	N	Y	
	CE27	FC11	0	0	Y	Y		CE31	FC4	0	0	N	Y	
			1	1	Y	Y				1	1	Y	Y	
			2	2	Y	Y				2	2	N	Y	
			3	3	Y	Y				3	3	N	Y	
Tomahawk 1	CE28	FC4	3	3	Y	N	To FAB 4#	CE24	FC10	3	3	N	Y	To LC 4#
			2	2	Y	N				2	2	N	Y	
			1	1	Y	N				1	1	N	Y	
			0	0	Y	N				0	0	N	Y	

	CE29	FC5	0	0	N	Y		CE25	FC9	0	0	Y	N
			1	1	N	Y				1	1	Y	N
			2	2	N	Y				2	2	Y	N
			3	3	N	Y				3	3	Y	N
	CE30	FC6	3	3	N	N		CE26	FC7	0	0	Y	N
			2	2	N	N				1	1	Y	N
			1	1	N	N				2	2	Y	N
			0	0	N	N				3	3	Y	N
	CE31	FC7	0	0	N	N		CE27	FC11	1	1	Y	N
			2	2	N	N				3	3	Y	N
			1	1	N	N				0	0	Y	N
			3	3	Y	Y				2	2	Y	N
Tomahawk 2	CE28	FC4	3	0	N	N		CE28	FC8	3	3	N	Y
			0	1	Y	N				2	1	N	Y
			2	3	Y	N				0	2	N	Y
			1	2	Y	N				1	0	N	Y
	CE29	FC5	0	0	N	N		CE29	FC5	3	3	Y	N
			1	1	N	N				2	2	Y	N
			2	2	N	N				1	1	Y	N
			3	3	N	N				0	0	Y	N
	CE30	FC6	3	3	N	Y		CE30	FC6	0	0	N	Y
			2	2	N	Y				1	1	N	Y
			1	1	N	Y				2	2	N	Y
			0	0	N	Y				3	3	N	Y
	CE31	FC7	0	0	N	Y		CE31	FC4	0	0	N	Y
			1	1	N	Y				1	1	Y	Y
			2	2	N	Y				2	2	N	Y
			3	3	N	Y				3	3	N	Y

Table 27: LC-4 Port Mapping to FAB

6.3. Control Plane

Main control plane features are listed below:

- COM-Express Baytrail CPU module from Portwell as CPU module
  - 8mm mating distance.
  - Can upgrade to Broadwell-DE COM-E module
  - Implemented on SCM
- BMC as management entity to control Switch ASIC and COM-E CPU module
  - Enable/disable power of switch ASIC or SCM
  - OOB ethernet to CMM
  - Console port to CMM
  - SMB bus and I2C bus to SCM COM-E CPU module
- Front panel management and debug interface
  - Facebook 14-pin debug connector, CMM only
  - Facebook new Debug interface using USB3 connector, CMM only
  - OOB GbE for Management port access
  - RJ45 Console port for UART console access
- PCIe Interface
  - PCIe x4 gen2 between SCM COM-E and Switch ASIC(Tomahawk)
  - PCIe clock is from COM-E module to Switch ASIC
- LPC bus
  - SCM COMe LPC bus control the following devices
    - LPC TPM on SCM
    - BMC on LC and FAB
    - SYSCPLD of LC and FAB
    - SYSCPLD as LPC-I2C bridge for LC or FAB I2C access
  - LC and FAB SYSCPLD implement LPC to I2C bridge function
- OOB Ethernet
  - 8-port OOB GbE switch BCM5389 for each switch element(LC or FAB)
    - BMC GBE ethernet interface
    - SCM COM-E ethernet interface
    - Switch ASIC management GBE port(SGMII)
    - CMM0 OOB ethernet interface
    - CMM1 OOB ethernet interface
    - On-board debug RJ45 port
    - 2 ports unused
  - All LC and FAB OOB ethernet ports are aggregated to CMM.
    - 16-port OOB GbE switch BCM5396 on CMM
      - 8 ports from LC
      - 4 ports from FAB
      - 1 port from CMM BMC
      - 1 port front panel RJ45 port of CMM
      - 1 port from paired CMM BCM5396

- 1 port unused

- USB
  - COM-E is root-complex port
  - 3-port USB hub on LC or FAB
    - BMC USB slave port
    - On-board debug USB type-A port
    - CP2112 USB port for QSFP28 I2C access

6.4. Chassis management Plane

CMM is the chassis management module, two CMMs are available in the system, one is working as active, and the other is standby. Chassis management bus is I2C, the management bus can access the following modules:

- Line Cards (LC)
  - G4: LC-#1, LC-#2, LC-#3, LC-#4
- Fabric Card(FAB)
  - G4: FAB-#1, FAB-#2, FAB-#3, FAB-#4, each FAB has one tomahawk
- System Control Module
  - G4:
    - SCM-L1, SCM-L2, SCM-L3, SCM-L4
    - SCM-FAB1, SCM-FAB2, SCM-FAB3, SCM-FAB4

Chassis management I2C bus topology is shown in the following diagram.

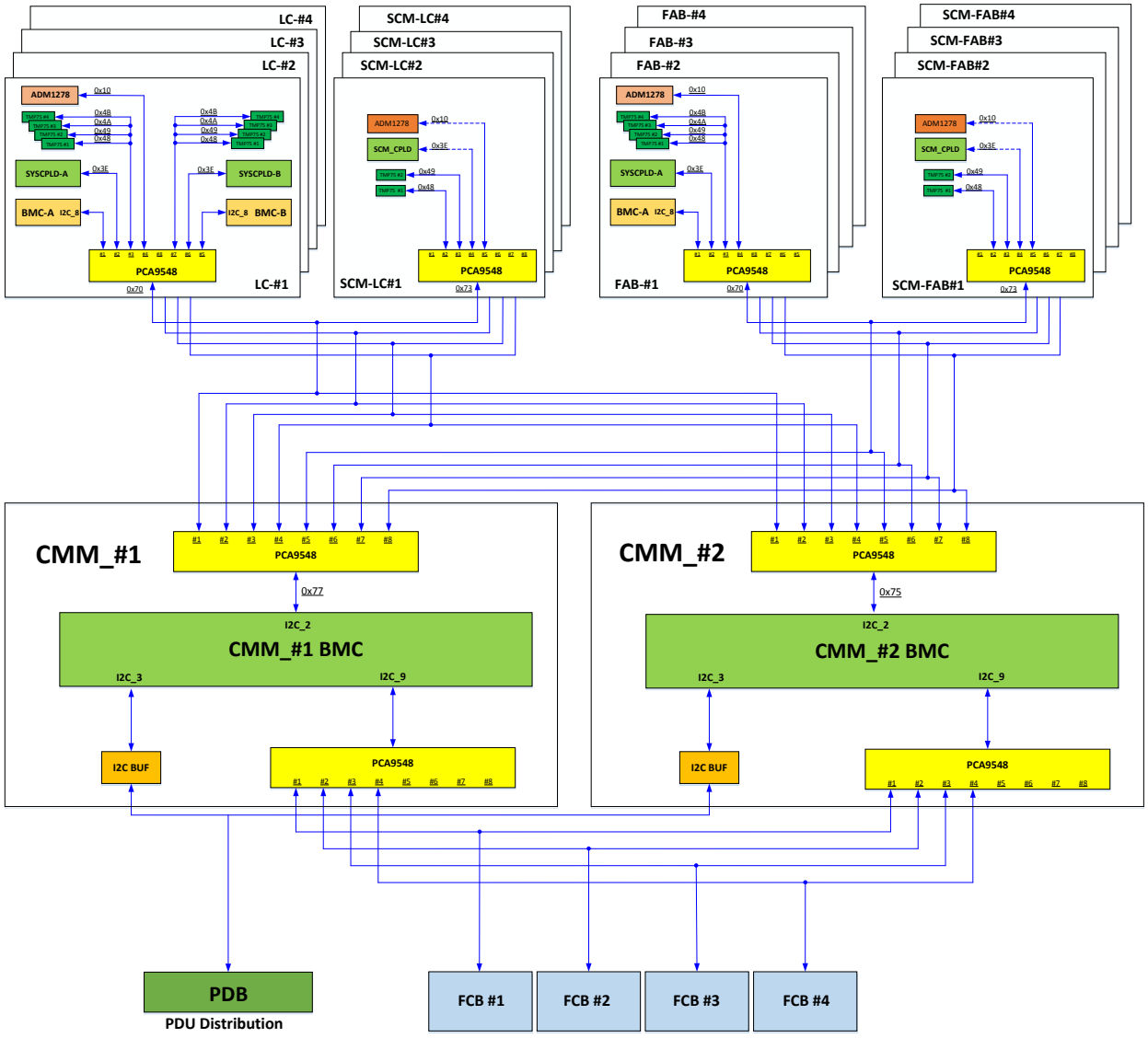

Figure 43: Chassis Management I2C bus Diagram

Please refer to PDB and FCB I2C section for more detail information about the I2C topology inside these two Boards.

6.5. Orthogonal Direct architecture

Backpack uses orthogonal direct architecture for chassis design. It does not have high speed data midplane, LC high speed connector directly mate to the high speed connector of FAB, providing more air channel for air flow inside chassis; orthogonal direct architecture can minimize the high speed PCB trace length to provide much better signal integrity performance than traditional backplane architecture.

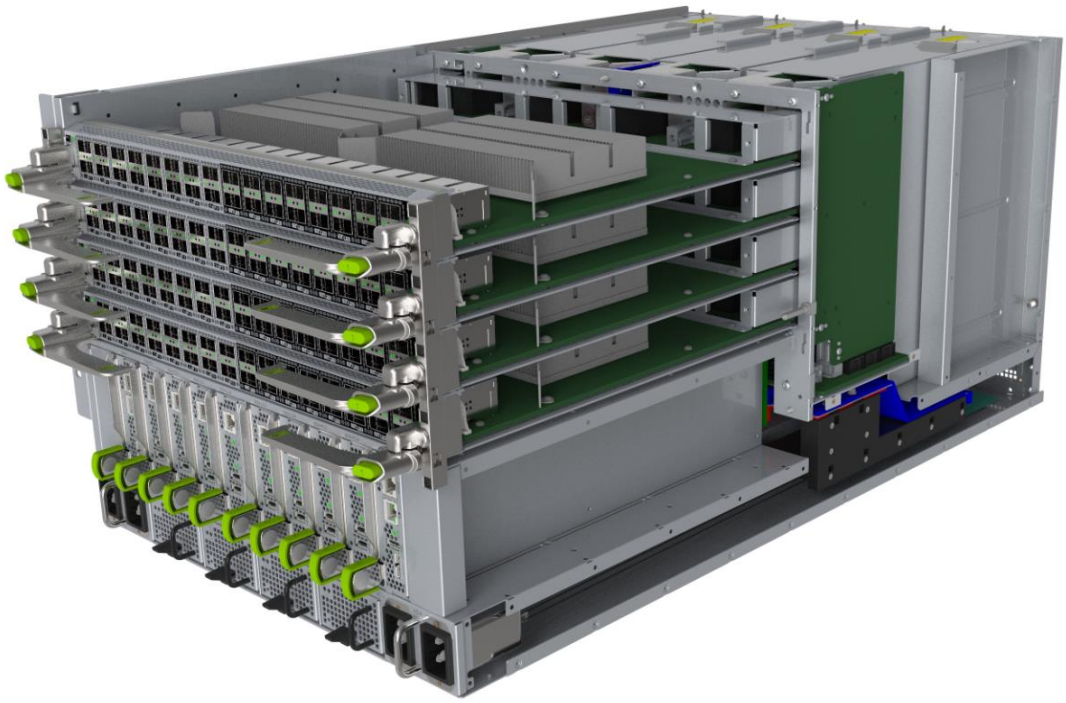

Figure 44: front ISO view of Backpack Orthogonal Architecture

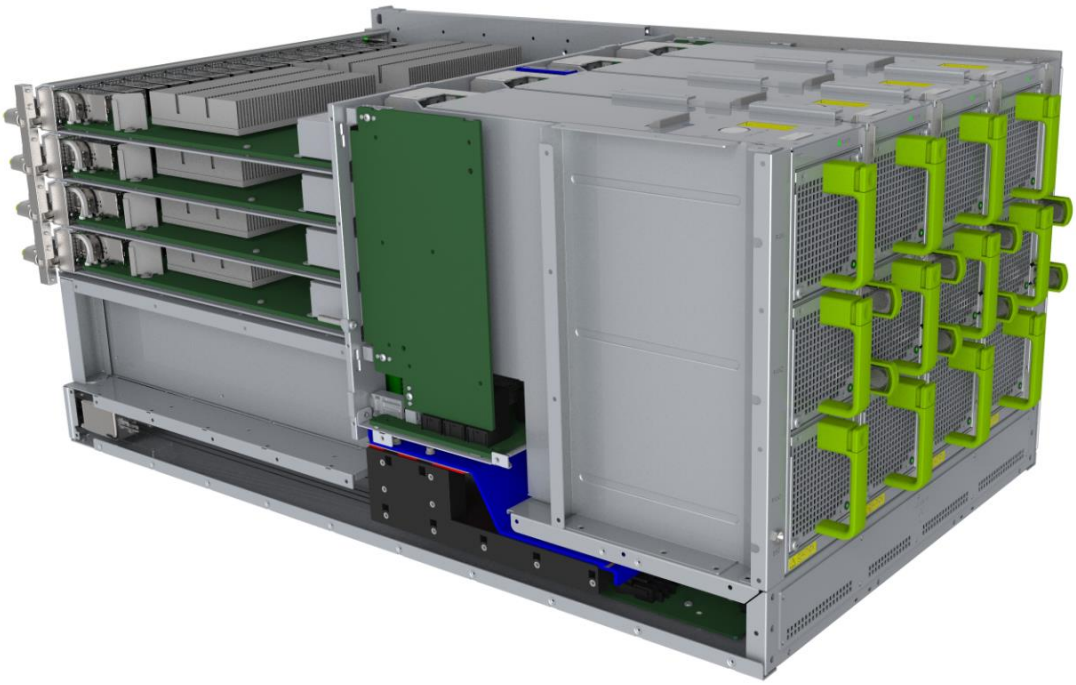

Figure 45: Rear ISO view of Backpack Orthogonal Architecture

Figure 46: Front View of empty Chassis

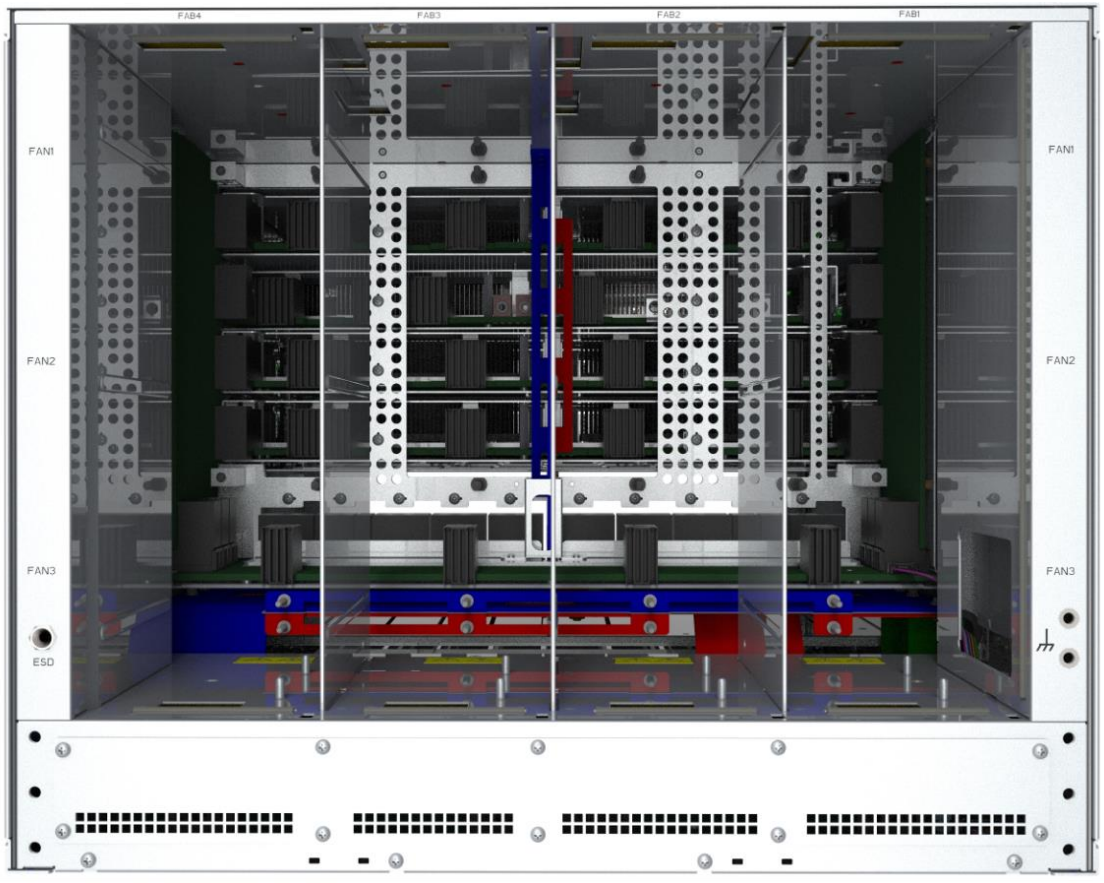

Figure 47: Rear View of Backpack Chassis without fabric card

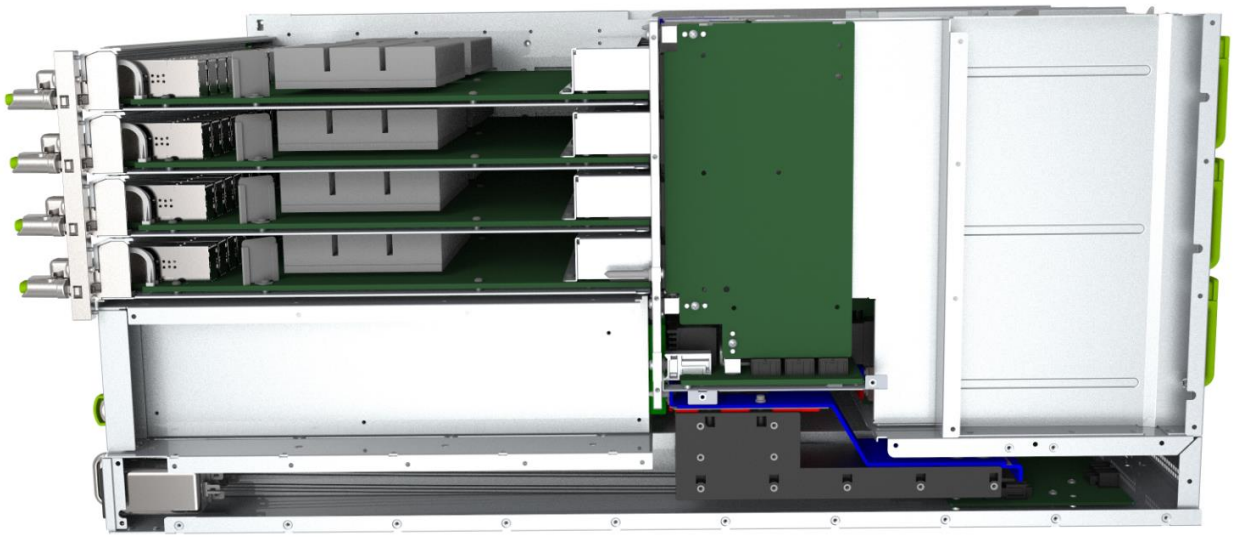

Figure 48: Backpack Side View

6.5.1. Direct Mated Orthogonal Connector

Backpack uses FCI EXAMAX DMO (Direct Mated Orthogonal) connector for both data plane and control plane interconnect. The following picture shows the typical direct mating diagram of EXAMAX orthogonal direct connector, more information can be downloaded from Amphenol FCI website.

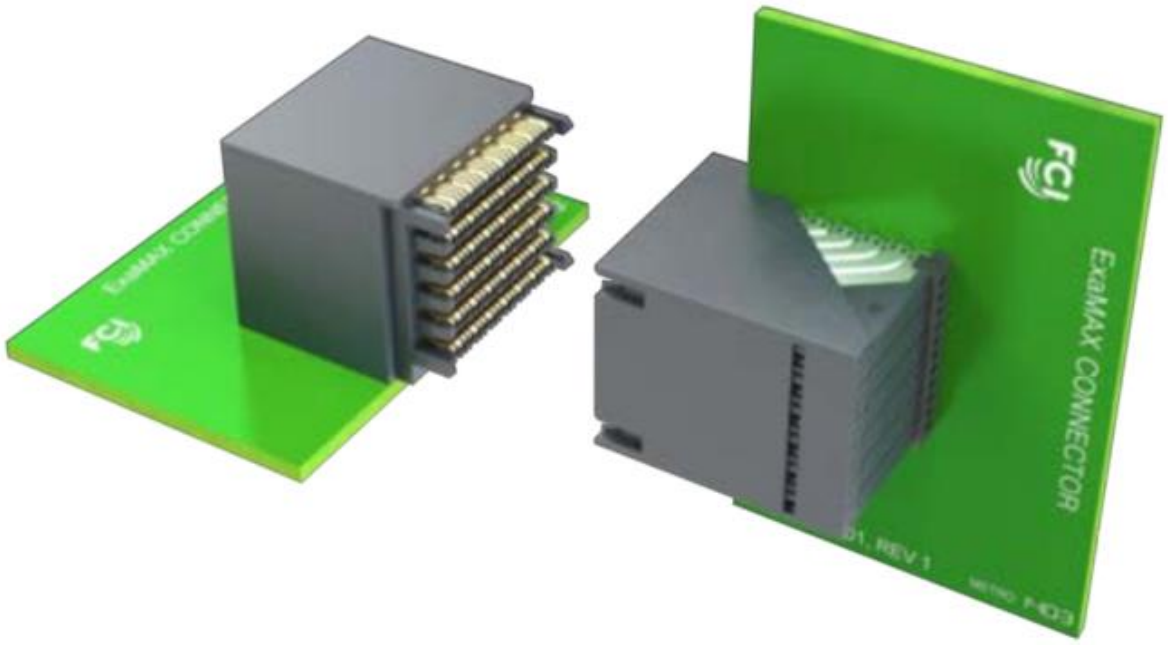

Figure 49 : Amphenol FCI EXAMAX DMO connector

For highspeed data plane signals, LC uses four 6x12 Daughter Card RAR(Right Angle Receptacle) to mate RAOH(Right Angle Orthogonal Header) connector of four FAB cards, only 64 pairs are used among 72 pairs in the 6x12 DMO pair. For control plane signals, Left SWE of LC uses one 6x8 Daughter Card RAR (Right Angle Receptacle) connector to mate the RAOH(Right Angle Orthogonal Header) connector of VCP-LEFT, and right SWE of LC uses one 6x8 Daughter Card RAR (Right Angle Receptacle) connector to mate the RAOH(Right Angle Orthogonal Header) connector of VCP-RIGHT

6.6. Chassis Power

Power of the chassis is provided by four power supply units. Each PSU is rated to supply up to 3000W at 12V.

Card	Backpack 4-slot Chassis		
	Unit Power	Qty	Power (W)
FAB	200	4	800
LC	500	4	2000
SCM (2x COMe)	80	4	320
SCM (1x COMe)	40	4	160
CMM	20	2	40
Fan (<80%)	50	12	600
Total			3920

Table 28: Power Consumption Under worst operating scenario

The worst scenario could happen in real operating scenario, such as all fan-tray spinning at maximal allowed speed (Backpack thermal policy software set it to 80% maximal to reduce the power consumption); in normal operating environment, the typical power consumption is much less than the table above, the following table is a more realistic estimate and can be used for data center power budgeting.

Please also note that the Backpack hardware design support much more power consumption that the worst operation scenario. The power consumption under worst operation scenario is for data center budgeting purpose.

Card	Backpack		
	Unit Power	Qty	Power (W)
FAB	160	4	640
LC	400	4	1600
SCM (2x COMe)	40	4	160
SCM (1x COMe)	20	4	80
CMM	10	2	20
Fan	5	12	60
Total			2560

Table 29: Power Consumption under normal operating conditions

VBAR needs to provide power to all line cards, so totally HBAR needs to provide 240A to VBAR. HPD needs to provide power to both fabric cards and SCMs, HPD receives power from HBAR, then provides power to VBAR, 4 FAB, and SCMs.

6.6.1. Power Distribution System

Backpack Power distribution system consists of the following items:

- PSU: 3000W PSU from PowerOne PFE3000-12
- PDB: Power Distribution Board, 4 AC inlet, provide AC input voltage to four PSU.
- HBAR: Horizontal bus bar, combine the 12V outputs of four PSU.
- HPD: Horizontal Power Distribution Module, HPD is part of copper bus Bar Assembly.
- VBAR: Vertical bus Bar to provide power to Line Cards

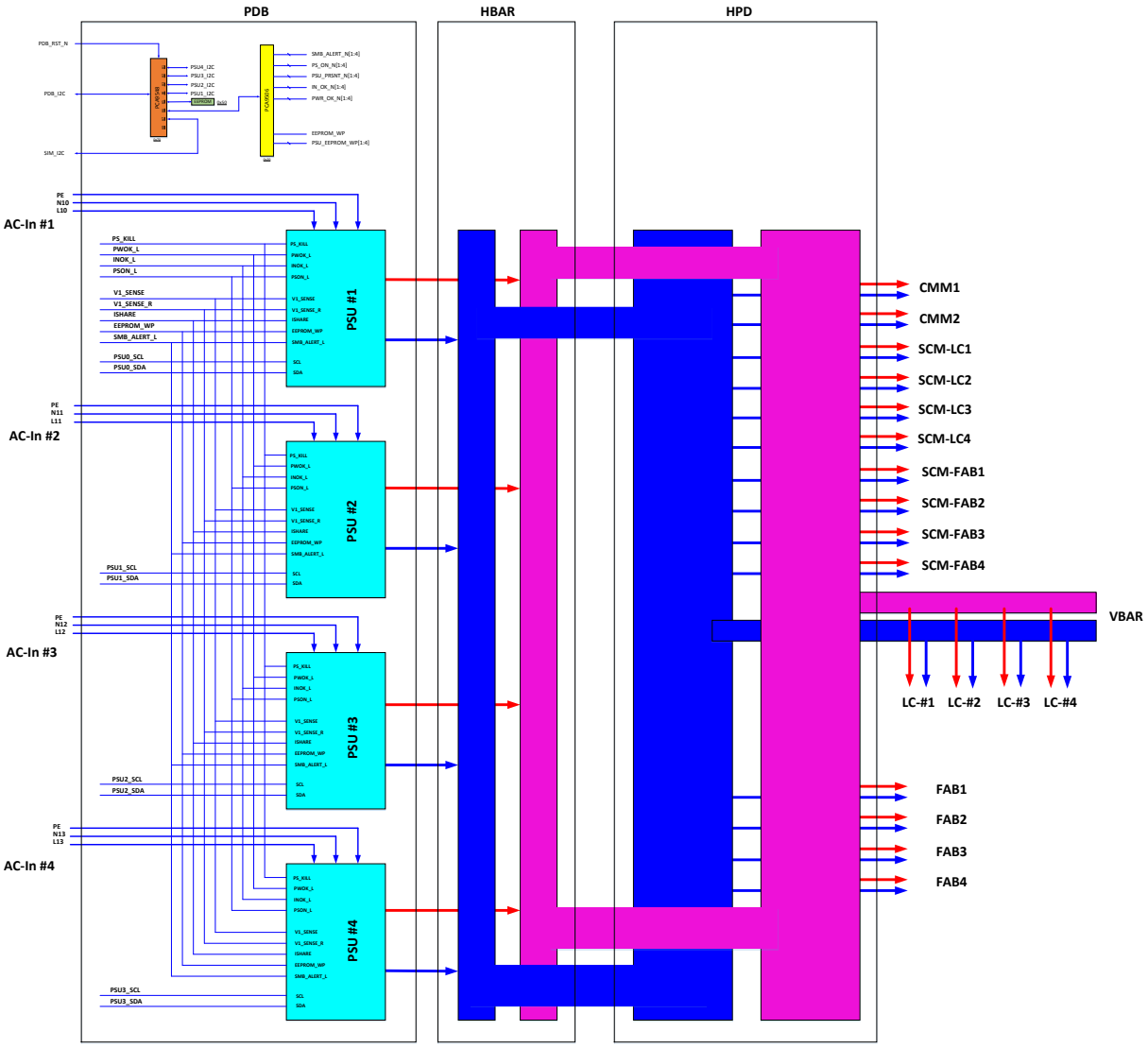

Figure 50: Backpack Power Distribution System

Backpack bus bar assembly is shown by the following diagram

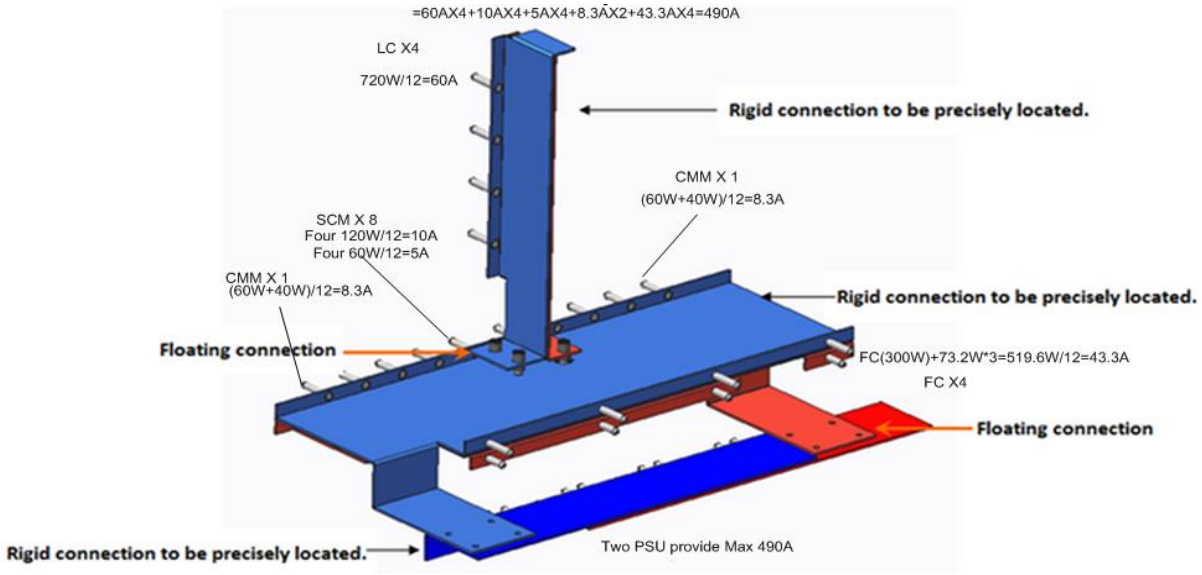

Figure 51: Backpack Bus Bar Assembly

Each Redsok connector on the Bus Bar could support the maximum current as below table

Redsok location	Power (W)	Qty.	Total Power (W)	Current (A)	Total Current (A)
Line Card	720	4	2880	60.0	240.0
Fabric Card/3 FAN	519.6	4	2078.4	43.3	173.2
CMM	100	2	200	8.3	16.7
SCM-FAB	60	4	240	5.0	20.0
SCM-LC	120	4	480	10.0	40.0
		Total	5878.4		489.9

Table 30: Backpack Power Bar System Specification

6.6.2. PSU

Backpack uses BelPower PFE3000-12 AC power supply unit (PSU) to provide power to the chassis. There are 4 PSU in the chassis. Each PSU is rated at 3000W with 12V output. The power system of Backpack is load sharing of four PSU, usually it is used as 2+2 PSU redundancy, two PSU connect to one AC feed and two other PSU connect to redundant feed, providing feed redundancy, And two PSU in one feed can also provide PSU redundancy. The following Figure shows the AC PSU from BelPower/PowerOne.

Figure 52: PFE3000-12 3KW PSU

6.7. Thermal design

The thermal design of Backpack is optimized for better thermal performance to support 55C CWDM4 optics, which is specified by facebook. It is also targeting much better performance than current 128 x 100G configuration, enabling Backpack platform to support future 200G or even 400G design.

Totally there are 12 fan-tray in Backpack chassis, each fan-tray has one 80mm x 80mm x 76mm CR fan. Each FAB carries one FCB(Fan Control Board), and each FCB supports 3 fan-tray.

6.7.1. Fan tray

Backpack chassis supports four fan-tray with 3+1 redundancy. For G4, each fan-tray has three 80mm CR fans, for G8, each fan-tray has five 80mm CR fan.

Figure 53: Backpack Fan-tray

The following Sanyo Denki CR fan is recommended.

- Sanyo Denki: 9CRA0812P8G001 (80mm x 80mm x 80mm)
    - 63.6W Max
    - Rated speed: 12000 inlet, 11300 outlet
    - Max Airflow: 4.5 M3/min, or 158.9CFM
    - Max Static Pressure: 4.62 inchH2O

Figure 54 Backpack fan

80mm CR fan 9CRA0812P8G001 from Sanyo Denki has the following technical parameters

9CRA0812P8G001	
Item	Description
Rated voltage	12 VDC
Operating voltage	7.0 ~ 13.2 VDC
Input current	5.30A
Input power	63.6W
speed	Front 12000, Rear 11300 RPM +/-10%
Max Air flow at zero static	4.50m3/min, or 158.9CFM
Max Air Pressure	4.62 in-H2O
acoustic	76 dB-A
Lead Wire	

Table 31: Sanyo Denki fan 9CRA0812P8G001

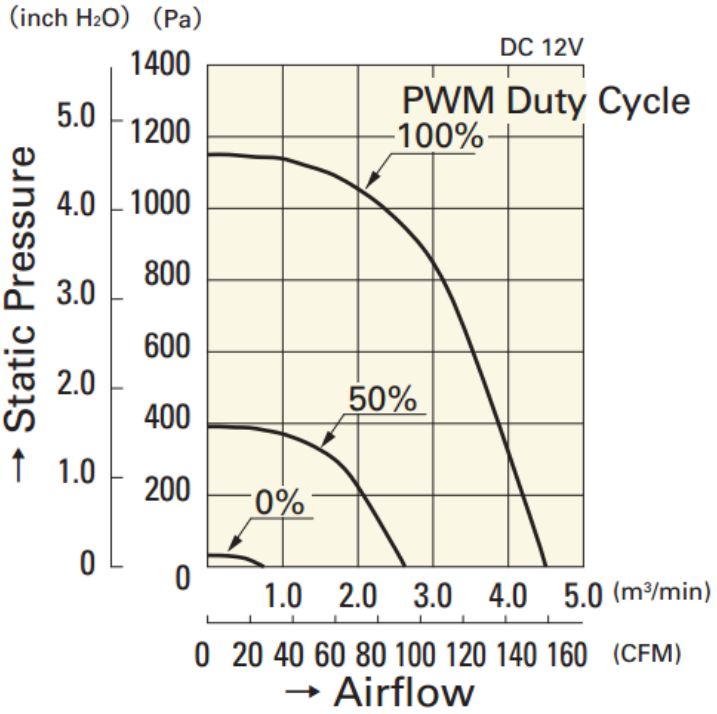

Figure 55: PQ Curve of CR Fan 9CRA0812P8G001

6.7.2. Temperature Sensors

Each module card can have multiple temperature sensors to monitor temperature. Temperature information needs to be reported to the CMM via system management I2C bus.

Additionally, over-temperature thresholds are configurable and an alert mechanism is provided to enable thermal shutdown and / or an increase in airflow. The sensors are accurate to +/-2C.

The ambient temperature sensor can be a *TMP75* from Texas Instruments or an equivalent part from other vendors. Its I2C address can be set to 0x98 to 0x9F. 8 TMP75 temperature sensors can share one i2c bus.

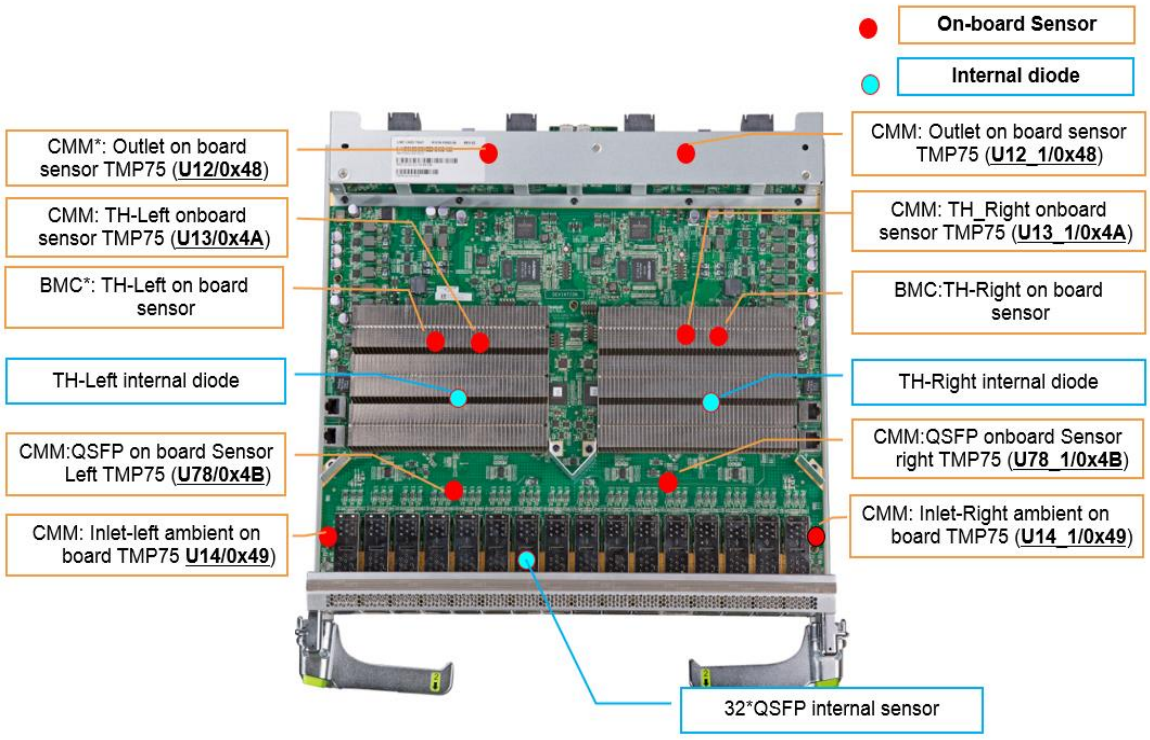

Figure 56 : Temperature Sensor Location on LC

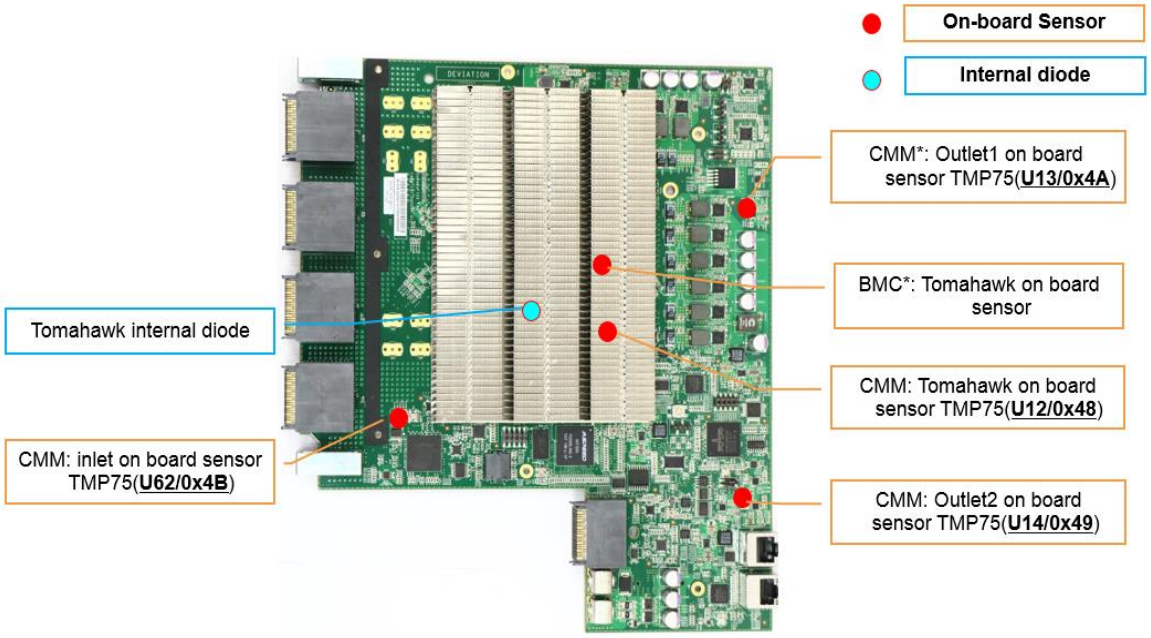

Figure 57: Temperature Sensor Location on FAB

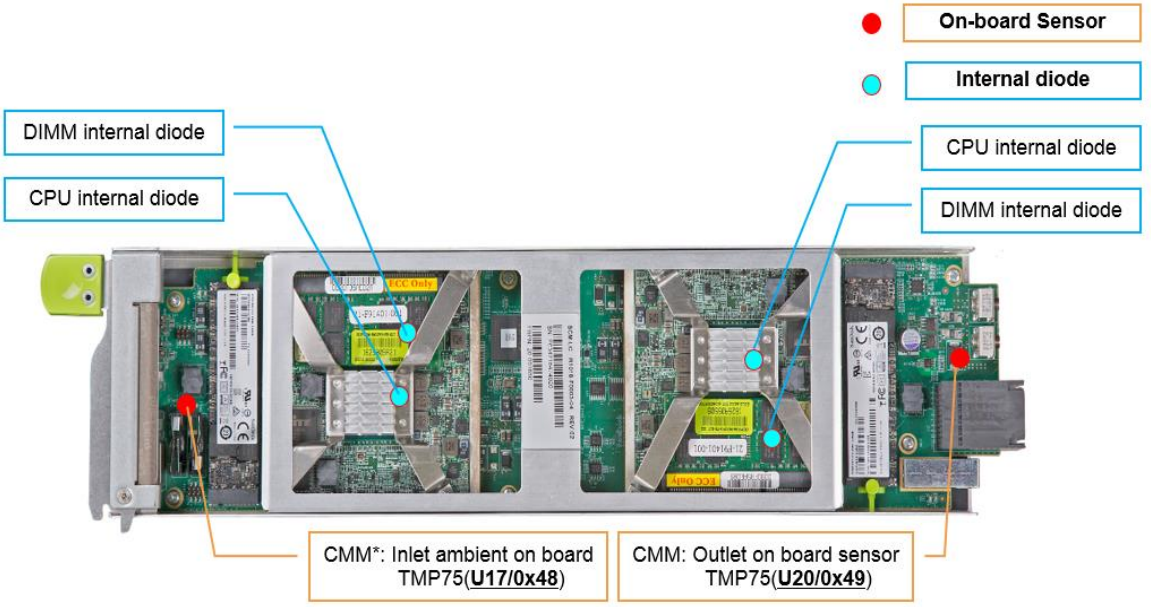

Figure 58: Temperature Sensor Location on SCM

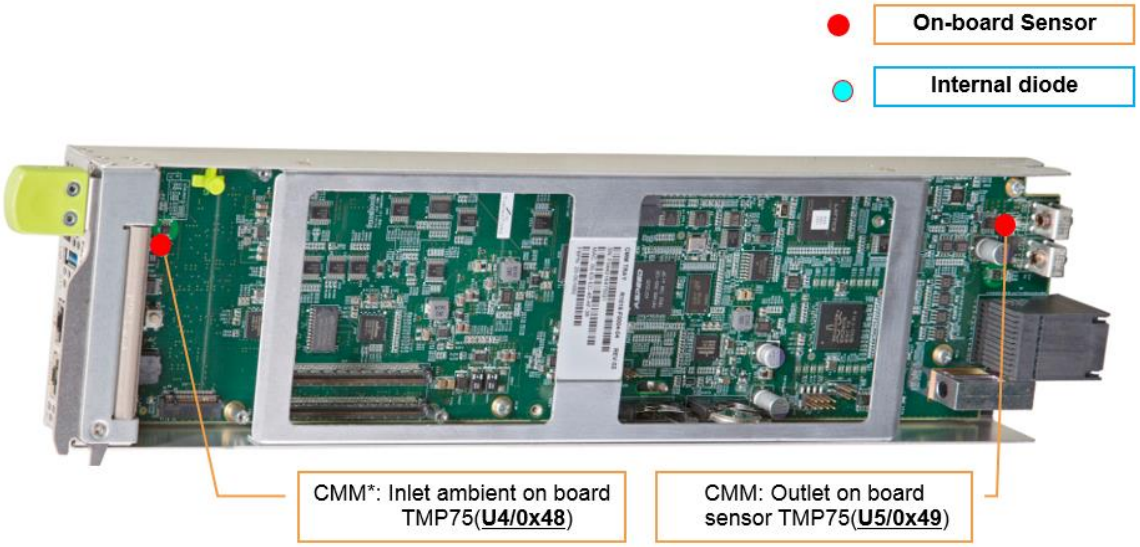

Figure 59: Temperature Sensor Location on CMM

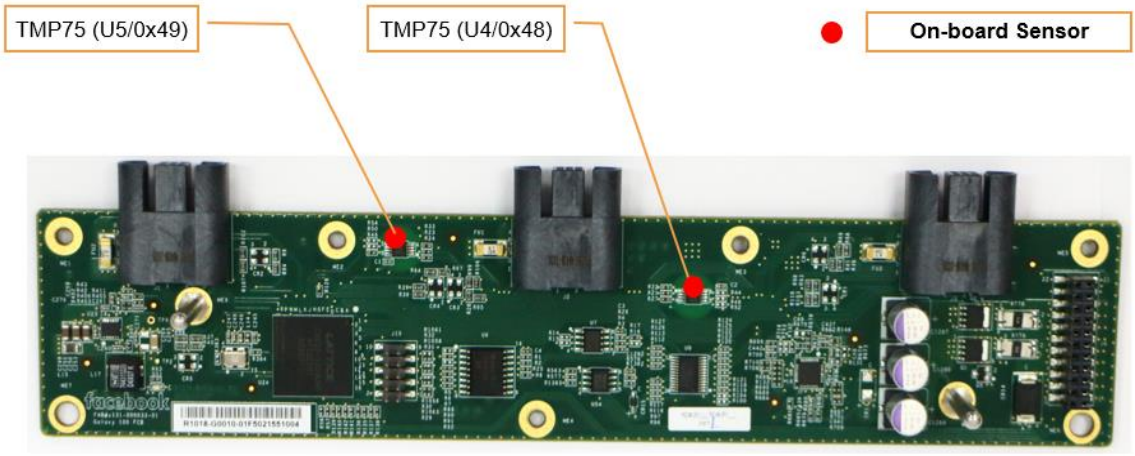

Figure 60: Temperature Sensor Location on FCB

6.8. FRU and Module Numbering

6.8.1. FRU Name

Each module or FRU has an user identification number. The following table lists the FRU in Backpack G4 system.

G4 Chassis	Notes
LC1 – LC4	Backpack G4 chassis has four Line Card: LC1 to LC4
FAB1 - FAB4	Backpack G4 chassis has four fabric card: FAB1 to FAB4
CMM1 – CMM2	Primary and secondary CMM: CMM1 and CMM2
SCM-L1, SCM-L2, SCM-L3, SCM-L4	SCM for Line Card LC1 to LC4, two COM-E CPU module populated
SCM-FAB1, SCM-FAB2, SCM-FAB3, SCM-FAB4	SCM for Fabric card FAB1 to FAB4, one COM-E CPU module populated
FAN1 – FAN4	Fan-tray 1 to 4

Table 32: FRU Numbering

6.8.2. Slot ID for CMM and SCM

Every line card, fabric card, SCM and CMM has one unique slot ID.

On SCM and CMM, the following table show the slot ID definition. Software can read the slot ID information from SCM CPLD SLOT_ID register 0x03, or from CMM CPLD register SLOT_ID 0x03.

SCM_SLOT_ID[3:0]	Indication
0000	Slot-1, unused in G4
0001	Slot-2, CMM1 in G4
0010	Slot-3, SCM-FAB1
0011	Slot-4, SCM-FAB2
0100	Slot-5, SCM-LC1
0101	Slot-6, SCM-LC2
0110	Slot-7, SCM-LC3
0111	Slot-8, SCM-LC4
1000	Slot-9, SCM-FAB3
1001	Slot-10, SCM-FAB4
1010	Slot-11, CMM2 in G4
1011	Slot-12, unused in G4
1100	Unused ID
1101	Unused ID
1110	Unused ID
1111	Unused ID

Table 33: SCM Slot ID

6.8.3. Slot ID for LC and FAB

On LC and FAB, the following table show the slot ID definition. Software can read the slot ID information from LC CPLD SLOT_ID register 0x03, or from FAB CPLD SLOT_ID register 0x03.

LC_FAB_SLOT_ID[3:0]	Indication
0000	Slot-1, LC-#1
0001	Slot-2, LC-#2
0010	Slot-3, LC-#3
0011	Slot-4, LC-#4
0100	Slot-5, LC-#5
0101	Slot-6, LC-#6
0110	Slot-7, LC-#7
0111	Slot-8, LC-#8
1000	Slot-1, FAB-#1
1001	Slot-2, FAB-#2
1010	Slot-3, FAB-#3
1011	Slot-4, FAB-#4
1100	Unused ID
1101	Unused ID
1110	Unused ID
1111	Unused ID

Table 34: LC and FAB Slot ID

6.8.4. Module Board ID

Every line card, fabric card, CMM has one unique board ID.

BRD_ID[7:0]	Indication
1111_0000	Backpack LC Type-1
1111_0001	Backpack LC Type-2 (Reserved)
1111_0010	Backpack LC Type-3 (Reserved)
1111_0011	Backpack LC Type-4 (Reserved)
1111_0100	Backpack FAB Type-1
1111_0101	Backpack FAB Type-2 (Reserved)
1111_0110	Backpack FAB Type-3 (Reserved)
1111_0111	Backpack FAB Type-4 (Reserved)
1111_1100	Backpack CMM Type-1
1111_1101	Backpack CMM Type-2 (Reserved)
1111_1110	Backpack CMM Type-3 (Reserved)
1111_1111	Backpack CMM Type-4 (Reserved)
Others	Reserved

Table 35: LC, FAB and CMM Board ID

7. Transceivers and cables

7.1. 100G optic

- QSFP28 CWDM4 100G transceiver (MSA)
- QSFP28 LR4/LR4-lite 100G transceiver (IEEE)
- QSFP28 SR4 100G transceiver (IEEE)
- QSFP28 CLR4 100G transceiver (MSA)

7.2. 100G DAC Cable

- QSFP28 100GE to QSFP28 100GE cable, 1M, 2M, 3M
- QSFP28 100GE to 2 QSFP28 50GE split cable, aka Y-cable, 1M, 2M, 3M
- QSFP28 100GE to 4 SFP28 25GE fanout cable, 1M, 2M, 3M

7.3. 40G optic

- QSFP SR4 40G transceiver
- QSFP LR4 40G transceiver

7.4. 40G DAC cable

- QSFP 40GE to 40GE cable, 1M, 2M, 3M
- QSFP 40GE to 4 SFP 10GE fanout cable, 1M, 2M, 3M

8. Backpack Mechanical

8.1. Chassis Dimension

Backpack G4 is a standard 19-in chassis with 8 RU height.

Feature Name	Description	Comment
Chassis width	443mm (17.44”)	Width, Outer dimension
Chassis depth	749mm (29.49”)	Depth, Outer dimension
Chassis height	352mm (13.86”)	Height, Outer dimension

Table 36: Backpack chassis Dimension

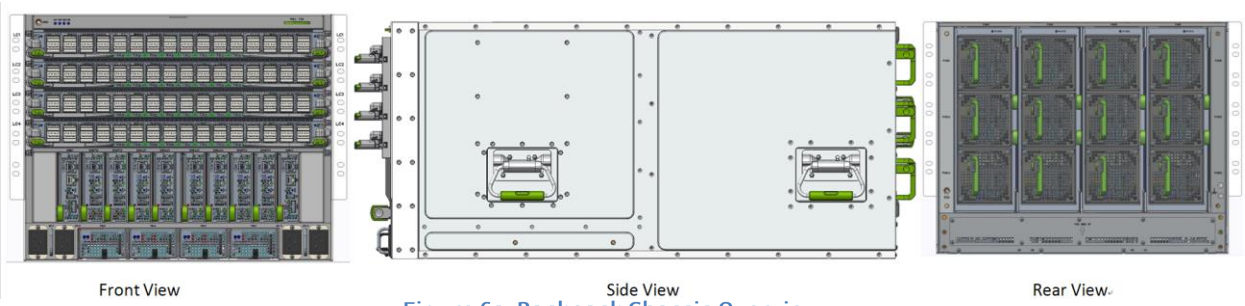

Figure 61: Backpack Chassis Overview

The following picture shows the assembly diagram of Backpack chassis.

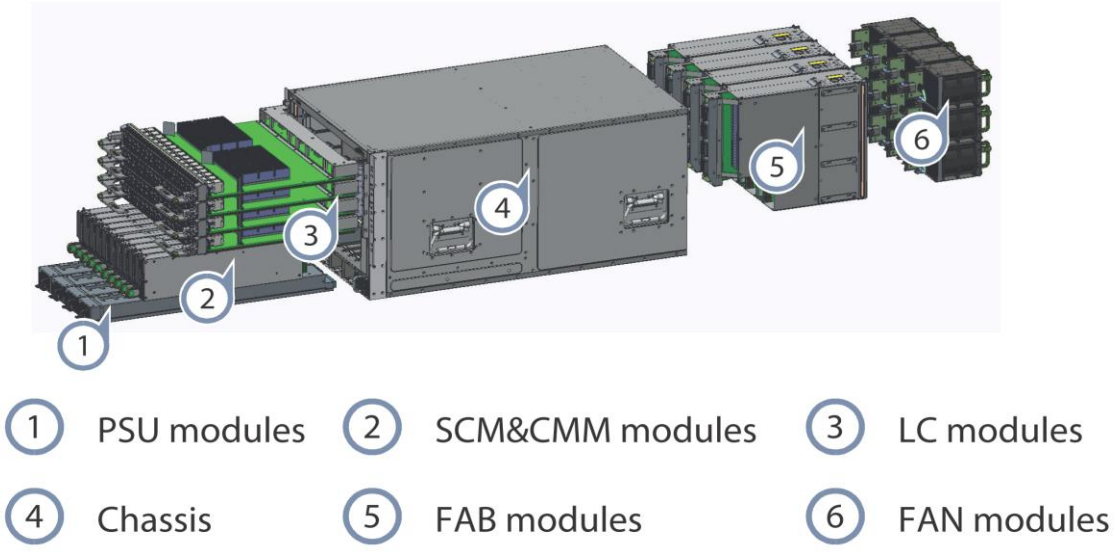

Figure 62: Backpack Chassis Assembly Diagram

8.2. Line Card (LC)

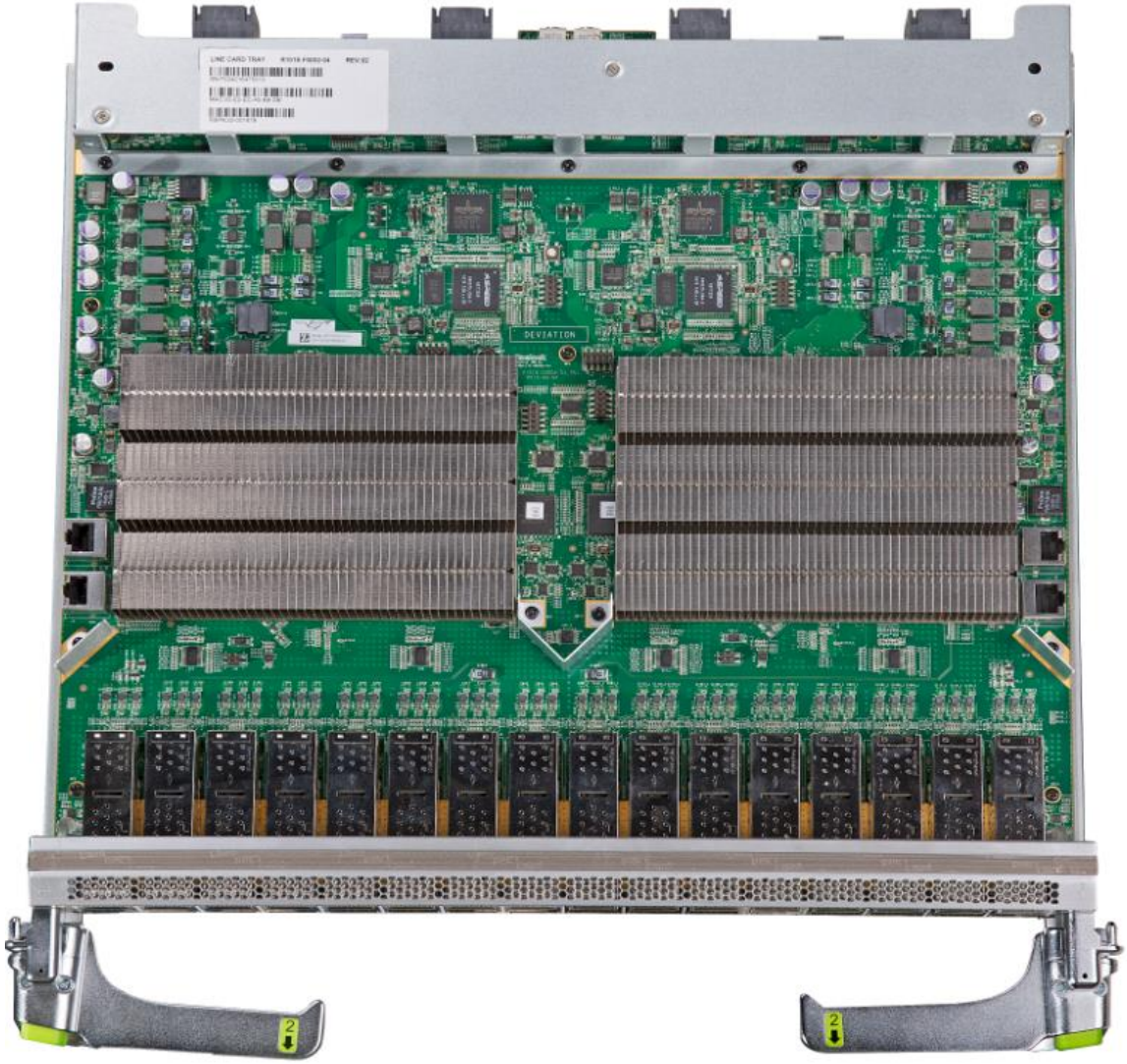

Figure 63: Line Card Top View

Figure 64: Front Pnael View of LC

8.3. Fabric Card (FAB)

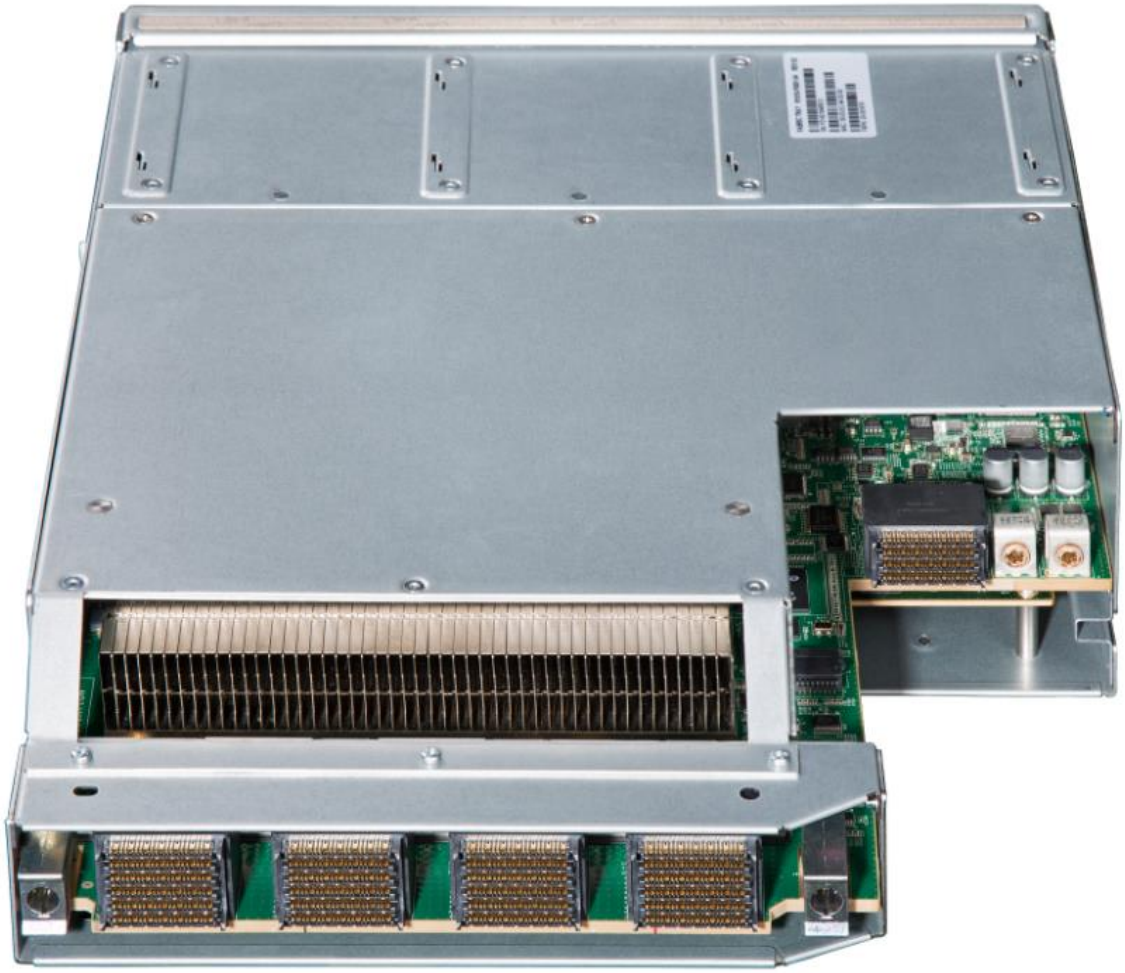

Figure 65: Fabric Card Picture 1

Figure 66: Fabric Card Picture 2

8.4. System Control Module (SCM)

Figure 67: SCM Top View

Figure 68: SCM front panel

8.5. Chassis Management Module (CMM)

Figure 69: CMM Top View

Figure 70: CMM front panel view

8.6. Horizontal Control Plane (HCP)

HCP is horizontal control plane, used to connect the 8 SCM and 2 CMM horizontally, then route those control signals to four LC via VCP-L and VCP-R, and FAB via FAB connector at the rear side of HCP.

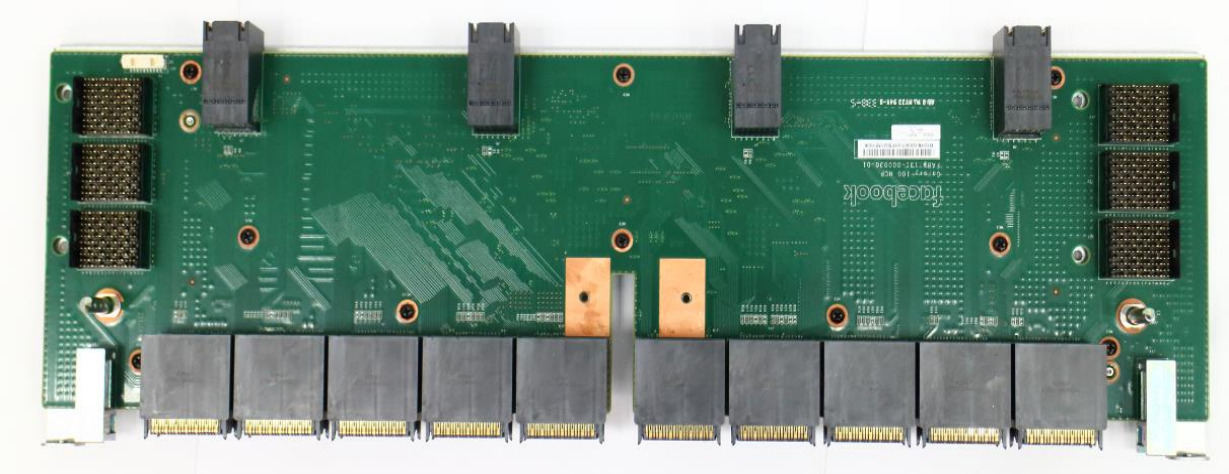

Figure 71: Horizontal Control Plane (HCP)

8.7. Vertical Control Plane (VCP)

VCP is vertical control plane, Backpack has one right VCP,(VCP-R) and one left VCP(VCP-L), VCP-R and VCP-L have the same signal connection, but mechanically they are mirrored PCB for better system air flow and enable the future 8x16 OD connector.

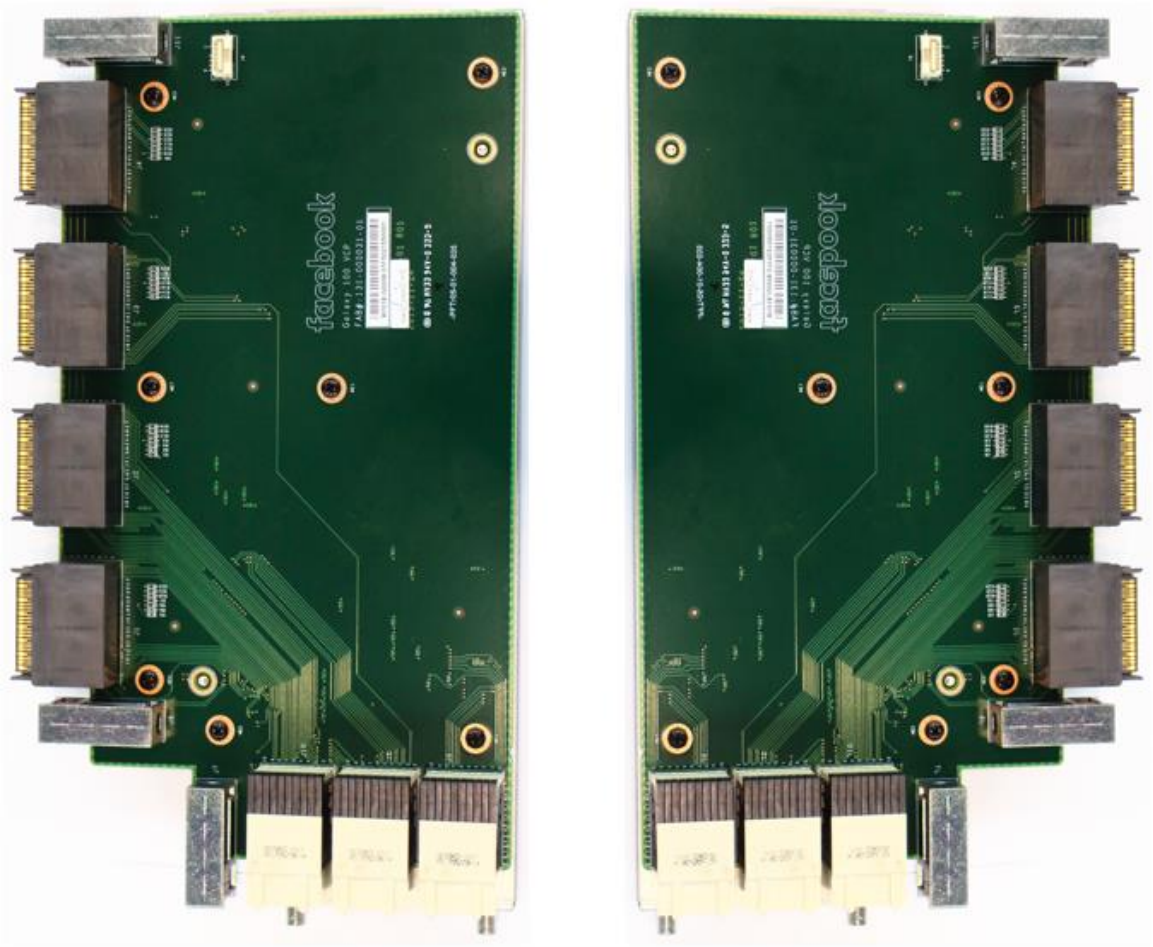

Figure 72: Vertical Control Plane (VCP): VCP-L and VCP-R

8.8. Power Distribution Board (PDB)

PDB is power distribution board, it is used to receive 4 AC input, and provide input to four PSU. CMM can access PDB via management i2c bus, enabling software to check the status of four PSU, it also provides the i2c access path to SIM card, so CMM BMC can control the SIM LED to display the chassis status to front panel SIM LED.

The following picture is PDB.

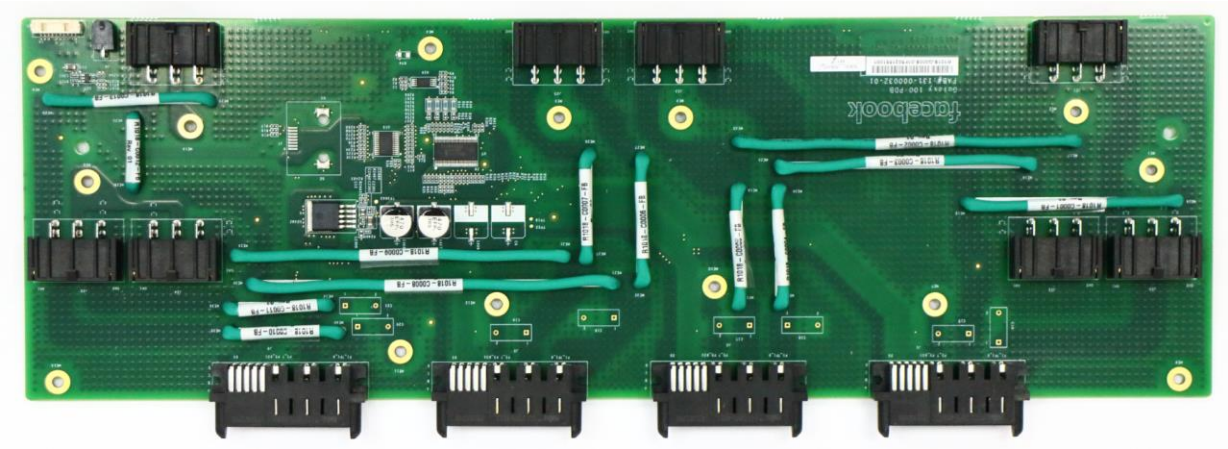

Figure 73: PDB (Power Distribution Board)

8.9. Fan Control Board (FCB)

FCB is Fan Control Board, it is a mezzanine board of FAB or FCC, and provide the fan control and status check for 3 fan-tray.

Figure 74: FCB(Fan Control Board)

8.10. Bus Bar Assembly (BBA)

BBA is Bus Bar Assembly, the following is the picture of BBA.

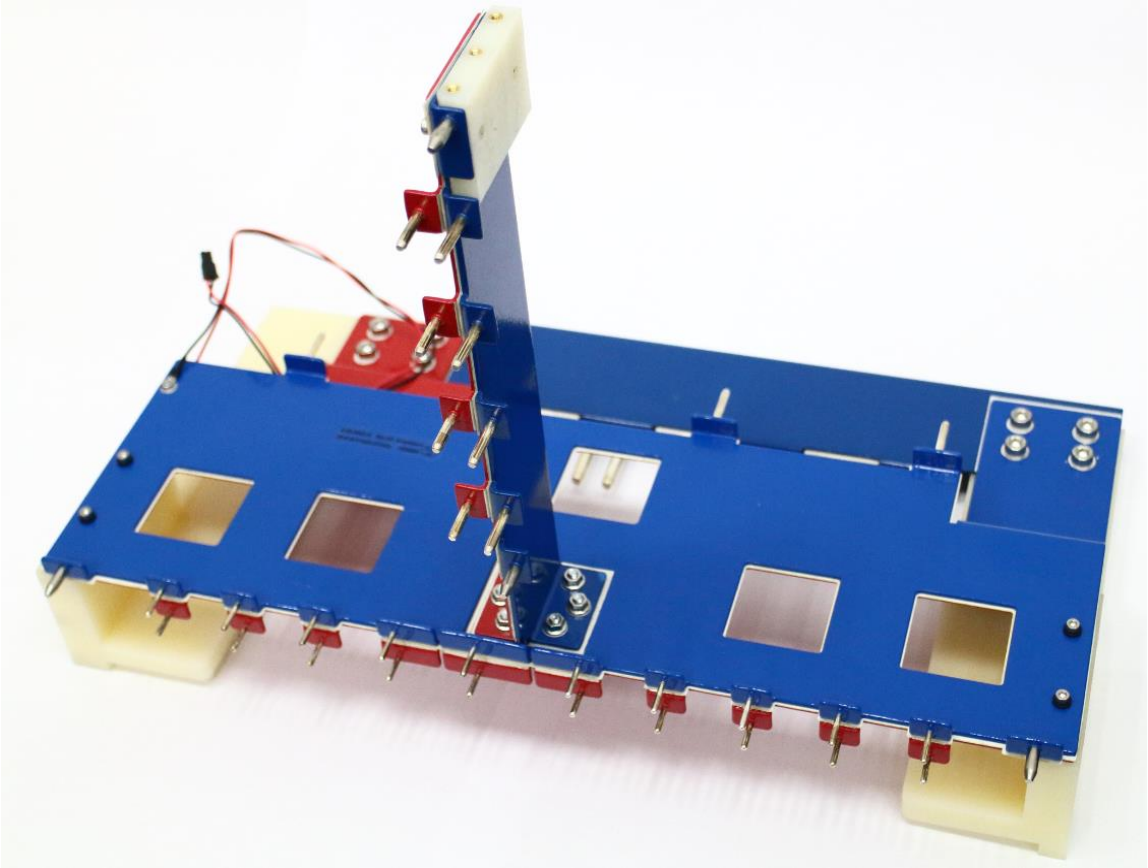

Figure 75: Bus Bar Assembly


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Compute Project

9. Host CPU and BMC Functional features

9.1. COM-Express CPU BIOS Feature List

The CPU BIOS design will follow the same requirements as the generic Micro-Server card. Highlighted key items as below:

- UEFI compatible
- Configuration and features
  - Disable unused devices
  - BIOS setup menu
  - SoC settings to allow tuning to achieve the optimal combination of performance and power consumption
- BIOS settings tools
- PXE boot
  - Supports PXE boot and provide the ability to modify the boot sequence. When PXE booting, the card first attempts to boot from the first Ethernet device (etho). If this fails, the PXE boot is attempted on the next Ethernet device.
  - PXE timeout timer set to 10 seconds
  - Default boot device priority is: Network -> M.2 SSD module -> NGFF flash card -> Other removable devices
- iSCSI network boot
- Other boot options
  - Also supports booting from SATA/SAS and USB interfaces
  - Provides the capability to select boot options

  Remote BIOS update
  - BMC can upgrade COM-E SPI booting flash via SPI bus.
- Logged errors
  - CPU / memory errors
  - PCI-E errors
  - SATA errors
  - POST errors
  - System reboot events
  - Sensor values exceeding warning or critical thresholds
- Error thresholds
  - Setting must be enabled for both correctable and uncorrectable errors
  - Threshold for Memory Correctable ECC is TBD
  - PCI-E error, follow chipset vendor's suggestion

  POST codes
  - To be displayed on debug card
  - To be provided on the serial console

9.2. BMC Feature Support

The BMC on Backpack modules need to support the following features:

- All SEL commands

- All sensor commands
- All SDR commands
- Power on/off/cycle / hardware reset / soft reset commands
- I2C access to Power Sequencer, and DC-DC convertor
- Inventory EEPROM access
- Fan-tray present status check, fan PWM control and speed status read
- Dual SPI boot
- On-board OOB switch MDIO interface access
- On-board PHY MDIO interface access
- CPLD online upgrade(disabled in MP)

10. Environmental Requirements and Reliability

10.1. Environmental Requirements

The Backpack chassis should support the related system(s) to meet the following environmental requirements:
Gaseous contamination: Severity Level G1 per ANSI/ISA 71.04-1985
Operating and storage relative humidity: 10% to 85% (non-condensing)
Storage temperature range: -40°C to +70°C (long-term storage)
Transportation temperature range: -55°C to +85°C (short-term storage)
Operating altitude with no de-rating to 1,000m (3,300 feet)

10.2. Vibration and Shock

Operational Sine Vibration Test

Reference : GR-63 Core .i04

Frequency Range(Hz)	5~100~5
Acceleration(m/s^2)	0.981
Duration	90 minutes/axes, 3 axis
Sweep rate	0.1 oct/minute

10.3. Unpackaged Drop Test

The unpackaged drop tests consist of rotational and free-fall drops.

Reference:

GR_3108_CORE.i02

GR_63_CORE.i04

Test Level:

Mass	Drop Height
0 to <10 Kg	100 mm
10 to <25 Kg	75 mm
25 to <50 Kg	50 mm
>=50 Kg	25 mm

IEC 68-2-36, IEC 68-2-6

10.4. Mean Time Between Failures (MTBF) Requirements

TBD

10.5. Regulations

The Backpack chassis should support the related system(s) to obtain CB reports by the vendor(s). Facebook will need these documents to have rack level CE.

Environment	
Temperature	0 to 45C, sea level with 70C Optics; 35C, sea level with 55C optics
Humidity	Relative humidity: 5% to 85% in operation, non-condensing
Storage	5km
Acoustic	<70dbA
Vibration	IEC 68-2-36, IEC 68-2-6
Environment Regulatory Compliance	Must Comply with ROHS requirement through 2017
Regulatory and Safety	
Safety	CAN/CSA-C22.2 NO. 60950-1-07
	UL 60950-1 (2nd Edition), am 1(2011)
	IEC 60950-1 (2nd Edition), Am 1:2009
	EN 60950-1:2006 + A11:2009 + A1:2010 + A12:2011
	EN 60825-1:2007
	EN 60825-2:2004+A1
	ZEK 01.4-811.11 (For GS)
EMC	FCC Title 47 CFR, part 15, Subpart B, 2012 (for frequency > 1G) Class A
	ICES-003: 2012 Issue 5(Canada)Class A
	VCCI V-3:2013.04 /V-4:2012.04 (Japan) Class A
	AS/NZS CISPR 22:2009+A1:2010 (Australia/New Zealand) Class A
	EN 55022:2010+AC: 2011 Class A

	EN 61000-3-3:2008
	EN 55024:2010
	EN 300 386 (V1.6.1):2012
	IEC 61000-4-2: 2008 (Criteria A)
	IEC 61000-4-3: 2010 (Criteria A)
	IEC 61000-4-4: 2012 (Criteria A)
	IEC 61000-4-5: 2005 (Criteria A)
	IEC 61000-4-6: 2008 (Criteria A)
	IEC 61000-4-8: 2009 (Criteria A)
	IEC 61000-4-11: 2004 (Criteria A/A/C)

Table 37: Regulatory Requirements

11. Labels and Markings

11.1. PCBA Labels and Markings

Backpack PCBAs shall include the following labels on the component side of the boards. The labels shall not be placed in such a way that may cause them to disrupt the functionality or the airflow path of the system.

Table 38 PCBA Label Requirements

Description	Type	Barcode Required?
Safety markings	Silkscreen	No
Vendor P/N, S/N, REV (revision would increment for any approved changes)	Adhesive label	Yes
Vendor logo, name & country of origin	Silkscreen	No
PCB vendor logo, name	Silkscreen	No
Facebook P/N	Adhesive label	Yes
Date code (industry standard: WEEK/YEAR)	Adhesive label	Yes
DC input ratings	Silkscreen	No
RoHS compliance	Silkscreen	No
WEEE symbol:  The motherboard will have the crossed out wheeled bin symbol to indicate that it will be taken back by the manufacturer for recycling at the end of its useful life. This is defined in the European Union Directive 2002/96/EC of January 27, 2003 on Waste Electrical and Electronic Equipment (WEEE) and any subsequent amendments.	Silkscreen	No

11.2. Chassis Labels and Markings

TBD

12. Appendix

12.1. Appendix: Commonly Used Acronyms

This section provides definitions of acronyms used in the system specifications.

ANSI – American National Standards Institute

BIOS – basic input/output system

BMC – baseboard management controller

CFM – cubic feet per minute (measure of volume flow rate)

CPLD – complex Programmable Logic Device

DCMI – Data Center Manageability Interface

DDR3 – double data rate type 3

DHCP – dynamic host configuration protocol

DIMM – dual inline memory module

DPC - DIMMs per memory channel

DRAM – dynamic random access memory

ECC – error-correcting code

EEPROM - electrically erasable programmable read-only memory

EMI – electromagnetic interference

FRU – field replaceable unit

GPIO – general purpose input output

I²C – inter-integrated circuit

IPMI – intelligent plattform management interface

LPC – low pin count

MAC – media access control

MTBF – mean time between failures

MUX – multiplexer

NIC – network interface card

OOB – out of band

PCB – printed circuit board

PCIe – peripheral component interconnect express

PCH – platform control hub

POST – power-on self-test

PSU – power supply unit

PWM – pulse-width modulation

PXE – preboot execution environment

QSFP – Quad small form-factor pluggable

QSFP28 – Quad small form-factor pluggable for 4x28Gbps.

RU – rack unit (1.75”)

SAS – serial-attached small computer system interface (SCSI)

SATA – serial AT attachment

SCK – serial clock

SDA – serial data signal

SDR – sensor data record

SFP - small form-factor pluggable

SMBUS – systems management bus

TOR – top of rack

TPM – trusted platform module

COM-e: COM express Module