Edgecore AS7726-32X

Switch Specification

Revision 1.0

OPEN
Compute Project

Revision History

Revision	Date	Author	Description
1.0	9/10/2018	Jeff Catlin	Initial Draft

Contents

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Component	Vendor	MFG P/N	Quantity	Remark
CPU Board-CPU	Intel	Broadwell-DE XeonD-1518	1	
MAC	Broadcom	BCM56870	1	
NIC	Broadcom	BCM5720	1	
EMP PHY	Broadcom	BCM54616S	1	
CPLD	Altera	5M1270	1	For CPU system
CPLD	Altera	5M1270	1	For Main board System
CPLD	Altera	5M1270	2	For QSFP28 LED
I2C Switch	NXP	PCA9548APW	7	
Thermal Sensor	NS	LM75BD/SO8	4	
USB HUB IC	SMSC	USB2514B-AEZC	1	
Power Monitor	Lattice	POWR1014A	1	
UART IC	TI	MAX3232CPWR	1	Transceiver
PSU (AC/DC)	3Y	YM-2651Y	1	650W AC

Scope

This document outlines the technical specifications for the Edgecore AS7726-32X Open Switch Platform submitted to the Open Compute Foundation.

Overview

This document describes the technical specifications of the AS7726-32X Switch designed by Edgecore Networks Corporation. The AS7726-32X is a cost optimized design focused Top of Rack and/or Spine layer usage providing 10G/25G/40G/100G connectivity.

The AS7726-32X supports thirty two QSFP28 ports and two SFP+ ports for network connectivity.

The AS7726-32X is a PHY-Less design with the network interface connections directly attaching to the Serdes interfaces of the Broadcom 56870 switching silicon providing the lowest cost, latency, and power. The AS7726-32X supports traditional features found in switches such as:

- Redundant field replaceable power supply and fan units
- Support for "Front to Back" air flow direction
- Supports a modular CPU card that allows flexibility in the CPU and/or memory configurations that can be offered.
- Support for AC or DC power supply units

1. Introduction

The AS7726-32X is a 1U high and 515mm deep switch based on Broadcom Trident3 chipset. The physical layer consists of 32 100G QSFP28 ports and 2 10G SFP+ ports. The switch has a nominal operating temperature range of 0 to +45 Degree C.

The CPU board is based upon the Intel BroadWell-DE which provide the following interfaces: x4 PCIe2.0, SGMII, MDC/MDIO, USB2.0, and 2channel I2C connect to the switch board. There are mSATA and eUSB devices in the CPU board and memory support DDR4 with ECC sodimm.

The following are key features of the product:

- Redundant and hot-swappable PS (1+1)
- Front facing for all connections
- Redundant and hot swappable fans (5+1)
- 1U rank mountable
- 32 QSFP28 40G/100G ports
- CPU module
  - CPU: Intel Broadwell-DE XeonD-1518
  - DDR SDRAM: 8GB x 2 2133MHz with ECC (DDR4 SO-DIMM)
  - SPI Flash (Boot): 16MB
  - USB to NAND Flash memory : 8GB SLC
  - mSATA: 32GB MLC (Reserve)
  - m.2: 32GB MLC (Reserve)
- USB port (5V/1A)
- SyncE & 1588 support
- Environmental 0 to +45 degree C operation

1.1. Reference Documents

- Broadcom **BCM56870** Data Sheet
- IDT**89307** WANPLL Data Sheet
- 544040_Broadwell_DE_EDS_vol1_544040_rev1p0.pdf
- 544041_Broadwell_DE_EDS_Registers_Vol2_544041_v1_0.pdf
- 544042_Broadwell_DE_SoC_EDS_vol3_544042_v1_0.pdf
- 544043_Broadwell_DE_EDS_rev_0_75.pdf
- 544044_Broadwell_DE_EDS_Vol5_544044_rev0_71.pdf
- BCV-R-SB_SCH_20140804.pdf
- CamelBackMnt_FAB-B_NCOR2_09-09-14.pdf

1.2. Acronyms and Terminology

POR Power On Configuration

PSUPower Supply Unit

2. Hardware Architecture

2.1. Overview

The AS7726-32X provides 32 x 100G QSFP28 ports, 2 x 10G SFP+ ports directed by a mux function, dedicated 1G management port, USB, and serial console port.

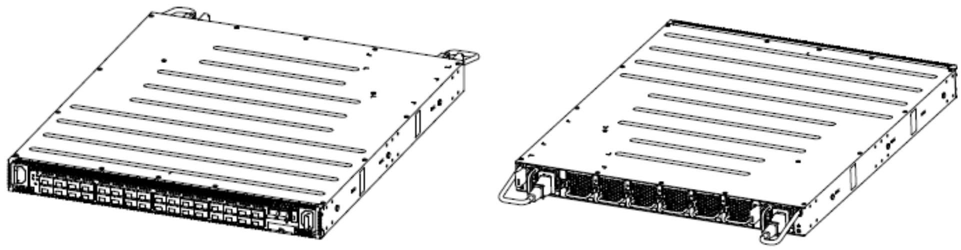

Table 2-1 System Overview

AS7726-32X	
CPU sub-system	CPU: **Intel Broadwell-DE XeonD-1518** DDR SDRAM: **8GB x 2 2133MHz with ECC (DDR4 SO-DIMM)** SPI Flash (Boot): **16MB x 2** USB to NAND Flash memory : **8GB SLC** mSATA: **32GB MLC (Reserve)** m.2: **32GB MLC**
Management	UART RS232 console port (RJ45), Out-band Management Ethernet port (RJ45)
USB	One type-A USB port at front panel, support USB 2.0 (480Mbps)
CPLD	CPLDs access by I2C and CPLDs code field upgraded by CPU GPIO
RJ45 LED X'FMR	One RJ45 with LED and X'FMR embedded
MAC	Broadcom Tomahawk BCM56870, 1 pcs, 3200Gbs multi-layer Ethernet switch controller
NIC	1 x BCM5720
EMP PHY	1 x BCM54616S
Ethernet Ports	32x QSFP100 ports and 2 x SFP+ ports(option)
PCB	12-Layers for CPU module 14-Layers for Mainboard 4-Layers for FAN board
Power Supply	650W PSU back to front airflow, AC to DC ; front to back airflow, DC to AC), 1+1 redundant load-sharing, hot-swappable +12V/52.9A output / +5Vsb/4A output

AS7726-32X	
Cooling	6 fan-tray modules with 6 pcs of 40mm x40mm x 56mm 12V fans, hot-swappable; 5+1 FAN redundancy
System LED	Driving by CPLD
100G/40G/25G/10G LED	Driving by MAC LED stream
Push Button	One push button for reset at front panel
Dimension	515 mm (L: Depth) x 438.4mm (W: Width) x 43.5 mm (H: Height maximum)
Mounting Options	Rack Mount

Table 2-2 Key component Table

Component	Vendor	MFG P/N	Quantity	Remark
CPU Board-CPU	Intel	Broadwell-DE XeonD-1518	1	
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Power Monitor	Lattice	POWR1014A	1	
UART IC	TI	MAX3232CPWR	1	Transceiver
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2.2. Block Diagram

The AS7726-32X provides 32 x 100G ports and 2 x 10G ports on the board and supports1 x 1G port for management and control. It is formed by **BCM56870**, a 32 Falconcore with maximum 3.2T switch capacity. The BCM56870 is connected to CPU module via PCIe Gen2.0 x 4 bus. The host system includes two banks of 8GBDDR4 SO-DIMM, 16MB boot Flash, Watchdog timer, Thermal detector, SYNC Ethernet and other glue logic.

The Merlin core of BCM56870 can provide 2 x 10G channels, which are connected through a multiplexer with either CPU board or SFP+ front ports.

The Base unit uses 12VDC and 5VDC from the Hot swappable Power module. The on-board DC/DC is used to generate 3.3V/ 1.8V/1.2V/ 1.2V/ 0.8V/1.0V(ROV) from 12VDC.

Figure 2-1 Switch board Block Diagram

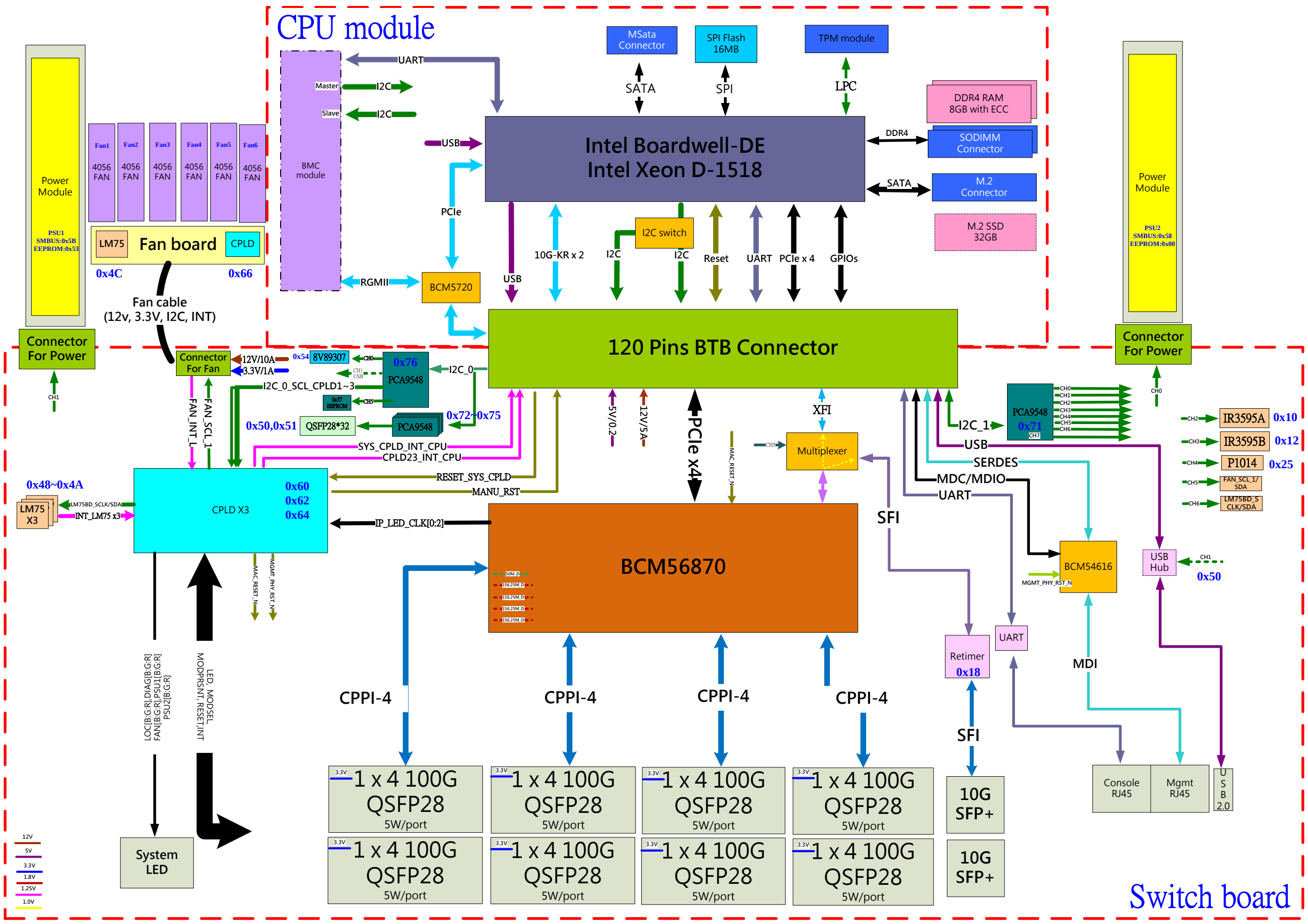
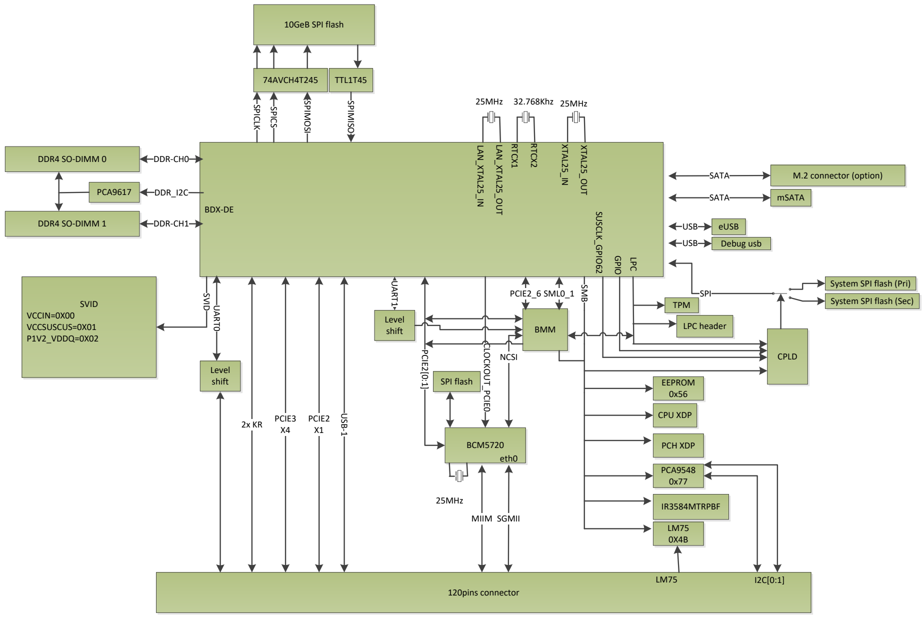


Figure 2-2 CPU board Block Diagram



2.2.1. Clock Tree

The AS7726-32X supports Synchronous logic which consists of Network Interface Synchronizer chip, Jitter attenuators and clock buffers. The key component is a Network Interface Synchronizer chip. The Network Interface Synchronizer chip selects a reference clock from one of two valid clock sources generating a Stratum 3 compliant reference clock for the Broadcom Trident chip. This clock is also used as a transmit reference clock for all external interface ports. This logic consists of a IDT 89307 Network Interface Synchronizer chip and Oven controlled crystal oscillator. This synchronizer chip when properly configured will produce 25MHz and 156.25MHz clock which is frequency locked to a selected port recovered clock.

The IDT 89307 is configured through an I2C interface, it reports major state information via a number of status and control signals.

Figure 2-3 Switch board clock Tree

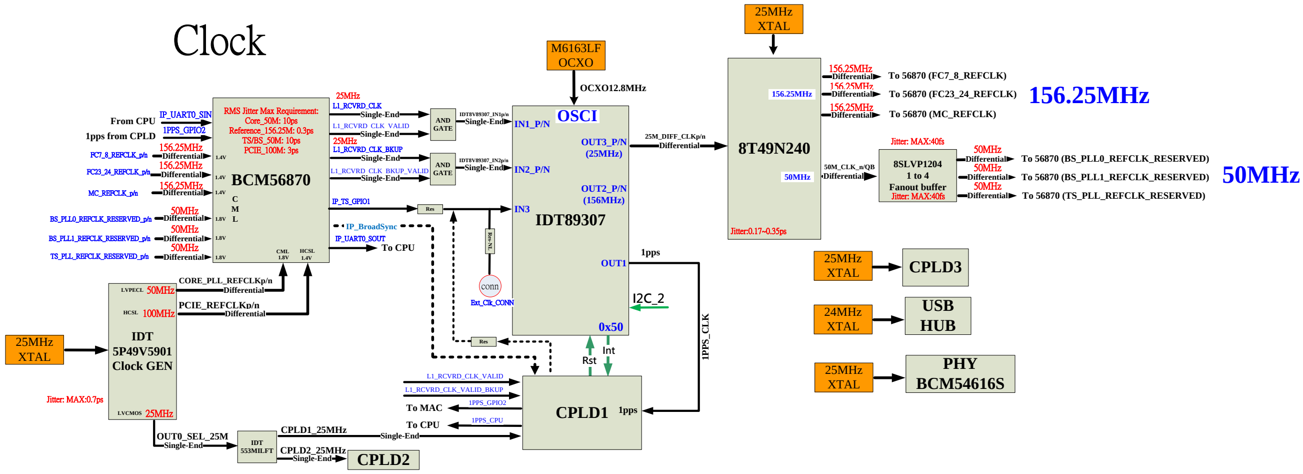
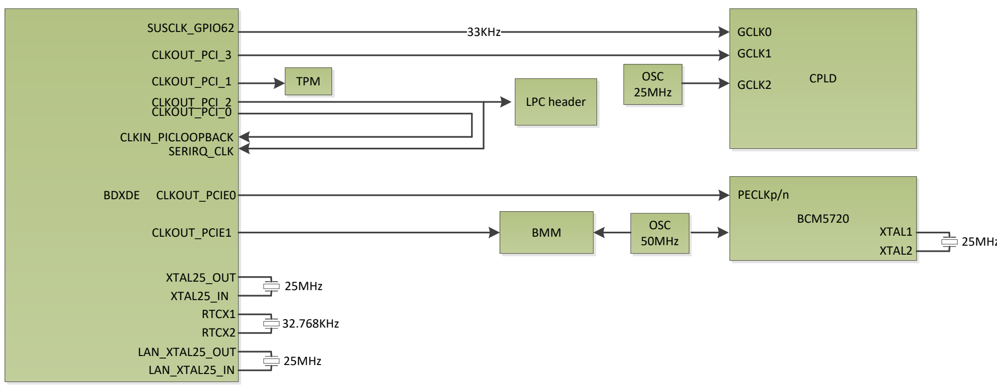


Figure 2-4 CPU board clock Tree



2.2.2. Power Tree

Based on the power estimation in Table 2, we have selected a suitable DC/DC with the best efficiency as possible.

In addition to convert the voltage from SPS, the regulation of each voltage is also very important. Each DC/DC is monitored to alarm the system through backplane connector if there is any DC/DC lower than monitored threshold. The power supply can support 12V output and standby 5V output, but the system only uses 12V output to be converted to other low system voltage.

The DC/DC is also shut down when the temperature is higher than the shutdown threshold of the thermal sensors.

The system power sequence is starting from high voltage to low voltage.

The following is about the power tree topology.

Figure 2-5 Switch board Power Tree

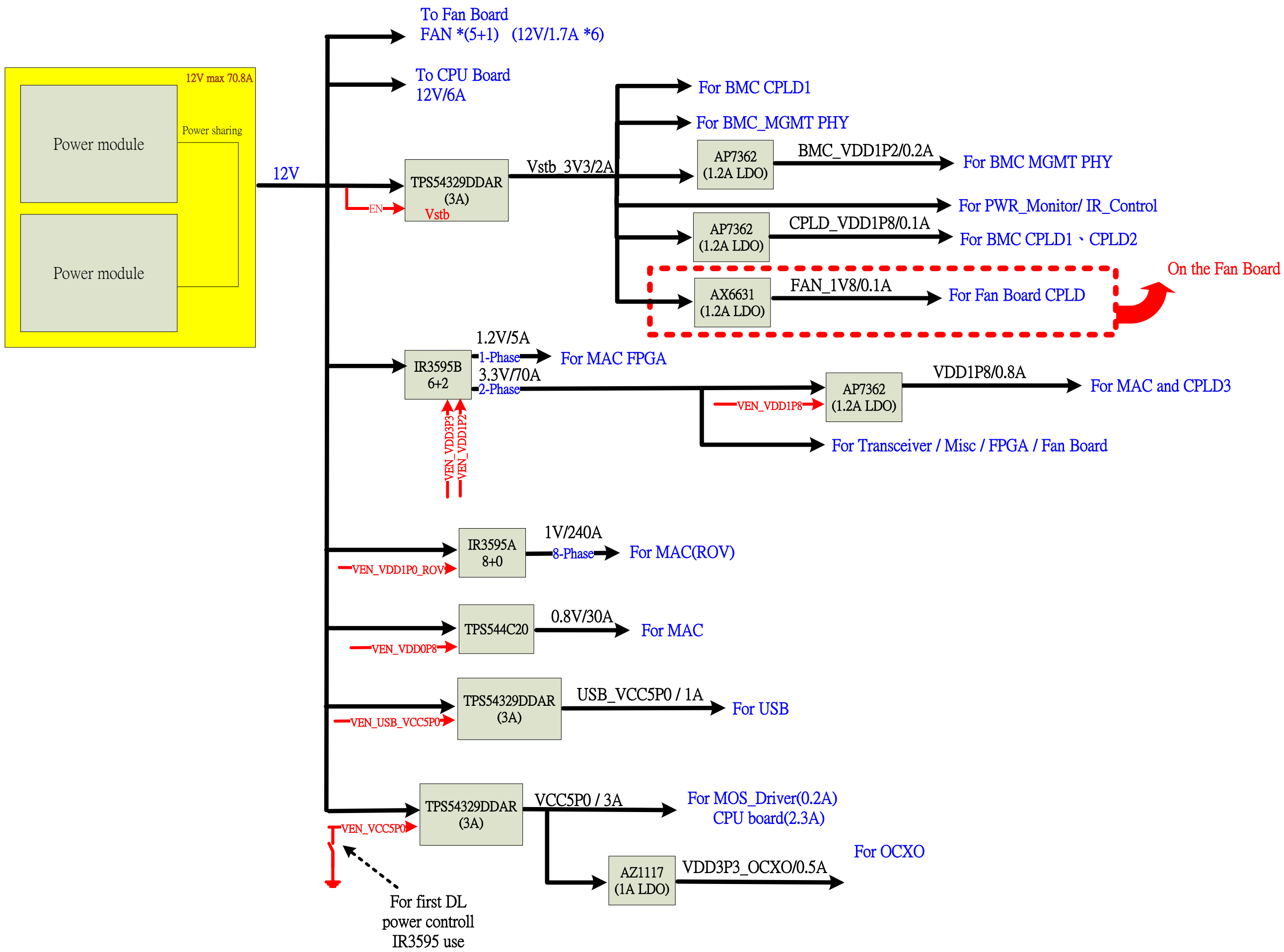
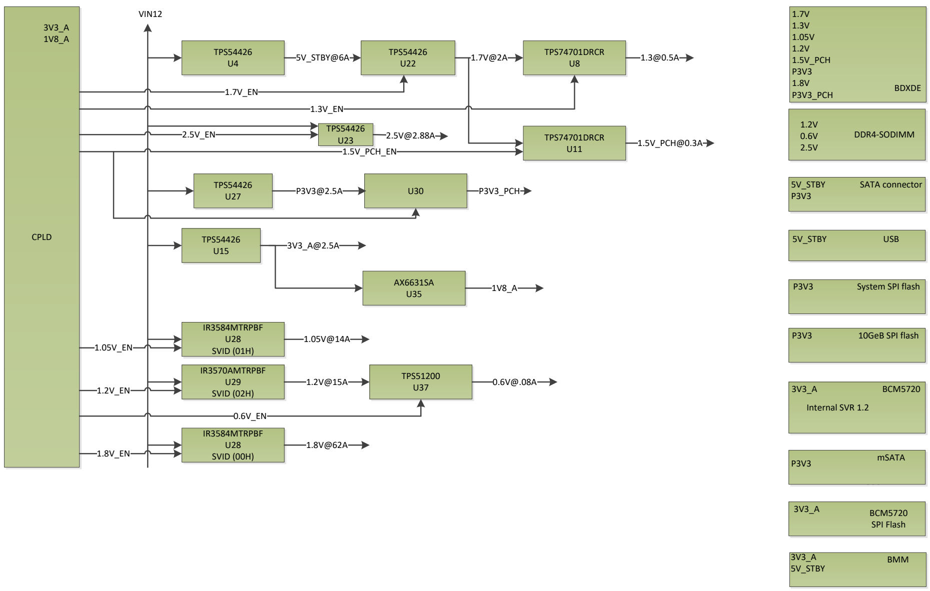


Figure 2-6 CPU board Power Tree



2.2.3. Reset Tree

The reset system will follow as below.

1. The CPU board and switch board will be power on. And the reset monitor IC will check DC power voltage if reach the threshold.
2. The monitor IC will send Power_RST signal to CPLD if all power is OK.
3. CPLD pass the MANU_RST signal to CPU board, and hold the all reset signals of switch board's device
4. CPU get the switch board's MANU_RST signal from switch board's CPLD, it means switch is ready to boot up. CPU board will check itself status and pull up Reset_SYS_CPLD signal to switch's CPLD to boot up switch board.
5. When switch's CPLD get the Reset_SYS_CPLD signal, switch's CPLD will pass to all device on switch to boot up device.
6. When the system running, the switch's CPLD has different register for every device's rest signal. CPU can reset switch's device separately via switch's CPLD register.

If CPU the wants to reset itself without main board system, CPU can set "1" in "reset_lock" register of main board's CPLD1 (0x0B).Main board CPLD1 will block "reset_sys_cpld" signal to CPLD1, and main board CPLD1 will send "reset_lock" signal to CPU to indicate the "reset_lock" register status. The default value of "reset_lock" register is "0".
The following is about the reset tree topology.

Figure 2-7 Switch board Reset Tree

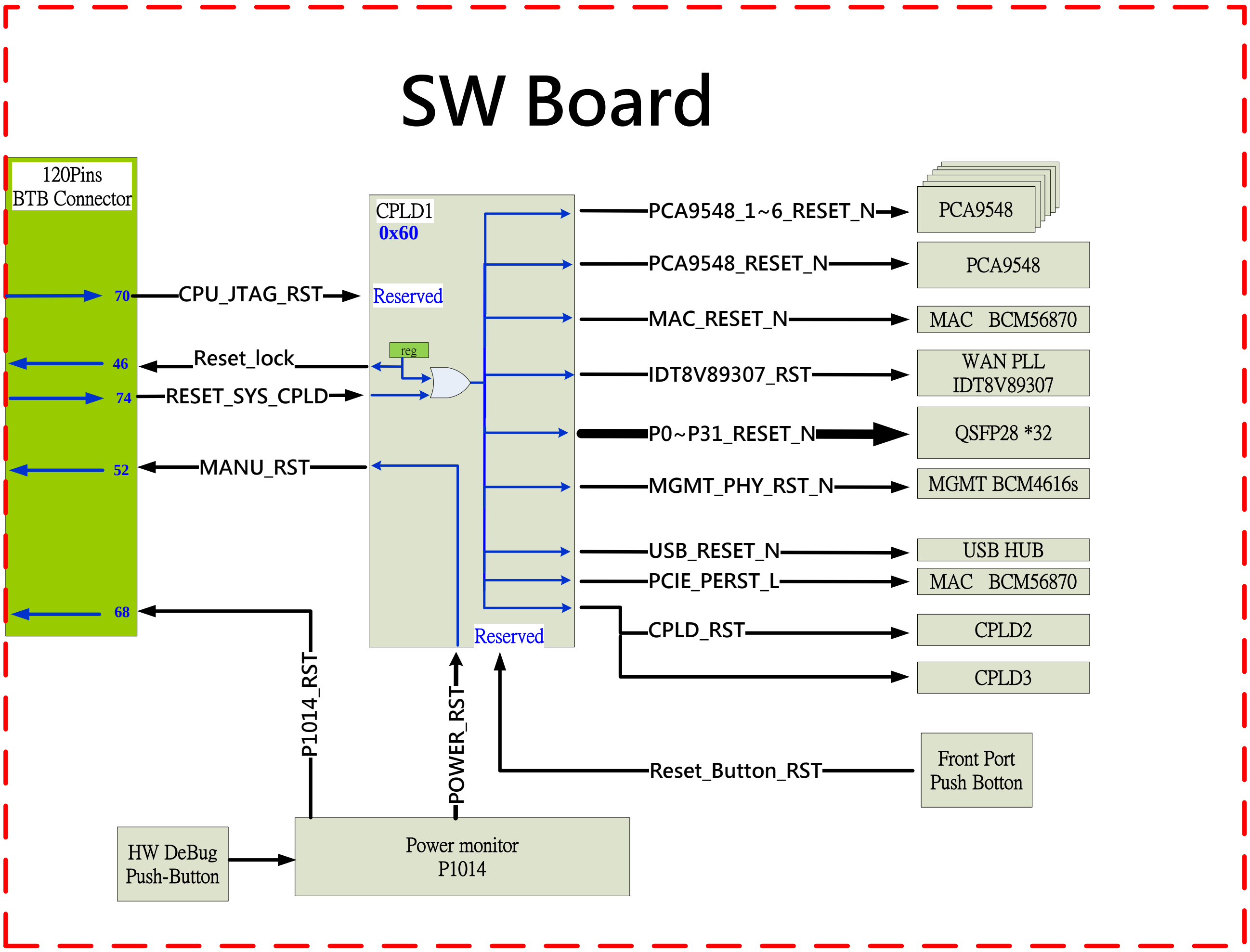
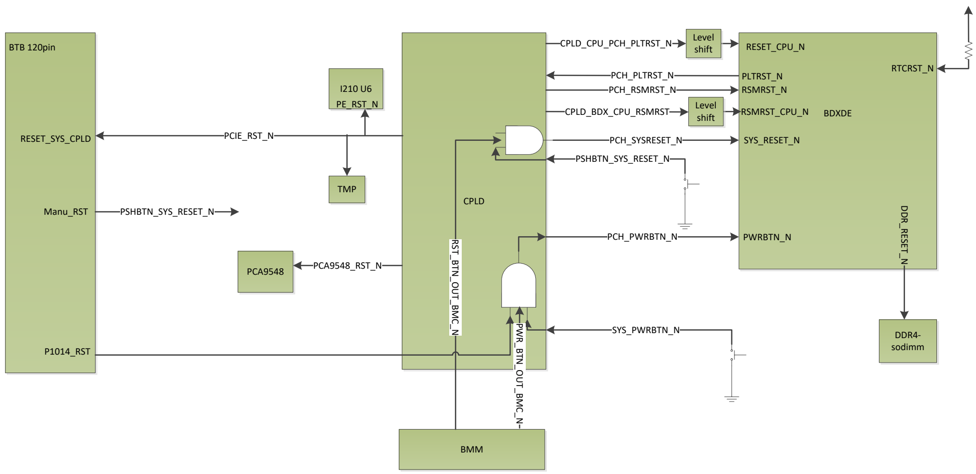


Figure 2-8 CPU board Reset Tree



2.2.4. Others

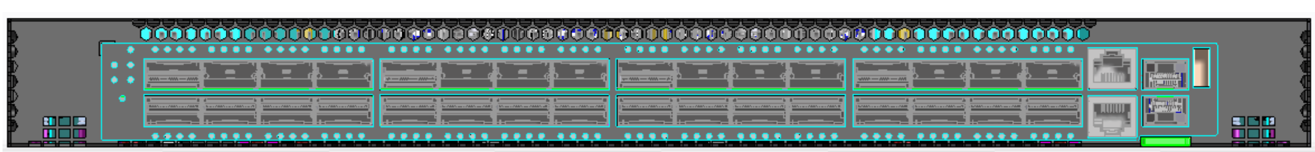
2.3. LED Indicator

The system has 5 status LEDs and 130 port LEDs. The 5 status LEDs are for PWR1, PWR2, Fan, Alarm and LOG. The 128 port LEDs are for 32 40G/100G Ethernet ports and 2 port LEDs are for 1G/10G SFP+ ports.

The 5 system LEDs are on left side.

The port numbering scheme on the front panel is starting from 0 to 31, even on top, odd on bottom, left to right.

Figure 2-9 Front panel



2.3.1. Status LED

Figure 2-10 Status LED

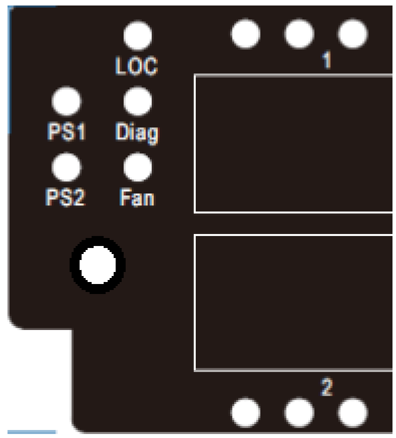


Table 2-3 Status LED Definition

LED	Color	Mode
Power Supply 1	Red	Error/Failure/Bad
	Green	Good
	Off	Not present
Power Supply 2	Red	Error/Failure/Bad
	Green	Good
	Off	Not present
FANs	Red	Error/Failure/Bad
	Green	Good
Diag	Red	Error/Fault/Failure
	Green	Good
	Blinking Green	System boot in progress
LOC	Red	TBD
	Green	TBD
	Blue	TBD
	Off	TBD

2.3.2. Port LED

There are 128 bi-color(Green/Yellow) LEDs for 100G QSFP 32 ports, with 4 lanes per port and 2 bi-color (Green/Yellow) LED for SFP+ 2 ports, so 1 bi-color LED indicates 1 SFP+ port or 1 Lane per QSFP port. The QSFP28 port can run in 40G/4x10G or 100G/4x25G breakout mode. Note: The LEDs flash to indicate activity.

Figure 2-11 Port LED

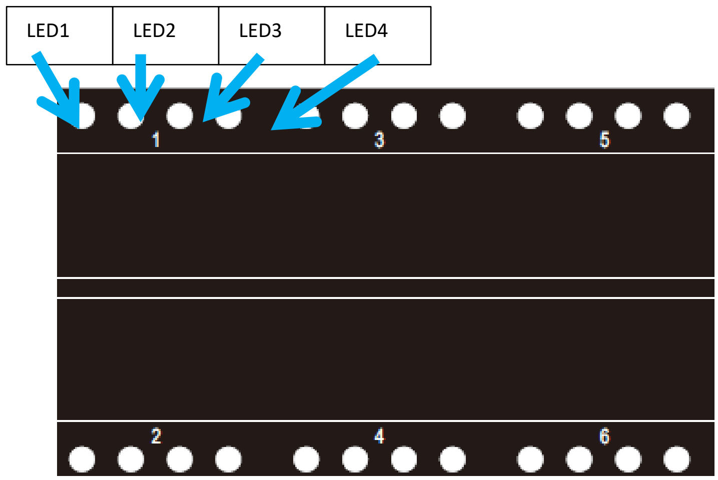


Table 2-4 Port LED Definition

LED	Color	Mode
LED 1	Blue	100G (4 x 25G)
	Orange	40G (4 x 10G)
	White	25G
	Green	10G
	off	not present
LED 2~4	White	25G
	Green	10G
	off	not present

The CPLD drives the R/G/B LED by de-coding the MAC's LED bus.

2.3.3. Management Port LED

The management port support 1G/ 100M / 10M speed. Two port LEDs are reserved and integrated into the RJ-45, yellow at the left side and green at the right side.

Figure 2-12 Management Port LED

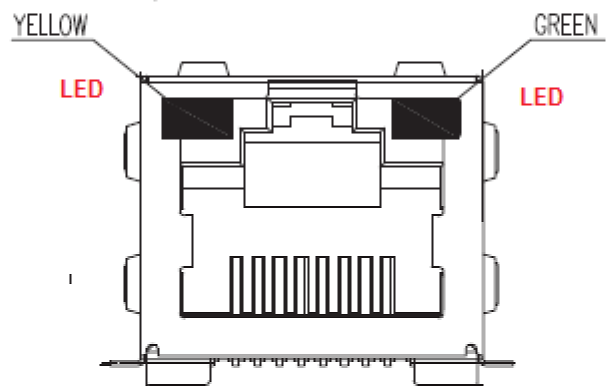


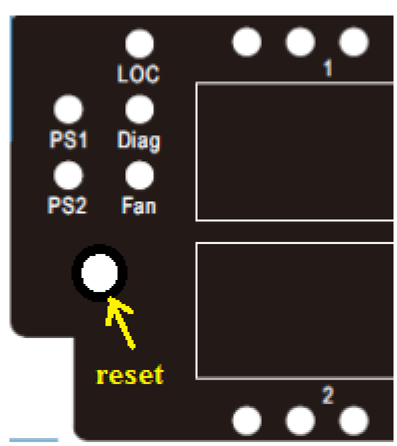
Table 2-5 Management Port LED Definition

LED	Color	Mode
LED	Green	TBD
	Yellow	TBD
	off	TBD

2.3.4. Button

A reset button is reserved on the front panel to reboot the system.

Figure 2-13 Front reset button



3. CPU Sub-system

3.1. Configurations of CPU

- 2 DDR channels support DDR4 ECC and non-ECC UDIMM, SODIMM, RDIMM
- Memory speed : DDR4 1600, 1867, 2133, 2400 MT/s
- PCI Express Lanes :
  - 24Gen3, 1x16 and 1x8, 6 controllers x4 granularity (Uncore)
  - 8 Gen2, 2x4, 8controlles x 1 granularity (Integrated PCH logic)
- Integrated 10GbE Controller contains two independent 10GbE MACs that support an XGMII interface link to the either KX4 or KR PHY device interfaces.
  - KX4 PHY supports
    - XAUI for XGMII extension
    - 10GBASE-KX4 for gigabit backplane applications.
    - 2500BASE-KX for gigabit backplane applications.
    - 1000BASE-KX for gigabit backplane applications.
  - KR PHY supports
    - 10GBASE-KR for gigabit backplane application
    - 1000BASE-KX for gigabit backplane application.
    - 10GBASE SFP+ through a XFI compatible interface
    - 10GBASE-T through a XFI compatible interface
- Integrated PCH logic
  - PCI Express Base specification, revision 2.0 support for up to eight ports with transfers up to 5GT/s
  - ACPI power management logic support revision 4.0a
  - Enhanced DMA controller, interrupt controller, and timer function.
  - Integrated Serial ATA host controllers with independent DMA operation on up to six ports.
  - xHCI USB controller provides support for up to 4 USB ports, of which four can be configured as SuperSpeed USB 3.0 ports.
  - One legacy EHCI USB controller provides a USB debug port.
  - Integrated 10/100/1000 Gigabit Ethernet MAC witch system defense.
  - System Management Bus (SMBus) specification, version 2.0 with additional support for I2C devices
  - Supports intel Virtualization Technology for Directed I/O (Intel VT-d)
  - Supports intel Trusted Execution Technology (Intel TXT)
  - Integrated clock controller
  - Low Pin Count (LPC) interface
  - Firmware Hub (FWH) interface support
  - Serial Peripheral Interface (SPI) support
  - JTAG Boundary scan support.

3.1.1. POR of CPU

The cores and uncore supports the following reset types. Note PWRGOOD_CPU is driven by the PCH.

Cold reset is the first time when the platform asserts PWRGOOD_CPU and asserts RESET_CPU_N to the uncore. The platform has to wait for the Base Clock (BCLK) and the power to be stable before asserting PWRGOOD_CPU. This results in reset of all the states in the processor, including the sticky state that is preserved on the other resets. PLLs come up, I/O (DMI2,uncore PCI Express, and DDR) links undergo initialization and calibration. Components in fixed and variable power planes are brought up. Ring, router, SAD, and various lookup tables in the core/Cbo are initialized. Once the uncore initialization has completed, then the power is enabled to the cores and cores are brought out of reset. BIOS is fetched from the PCH.

Warm reset is typically a platform wide event and is indicated by assertion and deassertion of the RESET_CPU_N signal on the socket while PWRGOOD_CPU remains asserted. This reset preserves the error log state and machine check bank states for use by platform debug. The warm reset preserves the error log state and machine check bank states for use by platform for post error event analysis. To maintain the DDR memory attached to the processor self refresh and sticky registers remain valid through out a warm reset, the "Reset_warn" message must complete by the processor. The "Reset_warn" is a message that gets issued from the PCH to all sockets prior to warm reset. BIOS will need to program the FlexRatioMSR/CSR in each socket and invoke the Warm Reset to the platform.

The reset flow is divided into the following 5 phases.

- Phase 0: Expectations from the platform (before assertion of PWRGOOD_CPU)
  - Initially PWRGOOD_CPU signal is deasserted and RESET_CPU_N is asserted to the socket. PWRGOOD_CPU cannot deassert until RESET_CPU_N is asserted.
  - PWRGOOD_CPU must be asserted no sooner than 2 ms after the IVR Vccin supply has fully ramped-up.
  - Vccioin may be brought up before Vccin for IVR is brought up if not at the same time. Vccioin is intended to source the PECI IO.
  - The PWRGOOD_CPU and RESET_CPU_N signals have "clean" edges.
  - The reference clock (BCLK) is stable.
  - All external power rails have ramped as follows: Vccin, Vccioin, VCCD are up and stable at their nominal values
  - Assert PWRGOOD_CPU (RESET_CPU_N still asserted) only after 2 msec of Vccin, Vccioin and VCCD at tolerance.
  - After the power rails are up and stable for 2 msec and reference clocks are stable, platform asserts PWRGOOD_CPU and continues to assert RESET_CPU_N signal to the socket.
  - PWRGOOD_CPU remains asserted as long as Vccin, Vccioin and VCCD remain stable.
  - No power sequencing between Vccin and VCCD is required.
- Phase 1: PCU bring-up
  - Phase 1a: Activity Leading to PCU Start-up
    - Assertion of PWRGOOD_CPU (the trigger to move from the end Phase 0 to thestart of Phase 1a).
    - Processor starts a timer (using BCLK) for determinism interval.
    - The PECI and SVID interfaces are held in reset until IVR asserts its power good signal.
    - The PCU PLL is enabled.
  - Phase 1b: Pcode Controlled Preparing for Broad uncore Bring-Up
    - Starting at the sub-phase, all steps should be synchronous.
    - PCU micro controller comes out of reset to start reset pcode execution. This is the planned "re-entry" point for Warm Reset processing.
    - Early reset pcode determines that it is at the start of Phase 1b.
    - Pcode brings the rest of the PCU hardware out of reset.
    - Pcode determines the boot config.

      - Pcode issues SVID command to ramp Vccin to 1.8V for cold reset.
      - Pcode reads and compares Vccin MBVR ICCMAX limit (reg 21h) vs its own supported ICCMAX limit:
        - If VR's ICCMAX ≥ supported ICCMAX then bootup continues.
        - If VR's ICCMAX < supported ICCMAX then bootup halts and system shuts down. MSR 411h IA32_MC4_STATUS logs Error code 0x1e - MCA_VR_ICC_MAX_LESS_THAN_FUSED_ICC_MAX in field MSEC_FW.
      - Pcode sequences uncore non-boot IVRs to ramp up.
      - Pcode signals uncore power good to IIO, IMC.
      - Delivery of the uncore power good signals defines the transition from the end of phase 1b to the beginning of phase 1c.
    - Phase 1c: PLL locking and IO Calibration
      - Pcode initiates thermal sensors.
      - Pcode locks PLLs in the following order: IIO, and IMC.
      - Pcode instructs the ring PLLs to start locking.
      - RESET_CPU_N signal is deasserted.
      - De-assertion of RESET_CPU_N signal will bring PCU out of reset and signifies the transition from the end of Phase 1c to the beginning of Phase 2.
- Phase 2: Uncore initialization and core bring up
    - The starting assumptions are:
      - All IVRs except core IVRs have ramped-up and are stable.
      - All PLLs except core PLLs have locked.
      - Phase 2 is entered as a result of de-assertion of external pin RESET_CPU_N.
      - Boot mode related straps have been sampled and are available.
      - Some IO link calibration have started and may or may not have completed by the start of this phase.
    - In this phase
      - PCU comes out of reset again and again determines the reset type.
      - Reset is deasserted to the ring units (HA, Cbo, IIO).
      - Reset is de-asserted to System Agents (IMC, IIO).
      - Pcode initializes the ring stops
      - Pcode performs boot mode processing based on straps. Set the advertised firmware, IO, and Intel TXT agent bits appropriately.
      - Pcode services DMI2 handshake protocol. If DMI2 links are used in DMI2 mode, pcode checks if the links have trained to L0. If it's the legacy socket, and if DMI2 links does not reach L0 within 3-4 ms, pcode executes error flow.
      - Pcode determines number of cores, slices and st/mt-threading for the core. In this step pcode also takes into account number of BIOS-disabled cores. Pcode determines whether BIST should be executed. BIST is executed if BIST Strap is set or requested.
      - Pcode programs the logical ids and switches from physical to logical mode.
      - LLC reset and configuration.
      - If it's not service processor boot mode, pcode waits for links to get to parameter exchange.
      - Pcode releases links to get to Normal operation (i.e. L0)
      - Pcode sets core Cstate to C1
- Phase 3: Reset execution (from core reset to fetch boot vector)

- The starting assumptions are:
  - Before this phase starts, following information is provided to the core: APIC-ID, whether it's the BSP, SMT enable/disable, reset type (cold, warm, C6 exit).
  - Uncore necessary to the get to the BIOS and Intel TXT Address space is fully initialized.
- In this phase:
  - Initialize core's internal structures, arrays, microarchitectural and architectural state.
  - Execute MLC BIST if BIST enabled.
  - Initialize uncore.
  - Read LLC BIST results from the uncore and report it in the EAX register.
  - Report LLC and MLC BIST results.
  - The core and thread selected as package BSP fetches BIOS or goes to "Wait-for-SIPI" state
  - The end assumption is there is at least one thread that was designated as package BSP.

➢ Phase 4: BIOS execution

Figure 3-1 Power Sequencing Diagram G3 with RTC loss to S5

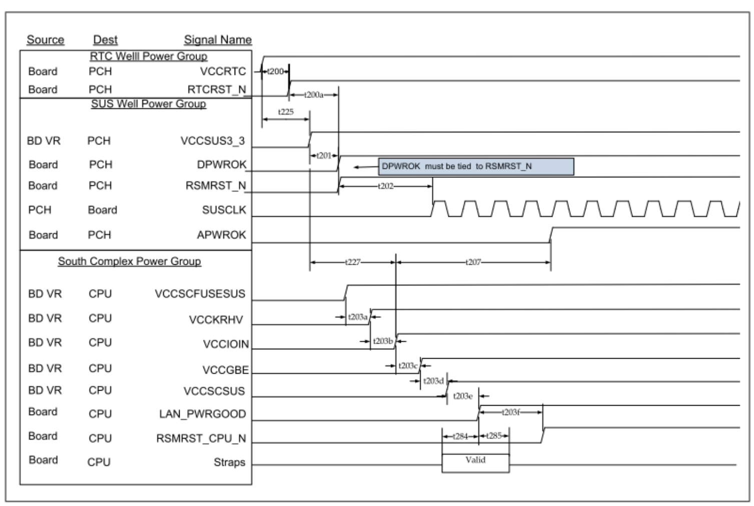
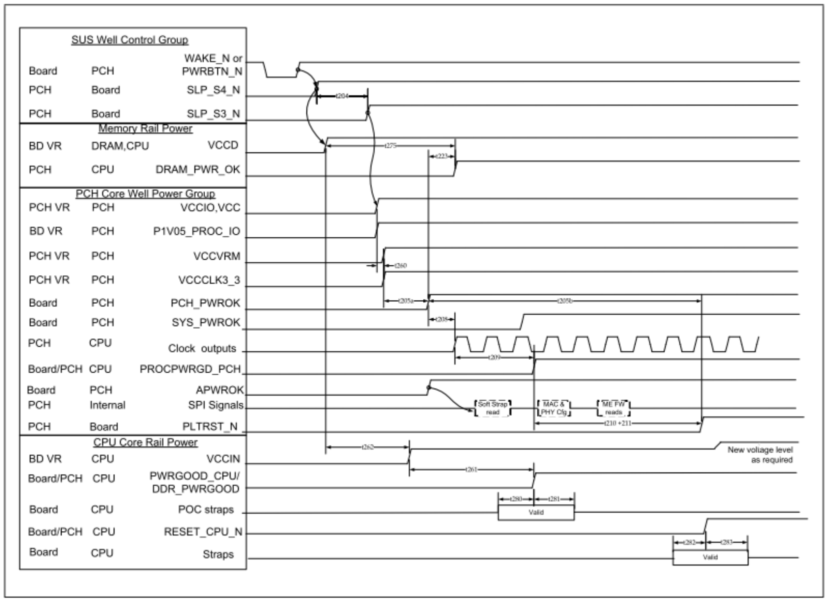


Figure 3-2 Power Sequencing Diagram S5 to S0



3.1.2. **Software Configurations of CPU**

Table 3-1 GPIO

Pin name	GPIO_USE_SEL 1: GPIO 0: Native	GPIO_IO_SEL 1: input 0: output	function
GPIO0	0	X	BMBUSY#
GPIO1	0	X	TACH1.
GPIO2	0	X	PIRQE#
GPIO3	0	X	PIRQF#.
GPIO4	0	X	PIRQG#
GPIO5	0	X	PIRQH#
GPIO6	0	X	NC
GPIO7	0	X	NC
GPIO8	1	0	PCH_XDP_NCLK1

GPIO9	1	1	XDP_NOA5_PCH/ BDX_CPLD_JTAG_TDI
GPIO10	1	0	XDP_NOA6_PCH/ BDX_CPLD_JTAG_TDO
GPIO11	0	X	SMBALERT#
GPIO12	0	X	LAN_PHY_PWR_CTRL
GPIO14	1	0	XDP_NOA7_PCH/ BDX_CPLD_JTAG_TCK
GPIO15	1	0	SOC_FPGA_CLK
GPIO16	1	0	FM_THROTTLE_PCH_N/ FM_THROTTLE_N
GPIO17	0	X	TACH0
GPIO18	1	0	XDP_NOA14_PCH/ BDX_CPLD_JTAG_TMS
GPIO19	1	BI-DIR	XDP_NOA9_PCH
GPIO20	1	0	FM_SMI_ACTIVE_PCH_N/ FM_SMI_ACTIVE_CPLD_N
GPIO21	1	BI-DIR	XDP_NOA8_PCH
GPIO22	0	X	SCLOCK
GPIO23	X	X	NC
GPIO24	1	0	USB1_VBUS
GPIO25	1	1	1PPS_CPU
GPIO26	1	1	SYS_CPLD_INT_CPU
GPIO27	1	1	SOC_FPGA_DIN
GPIO28	1	0	SOC_FPGA_DOUT

GPIO29	1	1	IP_UART0_SOUT
GPIO30	1	0	IP_UART0_SIN
GPIO31	1	1	SMB_PWR_ALERT
GPIO32	X	X	NC
GPIO33	1	1	4.7K TO GND
GPIO35	1	0	FM_NMI_EVENT_PCH_N/ FM_NMI_EVENT_CPLD_N
GPIO36	1	0	ADR_STATUS_RD
GPIO37	1	1	ADR_STATUS_CLR
GPIO38	0	X	SLOAD
GPIO39	0	X	SDATAOUT0
GPIO40	0	X	OC1#
GPIO41	1	0	XDP_NOA2_PCH/ CPLD_CONFIG_CLK
GPIO42	1	0	XDP_NOA3_PCH/ CPLD_CONFIG_DATA
GPIO43	1	X	XDP_NOA4_PCH_R
GPIO44	1	1	MAC_INT_L
GPIO45	1	1	CPLD23_INT_CPU
GPIO46	1	0	CPU_JTAG_RST
GPIO48	0	X	SDATAOUT1
GPIO49	1	X	FM_CPU_PROCHOT_PCH_N/ FM_PROCHOT_N
GPIO50	X	X	NC

GPIO51	1	1	4.7k pull to 3.3V
GPIO52	1	1	CPU_SV
GPIO53	1	1	1k pull to gnd
GPIO54	X	X	NC
GPIO55	1	1	FM_BIOS_RCRV_BOOT_N
GPIO57	1	1	FM_ME_RCRV_N
GPIO58	0	X	SML1_CLK
GPIO59	1	X	XDP_NOA0_PCH/ USB1_PWRFAULT
GPIO60	0	X	SML0ALERT#
GPIO61	X	X	NC
GPIO62	1	0	PCH_SUSCLK_33K
GPIO65	X	X	NC
GPIO67	X	X	NC
GPIO68	X	X	NC
GPIO69	X	X	NC
GPIO70	X	X	NC
GPIO71	X	X	NC
GPIO72	1	1	1K pull to 3.3V
GPIO74	0	X	SML1ALERT#/TEMP_ALERT#.
GPIO75	0	X	SML1DATA

Table 3-2 PCH Strap definitions

Strap pin	description	value

SATA1GP/ GPIO19	This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 Reserved 1 1 SPI (default) 0 0 LPC	1
GPIO51	This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.	1
SATA3GP /GPIO37	0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).	0
MFG_MODE_STRAP	0 = Enable security measures defined in the Flash Descriptor. 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.	0
INTVRMEN	0 = DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source (should be connected to an external VRM). It should not pull the strap low. 1 = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left as No Connect.	1
GPIO62 / SUSCLK	0 = Disable PLL On-Die voltage regulator. 1 = Enable PLL On-Die voltage regulator.	1
DSWODVREN	0 = Disable Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This mode is only	1

	supported for testing environments. 1 = Enable DSW 3.3 V-to-1.05 V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards.	
SPKR	0 = Disable “No Reboot” mode. 1 = Enable “No Reboot” mode (integrated PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.	
SATA2GP/GPIO36	0 = SoC RX is terminated to VSS. Grangeville platform only supports SoC Rx terminated to VSS. 1 = SoC RX is terminated to VCC/2.	0
GPIO33	0 = SoC TX is terminated to VSS. Grangeville platform only supports SoC Tx terminated to VSS 1 = SoC TX is terminated to VCC/2.	0
GPIO53	0 = SoC is in AC-coupling mode. Grangeville platform only supports AC-coupling mode. 1 = SoC is in DC-coupling mode.	0
GPIO55	0 = Enable “Top Swap” mode. This inverts an address on access to SPI and firmware hub, so the processor believes its fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64 KB blocks in the FWH or the appropriate address lines (A16, A17, A18, A19, or A20) as selected in Top-Swap Block size soft strap (handled through FITc. 1 = Disable “Top Swap” mode.	1
GPIO8	This pin must not be driven low until after rising edge of RSMRST_N.	1
GPIO44	This pin must not be driven low until after rising edge of RSMRST_N.	1
GPIO46	This pin must not be driven low until after rising edge of RSMRST_N.	1

BIST_ENABLE	Build-in Self Test (BIST) enable strap: 0 = BIST Disable 1 = BIST Enable	0
BMCINIT	Integrated Service Processor Boot Mode Selection: 0 = Integrated Service Processor Boot Mode Disabled. 1 = Integrated Service Processor Boot Mode Enable	1
TXT_PLTEN	0 = The platform is not Intel TXT enabled. 1 = Default. The platform is Intel TXT enabled.	0
TXT_AGENT	0 = Default. The SoC is not the Intel TXT Agent. 1 = The SoC is the Intel TXT Agent.	0
SAFE_MODE_BOOT	0 = Safe Mode Boot Disabled 1 = Safe Mode Boot Enabled	1
DEBUG_EN_N	0 = Debug Mode 1 = Normal Mode	XDP_PRESENT_N
DDR3_4_STRAP	Select between DDR4 and DDR3 0 = DDR3, it requires <1K ohm pull down in order to out drive the internal pull up. 1= DDR4 (Default)	1
PECI0 ; PECI1 ; PECI2	In micro-server design space, there will be multiple sockets that share a PECI bus. However these sockets are effectively independent agents. The PECI IDs are used as straps to identify which socket is which in order for PECI bus to work.	000
LAN_MDIO_DIR_CTL_0; LAN_MDIO_DIR_CTL_1	00 = Both LAN ports are disabled. Note: In this mode manageability is not functional and must not be enabled in NVM control word 1. 01 = Port 1 is disabled. Port 0 is enabled.	11

	10 = Reserved 11 = Both Port 0 and 1 are enabled. Recommend 5.1K ohm pull up to VCCIOIN or 5.1K ohm pull down to GND.	
RSVD12_AJ67	This pin should have a 5.1K ohm pull down to GND.	0
RSVD11_AG67	This pin should have a 5.1K ohm pull down to GND.	0
RSVD10_AN78	This pin should have a 5.1K ohm pull down to GND.	0
RSVD09_AC64	This pin should have a 5.1K ohm pull down to GND.	0
SERIRQ_DIR	Recommend 5.1k ohm pull up to VCCIOIN.	1
UART_TXD[0]	Recommend 5.1k ohm pull down to GND.	0
UART_TXD[1]	Controls the security attributes on the NVM - for pre-production usage only. 0 = Disable NVM Security (Default) 1 = Security Enabled Recommend 5.1K ohm pull down to GND.	0
LAN_NCSI_RXD0	Recommend 5.1K ohm pull up to VCCIOIN.	1
LAN_NCSI_RXD1	Enable/Disable manageability traffic: 0 = LAN available in S5 for WoL (Default) 1 = LAN not available in S5. Manageability is disabled. Recommend 5.1K ohm pull down to GND.	0
LAN_NCSI_ARB_OUT	Selects SVID VR Operating Mode 1 - VCCSCSUS, P1V05_PCH, VCCGBE, VCCIOIN are combined into one SVID controlled supply. 0 - Separate SVID controllers (default).	1
RSVD84	49.9Ω 1% to GND	0
RSVD93	1k - 5.1kΩ to GND	0
RSVD94	1k - 5.1kΩ to GND	0
RSVD00	1k - 5.1kΩ to VCC3_3	1

RSVD18	1k - 5.1kΩ to GND	0
RSVD16	1k - 5.1kΩ to GND	0
RSVD17	1k - 5.1kΩ to GND	0
RSVD21	1k - 5.1kΩ to GND	0
NCTF/TP	1k - 5.1kΩ to VCC3_3	1

3.2. Memory Mapping

Broadwell-DE SoC contains registers that are located in the processor I/O space and memory space and sets of PCI configuration registers that are located in PCI configuration space. This chapter describes Broadwell-DE SoC I/O and memory maps at the register-set level. Register access is also described.

Table 3-3 PCI devices and functions

Bus:Device:Function	**Function Description**
Bus0:Device31:Function0	LPC controller
Bus0:Device31:Function2	SATA controller #1
Bus0:Device31:Function3	SMBus controller
Bus0:Device31:Function5	SATA controller#2
Bus0:Device31:Function6	Thermal subsystem
Bus0:Device29:Function0	USB EHCI controller#1
Bus0:Device28:Function0	PCI-e port1
Bus0:Device28:Function1	PCI-e port2
Bus0:Device28:Function2	PCI-e port3
Bus0:Device28:Function3	PCI-e port4
Bus0:Device28:Function4	PCI-e port5
Bus0:Device28:Function5	PCI-e port6
Bus0:Device28:Function6	PCI-e port7
Bus0:Device28:Function7	PCI-e port8
Bus0:Device25:Function0	Gigabit Ethernet controller
Bus0:Device22:Function0	Intel management engine interface#1
Bus0:Device22:Function1	Intel management engine interface#2
Bus0:Device22:Function2	IDE-R
Bus0:Device22:Function3	KT

Bus0:Device20:Function0	xHCI controller

Table 3-4 Fixed I/O ranges decoded by Broadwell-DE

I/O Address	Read Target	Write Target	Internal Unit
00h-08h	DMA controller	DMA controller	DMA
09h-0Eh	reserved	DMA controller	DMA
0Fh	DMA controller	DMA controller	DMA
10h-18h	DMA controller	DMA controller	DMA
19h-1Eh	reserved	DMA controller	DMA
1Fh	DMA controller	DMA controller	DMA
20h-21h	Interrupt controller	Interrupt controller	interrupt
24h-25h	Interrupt controller	Interrupt controller	interrupt
28h-29h	Interrupt controller	Interrupt controller	interrupt
2Ch-2Dh	Interrupt controller	Interrupt controller	interrupt
2Eh-2Fh	LPC SIO	LPC SIO	Forwarded to LPC
30h-31h	Interrupt controller	Interrupt controller	interrupt
34h-35h	Interrupt controller	Interrupt controller	interrupt
38h-39h	Interrupt controller	Interrupt controller	interrupt
3Ch-3Dh	Interrupt controller	Interrupt controller	interrupt
40h-42h	Timer/Counter	Timer/Counter	PIT
43h	reserved	Timer/Counter	PIT
4Eh-4Fh	LPC SIO	LPC SIO	Forwarded to LPC
50h-52h	Timer/Counter	Timer/Counter	PIT
53h	reserved	Timer/Counter	PIT
60h	microcontroller	microcontroller	Forwarded to LPC
61h	NMI controller	NMI controller	Processor I/F
62h	microcontroller	microcontroller	Forwarded to LPC
64h	microcontroller	microcontroller	Forwarded to LPC
66h	microcontroller	microcontroller	Forwarded to LPC
70h	reserved	NMI and RTC controller	RTC

71h	RTC controller	RTC controller	RTC
72h	RTC controller	NMI and RTC controller	RTC
73h	RTC controller	RTC controller	RTC
74h	RTC controller	NMI and RTC controller	RTC
75h	RTC controller	RTC controller	RTC
76h	RTC controller	NMI and RTC controller	RTC
77h	RTC controller	RTC controller	RTC
80h	DMA controller, LPC, PCI or PCIe	DMA controller, LPC, PCI or PCIe	DMA
81h-83h	DMA controller	DMA controller	DMA
84h-86h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
87h	DMA controller	DMA controller	DMA
88h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
89h-8Bh	DMA controller	DMA controller	DMA
8Ch-8Eh	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
8Fh	DMA controller	DMA controller	DMA
90h-91h	DMA controller	DMA controller	DMA
92h	Reset generator	Reset generator	Processor I/F
93h-9Fh	DMA controller	DMA controller	DMA
A0h-A1h	Interrupt controller	Interrupt controller	interrupt
A4h-A5h	Interrupt controller	Interrupt controller	interrupt
A8h-A9h	Interrupt controller	Interrupt controller	interrupt
ACh-ADh	Interrupt controller	Interrupt controller	interrupt
B0h-B1h	Interrupt controller	Interrupt controller	interrupt
B2h-B3h	Power management	Power management	Power management
B4h-B5h	Interrupt controller	Interrupt controller	interrupt
B8h-B9h	Interrupt controller	Interrupt controller	interrupt
BCh-BDh	Interrupt controller	Interrupt controller	interrupt

C0h-D1h	DMA controller	DMA controller	DMA
D2h-DDh	reserved	DMA controller	DMA
DEh-DFh	DMA controller	DMA controller	DMA
F0h	Ferr#/interrupt controller	Ferr#/interrupt controller	Processor I/F
170h-177h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
1F0h-1F7h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
200h-207h	Gameport low	Gameport low	Forwarded to LPC
208h-20Fh	Gameport high	Gameport high	Forwarded to LPC
376h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
3F6h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
4D0h-4D1h	Interrupt controller	Interrupt controller	interrupt
CF9h	Reset generator	Reset generator	Processor I/F

Table 3-5 Variable I/O decode ranges

Range name	**Mappable**	**Size (bytes)**	**Target**
ACPI	Anywhere in 64KB I/O space	64	Power management
IDE bus master	Anywhere in 64KB I/O space	1. 16 or 32 2. 16	1. SATA host controller #1, #2 2. IDE-R
Native IDE command	Anywhere in 64KB I/O space	8	1. SATA host controller #1, #2 2. IDE-R
Native IDE control	Anywhere in 64KB I/O space	4	1. SATA host controller #1, #2 2. IDE-R
SATA index/data pair	Anywhere in 64KB I/O space	16	1. SATA host controller #1, #2 2. IDE-R
SMBus	Anywhere in 64KB I/O space	32	SMB unit
TCO	96 bytes above ACPI base	32	TCO unit
GPIO	Anywhere in 64KB I/O space	128	GPIO unit
Parallel port	3 ranges in 64KB I/O space	8	LPC peripheral
Serial port 1	8 ranges in 64KB I/O space	8	LPC peripheral

Serial port 2	8 ranges in 64KB I/O space	8	LPC peripheral
Floppy disk controller	2 ranges in 64KB I/O space	8	LPC peripheral
LAN	Anywhere in 64KB I/O space	32	LAN unit
LPC generic 1	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 2	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 3	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 4	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
I/O trapping ranges	Anywhere in 64KB I/O space	1 to 256	Trap on backbone
PCI bridge	Anywhere in 64KB I/O space	I/O base/limit	PCI bridge
PCI-E root ports	Anywhere in 64KB I/O space	I/O base/limit	PCI-E root ports 1-8
KT	Anywhere in 64KB I/O space	8	KT

Table 3-6 Memory decode ranges from processor perspective

Memory range	**target**	**Dependency/comments**
0000 0000h-000D FFFFh 0010 0000h-TOM	Main memory	TOM registers in host controller
000E 0000h-000E FFFFh	LPC or SPI	Bit 6 in BIOS decode enable register is set
000F 0000h-000F FFFFh	LPC or SPI	Bit 7 in BIOS decode enable register is set
FEC_ _000h-FEC_ _040h	IOx APCI inside broadwell-de SoC	_ _ is controlled using APIC range select (ASEL) field and APIC enable (AEN) bit.
FEC1 0000h-FEC1 7FFFh	PCI-E port 1	PCI-E root port 1 I/OxAPIC enable (PAE) set
FEC1 8000h-FEC1 FFFFh	PCI-E port 2	PCI-E root port 2 I/OxAPIC enable (PAE) set
FEC2 0000h-FEC2 7FFFh	PCI-E port 3	PCI-E root port 3 I/OxAPIC enable (PAE) set
FEC2 8000h-FEC2 FFFFh	PCI-E port 4	PCI-E root port 4 I/OxAPIC enable (PAE) set
FEC3 0000h-FEC3 7FFFh	PCI-E port 5	PCI-E root port 5 I/OxAPIC enable (PAE) set

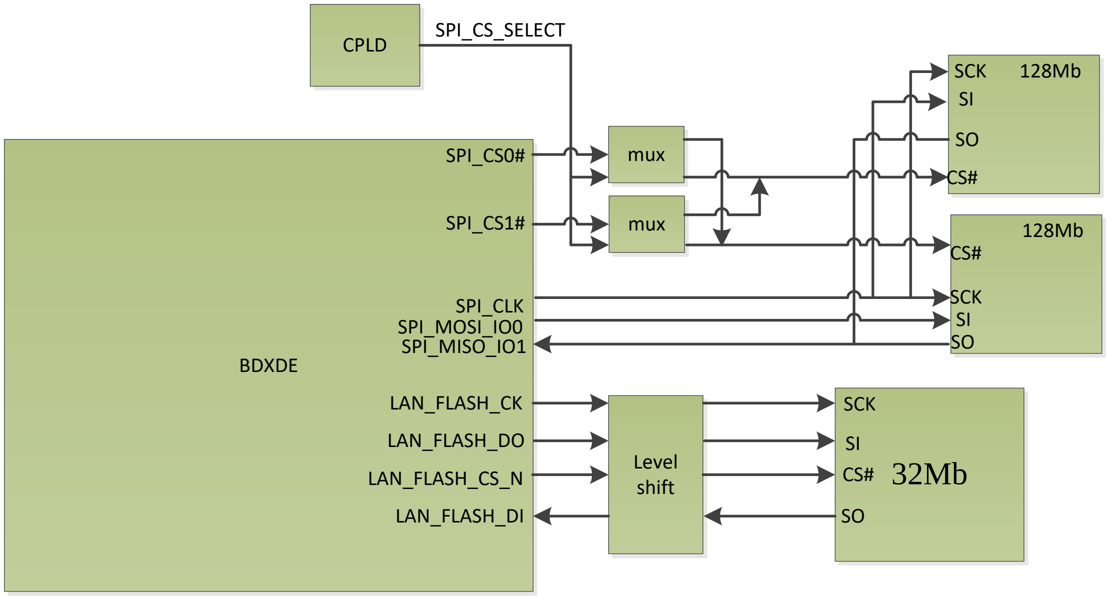
FEC3 8000h-FEC3 FFFFh	PCI-E port 6	PCI-E root port 6 I/OxAPIC enable (PAE) set
FEC4 0000h-FEC4 7FFFh	PCI-E port 7	PCI-E root port 7 I/OxAPIC enable (PAE) set
FEC4 8000h-FEC4 FFFFh	PCI-E port 8	PCI-E root port 8 I/OxAPIC enable (PAE) set
FFC0 0000h-FFC7 FFFFh FF80 0000h- FF87 FFFFh	LPC or SPI (or PCI)	Bit 8 in BIOS decode enable register is set
FFC8 0000h-FFCF FFFFh FF88 0000h- FF8F FFFFh	LPC or SPI (or PCI)	Bit 9 in BIOS decode enable register is set
FFD0 0000h-FFD7 FFFFh FF90 0000h- FF97 FFFFh	LPC or SPI (or PCI)	Bit 10 in BIOS decode enable register is set
FFD8 0000h-FFDF FFFFh FF98 0000h- FF9F FFFFh	LPC or SPI (or PCI)	Bit 11 in BIOS decode enable register is set
FFE0 0000h-FFE7 FFFFh FFA0 0000h- FFA7 FFFFh	LPC or SPI (or PCI)	Bit 12 in BIOS decode enable register is set
FFE8 0000h-FFEF FFFFh FFA8 0000h- FFAF FFFFh	LPC or SPI (or PCI)	Bit 13 in BIOS decode enable register is set
FFF0 0000h-FFF7 FFFFh FFB0 0000h-FFB7 FFFFh	LPC or SPI (or PCI)	Bit 14 in BIOS decode enable register is set
FFF8 0000h–FFFF FFFFh FFB8 0000h–FFBF FFFFh	LPC or SPI (or PCI)	Always enabled. The top two 64KB blocks of this range can be swapped.
FF70 0000h–FF7F FFFFh FF30 0000h–FF3F FFFFh	LPC or SPI (or PCI)	Bit 3 in BIOS Decode Enable register is set
FF60 0000h–FF6F FFFFh FF20 0000h–FF2F FFFFh	LPC or SPI (or PCI)	Bit 2 in BIOS Decode Enable register is set
FF50 0000h–FF5F FFFFh FF10 0000h–FF1F FFFFh	LPC or SPI (or PCI)	Bit 1 in BIOS Decode Enable register is set
FF40 0000h–FF4F FFFFh FF00 0000h–FF0F FFFFh	LPC or SPI (or PCI)	Bit 0 in BIOS Decode Enable register is set
128 KB anywhere in 4 GB range	Integrated LAN Controller	Enable using BAR in D25:F0 (Integrated LAN Controller MBARA)
4 KB anywhere in 4 GB range	Integrated LAN Controller	Enable using BAR in D25:F0 (Integrated LAN

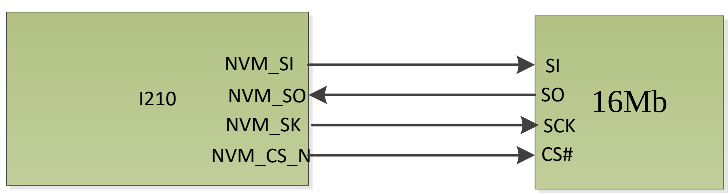
		Controller MBARB)
1 KB anywhere in 4 GB range	USB EHCI Controller #1	Enable using standard PCI mechanism (D29:F0)
64 KB anywhere in 4 GB range	USB xHCI Controller	Enable using standard PCI mechanism (D20:F0)
FED0 X000h–FED0 X3FFh	High Precision Event Timers	BIOS determines the "fixed" location which is one of four, 1-KB ranges where X (in the first column) is 0h, 1h, 2h, or 3h.
FED4 0000h–FED4 FFFFh	TPM on LPC	None
Memory Base/Limit anywhere in 4 GB range	PCI Bridge	Enable using standard PCI mechanism (D30:F0)
Prefetchable Memory Base/Limit anywhere in 64-bit address range	PCI Bridge	Enable using standard PCI mechanism (D30:F0)
64 KB anywhere in 4 GB range	LPC	LPC Generic Memory Range. Enable using setting bit[0] of the LPC Generic Memory Range register (D31:F0:offset 98h).
32 Bytes anywhere in 64-bit address range	SMBus	Enable using standard PCI mechanism (D31:F3)
2 KB anywhere above 64 KB to 4 GB range	SATA Host Controller #1	AHCI memory-mapped registers. Enable using standard PCI mechanism (D31:F2)
Memory Base/Limit anywhere in 4 GB range	PCI Express* Root Ports 1-8	Enable using standard PCI mechanism (D28: F 0-7)
Prefetchable Memory Base/Limit anywhere in 64-bit address range	PCI Express Root Ports 1-8	Enable using standard PCI mechanism (D28:F 0-7)
4 KB anywhere in 64-bit address range	Thermal Reporting	Enable using standard PCI mechanism (D31:F6 TBAR/ TBARH)
4 KB anywhere in 64-bit address range	Thermal Reporting	Enable using standard PCI mechanism (D31:F6 TBARB/TBARBH)
16 Bytes anywhere in 64-bit address range	Intel® MEI #1, #2	Enable using standard PCI mechanism (D22:F 1:0)
4 KB anywhere in 4 GB range	KT	Enable using standard PCI mechanism (D22:F3)
16 KB anywhere in 4 GB range	Root Complex Register Block (RCRB)	Enable using setting bit[0] of the Root Complex Base Address register (D31:F0:offset F0h).

3.3. FLASH

There are four SPI flash 2 x 128Mb, 1 x 32Mb and 1 x 16Mb, the 128Mb flash are for system boot one is primary another one is backup, 32Mb flash is for 10G controller setup that need level shift because of that SPI interface voltage level of BDXDE LAN is 1.05volt different SPI flash voltage level, the 16Mb flash is for I210 MAC setup. The system boot flash SPI clock rate is 20MHz via the SPI memory mapped configuration register SSFC[18:16] = “000” setting and the CPU GbE LAN SPI flash clock rate is 20MHz via the GbE LAN memory mapped configuration register SSFC[18:16] = “000” setting.

Figure 3-3 FLASH Connection

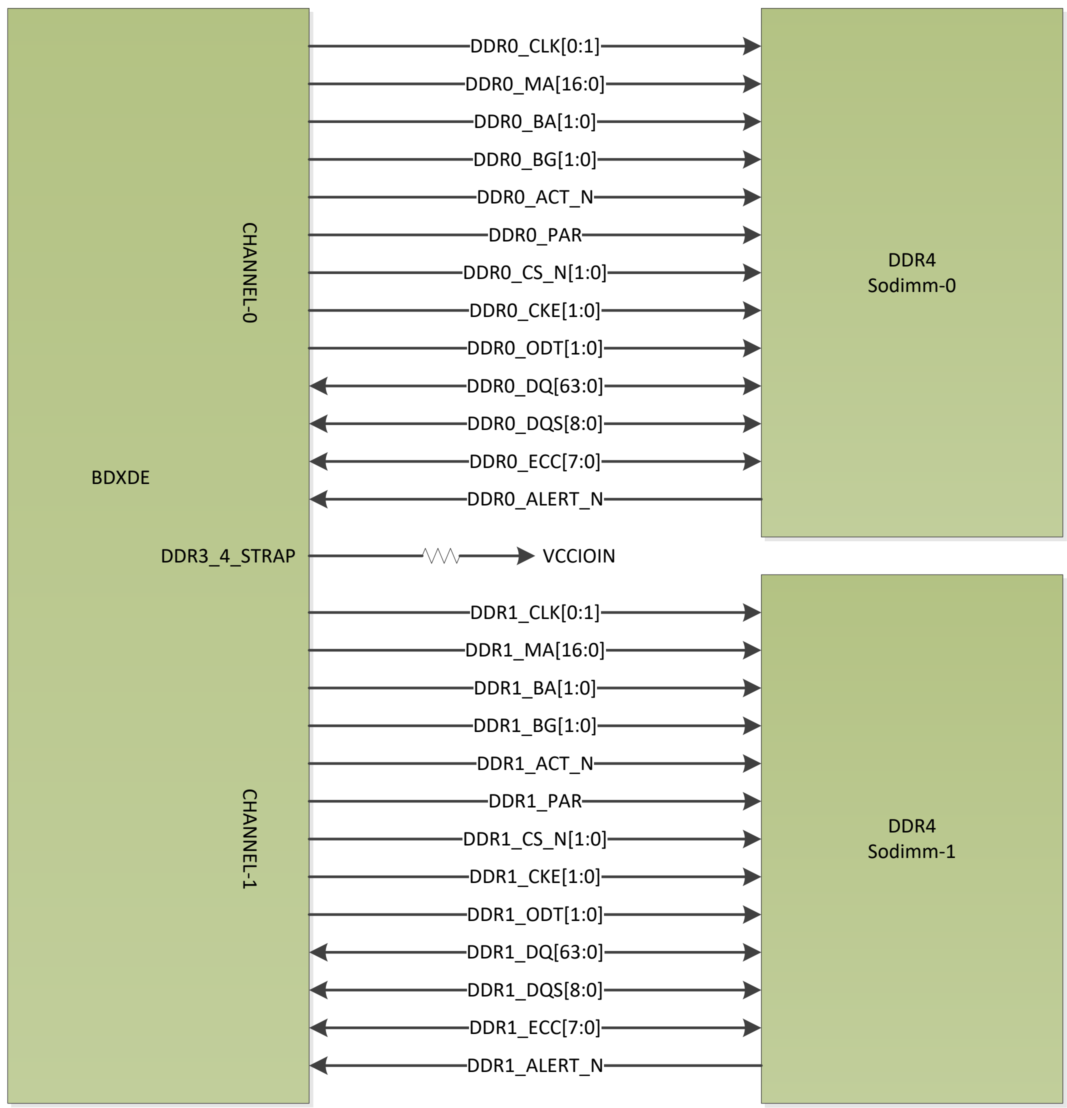




3.4. RAM

The BDXDE can support memory DDR3 and DDR4 that need via strap pin DDR3_4_STRAP to configure which one be supported. The project support two DDR4 SODIMM with ECC that has to pull DDR3_4_STRAP to high.

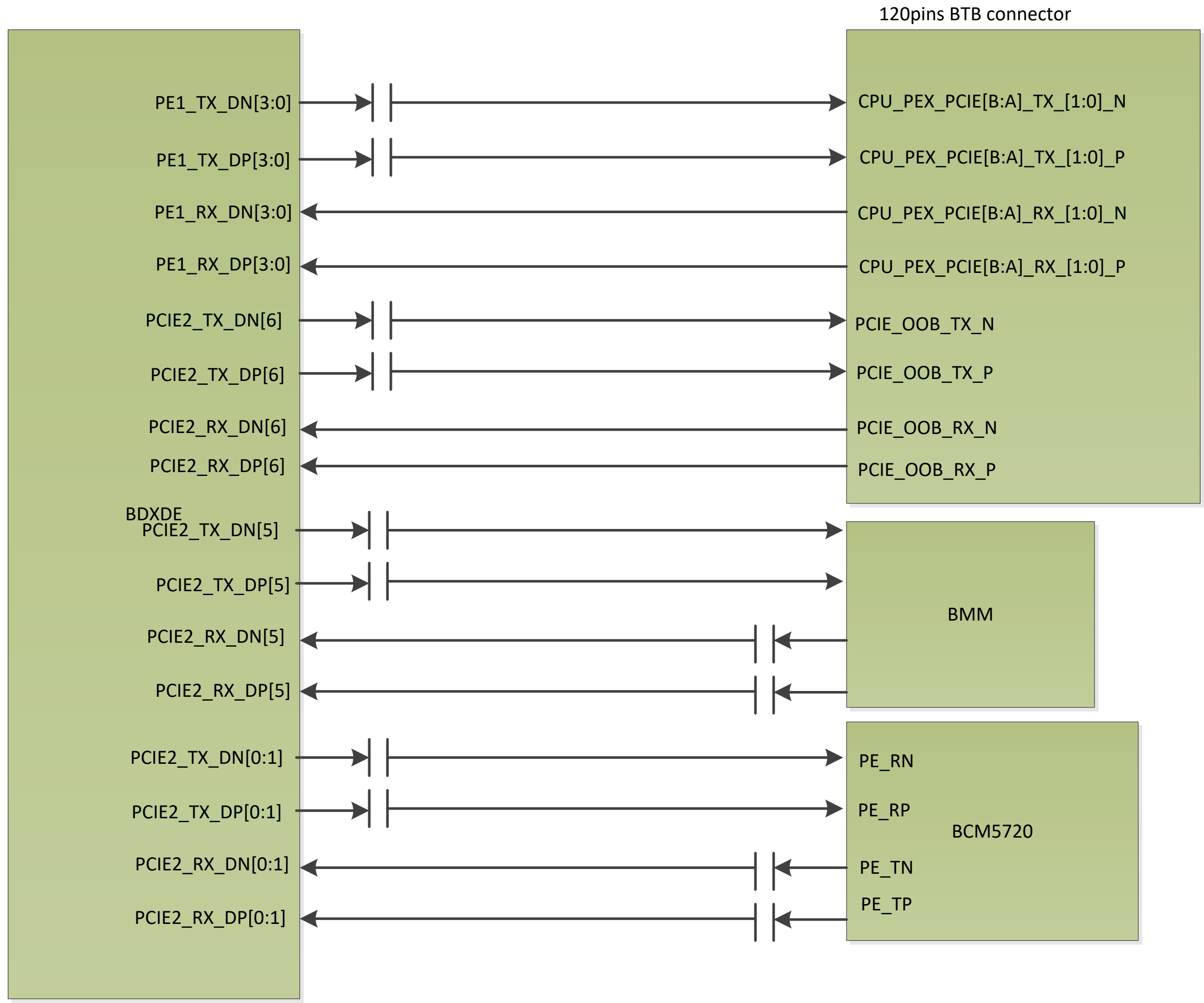
Figure 3-4 RAM Connection



3.5. PCIe

The project has to provide the x4 PCIe Gen2.0 to switch board that are for data package, another x1 PCIE Gen2 interface is needed to be translated to SGMII interface for management PHY.

Figure 3-5 PCIe Connection



120pins BTB connector
PE1_TX_DN[3:0]
CPU_PEX_PCIE[B:A]_TX_[1:0]_N
PE1_TX_DP[3:0]
CPU_PEX_PCIE[B:A]_TX_[1:0]_P
PE1_RX_DN[3:0]
CPU_PEX_PCIE[B:A]_RX_[1:0]_N
PE1_RX_DP[3:0]
CPU_PEX_PCIE[B:A]_RX_[1:0]_P
PCIE2_TX_DN[6]
PCIE_OOB_TX_N
PCIE2_TX_DP[6]
PCIE_OOB_TX_P
PCIE2_RX_DN[6]
PCIE_OOB_RX_N
PCIE2_RX_DP[6]
PCIE_OOB_RX_P
BDXDE
PCIE2_TX_DN[5]
PCIE2_TX_DP[5]
BMM
PCIE2_RX_DN[5]
PCIE2_RX_DP[5]
PCIE2_TX_DN[0:1]
PE_RN
PCIE2_TX_DP[0:1]
PE_RP
BCM5720
PCIE2_RX_DN[0:1]
PE_TN
PCIE2_RX_DP[0:1]
PE_TP

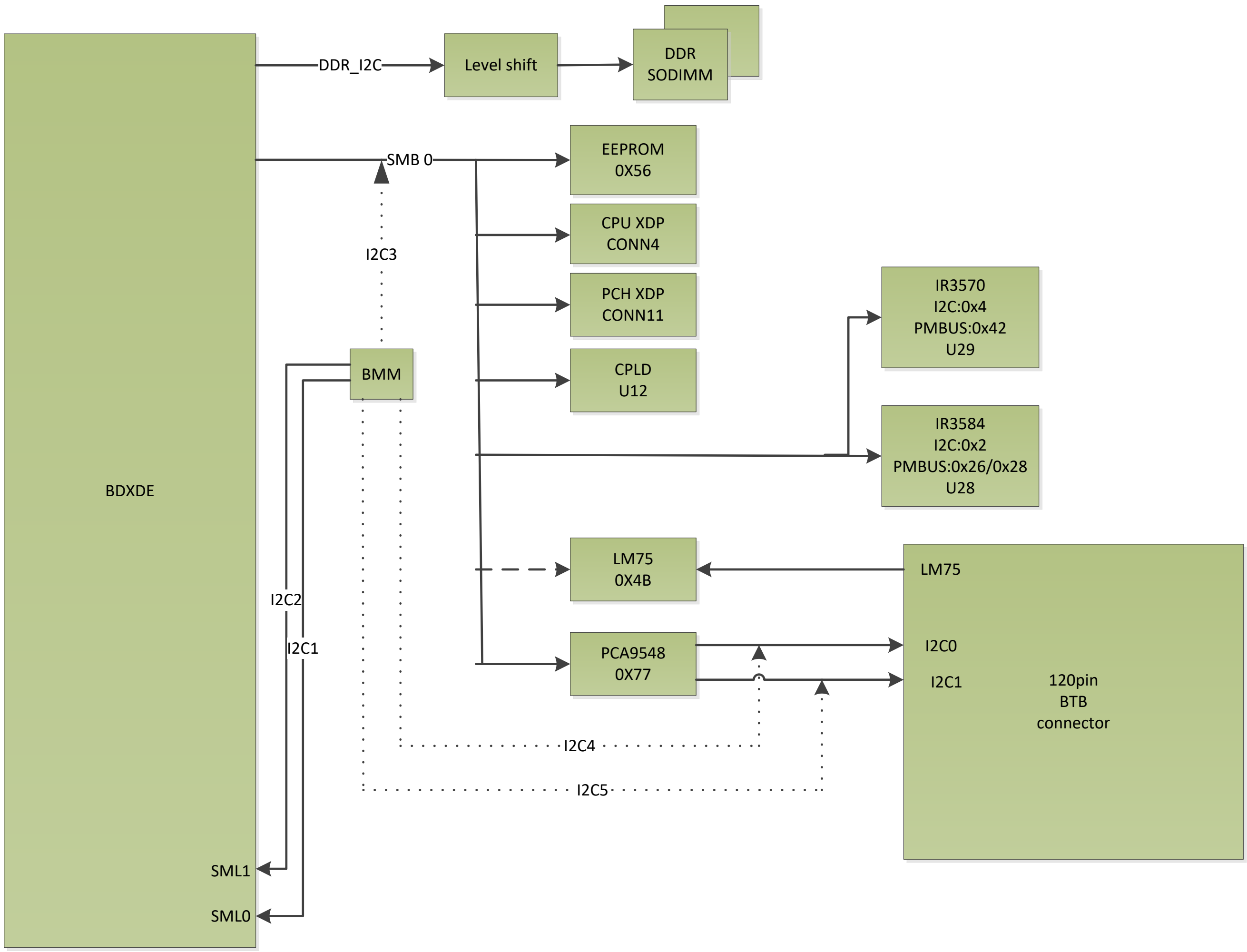
3.6. SMbus

The SMbus from Broadwell-De can access the CPU board and main board device via SMBUS0.

The LM75 (0x4B) is accessed by the CPLD on main board.

The I2C information from DDR SPD EEPROM need to read via another SMbus only used for DDR SPD.

Figure 3-6 I2C Connection



Note: I2C[1:5] are from the BMM point of view, not related to the I2C[0:1] through the B2B CONN

Table 3-7 SMBus 0 Address Table

Device	I2C address	Note
DDR4 SODIMM 1	0x50	This device need to be accessed by DDR_I2C interface
DDR4 SODIMM 2	0x52	This device need to be accessed by DDR_I2C interface
LM75	0x4B	This device need to be accessed by main board CPLD, and not display at SMBus 0.
EEPROM	0x56	
IR3584 (I2C)	0x02	
IR3584 (PMBUS-Loop1)	0x26	
IR3584 (PMBus-Loop2)	0x28	
IR3570 (I2C)	0x4	
IR3570 (PMBus Loop1)	0x42	
PCA9548	0X77	

3.7. UART

There are two UART interfaces, one is for chassis diagnostic via the 120pins BTB connector to front panel console port , also to a 4pin connector (CONN18)

Another one is for CPU board debug that is pin stick connector type.

Figure 3-7 UART Connection

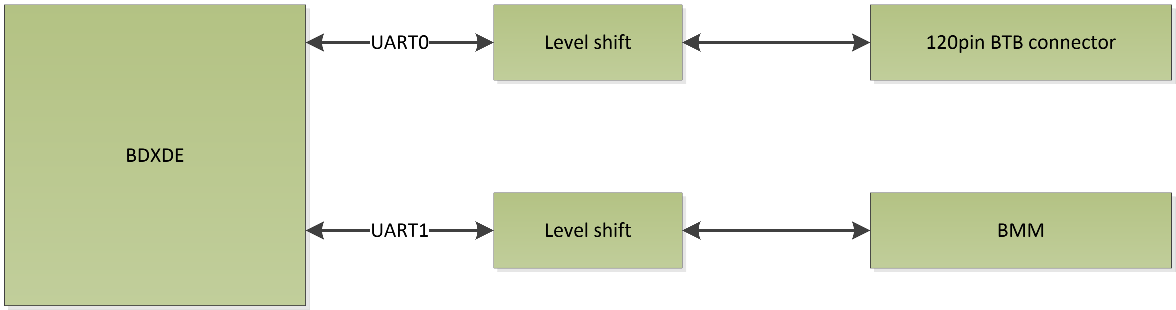


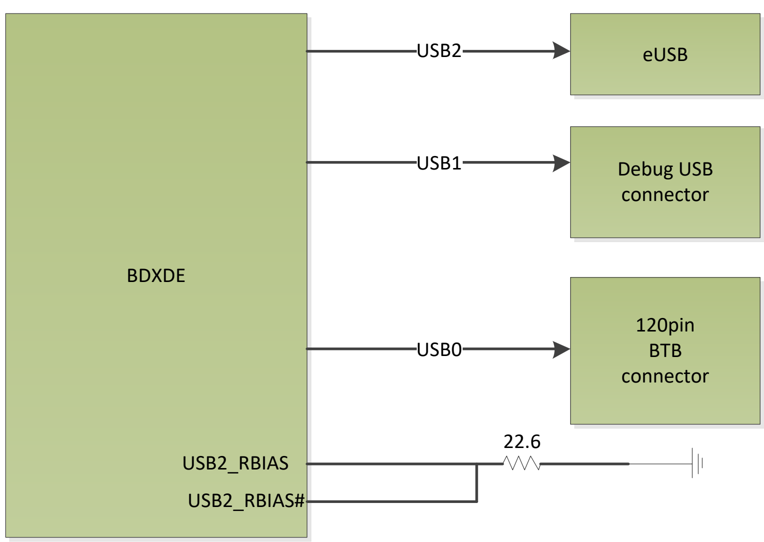
Table 3-8 CONN18 PIN ASSIGNMENT

Pin Number	Description
1	VCC
2	TX
3	RX
4	GND

3.8. USB

There are three USB 2.0 interfaces in the project. The USB-0 via the 120pins BTB connector to switch board for chassis USB connector, USB-1 is for debug function and USB-2 connect to eUSB module for internal USB access.

Figure 3-8 USB Connection



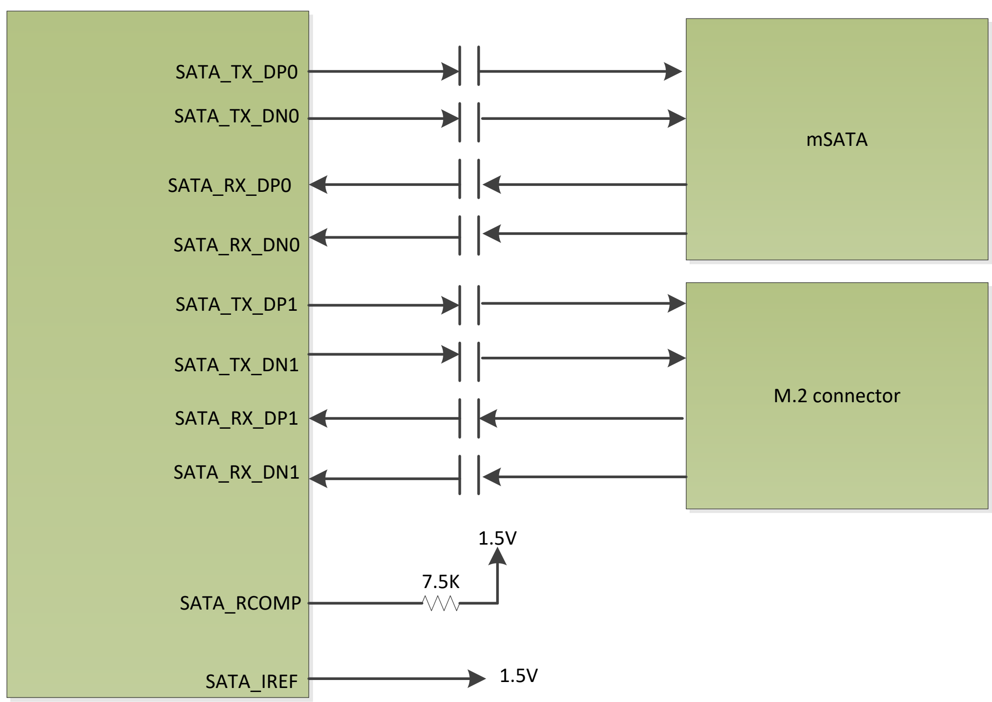
3.9. SATA

The CPU board supports 2 SATA SSD devices via SATA 3.0 interface.
SATA 3.0 CH0 support mSATA SSD module.
SATA 3.0 CH1 support m.2 SSD module.
The following table shows the mSATA and m.2 SSD module dimension and size.

Table 3-8 SATA SSD Module Table

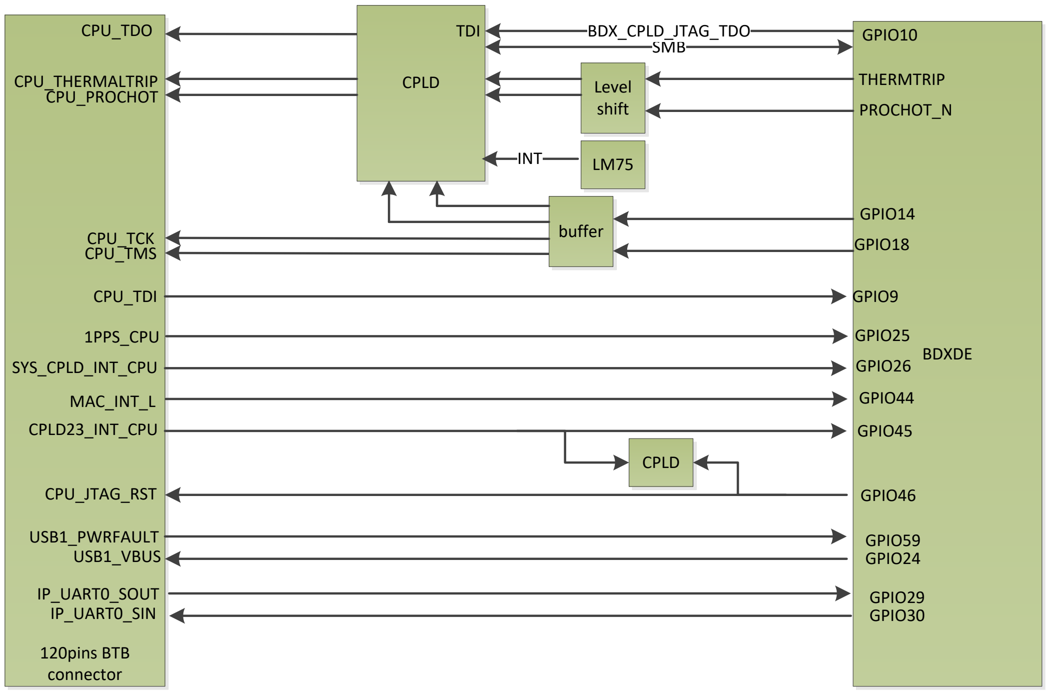
Type	Dimension	Capacity
mSATA SSD	50.8mm x 29.85mm x 4.0mm	16GB~512GB
M.2 SSD	42.0mm × 22.0mm × 3.5mm	32GB~256GB

Figure 3-9 SATA Connection



3.10. GPIO

Figure 3-10 GPIO Connection



CPLD

Figure 3-11 CPLD block diagram

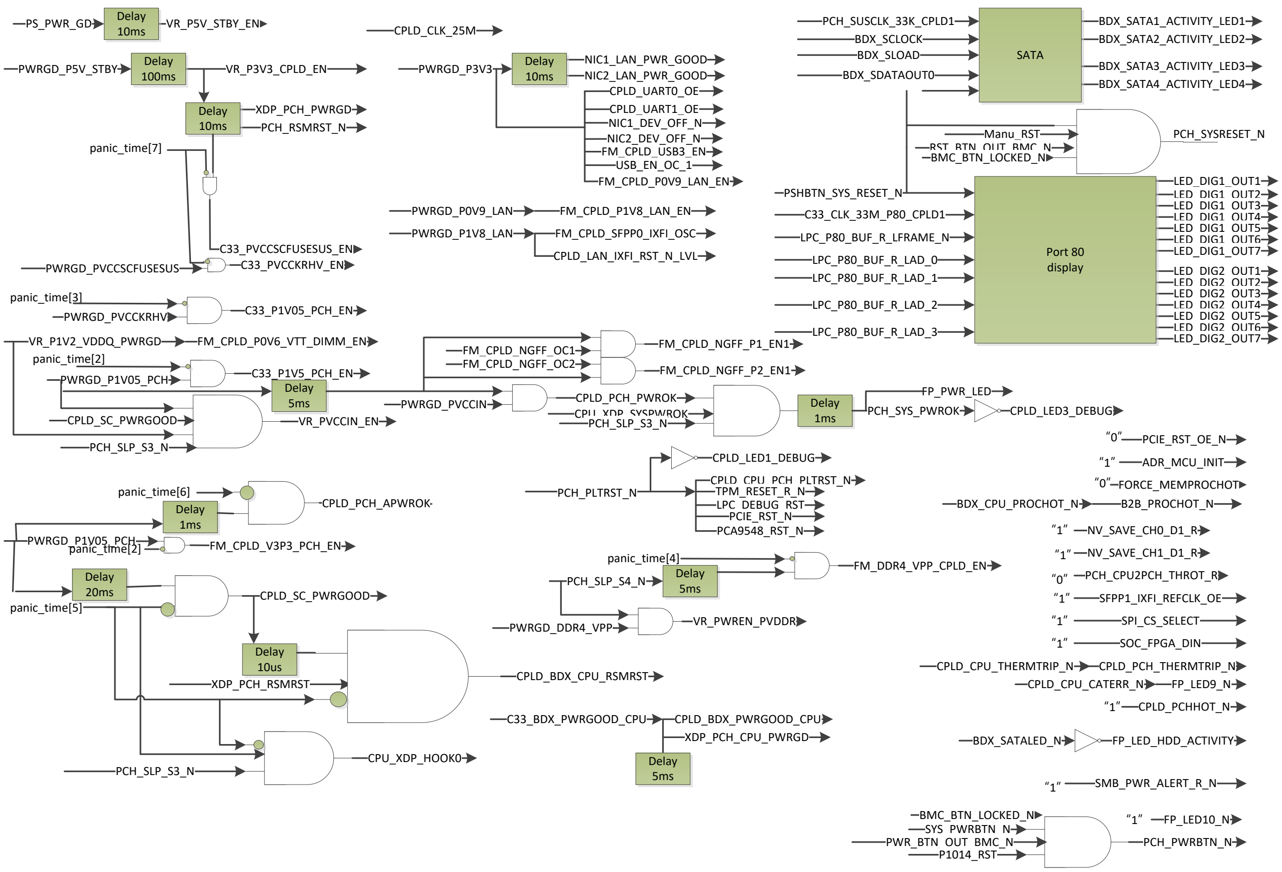
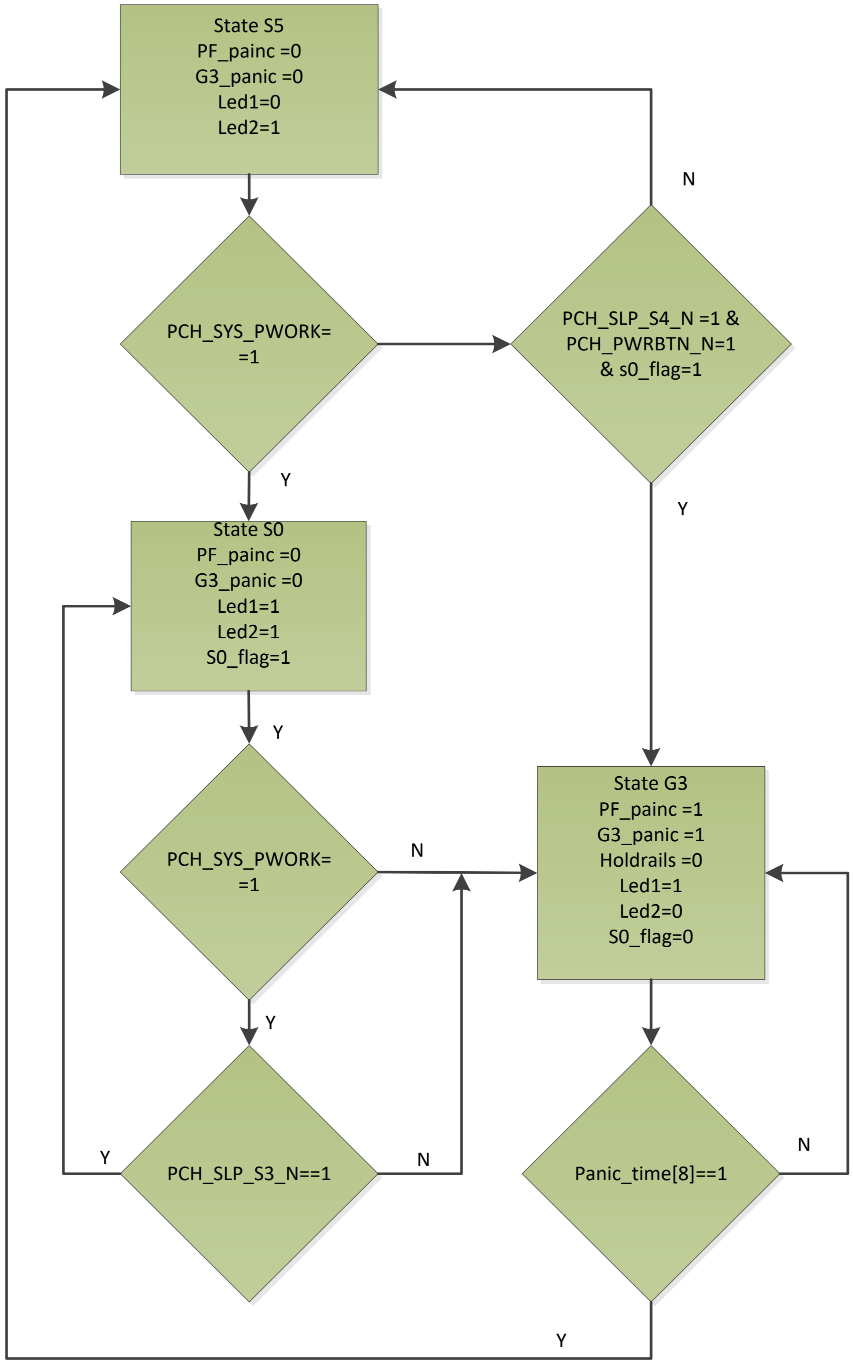


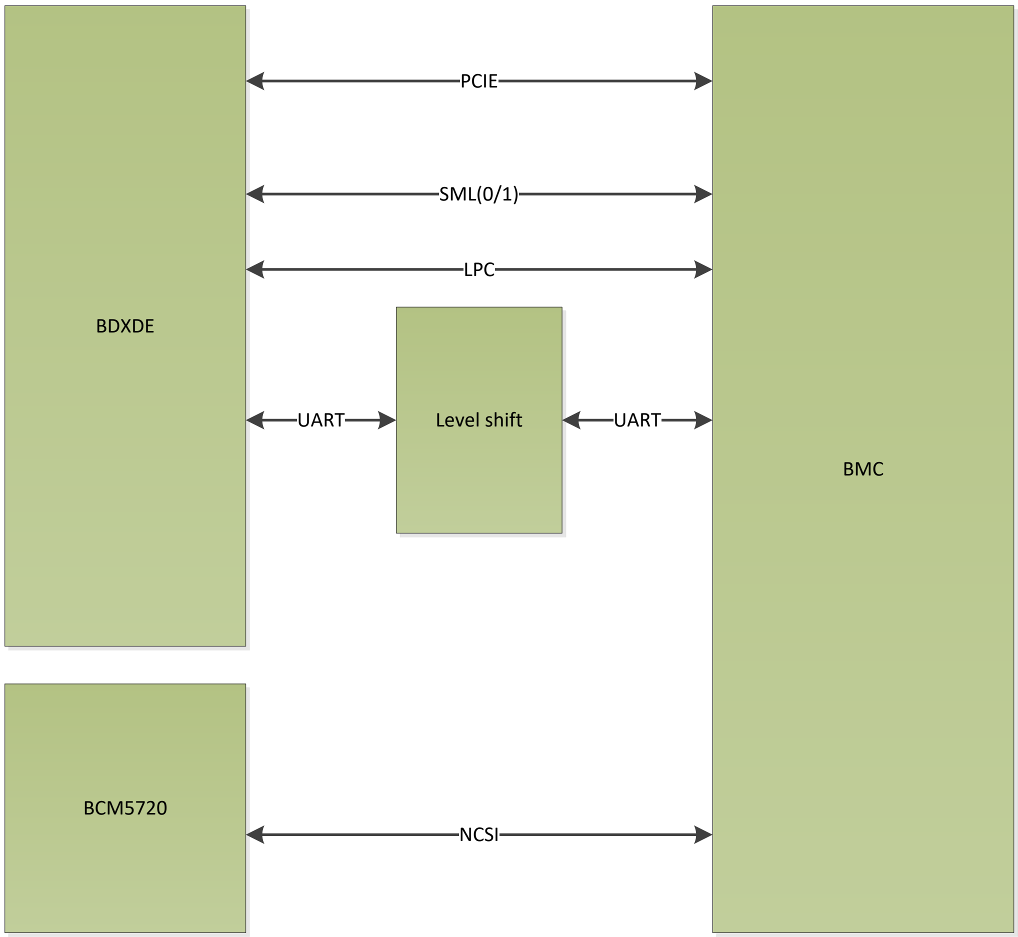
Figure 3-12 power sequence flow chat



3.11. BMC (Option)

The BMC (Baseboard management controller) is controller that can monitor thermal, power, FAN and CPU status when system in the S5 stage.

Figure 3-13 BMM connection



4. Switch Sub-system

The BCM56870 incorporates 32 falconcore, where each falconcore can operate at 40G/ 100Gbps.The PCIe interfaces the high bandwidth to transfer any packet to or from CPU. The PCI interface is configured at PCIe Gen2. It is to directly connect to CPU, and the bandwidth can be reached PCI2 Gen2 4 lanes.

4.1. Configurations of MAC (BCM56870)

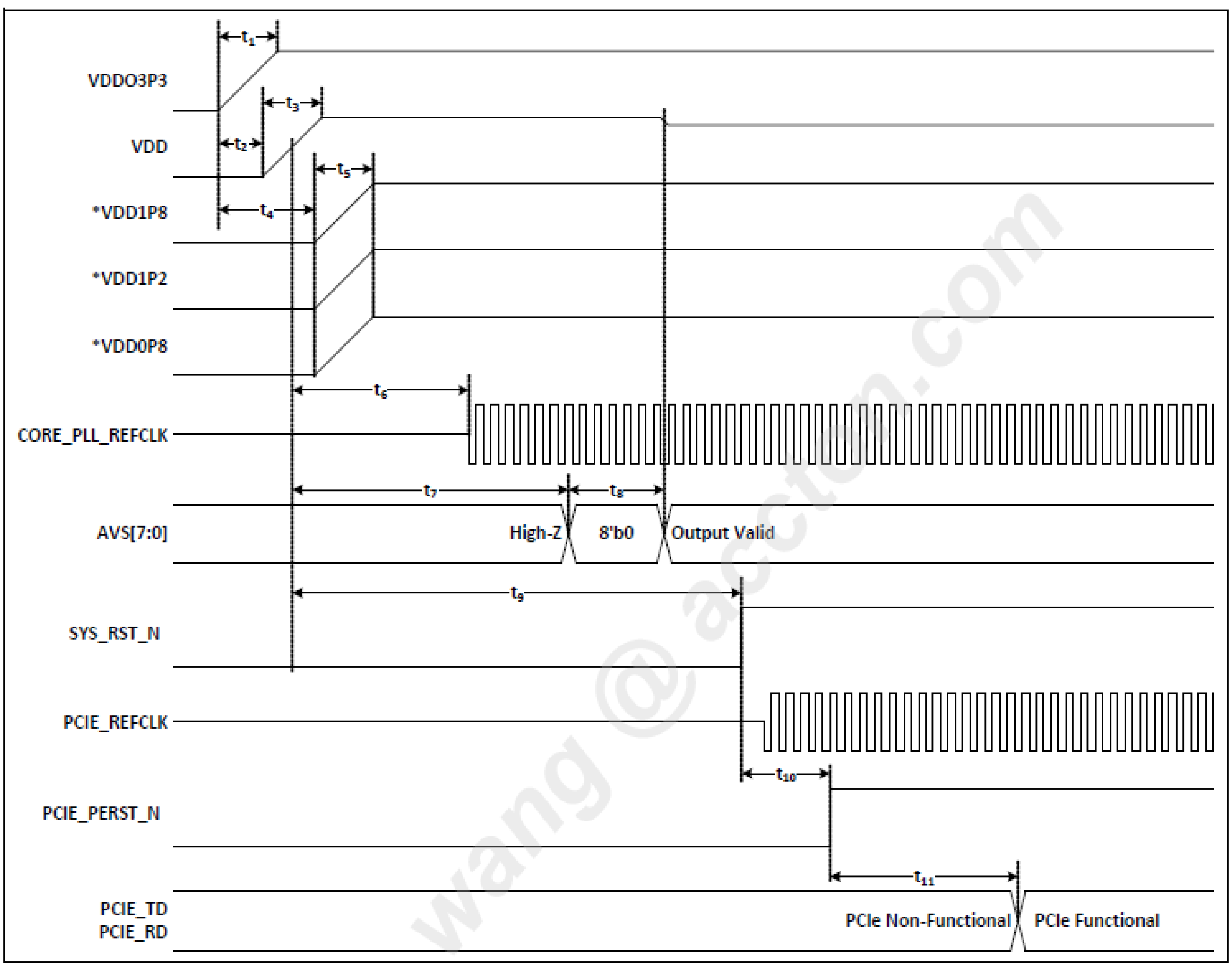
Pin Number	Pin Name	Function Description
AU27	BSC_DEBUG_MODE_RESERVED	*0:PCIe is enabled(BSC master supported, not BSC slave mode) 1:Reserved mode

N32	EEPROM_LOAD_EN_RESERVED	*0:EEPROM load not enable 1:EEPROM load enable
Y36	MDIO_22_SEL	Pull-L: Clause 45(MIIM logic 1.2V) *Pull-H: Clause 22(MIIM logic 2.5V/3.3V)

4.1.1. POR of MAC (BCM56870)

The detailed power-on reset (POR) flow is as follows:

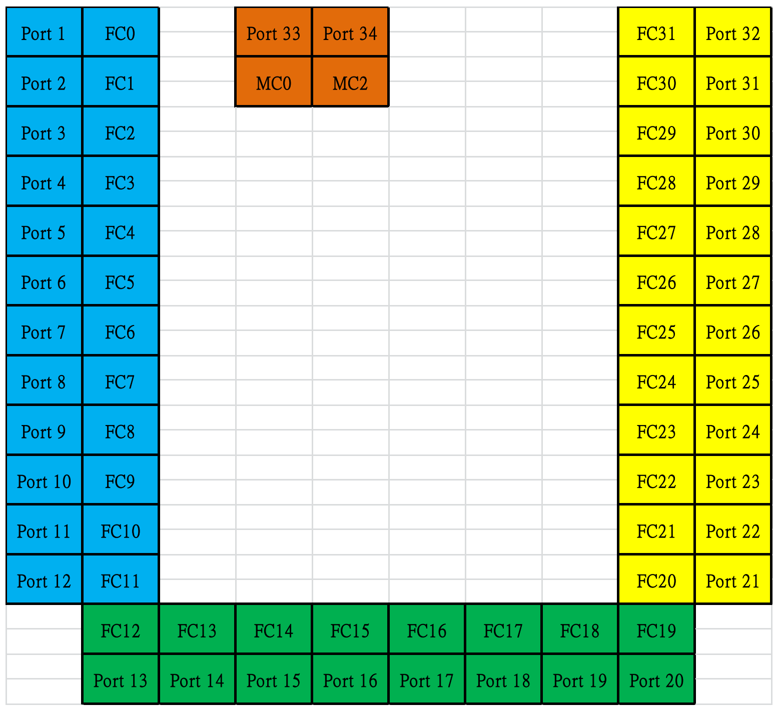
1. The recommend power-up voltage sequence is from highest 3.3V to VDD1V0_ROV and 0.8V, 1.2V, 1.8V can ramp up until VDD1V0_ROV reaches 0.55V.
2. 3.3V : ramp up time min = 660us , max = 10ms.
3. VDD1V0_ROV : ramp up time min = 50us , max = 10ms.
4. 0.8V, 1.2V, 1.8V : ramp up time min = 100us , max = 10ms.
5. Minimum system reset de-asserted time is 80ms.



4.1.2. Software Configurations of MAC (BCM56870)

4.2. Port Mapping

Figure 4-1 Physical Port mapping



CE	CE0	CE2	CE4	CE6	CE8	CE10	CE12	CE14	CE16	CE18	CE20	CE22	CE24	CE26	CE28	CE30
Port	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
Port	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32
CE	CE1	CE3	CE5	CE7	CE9	CE11	CE13	CE15	CE17	CE19	CE21	CE23	CE25	CE27	CE29	CE31

Table 4-1 Switch Port MAPPING TABLE

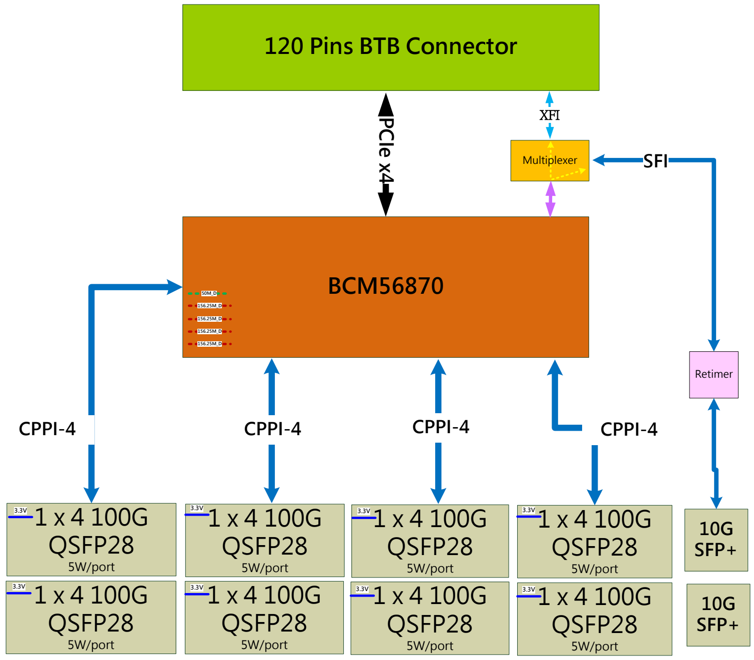
FalconCore	Mac(BCM56870)		ZQSFP+ Connector Location	Connector		Port Number (front-end)
	TX polarity (TD)	RX polarity (RD)		TX polarity	RX polarity	
FC[31:0]	FC[31:0]_TD0[P FC[31:0]_TD1[P FC[31:0]_TD2[P FC[31:0]_TD3[P	FC[31:0]_RD0[F FC[31:0]_RD1[F FC[31:0]_RD2[F FC[31:0]_RD3[F	U?	TX1_[P:N] TX2_[P:N] TX3_[P:N] TX4_[P:N]	RX1_[P:N] RX2_[P:N] RX3_[P:N] RX4_[P:N]	Port[32:1]
FC0	FC0_TD0[P:N] FC0_TD1[N:P] FC0_TD2[P:N] FC0_TD3[N:P]	FC0_RD0[P:N] FC0_RD3[N:P] FC0_RD1[P:N] FC0_RD2[N:P]	U42	FC0_TD0[P:N] FC0_TD1[P:N] FC0_TD2[P:N] FC0_TD3[P:N]	FC0_RD0[P:N] FC0_RD1[P:N] FC0_RD2[P:N] FC0_RD3[P:N]	Port 1
FC1	FC1_TD0[P:N] FC1_TD1[N:P] FC1_TD2[P:N] FC1_TD3[N:P]	FC1_RD3[N:P] FC1_RD2[P:N] FC1_RD1[N:P] FC1_RD0[P:N]	U59	FC1_TD0[P:N] FC1_TD1[P:N] FC1_TD2[P:N] FC1_TD3[P:N]	FC1_RD0[P:N] FC1_RD1[P:N] FC1_RD2[P:N] FC1_RD3[P:N]	Port 2
FC2	FC2_TD0[N:P] FC2_TD1[P:N] FC2_TD2[N:P] FC2_TD3[P:N]	FC2_RD3[N:P] FC2_RD2[P:N] FC2_RD1[N:P] FC2_RD0[N:P]	U43	FC2_TD0[P:N] FC2_TD1[P:N] FC2_TD2[P:N] FC2_TD3[P:N]	FC2_RD0[P:N] FC2_RD1[P:N] FC2_RD2[P:N] FC2_RD3[P:N]	Port 3
FC3	FC3_TD0[N:P] FC3_TD1[P:N] FC3_TD2[N:P] FC3_TD3[P:N]	FC3_RD3[P:N] FC3_RD2[N:P] FC3_RD1[P:N] FC3_RD0[N:P]	U60	FC3_TD0[P:N] FC3_TD1[P:N] FC3_TD2[P:N] FC3_TD3[P:N]	FC3_RD0[P:N] FC3_RD1[P:N] FC3_RD2[P:N] FC3_RD3[P:N]	Port 4
FC4	FC4_TD3[N:P] FC4_TD2[P:N] FC4_TD1[N:P] FC4_TD0[P:N]	FC4_RD0[N:P] FC4_RD1[P:N] FC4_RD2[N:P] FC4_RD3[P:N]	U44	FC4_TD3[P:N] FC4_TD2[P:N] FC4_TD1[P:N] FC4_TD0[P:N]	FC4_RD3[P:N] FC4_RD2[P:N] FC4_RD1[P:N] FC4_RD0[P:N]	Port 5
FC5	FC5_TD0[N:P] FC5_TD1[P:N] FC5_TD2[N:P] FC5_TD3[P:N]	FC5_RD3[P:N] FC5_RD2[N:P] FC5_RD1[P:N] FC5_RD0[N:P]	U61	FC5_TD0[P:N] FC5_TD1[P:N] FC5_TD2[P:N] FC5_TD3[P:N]	FC5_RD0[P:N] FC5_RD1[P:N] FC5_RD2[P:N] FC5_RD3[P:N]	Port 6
FC6	FC6_TD0[N:P] FC6_TD1[P:N] FC6_TD2[N:P] FC6_TD3[P:N]	FC6_RD3[N:P] FC6_RD2[P:N] FC6_RD1[P:N] FC6_RD0[N:P]	U45	FC6_TD0[P:N] FC6_TD1[P:N] FC6_TD2[P:N] FC6_TD3[P:N]	FC6_RD0[P:N] FC6_RD1[P:N] FC6_RD2[P:N] FC6_RD3[P:N]	Port 7
FC7	FC7_TD3[N:P] FC7_TD1[P:N] FC7_TD2[N:P] FC7_TD0[P:N]	FC7_RD3[P:N] FC7_RD0[N:P] FC7_RD1[P:N] FC7_RD2[N:P]	U62	FC7_TD3[P:N] FC7_TD2[P:N] FC7_TD1[P:N] FC7_TD0[P:N]	FC7_RD3[P:N] FC7_RD2[P:N] FC7_RD1[P:N] FC7_RD0[P:N]	Port 8
FC8	FC8_TD3[P:N] FC8_TD2[N:P] FC8_TD1[P:N] FC8_TD0[N:P]	FC8_RD3[P:N] FC8_RD2[N:P] FC8_RD1[P:N] FC8_RD0[N:P]	U46	FC8_TD0[P:N] FC8_TD1[P:N] FC8_TD2[P:N] FC8_TD3[P:N]	FC8_RD0[P:N] FC8_RD1[P:N] FC8_RD2[P:N] FC8_RD3[P:N]	Port 9
FC9	FC9_TD0[N:P] FC9_TD1[P:N] FC9_TD2[N:P] FC9_TD3[P:N]	FC9_RD0[P:N] FC9_RD1[N:P] FC9_RD2[P:N] FC9_RD3[N:P]	U63	FC9_TD0[P:N] FC9_TD1[P:N] FC9_TD2[P:N] FC9_TD3[P:N]	FC9_RD0[P:N] FC9_RD1[P:N] FC9_RD2[P:N] FC9_RD3[P:N]	Port 10
FC10	FC10_TD3[P:N] FC10_TD2[N:P] FC10_TD1[P:N] FC10_TD0[N:P]	FC10_RD3[P:N] FC10_RD2[N:P] FC10_RD1[P:N] FC10_RD0[N:P]	U47	FC10_TD0[P:N] FC10_TD1[P:N] FC10_TD2[P:N] FC10_TD3[P:N]	FC10_RD0[P:N] FC10_RD1[P:N] FC10_RD2[P:N] FC10_RD3[P:N]	Port 11
FC11	FC11_TD0[N:P] FC11_TD1[P:N] FC11_TD2[N:P] FC11_TD3[P:N]	FC11_RD0[P:N] FC11_RD1[N:P] FC11_RD2[P:N] FC11_RD3[N:P]	U64	FC11_TD0[P:N] FC11_TD1[P:N] FC11_TD2[P:N] FC11_TD3[P:N]	FC11_RD0[P:N] FC11_RD1[P:N] FC11_RD2[P:N] FC11_RD3[P:N]	Port 12
FC12	FC12_TD2[N:P] FC12_TD3[N:P] FC12_TD1[N:P] FC12_TD0[N:P]	FC12_RD1[N:P] FC12_RD3[P:N] FC12_RD0[N:P] FC12_RD2[P:N]	U48	FC12_TD2[P:N] FC12_TD3[N:P] FC12_TD0[N:P] FC12_TD1[P:N]	FC12_RD2[N:P] FC12_RD3[N:P] FC12_RD0[N:P] FC12_RD1[N:P]	Port 13
FC13	FC13_TD3[P:N] FC13_TD2[N:P] FC13_TD1[P:N] FC13_TD0[N:P]	FC13_RD3[N:P] FC13_RD0[P:N] FC13_RD2[N:P] FC13_RD3[N:P]	U65	FC13_TD3[P:N] FC13_TD2[P:N] FC13_TD1[P:N] FC13_TD0[P:N]	FC13_RD3[N:P] FC13_RD2[N:P] FC13_RD1[N:P] FC13_RD0[N:P]	Port 14
FC14	FC14_TD2[N:P] FC14_TD1[N:P] FC14_TD0[P:N] FC14_TD3[P:N]	FC14_RD1[P:N] FC14_RD0[N:P] FC14_RD3[P:N] FC14_RD2[N:P]	U49	FC14_TD2[P:N] FC14_TD3[N:P] FC14_TD0[N:P] FC14_TD1[N:P]	FC14_RD2[N:P] FC14_RD3[N:P] FC14_RD0[N:P] FC14_RD1[N:P]	Port 15
FC15	FC15_TD0[P:N] FC15_TD3[P:N] FC15_TD2[P:N] FC15_TD1[P:N]	FC15_RD3[N:P] FC15_RD2[N:P] FC15_RD1[N:P] FC15_RD0[N:P]	U66	FC15_TD0[N:P] FC15_TD1[P:N] FC15_TD2[P:N] FC15_TD3[P:N]	FC15_RD0[P:N] FC15_RD1[P:N] FC15_RD2[P:N] FC15_RD3[P:N]	Port 16

FalconCore	Mac(BCM56870)		ZQSFP+ Connector Location	Connector		Port Number (front-end)
	TX polarity (TD)	RX polarity (RD)		TX polarity	RX polarity	
FC16	FC16_TD3[N:P] FC16_TD1[P:N] FC16_TD2[P:N] FC16_TD0[P:N]	FC16_RD2[P:N] FC16_RD3[N:P] FC16_RD0[P:N] FC16_RD1[N:P]	U50	FC16_TD2[N:P] FC16_TD3[P:N] FC16_TD0[P:N] FC16_TD1[P:N]	FC16_RD2[P:N] FC16_RD3[P:N] FC16_RD0[P:N] FC16_RD1[P:N]	Port 17
FC17	FC17_TD0[N:P] FC17_TD1[P:N] FC17_TD2[N:P] FC17_TD3[P:N]	FC17_RD1[P:N] FC17_RD0[N:P] FC17_RD3[P:N] FC17_RD2[N:P]	U67	FC17_TD3[P:N] FC17_TD2[P:N] FC17_TD1[P:N] FC17_TD0[P:N]	FC17_RD3[P:N] FC17_RD2[P:N] FC17_RD1[P:N] FC17_RD0[P:N]	Port 18
FC18	FC18_TD3[P:N] FC18_TD2[N:P] FC18_TD1[P:N] FC18_TD0[N:P]	FC18_RD2[P:N] FC18_RD3[N:P] FC18_RD0[P:N] FC18_RD1[N:P]	U56	FC18_TD2[P:N] FC18_TD3[N:P] FC18_TD0[N:P] FC18_TD1[N:P]	FC18_RD2[P:N] FC18_RD3[P:N] FC18_RD0[P:N] FC18_RD1[P:N]	Port 19
FC19	FC19_TD1[P:N] FC19_TD2[N:P] FC19_TD0[P:N] FC19_TD3[N:P]	FC19_RD2[P:N] FC19_RD3[P:N] FC19_RD1[P:N] FC19_RD0[P:N]	U73	FC19_TD3[P:N] FC19_TD2[P:N] FC19_TD1[P:N] FC19_TD0[P:N]	FC19_RD3[P:N] FC19_RD2[N:P] FC19_RD1[P:N] FC19_RD0[P:N]	Port 20
FC20	FC20_TD0[P:N] FC20_TD1[N:P] FC20_TD2[N:P] FC20_TD3[N:P]	FC20_RD0[P:N] FC20_RD2[N:P] FC20_RD1[P:N] FC20_RD3[N:P]	U51	FC20_TD0[N:P] FC20_TD1[N:P] FC20_TD2[N:P] FC20_TD3[N:P]	FC20_RD0[P:N] FC20_RD1[P:N] FC20_RD2[P:N] FC20_RD3[P:N]	Port 21
FC21	FC21_TD3[P:N] FC21_TD2[N:P] FC21_TD1[P:N] FC21_TD0[N:P]	FC21_RD3[P:N] FC21_RD2[N:P] FC21_RD1[P:N] FC21_RD0[N:P]	U68	FC21_TD0[P:N] FC21_TD1[P:N] FC21_TD2[P:N] FC21_TD3[P:N]	FC21_RD0[P:N] FC21_RD1[P:N] FC21_RD2[P:N] FC21_RD3[P:N]	Port 22
FC22	FC22_TD0[N:P] FC22_TD1[P:N] FC22_TD2[N:P] FC22_TD3[P:N]	FC22_RD0[P:N] FC22_RD1[N:P] FC22_RD2[P:N] FC22_RD3[N:P]	U52	FC22_TD0[P:N] FC22_TD1[P:N] FC22_TD2[P:N] FC22_TD3[P:N]	FC22_RD0[P:N] FC22_RD1[P:N] FC22_RD2[P:N] FC22_RD3[P:N]	Port 23
FC23	FC23_TD3[P:N] FC23_TD2[N:P] FC23_TD1[P:N] FC23_TD0[N:P]	FC23_RD3[N:P] FC23_RD2[P:N] FC23_RD1[N:P] FC23_RD0[P:N]	U69	FC23_TD0[P:N] FC23_TD1[P:N] FC23_TD2[P:N] FC23_TD3[P:N]	FC23_RD0[P:N] FC23_RD1[P:N] FC23_RD2[P:N] FC23_RD3[P:N]	Port 24
FC24	FC24_TD3[N:P] FC24_TD2[P:N] FC24_TD1[N:P] FC24_TD0[P:N]	FC24_RD2[P:N] FC24_RD1[N:P] FC24_RD0[P:N] FC24_RD3[N:P]	U53	FC24_TD0[N:P] FC24_TD1[N:P] FC24_TD2[N:P] FC24_TD3[N:P]	FC24_RD0[P:N] FC24_RD1[N:P] FC24_RD2[P:N] FC24_RD3[N:P]	Port 25
FC25	FC25_TD0[P:N] FC25_TD1[N:P] FC25_TD2[P:N] FC25_TD3[N:P]	FC25_RD3[P:N] FC25_RD2[N:P] FC25_RD1[N:P] FC25_RD0[P:N]	U70	FC25_TD3[P:N] FC25_TD2[P:N] FC25_TD1[P:N] FC25_TD0[P:N]	FC25_RD3[P:N] FC25_RD2[P:N] FC25_RD1[P:N] FC25_RD0[P:N]	Port 26
FC26	FC26_TD0[P:N] FC26_TD1[N:P] FC26_TD2[P:N] FC26_TD3[N:P]	FC26_RD3[N:P] FC26_RD2[P:N] FC26_RD1[N:P] FC26_RD0[P:N]	U57	FC26_TD3[P:N] FC26_TD2[P:N] FC26_TD1[P:N] FC26_TD0[P:N]	FC26_RD3[P:N] FC26_RD2[P:N] FC26_RD1[P:N] FC26_RD0[P:N]	Port 27
FC27	FC27_TD3[P:N] FC27_TD2[N:P] FC27_TD1[P:N] FC27_TD0[N:P]	FC27_RD0[P:N] FC27_RD1[N:P] FC27_RD2[P:N] FC27_RD3[N:P]	U74	FC27_TD0[P:N] FC27_TD1[P:N] FC27_TD2[P:N] FC27_TD3[P:N]	FC27_RD0[P:N] FC27_RD1[P:N] FC27_RD2[P:N] FC27_RD3[P:N]	Port 28
FC28	FC28_TD0[P:N] FC28_TD1[N:P] FC28_TD2[P:N] FC28_TD3[N:P]	FC28_RD3[N:P] FC28_RD2[P:N] FC28_RD1[N:P] FC28_RD0[P:N]	U54	FC28_TD3[P:N] FC28_TD2[P:N] FC28_TD1[P:N] FC28_TD0[P:N]	FC28_RD3[P:N] FC28_RD2[P:N] FC28_RD1[P:N] FC28_RD0[P:N]	Port 29
FC29	FC29_TD0[P:N] FC29_TD1[N:P] FC29_TD2[P:N] FC29_TD3[N:P]	FC29_RD3[P:N] FC29_RD2[N:P] FC29_RD1[P:N] FC29_RD0[N:P]	U71	FC29_TD3[P:N] FC29_TD2[P:N] FC29_TD1[P:N] FC29_TD0[P:N]	FC29_RD3[P:N] FC29_RD2[P:N] FC29_RD1[P:N] FC29_RD0[P:N]	Port 30
FC30	FC30_TD0[P:N] FC30_TD1[N:P] FC30_TD2[P:N] FC30_TD3[N:P]	FC30_RD3[N:P] FC30_RD2[P:N] FC30_RD1[N:P] FC30_RD0[P:N]	U55	FC30_TD3[P:N] FC30_TD2[P:N] FC30_TD1[P:N] FC30_TD0[P:N]	FC30_RD3[P:N] FC30_RD2[P:N] FC30_RD1[P:N] FC30_RD0[P:N]	Port 31
FC31	FC31_TD0[P:N] FC31_TD1[P:N] FC31_TD2[N:P] FC31_TD3[P:N]	FC31_RD3[P:N] FC31_RD2[N:P] FC31_RD1[P:N] FC31_RD0[P:N]	U72	FC31_TD3[P:N] FC31_TD2[P:N] FC31_TD1[P:N] FC31_TD0[P:N]	FC31_RD3[P:N] FC31_RD2[P:N] FC31_RD1[P:N] FC31_RD0[P:N]	Port 32
MC 0	MC_TD0[P:N]	MC_RD0[P:N]		MC_TD0[P:N]	MC_RD0[P:N]	Port 33
MC 2	MC_TD2[P:N]	MC_RD2[P:N]		MC_TD2[P:N]	MC_RD2[P:N]	Port 34

4.3. 10G/40G/ 100G Interface

The AS7726-32X is phy-less system, BCM56870 connects with QSFP28 directly and SFP+ via a multiplexer. CPU control of the transceiver's I2C and status is via CPLD.

Figure 4-2 10G/40G/100G Interface Connection



4.4. LED interface

The BCM56870's three separate LED interfaces: LED-0, LED-1

- LED-0 provides port status for ports 17-23.
- LED-1 provides port status for ports 1-16.

Port status information includes link status, transmit and receive activity, and speed settings

LED0 stream

The sequence of LED0 is as below. The port status of lane 99 arrives first and lane 13's LED status arrives last.

CE24		Port	17	CE25		Port	18	CE26		Port	19	CE27		Port	20
99	100	97	98	104	103	102	101	107	108	105	106	112	111	110	109
2	3	0	1	3	2	1	0	2	3	0	1	3	2	1	0
CE4		Port	21	CE5		Port	22	CE6		Port	23	CE7		Port	24
17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
CE28		Port	25	CE29		Port	26	CE30		Port	27	CE31		Port	28
113	114	115	116	120	119	118	117	124	123	122	121	125	126	127	128
0	1	2	3	3	2	1	0	3	2	1	0	0	1	2	3
CE0		Port	29	CE1		Port	30	CE2		Port	31	CE3		Port	32
4	3	2	1	8	7	6	5	12	11	10	9	16	15	14	13
3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0

Table 4-2 LED0 stream TABLE

LED1 stream

The sequence of LED1 is as below. The port status of lane 49 arrives first and lane 95's LED status arrives last.

CE12		Port	1	CE13		Port	2	CE14		Port	3	CE15		Port	4
49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
CE16		Port	5	CE17		Port	6	CE18		Port	7	CE19		Port	8
68	67	66	65	69	70	71	72	73	74	75	76	80	79	78	77
3	2	1	0	0	1	2	3	0	1	2	3	3	2	1	0
CE8		Port	9	CE9		Port	10	CE10		Port	11	CE11		Port	12
33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
CE20		Port	13	CE21		Port	14	CE22		Port	15	CE23		Port	16
83	84	81	82	88	87	86	85	91	92	89	90	93	94	95	96
2	3	0	1	3	2	1	0	2	3	0	1	0	1	2	3

Table 4-3 LED1 stream TABLE

The interface to the LED status indicators is implemented through a serial protocol carried out on two pins: LED_CLK and LED_DATA. If there are n LED status lights, it takes nclock cycles to shift the data out of the LED interface. The shifted-out LED data is out-of-phase with respect to the LED_CLK. After all n bits have been shifted out, the LED_CLK and LED_DATA lines go idle until the next time the LED status is refreshed. An external shift register is responsible for holding the state of the LED status between scan (refresh) events.

Figure 20: LED_CLK/LED_DATA Refresh Interval

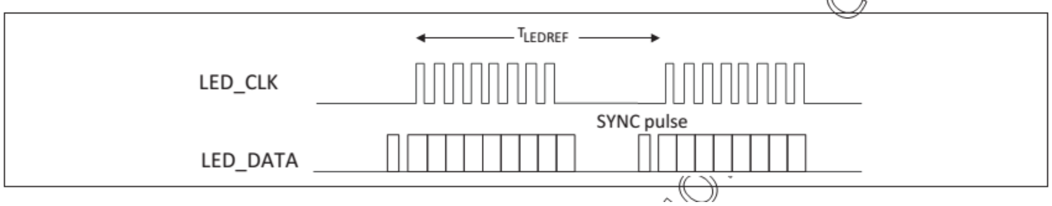


Figure 4-3 LED bus

LED stream format:

There have four lanes per port. MAC will send lane[1:0] first, then send speed[1:0] and link-up/activity information per lane. A port will have 14 bits information. A LED bus is for 16 ports, so the total bits per led bus is 224 bits.

Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port_N													
		Lane 1			Lane 2			Lane 3			Lane 4		
Lane [1:0]		Speed [1:0]		Link-up / Activity	Speed [1:0]		Link-up / Activity	Speed [1:0]		Link-up / Activity	Speed [1:0]		Link-up / Activity
Port_N+1													
		Lane 1			Lane 2			Lane 3			Lane 4		
Lane [1:0]		Speed [1:0]		Link-up / Activity	Speed [1:0]		Link-up / Activity	Speed [1:0]		Link-up / Activity	Speed [1:0]		Link-up / Activity
…													
…													
…													

Table 4-4 LED stream format

Speed [1:0] shows the lane speed. Lane[1:0] shows the lane number for a port. So the lane[1:0] and speed[1:0] shows the port configuration.

The bit of link-up/ Activity control the LED on/ off / toggle.

Lane Speed	Speed [1:0]
reserve	11
25G	10
20G	01
10G	00

Lane Number	Lane [1:0]
reserve	11
4	10
2	01
1	00

Port configuration	Lane [1:0]	Speed [1:0]
100G	10	10
~~80G~~	~~10~~	~~01~~
40G	10	00
~~2x50G~~	~~01~~	~~10~~
~~2x40G~~	~~01~~	~~01~~
~~2x20G~~	~~01~~	~~00~~
4x25G	00	10
~~4x20G~~	~~00~~	~~01~~
4x10G	00	00

Link-up / Activity	LED
1	ON
0	OFF
Toggle	Activity

Table 4-5 LED Bit Description

If the lane[1:0] is "10", the link-up/ activity bit of first lane will be active and other lanes will be inactive. If the lane[1:0] is "01", the link-up/ activity bit of first and three lane will be active and other lanes will be inactive. If the lane[1:0] is '00", the link-up/ activity bit of all lanes will be active.

4.5. QSFP28

The AS7726-32X has 32 x QSFP28 ports, and each QSFP28 port can support 100Gbps. The QSFP28 port supports optical transceiver and DAC. The power class can support up to 5W.

5. Sub-system

5.1. Management PHY (BCM54616S)

The management port support 10/ 100/ 1000M Ethernet speed.

5.1.1. Configurations of PHY (BCM54616S)

Pin Number	Pin Name	Function Description
G7 G6 H6 G10	LED1 LED2 LED3 LED4	LED1 High >> Copper AN enable LED2 High >> Full-duplex LED3 High >> LED4 High >> AN at 10/100/1000BASE-T
F5 H5	MODE_SEL_0 MODE_SEL_1	MODE_SEL[1:0] * 01 RGMII (2.5V) 10 RGMII (HSTL1.8V) 11 RGMII (3.3V) 00 RGMII (3.3V)
H10 J0 J9 K10 K9	PHY_ADDR_0 PHY_ADDR_1 PHY_ADDR_2 PHY_ADDR_3 PHY_ADDR_4	ADDR = 00001

5.1.2. POR of PHY (BCM54616S)

The detailed power-on reset (POR) flow is as follows:

1. 3.3V up and Ref clock up
2. 3.3V enable MPS1484 to generate 2.5V
3. All powers are stable, POWR607 inform CPLD
4. CPLD receive the signal, CPLD assert Reset_N high

5.2. I2C

The CPU has one I2C channels for our application. The I2C used for system peripheral access include SODIMM, RTC and DC/DC. The I2C_0 and I2C_1 are for Mainboard function used.

Figure 5-1 Switch board I2C Connection

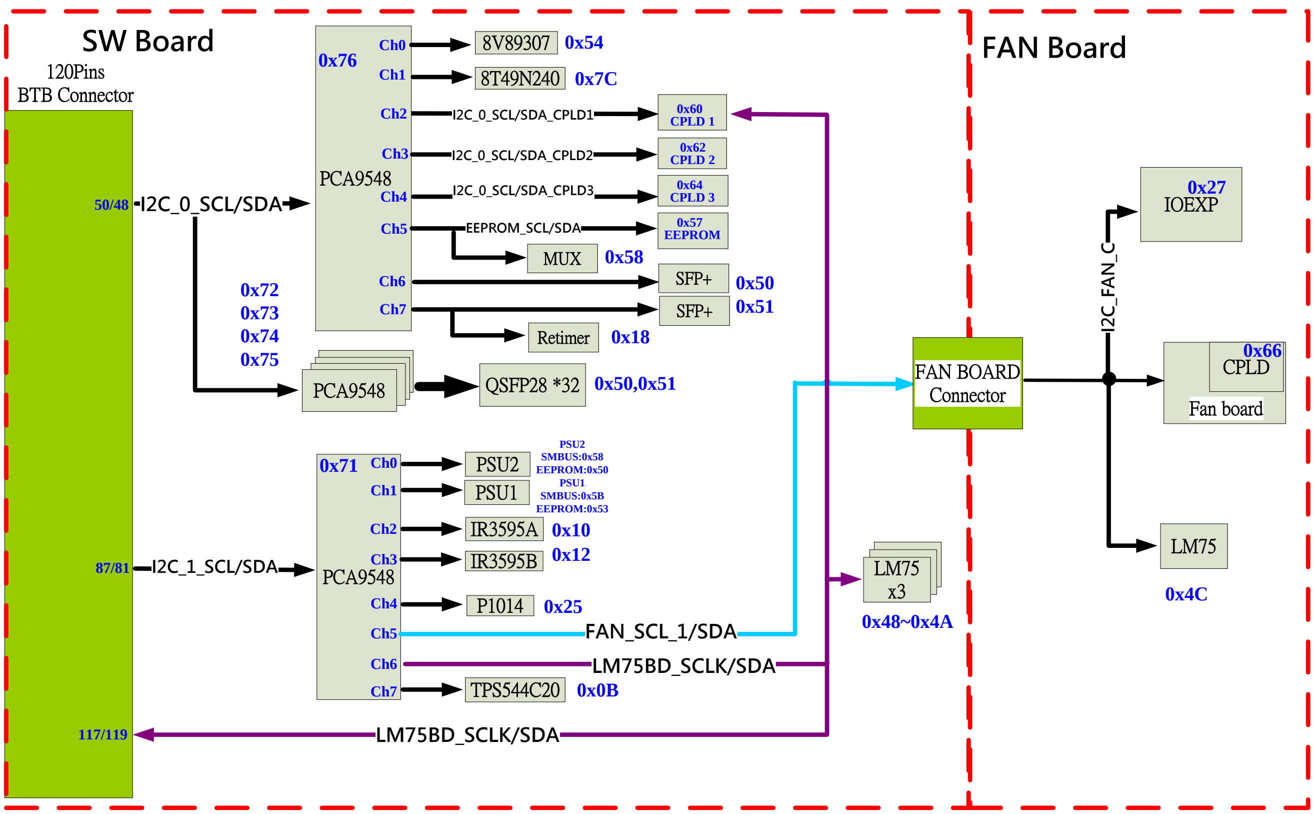
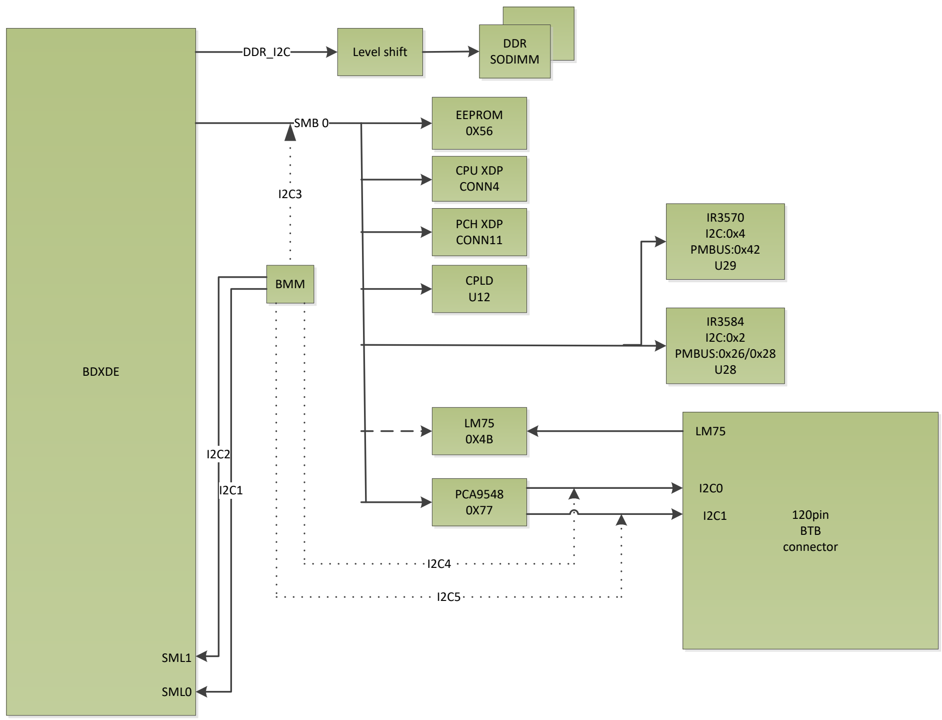


Figure 5-2 CPU board I2C Connection



Note: I2C[1:5] are from the BMM point of view, not related to the I2C[0:1] through the B2B CONN

Table 5-1 Switch board I2C Address Table

	Channel	Device	Address
CPU	SMB_9548_i	I2C switch (77)	77
I2C switch (77)	I2C 0	I2C switch (76)	76
		I2C switch (72)	72
		I2C switch (73)	73
		I2C switch (74)	74
		I2C switch (75)	75
	I2C 1	I2C switch (71)	71
I2C switch (76)	switch_CH0	8V89307	54
	switch_CH1	8T49N240	7C
	switch_CH2	CPLD1	60
	switch_CH3	CPLD2	62
	switch_CH4	CPLD3	64
	switch_CH5	EEPROM (Reserved)	57
		Multiplexer	58

	switch_CH6	SFP+ PORT 33	50, 51
	switch_CH7	SFP+ PORT 34	50, 51
		DS100DF410	0x18
I2C switch (72)	switch_CH0	QSFP28 PORT 9	50, 51
	switch_CH1	QSFP28 PORT 10	50, 51
	switch_CH2	QSFP28 PORT 11	50, 51
	switch_CH3	QSFP28 PORT 12	50, 51
	switch_CH4	QSFP28 PORT 1	50, 51
	switch_CH5	QSFP28 PORT 2	50, 51
	switch_CH6	QSFP28 PORT 3	50, 51
	switch_CH7	QSFP28 PORT 4	50, 51
I2C switch (73)	switch_CH0	QSFP28 PORT 6	50, 51
	switch_CH1	QSFP28 PORT 5	50, 51
	switch_CH2	QSFP28 PORT 8	50, 51
	switch_CH3	QSFP28 PORT 7	50, 51
	switch_CH4	QSFP28 PORT 13	50, 51
	switch_CH5	QSFP28 PORT 14	50, 51
	switch_CH6	QSFP28 PORT 15	50, 51
	switch_CH7	QSFP28 PORT 16	50, 51
I2C switch (74)	switch_CH0	QSFP28 PORT 17	50, 51
	switch_CH1	QSFP28 PORT 18	50, 51
	switch_CH2	QSFP28 PORT 19	50, 51
	switch_CH3	QSFP28 PORT 20	50, 51
	switch_CH4	QSFP28 PORT 25	50, 51
	switch_CH5	QSFP28 PORT 26	50, 51
	switch_CH6	QSFP28 PORT 27	50, 51
	switch_CH7	QSFP28 PORT 28	50, 51
I2C switch (75)	switch_CH0	QSFP28 PORT 29	50, 51
	switch_CH1	QSFP28 PORT 30	50, 51
	switch_CH2	QSFP28 PORT 31	50, 51
	switch_CH3	QSFP28 PORT 32	50, 51
	switch_CH4	QSFP28 PORT 21	50, 51
	switch_CH5	QSFP28 PORT 22	50, 51

	switch_CH6	QSFP28 PORT 23	50, 51
	switch_CH7	QSFP28 PORT 24	50, 51
I2C switch (71)	switch_CH0	PWR module2	58, 50
	switch_CH1	PWR module1	5B, 53
	switch_CH2	IR3595_A	10
	switch_CH3	IR3595_B	12
	switch_CH4	P1014	25
	switch_CH5	IO_expander	27
		Fan board CPLD	66
		Fan board LM75	4C
	switch_CH6	LM75*3	48,49,4A
		CPU's LM75	4B
	switch_CH7	TPS544C20	0B

Table 5-2 CPU board I2C Address Table

Device	I2C address	Note
DDR4 SODIMM 1	0x50	This device need to be accessed by DDR_I2C interface
DDR4 SODIMM 2	0x52	This device need to be accessed by DDR_I2C interface
LM75	0x4B	This device need to be accessed by main board CPLD, and not display at SMBus 0.
EEPROM	0x56	
IR3584 (I2C)	0x02	
IR3584 (PMBUS-Loop1)	0x26	
IR3584 (PMBus-Loop2)	0x28	
IR3570 (I2C)	0x4	

IR3570 (PMBus Loop1)	0x42	
PCA9548	0X77	

5.3. UART

The UART port will be configured to enable UART1 only and support RJ45 type.
The console port interface conforms to the RJ45 electrical specification.
The console port is located on the front panel. The interface supports asynchronous mode with default eight data bits, one stop bit, and no parity. The unit will operate at the following baud rates:

- **115200 (Default)**

Figure 5-3 Switch board Uart Connection

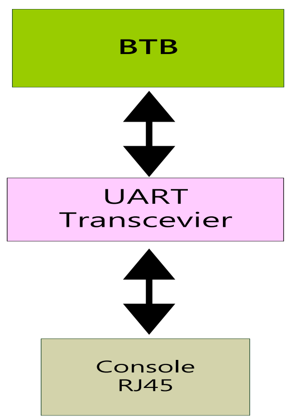


Figure 5-4 CPU board Uart Connection

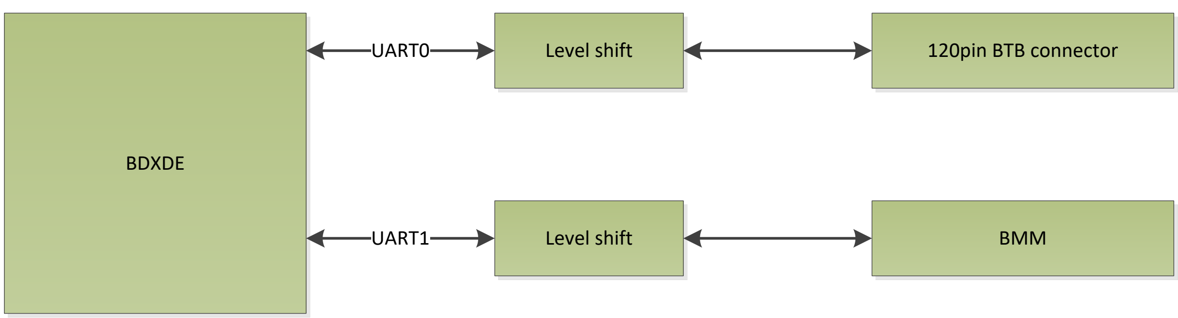


Table 5-3 RS-232 Pin definition (RJ45)

Pin number	Pin name	Pin number	Pin name
1	RTS	2	UART_TXD
3		4	
5	GND	6	UART_RxD
7		8	CTS

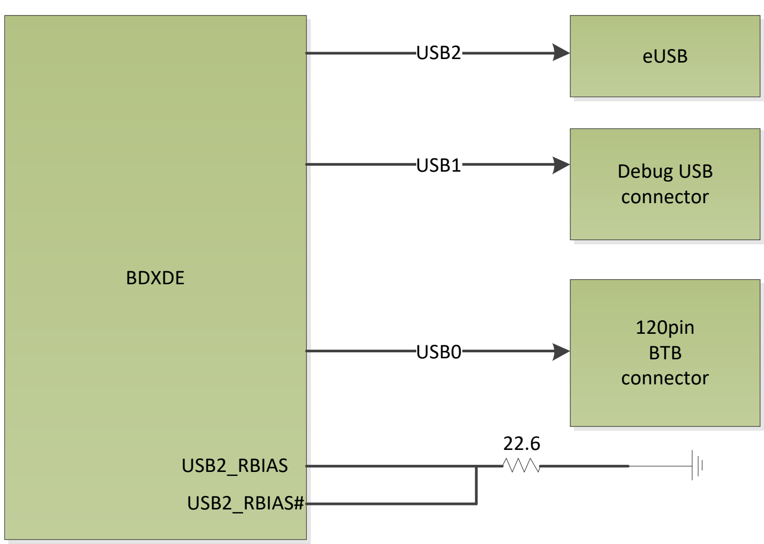
Table 5-4 CPU board CONN18 PIN ASSIGNMENT

Pin Number	Description
1	VCC
2	TX
3	RX
4	GND

5.4. USB

There are three USB 2.0 interfaces in the project. The USB-0 via the 120pins BTB connector to switch board for chassis external type A USB connector, USB-1 is for debug function and USB-2 connect to eUSB module for internal USB access.
The mapping table and connection are as below.

Figure 5-5 USB Connection

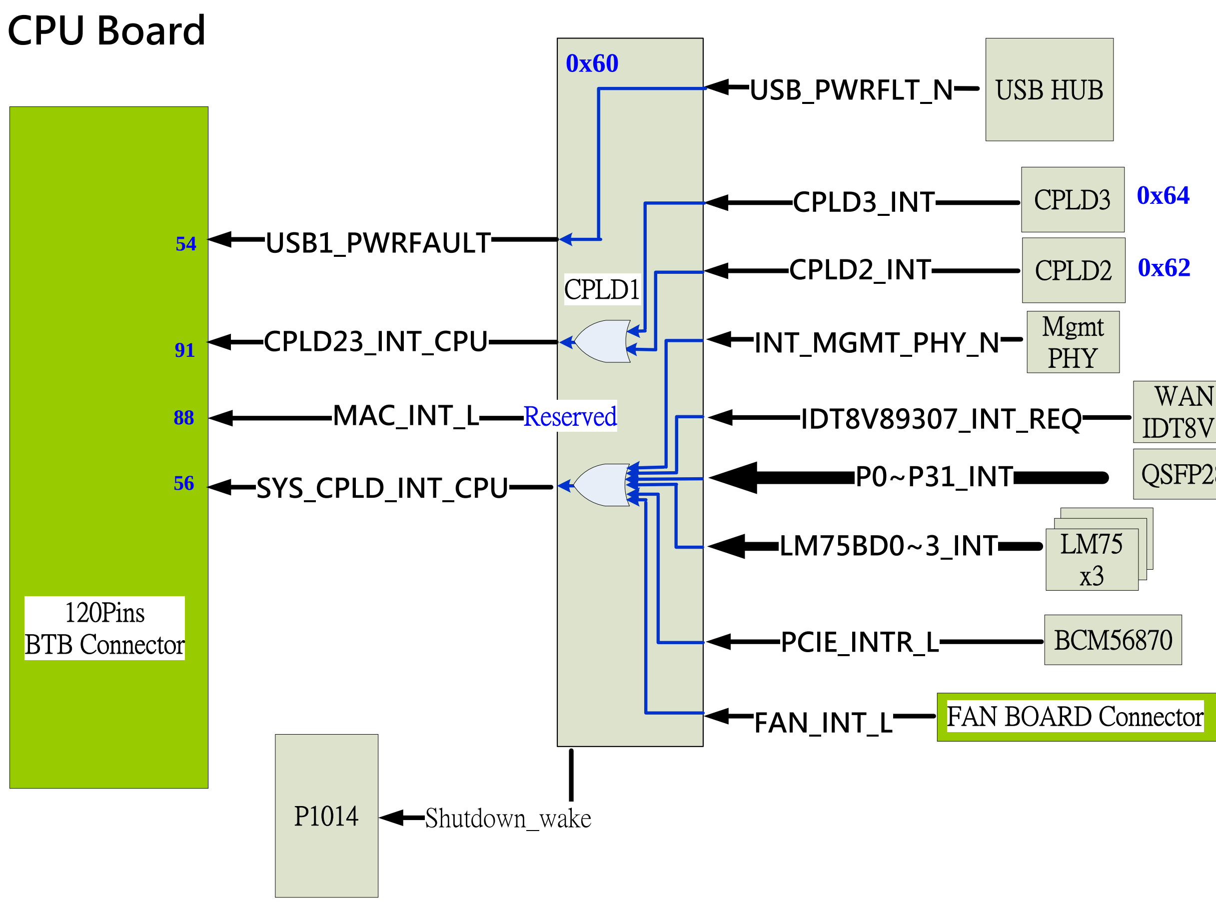


5.5. Interrupt

The CPLD in Switch board will collect all interrupts in Switch board from different devices, and then pass to CPU. Those devices are as below.

- MAC (BCM56870)
- Mgmt Phy(BCM54616s)
- Thermal sensor(LM75)
- Fan
- IDT 8V89307
- QSFP28 transcevier

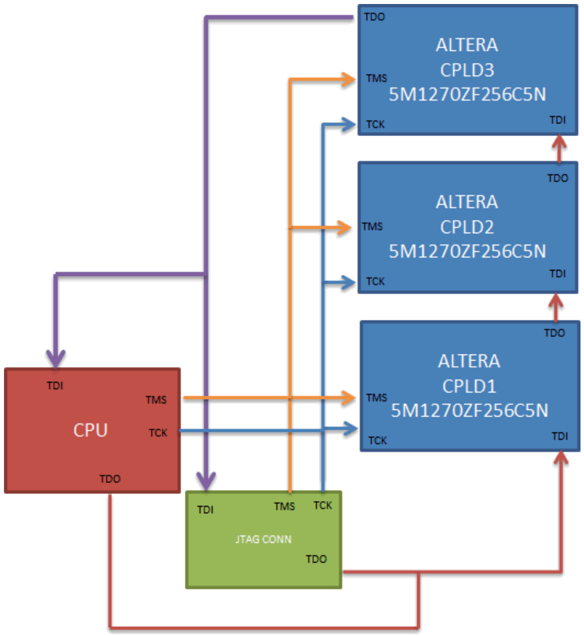
Figure 5-6 Interrupt Connection



5.6. JTAG

The AS7726-32X download chain for three CPLD with a JTAG interface, it makes the CPLD programing more quickly. The TCK and TMS pass to all devices by buffer. TDI and TDI are connecting directly.

Figure 5-7 JTAG chain



5.7. Thermal system

5.7.1. Temperature sensor

There are five temperature sensors in AS7726-32XBT system, and the locations are shown in the picture below. CPU can access the sensor via I2C interface, and the sensor has the interrupt signal connect with CPLD for over-temp event application.

The temp sensor solution is “LIN LM75BD 2.8-5.5V TEMP MINOTOR SO8 LT/LF NXP”

The thermal alarm will be 70 degree at initial value and it is via thermal sensor’s interrupt to CPU module. But the temperature value will be optimized after thermal test result.

Figure 5-8 Switch board - Temp sensor location

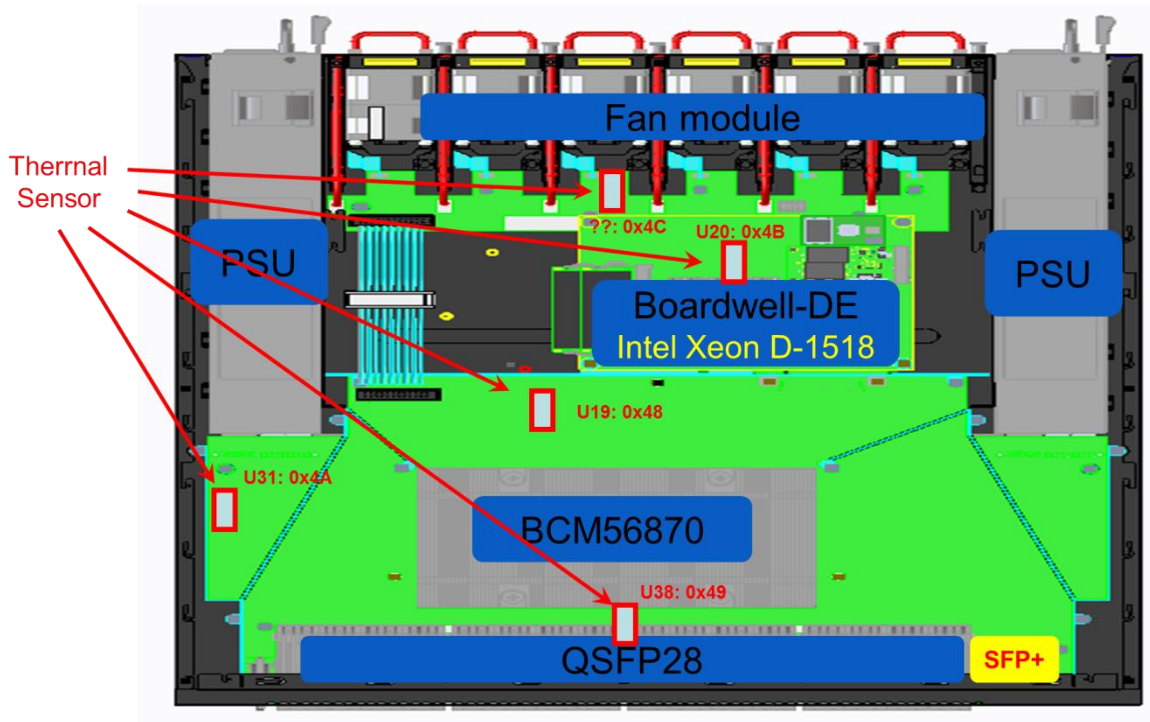
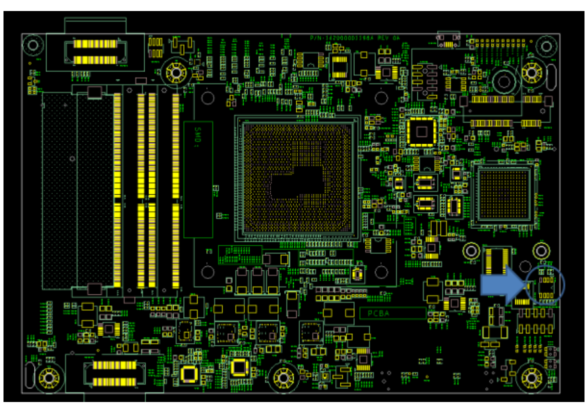
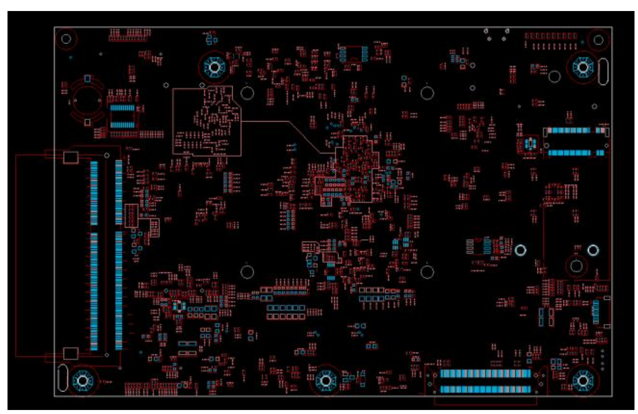


Figure 5-9 CPU board - Temp sensor location

Top	Bottom
	

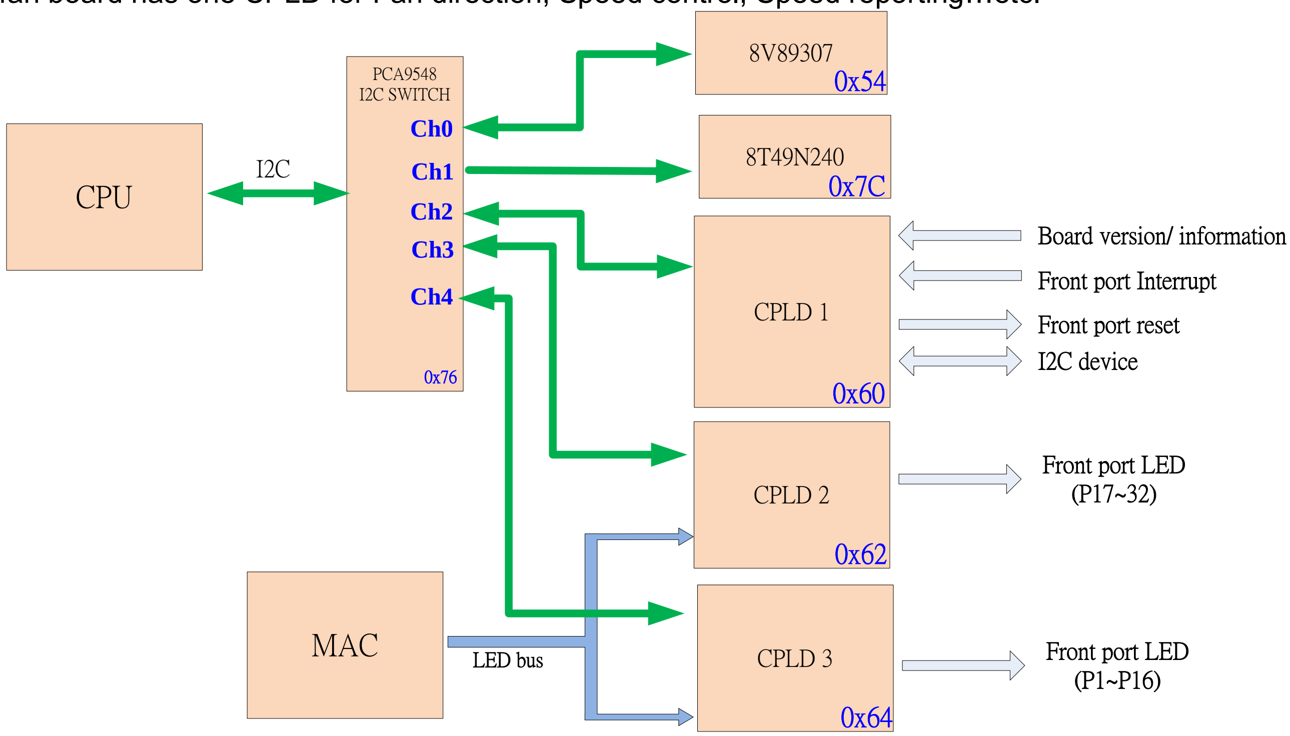
5.7.2. Fan controller system

The Fan board has a CPLD to do the fan controller function. The CPLD on the Fan board can control the Fan's PWM signal for adjust Fan speed and count the Fan's Tach signal for Fan speed reporting. CPU can read the thermal sensor to get thermal information, and then adjust Fan speed to reduce system's thermal. The Fan's CPLD had included I2C thermal watchdog to avoid system shutdown. If the register count to zero, the Fan speed will be set to high speed.

The CPLD information is “CPLD 5M1270ZF256C5N 3.3V FBGA256 LT/LF ALTERA”

5.8. CPLD

The AS7726-32X has three CPLDs for LED decoding, power module status,I2C switch, and System interrupt.
The fan board has one CPLD for Fan direction, Speed control, Speed reporting…etc.



These CPLDs are Altera MaxV EPM1270F256.

5.8.1. CPLD Field upgrade information

The system support CPLD field upgrade function for main CPLD and Fan CPLD.

5.8.1.1. JTAG connection

- Main board

Main board CPLD have three CPLD devices; CPLD1, CPLD2 and CPLD3. The updater can update three CPLD devices in same time. CPU connects with CPLD’s Jtag interface via CPU GPIO pin, and there has a JTAG chain in CPLD1, 2 and3.

- Fan board

Fan board has one CPLD device. The CPU connects with Fan CPLD Jtag interface via I2C expander IC. CPU use I2C expander to simulate JTAG signal for CPLD code update.

5.8.1.2. Upgrade procedure

- Command for main board CPLD upgrade:
  - **”TFTP_server_IP” : It is the IP address of TFTP server**
  - **”file_name.updater” : It is the file name of new CPLD image updater**

ONIE: / # update_url tftp://**”TFTP_server_IP”**/**”file_name**.updater”

5.8.1.3. Operational mode

The real-time ISP feature present in the Max V family is used for upgrade CPLD code.

5.8.1.4. Power cycling requirements

The system needs a power cycle after finish CPLD code update. It will run original CPLD code before power cycle.

5.9. IDT 8V89307

5.9.1. Configurations of IDT 8V89307

Pin Number	Pin Name	Function Description
J2	I2C_EN	0:SPI interface *1:I2C interface
E3	CS_B_ASEL0	6bit is fixed=>110011X ASEL0=0 ADD[6:0]=1100110
C2 D2	DPLL1_MOD_SEL0 DPLL1_MOD_SEL1	DPLL1_MOD_SEL[0:1] 00:Manual normal 01:Manual holdover mode 10:Manual free run mode 11:Automatic normal mode

5.9.2. POR of IDT 8V89307

The detailed power-on reset (POR) flow is as follows:

1. 3.3V up and Ref clock up

2. Then 3.3V enable MPS1482 to generate 1.8V

3. All power are stable, POWR607 inform CPLD

4. CPLD receive the signal, CPLD assert Reset_N high

5.10. Connector

5.10.1. Connector for CPU module

ES7632BT 120 Pin	ES7632BT 120 Pin	General	CONNECTOR				General	ES7632BT 120 Pin	ES7632BT 120 Pin
		Function		PIN #	PIN #		Function		
(I)LM75BD_SCLK	IN	TEMP_ANODE	IN/OUT	119	120	-	GND		GND
(IO)LM75BD_SDA	IN/OUT	TEMP_CATHODE	IN/OUT	117	118	OUT	10G_KR_TX0_P	OUT	CPU_XFI_MUX_TX_0P
GND		GND	-	115	116	OUT	10G_KR_TX0_N	OUT	CPU_XFI_MUX_TX_0N
CPU_MPHY_SGMII_TX_0_S_P	OUT	MPHY_SGMII_TX_P	OUT	113	114	-	GND		GND
CPU_MPHY_SGMII_TX_0_S_N	OUT	MPHY_SGMII_TX_N	OUT	111	112	-	GND		GND
GND		GND	-	109	110	IN	10G_KR_RX0_P	IN	CPU_XFI_MUX_RX_0P
MPHY_CPU_SGMII_RX_0_S_N	IN	MPHY_SGMII_RX_N	IN	107	108	IN	10G_KR_RX0_N	IN	CPU_XFI_MUX_RX_0N
MPHY_CPU_SGMII_RX_0_S_P	IN	MPHY_SGMII_RX_P	IN	105	106	-	GND		GND
GND		GND	-	103	104	-	GND		GND
CPU_MPHY_MDC	OUT	GPIO(MPHY_MDC)	OUT	101	102	IN	10G_KR_RX1_P	IN	CPU_XFI_MUX_RX_2P
Not Used		INTERRUPT(MPHY)	IN	99	100	IN	10G_KR_RX1_P	IN	CPU_XFI_MUX_RX_2N
CPU_MPHY_MDIO	IN/OUT	GPIO(MPHY_MDIO)	IN/OUT	97	98	-	GND		GND
GND		GND	-	95	96	-	GND		GND
IP_UART0_SOUT	IN	GPIO	IN/OUT	93	94	OUT	10G_KR_TX1_P	OUT	CPU_XFI_MUX_TX_2P
CPLD23_INT_CPU	IN		IN	91	92	OUT	10G_KR_TX1_N	OUT	CPU_XFI_MUX_TX_2N
1PPS_CPU	IN	GPIO	IN/OUT	89	90	-	GND		GND
I2C_1_SCL	OUT	I2C_1_SCL	OUT	87	88	-	GND		GND
CPU_PROCHOT				85	86	-	GND		GND
				83	84	IN/OUT	MGMT_USB_N	IN/OUT	USB2_N
I2C_1_SDA	IN/OUT	I2C_1_SDA	IN/OUT	81	82	IN/OUT	MGMT_USB_P	IN/OUT	USB2_P
UART1_CTS				79	80	-	GND		GND
CPU_TDI	IN	CPU_TDI	IN	77	78	OUT	HWIO	OUT	UCD9090_ALERT_L
UART1_TX	OUT	UART1_TX	OUT	75	76	OUT	MGMT_RS232_RTS	OUT	UART1_RTS
MAC_INT_L	IN	MAC_INT_L	IN	73	74	OUT	HWIO	OUT	RESET_SYS_CPLD
GND		GND	-	71	72	IN/OUT	GPIO	OUT	CPU_TMS
PCIE_OOB_TX_P	OUT	PCIE_OOB_TX_P	OUT	69	70	OUT	JTAG_TRST#	OUT	CPU_JTAG_RST
PCIE_OOB_TX_N	OUT	PCIE_OOB_TX_N	OUT	67	68	OUT	HWIO	IN	P1014_RST
GND		GND	-	65	66	IN/OUT	GPIO	OUT	CPU_TDO
UART1_RX	IN	UART1_RX	IN	63	64	IN/OUT	GPIO	OUT	CPU_TCK
GND		GND	-	61	62	IN/OUT	GPIO	OUT	IP_UART0_SIN
PCIE_OOB_RX_P	IN	PCIE_OOB_RX_P	IN	59	60	IN/OUT			
PCIE_OOB_RX_N	IN	PCIE_OOB_RX_P	IN	57	58	OUT			
GND		GND	-	55	56	IN	INTERRUPT	IN	SYS_CPLD_INT_CPU
GND		GND	-	53	54	OUT	HWIO	IN	USB1_PWRFAULT
CPU_PEX_PCIEA_TX_0_P	OUT	PCIE_TX_0_P	OUT	51	52	IN	RESET_MODULE_REQ#	IN	Manu_RST
CPU_PEX_PCIEA_TX_0_N	OUT	PCIE_TX_0_N	OUT	49	50	OUT	I2C_1_SCL	OUT	I2C_0_SCL
GND		GND	-	47	48	IN/OUT	I2C_1_SDA	IN/OUT	I2C_0_SDA
GND		GND	-	45	46	OUT	RESET_SYS_REQ#	OUT	RESET_MAC
CPU_PEX_PCIEA_TX_1_N	OUT	PCIE_TX_1_P	OUT	43	44	IN	SYS_PWR_GOOD	OUT	CPU_THERMALTRIP
CPU_PEX_PCIEA_TX_1_P	OUT	PCIE_TX_1_N	OUT	41	42	OUT	HWIO	OUT	USB1_VBUS
GND		GND	-	39	40	-	GND		GND
GND		GND	-	37	38	-	GND		GND
PEX_CPU_PCIEA_RX_0_N	IN	PCIE_RX_0_P	IN	35	36	OUT	PCIE_TX_2_P	OUT	CPU_PEX_PCIEB_TX_0_P
PEX_CPU_PCIEA_RX_0_P	IN	PCIE_RX_0_N	IN	33	34	OUT	PCIE_TX_2_N	OUT	CPU_PEX_PCIEB_TX_0_N
GND		GND	-	31	32	-	GND		GND
GND		GND	-	29	30	-	GND		GND
PEX_CPU_PCIEA_RX_1_N	IN	PCIE_RX_1_P	IN	27	28	IN	PCIE_RX_2_P	IN	PEX_CPU_PCIEB_RX_0_P
PEX_CPU_PCIEA_RX_1_P	IN	PCIE_RX_1_N	IN	25	26	IN	PCIE_RX_2_N	IN	PEX_CPU_PCIEB_RX_0_N
GND		GND	-	23	24	-	GND		GND
GND		GND	-	21	22	-	GND		GND
CPU_PEX_PCIEB_TX_1_N	OUT	PCIE_TX_3_N	OUT	19	20	IN	PCIE_RX_3_P	IN	PEX_CPU_PCIEB_RX_1_P
CPU_PEX_PCIEB_TX_1_P	OUT	PCIE_TX_3_P	OUT	17	18	IN	PCIE_RX_3_N	IN	PEX_CPU_PCIEB_RX_1_N
GND		GND	-	15	16	-	GND		GND
GND		GND	-	13	14	-	GND		GND
GND		GND	-	11	12	-	GND		GND
VCC12		12VDC	-	9	10	-	12VDC		VCC12
VCC12		12VDC	-	7	8	-	12VDC		VCC12
VCC5P0		5VDC	-	5	6	-	12VDC		VCC12
VCC5P0		5VDC	-	3	4	-	12VDC		VCC12
VCC5P0		5VDC	-	1	2	-	12VDC		VCC12

5.10.2. Connector for Fan board

Name	Type	Net Name	Description
1	power	VCC12	12V Power
2	power	VCC12	12V Power
3	power	VCC12	12V Power
4	power	VCC12	12V Power
5	power	GND	12V/ 3.3V return
6	power	GND	12V/ 3.3V return
7	power	GND	12V/ 3.3V return
8	power	VDD3P3	3.3V Power
9	out	FAN_IDLE	Enable/ disable the Fan baord's I2C Master
10	in	FAN_INT_L	Fan board send intrupt
11	power	GND	12V/ 3.3V return
12	power	GND	12V/ 3.3V return
13	in	FAN_SCL_2	For Fan CPLD access switch board's thermal sensor
14	inout	FAN_SDA_1	For CPU to access Fan CPLD status
15	inout	FAN_SDA_2	For Fan CPLD access switch board's thermal sensor
16	out	FAN_SCL_1	For CPU to access Fan CPLD status
17	power	GND	12V/ 3.3V return
18	power	GND	12V/ 3.3V return
19	power	GND	12V/ 3.3V return
20	power	GND	12V/ 3.3V return
21	power	VCC12	12V Power
22	power	VCC12	12V Power
23	power	VCC12	12V Power
24	power	VCC12	12V Power

6. Power Consumption

The total estimated power budget described in Table 2 is ~ 630W on the 32 x 100G switchboard with CPU system.
All calculating data are based on the maximum power dissipation in the spec of components. Combining the real measurement of simulated projects, the total power is less than this estimation by 1/4 ~ 1/3.

Table 6-1 Power Consumption Table

Power Consumption Estimation Table																
Voltage(V) / Current(mA)				ROV										(W)/device	Quantity	Total(W)
	1.8	1.2	0.6	1	1	1.05	1.3	1.7	1.5	3.3	5	3.3	12			
BDXDE	26000	3000				11283	500	350	162	487				65.34225	1	65.34225
SPI-Flash										50				0.165	4	0.66
m-SATA SSD 32G										182				0.6006	1	0.6006
M.2 SSD 32G										182				0.6006	1	0.6006
eUSB											500			2.5	1	2.5
BCM5720												359		1.1847	1	1.1847
DDR4		2176	750											3.0612	2	6.1224
CPLD										0		500		1.65	1	1.65
LED												10		0.033	11	0.363
MISC.										100		100		0.66	1	0.66
BMC Module											100	800		3.14	1	3.14
BCM56870	400	3100		173600	20500					300				199.53	1	199.53
QSFP28										1520				5.016	32	160.512
SFP+										500				1.65	2	3.3
USB											1000			5	1	5
LED										6				0.0198	134	2.6532
FAN													1600	19.2	6	115.2
														0	0	0
														0	0	0
														0	0	0
														0	0	0
Sub Current(mA)	26400	10452	1500	173600	20500	11283	500	350	162	51895	1600	1869				569.01875
3.3V+10%							550									
Efficiency=90%																632.243056
Note:Maximum Current				221500	26400										FMA-HW01003-01 R01	

7. PSU

The system supports 4 kinds of power module.

- AC power (Air direction : Front to back; red color panel)
- AC power (Air direction : Back to front; blue color panel)
- DC Power (Air direction : Front to back; red color panel)
- DC input Power (Air direction : Front to back; blue color panel)

Those are for difference application; the fan direction is front to back or back to front, the AC/DC Power or DC/DC power.

The AC/DC and DC/DC power are only different between power input; the output voltage SPEC is the same. The AC/DC power is 90~240Vac input, and DC/DC power is 36~72Vdc input. The power supply can support load sharing function.

7.1. Pinout

The power module output pin define is as below.

3.3. Pin assianment for DC output gold fingers

PIN NO.	CONDITION	PIN NO.	CONDITION
TS1	PDB_FAULT	BS13	+12VS+
TS2	PRESENT	BS14	+12VRS-
TS3	A0	BS15	12LS
TS4	PDB_ALERT	BS16	SMB_ALERT
TS5	AC-OK	BS17	SDA
TS6	Reserved	BS18	SCL
TS7	Reserved	BS19	PS-KILL
TS8	Reserved	BS20	PS ON
TS9	Reserved	BS21	PW OK
TS10	A2	BS22	A1
TS11	+5VSB	BS23	+5VSB
TS12	+5VSB	BS24	+5VSB
TP1	GND	BP1	+12V
TP2	GND	BP2	+12V
TOP		BOTTOM	

Figure 3: signal descriptions

7.2. Dimension

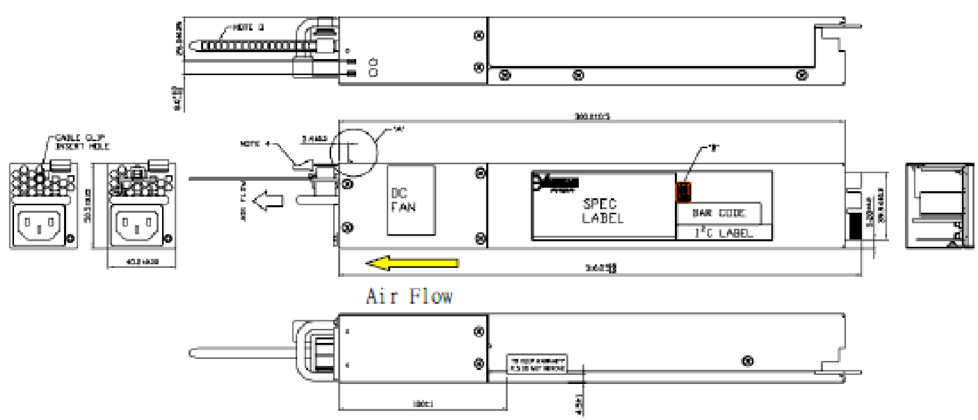
Nominal Dimensions

Height: 40.9mm (fits in 1U rack in vertical installation);

Width: 50mm

Depth: 310.2mm

3The casing dimension is W 50.5 mm x L 310.2 mm x H 40 mm(including gold finger)



3.

Figure 2: Outline drawing

3.

Figure 7-1 PSU Dimension

7.3. Efficiency

The Efficiency should meet at least 80Plus Platinum rating, specified in the below table. The efficiency test condition should be 230VAC and with external fan power source or deduction of the power consumed by the fan at specified loading, according to 80Plus efficiency measurement specifications.

(80Plus Platinum) test at 230VAC with external fan instead of self fan module.

Input	10% load	20% load	50%load	100%load
230VAC	*	90%	94%	91%
115VAC	*	*	*	*

7.4. Power Supply Management Controller (PSMC)

The PSMC device in the power supply shall derive its power of the +5V or +3.3V on the system side of the Oring device and shall be grounded to return. It shall be compatible with SMBus specification 2.0 and PMBusTM Power System Management Protocol Specification Part I and Part II in Revision 1.1 or later. It shall be located at the address set by the A0 and A1 pins. Refer to the specification posted on www.ssiforum.org and www.pmbus.org website for details of the power supply monitoring interface requirements and refer to followed section of supported features. The below table reflect the power module addresses complying with the position in the power system.

PDB position and PSMC address	PM1 B0h/B1h	PM2 B2h/B3h
Pin A1/A0	0/0	0/1

PSMC Addressing

7.5. Power Supply Field Replacement Unit (FRU)

The power supply shall support electronic access of FRU information over an I2C bus. Five pins at the power supply connector are allocated for this. They are named SCL, SDA, A1, A0 and Write protect. SCL is serial clock. SDA is serial data. These two bidirectional signals from the basic communication lines over the I2C bus. A0and A1 are input address lines to the power supply. The backplane defines the state of these lines such that the address to the power supply is unique within the system. The resulting I2C address shall be per table below. The Write protection pin is to ensure that data will not accidentally overwritten.

The device used for this shall be powered from a 3.3V bias voltage derived from the 5VSB output . No pull-up resistors shall be on SCL or SDA inside the power supply.

EEPROM Addressing

PDB position and FRU address	PM1 A0h/A1h	PM2 A2h/A3h
Pin A1/A0	0/0	0/1

7.6. PSMC Sensors

Sensors shall be available to the PSMC for monitoring purpose. All Sensors shall continue to provide real time data as long as the PSMC device is powered. This means in standby and operation mode, while in standby the main output(s) of the power supply shall read zero Amps and Volts.

Sensor	Description
Vinput	Input Voltage
Iinput	Input Current
Pinput	Input Power
Voutput_main	Output Voltage main output
Ioutput_main	Output Current main output
Poutput_main	Output Power main output
Voutput_aux	Output Voltage auxiliary output
Ioutput_aux	Output Current auxiliary output
Poutput_aux	Output Power auxiliary output
Tcomp(TBD)	Component Temperature
Tenv	Environmental Temperature
RPMFan	Fan Speed reading
PDBfail	PDB fail protection

PSMC Sensor list

7.7. LEDs of Power Supply units

The power supply has Green/ Red led to show the power supply status.

The LED TYPE: YCG317-EGW(R+G) or equal.

Power supply status	Power supply LED color
No AC power to all PSU	OFF
Only +5V standby output on (AC OK)	1Hz Blinking Green
Power supply DC output ON and OK	Green
Power supply fail	Red
Fan fail	1Hz Blinking Red
Power supply warning	0.5Hz Blinking Red/Green *

NOTE: * Blinking frequency: (Red and Green on 0.5 Sec and off 0.5 Sec separately and sequentially in two seconds)

Figure 7-2 LEDs of Power Supply units

8. PCB

There following PCB information included stack-up, dimension, and placement.

8.1. Stack-up

The Switch board PCB material is the ultra-low loss material for High speed signal. The PCB has 14 layers and power plane has 2oz for high current application.

Figure 8-1 Switch board PCB Stackup

Accton Tech 14 Layer Stack up Proposal

Customer Requirement			HCS Proposal (29/07/2014)													
										SE 50 ohms	DIFF 90ohms		DIFF 92ohms		DIFF 100ohms	
Layer #	A/W Code	Type	Estimated Thickness (um)	Cu Weight (oz)	Estimated Thickness (Mils)	Estimated Layer Cu Ratio (%)	Construction	Dk @ 1 GHz	Df @ 1 GHz	Line width (mils)	Line width (mils)	Air-gap (mils)	Line width (mils)	Air-gap (mils)	Line width (mils)	Air-gap (mils)
		Soldermask	25		1.0											
1	TOP	0.5oz Cu Foil+pl	48		1.9	20%				8.5	7.2	4.8	7.1	4.9	6.2	5.8
		Prepreg	106		4.2		2X 1035	3.09	0.0015							
2	GND	1.0 oz Cu	32	1.0	1.3	80%				REFERENCE LAYER						
	Core 1	CORE	130		5.1		2X 1078	3.27	0.0017							
3	S	0.5 oz Cu	16	0.5	0.6	20%				6.6	7.0	6.0	6.8	6.2	5.7	6.3
		Prepreg	159		6.3		2 X 1078	3.13	0.0017							
4	GND	1.0 oz Cu	32	1.0	1.3	80%				REFERENCE LAYER						
	Core 2	CORE	130		5.1		2X 1078	3.27	0.0017							
5	S	0.5 oz Cu	16	0.5	0.6	20%				6.6	7.0	6.0	6.8	6.2	5.7	6.3
		Prepreg	159		6.3		2 X 1078	3.13	0.0017							
6	GND	1.0 oz Cu	32	1.0	1.3	80%				REFERENCE LAYER						
	Core 3	CORE	130		5.1		1 x 2116	3.31	0.0017							
7	V	2.0 oz Cu	66	2.0	2.6	80%										
		Prepreg	210		8.3		2 x 2116	3.31	0.0018							
8	V	2.0 oz Cu	66	2.0	2.6	80%										
	Core 5	CORE	130		5.1		1 x 2116	3.31	0.0017							
9	GND	1.0 oz Cu	32	1.0	1.3	80%				REFERENCE LAYER						
		Prepreg	159		6.3		2 X 1078	3.13	0.0017							
10	S	0.5 oz Cu	16	0.5	0.6	20%				6.6	7.0	6.0	6.8	6.2	5.7	6.3
	Core 6	CORE	130		5.1		2X 1078	3.27	0.0017							
11	GND	1.0 oz Cu	32	1.0	1.3	80%				REFERENCE LAYER						
		Prepreg	159		6.3		2 X 1078	3.13	0.0017							
12	S	0.5 oz Cu	16	0.5	0.6	20%				6.6	7.0	6.0	6.8	6.2	5.7	6.3
	Core 7	CORE	130		5.1		2X 1078	3.27	0.0017							
13	GND	1.0 oz Cu	32	1.0	1.3	80%				REFERENCE LAYER						
		Prepreg	106		4.2		2X 1035	3.09	0.0015							
14	BOT	Cu Foil+plating	48		1.9	20%				8.5	7.2	4.8	7.1	4.9	6.2	5.8
		Soldermask	25		1.0											
Requested thickness			2.37	mm	93.4		mils (Soldermask to soldermask over copper)									

Note :
1. Material: **TUC TU-933**
2. Board Thickness Specification:
3. Board thickness and Impedance trace width are **estimated value** base on estimated layer Cu Ratio and subject to Fine Tune after scout run.
4. 14 Layer Stack up Proposal.
5. As at current, HCS has not obtain UL qualification for this material.

The CPU board PCB material is the low loss material for High speed signal. The PCB has 12 layers and power plane has 2oz for current application.

Figure 8-2 CPU board PCB Stackup

Layer Name	Plane Description	Remain Copper (%)	Material	reduce after pressed	finish Thickness	Er	Single-end		Single-end		Differential		Differential		Differential		Differential		Differential		Differential		Differential		Ref. Pin
							Impedance	Width	Impedance	Width	Impedance	Width/Space	Impedance	Width/Space	Impedance	Width/Space	Impedance	Width/Space	Impedance	Width/Space	Impedance	Width/Space	Impedance	Width/Space	
	solder mask				0.50																				
Layer 1	Signal		1/3oz HTE +Plating		1.45		40	7	50	4.5	68	8/6	80	6/7	63	9/5	83	5/5	85	5/5.5	90	5/8	100	4/7	L2
	PREPREG		1067		2.41	3.2																			
Layer 2	POW/GND	85	1/2oz HTE	0.09	0.60																				
	Core		0.0762		3.00	3.25																			
Layer 3	Signal	65	1/2oz HTE	0.21	0.60		40	6	50	4	68	8/8	80	5/4.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	L2&L4
	PREPREG		1078 + 1078HR		6.20	3.25																			
Layer 4	POW/GND	85	1/2oz HTE	0.09	0.60																				
	Core		0.0762		3.00	3.25																			
Layer 5	Signal	65	1/2oz HTE	0.21	0.60		40	6	50	4	68	8/8	80	5/4.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	L4&L6
	PREPREG		1078 + 1078HR		5.90	3.25																			
Layer 6	POW/GND	85	2oz HTE	0.39	2.60																				
	Core		0.2032		8.00	3.45																			
Layer 7	POW/GND	85	2oz HTE	0.39	2.60																				
	PREPREG		1078 + 1078HR		5.90	3.25																			
Layer 8	Signal	65	1/2oz HTE	0.21	0.60		40	6	50	4	68	8/8	80	5/4.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	L7&L9
	Core		0.0762		3.00	3.25																			
Layer 9	POW/GND	85	1/2oz HTE	0.09	0.60																				
	PREPREG		1078 + 1078HR		6.20	3.25																			
Layer 10	Signal	65	1/2oz HTE	0.21	0.60		40	6	50	4	68	8/8	80	5/4.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	L9&L11
	Core		0.0762		3.00	3.25																			
Layer 11	POW/GND	85	1/2oz HTE	0.09	0.60																				
	PREPREG		1067		2.41	3.2																			
Layer 12	Signal		1/3oz HTE +Plating		1.45		40	7	50	4.5	68	8/6	80	6/7	63	9/5	83	5/5	85	5/5.5	90	5/8	100	4/7	L11
	solder mask				0.50																				
Total Thickness=	1.60			1.98	62.92																				

The Fan PCB is a 4 layer PCB

8.2. Dimension

The Switch PCB dimension is 383 x 258.5 mm.

Figure 8-3 Switch board PCB Dimension

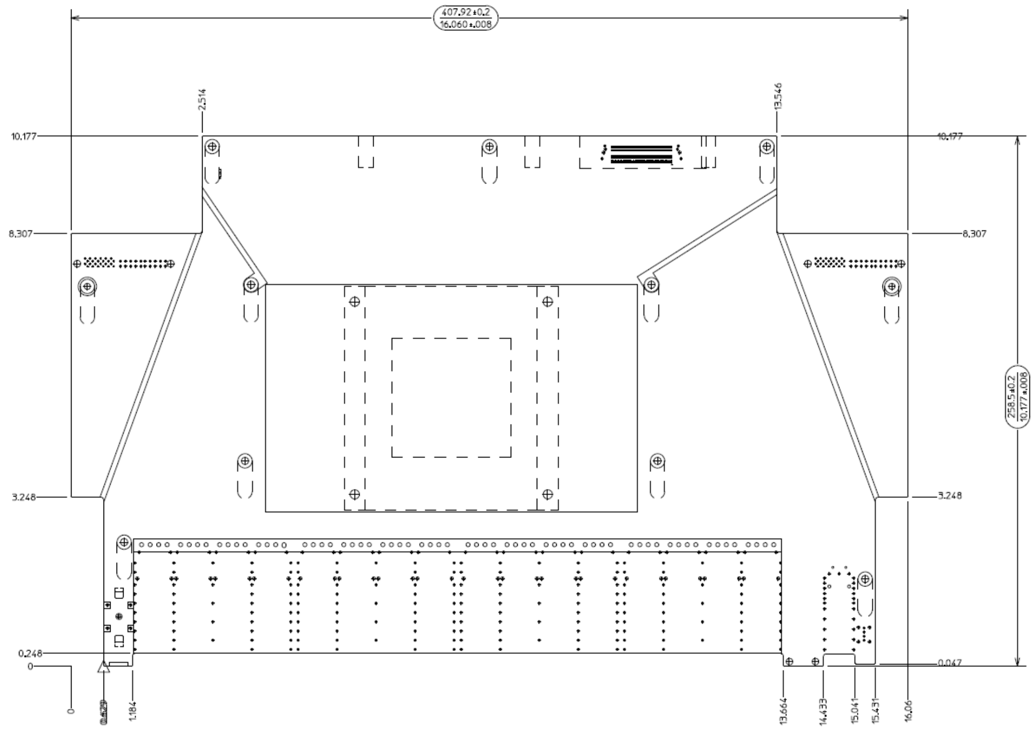
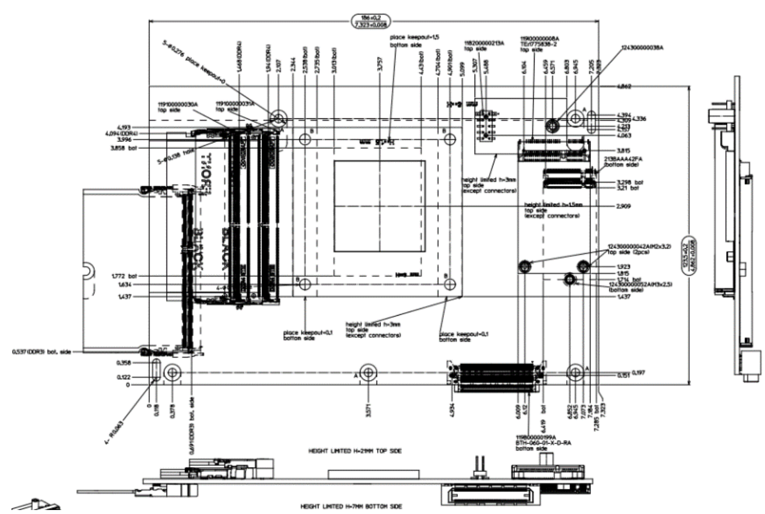
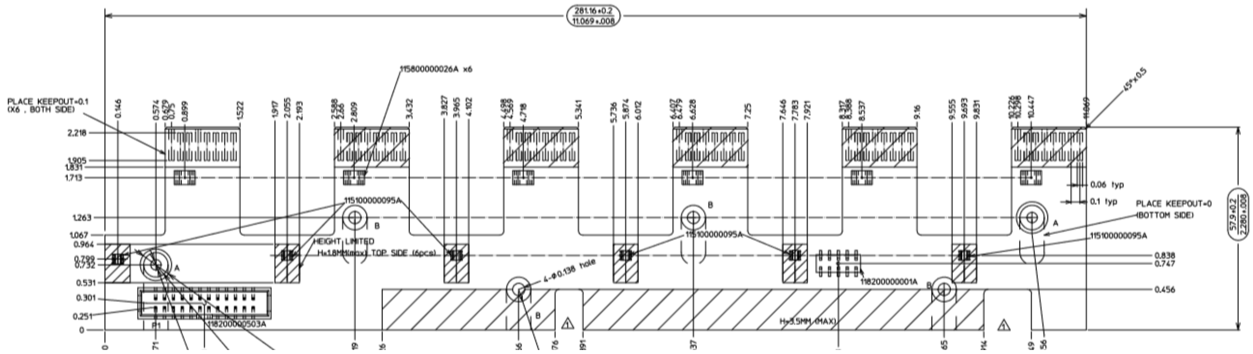


Figure 8-4 CPU board PCB Dimension



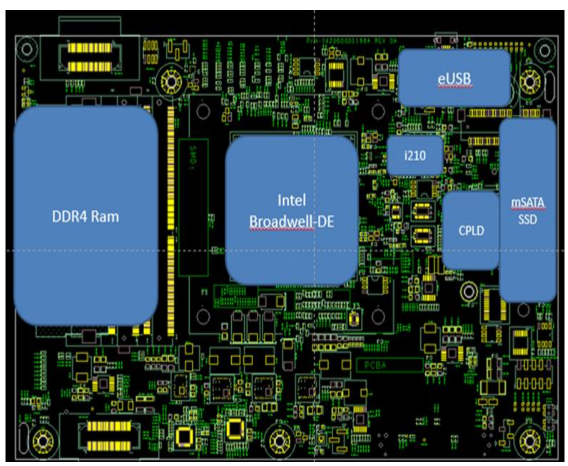
Fan PCB Dimensions

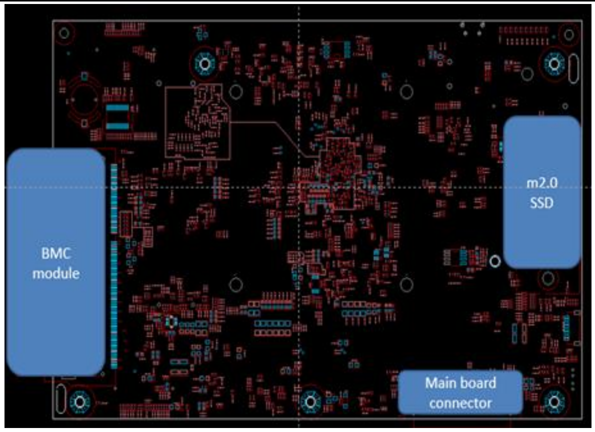


8.3. Placement

Figure 8-5 CPU board - PCB Placement

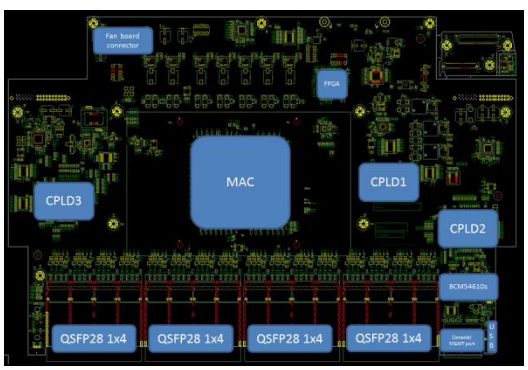
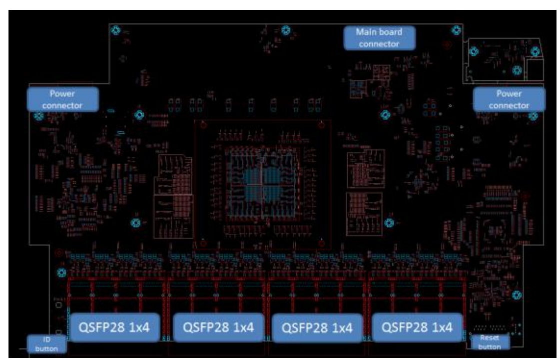
Top





Bottom

Figure 8-6 Switch board - PCB Placement

Top	Bottom
	

9. Mechanical

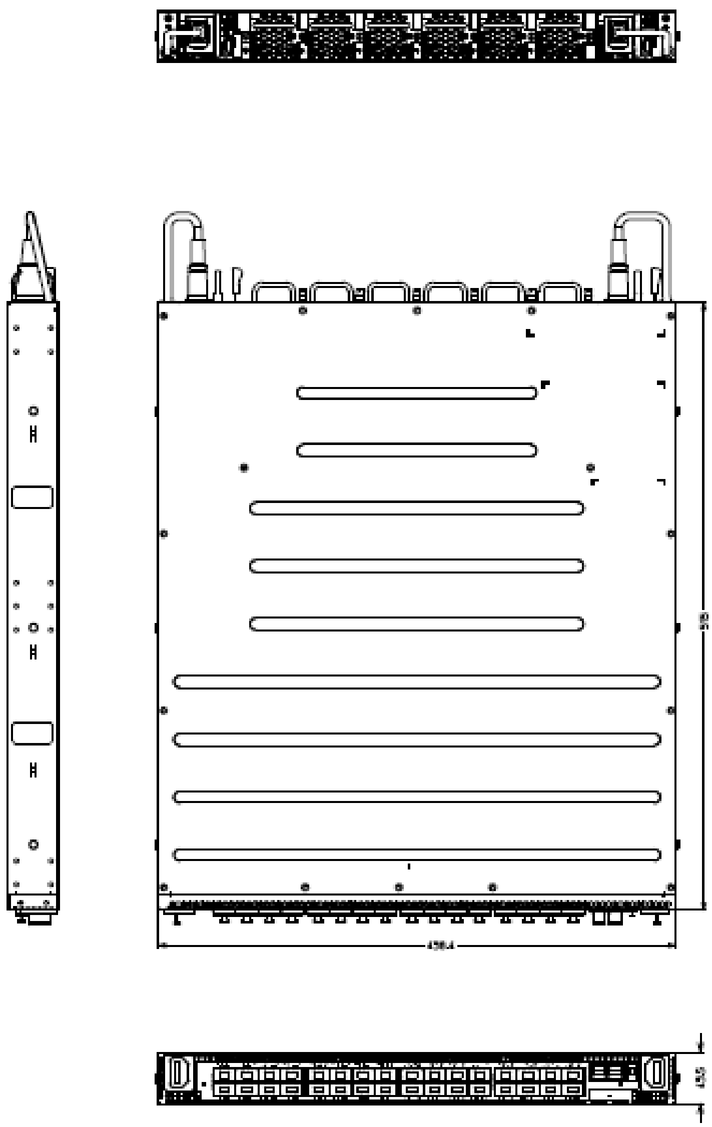
9.1. Dimension

Height: 43.5mm(maximum)

Width: 438.4mm

Depth: 515mm

Figure 9-1 Mechanical Dimension



9.2. Placement

Figure 9-2 Mechanical Placement (Top)

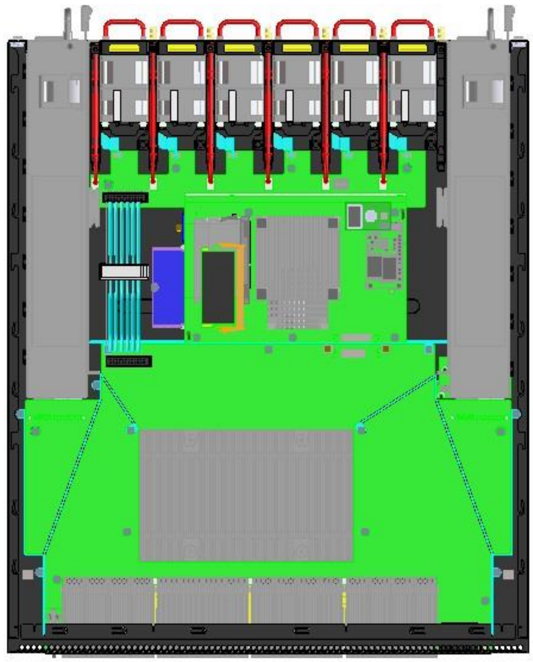


Figure 9-3 Mechanical Placement (Front)

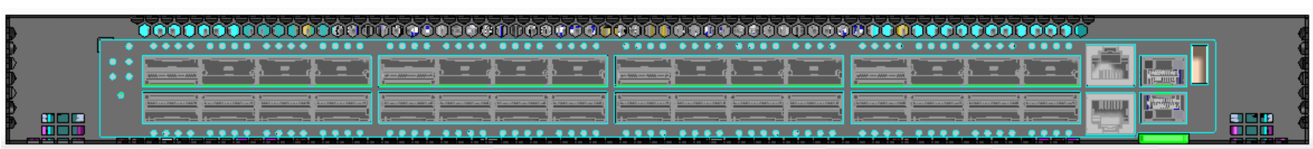
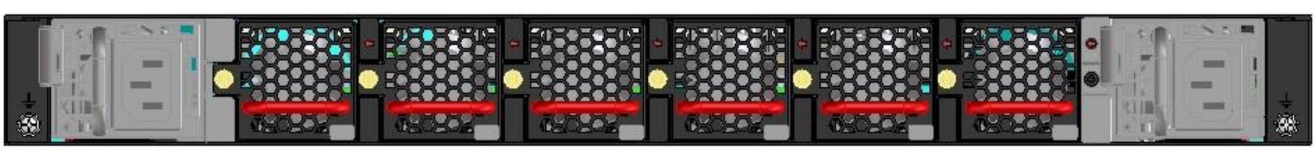


Figure 9-4 Mechanical Placement (Rear)



9.3. Cooling Method

9.3.1. Fan module

AS7726-32XBT system supports two kinds Fan module.

- Front to back Fan module with red color handle
- Back to Front Fan module with blue color handle
-

Figure 9-5 Back to front fan module

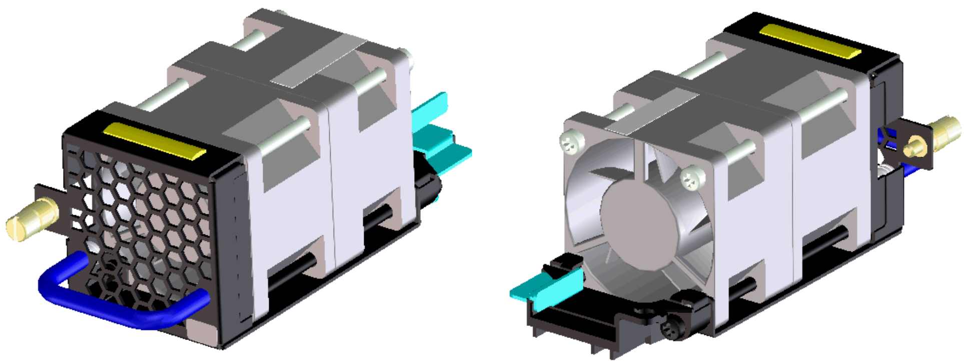


Figure 9-6 Front to Back fan module

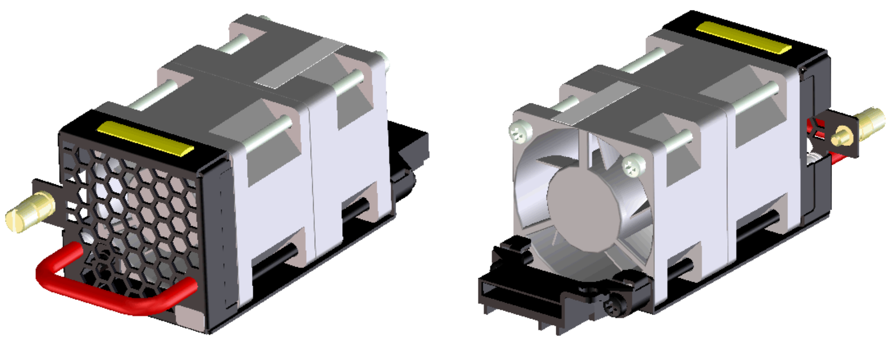


Figure 9-7 Fan Speed information

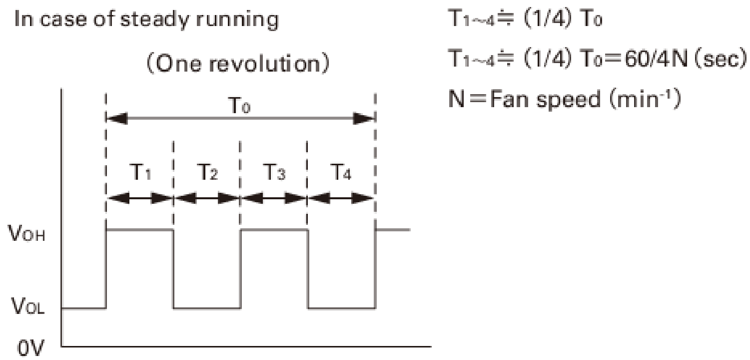
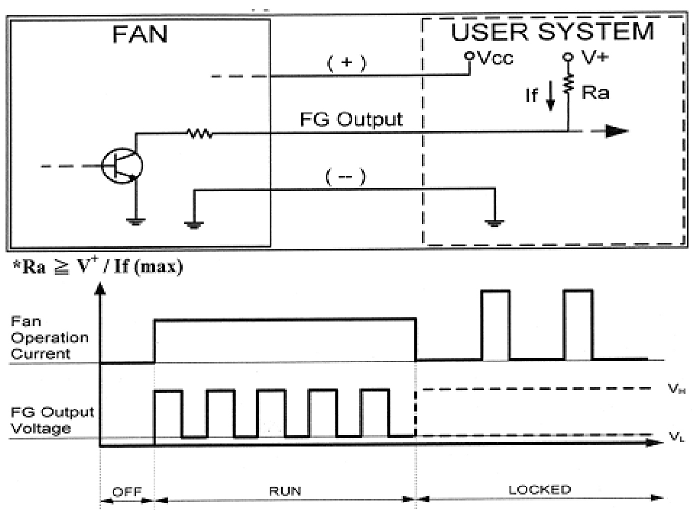


Figure 9-8 Fan failed information

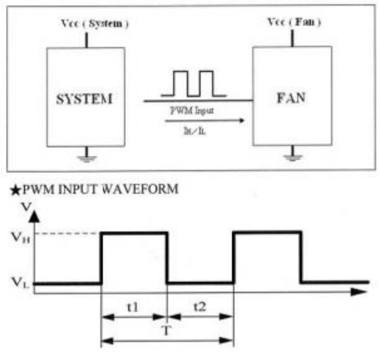


★Electrical Characteristics ：(at Ta = 25℃, V_{CC}=12V)

Parameter	Ratings			Unit
	min	typ.	max	
FG Supply Voltage(V+)	3	--	13.2	Voltage
FG Output Current (If)	--	--	5	mA
FG Output (VL)	0	--	0.5	Voltage
FG Output (VH)	--	V+	--	Voltage

Figure 9-9 Fan PWM

PWM INPUT SIGNAL



1. Period : $T = \frac{1}{f_{PWM}} = t1 + t2(sec)$

2. Duty Cycle (D.C.) $\frac{t1}{t1+t2} * 100 = \frac{t1}{T} * 100(\%)$.

3.PWM Duty Cycle VS Speed (at Ta = 25℃ Vcc =12VDC)

PWM Duty Cycle (%)	IN FAN Speed (R.P.M.) (REF.)	OUT FAN Speed (R.P.M.) (REF.)
100	21500	18000
60	13800	12150

★ Electrical Characteristics at Ta = 25℃ : Vcc=12V

Parameter	Min	Typical	Max	Unit
f pwm	22K	25K	28K	Hz
V_H	2.8	--	5.5	V
V_L	0	--	0.8	V
I_H	--	--	1	mA
I_L	--	--	-1	mA
D.C.	0	—	100	%

* The speed is default to be maximum if PWM input pin is unconnected.

The system only can provide 3.3V PWM signal. The min of Vh of fan need be low than 3.3V.

10. Specifications and Standards

10.1. Safety

- UL (CAN/CSA 22.2 No 60950-1 & UL60950-1)
- CB (IEC/EN60950-1)
- CCC (GB4943.1-2011)
- BSMI (CNS14336-1)

10.2. Electromagnetic Compatibility

- CE Mark
  - EN55032 Class A
  - EN55024 (Immunity) for Information Technology Equipment
  - EN 61000-3-3
  - E N 61000-3-2
- FCC Title 47, Part 15, Subpart B Class A
- VCCI Class A
- CNS 13438 (BSMI) → by Request
- CCC (GB9254-2008) → by Request

10.3. Environmental

- Low-Temperature Exposure and Thermal Shock (packaged) : NEBS GR63-CORE ISSUE 4 , Section 4.1.1.1
- High Relative Humidity Exposure (Packaged) : NEBS GR63-CORE ISSUE 4 , Section 4.1.1.2
- High-Temperature Exposure and Thermal Shock (Packaged) : NEBS GR63-CORE ISSUE 4 , Section 4.1.1.3
- Operating Temperature and Relative Humidity : NEBS GR63-CORE ISSUE 4 , Section 4.1.2
- Altitude : NEBS GR63-CORE ISSUE 4 , Section 4.1.3
- Handling Drop Tests -Packaged Equipment : NEBS GR63-CORE ISSUE 4 , Section 4.3.1.1
- Unpackaged Equipment -Drop Tests (All Equipment) : NEBS GR63-CORE ISSUE 4 , Section 4.3.2
- Earthquake (10U Rack) : NEBS GR63-CORE ISSUE 4 , Section 4.4.1 (Zone4)
- Office Vibration Test Procedure; 90 minutes/axis (Stand & 42U Rack) : NEBS GR63-CORE ISSUE 4 , section 4.4.4
- Transportation Vibration-Packaged Equipment : NEBS GR63-CORE ISSUE 4 , section 4.4.5
- Acoustic noise : NEBS GR63-CORE ISSUE 4 , section 4.6
- Bump : IEC60068-2-29- packaged
- Shock : ETSI EN 300 019-2-3 -Operational Tests, Class T3.2 op

10.4. ROHS (6/6) Requirement

Restriction of Hazardous Substances (6/6):

Compliance with Environmental procedure 020499-00, primarily focused on Restriction of Hazardous Substances (ROHS Directive 2002/95/EC) and Waste Electrical and Electronic Equipment (WEEE Directive 2002/96/EC).

10.5. WEEE Standards

The switches complied with the following WEEE standards:
Waste Electrical and Electronic Equipment (WEEE Directive 2002/96/EC)

10.6. IEEE Standards

- IEEE 802.3ba 40G/25GBASE
- IEEE 802.3bm next generation 40G/25G Optical Ethernet
- IEEE P802.bj 100 Gb/s & FEC support

10.7. Internet Standards

- SFF-8431 SFP+ 10 Gb/s and Low Speed Electrical Interface
- SFF-8436 QSFP+ 10 Gb/s 4X Pluggable Transceiver
- SFF-8635 QSFP+ 10 Gb/s 4X Pluggable Transceiver Solution
- SFF-8665 QSFP+ 28 Gb/s 4X Pluggable Transceiver Solution