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Barreleye G1 Specification

Chassis, Motherboard, IO Board, Lunchbox Power Supply

Revision 1.0.1

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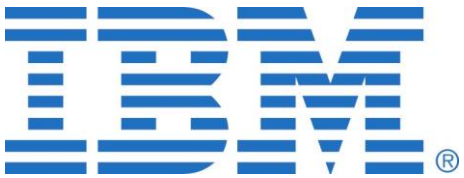


3 Revision History

Revision	Date	Name	Description
0.1	04/28/2015		Preliminary Release
0.2	05/12/2015		Update POWER8 DIMM Support
0.3	07/18/2015		1. Update Sled Block Diagram 2. Update PCB information
0.4	08/20/2015		1. Add PEB and BP placement 2. Update Chapter 9 Mechanical
0.5	08/25/2015		Add 9.9 Rack and 9.10 Rack Knife section
0.6	08/25/2015		Edits for grammar and flow
0.7	08/28/2015		1. Add MB and IO stack-up 2. Add board to board connector section 3. Add Lunch Box Chapter
0.7.1	09/08/2015		Additional edits for grammar and flow
0.7.2	09/18/2015		Additional edits for grammar and flow
0.8	11/23/2015		1. Add 9.9 HDD tray dimension 2. Correct the number of CPU pin to 2296 pins 3. Update mSATA to M.2 SATA due to design change 4. Update APSS function description 5. Correct the location of fan connectors which are all on MB 6. BMC firmware update methoed 7. Add connector pin define

			8. Update Lunch Box picture 9. Remove original section, 7.3.2 and 7.4.2 for VR optimiztions, since VR doesn't support auto-phase dropping for light loading
0.8.1	01/22/2016		1. 8.9.2, Add Beep LED behavior 2. Remove 8.11 TPM connector 3. Update ME drawing to PVT version
0.8.2	01/25/2015		Numerous Edits: 1. Added IBM / OpenPOWER notice page 2. Added recognition & logos page 3. Added OCP-HL-P license information 4. Updated authors information
0.9	05/04/2016		1. 1. Update BMC chapter 2. 2. 8.9.2, Update Power/ID, Beep and M.2 SATA LED behavior 3. 3. 8.10.2, Update Fan LED behavior 4. 4. Add DIMM population Rule in 3.5.4
1.0	08/05/2016		1. Edits for grammar and flow 2. Added various BMC-based firmware update methods. 3. Added host-based CPLD firmware update methods.
1.0.1	10/23/2016		Change in attribution for Poly Yeh

Table of Contents

4 Scope

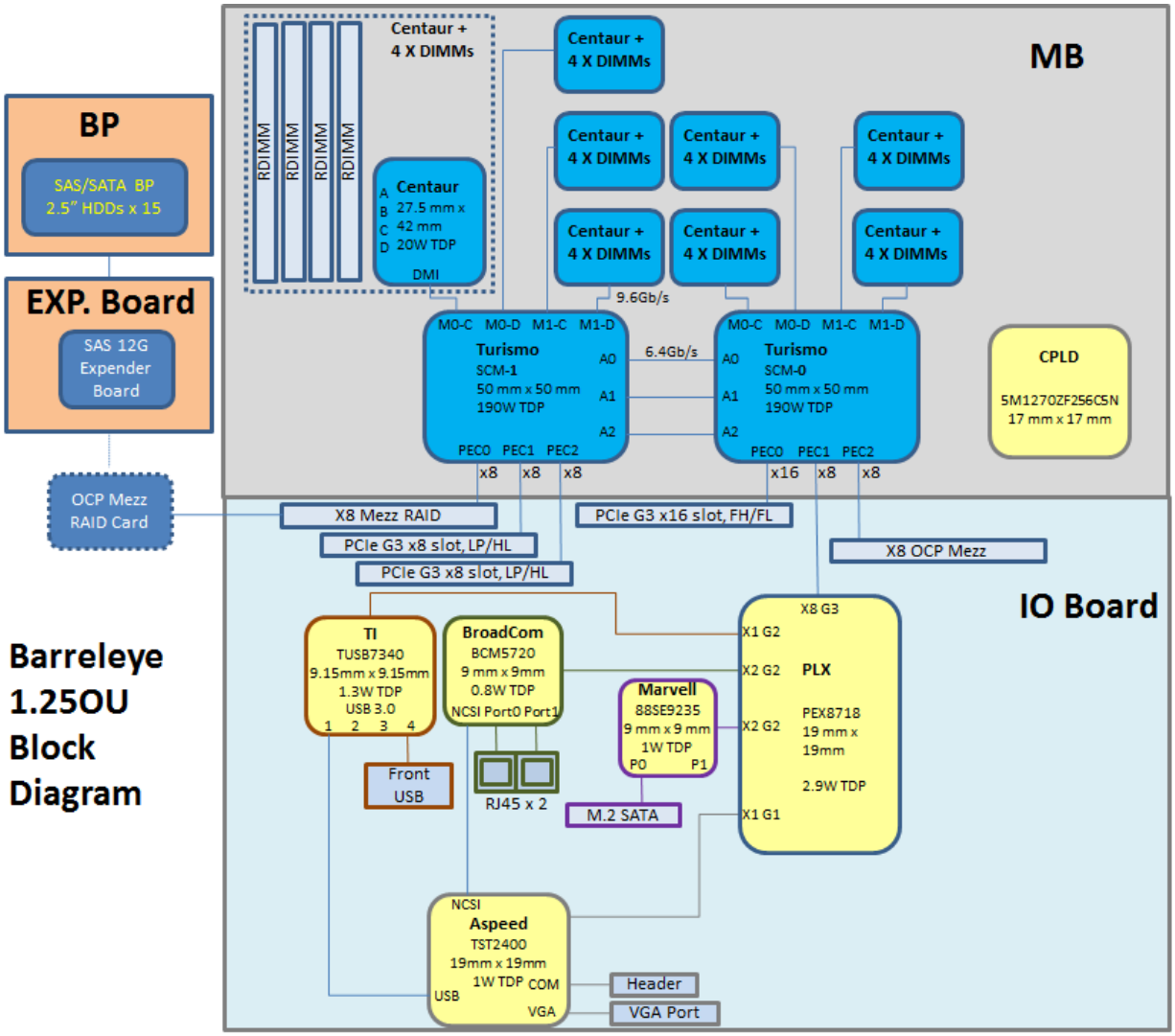
This document describes the specification of Barreleye, an OpenPOWER-based Open Compute server, with a mechanical & electrical package designed for Open Rack.

The hardware engineering specification provides technical details for the server board's functional architecture and feature set, and some mechanical design details.

5 System Block Diagram

The Barreleye platform consists of IBM POWER8 "Turismo" SCM (Single Chip Module) Processor with IBM "Centaur" Memory Buffers, with PCI-E Gen 3 integrated on chip. Additional details follow.

- IBM POWER8 "Turismo" SCM Processors connects directly to Memory Buffers through a DMI interface operating at 9.6 GTs x 3B.
    - Each processor is directly connected to four buffers, with 8 total buffers on board.
    - Each buffer connects to 4 DIMM slots
    - Each buffer also functions as a 16MiB L4 cache (128 MiB of cache, total)
    - Each buffer provides an additional 9.6 GTs x 3B of memory bandwidth, to the system
    - In this configuration, maximum bandwidth to DRAM is 115.2 GiBps, per socket, and 230.4 GiBps per system.
- The communication between each CPU is A-Bus, operating at 6.4 GTs x 2B.
    - There are three A-Bus links between the CPUs, providing a total bandwidth of 38.4 GiBps
- POWER8 "Turismo" includes an integrated PCI Gen 3 interface, with a total of 56 lanes spread between processors.



Barreleye 1.25OU Block Diagram

6 Product Features

6.1 Feature List

Project name	Barreleye
Chassis Size	1.25OU
CPU	IBM POWER8 "Turismo" SCM Processor x 2, 2296 pins Socket (support up to 12-core, 190W CPU)
Memory Buffer	IBM Centaur, 4 Memory buffers per Processor, total 8 memory buffer
Memory	4 DDR3 Memory channels per memory buffer; total 32 DDR3 RDIMMs,1333 MHz(1DPC), 8/16/32GB
Storage	15x 12Gb/s SAS or 6Gb/s SATA 2.5" drive slots, up to 15mm thickness, connected via SEB, to an onboard HBA. One M.2 SATA slot, also on board.
Graphic	Integrated in iBMC (ASPEED AST2400) chip
Onboard Network	BroadCom BCM5720, GbE Controller, dual ports
PCIE Bridge	PLX PEX 8718
USB Controller	TI TUSB 7340, support USB 3.0
SATA Controller	Marvell 88SE9235, support for M.2 SATA

Front I/O	VGA, 2x RJ45 connector, 1x USB3.0(Front side), Power/Reset button, Power/ID LED, M.2 SATA HDD LED, BEEP LED
Management	iBMC ASPEED AST2400 with a share NIC 1GbE LAN port(BroadCom BCM5720)
PCI-e Slot	1 x 16 Gen3 FH/FL, 2 x8 Gen3 LP/HL, 1 x8 OCP Mez with front Panel access, 1 x8 PCIe OCP Mez in a non-front-accessible internal slot to support SAS HBA or Raid-on-Chip with SuperCap.
Board Size	MB : 600mm x380mm(20-Layer); I/O Board : 367.5mm x 161.74mm(14-Layer); BPx15 : 485.5mmx50mm(14-Layer); Power Expander Board : 130mmx120mm(10-Layer); PCIEx16 Riser : 137.9mm x 40.3 mm(4-Layer); PCIEx8 Right Riser: 98.09mm x 44.10mm(6-Layer); PCIEx8 Left Riser : 97.65 x 44.0 mm(4-Layer); Mez RAID Card : 110.5 mm x 68mm(10-Layer) RMC : 358.3 mm x 76 mm (6-Layer)

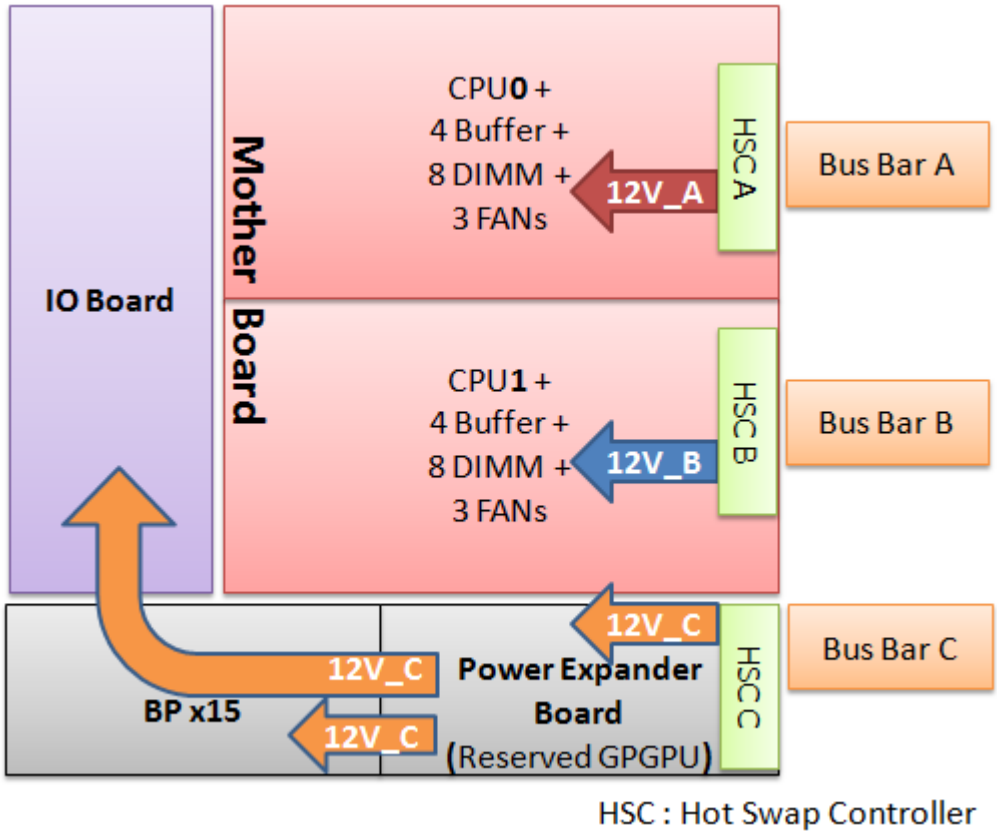
6.2 Power Distribution from Each Bus Bar

Bus Bar A : Max. 522.36W, Typical 464.62W, Usage Power 394.73W

Bus Bar B : Max. 522.36W, Typical 464.62W, Usage Power 394.73W

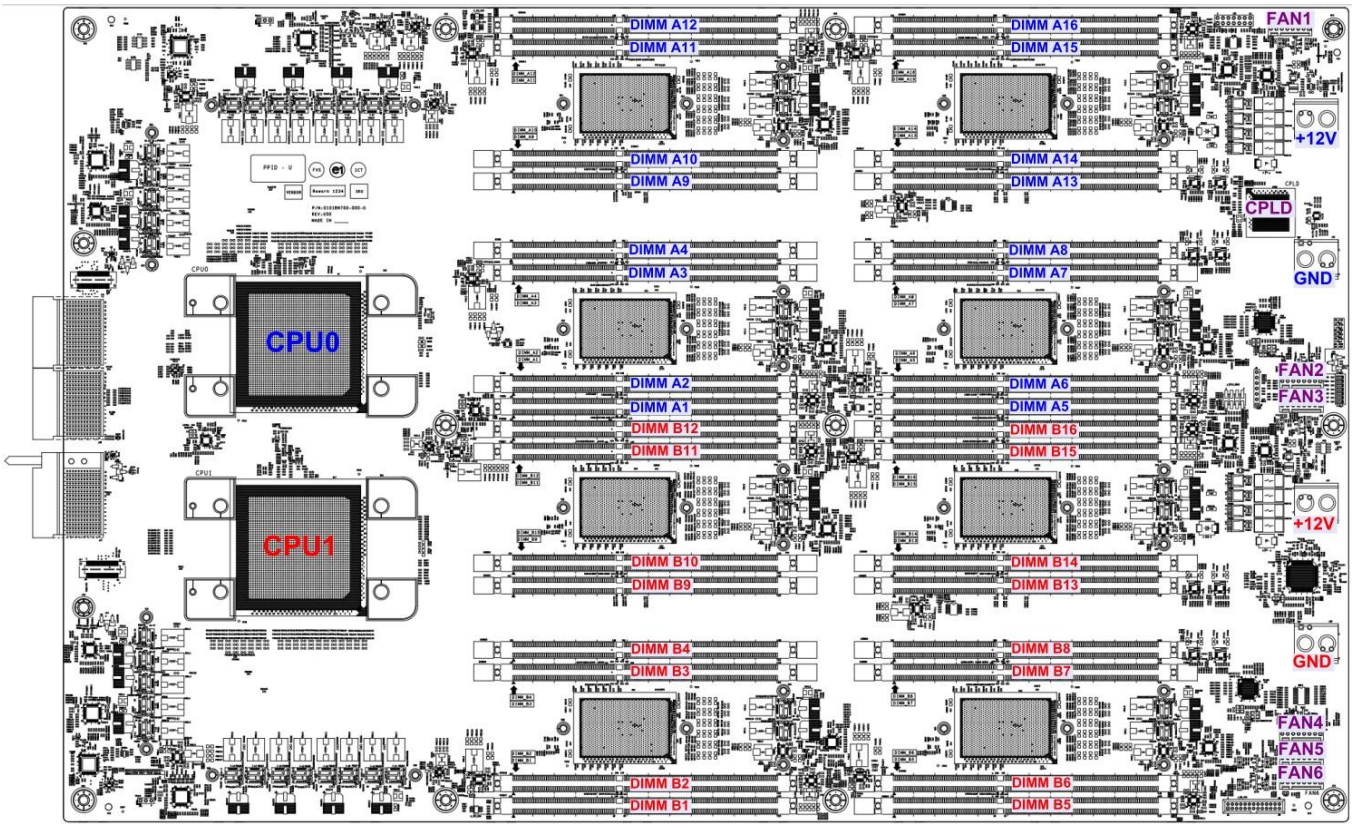
Bus Bar C : Max. 516.07W, Typical 490.22W, Usage Power 336.52W

Total usage power : ~1.2KW, attachment is power budget.

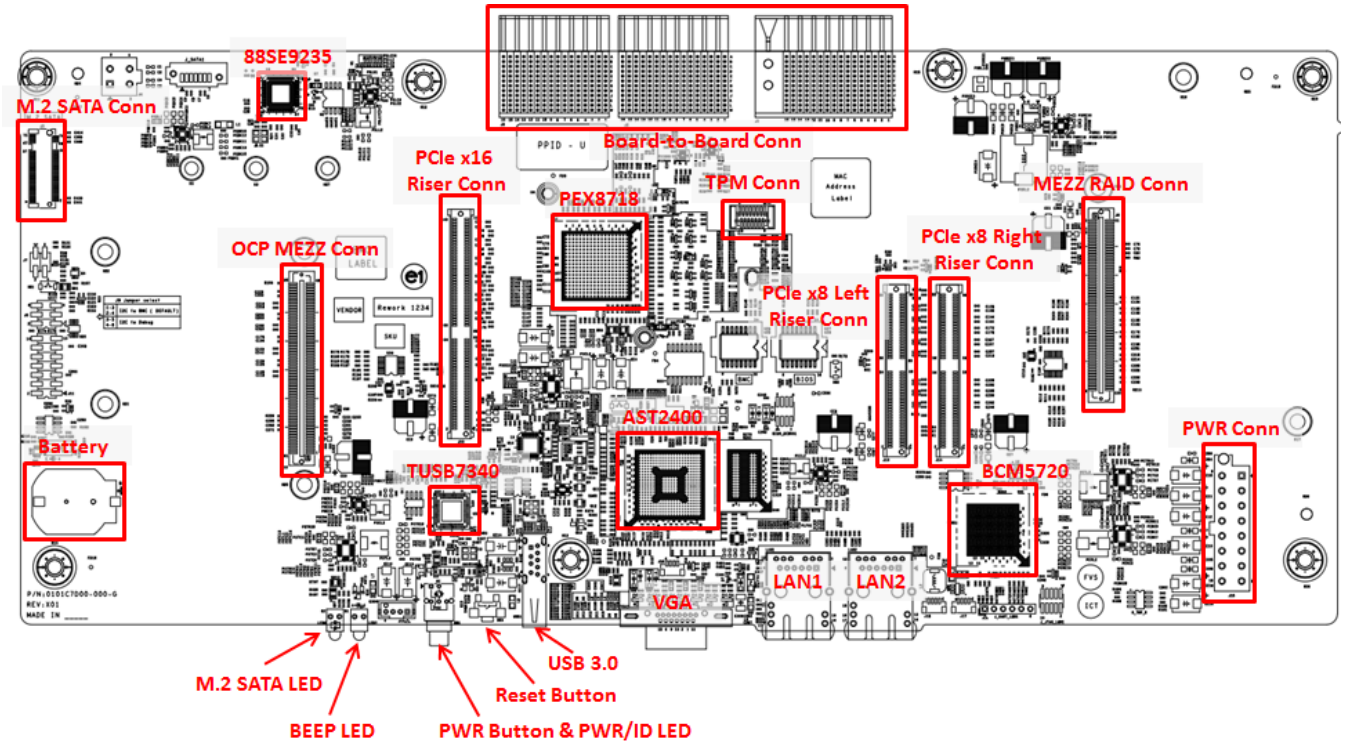


HSC : Hot Swap Controller

6.3 MB Placement



6.4 I/O Board Placement



6.5 Processor and Memory

6.5.1 Processor Feature Set

IBM POWER8 "Turismo" SCM Processor x 2, 2296 pins Socket, support up to 12-core, 190W CPU.

6.5.2 Memory Buffer

IBM Centaur, 4 Memory buffers per Processor, total 8 memory buffer connect to CPU0/1 through DMI interface.

6.5.3 Memory Support

The OpenPOWER memory subsystem supports IS RDIMM DDR3 memory of sizes 4 GB, 8 GB, 16 GB, and 32 GB. All memory configurations run at 1333 Mbps with the exception of the 4-rank dual-drop configuration which runs at 1066 Mbps. Below table shows the configuration of the supported DIMMs.

POWER8 DIMM Support

Raw Card	DRAM Type	DIMM Configuration	DIMM Type	4 Gb DRAM Density		
				DIMM Capacity	DRAM V_{DD}	DRAM Speed (MHz)
A	DDR3	1Rx8	RDIMM	4 GB	1.35	1333
C		1Rx4		8 GB		1333
B		2Rx8		8 GB		1333
E		2Rx4		16 GB		1333
F, AB		4Rx4		32 GB		1333 (single drop), 1066 (dual drop)

6.5.4 DIMM Population Rule

The following rules for attaching memory to the memory buffer ports must be followed at all times:

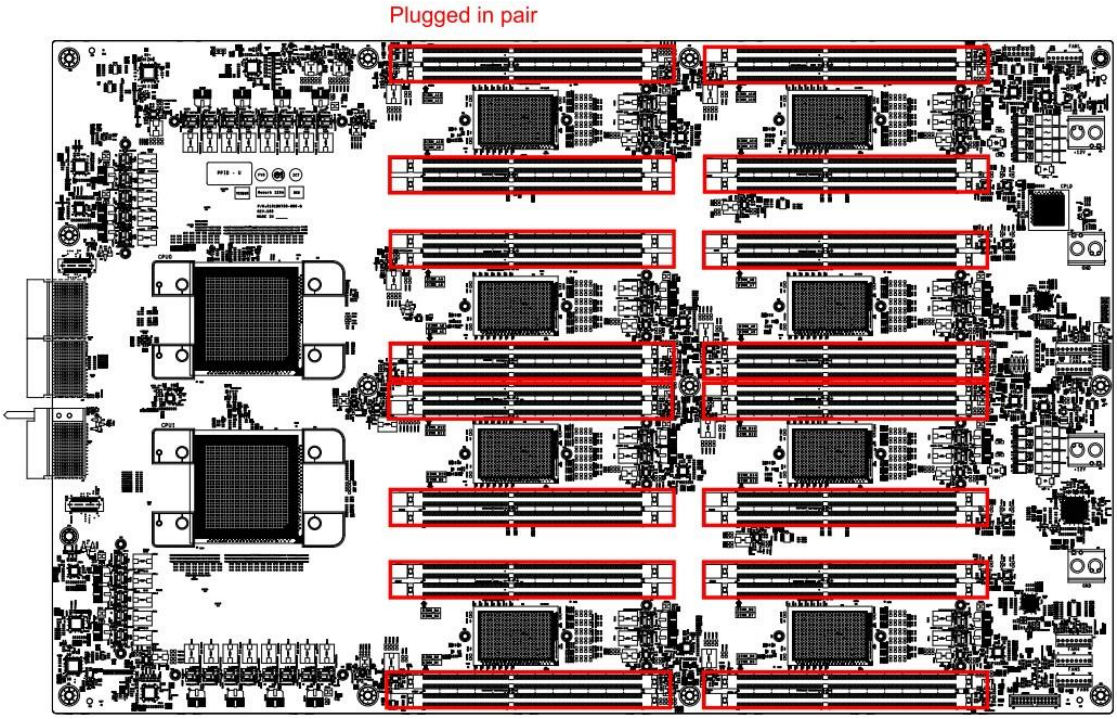
1. All memory attached to a port pair must be of the same speed, type, size, and technology.
2. Port pairs can contain different sizes and types of the same SDRAM generation. For example, port A/B (0/1) can attach to 2 GB industry standard (IS) DIMMs while port C/D (2/3) is attached to 4 GB IS DIMMs.
3. All memory across all the ports must operate at the same frequency.

In summary, the minimum requirement for IPL is at least one port pair behind a memory buffer in the system has 2 DIMMs (the 2 DIMMs must be the same), because Power8 supports only 2 DIMMs behind a port pair to IPL.

Barreleye enables a memory interleave feature by default. Unless this setting is changed in firmware, the default minimum requirement for IPL is 4 DIMMs because the paired port pair needs at least 2 DIMMs in each. The following table shows the DIMM label of paired port pair.

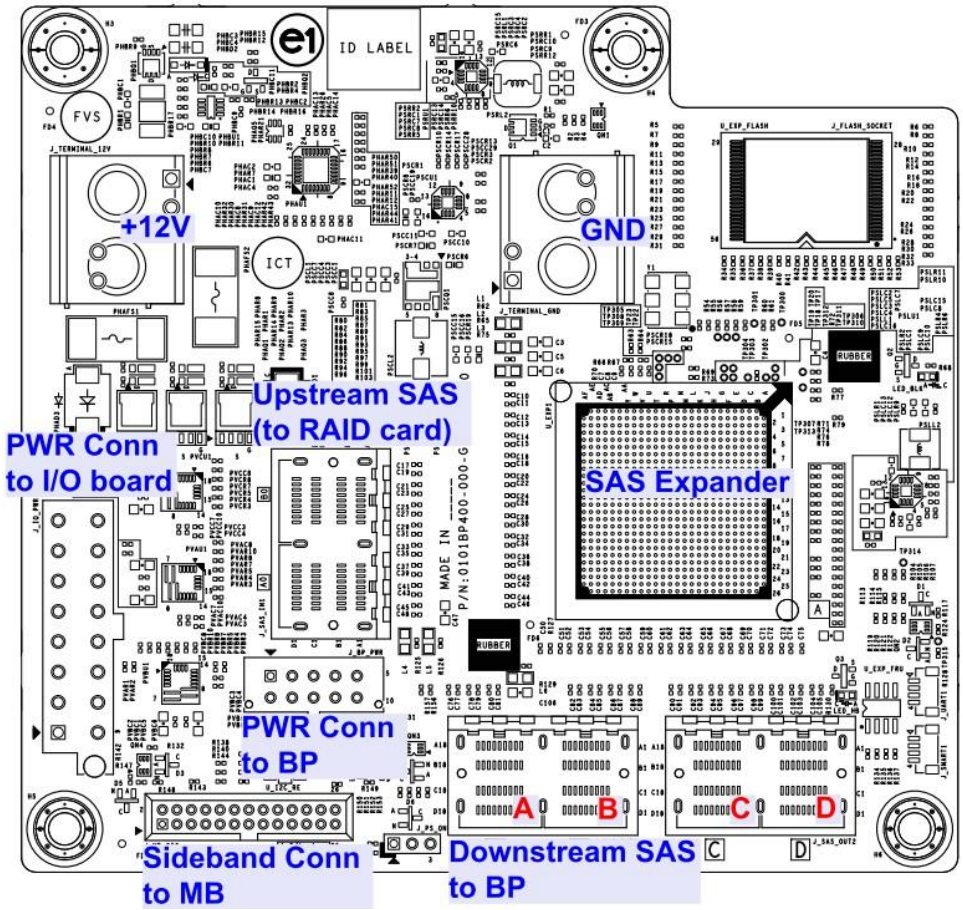
DIMM Population Rule

	DIMM Labels
Paired 1	A1, A2, A5, A6
Paired 2	A3, A4, A7, A8
Paired 3	A9, A10, A13, A14
Paired 4	A11, A12, A15, A16
Paired 5	B1, B2, B5, B6
Paired 6	B3, B4, B7, B8
Paired 7	B9, B10, B13, B14
Paired 8	B11, B12, B15, B16

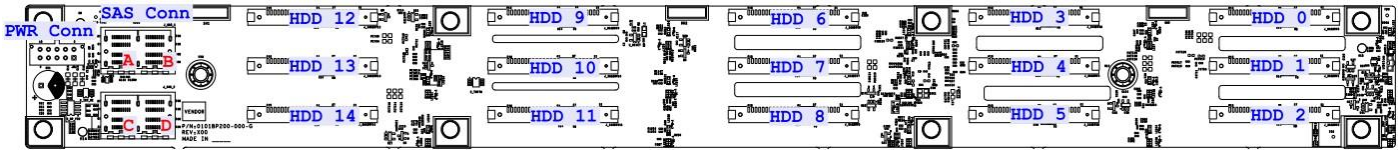


6.6 Storage

6.6.1 Power Expander board Placement



6.6.2 BPX15 Placement

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6.7 Printed Circuit Board Information

Each PCB material and stack-up are defined in the figure below.

Board	PCB Material	PCBA Dimension (L*W*H)（mm)
MB	IT-150DA (VLP + RTF copper)	600*380*2.65
IO Board	TU-862HF (RTF copper)	367.5*161.73*2.65
BPX15	IT-150DA (VLP + RTF copper)	485.5*50 *2.82
Power Expander Board	TU-862HF (RTF + HTE copper)	120 *130*2.37
Power Fixture Board	Standard FR4 (HTE copper)	208.45*94*1.59
PCIEx16 Riser	TU-862HF (RTF copper)	137.9*40.3*1.58
PCIEx8 Right Riser	TU-862HF (RTF copper)	98.09*44.109*1.58
PCIEx8 Left Riser	TU-862HF (RTF copper)	97.65*44.0*1.58
Mez RAID	Standard FR4	110.05*68*1.57
RMC board	Standard FR4 (HTE copper)	358.3*76

6.6.1 MB 20-Layer Stack-up

20-Layer Board Stack-Up (2.91 mm)

Layer Name	Layer Description	Material	DK	Layer Thickness (mil)	Copper Weight (oz)
	SOLDER MASK	Solder Mask	3.80	0.50	
Signal1	SIGNAL	Copper		1.90	0.5 + 1 (plating)
	PREPREG	FR4	3.50	2.59	
PPlane2	GND	Copper		1.20	1.0
	CORE	FR4	3.50	4.00	
Signal3	SIGNAL	Copper		1.20	1.0
	PREPREG	FR4	3.50	3.85	
PPlane4	GND/PWR	Copper		1.20	1.0
	CORE	FR4	3.50	4.00	
Signal5	SIGNAL	Copper		1.20	1.0
	PREPREG	FR4	3.50	3.85	
PPlane6	GND/PWR	Copper		1.30	1.0
	CORE	FR4	3.50	10.50	
Signal7	SIGNAL	Copper		1.20	1.0
	PREPREG	FR4	3.50	3.50	
PPlane8	GND/PWR	Copper		1.20	1.0
	CORE	FR4	3.50	4.00	
PPlane9	GND/PWR	Copper		2.40	2.0
	PREPREG	FR4	3.50	4.00	
PPlane10	GND/PWR	Copper		2.40	2.0
	CORE	FR4	3.50	4.00	
PPlane11	GND/PWR	Copper		2.40	2.0
	PREPREG	FR4	3.50	4.00	
PPlane12	GND/PWR	Copper		2.40	2.0
	CORE	FR4	3.50	4.00	
PPlane13	GND/PWR	Copper		1.20	1.0
	PREPREG	FR4	3.50	3.50	
Signal14	SIGNAL	Copper		1.20	1.0
	CORE	FR4	3.50	10.50	
PPlane15	GND/PWR	Copper		1.30	1.0
	PREPREG	FR4	3.50	3.85	
Signal16	SIGNAL	Copper		1.20	1.0
	CORE	FR4	3.50	4.00	
PPlane17	GND/PWR	Copper		1.20	1.0
	PREPREG	FR4	3.50	3.85	
Signal18	SIGNAL	Copper		1.20	1.0
	CORE	FR4	3.50	4.00	
PPlane19	GND	Copper		1.20	1.0
	PREPREG	FR4	3.50	2.59	
Signal20	SIGNAL	Copper		1.90	0.5 + 1 (plating)
	SOLDER MASK	Solder Mask	3.80	0.50	
Overall Board Thickness w/SM				**115.98**	**mils Tol: +/-10%**

6.6.2 IO 14-layer Stack-up

14-Layer Board Stack-Up

Layer Name	Layer Description	Material	DK	Layer Thickness (mil)	Copper Weight (oz)
	SOLDER MASK	Solder Mask	3.80	0.50	
Signal1	SIGNAL	Copper		1.90	0.5 + 1 (plating)
	PREPREG	FR4	3.70	4.00	
GPlane2	GND	Copper		1.20	1.0
	CORE	FR4	3.70	4.00	
Signal3	SIGNAL	Copper		1.20	1.0
	PREPREG	FR4	3.70	11.56	
GPlane4	GND	Copper		1.20	1.0
	CORE	FR4	3.70	4.00	
Signal5	SIGNAL	Copper		1.20	1.0
	PREPREG	FR4	3.70	11.56	
GPlane6	GND	Copper		1.20	1.0
	CORE (2-ply)	FR4	3.70	4.00	
PPlane7	GND/PWR	Copper		2.40	2.0
	PREPREG (2-ply)	FR4	3.70	16.14	
PPlane8	GND/PWR	Copper		2.40	2.0
	CORE (2-ply)	FR4	3.70	4.00	
GPlane9	GND	Copper		1.20	1.0
	PREPREG	FR4	3.70	11.56	
Signal10	SIGNAL	Copper		1.20	1.0
	CORE	FR4	3.70	4.00	
GPlane11	GND	Copper		1.20	1.0
	PREPREG	FR4	3.70	11.56	
Signal12	SIGNAL	Copper		1.20	1.0
	CORE	FR4	3.70	4.00	
GPlane13	GND	Copper		1.20	1.0
	PREPREG	FR4	3.70	4.00	
Signal14	SIGNAL	Copper		1.90	0.5 + 1 (plating)
	SOLDER MASK	Solder Mask	3.80	0.50	
Overall Board Thickness w/SM				**115.98**	**mils Tol: +/-10%**

7 System Firmware (System BIOS) & CPLD

Barreleye uses OpenPOWER's open source system firmware, made available under open source licensing schemes, available at https://github.com/open-power.

Barreleye machine configuration data files are available here: https://github.com/open-power/barreleye-xml

Barreleye also includes a Complex Programmable Logic Device, to control power up/down/reset sequencing. Firmware for the CPLD is included in Barreleye design collateral available at on opencompute.org.

BIOS update methods are available with documentation on https://github/open-power.

CPLD update methods are available below.

7.1 Update Complex Programmable Logic Device (CPLD)

1. Download and extract CPLD firmware archive, it will contain a *.jbc (Jam Byte Code) file and a binary "jbi" that can be used to flash the CPLD with the bytecode
2. From petitboot or an OS loaded on the host use jbi to update the CPLD:
    a. `./jbi -aprogram barreleye_v20_160120.jbc`

8 BMC

The motherboard uses a BMC for various platform management services and interfaces with hardware, BIOS.

The BMC is a standalone system in parallel to the host. The health status of the host system should not affect the normal operation and network connectivity of the BMC. The BMC cannot share memory with the host system. BMC management connectivity should work independently from the host. If using a shared NIC, there should be no NIC driver dependency for out-of-band (OOB) communication.

8.1 Management Network Interface

The BMC support RMII/NCSI port for OOB access. Shared-NIC (host and BMC) uses RMII/NCSI interfaces to pass management traffic on BroadCom BCM5720. BCM5720 has 10/100/1000 MDI interface to RJ45(LAN1). Some Barreleye implementations can also support a BCM5719A for Link Flap Avoidance improvements, but are not presently documented here. A 5719A implementation (including board files) may be added as an addendum to a future version of this specification.

8.2 Local Serial Console and Serial-Over-LAN(SOL)

The BMC needs to support two access paths to the serial console:

1. A local serial console on debug header, described in section 8.12.2.
2. A remote console, available via IPMI Serial-Over-LAN (IPMI-SOL), or Secure Shell (SSH), through the management network.

8.3 Graphic and GUI

Graphic and GUI features integrated in BMC (ASPEED AST2400) chip.

8.4 Remote Power Control and Power Policy

BMC firmware to support remote system power on/off/cycle and warm reboot through the In-Band or Out-of-Band IPMI, ReST, or SSH commands.

BMC firmware to support power on policy to be last-state, always-on and always-off. The default setting is Last-State. The change of power policy should be supported by IPMI, ReST, or SSH command and take effect without a BMC firmware cold reset or a system reboot.

It should take less than 3 seconds from AC on, for the BMC to process the power button signal and to power the system for POST. A long waiting period for the BMC firmware to get ready before allowing a system POST start is NOT allowed.

8.5 Power and System Identification LED

The motherboard must combine the Power LED and the System Identification LED into a single blue LED at the front side.

There are 4 states of Power/system identification LED depending on system power state, and chassis identify status.

Power off, Chassis identify off: LED consistently off

Power off, Chassis identify on: LED on for 0.1sec, off for 0.9sec, and loop

Power on, Chassis identify off: LED consistently on

Power on, Chassis identify on: LED on for 0.9sec, off for 0.1sec, and loop

Power LED on is defined by the readiness of all power rails

Blinking the Power LED blinking is used as a system identifier. The on time is different during power on and power off.

8.6 BMC Heartbeat LED

LED always Light: AUX PW OK

LED Blink: BMC ACTIVE(FW Ready)

8.7 Power and Thermal Monitoring and Power Limiting

BMC firmware supports platform power monitoring. Power limiting for processor, memory, and platform is required. Access to this function must be available through In-Band and Out-of-Band.

BMC FW supports thermal monitoring, including processor, memory, chipset, and Inlet/outlet air temperatures.

8.8 Sensors

This portion of the specification is still in development. See production files and BoM available alongside this specification for current implementation.

8.9 System Event Log (SEL)

This portion of the specification is still in development. See production files and BoM available alongside this specification for current implementation.

8.10 Fan Speed Control in BMC

BMC I2C connect to HW monitor1/2 to control FAN PWN and read FAN tach. Blue & Red LEDs show FAN status, and these 2 LEDs are controlled by BMC.

8.11 BMC Firmware

Barreleye can support a variety of BMC firmware solutions, including OpenBMC.

OpenBMC is available primarily through two GitHub repositories:

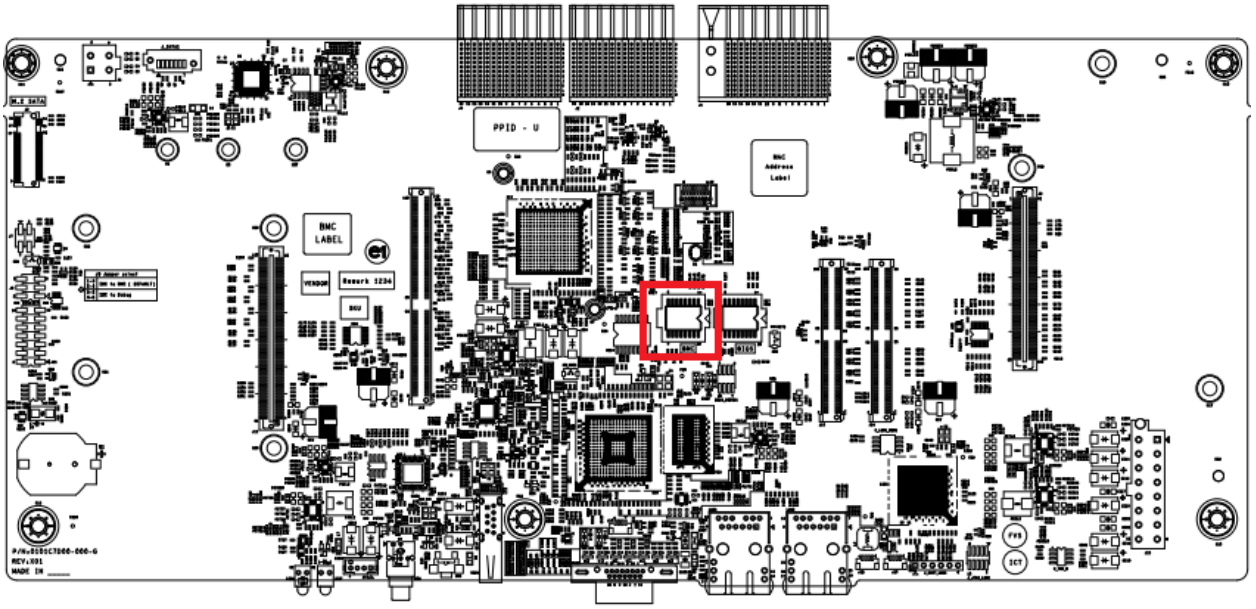
1. The Facebook / OpenBMC repository: https://github.com/facebook/openbmc
2. The OpenBMC / OpenBMC repository: https://github.com/openbmc/openbmc
    a. This repository includes most OpenPOWER & Barreleye-specific contributions.
    b. Specific drivers for OpenPOWER machines were contributed here: https://github.com/openbmc/openbmc/tree/master/meta-openbmc-machines/meta-openpower

OpenBMC source code is available under its own license scheme.

8.12 BMC Firmware Update Methods

8.12.1 Physical Method

Replace BMC ROM with the updated one. The following figure shows the location of BMC ROM socket on IO board.



8.12.2 Host Operating System Method

1. Log in Linux OS
2. Copy the package into disk
3. Execute socflashtool.sh in folder `\SOCFlash\Linux`

When BMC is finished updating, the system will be shut down and BMC reset and Beep LED(amber) will be lighted. After Beep the LED turns off, the BMC is ready and can be power on again, by pushing power button

8.12.3 Direct-to-BMC-Over-Network-Interface Method

1. Connect to BMC via LAN (ssh connection)
2. Update settings:

   ◦ preserve_network_settings = Preserve network settings, only needed if updating uboot

   ◦ restore_application_defaults = update read-only file system

   ◦ update_kernel_and_apps_only = update kernel and initramfs

   ◦ clear_persistent_files = Erase persistent files
3. Set settings:

   ```
   curl -k -H "Content-Type: application/json" -X PUT -d "{\"data\": 1}"
   ```

   https://bmc/org/openbmc/control/flash/bmc/attr/<setting>
4. Update from a TFTP server:

   ```
   curl -k -H "Content-Type: application/json" -X POST -d
   "{\"data\": “<TFTP server IP address>”,”<filename>”}"
    https://bmc/org/openbmc/control/flash/bmc/action/updateViaTftp
   ```

8.13 BMC Update BIOS

1. Transfer a copy of the BIOS image to flash into the /tmp directory of OpenBMC
2. Use the "pflash" utility to erase and program the BIOS PNOR
   a. `pflash -E -p /tmp/barreleye_0.2.0.pnor`

9 Thermal Design Requirements

Thermal design can support 35degC ambient with two 190W Power8 in 1.25OU sled under one fan fail condition. Please refer to Barreleye Thermal Spec for more details.

10 Motherboard Power system

10.1 Input Voltage

The motherboard can accept and operate normally at an input voltage tolerance range between 10.8V and

13.2V. The motherboard's main power under-voltage protection level is 9.5V (Typ.).

10.2 Hot Swap Controller (HSC) Circuit

In order to have better control of the 12.5VDC power input to motherboard.

The motherboard include three hot swap controllers, two for main power and one for stand-by power. The hot swap controller provides:

- Inrush current control when the motherboard is inserted and the server is powered on.
- Current limiting protection for short circuits.
- PMBUS interface to enable the BMC to report server input power.

10.3 CPU Voltage Regulator (VR)

7.3.1 CPU Maximum Power

The motherboard shall be designed to handle a processor with a maximum TDP of 190W CPU.

7.3.2 CPU VRM Efficiency

The minimum efficiency for the CPU VRM efficiency is 82% over the 30% to 90% load range and 84% over the 50% to 70% load range for TDP power of CPU, measured from the 12.5V input to the VRM output.

7.3.3 CPU Core VR Configuration

The guaranteed rewrite count of NVRAM should be equal to 8.

7.4 Memory Buffer Voltage Regulator

7.4.1 DIMM Power Rails

The motherboard design should have DIMM Power Rails for DDR3.

7.4.2 DIMM VR Configuration

The guaranteed rewrite count of NVRAM should be equal to 8.

7.5 Voltage Regulator Module Design Guideline

All regulators in the system response to an over-current event must be verified. A typical over-current set point is 25% or more above the maximum load current.

7.6 Hard Drive Power

7.7 System VRM Efficiency

High-efficiency VRMs for all other voltage regulators over 20W and under 5W not defined in this specification. All other voltage regulation modules shall be 82% efficiency over the 30% to 90% load range.

7.8 Power On

The motherboard should be set to restore the last power state during AC on/off. This means when the AC cycles on/off, the motherboard should power on automatically without someone pressing the power button. When the motherboard is powered off on purpose, it should be kept off through AC on/off.

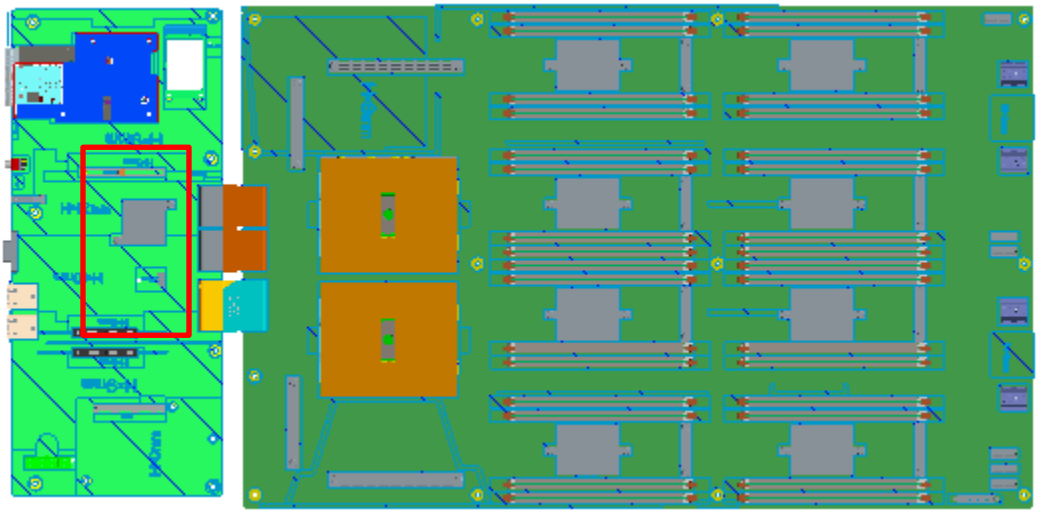
7.9 APSS

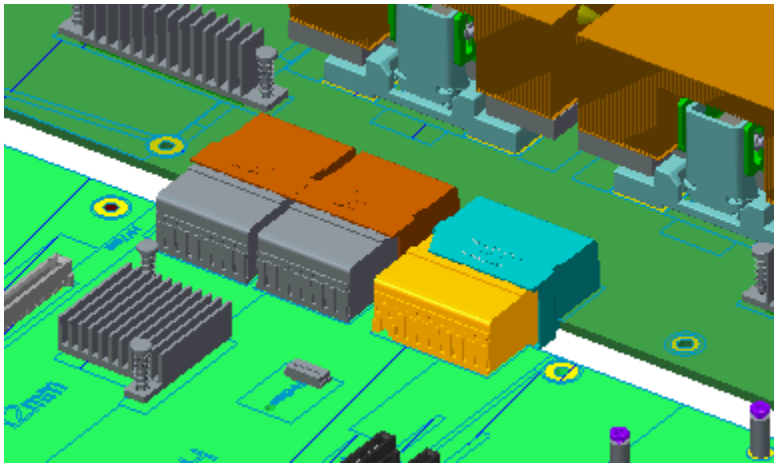
Use for current monitoring of all 240VA, and connect to CPU through SPI interface. On Chip Controller(OCC) of CPU communicates with APSS and calculates the total power consumption of system, then determines if the system needs to do the power capping. APSS also connects to BMC through I2C interface, so BMC can know the system load current as well.

8 I/O System

8.1 Impact Board to Board Connector

The Impact board to board connectors are connected between MB and I/O board. There are 3 Impact connectors, refer to the attachment for more details.





Molex Connector Pinout_20150519_17

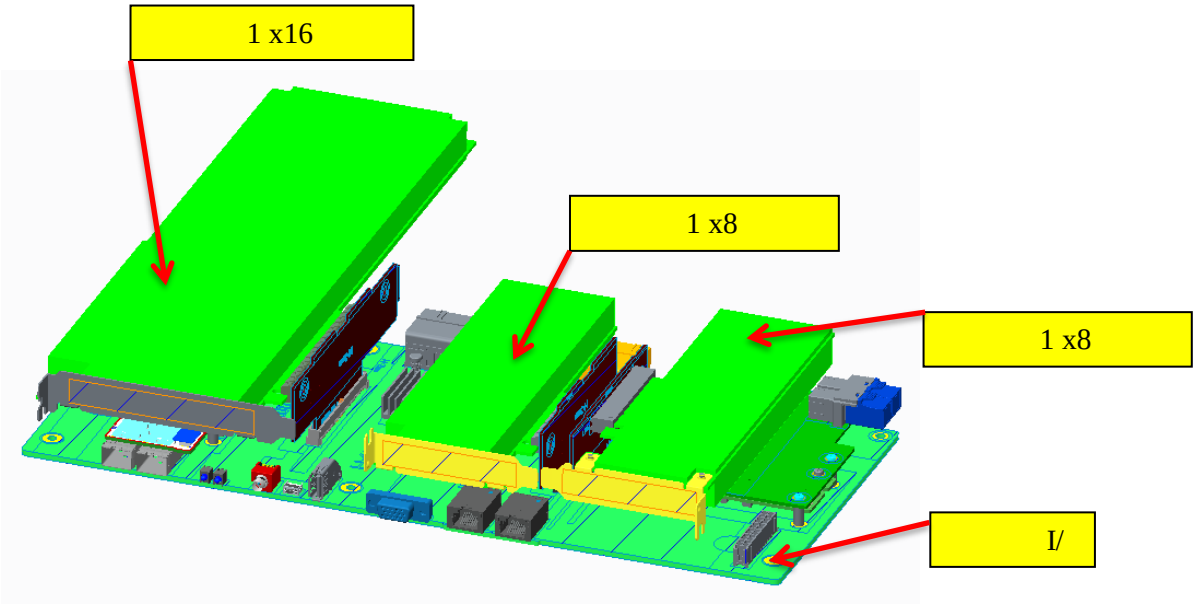
8.2 DIMM Connector

The DIMM connector is SMT type and support DDR3 DIMM. DIMM connectors must also include lubricant/sealant applied by the connector manufacturer which can remain intact after soldering and other manufacturing processes. The sealant is required to displace any voids in the connector gold plating.

8.3 PCIe Slot Connector/Riser Card

The mother board support 3 PCIE cards, but use non-standard PCIE connectors on mother board, need the corresponding riser cards to support standard PCIE cards. Can support 1 x 16 Gen3 FH/FL and 2 x8 Gen3 LP/HL.

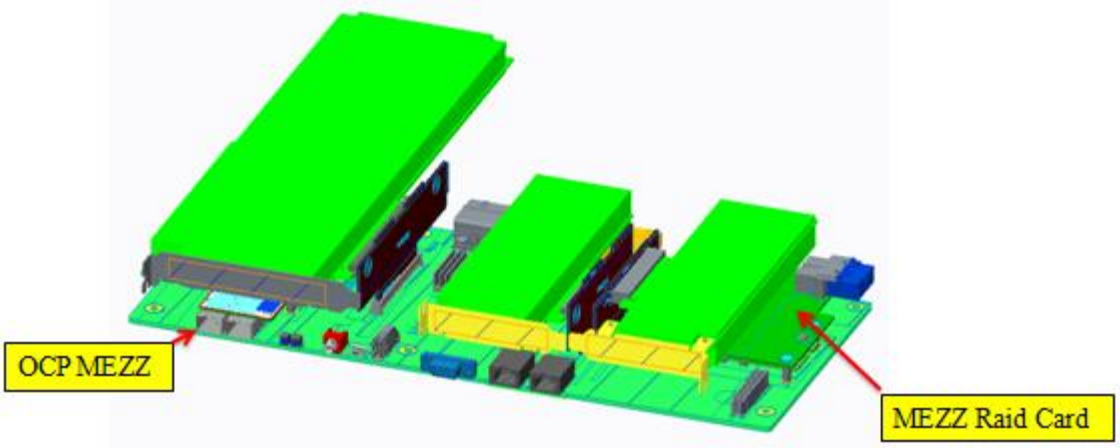
See below for the figures of 3 riser cards.



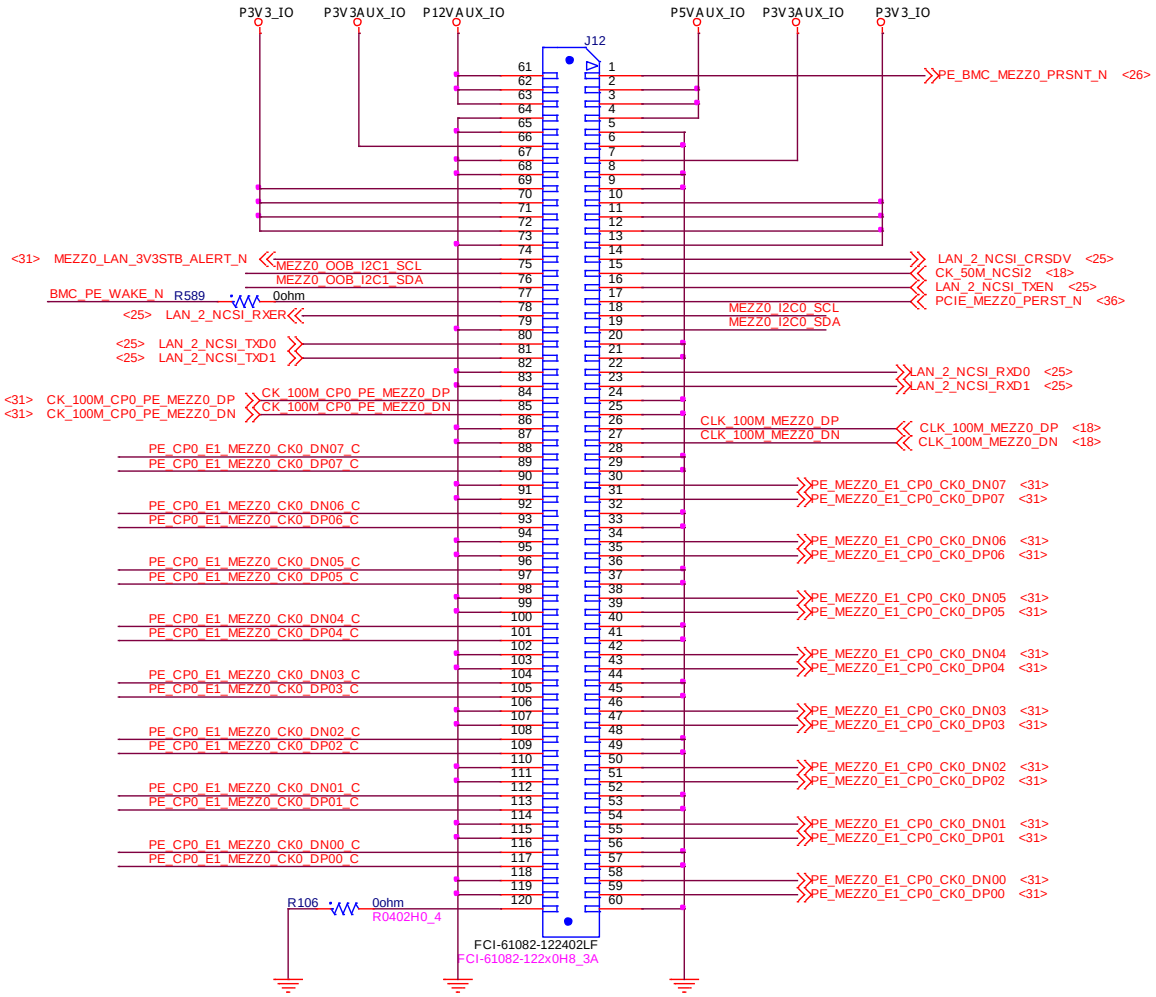
8.4 OCP PCI-E Mezzanine Card

Two OCP mezzanine connectors (support PCIE Gen3) are placed on the IO board to support 1 x8 OCP mez connector with front Panel access and 1 x8 mez connector for internal slot to support Raid-on-chip with battery backup or SuperCap.

1 x8 OCP mez connector with front Panel access supports standard OCP form factor card. Another 1 x8 OCP mez connector for internal slot loosely follows OCP mezzanine specifications, which is only for RAID function and built LSI 3108 on board.



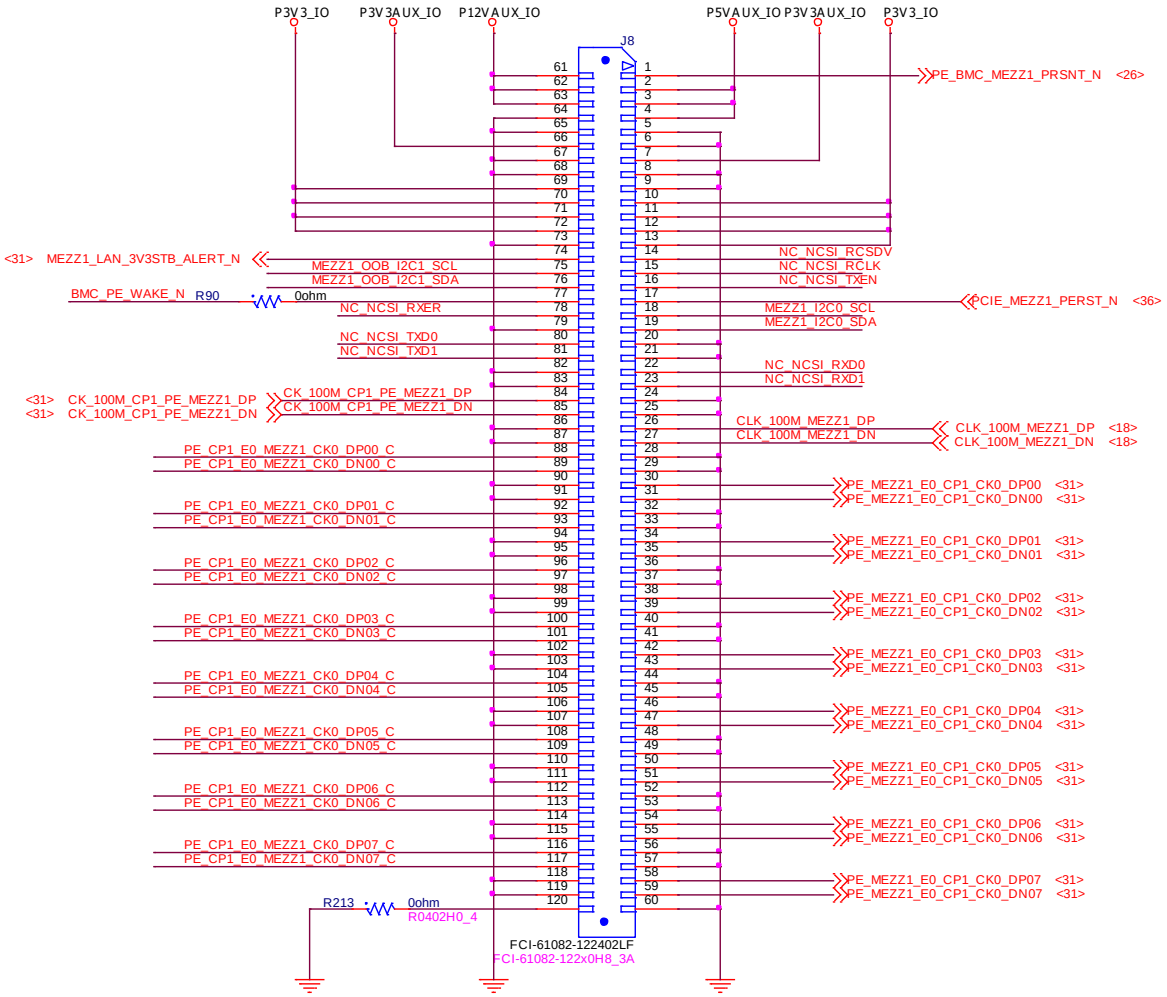
OCP MEZ connector



OCP MEZ Connector Signal Definitions		
Signal	**I/O**	**Definition**
PE_BMC_MEZZ0_PRSNT_N	O	OCP MEZ Connector present pin, connect to pin 120 on MEZ card with 0ohm
LAN_2_NCSI_RXER	I	NC-SI for OOB management
LAN_2_NCSI_RXD[0:1]	I	

LAN_2_NCSI_CRSDV	I	
LAN_2_NCSI_TXEN	O	
LAN_2_NCSI_TXD[0:1]	O	
LAN_2_NCSI_TXEN	O	
CK_50M_NCSI2	I	NC-SI 50M input clock
MEZZ0_I2C0_SCL	I	PCIe I2C Clock for Mez slot/EEPROM;
MEZZ0_I2C0_SDA	I/O	PCIe I2C Data for Mez slot/EEPROM;
MEZZ0_LAN_3V3STB_ALERT_N	O	I2C Alert for OOB management
MEZZ0_OOB_I2C1_SCL	I	I2C Clock for OOB management
MEZZ0_OOB_I2C1_SDA	I/O	I2C Data for OOB management
BMC_PE_WAKE_N	I	PCIe wake up signal
CK_100M_CP0_PE_MEZZ0_DP/N	I	1st MB clock output for PCIe devices
CLK_100M_MEZZ0_DP/N	I	2nd MB clock output for PCIe devices
PE_CP0_E1_MEZZ0_CK0_DP/N[00:07]	I	PCIe Gen3 from CPU to OCP MEZ
PE_MEZZ0_E1_CP0_CK0_DP/N[00:07]	O	PCIe Gen3 from OCP MEZ to CPU
P3V3_IO	O	3.3V input power
Ground	I/O	Ground pins

MEZ RAID connector

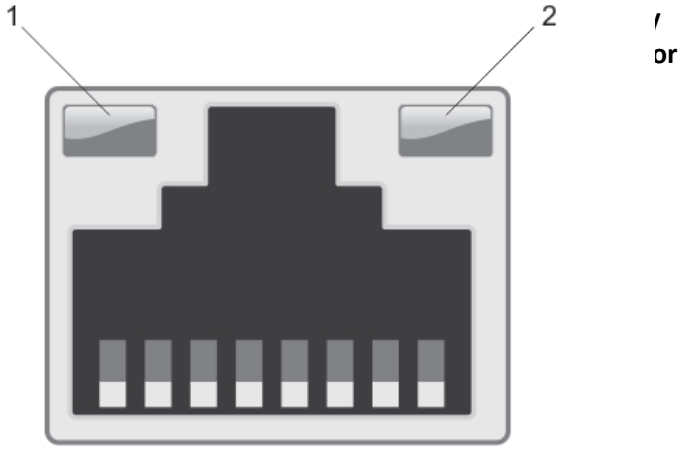


MEZ RAID Connector Signal Definitions		
Signal	**I/O**	**Definition**
PE_BMC_MEZZ1_PRSNT_N	O	OCP MEZ Connector present pin, connect to pin 120 on MEZ card with 0ohm
MEZZ1_I2C0_SCL	I	PCIe I2C Clock for Mez slot/EEPROM;
MEZZ1_I2C0_SDA	I/O	PCIe I2C Data for Mez slot/EEPROM;

MEZZ1_LAN_3V3STB_ALERT_N	O	I2C Alert for OOB management
MEZZ1_OOB_I2C1_SCL	I	I2C Clock for OOB management
MEZZ1_OOB_I2C1_SDA	I/O	I2C Data for OOB management
BMC_PE_WAKE_N	I	PCIe wake up signal
CK_100M_CP1_PE_MEZZ1_DP/N	I	1st MB clock output for PCIe devices
CLK_100M_MEZZ1_DP/N	I	2nd MB clock output for PCIe devices
PE_CP1_E0_MEZZ1_CK0_DP/N[00:07]	I	PCIe Gen3 from CPU to MEZ RAID
PE_MEZZ1_E0_CP1_CK0_DP/N[00:07]	O	PCIe Gen3 from MEZ RAID to CPU
P3V3_IO	O	3.3V input power
Ground	I/O	Ground pins

8.5 Network

Support two RJ-45 10/100/1000 LAN ports. NIC Indicators are shown below.

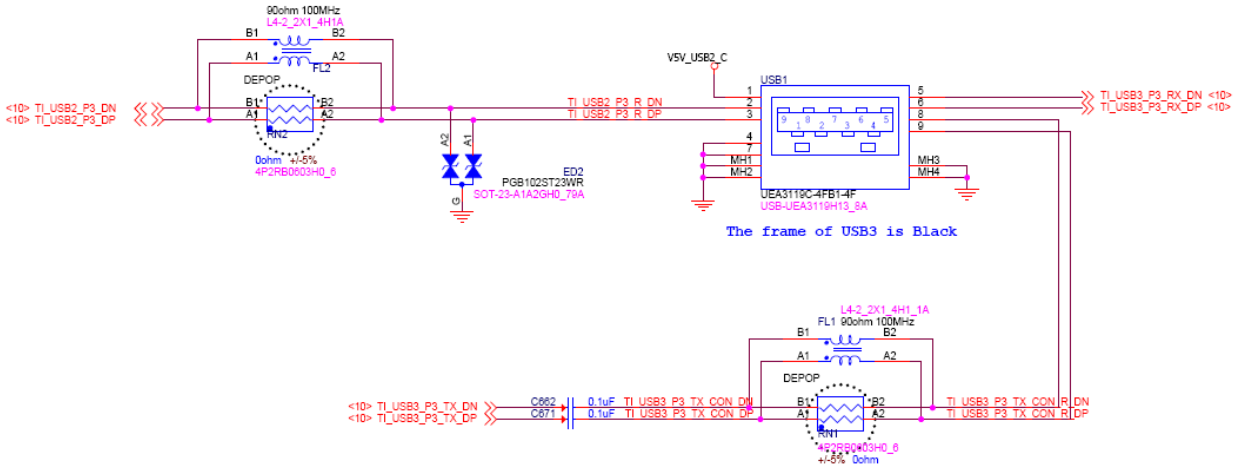


LAN LED Behavior	
Indicator	**Indicator Code**
Link and activity indicators are off	The NIC is not connected to the network
Link indicator is green	The NIC is connected to a valid network at its maximum port speed (1Gbps or 10Gbps)
Link indicator is amber	The NIC is connected to a valid network at less than its maximum port speed
Activity indicator is green blinking	Network data is being sent or received

8.6 USB

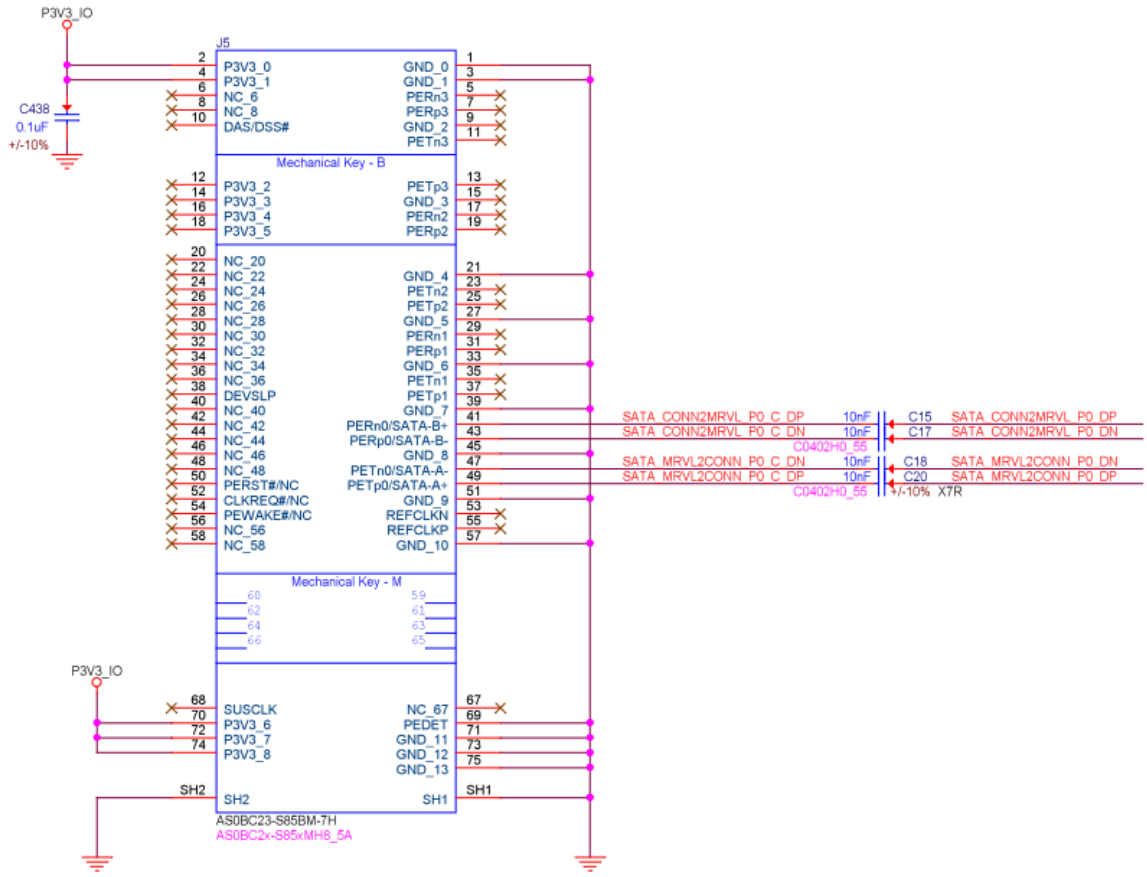
Support one USB3.0 connector put on front side for user used

USB 3.0 Circuit : USB1 is USB3.0 connector, can support USB3.0 device.



8.7SATA

Support one M.2 connector on I/O board to support M.2 SATA device.



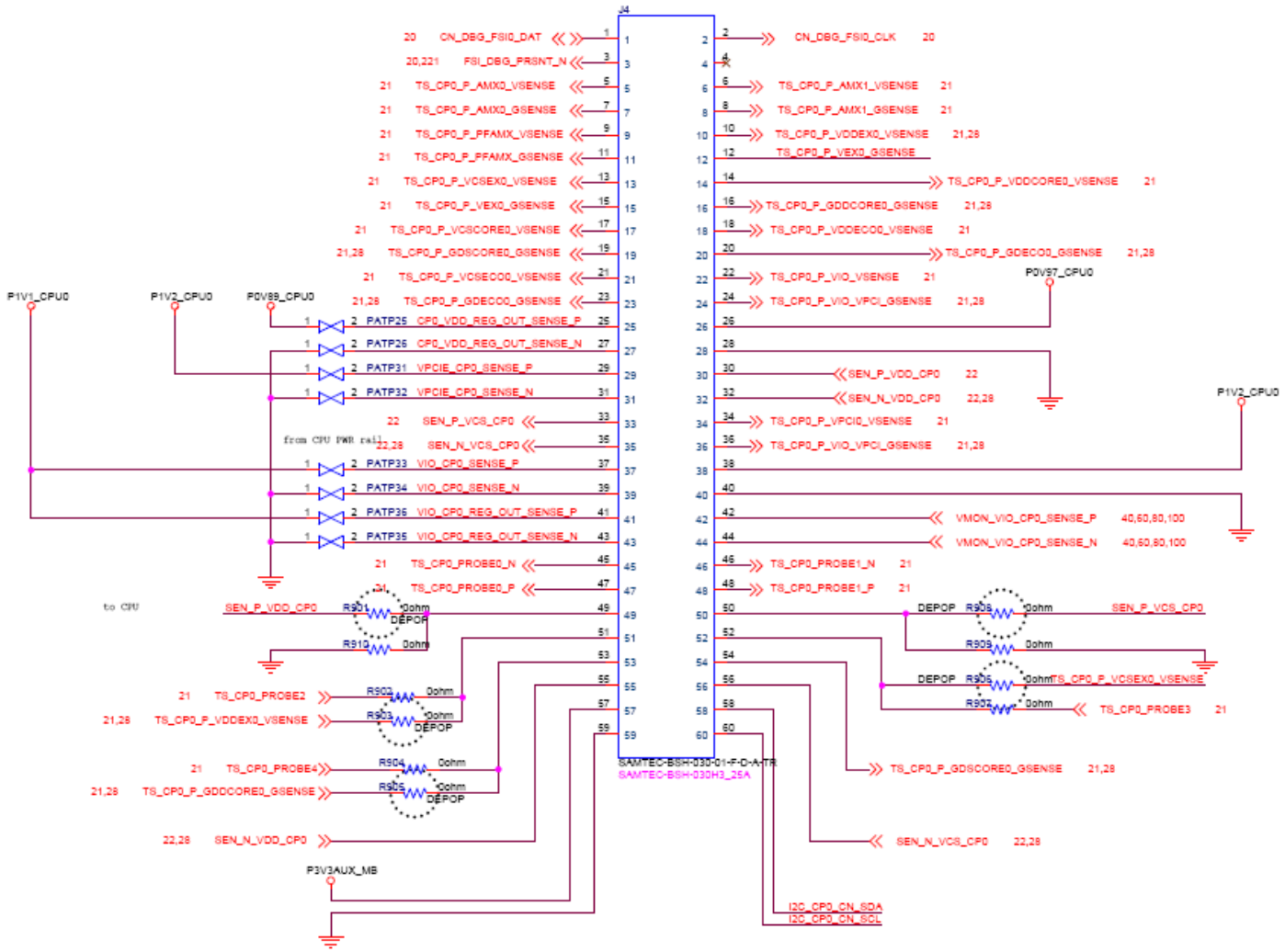
M.2 Connector Signal Definitions		
Signal	**I/O**	**Definition**
SATA_MRVL2CONN_P0_C_DP/N	I	SATA signals from SATA controller to M.2 connector

SATA_CONN2MRVL_P0_C_DP/N	O	SATA signals from M.2 connector to SATA controller
P3V3_IO	O	3.3V input power
Ground	I/O	Ground pins

8.8Debug Header

There's a debug header (J4 Connector), the function is CPU status monitoring and some Power sensor.

J4 Connector



8.9 Switches and LEDs

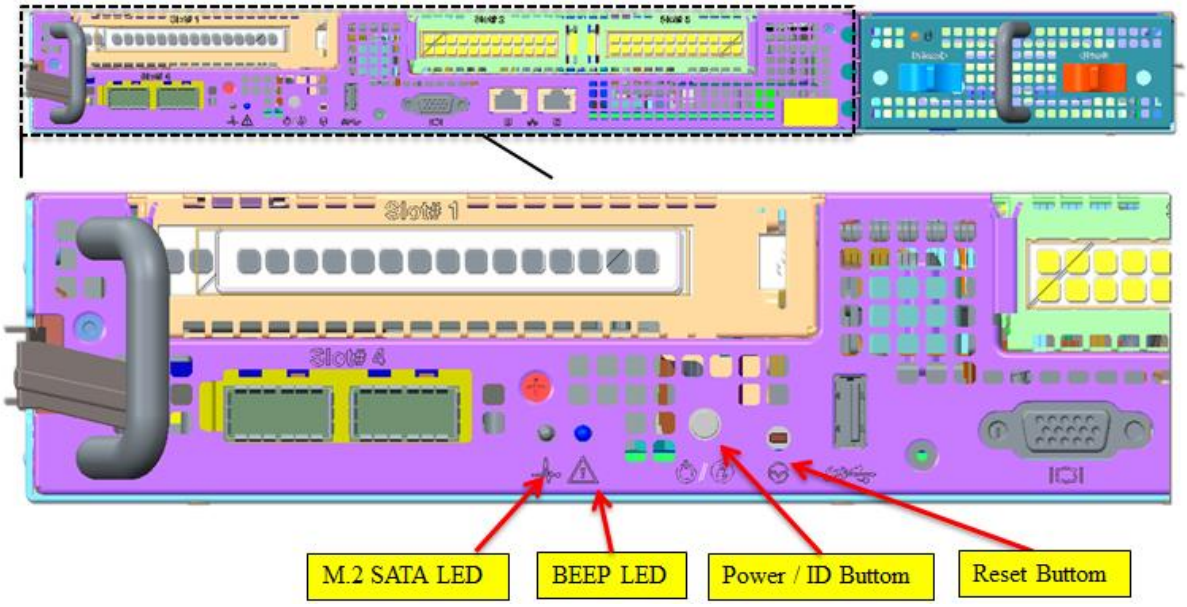
The motherboard shall include a power switch, a reset switch, a power LED(combine ID LED), an M.2 SATA HDD activity LED and a beep error LED on front side.

8.9.1 Switches

Two switches put on front-side, one is POWER button and another is RESET button.

When the motherboard is powered off, the end user must push the Power / ID button to power on the system.

The RESET button is designed to generate a platform reset to reset BMC and TPM module.



8.9.2 Power, M.2 SATA HDD & BEEP LEDs

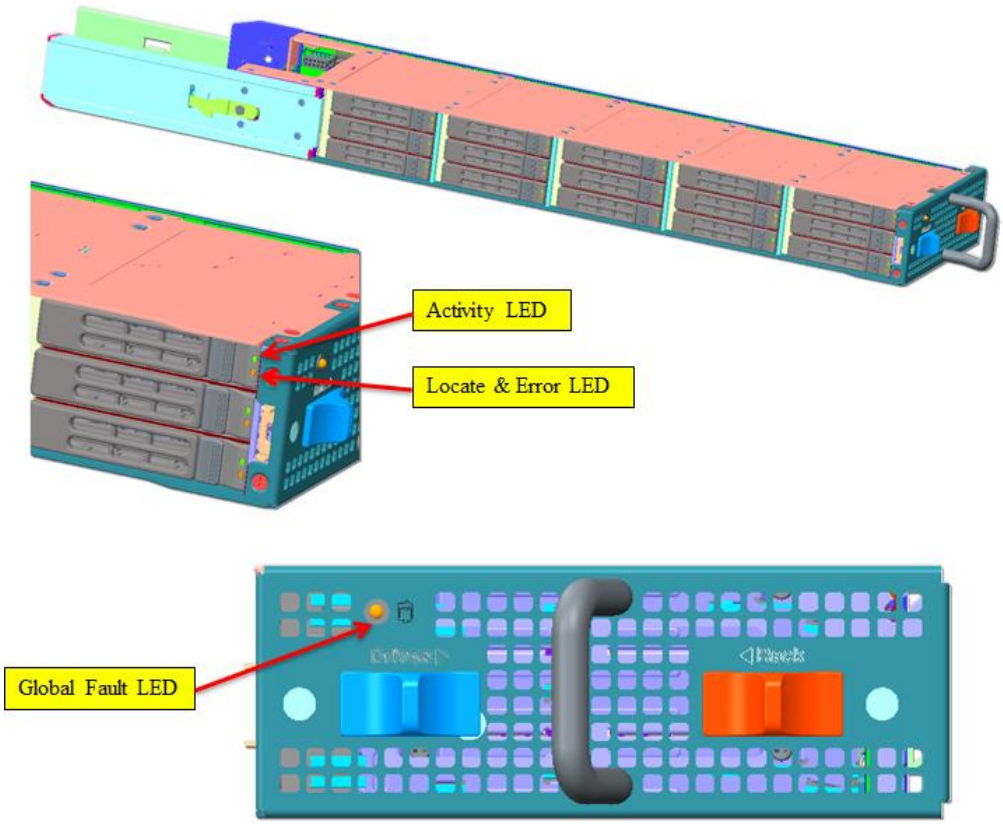
The label describes the functionality of Power, M.2 SATA HDD & BEEP LED.

Front I/O LED Behavior			
LED Type	**LED Color**	**Function**	**LED Pattern**
Power/ System ID LED	Blue	Power LED on is defined by the readiness of all power rails. Blinking the Power LED blinking is used as a system identifier	**Power off, Chassis identify off:** LED consistently off **Power off, Chassis identify on:** LED on for 0.1sec, off for 0.9sec, and loop **Power on, Chassis identify off:** LED consistently on **Power on, Chassis identify on:** LED on for 0.9sec, off for 0.1sec, and loop
BEEP LED	Yellow	This LED indicates the BMC status. When the LED becomes off, BMC is ready and will power on the system automatically	**BMC code initialing:** LED consistently on **BMC ready:** LED consistently off
M.2 SATA LED	Green	SATA controller detected M.2 SATA HDD, but M.2 SATA hard drive no activity	Always light
		M.2 SATA hard drive activity. This LED illuminates when M.2 SATA hard drive is activity	Blinking

8.9.3 HDD Carrier & Tray LEDs

Controlled by expander FW.

<table>
<tr><th colspan="5">HDD Carrier and Tray LED Behavior</th></tr>
<tr><th>Location</th><th>LED Type</th><th>LED Color</th><th>Function</th><th>LED Pattern</th></tr>
<tr><td rowspan="3">HDD Carrier</td><td>Locate LED</td><td>Green</td><td rowspan="3"><table>
<tr><th>Condition/Event</th><th>Priority (Highest = 0x0 Lowest = 0x11)</th><th>Error LED Pattern</th><th>Locate LED pattern</th></tr>
<tr><td>INDENT</td><td>0x00</td><td>OFF</td><td>ON 125ms
OFF 125ms</td></tr>
<tr><td>FAULT</td><td>0x01</td><td>ON</td><td>OFF</td></tr>
<tr><td>RR_ABORT</td><td>0x02</td><td>ON 125ms
OFF 125ms</td><td>OFF</td></tr>
<tr><td>REBUILD_REMAP</td><td>0x03</td><td>OFF</td><td>ON 500ms
OFF 500ms</td></tr>
<tr><td>HOT_SPARE</td><td>0x04</td><td>ON 500ms
OFF 500ms</td><td>OFF</td></tr>
<tr><td>NO_COND</td><td>0x05</td><td>OFF</td><td>OFF</td></tr>
<tr><td>DO_NOT_REMOVE</td><td>0x06</td><td>OFF</td><td>OFF</td></tr>
</table></td></tr>
<tr><td>Error LED</td><td>Amber</td></tr>
<tr><td>Activity LED</td><td>Green</td></tr>
<tr><td rowspan="2">HDD Tray</td><td rowspan="2">Global Fault LED</td><td rowspan="2">Amber</td><td>“link” down errors between SEB and HDD drives – When HDDs occur “FAULT”, “PRD_FAULT”, “PR_ABORT” or “HOT_SPARE” event</td><td>Always light</td></tr>
<tr><td>“link” down errors between the RoC & SEB</td><td>ON 500ms
OFF 500mS</td></tr>
</table>

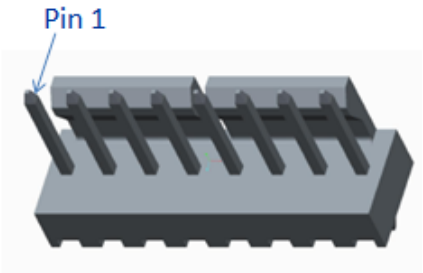

Activity LED
Locate & Error LED
Global Fault LED

8.10 Fan Connector & LEDs

8.10.1 Fan Connector

The motherboard has six fan connectors, and support one fan fail functionality.

The fan connector pin definitions as below, support a dual rotor fan that shares a PWM control signal but has separate tachometer signals. And support two LED to show FAN status.

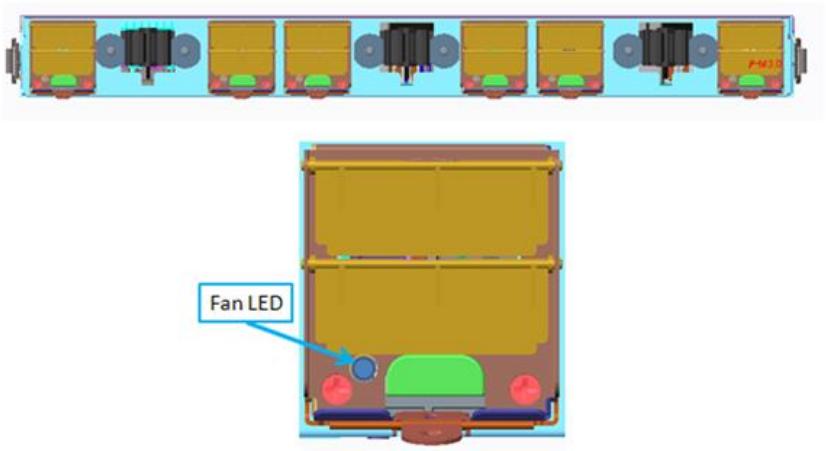


Fan Connector Signal Definitions		
Pin	**Wire**	**Definition**
1	White Wire	LED Power, Connect to 3.3V AUX
2	Blue Wire	Blue LED -
3	Red Wire	Red LED -
4	Blue Wire	Fan Tach of Front Fan
5	White Wire Green Wire	PWM of Front FAN PWM of Rear FAN
6	Yellow Wire	Fan Tach of Rear Fan
7	Red Wire Orange Wire	Main Power of Front Fan, Connect to 12V

		Main Power of Rear Fan, Connect to 12V
8	Black Wire Brown Wire	GND of Front Fan GND of Rear Fan

8.10.2 Fan LEDs

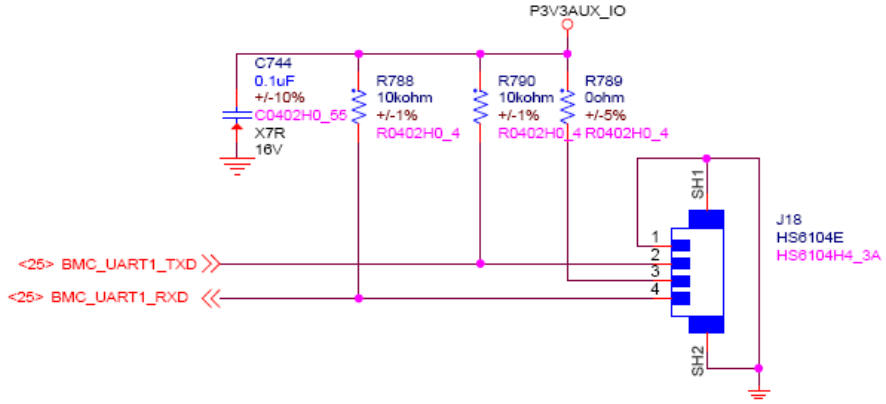
Fan LED Behavior			
LED Color	**Function**	**LED Pattern**	**Comment**
Blue	Fan normal operation	Always light	Bi-color LED and integrated Fan modules
Red	Fan fault	Always light	



8.11 UART Connector

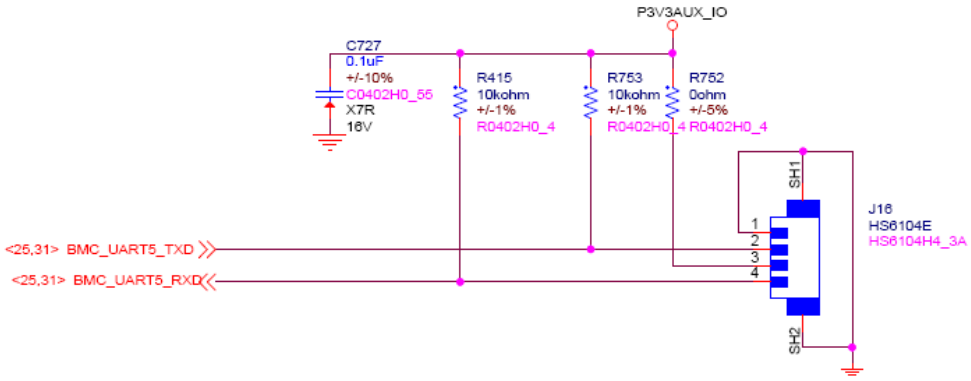
8.11.1 System UART

There is a system UART connector J18, which can be redirected to be controlled by LPC bus as physical UARTs of host system.



8.11.2 BMC Debug UART

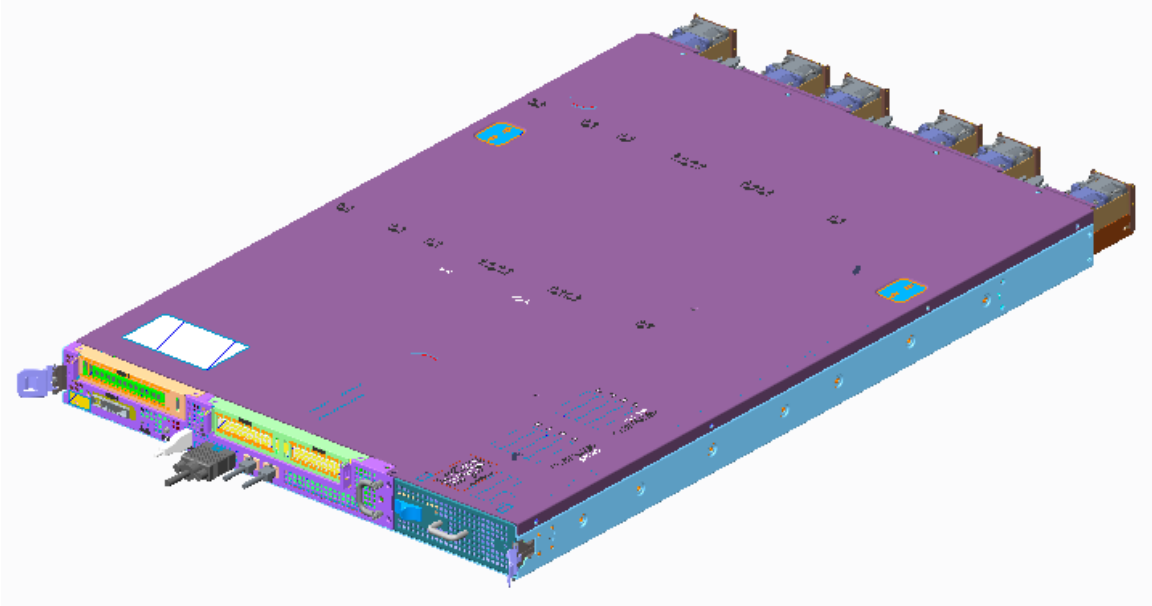
There is a debug UART connector J16 only for BMC console, which is only for BMC designer debug used.



9 Mechanical

9.1 Sled

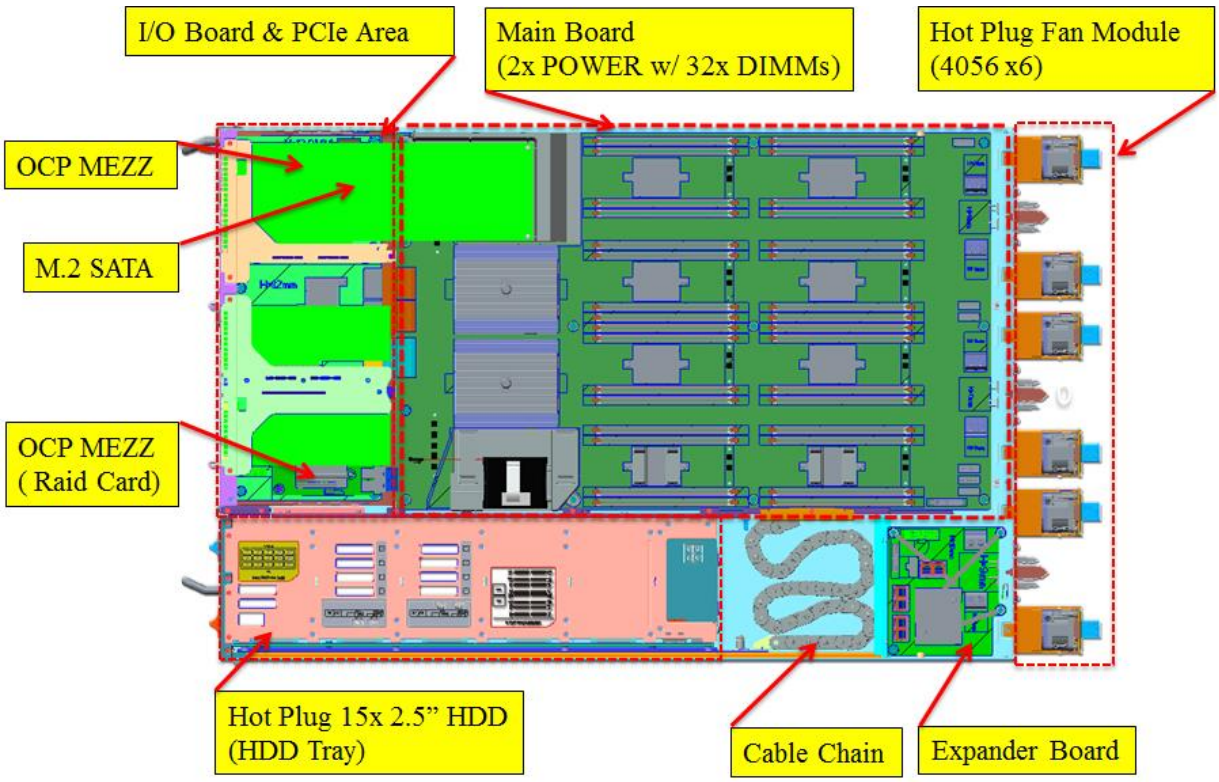
The 1.25OU sled has the dimensions, 537x897.1x56.8mm.



9.2 Top View

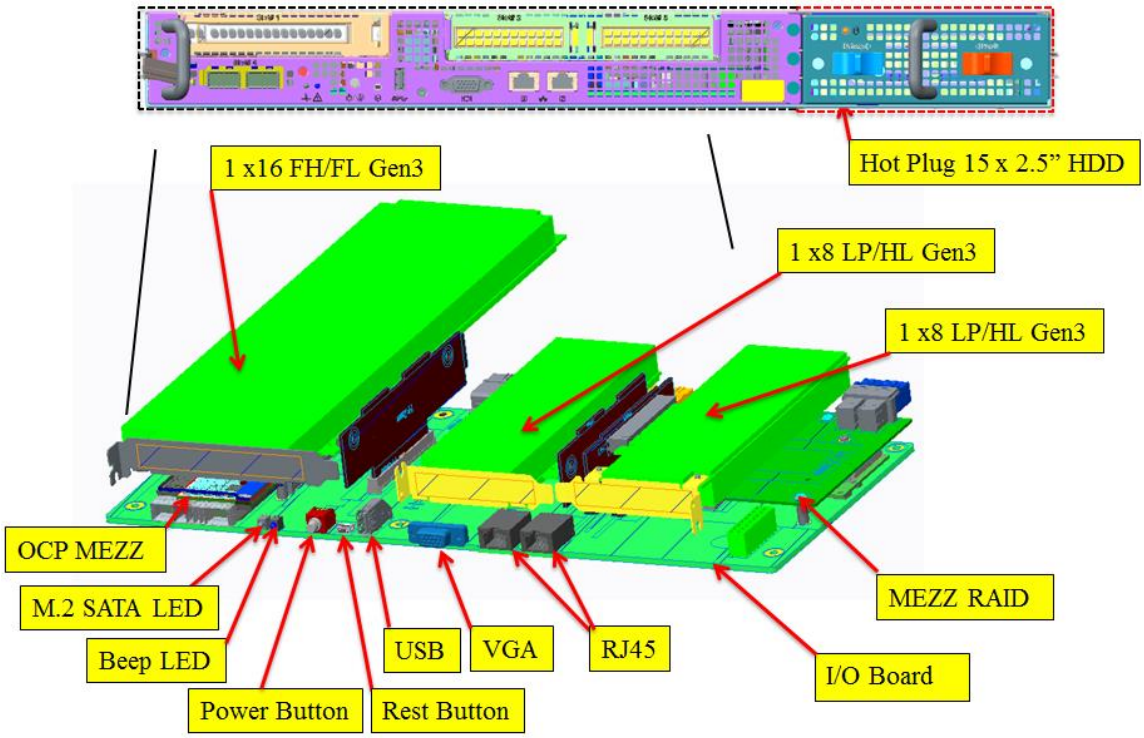
Barreleye supports hot-pluggable 2.5" HDD drives and Fan modules. There are 4 main boards in the system.

They are Main board, I/O board, Expander board and HDD BP.



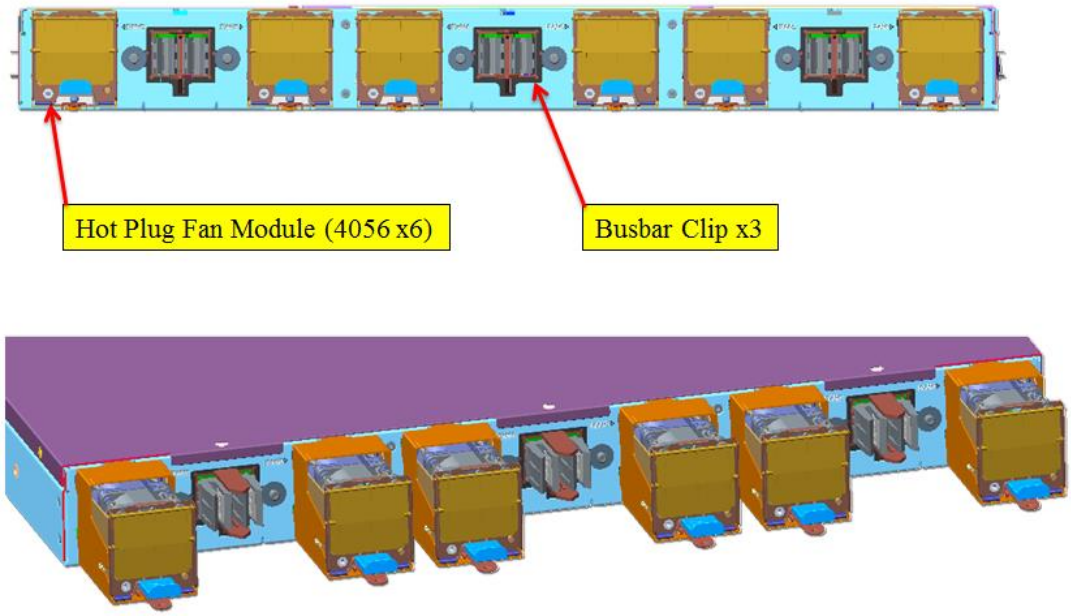
9.3 Front View

Barreleye supports two x8 LP/HL Gen 3, one x16 FH/FL Gen3 cards and one OCP MEZ Raid Card. The I/O connectors are located on the front. There is one HDD Tray on the right which contains 15pcs Hot-Pluggable 2.5" HDD drives.



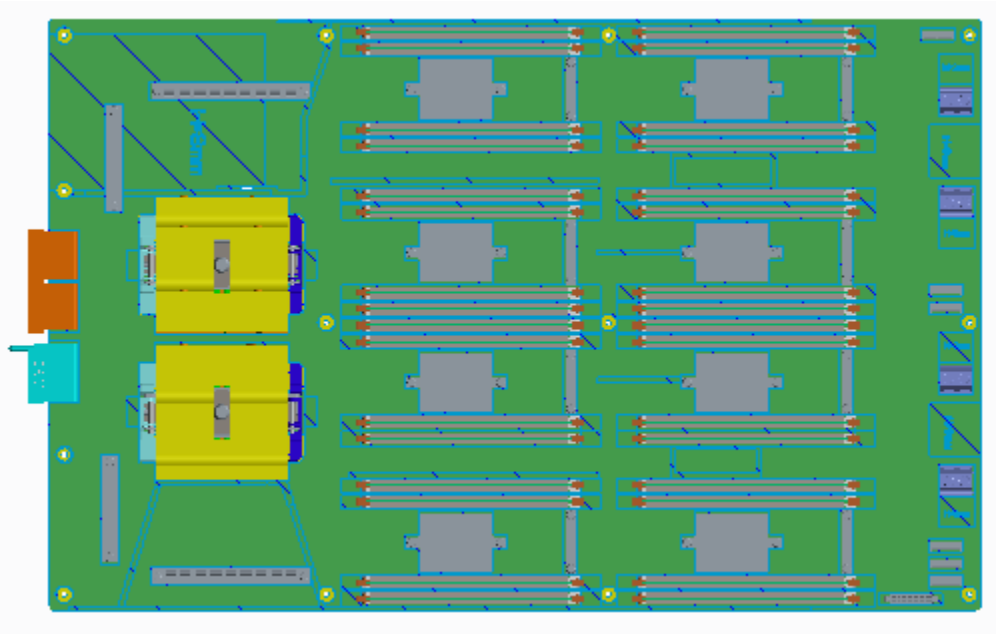
9.4Rear View

There are three standard OCP Bus bar clips and 6 Hot-pluggable Fan Modules on the rear wall.



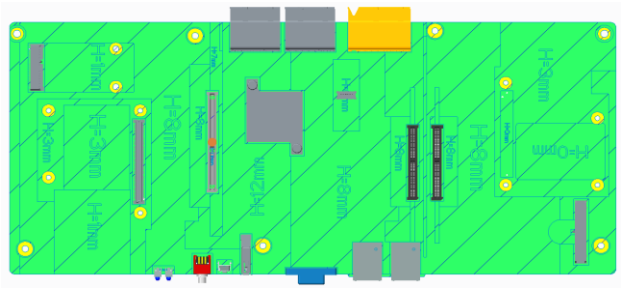
9.5 MB

The dimensions of Main board are 600x380mm. It supports two Power CPUs and 32 DIMMs.



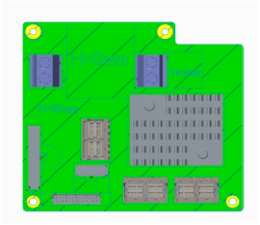
9.6 I/O Board

The dimensions of I/O board are 367.5x160mm. It connects to the main board through the BTB connectors.



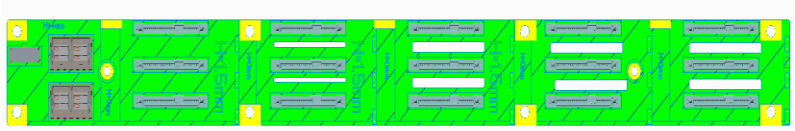
9.7 Power Expander Board

The dimensions of Power Expander board are 130x120mm. It conducts the SAS signal and Power to I/O board and HDD BP through the cables.



9.8 BPx15

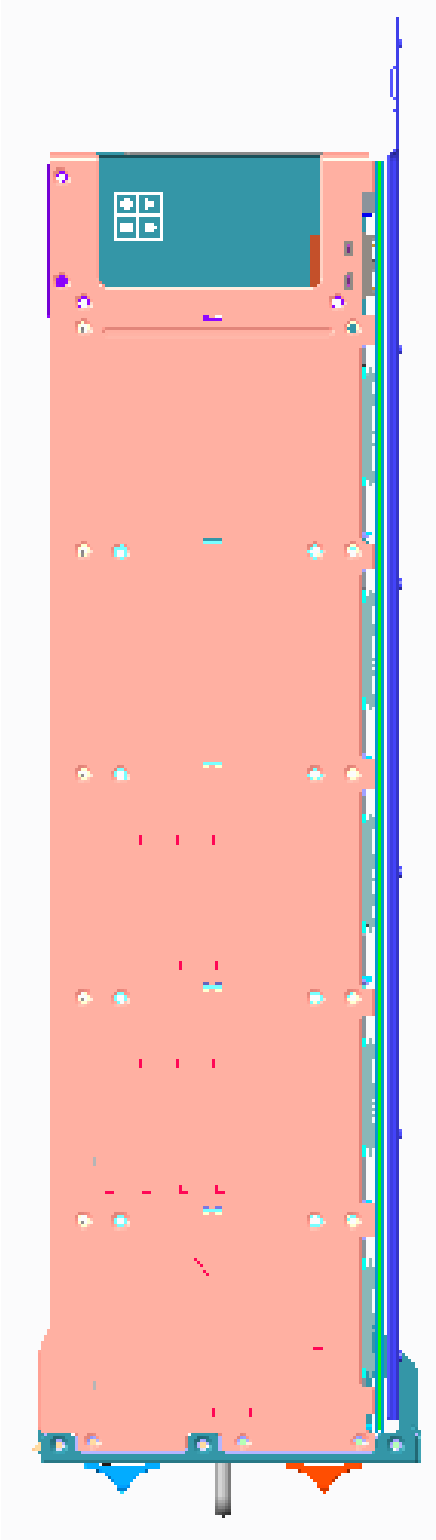
The dimensions of HDD BP are 485.5x50mm.



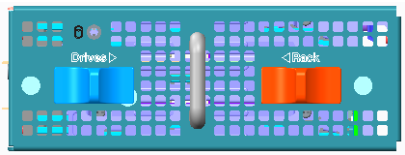
9.9 Hard Drive Tray

The dimension of Hard Drive Tray is 573.8mm (L) x 146.1mm (W) x 53.6mm (H).

9.9.1 Top View



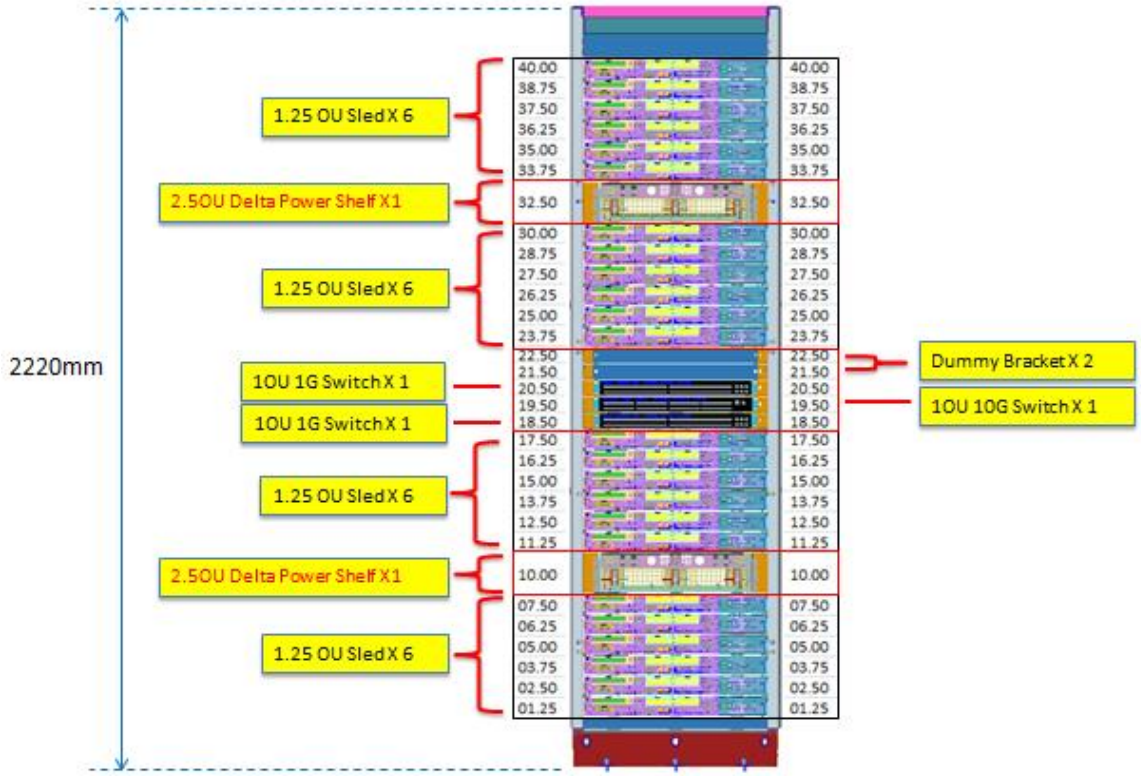
9.9.2 Front View



9.10 Rack

Barreleye Rack is one standard OCP rack. The configuration shows below. The Switch zone is in the middle.

One Powershelf to support 12 sleds is on the top and another Powershelf with 12 Sleds on the bottom.



9.11 Rack Knife

In order to accommodate the 1.25OU sled into this standard OCP rack, except the standard Support Bracket, we have one special Support Bracket which has 12mm gap from the standard one. These two kinds of brackets are assembled on the rack alternately.

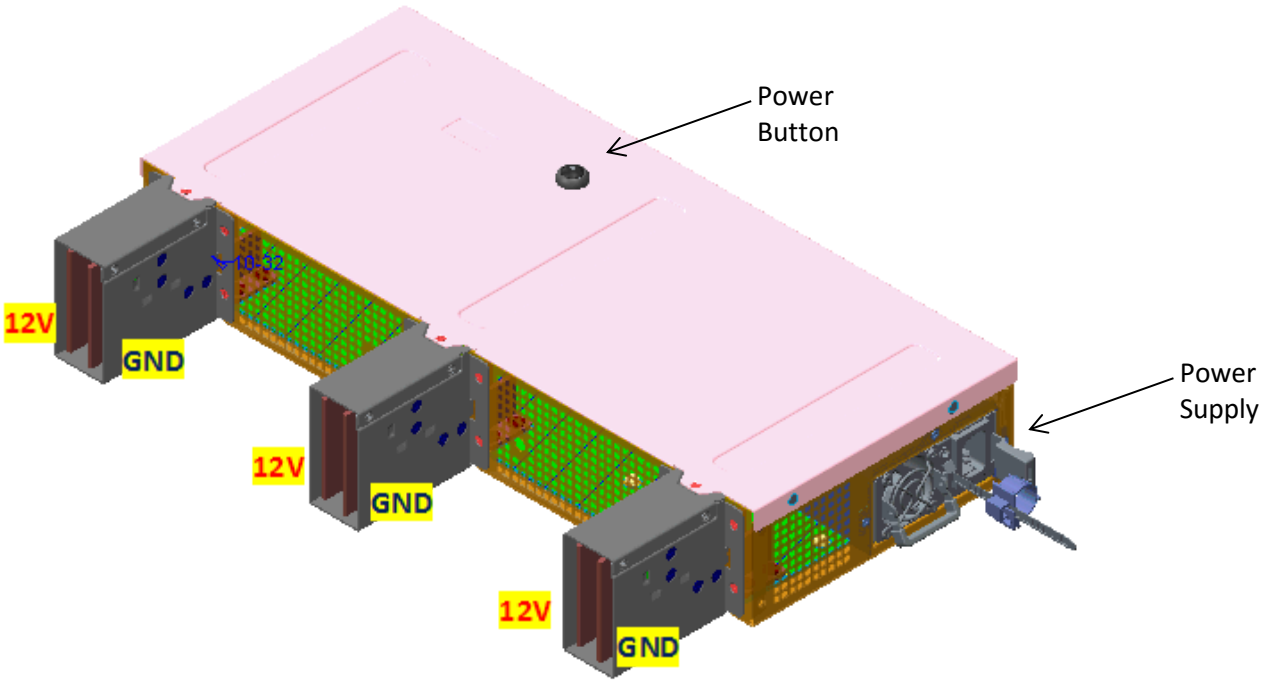

60mm
60mm
Standard Support BKT
Special Support BKT
12mm(0.25OU)

10. Lunch Box

10.1 Lunch Box Feature

Lunch box is a power fixture which supports OCP 1U or 2U sled to power on without Open Rack.

10.1.1 Top View



10.2 Power Supply Specification

The power supply used in Lunch Box is Chicony R1K6A008L.

10.2.1 Power Supply Overview

Form Factor		Custom"1U 86.3(W) x 197.6(D) x 39.3(H)"	
Power Factor Correction (PFC)		Active	
PSU Type		Server	
EMC Classification (Surge Immunity)		IEC 61000-4-5 : Common mode 2.0KV Differential mode 1.0KV phases 0, 90, 180, 270 deg.	
FCC Classification (Conducted and Radiated)		Class A	
Output Voltage	**Regulation Range**	**Minimum Load**	**Maximum Load**
+12V	11.4V – 12.6V	1 A	133 A
+12VSB	11.4V – 12.6V	0.1 A	2.5 A

AC Input Voltage Range

	Minimum	**Nominal**	**Maximum**
Input Voltage(High line)	180 V	200V~240V	264 V
Frequency	47 Hz	50/60 Hz	63 Hz
Vin(turn-on)	170 V		180 V
Vin(turn-off)	160 V		175 V
Current (Iin)			10A@200Vac
Input Power			1850W
Vin_OVP Behavior	If input voltage over 290Vac the power supply unit will shutdown and latch off, this latch shall be cleared by an AC cycling.		
Iin_OCP Behavior	If input current over 13.5A the power supply unit will shutdown and latch off, this latch shall be cleared by an AC cycling.		

11. Regulatory & Safety Requirements

Barreleye should conform to FCC Part 15, UL, CE, and other similar standards for EMI, Regulatory, and Safety requirements. The design files included in this contribution support common standards in the US, UK, EU, Hong Kong, and Australia.