Design Guide for
Open Rack Management Backplane Connection

Draft: September 30th, 2015

Version: 0.52

Authors:
Ethan Long, Intel
John He, Intel
Bill Carter, Intel
Terry Trausch, Intel
Alex Lee, Quanta
Alan Chang, Quanta

1 Contents

1 Contents 2

2 Revision History 3

3 Introduction 4

3.1 Goal 4

3.2 Confidentiality 4

3.3 Terms and Acronyms 4

4 Overview 5

4.1 MBP Connection in the Rack 5

4.2 MBP Connection on IT Equipment 6

4.3 MBP Mechanical Requirements 7

5 Rack MBP Connector 8

5.1 Connector Part Numbers 8

5.2 Connector Pin Out 8

6 Management Backplane Location in Open Rack 13

7 Appendices 16

7.1 Open Compute Mechanical Reference Documents 16

7.2 Design Collateral 16

7.3 Other Reference Materials 16

2 Revision History

Revision History			
Revision	**Revised Person**	**Date**	**Changes**
0.1	Ethan Long	07/31/2015	First Draft
0.2	Ethan Long/Alex Lee	8/7/2015	Second Draft
0.3	Ethan Long/Alex Lee	8/11/2015	3rd Draft
0.4	Ethan Long/Alex Lee	8/12/2015	4th Draft
0.5	Ethan Long/Alex Lee	8/18/2015	Added drawing images to Figures 6, 7, and 8.
0.52	Terry Trausch	9/30/2015	Updated descriptions in pin out table

3 Introduction

3.1 Goal

This document describes a mechanical implementation of a rack management backplane connection (MBP) in an Open Rack. IT equipment equipped with the appropriate connector could then mate to the rack MBP via a blind mate installation into the rack. This will supplement the existing Open Rack Standard v. 1.2 which does not address the use of a management backplane.

The benefits of a rack MBP include:

- Less cabling at the front of the rack, which also potentially reduces service costs
- Reduced network port count
- A physically isolated rack management network

3.2 Confidentiality

The rights and confidentiality of this document will be controlled by Open Compute Project.

3.3 Terms and Acronyms

Acronym	Description
MBP	Rack Management Backplane
Bus bar	A pair of main copper strips which provide 12V DC power for all components in rack
OCP Rack:	Same as Open Rack
OU Height	Open Compute Rack Unit Height, 1 OU Height = 48mm
Sled	IT equipment tray

4 Overview

4.1 MBP Connection in the Rack

Intel and Quanta recently collaborated on the development of a rack MBP for Open Compute. Intel has showcased hardware featuring this design in a demo rack shown at Intel Developer Forum 2015.

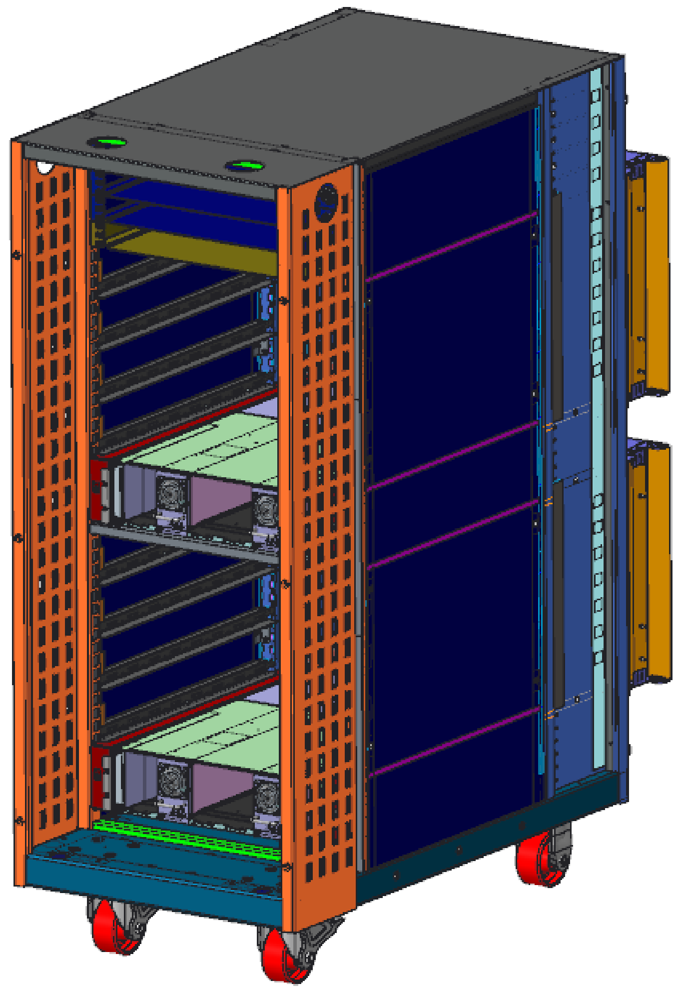

Figure 1 A demo rack shown at IDF 2015, the result of a joint effort between Intel and Quanta

The Open Rack Standard v 1.2 allows for use of a single central bus bar pair for distributing rack power, or for use of all three bus bar locations outlined in previous versions of the standard. Intel and Quanta chose to reduce the number of bus bars used, so that one of the side bus bar locations might be used for the rack management hardware. Figure 2 features a front view of a rack with a MBP located at the left hand bus bar location, with a central bus bar remaining for the delivery of rack power. The MBP does not exceed the width of the allocated bus bar zone at that location.

Figure 2 also defines the key mechanical interfaces of the backplane: The backplane connector and alignment holes. The backplane connector is suitable for blind-mate applications but is limited in how much connector misalignment it can tolerate. The alignment holes in the backplane module are intended to provide a means for coarse adjustment of the system-to-rack misalignment by accepting alignment pins from the installed IT equipment.

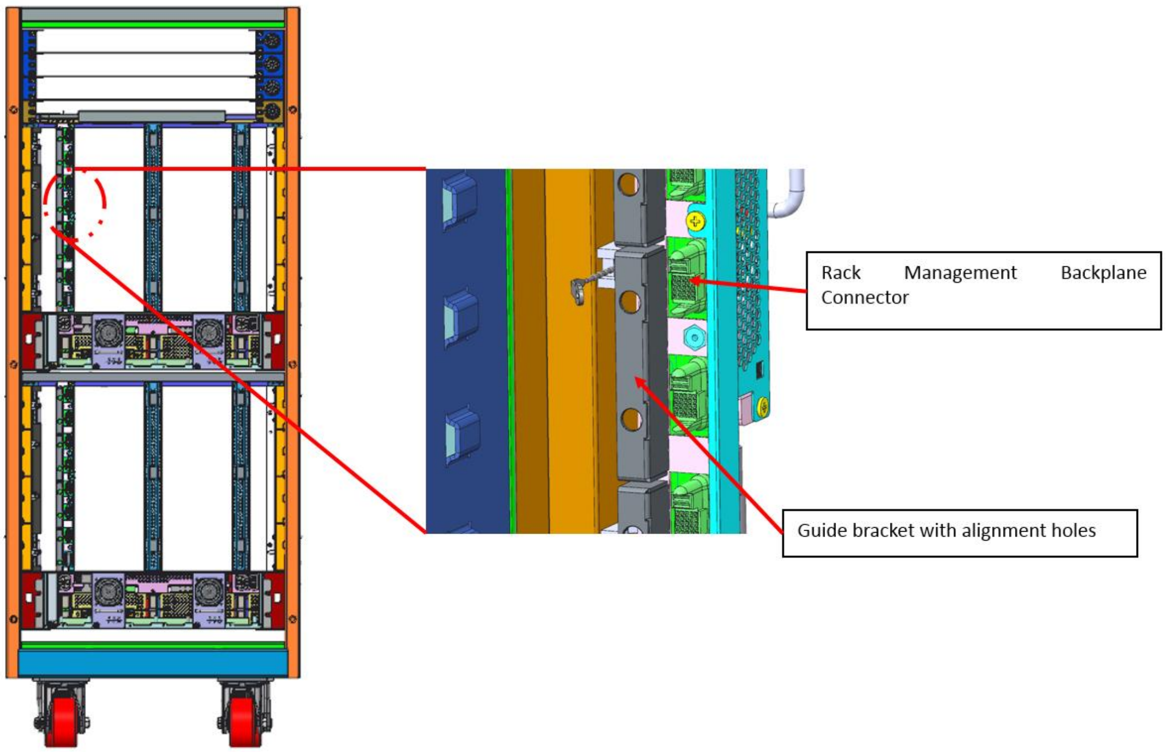

Figure 2 Front view of the Open Rack featuring a management backplane (MBP), in place of the left-hand bus bar.

4.2 MBP Connection on IT Equipment

The critical mechanical interfaces on compatible IT equipment include the MBP header and the coarse alignment pins (shown in Figure 3). It is recommended that the MBP interface at the rear of the IT equipment chassis incorporate a floating or compliant mounting to accommodate the significant chassis and rack tolerances without inhibiting mating to the backplane or imparting side loads onto the connectors.

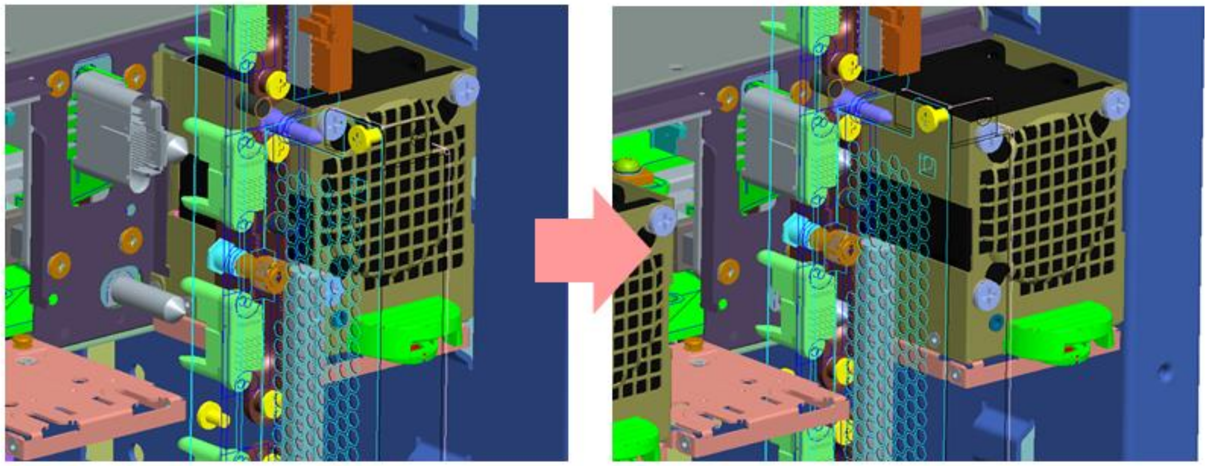

Figure 3 Example of a MBP interface on a 2OU server chassis, including a single MBP header mounted to an interposer card, and coarse alignment pins.

4.3 MBP Mechanical Requirements

The architecture and hardware of a rack MBP may vary depending on the application, but there are some key features that must remain consistent in order to ensure compatibility with properly equipped IT equipment of any “OU” height. This document will specify the following:

- A common connector for use in the MBP application
- A common pin out scheme for all MBP connectors
- Location of connector and alignment features in the Open Rack

5 Rack MBP Connector

5.1 Connector Part Numbers

The connectors chosen for the MBP interface are FCI PWR LoPro series headers and receptacles, with 2 power blades and 25 signal pins (see Figure 4):

IT Equipment-side Header: **FCI 10122460 - 011LF**

Rack-side Receptacle: **FCI 10121382-R02253SLF**

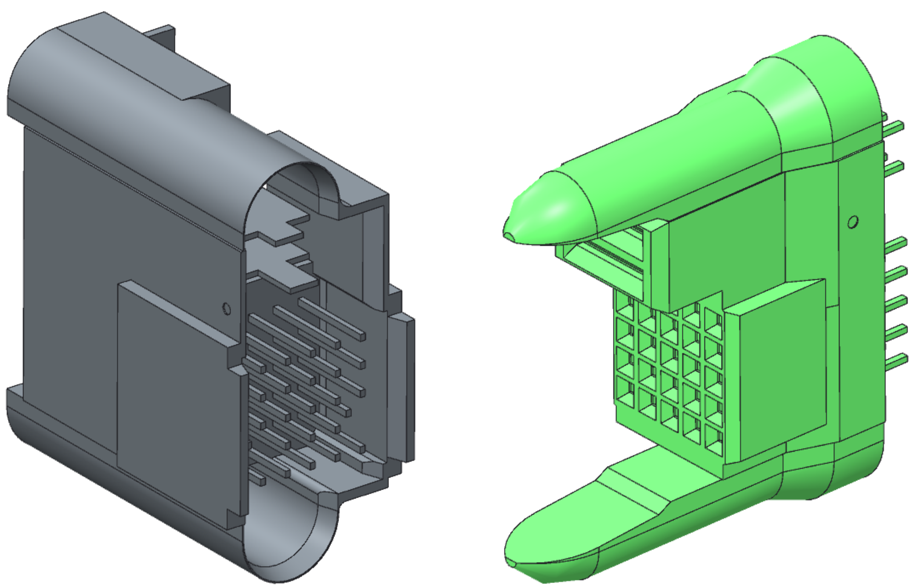

Figure 4 The Rack MBP connectors: IT Equipment MBP header (left), and rack MBP receptacle (right)

5.2 Connector Pin Out

The pin assignments for the connections are shown in Figure 5.

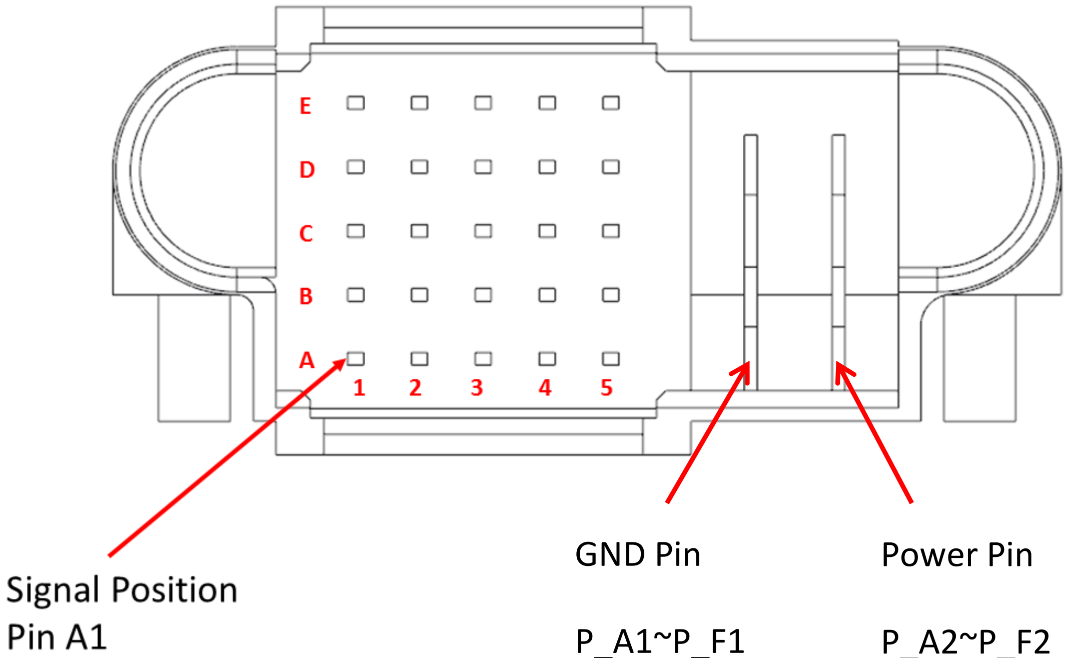

Figure 5 Signal pin number assignments shown on a front view of the MBP Header

Table 1, below, specifies the tray I/O to the MBP over the FCI MBP connectors. Inputs (including the label RX) are defined as inputs to the tray from the MBP and outputs (including the label TX) as outputs from the tray to the MBP.

Table 1 Tray Management Backplane Connector I/O

Name	Pin	Voltage	Type	Description
PSOC_INT_N	C4	3.3V	O	**Tray Interrupt**: Interrupt signal from the tray management subsystem to the MBP, active low.
TRAY_ID[2] **TRAY_ID[1]** **TRAY_ID[0]**	B2 C2 D2	3.3V	I	**Tray ID**: Signals from the management backplane to the tray indicating the location of the tray within the rack's management backplane segment. The largest MPB segment is limited to eight tray interfaces (one binary ID setting per OU).

Name	Pin	Voltage	Type	Description
THROTTLE_N	B5	3.3V	I	**Throttle, Power to the Tray Critical**: This signal indicates that the DC power supplied to the tray is in a critical state. The expected action for the tray is to quickly reduce power consumption by reducing IT equipment power consumption. The tray DC power is in a critical state when this signal is logic 0.
TRAY_RESET_N	C5	3.3V	I	**Tray, Management CPU Reset**: Signal indicating the tray management controller(s) should reset. This signal has two definitions. If management controllers see this signal active for less than four seconds, they should initiate a graceful reset. If management controllers are unable to provide a graceful/warm reset, this signal may be held for four seconds or more resulting in a forced/cold reset. This is intended to be the equivalent function of a reset button to the management controller. The reset is active when this signal is logic 0.
BP_PRSNT_N	A2	3.3V	I	**Backplane Present**: This signal indicates to the tray management controller that the tray is physically connected to a management backplane. The management backplane is present when this signal is logic 0.
TRAY_PRSNT_N	A4	3.3V	O	**Tray Present**: Signal indicating to the MBP that a tray is physically connected to that MBP interface. A tray is present when this signal is logic 0.
KX_TX_P, KX_TX_N	B1 A1	--	O	**Management Ethernet KX TX**: One high speed serial differential output pair complying with the IEEE Ethernet 1000Base-KX specification. This provides a tray management network interface.
KX_RX_P, KX_RX_N	E1 D1	--	I	**Management Ethernet KX RX**: One high speed serial differential input pair complying with the IEEE Ethernet 1000Base-KX specification. This provides a tray management network interface.
TRAY_IOEXP_INT_N	C3	3.3V	O	**Tray IO Expander Interrupt**: Interrupt generated to the MBP when vital status of any tray module changes. The interrupt is asserted when this signal is logic 0.
IPMB_CLK, **IPMB_DAT**	E3 D3	3.3V	I/O I/O	**IPMB Clock, Data**: An I2C bus supporting the IPMB protocol for management traffic destined to the tray that handles traffic between the management backplane (initiator) and the tray management controller (target).
UART_TX	D5	3.3V	O	**UART 1 TX**:

Name	Pin	Voltage	Type	Description
				A TTL level serial output from any module in the tray or from the tray management controller to the MBP. The default baud rate is 115K at 8 bits, no parity, and one stop bit. Recommend for trays that include a front panel and MBP interface for management console that this signal be a simple buffer copy of the UART TX to each location instead of using a multiplexer that enables and disables the interface to each location.
UART_RX	E5	3.3V	I	**UART 1 RX:** A TTL level serial input from the MBP to any module in the tray or to the tray management controller. The default baud rate is 115K at 8 bits, no parity, one stop bit. Recommend for trays that include a front panel and MBP interface for management console that this signal be a simple wire-or of signal from the front panel and the MBP to the management controller instead of using a multiplexer that enables and disables the interface to each location.
MP_HSC_EN_N	D4	3.3V	I	**Midplane HSC Enable**: A TTL level input signal that may control the power state of the tray management controller. This is intended to be the equivalent function of a power button to the management controller. The power is enabled when this signal is logic 0. **Note**: The signal does NOT necessarily control the power flow between the rack bus bar and the rest of the tray electronics. It is ONLY required to control of power to the tray management controller.
NC	A3 A5 B3 B4	--	--	**No Connect:** Reserved.

Name	Pin	Voltage	Type	Description
12V	P_A2 P_B2 P_C2 P_D2 P_E2 P_F2	12V	P	**12V Output Power:** This is power sourced from the tray to the management backplane exclusively for use by active devices that may exist on the management backplane. It may be used as a power source for fans. Recommend that this power be sourced through a diode so that one tray does not have current flow to another tray. The current limit is **22** Amps. This is power sourced from the tray (that connects to a power bus bar) to the management backplane. It is strongly recommended that this output power be diode isolated from the rest of the tray power so that one tray does not have a power path to another tray.
GND	C1 E2 E4 P_A1 P_B1 P_C1 P_D1 P_E1 P_F1	--	GND	**GND:** Ground. The current limit is **22** Amps.

6 Management Backplane Location in Open Rack

The rack MBP shall occupy the left-most bus bar location, and provide connections for IT equipment at 1OU increments. Figures 6, 7, and 8 define the location of key connector and alignment features with respect to existing Open Rack features.

Figure 6 Side View of MBP Connection in the Open Rack

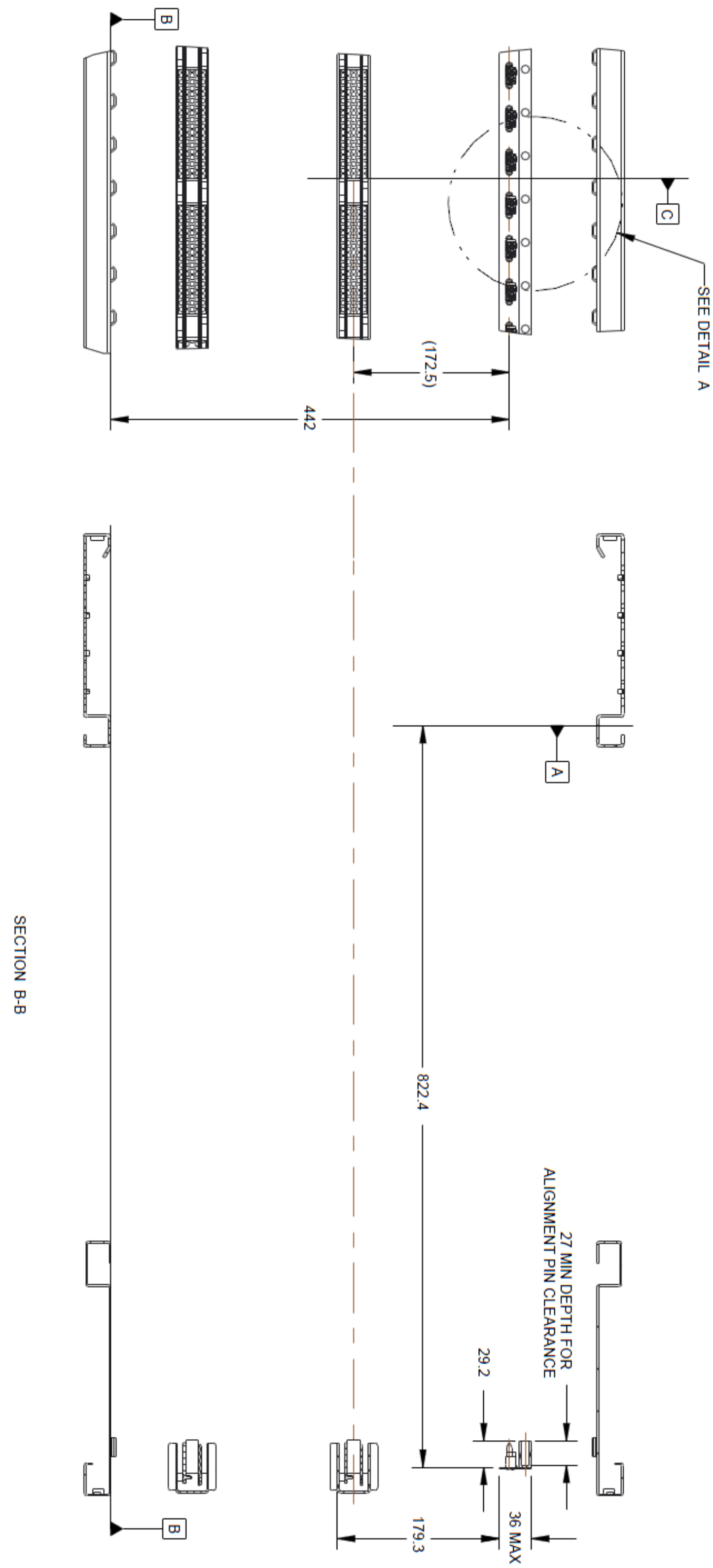

Figure 6 Front and Top Views of MBP Connection Features and Locations in the Open Rack

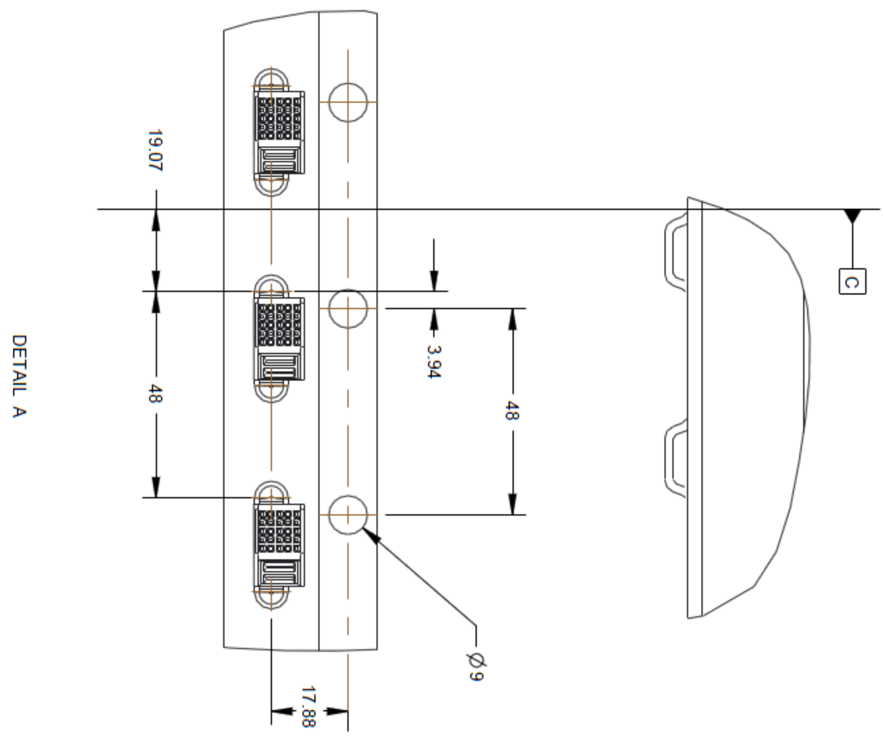

Figure 8 Front Detail View of MBP Connection

7 Appendices

7.1 Open Compute Mechanical Reference Documents

The following specifications are available on the Open Compute website:

- Open Rack Standard Preliminary v 1.2

(http://files.opencompute.org/oc/public.php?service=files&t=78595a633a8ddbdf57d41b3cc24a0803)

- Open Rack Design Guide v 1.1

(http://files.opencompute.org/oc/public.php?service=files&t=2db91c3317610dfcc383ba4dc720a186)

7.2 Design Collateral

Additional design collateral will be made available as needed.

7.3 Other Reference Materials

- I2C Specification –

(http:/www.nxp.com/documents/user_manual/UM10204.pdf)

- IEEE 802.3 Specification -
(http:/standards.ieee.org/about/get/802/802.3.html)