Open. Together. OCP SUMMIT

Fronthaul Gateway (FHG) and Converged Access Switch (CAS)

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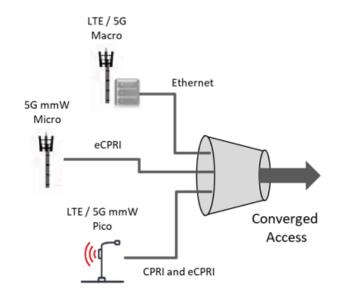




Fronthaul Gateway Introduction

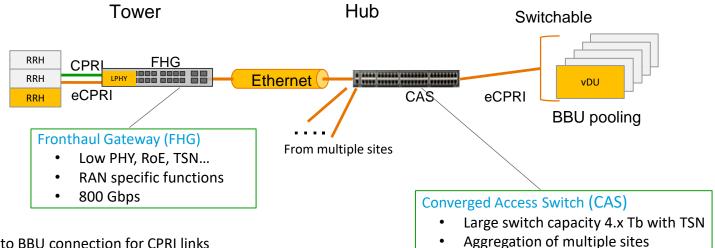
Objective: Consolidate multi-protocols into a common transport solution

- Interoperable without vendor lock-in
 - Standards based open interfaces
- Agility via modular, μs-latency, flexible architectures
 - Ethernet based aggregation
 - Converged protocols
- Customized model and policy driven automation
 - SDN controlled
- White Box Solution
 - Open Compute Project (OCP) design





Ethernet Solution for Fronthaul switchable/routeable



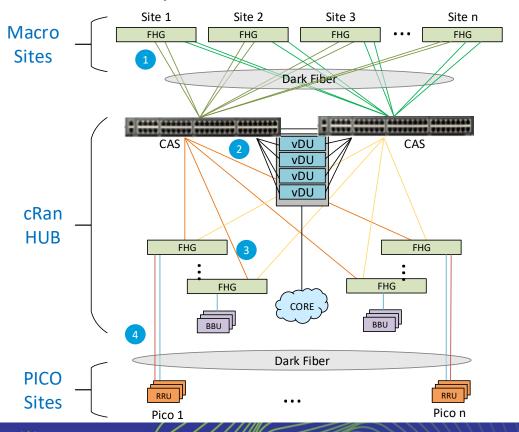
- Semi Dynamic TRP to BBU connection for CPRI links
 - Semi-Dynamic Switchable CPRI
- Dynamic TRP to BBU connection for eCPRI links
 - eCPRI switching
 - Dynamic load balancing
- Load balancing & BBU resource sharing
- Less exotic optics
- Fewer Fiber connections



Converged White Box

Switching and routing functions

FHG / CAS Transport Architecture



Architecture

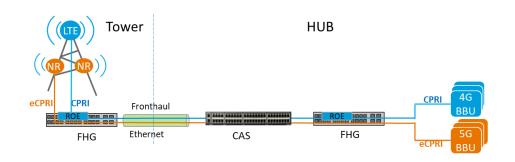
- 1 Point to Point Dark Fiber from Macro to CAS
- 2 eCPRI traffic switched to vDU
- 3 RoE traffic
- 4 PICO site transport CPRI over dark fiber to Hub



RoE vs Low PHY

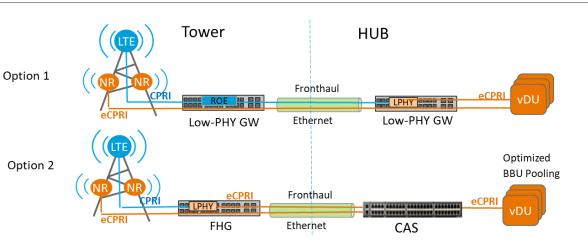
RoE

- CPRI over ethernet using 1914.3 standard
 - Tunneling Mode
 - Line Code Aware
 - Structure Aware



Low PHY

- Convert CPIR to eCPRI
- Target Architecture
- Functional 7.2x split from ORAN Standard





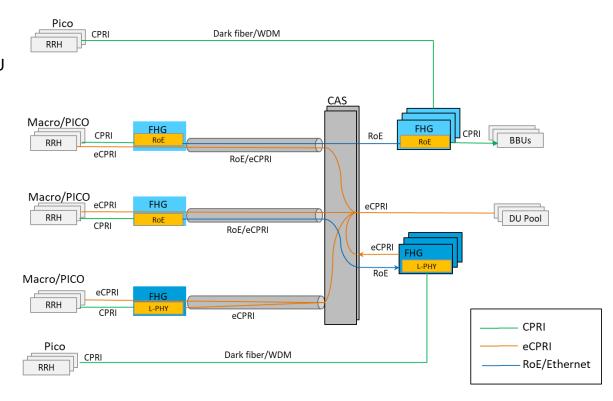
Deployment Scenarios

Target architecture

- CAS routing capability for efficient DU pooling, load balancing
- Multiple sites connected to CAS
- Dual CASs for resiliency
- L-PHY at hub (or site) to enable LTE pooling with NR

Combability to early step deployment

- Direct fiber to FHG to achieve routeability to BBUs
- Rack mount at site with RoE enables co-existence of LTE and NR





Fronthaul Gateway (FHG) & Converged Access Switch (CAS)

Form Factor	Deployment Environment	Port Capacity	Switching Bandwidth	Power	Cooling	Environmental	Size	LPHY	RoE	Synch	Preferred Silicon Options
FHG- Pico	Pole Mount Strand Mount	(6) X 10/25G CPRI/RoE/eCPRI (2) X 25G eCPRI (1) X 100G	200Gbps	AC (100 to 240 VAC) DC (-57 to -40VDC)	Passive	Outdoor Enclosure NEBS 3 OSP Class 4 -40C to + 70C Ambient IP65	10"x8"x4" < 35lbs	Optional (Desired)	Required	Boundary Clock	1) Monterey 2) Xilinx FPGA
FHG	Tower- Cabinet Hub Site MTSO/CO	(18) X 10/25G CPRI/ROE/eCPRI (6) X 25G eCPRI (4) X 100G	800Gbps	AC (100 to 240 VAC) DC (-57 to -40VDC)	Redundant Fans Front to back	Rack Mount: 19" NEBS 3 OSP Class 2 -40C to + 65C Ambient IP54 Front access	1-2 RU 19" Rack 11.8" Deep	Required	Required	Boundary Clock	1) Monterey 2) ASIC + FPGA Qumran MX Marvell Xilinx 3) FPGA
CAS	Hub Site MTSO/CO	(40) X 100G	4.8Tbps	AC (100 to 240 VAC) DC (-57 to -40VDC)	Redundant Fans Front to back	Rack Mount: 19" NEBS 3 OSP Class 2 -40C to + 65C Ambient IP54 Front access	2 RU 19" Rack	No	No	Edge Grand Master (S-Plane config 3)	1) Jericho 2C

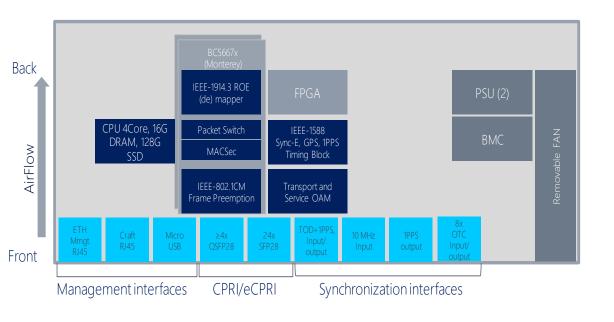


Required Standards Compliance

Standards Specification	FHG	CAS		
IEEE STD 802.1CM-2018 Time Sensitive Networking for Fronthaul, Profile A (support strict priority queuing) for Class 1 & 2 (CPRI and eCPRI) traffic				
EEE STD 802.1CM-2018 Time Sensitive Networking for Fronthaul – Profile B (support IEEE 802.1Qbu frame preemption and IEEE 802.3br Interspersed Express Traffic) on ports used as an NNI port whose date rate is not higher than 25Gbps.	Yes	No		
O-RAN WG4, Control, User and Synchronization Plane Specification, for Low PHY functionality and interfaces	Yes	No		
CPRI Specification v7.0 Common Public Radio Interface	Yes	No		
eCPRI specification v1.2, Common Public Radio Interface: eCPRI Interface Specification	Yes	Yes		
IEEE 1914.1 NGFI node processing time (latency) class A (< 2us for 25-100GbE).	Yes	No		
EEE 1914.3-2018 Radio over Ethernet Encapsulations and Mappings	Yes	No		
ITU-T G.8262.1 – Timing characteristics of enhanced synchronous Ethernet equipment slave clock	Yes	Yes		
ITU-T G.8273.2 Telecom Boundary Clock Class C	Yes	Yes		
ITU-T G.8273.4 – Timing characteristics of partial timing support telecom boundary clocks and telecom time slave clocks	Yes	No		
ITU-T G.8275.1 – Precision time protocol telecom profile for phase/time synchronization with full timing support from the network	Yes	Yes		
ITU-T G.8275.2 — Precision time protocol telecom profile for time/phase synchronization with partial timing support from the network	Yes	Yes		
Ethernet Service OAM (IEEE 802.1Q/ag, ITU-T Y.1731, MEF17/30.1/35.1)	Yes	Yes		



FHG: RoE ASIC + Low PHY FPGA (Optional)



RoE Configuration

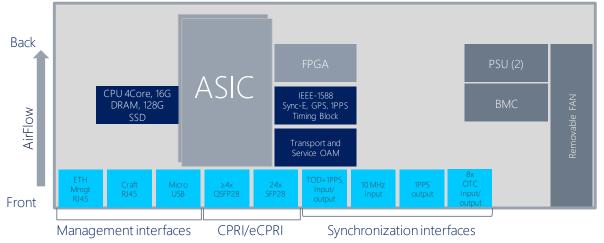
- Monterey (BCM5667x) for ROE
- · FPGA not required

Low PHY Configuration

- Monterey handling L2/L3 Functions
- Xlinx FPGA (KU15) supporting Low PHY



FHG: L2/L3 ASIC + FPGA



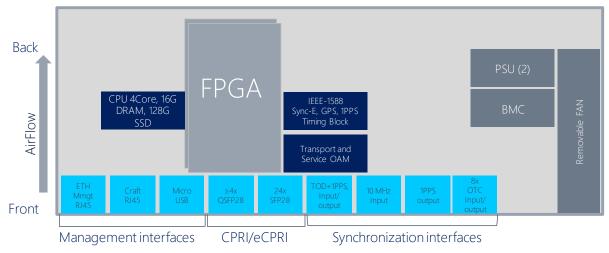
L2 / L3 ASIC

- Monterey (BCM5667x), Qumran MX, Marvell
- Handling L2/L3 Switching and Routing

FPGA

- Xlinx FPGA (KU15) supporting Low PHY
- Could be programmed to support:
 - RoE (IEEE 1914.3)
 - Low PHY

FHG: FPGA



FPGA

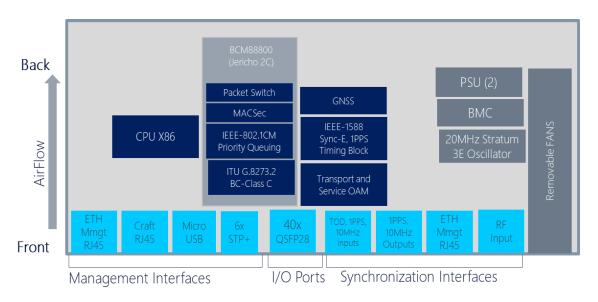
- Xlinx FPGA (KU15) supporting Low PHY
- Could be programmed to support:
 - RoE (IEEE 1914.3)
 - Low PHY

L2/L3 Switching

Could be accommodated by the CAS



CAS: Jericho 2C ASIC



Fronthaul Aggregation + Timing

- Jericho 2C (BCM88800)
- IEEE STD 802.1CM-2018 Time Sensitive Networking for Fronthaul, Profile A (support strict priority queuing) for Class 1 & 2 (CPRI and eCPRI) traffic
- ITU-T G.8273.2 Telecom Boundary Clock Class C
- ITU-T G.8262.1 Timing characteristics of enhanced synchronous ethernet equipment slave clock

