Bryce Canyon
Storage System Specification

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Version History

Version	Author	Comments
0.1	Jason Adrian	Initial version
0.2	Dominic Cheng	Many additions to prepare for initial spec submission
0.3	Jason Adrian Dominic Cheng	Updates for project kickoff
0.4	Jason Adrian Dominic Cheng	1st milestone release pre-EVT
0.5	Jason Adrian Dominic Cheng Austin Cousineau	EVT feature lock (v0.5.2)
0.6	Jason Adrian Dominic Cheng Austin Cousineau	Updated details for final EVT implementation
0.7	Jason Adrian Dominic Cheng Austin Cousineau Madhavan Ravi	OCP Specification Release

Commonly Used Terms

SCC	Storage Controller Card
IOM	I/O Module
DPB	Drive Plane Board
BMC	Baseboard Management Controller
IOC	I/O Controller
NIC	Network Interface Controller
TPM	Trusted Platform Module
OCP	Open Compute Platform
JBOD	Just a Bunch Of Disks
PCIe	PCI Express
SAS	Serial Attached SCSI
SATA	Serial ATA
HDD	Hard Disk Drive

1   Introduction

This document describes the hardware design of a Facebook storage system, hereinafter referred to as "Bryce Canyon." Bryce Canyon is a four OU-tall, single drawer storage chassis that contains up to 72 3.5" hard disk drives (HDDs), and two compute modules. This design leverages the Open Compute 1S Server Card, also known as "Mono Lake," and is Open Rack v2 (ORv2) compliant.

2   License

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3   System Architecture

3.1   System design and flexibility

The architectural intent behind the Bryce Canyon design is to fulfill Facebook's rotating storage needs with a flexible storage platform. The Bryce Canyon storage system is a 4OU system, with a majority of the components installed and serviced from the top. To enable this, there is an inner drawer design that fully extends the unit out of the rack. A mechanical overview is shown in Figure 1.

In its nominal configuration, the chassis supports up to 72 drives and two compute modules. Each compute module connects to a Storage Controller Card (SCC) that controls 36 drives, and is logically separate from the other compute module and its drives. The only common component shared by these two compute-storage groups is the incoming power (12V) delivered by the busbar clip. The chassis is designed such that the highest failure rate components (HDDs, compute modules, major ICs) are hot-swappable, without affecting the other host that resides in the same enclosure.

Several configurations of the chassis exist to satisfy various applications. The architecture is designed to maximize common components between configurations, and modularize the components that differ.
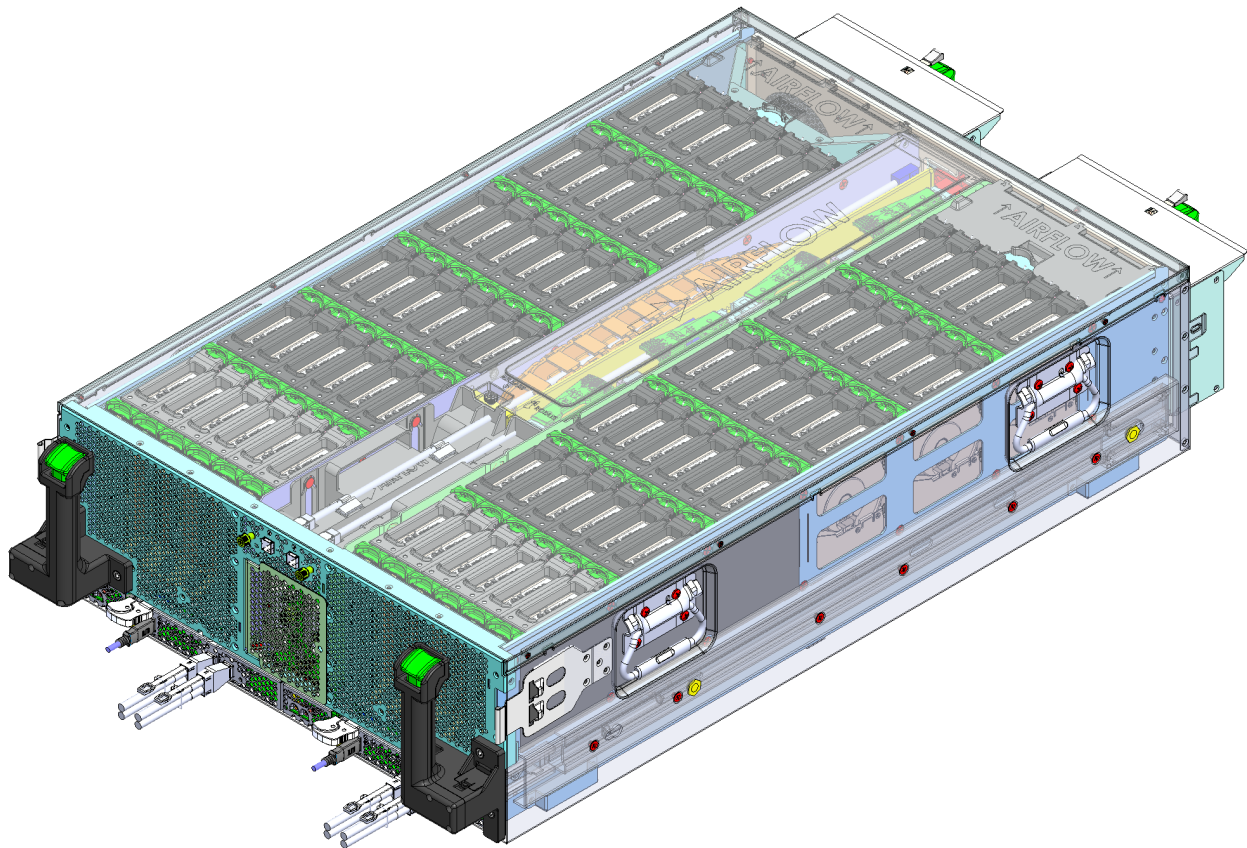
Figure 1. System overview

3.2   System components

This section outlines the major blocks that comprise the system.

3.2.1 Drive Plane Boards

The Drive Plane Boards (DPBs) sit at the base of the chassis. There are physically two Printed Circuit Boards (PCBs) that make up the drive plane board assembly, and these are connected via high speed connectors and an air baffle that create a single unit. The DPBs connect all of the boards in the system together, along with the drives, fans, etc. Its function is to support:

- Drives (up to 72)

- Fans (up to four)

- Drive power control (individual 5V/12V control to each slot)

- Sensors (temperature, drawer open)

- Incoming power (12V)

3.2.2 I/O Module

The I/O Module is a front-accessible card that provides key distinguishing features between the configurations. There are 16 lanes of PCIe Gen 3 routed to this board, with eight lanes going to the NIC mezzanine connector, and eight lanes going to the optional devices (M.2 slots or SAS IOC). An overview is shown in Figure 2, with all ports populated.
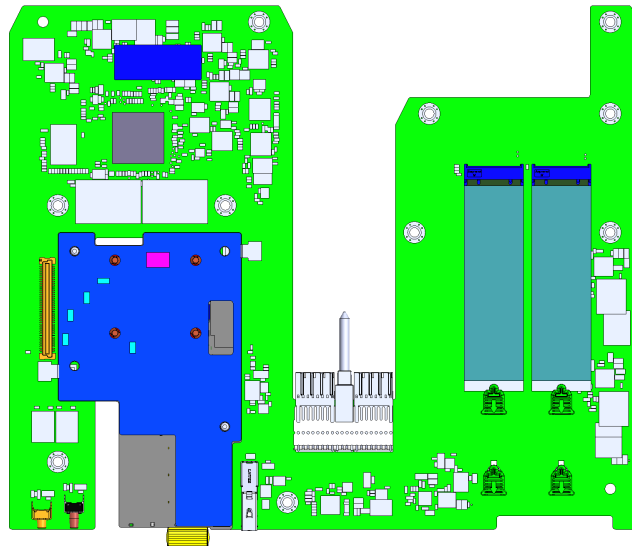
Figure 2. I/O Module overview

The I/O module supports:

- 25/50 Gb NIC

- BMC

- SAS IOC (optional)

- 2x M.2 PCIe x4 SSDs (optional)

The population of these components is dependent on the overall system configuration (see section 3.3).

3.2.3 Storage Controller Card

The Storage Controller Card is a top-accessible (with the drawer extended) module that contains the ICs needed to run SAS/SATA to the HDDs. Architecturally, this card could implement other protocols, but the initial version of the design will focus solely on SAS/SATA. The Storage Controller Card supports:

- SAS IOC

- SAS Expander

- SAS connection to the front bulkhead (to enable JBOD functionality)

The Storage Controller Card connects to the compute card via a PCIe Gen 3 x8 link.
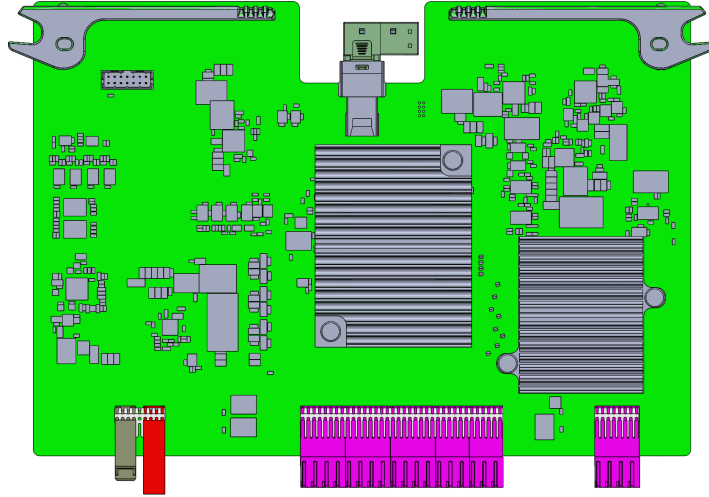
Figure 3. Storage Controller Card overview

3.3   System configurations

This section outlines the different possible configurations of the overall system. The Bryce Canyon platform covers all HDD storage, including Type IV, Type V, and Type VII rack types. There is a single base Bryce Canyon chassis, but a few FRUs that can be installed to create simple JBODs, or single and dual integrated storage servers. The table below shows the current configurations considered for production.

Table 1. Bryce Canyon system types and configurations

	Compute				Storage Controller Card				IO Module				Fans		Drives	
	# Monolake Cards	# CPU Core	Mem. Capacity	Mem. Config	# SCC	SCC Type	Expander	IOC	# IOM	OCP NIC	SAS IOC	M.2	# Fans	Fan size	# Drives	# Drives Spun up
Type IV JBOD	0				2	JBOD	Yes	No	0				4	92mm	72	72
Type V 2x 1:36	2	16	64GB	2x 32GB	2	INT	Yes	Yes	2	25Gb		2	4	92mm	72	72
Type VII Headnode	1	16	128GB	4x 32GB	2	1x INT, 1x JBOD	Yes	*Yes	1	25Gb	1		4	92mm	66	~5
Type VII JBOD	0				2	JBOD	Yes	No	0				2	92mm	72	~5

3.3.1 Dual Storage Server

The nominal configuration as described thus far is the Dual Storage Server. This configuration is used for Type V racks. The block diagram for this configuration is shown in Figure 4.
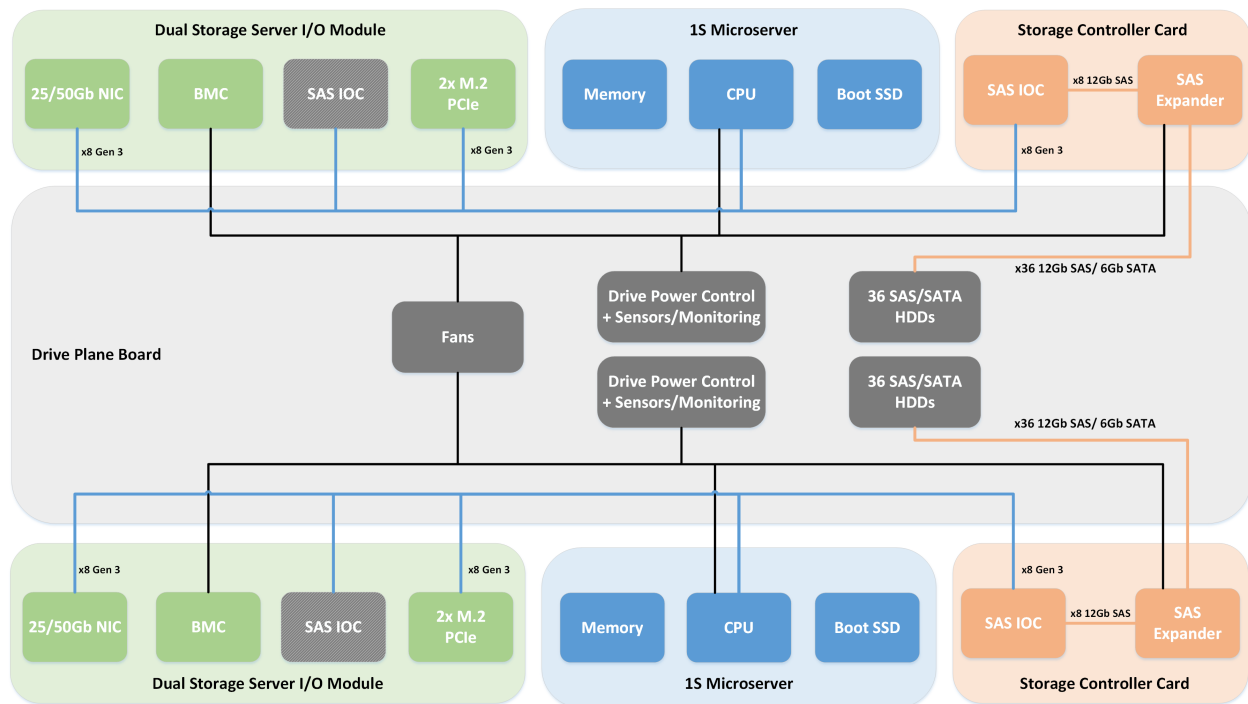
Figure 4. Dual Storage Server system configuration block diagram

The only external connection used in this configuration is a single 25/50 Gb Ethernet link. The SAS IOC on the I/O Module is not populated, as all drives are directly connected within the system. Instead, the SAS IOC present on the Storage Controller Card is used to connect to the SAS expander, which attaches the 36 drives in the system.

3.3.2 Single Storage Server

The configuration is intended for applications that use a lower compute-to-storage ratio. The block diagram is shown in Figure 5. This configuration serves as the head-node for a cold storage configuration, with several JBODs connected downstream to increase the number of drives behind a single node. To connect all 72 drives slots within the chassis, an internal MiniSAS HD connector on both SCCs can be connected via an x4 cable.
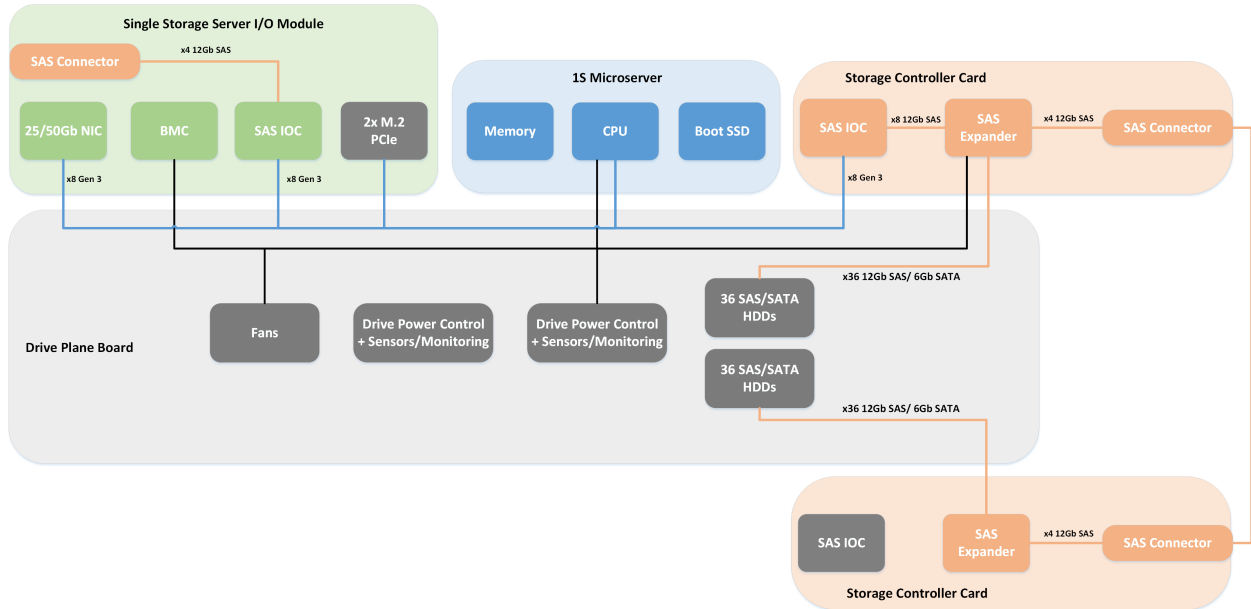
Figure 5. Single Storage Server system configuration block diagram

3.3.3 JBOD

The JBOD configuration allows for an external compute module to connect to Bryce Canyon. This compute module is cabled to the system via a SAS connector that is exposed on the front panel of the chassis.

The Storage Controller Card, in this configuration, does not have a SAS IOC populated. The I/O Modules are also not installed; the fan control is coordinated by the SAS expander in lieu of the IOM BMC.
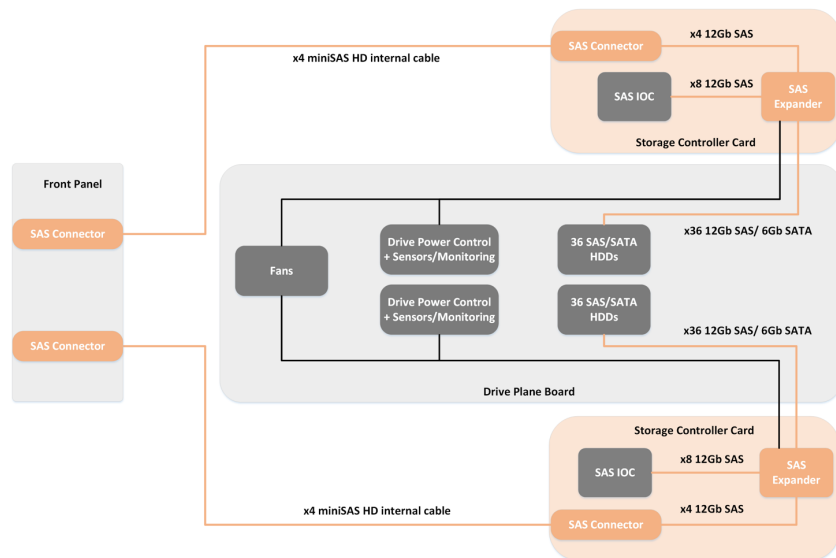
Figure 6. JBOD system configuration block diagram

3.4 Systems management overview

The system is managed by two to four controllers (two BMCs and two expanders). Each of these controllers (referred to as "peers" below) have ownership of part of the chassis. Interactions among these peers are limited to:

1. Insertion detection of all peers, and Mono Lake;
2. Heartbeat of all peers;
3. Access to master hot swap controller (through multi-master I2C);
4. Access to TACH sensor (through multi-master I2C);
5. Fan speed control through PWM comparators.

At a high level, the BMCs own sensors on the IOM, on Mono Lake, and own the IOC on SCC; the expanders own other sensors in the chassis (including HDD SMART temperature). The BMCs primarily generate PWM for fans in the middle; while the expanders generate PWM for all fans (one PWM for two fans in the middle, another PWM for two fans on the sides); however, the BMC does have the capability to drive fans on the sides if need be. For more information on fan control, see section 6.2.9.

Each peer in the system monitors insertion and heartbeat of other peers. If an expected peer is not presented or does not generate proper PWM, the firmware should increase fan PWM to a predefined value (e.g., 100%).

I2C device and sensor ownership information (per-configuration) can be found in Table 6.

3.4.1 Dual Storage Server

In the Dual Storage Server configuration, the two BMCs handle the majority of systems management for the box. Each BMC manages a connected compute server, the SCC, drives, and power and system signaling independently of the other side of the box.

The SAS Expanders handle communication with individual drives, as well as monitor certain sensors and affect indicators throughout the box. Fan control and thermal regulation is controlled mutually from each chip (see section 6.2.9). There are some shared resources as well, such as the SCC FRUID and temperature sensors on the DPB; however, while both the BMC and expander can initiate requests to these devices over I2C multi-master, the primary intent is for the BMC to request this information via IPMB to the SAS Expander on the SCC.

3.4.2 Single Storage Server

In the Single Storage Server configuration, a single BMC controls the majority of systems management on its own side of the box, while the opposite-side SCC manages the opposite side of the box (its side).

3.4.3 JBOD

In the JBOD configuration, the SAS Expanders on the Storage Controller Card handle all of the systems management for the box; this includes sensors on the SCCs and DPBs, all indicators within the box, and thermal (Fan) control.

4 System Interaction and Serviceability

4.1 Labeling of logical domains

As described in Section 10, the drive domains are physically divided between the front and rear of the chassis via the two Drive Plane Boards; however, as shown in Figure 4. Dual Storage Server system configuration block diagram, the drives, Compute Modules, and I/O Modules are separated in a left/right fashion. Consequently, the correct logical division of the two domains must be made clear through highly-visible labeling. An example of this is shown below, in a diagram of how Mylar labels can be used to clarify the FRU and drive location.

One important design point to make drive swaps intuitive is to implement light pipes near the drives to bring the light from the activity/fault LEDs to a visible location. If the labels are metal-backed or are otherwise normally opaque, but clear over the light pipe area, this will help contain the light. Also, the drive numbers can also be opaque, essentially creating a backlit number for the drive slots. The shape pointing to the drive should be a trapezoid instead of a triangle to allow the largest space to put the drive numbers for clear identification of the drive slot, while at the same time making the direction of the indicator obvious; a close-up of the drives showing these indicators is shown in Figure 8.
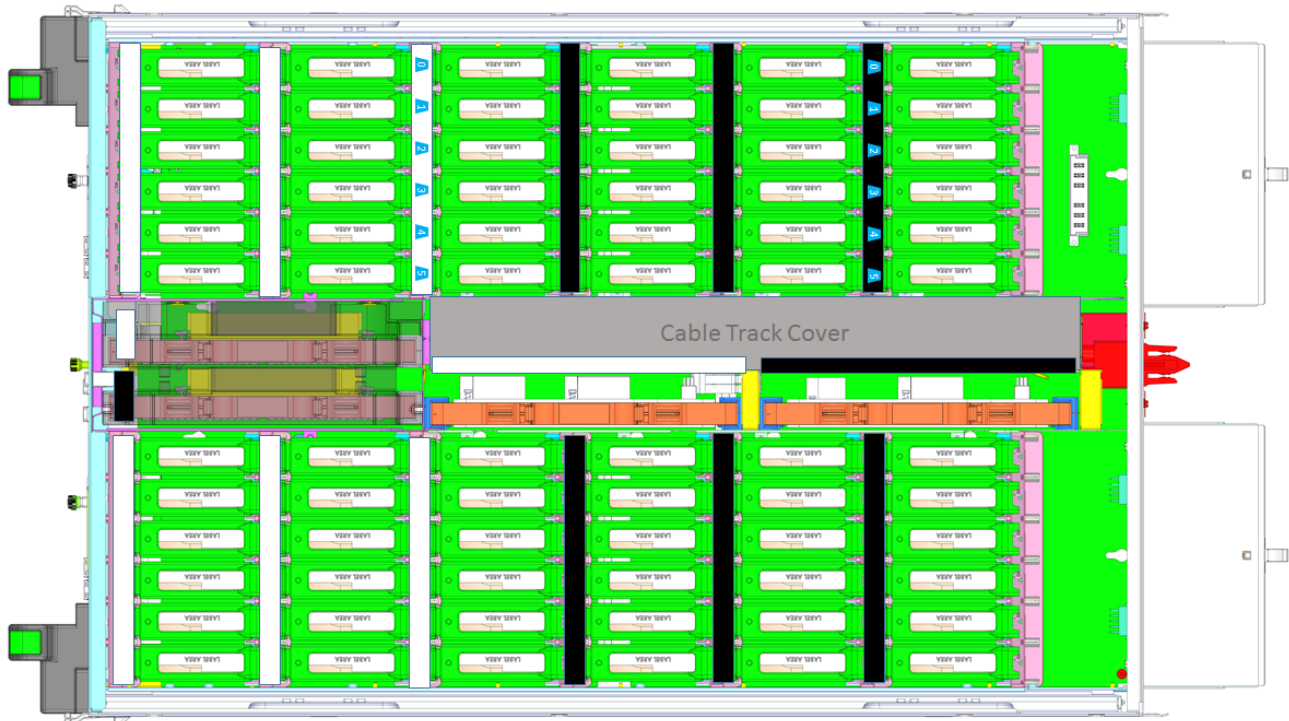
Figure 7. Labeling of logical domains
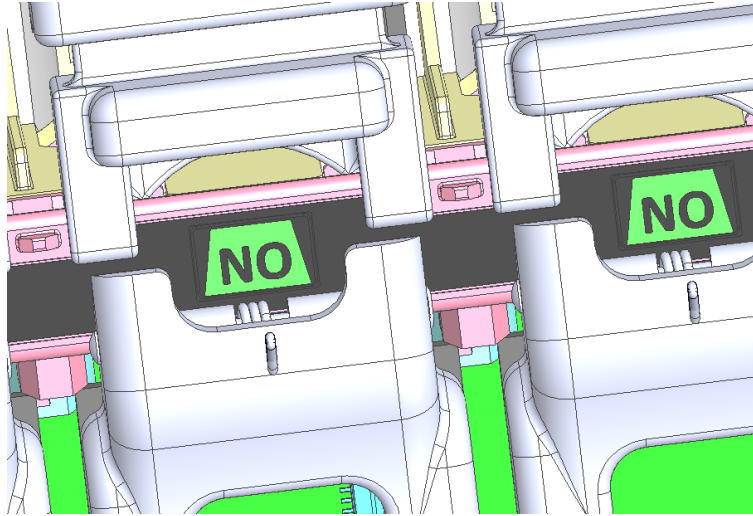
Figure 8. Drive numbering label

4.2   LEDs and buttons

This section gives an overview of the various LEDs and buttons within Bryce Canyon. A summary of the user interface is shown in Figure 9.
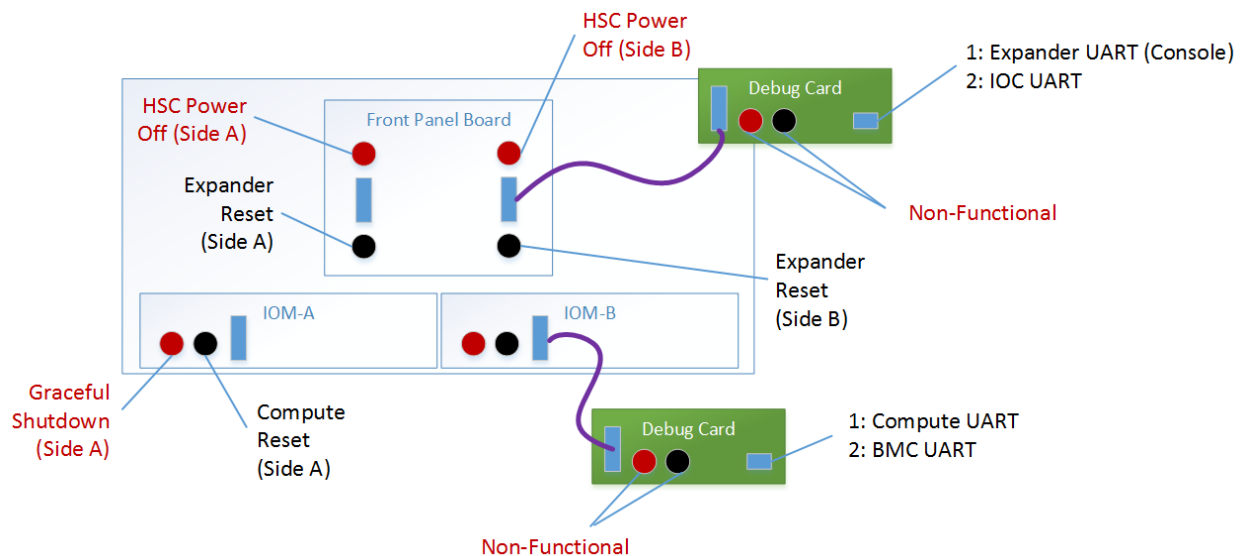
Figure 9. User interface diagram

4.2.1   Front Panel Buttons and LEDs

In all chassis configurations, there will be a power button, reset button, system power LED, system fault LED, and a USB debug port. There will be two instantiations of the front panel, one for each of the two logical systems in the physical chassis. Due to space limitations on the drive plane board, these buttons and LEDs will be located on front panel module as shown below.
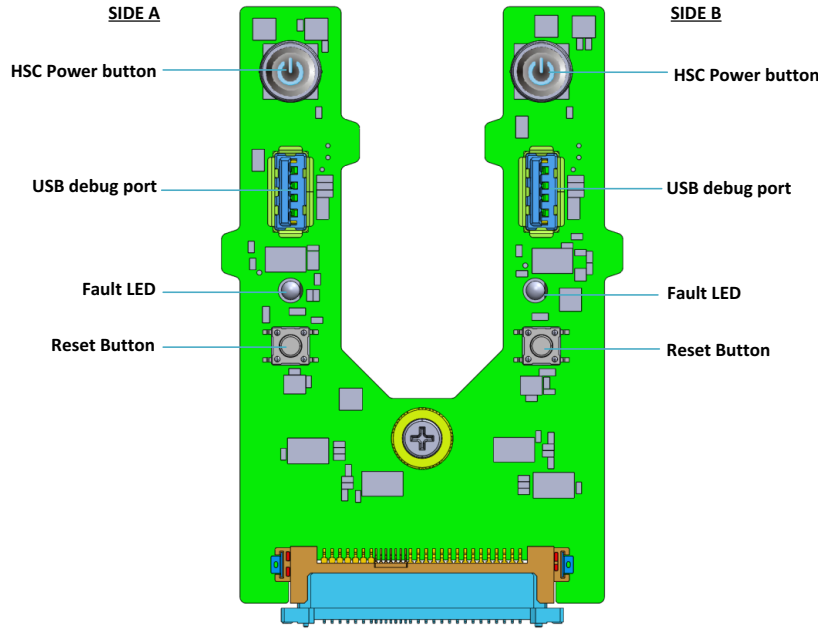
Figure 10. Front panel LEDs and buttons

4.2.1.1   Power Button

The functionality of the power button is to physically turn on/off the hot swap controller that gates the power to one server subsystem of the Bryce Canyon system. This is used for service events, such as the server replacement or SCC replacement, to allow the technician to power off the server subsystem to perform this action. The button shall be a push-on/push-off type switch, so that the state is persistent until an operator pushes the button again. The system should ship with this button in the "ON" position.

4.2.1.2   Power LED

In order to minimize the space needed, and to make servicing the system intuitive, the system power LED is desired to be integrated into the power button. If this is not possible, a separate button and LED is acceptable. The LED shall be blue. The LED will have the ability to be controlled by both the SCC and the IOM's BMC to allow blink patterns for system identification. A blink pattern of 1s on, 1s off will indicate unit identification.

4.2.1.3   Reset Button

The reset button shall be a momentary on pushbutton switch with a black plunger. This reset button is routed to the SCC card. The system level reset (for the storage server configuration) is accomplished by the reset button on the IOM as described in more detail below.

4.2.1.4   Fault LED

The system fault LED informs the user of a problem with the system. This can be driven by either the SCC (for JBOD configurations) or the BMC (for the storage server configuration). The fault LED shall be a yellow LED.

4.2.1.5   USB Debug Port

The USB debug port on the front panel is used for the debug signals only. The USB 2.0 portion is not connected, but the USB 3.0 remapped signals enable the use of the debug card.

4.2.2 I/O Module Buttons and LEDs
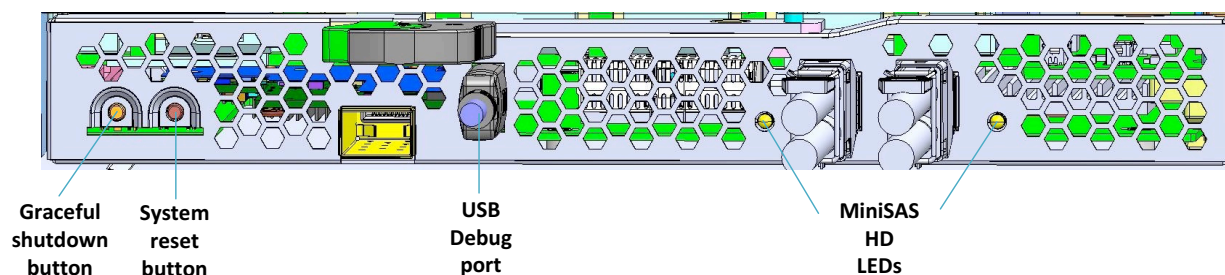
Figure 11: IOM LEDs and Buttons

4.2.2.1 *Graceful Power Down Button*

There is a pushbutton on the IOM that signals the BMC to perform a graceful shutdown. The length of button press is currently TBD.

4.2.2.2 *System Reset Button*

There is a reset button on the IO Module that allows the operator to reset the system if required. This signal is routed to the BMC, which will control the reset for the system.

4.2.2.3 *USB Debug Port*

The USB debug port serves two purposes. The USB 2.0 pins route to a USB hub located on the IOM, and the five pins normally used for USB 3.0 are repurposed for the debug signaling.

4.2.2.4 *MiniSAS HD LEDs*

There is a single blue/yellow LED per MiniSAS HD port. The behavior of the LED is described below:

Solid Blue – All four lanes up and linked at 12Gb SAS

Solid yellow – Fault/warning

Off – No cable present

4.2.3 Drive LED behaviors

Each drive slot has single light pipe with an LED indication as to the state of the drives. The behaviors are described below, and summarized in a table to identify the various states:

Drive powered off/ not installed – No LED illuminated

Drive powered on and PHY linked to Storage Controller Card – Blue LED illuminated

Drive fault – Yellow LED illuminated

Drive identify – Blinking yellow LED. If a drive is powered on, this behavior will show the yellow LED illuminated for one second, blue LED illuminated for one second, repeating. If the drive is powered off, this would appear as yellow LED on for one second, off for one second, repeating.

The following table identifies different conditions within the box, and the respective behaviors of the LEDs.

Table 2. Drive LED behaviors

Status	LED Indication	Blue (ACT)	Yellow (Fault)	Mechanical	Expander code
No Drive	No	Off	Off	Empty Slot	No
Drive Not Seated (or backwards)	No	Off	Off	Latch Won't Close	No
Drive Powered On, no Link	Yes	Blink (1s on, 1s off)	Off		Yes

Drive Powered On, SAS/SATA Link established	Yes	On	Off		Yes
Drive Faulted	Yes	Off	On		Yes
Drive Identify (Drive Off / Not Present)	Yes	Off	Blink (1s on, 1s off)		Yes
Drive Identify (Drive On)	Yes	Blink (1s on, 1s off)	Blink (1s on, 1s off)		Yes

For more information regarding drive LED behaviors, see Section 14.1.

4.2.4   Fan Module LEDs

The fan modules have LED indications to indicate the health of the fans.

Blue – (TBD if this is power to fan, or actively controlled via SCC)

Yellow – When illuminated, indicates a fan fault.

4.3   Service operations

The Bryce Canyon system provides hot swap controllers on the power rails, but the system will not support hot swap of the SCC, IOM, or compute module due to PCIe surprise removal/insertion and the issues. This functionality can be added later if needed, as the electrical subsystem supports this. The drive slots, however, all support hot plug.

4.3.1   Drive replacement

The drives are all hot pluggable, and it is up to the service flow if the drives are spun down or not before removal. To replace a drive, the latch should be opened, and pulled up to remove the drive from the system. By pulling up on the latch once it is opened to a vertical position, the drive is partially removed from the system to allow easy access to grab the drive. A new drive can then be inserted, and then the latch can be closed to lock the drive into place.

4.3.2   SCC replacement

To replace the SCC, the A/B domain should be shut down via the power button on the front panel module. The power button is illuminated blue while the power is on, and turns off when the power is off to that portion of the system. The SCC can then be removed, a new module installed, and then the power button can be pressed to turn the system back on.

4.3.3   IOM replacement

To replace the IOM, the A/B domain should be shut down via the power button on the front panel module. The power button is illuminated blue while the power is on, and turns off when the power is off to that portion of the system. The IOM can then be removed, a new IOM module installed. If the fault was with the IOM, and the NIC and/or M.2s are OK, they can be transferred to the new IOM. The power button can be pressed to turn the system back on.

4.3.4   NIC replacement

The NIC is installed as a module into the IOM, and thus requires the system to be shut down following the IOM instructions above. To replace the NIC, the IOM is removed from the system, the NIC replaced, and the IOM assembly is then reinstalled into the system.

4.3.5   Compute replacement

To replace the compute module, the A/B domain should be shut down via the power button on the front panel module. The power button is illuminated blue while the power is on, and turns off when the power is off to that portion of the system. The compute module can then be removed, a new module installed, and then the power button can be pressed to turn the system back on. The SSD and DIMMS are FRUs, and can be replaced separately if they are identified as failed instead of the compute module itself.

4.3.6 Fan module replacement

The fan modules are hot-swappable from the rear of the chassis. In most configurations the fan module consists of two fans integrated into an easy to service module. In the cold storage configuration there may only be a single fan contained in the module. It is expected that removing and replacing a fan will be a several-second operation. However, if the fan is removed for too long, the remaining fan module may increase its fan speeds in an effort to keep the system within its thermal operating limits. The fan module is considered the FRU, and will either be replaced as such, or the individual fans can be replaced individually at a later time.

4.3.7 Drive plane board replacement

There are two drive plane boards in the system, but these are always replaced as a single unit. For all intents and purposes, these should be considered as a single FRU that is only logically divided due to manufacturing limitations. Replacement of the drive plane board should be a rare event, but in the case of replacement the following procedure should be followed:

1) Power down both sides of the system via the power buttons on the front panel
2) Unplug the cables on the front of the system
3) Go to the rear of the machine and remove the fan modules
4) Pull the drawer out to its fully extended position
5) On the back left of the system, just in front of the fans, unplug the power cable connector, which is a squeeze to release connector (depress the sides where there are latch features)
6) Remove the SCCs, IOMs, and compute modules
7) Unlatch and lift up on all of the drives, which will hold them up and away from the DPB
8) Unscrew two thumb screws on the bottom of the DPB assembly, and slide the DPB towards the front of the chassis and down to remove the board.
9) Install the new DPB assembly by aligning the guide features in the back, and sliding back and lifting up
10) Follow steps 1-7 in the reverse order to put all of the components back into the system.

5 Rack Types

The Bryce Canyon platform will be used in a few configurations, to meet the needs of several rack types, as outlined in the following sections.

5.1 Type IV

The Type IV rack is designed for compute-heavy applications, and will utilize a Leopard 2S server with a hardware RAID card that connects to a Bryce Canyon JBOD. The Bryce Canyon system will present two JBODs, each with 36 drives connected to two different servers.
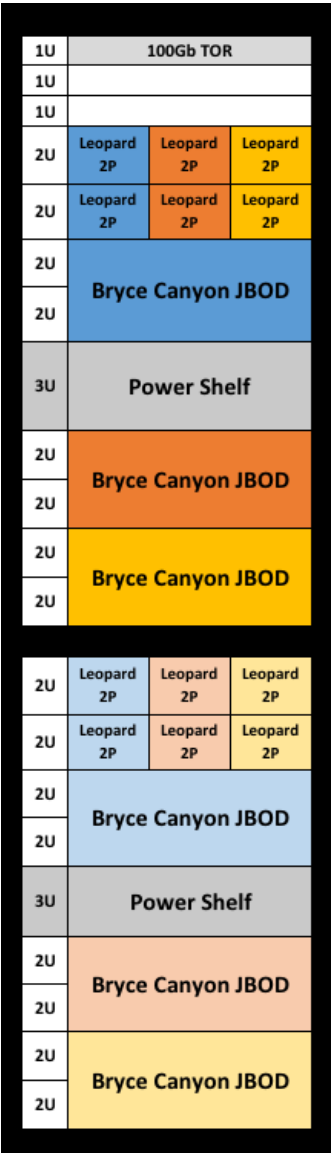
Figure 12. Type IV Rack Configuration
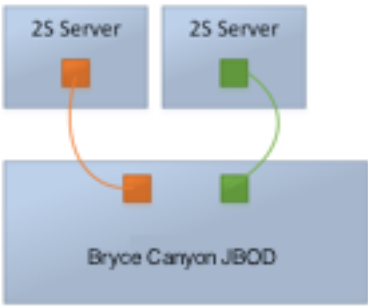
Figure 13. Type IV cabling diagram

The cabling configuration between a compute module and its corresponding Bryce Canyon JBOD is shown above. This will be a standard MiniSAS to MiniSAS HD cable (if used with a 6Gb HBA/RAID card in the server), or a MiniSAS HD to MiniSAS HD cable (if used with a 12Gb-capable HBA/RAID card).

5.2 Type V

The Type V rack configuration is expected to be the highest volume configuration of Bryce Canyon. In this configuration, there will be two storage servers with 36 drives each inside the Bryce Canyon chassis. The compute portion is an integrated 1S server.

1U	100 Gb TOR
1U	
1U	
2U 2U	Bryce Canyon - 2x Mono Lake (8 core)
2U 2U	Bryce Canyon - 2x Mono Lake (8 core)
3U	Power Shelf
2U 2U	Bryce Canyon - 2x Mono Lake (8 core)
2U 2U	Bryce Canyon - 2x Mono Lake (8 core)
2U 2U	Bryce Canyon - 2x Mono Lake (8 core)
2U 2U	Bryce Canyon - 2x Mono Lake (8 core)
3U	Power Shelf
2U 2U	Bryce Canyon - 2x Mono Lake (8 core)
2U 2U	Bryce Canyon - 2x Mono Lake (8 core)
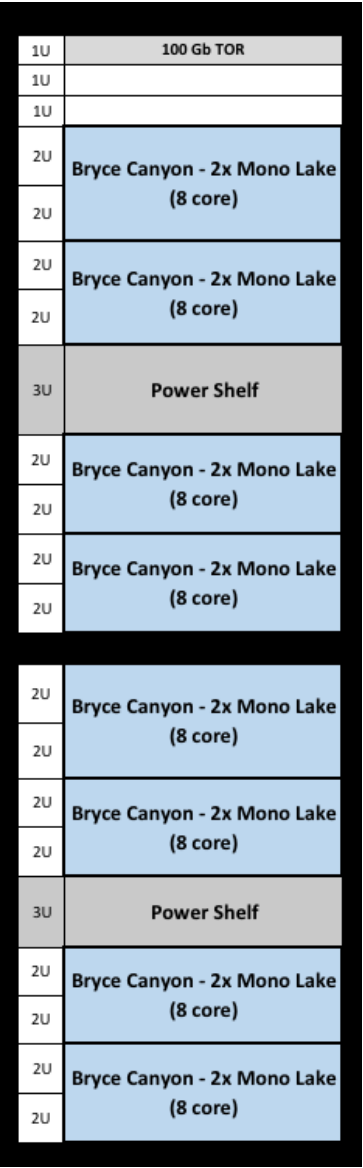
Figure 14. Type V Rack Configuration

5.3 Type VII

The Type VII rack configuration is designed for cold storage applications. There will be two different Bryce Canyon configurations populated within a rack of this type. There will be a main Bryce Canyon unit with compute, and two Bryce Canyon JBODs connected behind this, for a total of 210 drives in each functional system. In the base unit, there will be a single 1S server that connects to all drives in the base chassis. One unique configuration requirement here is that only 66 of the 72 drives are populated. This is to give the overall 210 drives needed, with 66 in the base unit, and 144 in the two JBODs, for a total of 210 drives.

1U	100 Gb TOR
1U	
2U	Bryce Canyon - 1 x Mono Lake (16 Core)
2U	
2U	Bryce Canyon - JBOD
2U	
2U	Bryce Canyon - JBOD
2U	
2U	Bryce Canyon - 1 x Mono Lake (16 Core)
2U	
2U	Bryce Canyon - JBOD
2U	
2U	Bryce Canyon - JBOD
2U	
2U	Bryce Canyon - 1 x Mono Lake (16 Core)
2U	
3U	Power Shelf
2U	Bryce Canyon - JBOD
2U	
2U	Bryce Canyon - JBOD
2U	
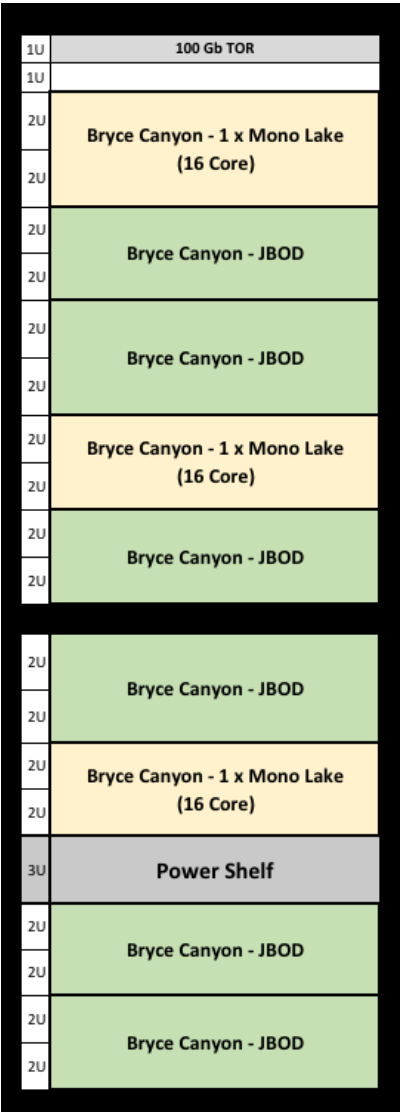
Figure 15. Type VII Rack Configuration
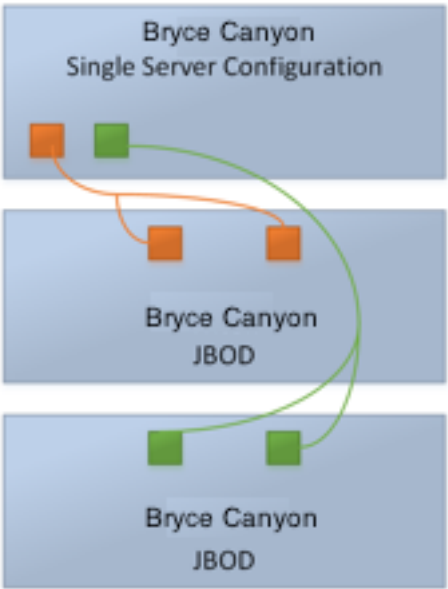
Figure 16. Type VII cabling diagram

The cabling between a Bryce Canyon with 1x Mono Lake and its two corresponding Bryce Canyon JBODs is shown above. A custom Y-cable will be used to connect the Single Server Configuration to the JBODs, such that the JBOD internal cabling will be the same between Type IV and Type VII.

6 Electrical Design

This section details the electrical design of the major system boards, the systems management topology, and other system details.

6.1 PCIe topology

There are 24 PCIe Gen 3 lanes, which originate from the compute server slot, that connect to devices on the SCC and IOM. There will be two potential configurations for the PCIe topology, depending on which IOM is installed. In all cases, however, an x8 will go to the SCC, and an x16 will go to the IOM. In one configuration of the IOM, x8 will go to the OCP Mezz slot, and the other x8 to a SAS IOC. In the second configuration, x8 will go to the OCP Mezz slot, and there will be two x4s connected to M.2 connectors.

6.1.1 PCIe Lane Mapping

Port configuration from the Broadwell-DE SoC:
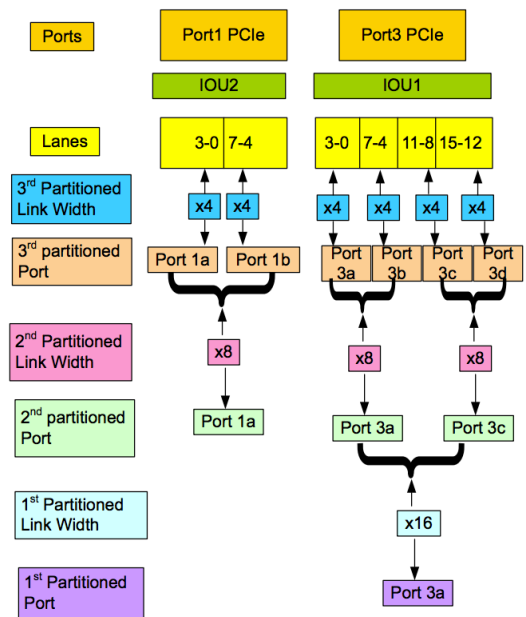
Figure 17: PCIe Port Configuration (Broadwell-DE)

The following table represents the different PCIe ports across various configurations of the system.

Table 3. PCIe ports and configurations

1S Port Spec	0	1	2	3	4	5
Intel Root Complex	IOU1				IOU2	
Lanes	3-0	7-4	11-8	15-12	3-0	7-4
Intel Port	3a		3c / 3d		1a	
Config 1	SAS IOC				OCP Mezzanine NIC	
Config 2	SAS IOC		SAS IOC		OCP Mezzanine NIC	
Config 3	SAS IOC		M.2		OCP Mezzanine NIC	
Config 4	SAS IOC		M.2	M.2	OCP Mezzanine NIC	

Table 4 below indicates the physical mapping of the ports routed from the 1S Server ports to IOM A and IOM B ports on the Front DPB PCB. It should be noted that lane reversal was utilized on port 1a in order to optimize the routing on the drive plane board.

Table 4. PCIe Port Routing on Bryce Canyon

1S Port Spec	0	1	2	3	4	5
Intel Root Complex	IOU1				IOU2	
Intel Port	3a		3c / 3d		1a	
IOM A	0-7		8-15		16-23	
IOM B (Lane Reversed)	0-7		8-15		23-16	

The topology and port assignments for Bryce Canyon are shown below in a physical orientation for clarity.
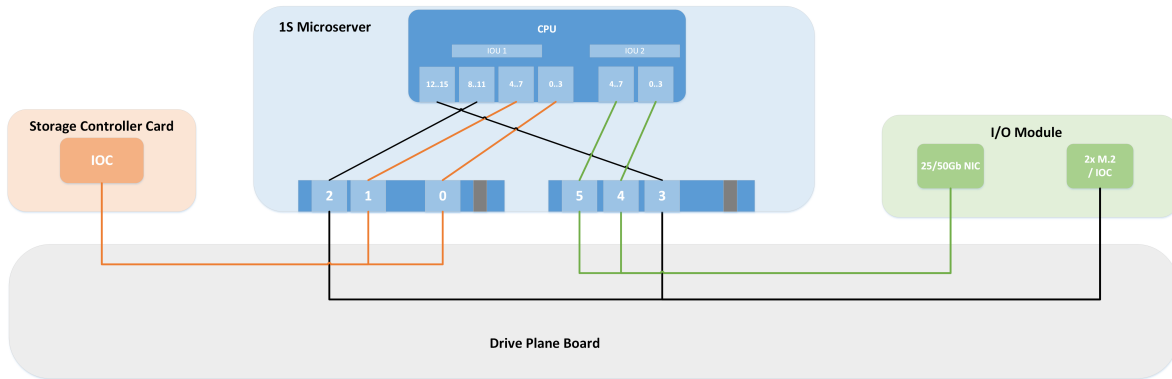
Figure 18: Bryce Canyon PCIe Topology

6.1.2 PCIe Clocks & Resets

The PCIe clocks and resets originate from the compute server, and connect to the various PCIe devices in the system. The routing of the clocks and resets is shown in Figure 19.

Due to the nature of PCIe reset signals, buffers with Schmitt Triggers should be used if the traces are deemed too long to have a sufficient edge rate.
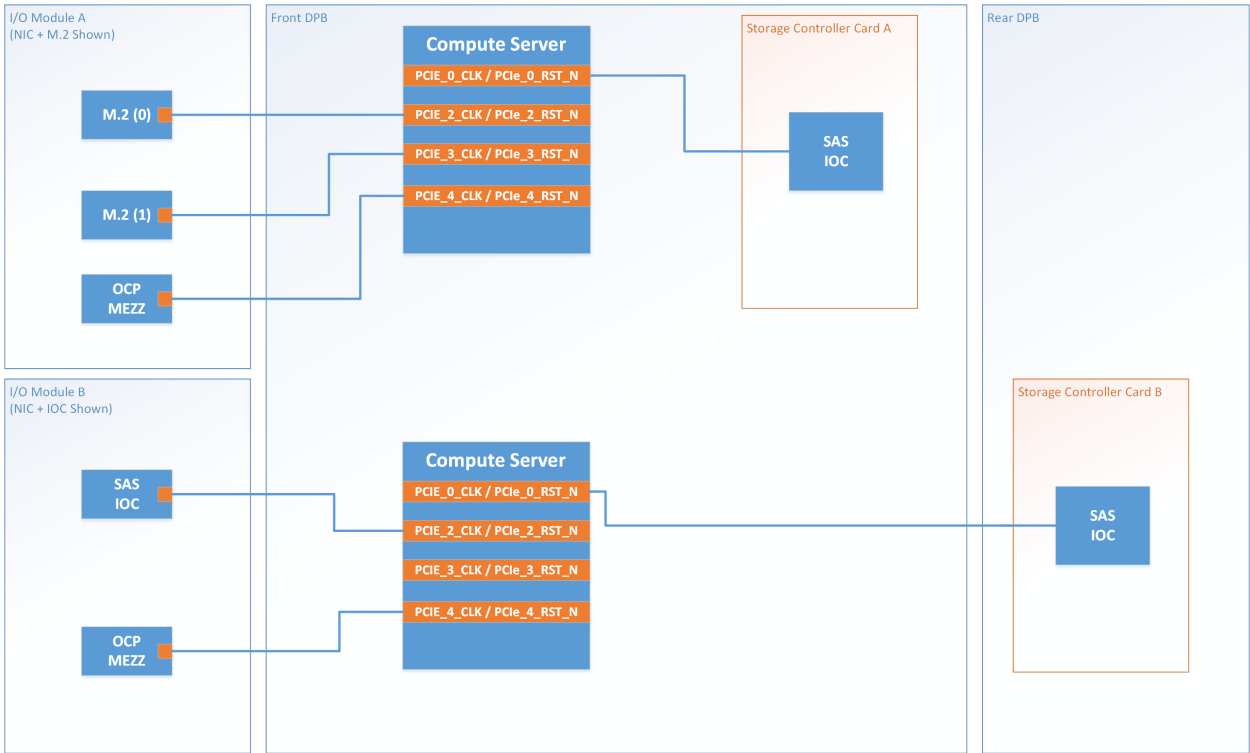
Figure 19. PCIe clock/reset block diagram

The table below shows the target pins on each IC that utilize the PCIe reset signals from the compute server. The IOM configurations in the table match the diagram shown in Figure 19 above. For all high-speed net names, refer to Table 14.

Table 5. PCIe clock/reset signal targets

PCIe Signal from Compute	Target Board	Target Device	Pin on Target Device
PCIE_COMP_A_TO_SCC_A_RST_0	SCC-A	IOC	SYS_RST_N[0]
PCIE_COMP_A_TO_IOM_A_RST_2	IOM-A	M.2 (0)	PERST#
PCIE_COMP_A_TO_IOM_A_RST_3	IOM-A	M.2 (1)	PERST#
PCIE_COMP_A_TO_IOM_A_RST_4	IOM-A	OCP Mezz	PERST_N0
PCIE_COMP_B_TO_SCC_B_RST_0	SCC-B	IOC	SYS_RST_N[0]
PCIE_COMP_B_TO_IOM_B_RST_2	IOM-B	IOC	SYS_RST_N[0]
PCIE_COMP_B_TO_IOM_B_RST_4	IOM-B	OCP Mezz	PERST_N0

6.2   Systems management

The systems management on Bryce Canyon must take into account its modularity. As covered in Section 3.3, there are several configurations that are possible: two BMCs and two SAS expanders (Dual Storage Server), a single BMC and two SAS expanders (Single Storage Server), and with SAS expanders alone (JBOD).

The BMCs shall be AST2500 chips, and run OpenBMC; DDR4 memory shall be used in conjunction with the AST2500.

6.2.1   Device management signaling

There are various connectivity protocols at work connecting the various devices and chips within the system. The Bryce Canyon design revolves around the following three configurations:

- **Dual Storage Server:** Two BMCs and two SAS expanders reside in the box.
    - o The BMCs perform the bulk of the systems management functions, while requesting some information from the expanders over dedicated I2C lines (e.g., I2C_BMC-A_EXP-A, I2C_BMC-B_EXP-B). The expanders manage the functions related to the drives, such as drive insert, power control, and LEDs (e.g., I2C_DRIVE_A_FLT_LED). The expander also manages the IOC.
    - o Between the BMC and expander, there are some shared resources: the elements on the SCC (FRUID, voltage monitor, etc.), as well as on the DPB (e.g., temperature sensors). Both the BMC and expander can initiate requests to poll the devices; however, this "multi-master" implementation can be augmented with GPIO lines between the BMC and expander. These lines can be used to request and grant access to these shared resources. Spare pins are provided for this reason.
    - o Each BMC manages its connected compute server, Storage Controller Card, and drives independently from the other BMC. The only shared resource should be the fans and the busbar HSC (P12V_CLIP), the latter monitored by the expander (SCC-B-only by default).
- **Single Storage Server:** One BMC (e.g. BMC-A) and two expanders reside in the box. The singular BMC performs the bulk of the systems management functions. However, the BMC must be able to communicate to the second expander (I2C_BMC-A_EXP-B) in order to request information that is not directly accessible to the BMC.
- **JBOD:** Two SAS expanders reside in the box. They take over the entire systems management.

To accommodate for the various configurations, the BMCs need to be aware if another healthy BMC resides in the box and also the configurations of the SCCs (to distinguish between Dual Storage Server and Single Storage Server configurations), and the expanders need to be aware if healthy BMCs are present (to distinguish between JBOD from the other configurations). Several measures are taken to accomplish this:

- **To establish presence,** the presence (or "insert") pins are routed between all IOMs and SCCs (please see Figure 25. Presence detect block diagram)

- **To self-identify location,** slot identification bits are used (refer to Table 7. Slot ID Configuration)

- **To identify hardware type,** type identification bits are used (refer to Table 18 for SCC Type pin configurations)

- **To establish health,** a heartbeat signal is run from each BMC and expander to each of the other devices within the box (see Figure 26. Miscellaneous GPIO block diagram)

6.2.2   I2C topology

See Figure 21 for the I2C system block diagram. As mentioned above, the system is built to accommodate three separate configurations, and the I2C layer was designed with this criterion in mind.

For the I2C block diagram (Figure 21), the following key should be used:
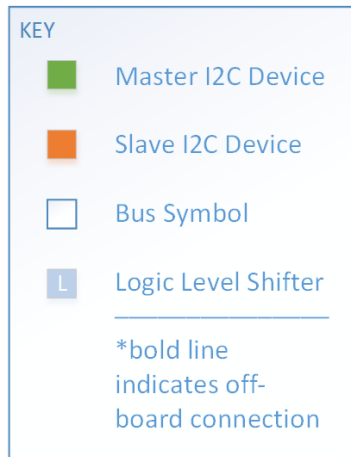
Figure 20. I2C block diagram (Key)
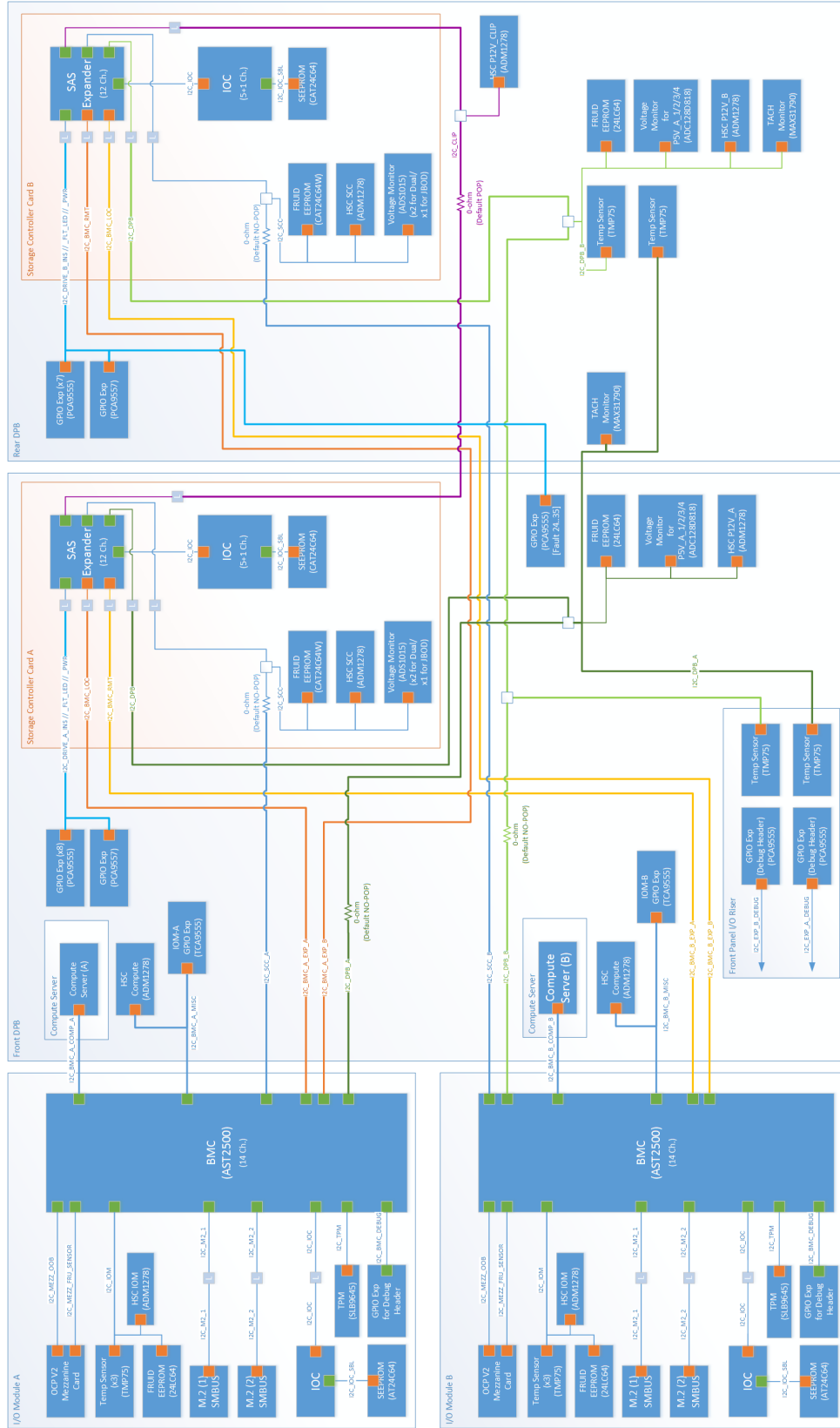
Figure 21. I2C block diagram

Note that this topology was explicitly designed to minimize the use of multimaster I2C (save for the I2C_CLIP bus, out of necessity), as well as minimize the shared resources between A/B sides. This helps improve the stability of the system by reducing firmware complexity and enabling the same DPB to be used between all system configurations.

To this end, the I2C_SCC_A/B buses are controlled by their respective expanders only; however, should multimaster wish to be enabled, this can be done through a BOM population explicitly outlined in the block diagram.

The following tables list all I2C devices in both the JBOD and Dual configurations, the buses or signals those devices are attached to, and the particular device's I2C address. The table is broken down in several sections; first, the I2C buses that are common to all system configurations are listed, and then the buses specific to certain configurations are described. This division is also made clearer when referring to Figure 21.

Table 6. I2C Device ownership table

Bus Name (on DPB)	Master	Chan.	Device	I2C Add.	Device Loc.	Purpose
[1] Buses on SCC and DPB common to Dual Storage, Single Storage, and JBOD configurations						
I2C_DPB_A/B	Expander	3	24LC64	0xA0	F/RDPB	DPBs FRUID EEPROM (Front/Rear for Side A/B)
			ADM1278	0x20	F/RDPB	HSC for P12V_A/B (Front/Rear for Side A/B)
			MAX31790	0x40	RDPB	TACH Monitor
			TMP75	0x94	Front IO Board	Temp Sensor
			TMP75	0x92	RDPB	Temp Sensor
			ADC128D818	0x3A	F/RDPB	Voltage monitor for P5V_A/B_1/2/3/4 (Front/Rear for Side A/B)
I2C_SCC_A/B	Expander	2	CAT24C64W	0xA0	SCC	SCC FRUID EEPROM
			ADM1278	0x20	SCC	HSC SCC
			ADS1015	0x90	SCC	Voltage Monitor ADC for Expander power rails
			ADS1015	**0x92**	**SCC**	**Voltage Monitor ADC for IOC power rails (not populated on JBOD SCC)**
I2C_DRIVE_A/B_PWR	Expander	4	TCA9555	0x40	F/RDPB	Drive Power [0:15]
			TCA9555	0x42	F/RDPB	Drive Power [16:31]
			TCA9557	0x30	F/RDPB	Drive Power

Bus Name (on DPB)	Master	Chan.	Device	I2C Add.	Device Loc.	Purpose
						[32:35]
I2C_DRIVE_A/B_INS	Expander	5	TCA9555	0x44	F/RDPB	Drive Insert [0:15]
			TCA9555	0x46	F/RDPB	Drive Insert [16:31]
			TCA9555	0x48	F/RDPB	Drive Insert [32:35], Fan [0:3] Insert, IOM A/B Insert, SCC B/A (remote SCC) Insert
I2C_DRIVE_A/B_FLT_LED	Expander	6	TCA9555	0x4C	F/RDPB	Drive Fault [0:15]
			TCA9555	0x4E	F/RDPB	Drive Fault [16:23] / Fan [0:3] LED
			TCA9555	0x4A	FDPB	Drive Fault [24:35]
I2C_EXP_A/B_DEBUG	Debug Card uC		TCA9555	0x4E	Front IO Board	GPIO expander for Debug Header on Front IO Board
I2C_CLIP	Expander B (and A) (Multimaster)	7	ADM1278	0x20	RDPB	HSC P12V_CLIP
[2] Buses Unique to Dual Storage Server Configuration of SCC						
I2C_IOC	Expander/IOC	8/4	LSISAS3008	0x0A	SCC	IOC to Expander
I2C_IOC_SBL	IOC (SCC)		AT24C64	0xA0	SCC	SCC IOC SEEPROM
[3] Buses on IOM common to Dual Storage and Single Storage Configuration						
I2C_BMC_A/B_COMP_A/B	BMC	4	TI Tiva MCU	0x40	Comp.	Bridge IC
			AST2500	0x20	IOM	BMC Slave
I2C_BMC_A/B_DPB_A/B_MISC	BMC	6	PCA9555	0x48	FDPB	GPIO expander to IOM A/B, for Fan [0:3] insert, Remote IOM insert, SCC A/B insert, Local SCC type detect, drawer close, etc.
			ADM1278	0x20	Comp.	HSC for P12V_A/B_COMP
I2C_IOM	BMC	1	24LC64	0xA0	IOM	FRUID EEPROM
			ADM1278	0x20	IOM	HSC IOM
			TMP75	0x90	IOM	Temp Sensor

Bus Name (on DPB)	Master	Chan.	Device	I2C Add.	Device Loc.	Purpose
			TMP75	0x94	IOM	Temp Sensor
			TMP75	0x98	IOM	Temp Sensor
I2C_MEZZ_OOB	BMC	13			IOM	OCPv2 Mezz OOB
I2C_MEZZ_FRU_SENSOR	BMC	5		0x3E	IOM	OCPv2 Mezz Thermal Sensor
I2C_TPM	BMC	14	SLB9645	0x40	IOM	Trusted Platform Module
I2C_BMC_DEBUG	Debug Card uC		PCA9555	0x4E	IOM	GPIO expander for Debug Header on IOM
[4] Buses Unique to Dual Storage Server Configuration of IOM						
I2C_M2_1	BMC	8			IOM	M.2 (1) SMBUS
I2C_M2_2	BMC	9			IOM	M.2 (2) SMBUS
[5] Buses Unique to Single Storage Server Configuration of IOM						
I2C_IOC	BMC/IOC	2/4	LSISAS3008	0x0A	IOM	IOC to BMC
I2C_IOC_SBL	IOC (IOM)		AT24C64	0xA0	IOM	IOM IOC SEEPROM
[6] Buses Between IOM and SCC, common to Dual Storage and Single Storage Configurations						
I2C_BMC_A/B_EXP_A/B	BMC	4	LSISAS3x48	0x24	Local SCC	BMC to Expander Direct
I2C_BMC_A/B_EXP_B/A	BMC	11	LSISAS3x48	0x24	Remote SCC	BMC to Remote Expander Direct

6.2.3   SPI topology

The BMCs present on the I/O Modules require dual SPI ROMs to support secure boot.
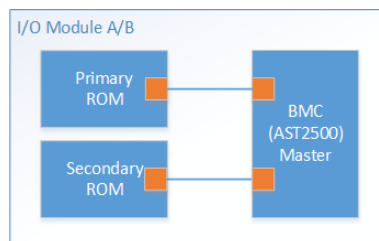
Figure 22. SPI block diagram

6.2.4   Network Controller Sideband Interface (NC-SI) requirements

NC-SI is used to provide a high speed sideband between the BMC and the NIC.

6.2.5   UART topology

The UART topology is outlined in Figure 23.

Bryce Canyon will support the new version of the OCP debug card, which uses a re-mapped USB 3.0 connector that routes the UART onto the SuperSpeed pins, and provides for a UART channel select. Please refer to Section 23.12 for more details. The UART channel select has the following behavior: The microcontroller on the debug card controls a GPIO expander on Bryce Canyon via I2C. The GPIO expander then drives an output that mirrors the channel select button on the debug card. That is, when the button is pressed, the GPIO expander will pull the output low; when the button is released, the GPIO expander will drive the output high. Because of this behavior, logic is required to count the pulses of this signal in order to transition between UART channels. The suggested implementation is to use a flip-flop (where this signal is connected as clock) to toggle between two states based on the rising edge of this signal. For the IOM debug header, the BMC can theoretically provide this logic, but the discrete logic implementation is preferred, simply to provide this functionality in the case where the BMC is unresponsive.

As indicated by the block diagram, the Compute console UART should be the default UART exposed to the debug port on the IOM. Similarly, the expander UART should be the default UART exposed to the debug port on the Front I/O Panel Riser.

The expander provides two UARTs; one (the Primary) is routed alongside the IOC UART to a UART MUX, which ultimately leads to the front panel debug connector. The Primary UART is responsible for providing the user with a console interface when directly connected to the system. The other UART (the Secondary) is routed to a header on the SCC itself, as well as to the BMC. The Secondary UART is responsible for providing a mechanism to load expander firmware code directly onto the chip.

The intention is to prove a pathway for the BMC to re-flash the expander firmware in the case that the expander is completely unresponsive. However, this low-level functionality is very dangerous as errant control can inadvertently brick or break the expander. As a result, the UART bus switch to the BMC must be disabled by default, and intentionally enabled via a GPIO asserted by the BMC.

Lastly, the BMC (AST2500) provides capability of updating its firmware over UART. This path remains functional even if the BMC is non-functional. This UART is routed to the Compute Server, which allows for updates or firmware recovery by the host.

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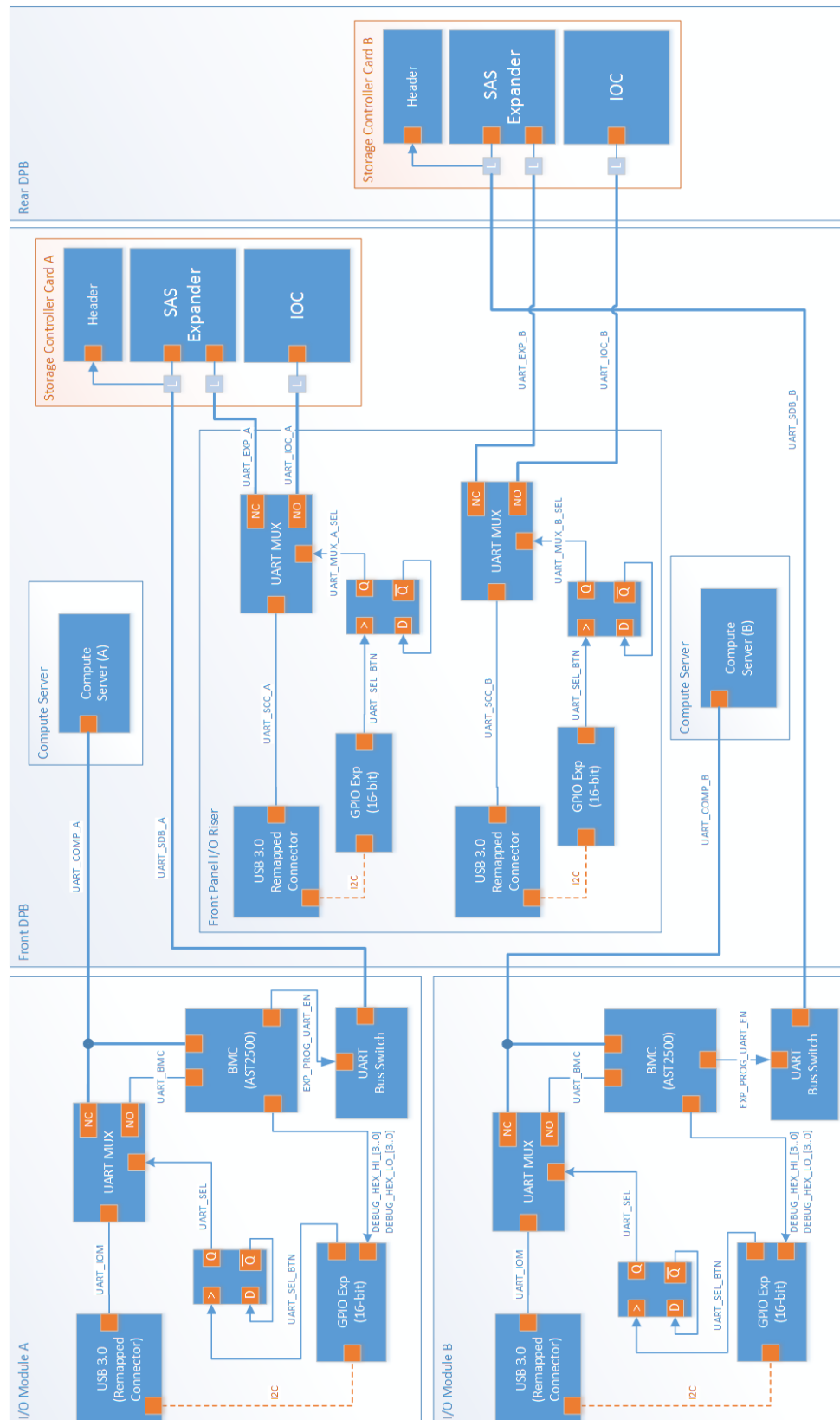
Figure 23. UART block diagram

6.2.6 USB topology

The USB topology is outlined in the diagram below. The debug header also functions as a USB port, which allows for connection of an external device (USB drive, keyboard, etc.) to the host compute server. Additionally, the BMC is connected as a device on the USB hub, which allows for a firmware upgrade path from the compute server.
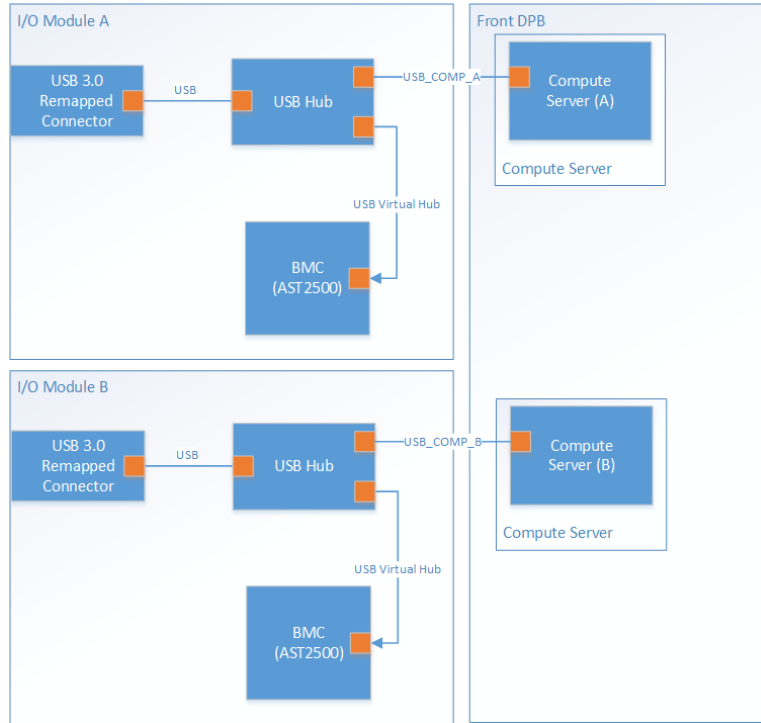
Figure 24. USB block diagram

6.2.7 GPIO (insert) topology

The IOMs and SCCs become aware of the slot in which they have been installed through SLOT_ID pins. The exact configuration of the SLOT_ID pins is specified in Table 7; for all configurations, both pins must be electrically connected.

Table 7. Slot ID Configuration

Board	SLOT_ID_0	SLOT_ID_1
IOM A	0	1
IOM B	1	0
SCC A	0	1
SCC B	1	0

The presence detect of all removable devices is shown in Figure 25.
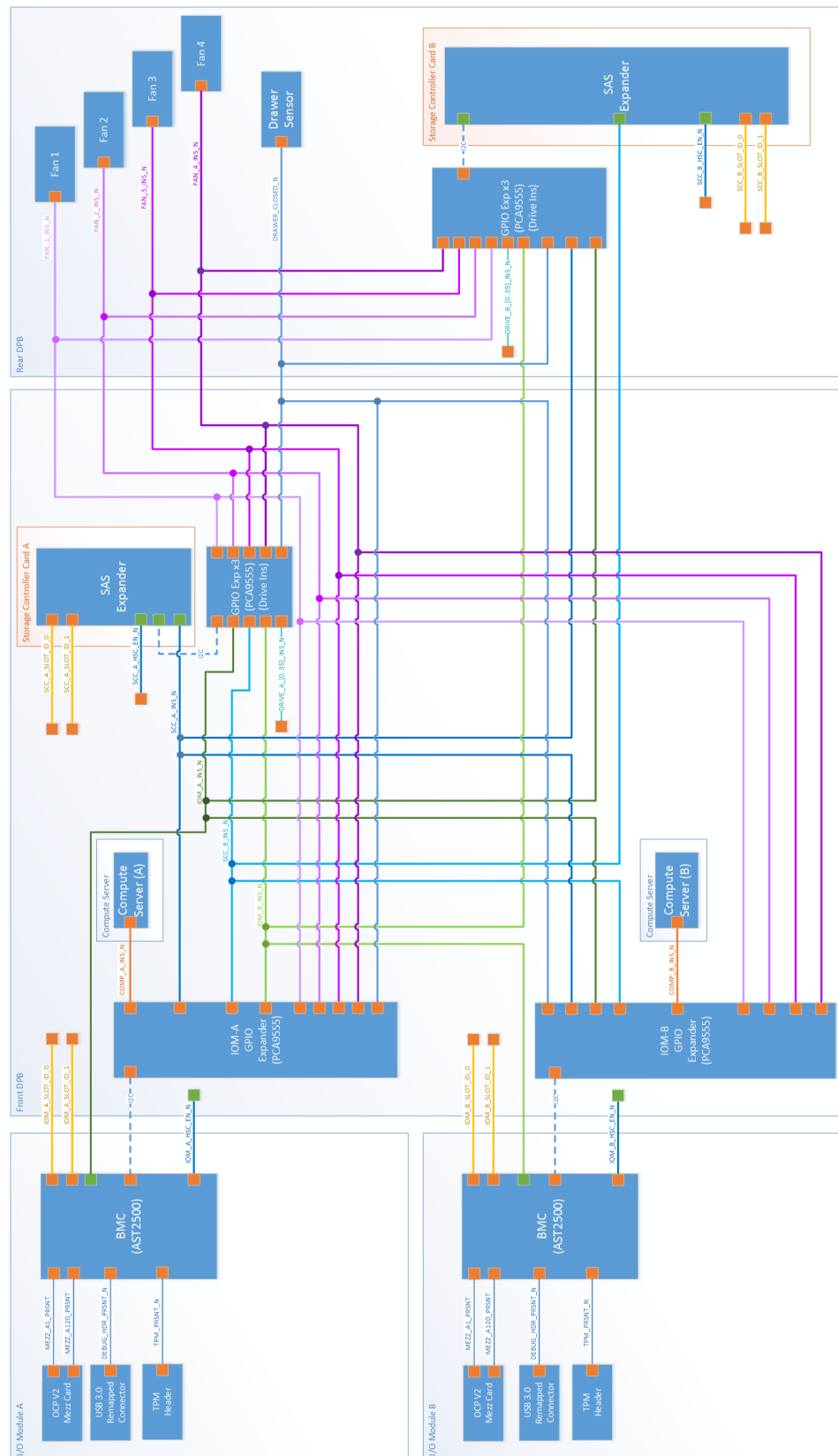
Figure 25. Presence detect block diagram

6.2.8 GPIO (miscellaneous) requirements

There are various "miscellaneous" GPIO signals that run within Bryce Canyon. The system-level block diagram of the GPIO layer can be seen in Figure 26. Among the various signals are two SPARE GPIOs, each routed from the Compute Server to the BMC and also to the expander.

Several GPIOs are run between the BMC and the Mono Lake. The following table shows the mapping between these GPIOs and the Mono Lake implementation as defined in that specification (using the "A" side as an example).

Table 8. BMC-Mono Lake GPIO Mappings

Bryce Canyon Definition	Mono Lake Definition	Pin	Logic Level	Strapping on Mono Lake	Direction	Notes
COMP_A/B_ BMC_A/B_ SPARE_0	SVR_ID0	A5	3V3	4.7k PU	To BMC	Spare
COMP_A/B_ BMC_A/B_ SPARE_1	SVR_ID1	A6	3V3	4.7k PU	To BMC	Spare
COMP_A/B_ EXP_A/B_ SPARE_0	SVR_ID2	A9	3V3	4.7k PU	To Expander	Spare
BMC_A_ RESET	SVR_ID3	A10	3V3	N/A	To BMC	For Compute to reset BMC
COMP_A_ BMC_A_ ALERT	I2C_ALERT#	B12	3V3	N/A	To BMC	I2C alert
COMP_A_ POWER_ FAIL_N	POWER_ FAIL_N	B82	3V3	4.7k PU		Active low open drain signal with pullup on 1S server. Platform generates this signal and uses it as a big hammer to throttle 1S server down to lowest possible power state as fast as possible.
COMP_A_ FAST_ THROTTLE_N	FAST_ THROTTLE_N	A41	3V3	4.7k PU		Active low open drain signal with pullup on 1S server. When this signal is asserted by platform, it informs 1S server that base system is going to cut 12V power to 1S server in certain amount of time, which is pre-defined by base system. It is possible for 1S server to perform graceful shutdown based on this signal.
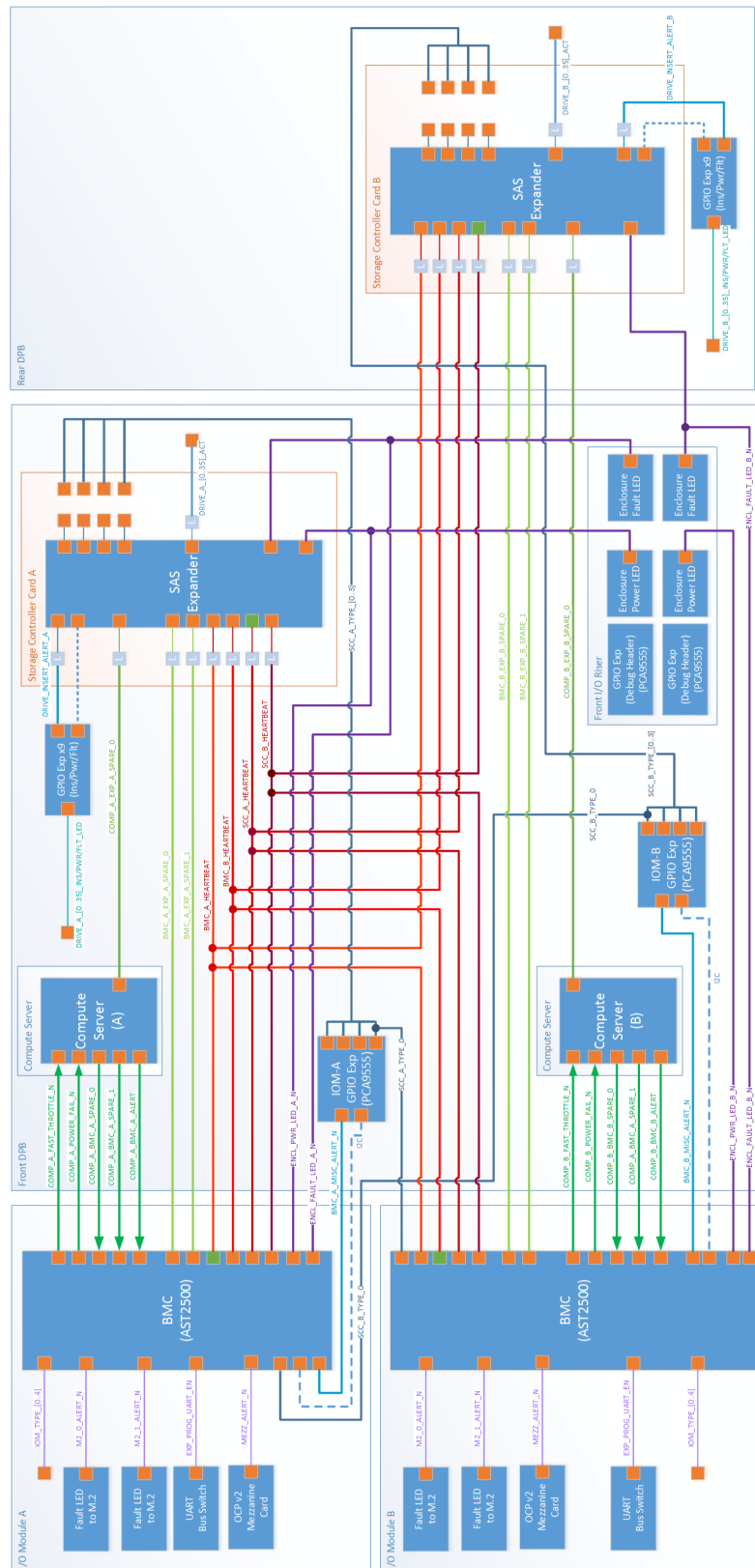
Figure 26. Miscellaneous GPIO block diagram

6.2.9   Fan control

Fan control is broken down into two zones, which are denoted as "Zone C" and "Zone D." Zone C controls fans 1 and 2, which mostly affect the compute modules and SCCs, and Zone D controls fans 0 and 3, which mostly affect the drives. The layout of these fans is depicted in Figure 76. System mechanical layout.

All BMCs and expanders will set a desired PWM for both Zone C and Zone D to the respective PWM comparator, which uses the highest of the four signals to set all fan speeds for that zone. In return, the TACH signals of all four fans (eight rotors in total) will be read by two independent TACH monitors, one corresponding to each system within the box. Both the expander and the BMC can poll their TACH monitor in a multi-master I2C arrangement. Should multi-master wish to be avoided, the BMC can opt to poll the fan information from the expander.
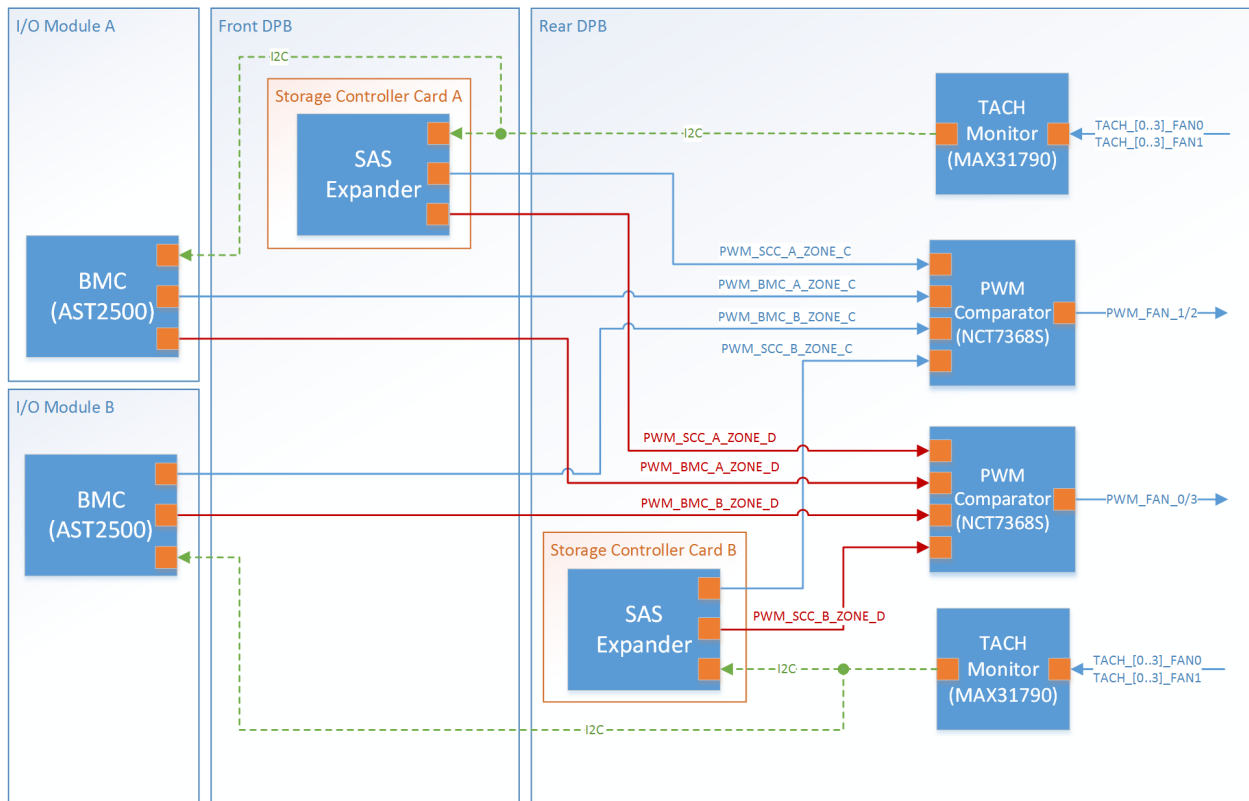
Figure 27. PWM and TACH block diagram

6.2.10 Reset and Power Enable

The control of how the system powers on/off and resets depends on the configuration. Figure 28 shows the complete topology for the entire system, and is intended to show all necessary hardware connections that would necessitate the desired control scheme. The following block diagrams show the specific implementation from the perspective of various boards.

Regardless of configuration, all systems have buttons that are accessible on the Front IO Panel (see Section 4.2), which is hidden behind the front sheet metal (see Section 20.5). The power buttons (for sides A and B) are hard power-off buttons that turn off the HSC supplying that respective side (see DPB_PWR_BTN_A/B on the diagram). If both sides are powered off, this will also switch off power to the fans (FAN_EN). This is intended to prevent the fans from running at full speed if there are no controllers to control the PWM. The reset buttons are intended to reset the expander (see DPB_RST_BTN_A/B_N). This reset is not a Power-On-Reset.

6.2.10.1 Integrated (*Dual*) Configuration
In this configuration, each BMC/expander pair is responsible for controlling its own side of the system. Upon initial power application to the IOM (P12V_IOM_PGOOD), the standby converters turn on to provide power to the BMC and NIC. The BMC is aware of this status (IOM_STBY_PGOOD). At the same time, upon initial power application to the SCC (P12V_SCC_PGOOD), the standby converters turn on to provide power for necessary end devices (e.g., FRUID EEPROM, voltage monitors) that the BMC can query in this standby scenario. The BMC is also aware of this status (SCC_A/B_STBY_PGOOD).

The BMC can control power to the remainder of the SCC (SCC_FULL_PWR_EN), which controls the converters that power the SAS expander and IOC. Upon successful sequencing of these converters (SCC_FULL_PGOOD), both chips are brought out of Power-On-Reset. The BMC is also aware of this event.

The expander is responsible for controlling power to the drives according to its spin-up/down algorithm. The P5V to the drives should already be available before this point, since it is automatically enabled once power is applied; the expander controls the FETs that gate power to individual drives.

The IOM also houses major functional components. In this configuration, the BMC controls power to the converters that supply the M.2 (IOM_FULL_PWR_EN). The BMC is also aware of this event (IOM_FULL_PGOOD).

The Compute Server houses a Bridge IC that exposes some management capability for the server. The BMC can control the power to this by turning on the HSC to the Compute Server (COMP_A/B_PWR_EN).

At this point, all major functional components should be turned on, and all PCIe devices should be held in PCIe reset, because the CPU on the Compute Server has not been switched on. The BMC does so with COMP_A/B_PWR_BTN_N.

To power off the system gracefully, a button on the IOM should be pressed and held (IOM_PWR_BTN_N).

To reset the Compute module, a button on the IOM should be pressed (IOM_RST_BTN_N), which the BMC uses to reset the module (SYS_A/B_RESET_N).

The Debug Card on the IOM has a reset button that, when pressed, can be read by the BMC (DEBUG_RST_BTN_N). Currently, there are no plans to use this button.

The BMC can also initiate a chip reset to its attached expander (BMC_A/B_TO_EXP_A/B_RESET_N). This is not a Power-On-Reset.

Lastly, the BMC itself can be reset from the Compute Server, through COMP_A/B_TO_BMC_A/B_RESET.

6.2.10.2 Integrated (*Single*) Configuration
In this configuration, there are two SCCs and one IOM installed. For illustration, we will assume IOM A is installed, although this configuration does not have side affinity.

The BMC A and expander A pair is responsible for controlling its own side of the system. The expander B is responsible for controlling its own side of the system (namely, its drives). Upon initial power application to the IOM (P12V_IOM_PGOOD), the standby converters turn on that provide power to the BMC and NIC. The BMC is aware of this status (IOM_STBY_PGOOD). At the same time, upon initial power application to the SCC (P12V_SCC_PGOOD), the standby converters turn on to provide power for necessary end devices (e.g., FRUID EEPROM, voltage monitors) that the BMC can query in this standby scenario. The BMC is also aware of this status (SCC_A/B_STBY_PGOOD).

SCC B only houses a SAS expander (no IOC) and, by virtue of minimizing SKUs, it has resistor strappings to enable it to turn on automatically once power is applied (SCC_FULL_PWR_EN goes high once SCC_STBY_PGOOD goes high). Upon successful sequencing of these converters (SCC_FULL_PGOOD), the SAS expander B is brought out of Power-On-Reset.

The BMC A can control power to the remainder of the SCC A (SCC_A_FULL_PWR_EN), which controls the converters that power the SAS expander and IOC. Upon successful sequencing of these converters (SCC_FULL_PGOOD), both chips are brought out of Power-On-Reset. The BMC is aware of this event.

The expander is responsible for controlling power to the drives according to its spin-up/down algorithm. The P5V to the drives should already be available before this point, since it is automatically enabled once power is applied; the expander controls the FETs that gate power to individual drives.

The IOM also houses major functional components. In this configuration, the BMC controls power to the converters that supply its on-board IOC (IOM_FULL_PWR_EN). The BMC is also aware of this event (IOM_FULL_PGOOD).

The Compute Server houses a Bridge IC that exposes some management capability for the server. The BMC can control the power to this by turning on the HSC to the Compute Server (COMP_A_PWR_EN).

At this point, all major functional components should be turned on, and all PCIe devices should be held in PCIe reset, because the CPU on the Compute Server has not been switched on. The BMC does so with COMP_A_PWR_BTN_N.

To power off the system gracefully, a button on the IOM should be pressed and held (IOM_PWR_BTN_N). Although SCC B is turned on automatically, BMC A can still turn it off (SCC_B_FULL_PWR_EN).

To reset the Compute module, a button on the IOM should be pressed (IOM_RST_BTN_N), which the BMC uses to reset the module (SYS_A_RESET_N).

The Debug Card on the IOM has a reset button that, when pressed, can be read by the BMC (DEBUG_RST_BTN_N). Currently, there are no plans to use this button.

The BMC can also initiate a chip reset to its attached expander (BMC_A_TO_EXP_A_RESET_N). This is not a Power-On-Reset.

Lastly, the BMC itself can be reset from the Compute Server, through COMP_A_TO_BMC_A_RESET.

6.2.10.3 JBOD Configuration
In this configuration, there are no BMCs. The two SCCs installed only have SAS expanders present (i.e., they are the same SKU as SCC B as described in the Integrated (Single) Configuration).

The SCC has resistor strappings to enable it to turn on automatically once power is applied (SCC_FULL_PWR_EN goes high once SCC_STBY_PGOOD goes high). Upon successful sequencing of these converters (SCC_FULL_PGOOD), the SAS expander B is brought out of Power-On-Reset.

The expander is responsible for controlling power to the drives according to its spin-up/down algorithm. The P5V to the drives should already be available before this point, since it is automatically enabled once power is applied; the expander controls the FETs that gate power to individual drives.

The system can only be powered off and reset from the Front IO Panel.
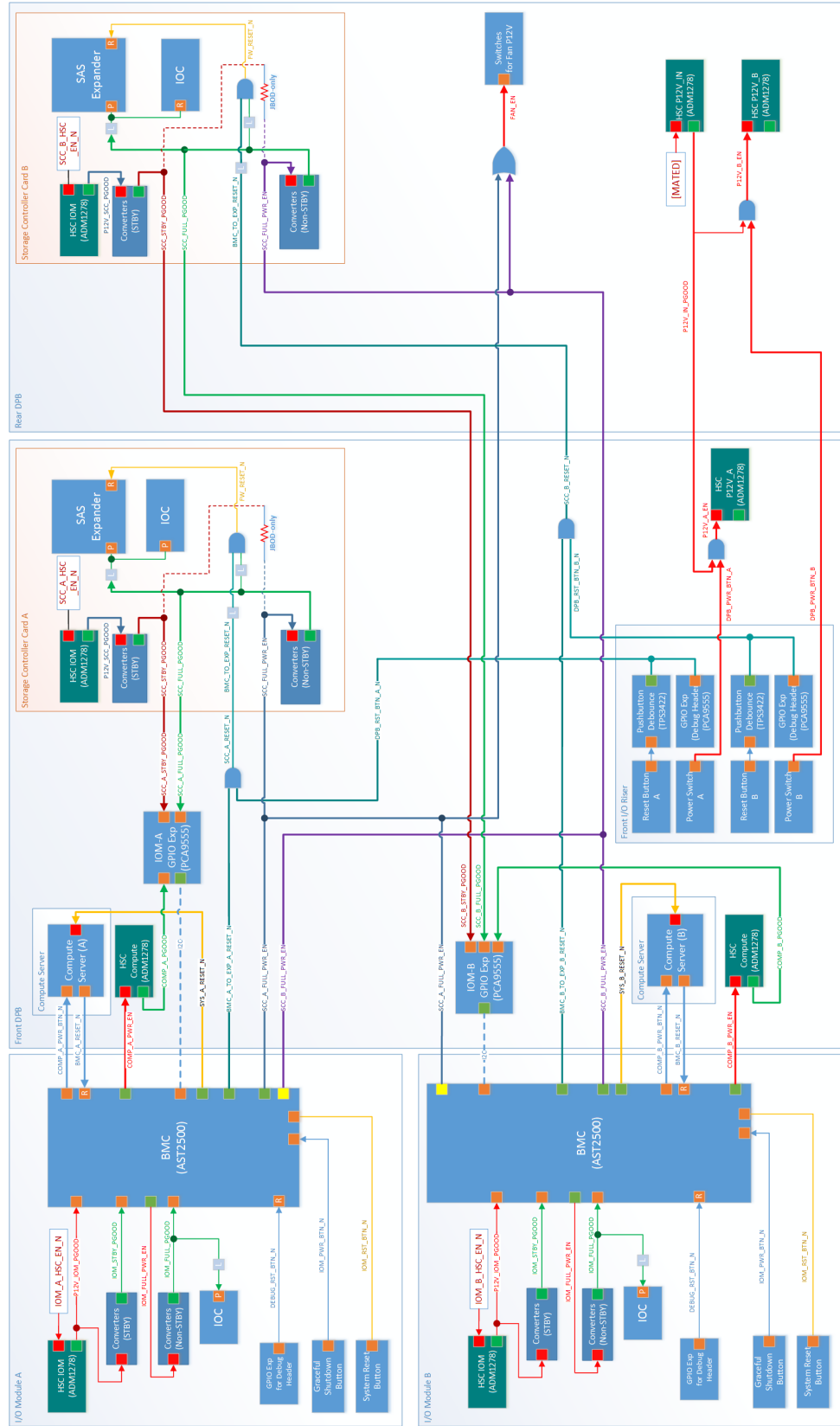
Figure 28. Power and Reset signal overview block diagram
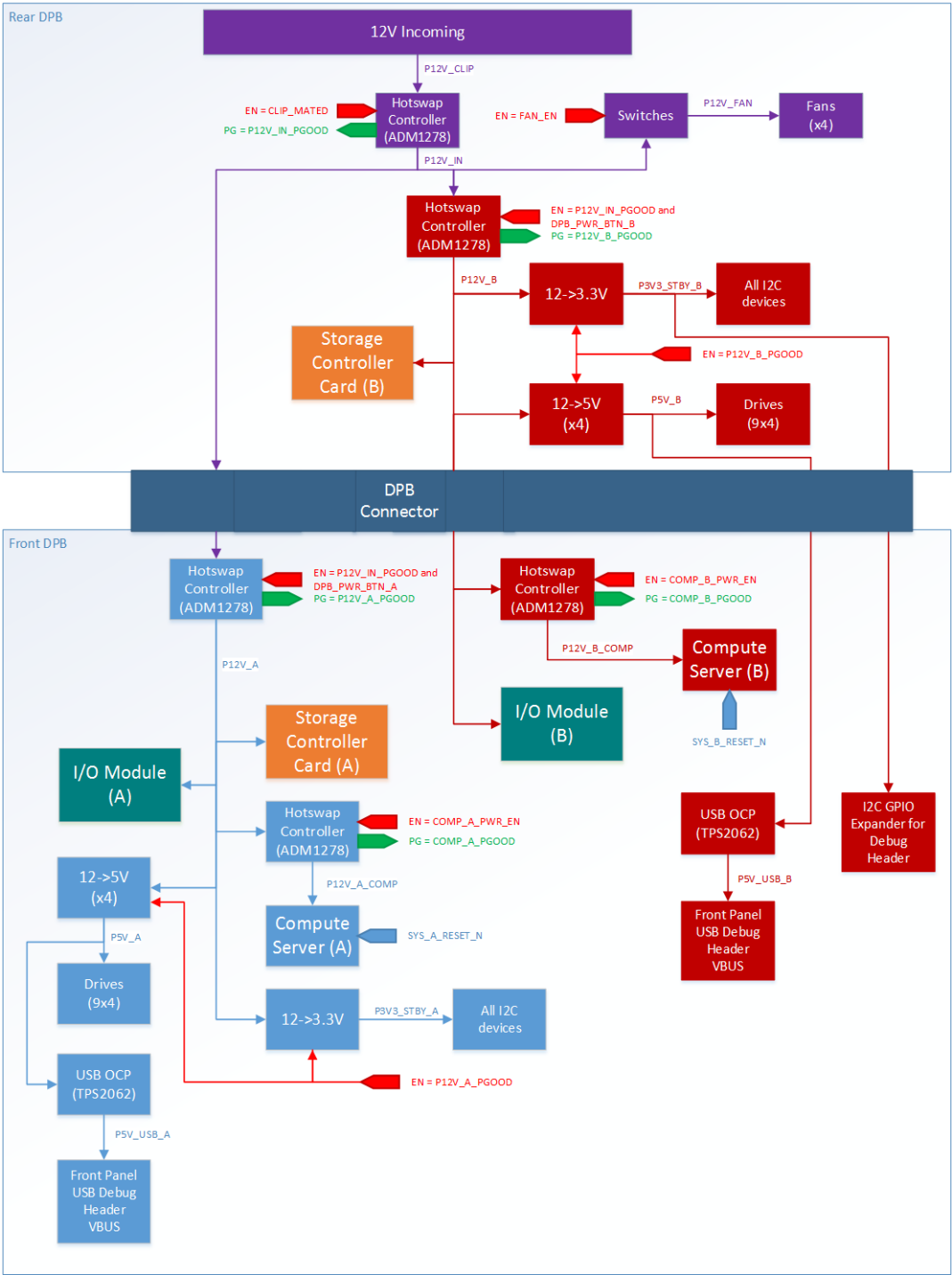
Figure 29. Power and Reset system overview block diagram
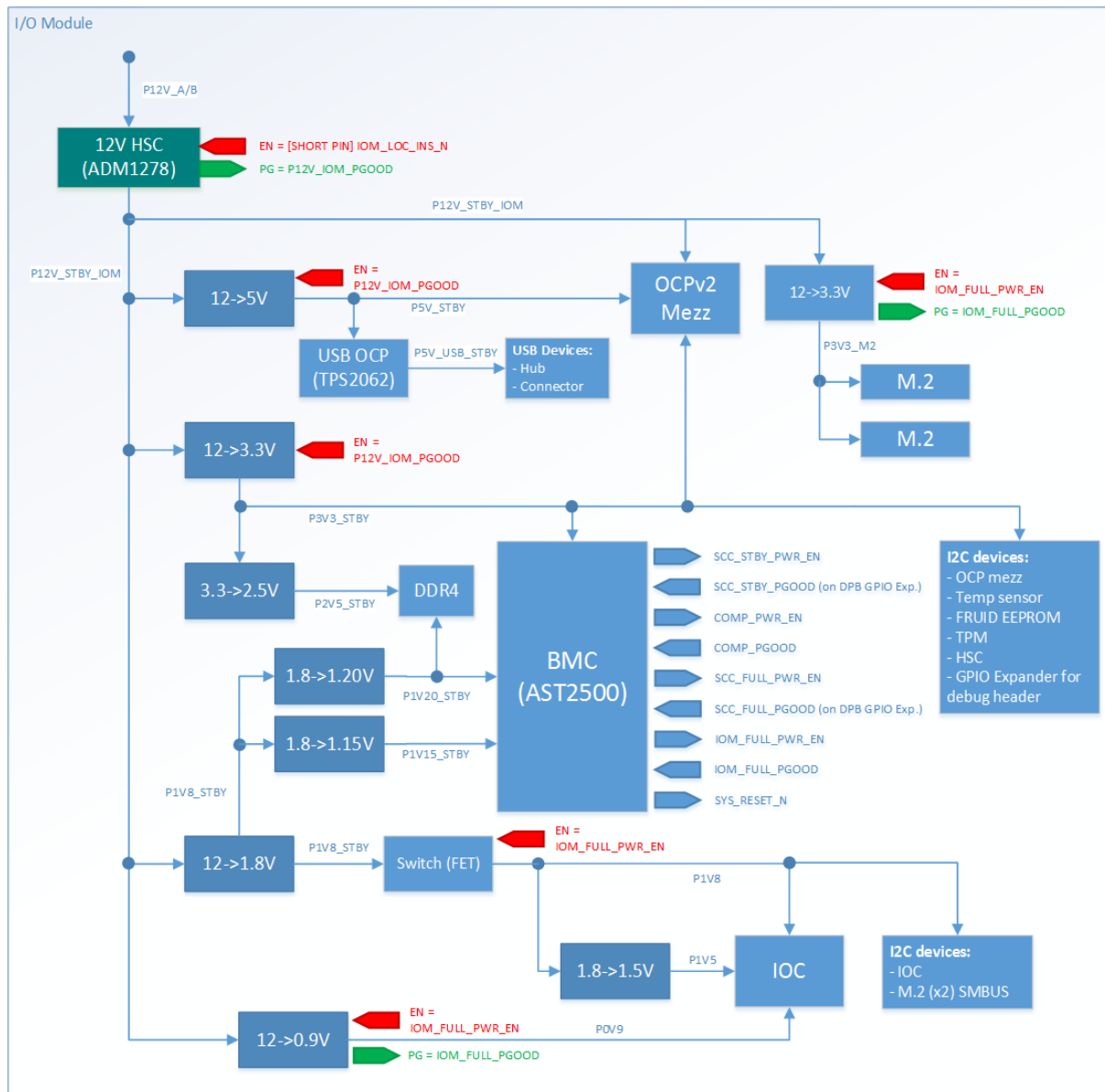
Figure 30. I/O Module Power and Reset block diagram
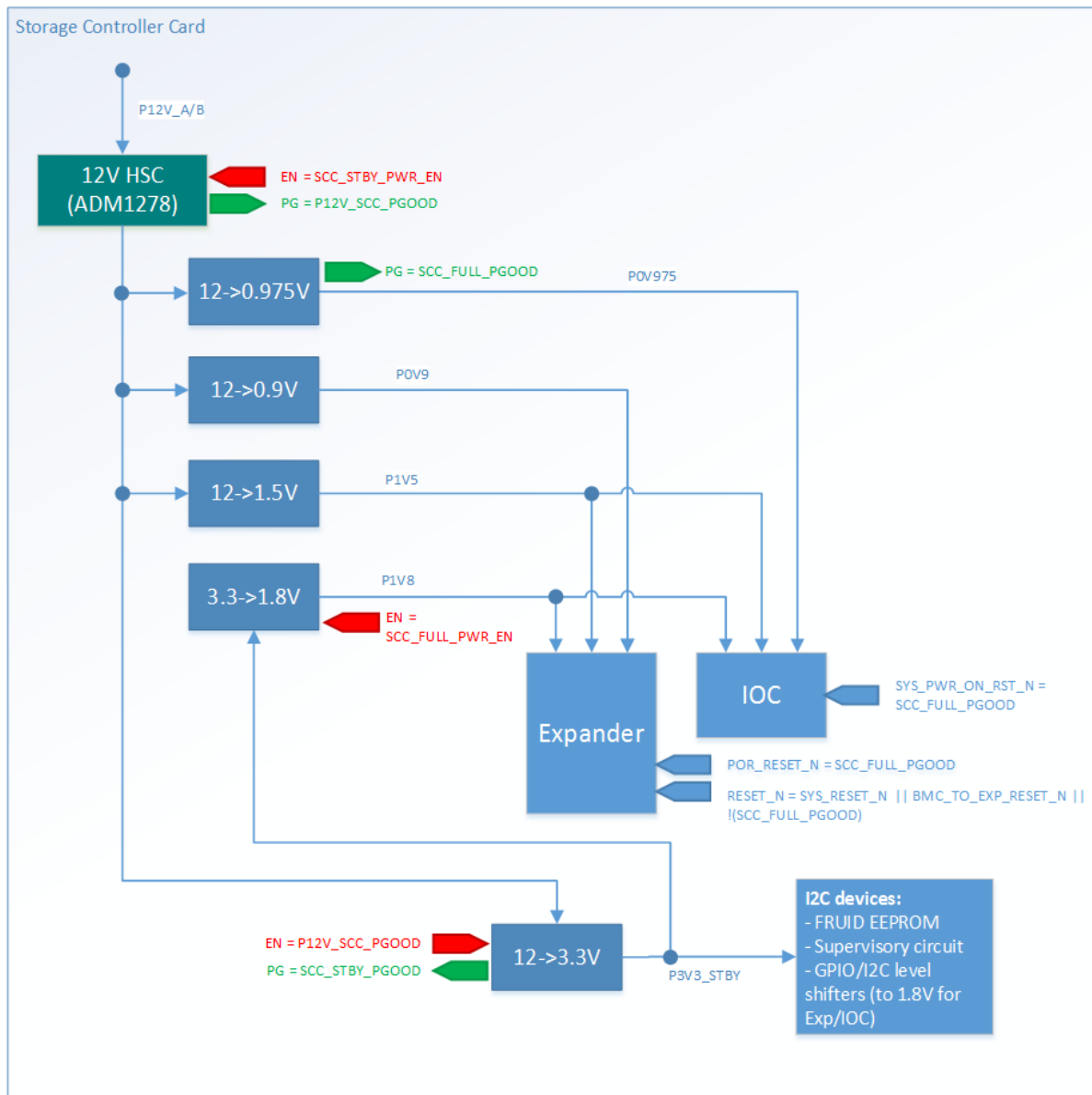
Figure 31. Storage Controller Card Power and Reset block diagram

6.2.11   Systems management signals and connections

This section includes details about the systems management signal scheme within Bryce Canyon.

6.2.11.1   Systems management signal strapping

The following tables denote various signals across the system and their default strapping value and direction (U = Up, D = Down). The tables also indicate whether buffers are required to re-drive a signal, where they should be located, and whether switches are required to prevent leakage in partial power-down scenarios.

In addition to the tables in this section, the GPIOs that specifically support the 1S server are outlined in Table 8.

Table 9. Resistor strapping table for I2C

Signal Name	DPB	IOM	SCC	Buffer	Notes
I2C_BMC_A_COMP_A		2.2kΩ U			Switch on IOM controlled by COMP_PWR_EN
I2C_BMC_A_EXP_A	2.2kΩ U	2.2kΩ U	1kΩ U	SCC	Switch on IOM controlled by P3V3_STBY_PGOOD (of P3V3 converter on IOM). PU on SCC intended for level shifter.
I2C_BMC_A_EXP_B	2.2kΩ U	2.2kΩ U	1kΩ U		Switch on IOM controlled by P3V3_STBY_PGOOD (of P3V3 converter on IOM). Pull-up on DPB should be on Rear DPB.
I2C_BMC_A_MISC	2.2kΩ U	2.2kΩ U			Switch on IOM controlled by P3V3_STBY_PGOOD (of P3V3 converter on IOM)
I2C_SCC_A	2.2kΩ U	2.2kΩ U	1kΩ U	DPB SCC	Switch on IOM controlled by P3V3_STBY_PGOOD (of P3V3 converter on IOM). Buffer on DPB meant to buffer signal between IOM and SCC; however, the path is 0Ω no-pop by default on DPB. PU on DPB both before and after buffer; values will need to be tuned if this I2C path is enabled. PU on SCC between level shifter and expander.
I2C_DPB_A	2.2kΩ U	2.2kΩ U		DPB	Switch on IOM controlled by P3V3_STBY_PGOOD (of P3V3 converter on IOM). Buffer on DPB meant to buffer signal between IOM and SCC; however, the path is 0Ω no-pop by default on DPB. Pull-up on DPB both before and after buffer; values will need to be tuned if this I2C path is enabled. Pull-up on SCC between level shifter and expander.
I2C_MEZZ_OOB		2.2kΩ U			
I2C_MEZZ_FRU_SENSOR		2.2kΩ U			
I2C_IOM		2.2kΩ U			
I2C_TPM		2.2kΩ U			
I2C_BMC_DEBUG		2.2kΩ U			
I2C_M2_1		2.2kΩ U 1kΩ U		IOM	Two pull-up values are listed for different sides of level shifter.
I2C_M2_2		2.2kΩ U 1kΩ U		IOM	Two pull-up values are listed for different sides of level shifter.
I2C_IOC (on IOM)		2.2kΩ U 2.2kΩ U		IOM	For IOC on IOM (not to be confused with IOC on SCC). Pull-up should be before and after level shifter.
I2C_IOC_SBL (on IOM)		2.2kΩ U		IOM	For IOC on IOM (not to be confused with IOC on SCC).
I2C_DRIVE_A_INS	2.2kΩ U		1kΩ U	SCC DPB	Pull-up on SCC between level shifter and expander.
I2C_DRIVE_A_FLT_LED	2.2kΩ U		1kΩ U	SCC DPB	Pull-up on SCC between level shifter and expander.
I2C_DRIVE_A_PWR	2.2kΩ U		1kΩ U	SCC DPB	Pull-up on SCC between level shifter and expander.

Signal Name	DPB	IOM	SCC	Buffer	Notes
I2C_CLIP	2.2kΩ U		1kΩ U	SCC DPB	Pull-up on SCC between level shifter and expander.
I2C_IOC (on SCC)			2.2kΩ U		
I2C_IOC_SBL (on SCC)			2.2kΩ U		
I2C_EXP_A_ DEBUG			2.2kΩ U		On Front IO Panel

Table 10. Resistor strapping table for GPIO (Presence Detect/Insert)

Signal Name	DPB	IOM	SCC	Buffer	Notes
COMP_A_INS_N	100kΩ U				100Ω pull-down on Pin A1 of both Primary and Secondary connectors of 1S Server (as per spec). Pull-ups on DPB exist for both connectors; both of these insert pins must be pulled low for COMP_A_INS_N to be pulled low.
DEBUG_CARD_ PRSNT_N		100kΩ D			Pull-up on debug card
DRAWER_CLOSED_N	10kΩ U				
DRIVE_A_[0:35]_ INS_N	10kΩ U				
FAN_0_INS_N	100kΩ U				
FAN_1_INS_N	100kΩ U				
FAN_2_INS_N	100kΩ U				
FAN_3_INS_N	100kΩ U				
IOM_A_ SLOT_ID_[0:1]	(config-dependent)		100kΩ U		Pull-up on IOM to P3V3; pull-down exists on DPBs, strapping depends on the slot
IOM_A_HSC_EN_N	0Ω D		10kΩ U		Inverted logic. Pull-up on IOM to P12V on pre-charge pins to drive inverter, which drives HSC enable pin low. When last-mate pin on SCC engages pull-down on DPB, inverter will drive HSC enable pin high.
IOM_A_INS_N	100kΩ U		0Ω D		Pull-down on IOM to indicate to other boards that the SCC is inserted
MEZZ_PRSNT_A1_N		See notes			See OCP Mezzanine 2.0 Spec v1.0 for implementation
MEZZ_PRSNT_A120_N		See notes			See OCP Mezzanine 2.0 Spec v1.0 for implementation
SCC_A_ SLOT_ID_[0:1]	(config-dependent)		10kΩ U		Pull-up on SCC to P1V8; pull-down exists on DPBs, strapping depends on the slot
SCC_A_HSC_EN_N	0Ω D		10kΩ U		Inverted logic. Pull-up on SCC to P12V on pre-charge pins to drive inverter, which drives HSC enable pin low. When last-mate pin on SCC engages pull-down on DPB, inverter will drive HSC enable pin high.
SCC_A_INS_N	100kΩ U		0Ω D		Pull-down on SCC to indicate to other boards that the SCC is inserted
TPM_PRSNT_N		10kΩ U			

Table 11. Resistor strapping table for GPIO (Miscellaneous)

Signal Name	DPB	IOM	SCC	Buffer	Notes
BMC_A_HEARTBEAT				SCC	Level shifted to expander on SCC
BMC_A_MISC_ALERT _N	100kΩ U	4.7kΩ U		DPB	Pull-ups reside on opposite sides of the buffer.
DRIVE_A_[0..35]_ PWR	100kΩ D				

Signal Name	DPB	IOM	SCC	Buffer	Notes
DRIVE_A_[0..35]_FLT_LED	100kΩ D				
DRIVE_A_[0..35]_INS	10kΩ U				
DRIVE_INSERT_ALERT_A	10kΩ U		10kΩ U	SCC	Pull-up on SCC between level shifter and expander. Wired-OR connection between all GPIO expanders.
ENCL_FAULT_LED_A_N	10kΩ U			SCC	Any device can pull the line low to drive the LED. Level shifted to expander on SCC
ENCL_PWR_LED_A_N	10kΩ U			SCC	Any device can pull the line low to drive the LED. Level shifted to expander on SCC
IOM_TYPE_[0..3]		(config-dependent)			See Table 23 for setting of pull-up/pull-downs on IOM. All of these exist solely on the IOM, since only the BMC needs to be notified of this information.
M2_1_ALERT_N		4.7kΩ U			
M2_1_ALERT_N		4.7kΩ U			
MEZZ_ALERT_N		4.7kΩ U			
SCC_A_HEARTBEAT				SCC	Level shifted to expander on SCC
SCC_TYPE_[0..3]	10kΩ U		(config-dependent)		See Table 18 for setting of pull-downs on SCC.

Table 12 describes the signals used for Reset/Power control to the boards of the system. Because these types of signals encapsulate fairly complicated logic (i.e., they depend on many inputs, and drive many outputs as a result), the table below is a guideline for the design, rather than an exhaustive description of the implementation. In general, these signals need to be buffered to ensure clean edges and prevent back-feeding in partial power-off scenarios.

Table 12. Resistor strapping table for GPIO (Reset/Power Control)

Signal Name	DPB	IOM	SCC	Buffer	Notes
BMC_A_EXP_A_RESET_N		4.7kΩ U		DPB	
BMC_TO_EXP_RESET_N (called SCC_A_RESET_N on DPB)			10kΩ U	SCC	Pull-up on SCC after level shifter
COMP_A_PGOOD	10kΩ U				HSC has open-drain output
COMP_A_PWR_BTN_N		10kΩ U			
COMP_A_PWR_EN	TBDΩ D			DPB	Final value may need to be tuned based on which voltage rail is driving this signal
DEBUG_RST_BTN_N		4.7kΩ U			
DPB_PWR_BTN_A_N	10kΩ U 10kΩ U			DPB	Pull-ups on both sides of buffer
FAN_EN				DPB	Driven from OR gate
FW_RESET_N			10kΩ U	SCC	Signal should be buffered before used as a chip reset on expander/IOC.
IOM_FULL_PGOOD		4.7kΩ U 4.7kΩ U		IOM	Pull-ups before and after level shifter. Signal should be buffered before used as a chip reset on IOC.
IOM_FULL_PWR_EN					BMC should have push-pull output

Signal Name	DPB	IOM	SCC	Buffer	Notes
IOM_PWR_BTN_N		4.7kΩ U 4.7kΩ U		IOM	Pull-ups on both sides of buffer
IOM_STBY_PGOOD		4.7kΩ U			
SCC_FULL_PGOOD			Multiple	SCC	This signal is ultimately routed to the SCC connector so it can be read by other devices from the DPB; however, on the SCC it must drive Power-On-Resets and Resets of the expander and IOC, so the exact implementation is not described in this specification.
SCC_FULL_PWR_EN			0Ω (JBOD) TBDΩ (Integrated)	SCC	In JBOD configuration, SCC_FULL_PWR_EN should be wired to SCC_STBY_PGOOD (since the entire power sequence should be automatically enabled without BMC intervention). In the Integrated configuration (with IOC), the BMC should be able to gate the IOC/expander core power. There are two implementation options, depending on whether the BMC output is configured as push-pull or open-drain.
SCC_STBY_PGOOD			10kΩ U	SCC	
SYS_A_RESET_N	100kΩ D			IOM DPB	Pull-down on DPB at 1S Server connector side

6.2.11.2 Systems management signals count for connectors

The following table describes the systems management signals that cross the boards in the system. That is, this table contains the pin counts for the board-to-board connectors, as well as the counts for the I2C GPIO expanders on the DPB (illustrated in Figure 25 and Figure 26). This is meant as a guide to provision the number of pins available.

The net names given are from the DPB perspective, since all system signals must traverse this board.

Table 13. Systems management signals count for connectors

Signal Name (DPB Ref)	Signal Type	IOM-A	IOM-A GPIO Exp.	IOM-B	IOM-B GPIO Exp.	SCC-A	SCC-A GPIO Exp.	DPB	SCC-B	SCC-B GPIO Exp.
BMC_A_EXP_A_RESET_N	GPIO	1				1				
BMC_A_EXP_A_SPARE_0	GPIO	1				1				
BMC_A_EXP_A_SPARE_1	GPIO	1				1				
BMC_A_HEARTBEAT	PWM	1		1		1		1	1	
BMC_A_MISC_ALERT	GPIO	1								
BMC_A_RESET_N	GPIO	1								
BMC_B_EXP_B_RESET_N	GPIO			1				1	1	
BMC_B_EXP_B_SPARE_0	GPIO			1				1	1	
BMC_B_EXP_B_SPARE_1	GPIO			1				1	1	
BMC_B_HEARTBEAT	PWM	1		1		1		1	1	
BMC_B_MISC_ALERT	GPIO			1						
BMC_B_RESET_N	GPIO			1						
COMP_A_BMC_A_ALERT	GPIO	1								
COMP_A_BMC_A_SPARE_0	GPIO	1								
COMP_A_BMC_A_SPARE_1	GPIO	1								
COMP_A_EXP_A_SPARE_0	GPIO					1				
COMP_A_FAST_THROTTLE_N	GPIO	1								
COMP_A_INS_N	GPIO		1							
COMP_A_PGOOD	GPIO		1							
COMP_A_POWER_FAIL_N	GPIO	1								
COMP_A_PWR_BTN_N	GPIO	1								
COMP_A_PWR_EN	GPIO	1								
COMP_B_BMC_B_ALERT	GPIO			1						
COMP_B_BMC_B_SPARE_0	GPIO			1						
COMP_B_BMC_B_SPARE_1	GPIO			1						
COMP_B_EXP_B_SPARE_0	GPIO							1	1	
COMP_B_FAST_THROTTLE_N	GPIO			1						
COMP_B_INS_N	GPIO				1					
COMP_B_PGOOD	GPIO				1					
COMP_B_POWER_FAIL_N	GPIO			1						
COMP_B_PWR_BTN_N	GPIO			1						
COMP_B_PWR_EN	GPIO			1						
DPB_PWR_BTN_A	INPUT							1		
DPB_PWR_BTN_B	INPUT							1		
DRAWER_CLOSED_N	GPIO		1		1		1	1		1
DRIVE_A_[0:35]_ACT	GPIO					36				
DRIVE_B_[0:35]_ACT	GPIO								36	
DRIVE_INSERT_ALERT_A_N	GPIO					1				
DRIVE_INSERT_ALERT_B_N	GPIO								1	
ENCL_FAULT_LED_A_N	GPIO	1				1				
ENCL_FAULT_LED_B_N	GPIO			1				1	1	

Signal Name (DPB Ref)	Signal Type	IOM-A	IOM-A GPIO Exp.	IOM-B	IOM-B GPIO Exp.	SCC-A	SCC-A GPIO Exp.	DPB	SCC-B	SCC-B GPIO Exp.
FAN_0_INS_N	GPIO		1		1		1	1		1
FAN_1_INS_N	GPIO		1		1		1	1		1
FAN_2_INS_N	GPIO		1		1		1	1		1
FAN_3_INS_N	GPIO		1		1		1	1		1
I2C_BMC_A_COMP_A	I2C	2								
I2C_BMC_A_EXP_A	I2C	2				2				
I2C_BMC_A_EXP_B	I2C	2						2	2	
I2C_BMC_A_MISC	I2C	2								
I2C_BMC_B_COMP_B	I2C			2						
I2C_BMC_B_EXP_A	I2C			2		2				
I2C_BMC_B_EXP_B	I2C			2				2	2	
I2C_BMC_B_MISC	I2C			2						
I2C_CLIP	I2C					2		2	2	
I2C_DPB_A	I2C	2				2		2		
I2C_DPB_B	I2C			2				2	2	
I2C_DRIVE_A_FLT_LED	I2C					2				
I2C_DRIVE_A_INS	I2C					2				
I2C_DRIVE_A_PWR	I2C					2				
I2C_DRIVE_B_FLT_LED	I2C								2	
I2C_DRIVE_B_INS	I2C								2	
I2C_DRIVE_B_PWR	I2C								2	
I2C_SCC_A	I2C	2				2				
I2C_SCC_B	I2C			2				2	2	
IOM_A_INS_N	GPIO	1			1		1	1		1
IOM_A_SLOT_ID_0	STRAP	1								
IOM_A_SLOT_ID_1	STRAP	1								
IOM_B_INS_N	GPIO		1	1			1	1		1
IOM_B_SLOT_ID_0	STRAP			1						
IOM_B_SLOT_ID_1	STRAP			1						
P12V_IOM_A	PWR	5								
P12V_IOM_B	PWR			5						
PCIE_COMP_A_TO_IOM_A_[8:23]_DP/N	PCIe (Diff.)	32								
PCIE_COMP_A_TO_IOM_A_CLK_[2:4]_DP/N	PCIe (Diff.)	6								
PCIE_COMP_A_TO_IOM_A_RST_[2:4]	PCIe	3								
PCIE_COMP_A_TO_SCC_A_CLK_0_DP/N	PCIe (Diff.)					2				
PCIE_COMP_A_TO_SCC_A_RST_0	PCIe					1				
PCIE_COMP_B_TO_IOM_B_[8:23]_DP/N	PCIe (Diff.)			32						
PCIE_COMP_B_TO_IOM_B_CLK_[2:4]_DP/N	PCIe (Diff.)			6						
PCIE_COMP_B_TO_IOM_B_RST_[2:4]	PCIe			3						
PCIE_COMP_B_TO_SCC_B_CLK_0_DP/N	PCIe (Diff.)							2	2	
PCIE_COMP_B_TO_SCC_B_RST_0	PCIe							1	1	
PCIE_IOM_A_TO_COMP_A_[8:23]_DP/N	PCIe (Diff.)	32								
PCIE_IOM_B_TO_COMP_B_[8:23]_DP/N	PCIe (Diff.)			32						
PWM_BMC_A_ZONE_C	PWM	1						1		

Signal Name (DPB Ref)	Signal Type	IOM-A	IOM-A GPIO Exp.	IOM-B	IOM-B GPIO Exp.	SCC-A	SCC-A GPIO Exp.	DPB	SCC-B	SCC-B GPIO Exp.
PWM_BMC_A_ZONE_D	PWM	1						1		
PWM_BMC_B_ZONE_C	PWM			1				1		
PWM_BMC_B_ZONE_D	PWM			1				1		
PWM_SCC_A_ZONE_C	PWM					1		1		
PWM_SCC_A_ZONE_D	PWM					1		1		
PWM_SCC_B_ZONE_C	PWM								1	
PWM_SCC_B_ZONE_D	PWM								1	
SCC_A_FULL_PGOOD	GPIO		1			1				
SCC_A_FULL_PWR_EN	GPIO	1		1		1				
SCC_A_HEARTBEAT	PWM	1		1		1		1	1	
SCC_A_INS_N	GPIO		1		1	1		1		1
SCC_A_SLOT_ID_0	STRAP					1				
SCC_A_SLOT_ID_1	STRAP					1				
SCC_A_STBY_PGOOD	GPIO		1			1				
SCC_A_STBY_PWR_EN	GPIO	1				1				
SCC_A_TYPE_0	GPIO		1	1		1		1		
SCC_A_TYPE_1	GPIO		1			1				
SCC_A_TYPE_2	GPIO		1			1				
SCC_A_TYPE_3	GPIO		1			1				
SCC_B_FULL_PGOOD	GPIO				1			1	1	
SCC_B_FULL_PWR_EN	GPIO	1		1				1	1	
SCC_B_HEARTBEAT	PWM	1		1		1		1	1	
SCC_B_INS_N	GPIO		1		1		1	1	1	
SCC_B_SLOT_ID_0	STRAP								1	
SCC_B_SLOT_ID_1	STRAP								1	
SCC_B_STBY_PGOOD	GPIO				1			1	1	
SCC_B_STBY_PWR_EN	GPIO			1				1	1	
SCC_B_TYPE_0	GPIO	1				1		1	1	
SCC_B_TYPE_1	GPIO					1		1	1	
SCC_B_TYPE_2	GPIO					1		1	1	
SCC_B_TYPE_3	GPIO					1		1	1	
SYS_A_RESET_N	GPIO	1				1				
SYS_B_RESET_N	GPIO			1				1	1	
SYS_PWR_LED_A	GPIO	1				1				
SYS_PWR_LED_B	GPIO			1				1	1	
UART_COMP_A	GPIO	2								
UART_COMP_B	GPIO			2						
UART_EXP_A	GPIO					2				
UART_EXP_B	GPIO							2	2	
UART_IOC_A	GPIO					2				
UART_IOC_B	GPIO							2	2	
UART_SDB_A	GPIO	2				2				
UART_SDB_B	GPIO			2				2	2	
USB_COMP_A	Diff. (85 Ω)	2								
USB_COMP_B	Diff. (85 Ω)			2						

6.2.11.3 Board net naming reference

The table below identifies how connected nets are represented or named differently on various boards, as well as the purpose of those specific signals. This table only includes signals passing through connectors; leveraging this, the signal as it is referred to on the DPB is used as the reference when referring to local or on-board signals. For example, the net "BMC_A_EXP_A_SPARE_0" is called just that on the DPB, "EXP_SPARE_0" on the IOM, and "BMC_SPARE_0" on the SCC.

Table 14. Net naming cross-reference

Signal Name (DPB Ref)	Signal Type	IOM-A	IOM-B	SCC-A	SCC-B	Notes
12V_IOM	PWR	12V_IOM	12V_IOM			12V power input to IOM
BMC_A_EXP_A_RESET_N	GPIO	BMC_TO_EXP_RESET_N		BMC_TO_EXP_RESET_N		Direct signal for BMC to reset SAS expander
BMC_A_EXP_A_SPARE_0	GPIO	EXP_SPARE_0		BMC_SPARE_0		Extra GPIO between IOM_A and SCC_A
BMC_A_EXP_A_SPARE_1	GPIO	EXP_SPARE_1		BMC_SPARE_1		Extra GPIO between IOM_A and SCC_A
BMC_A_HEARTBEAT	PWM	BMC_LOC_HEARTBEAT	BMC_RMT_HEARTBEAT	BMC_LOC_HEARTBEAT	BMC_RMT_HEARTBEAT	BMC_A heartbeat output
BMC_A_MISC_ALERT	GPIO	DPB_MISC_ALERT				
BMC_A_RESET_N	GPIO	RESET_N				
BMC_B_EXP_B_RESET_N	GPIO		BMC_TO_EXP_RESET_N		BMC_TO_EXP_RESET_N	Direct signal for BMC to reset SAS expander
BMC_B_EXP_B_SPARE_0	GPIO		EXP_SPARE_0		BMC_SPARE_0	Extra GPIO between IOM_B and SCC_B
BMC_B_EXP_B_SPARE_1	GPIO		EXP_SPARE_1		BMC_SPARE_1	Extra GPIO between IOM_B and SCC_B
BMC_B_HEARTBEAT	PWM	BMC_RMT_HEARTBEAT	BMC_LOC_HEARTBEAT	BMC_RMT_HEARTBEAT	BMC_LOC_HEARTBEAT	BMC_B heartbeat output
BMC_B_MISC_ALERT	GPIO		DPB_MISC_ALERT			
BMC_B_RESET_N	GPIO		RESET_N			
COMP_A_BMC_A_ALERT	GPIO	COMP_ALERT				
COMP_A_BMC_A_SPARE_0	GPIO	COMP_SPARE_0				Extra GPIO between IOM_A and COMP_A
COMP_A_BMC_A_SPARE_1	GPIO	COMP_SPARE_1				Extra GPIO between IOM_A and COMP_A
COMP_A_EXP_A_SPARE_0	GPIO			COMP_SPARE_0		Extra GPIO between SCC_A and COMP_A
COMP_A_FAST_THROTTLE_N	GPIO	COMP_FAST_THROTTLE_N				HOTPROC-equivalent signal to COMP_A
COMP_A_INS_N	GPIO	(expander)				Primary compute module insertion signal
COMP_A_PGOOD	GPIO	(expander)				
COMP_A_POWER_FAIL_N	GPIO	COMP_POWER_FAIL_N				Compute power failure signal
COMP_A_PWR_BTN_N	GPIO	COMP_PWR_BTN_N				Power button for COMP_B
COMP_A_PWR_EN	GPIO	COMP_PWR_EN				

Signal Name (DPB Ref)	Signal Type	IOM-A	IOM-B	SCC-A	SCC-B	Notes
COMP_B_ BMC_B_ ALERT	GPIO		COMP_ALERT			
COMP_B_ BMC_B_ SPARE_0	GPIO		COMP_SPARE_ 0			Extra GPIO between IOM_B and COMP_B
COMP_B_ BMC_B_ SPARE_1	GPIO		COMP_SPARE_ 1			Extra GPIO between IOM_B and COMP_B
COMP_B_EXP _B_SPARE_0	GPIO				COMP_SPARE_ 0	Extra GPIO between SCC_B and COMP_B
COMP_B_ FAST_ THROTTLE_N	GPIO		COMP_FAST_ THROTTLE_N			HOTPROC-equivalent signal to COMP_B
COMP_B_INS _N	GPIO		(expander)			Primary compute module insertion signal
COMP_B_ PGOOD	GPIO		(expander)			
COMP_B_ POWER_FAIL _N	GPIO		COMP_ POWER_FAIL _N			Compute power failure signal
COMP_B_ PWR_BTN_N	GPIO		COMP_PWR_ BTN_N			Power button for COMP_B
COMP_B_ PWR_EN	GPIO		COMP_PWR_ EN			
DRAWER_ CLOSED_N	GPIO	(expander)	(expander)	(expander)	(expander)	Box drawer sensor input
DRIVE_A_ [0:35]_ACT	GPIO			DRIVE_[0:35]_ ACT		Drive activity GPIOs
DRIVE_B_ [0:35]_ACT	GPIO				DRIVE_[0:35]_ ACT	Drive activity GPIOs
DRIVE_ INSERT_ ALERT_A	GPIO			DRIVE_INSERT_ ALERT_N		Drive and Module insert interrupt (from GPIO expander)
DRIVE_ INSERT_ ALERT_B	GPIO				DRIVE_INSERT_ ALERT_N	Drive and Module insert interrupt (from GPIO expander)
ENCL_FAULT _LED_A_N	GPIO	ENCL_FAULT_ LED_N		ENCL_FAULT_ LED_N		
ENCL_FAULT _LED_B_N	GPIO		ENCL_FAULT_ LED_N		ENCL_FAULT_ LED_N	
FAN_0_INS_N	GPIO	(expander)	(expander)	(expander)	(expander)	FAN_0 insertion signal
FAN_1_INS_N	GPIO	(expander)	(expander)	(expander)	(expander)	FAN_1 insertion signal
FAN_2_INS_N	GPIO	(expander)	(expander)	(expander)	(expander)	FAN_2 insertion signal
FAN_3_INS_N	GPIO	(expander)	(expander)	(expander)	(expander)	FAN_3 insertion signal
I2C_BMC_A_ COMP_A	I2C	I2C_COMP				BMC_A to COMP_A direct I2C bus
I2C_BMC_A_ EXP_A	I2C	I2C_EXP_LOC		I2C_BMC_LOC		BMC_A to EXP_A direct I2C bus
I2C_BMC_A_ EXP_B	I2C	I2C_EXP_RMT			I2C_BMC_RMT	BMC_A to EXP_B direct I2C bus
I2C_BMC_A_ MISC	I2C	I2C_DPB_MISC				
I2C_BMC_B_ COMP_B	I2C		I2C_COMP			BMC_B to COMP_B direct I2C bus
I2C_BMC_B_ EXP_A	I2C		I2C_EXP_RMT	I2C_BMC_RMT		BMC_B to EXP_A direct I2C bus
I2C_BMC_B_ EXP_B	I2C		I2C_EXP_LOC		I2C_BMC_LOC	BMC_B to EXP_B direct I2C bus
I2C_BMC_B_ MISC	I2C		I2C_DPB_MISC			

Signal Name (DPB Ref)	Signal Type	IOM-A	IOM-B	SCC-A	SCC-B	Notes
I2C_CLIP	I2C			I2C_CLIP	I2C_CLIP	I2C bus for P12V_CLIP HSC
I2C_DPB_A	I2C	I2C_DPB		I2C_DPB		I2C bus for devices on DPB_A
I2C_DPB_B	I2C		I2C_DPB		I2C_DPB	I2C bus for devices on DPB_B
I2C_DRIVE_A_FLT_LED	I2C			I2C_DRIVE_FLT_LED		I2C bus for drive fault LED (GPIO expander)
I2C_DRIVE_A_INS	I2C			I2C_DRIVE_INS		I2C bus for drive insertion (GPIO expander)
I2C_DRIVE_A_PWR	I2C			I2C_DRIVE_PWR		I2C bus for drive power (GPIO expander)
I2C_DRIVE_B_FLT_LED	I2C				I2C_DRIVE_FLT_LED	I2C bus for drive fault LED (GPIO expander)
I2C_DRIVE_B_INS	I2C				I2C_DRIVE_INS	I2C bus for drive insertion (GPIO expander)
I2C_DRIVE_B_PWR	I2C				I2C_DRIVE_PWR	I2C bus for drive power (GPIO expander)
I2C_SCC_A	I2C	I2C_SCC		I2C_SCC		I2C bus for devices on SCC_A
I2C_SCC_B	I2C		I2C_SCC		I2C_SCC	I2C bus for devices on SCC_B
IOM_A_INS_N	GPIO	IOM_LOC_INS_N	(expander)	(expander)	(expander)	IOM_A insertion signal
IOM_A_SLOT_ID_0	STRAP	SLOT_ID_0				IOM Slot ID
IOM_A_SLOT_ID_1	STRAP	SLOT_ID_1				IOM Slot ID
IOM_B_INS_N	GPIO	(expander)	IOM_LOC_INS_N	(expander)	(expander)	IOM_B insertion signal
IOM_B_SLOT_ID_0	STRAP		SLOT_ID_0			IOM Slot ID
IOM_B_SLOT_ID_1	STRAP		SLOT_ID_1			IOM Slot ID
PCIE_COMP_A_TO_IOM_A_CLK_[2:4]_DP/N	PCIe	PCIE_COMP_TO_IOM_CLK_[2:4]_DP/N				Compute PCIe Clock outputs to IOM
PCIE_COMP_A_TO_IOM_A_RST_[2:4]	PCIe	PCIE_COMP_TO_IOM_RST_[2:4]				Compute PCIe Reset outputs to IOM
PCIE_COMP_A_TO_SCC_A_CLK_0_DP/N	PCIe			PCIE_COMP_TO_SCC_CLK_0_DP/N		Compute PCIe Clock output to SCC
PCIE_COMP_A_TO_SCC_A_RST_0	PCIe			PCIE_COMP_TO_SCC_RST_0		Compute PCIe Reset output to SCC
PCIE_COMP_B_TO_IOM_B_CLK_[2:4]_DP/N	PCIe		PCIE_COMP_TO_IOM_CLK_[2:4]_DP/N			Compute PCIe Clock outputs to IOM
PCIE_COMP_B_TO_IOM_B_RST_[2:4]	PCIe		PCIE_COMP_TO_IOM_RST_[2:4]			Compute PCIe Reset outputs to IOM
PCIE_COMP_B_TO_SCC_B_CLK_0_DP/N	PCIe				PCIE_COMP_TO_SCC_CLK_0_DP/N	Compute PCIe Clock output to SCC
PCIE_COMP_	PCIe				PCIE_COMP_	Compute PCIe Reset

Signal Name (DPB Ref)	Signal Type	IOM-A	IOM-B	SCC-A	SCC-B	Notes
B_TO_SCC_B_RST_0					TO_SCC_RST_0	output to SCC
PWM_BMC_A_ZONE_C	PWM	PWM_OUT_ZONE_C				BMC_A fan control PWM output
PWM_BMC_A_ZONE_D	PWM	PWM_OUT_ZONE_D				
PWM_BMC_B_ZONE_C	PWM		PWM_OUT_ZONE_C			BMC_B fan control PWM output
PWM_BMC_B_ZONE_D	PWM		PWM_OUT_ZONE_D			
PWM_SCC_A_ZONE_C	PWM			PWM_OUT_ZONE_C		SCC_A fan control PWM output
PWM_SCC_A_ZONE_D	PWM			PWM_OUT_ZONE_D		
PWM_SCC_B_ZONE_C	PWM				PWM_OUT_ZONE_C	SCC_B fan control PWM output
PWM_SCC_B_ZONE_D	PWM				PWM_OUT_ZONE_D	
SCC_A_FULL_PGOOD	GPIO	(expander)		SCC_FULL_PGOOD		
SCC_A_FULL_PWR_EN	GPIO	SCC_LOC_FULL_PWR_EN	SCC_RMT_FULL_PWR_EN	SCC_FULL_PWR_EN		
SCC_A_HEARTBEAT	PWM	SCC_LOC_HEARTBEAT	SCC_RMT_HEARTBEAT	SCC_LOC_HEARTBEAT	SCC_RMT_HEARTBEAT	SCC_A Heartbeat output
SCC_A_INS_N	GPIO	(expander)	(expander)	SCC_LOC_INS_N	(expander)	SCC_A insertion signal
SCC_A_SLOT_ID_0	STRAP			SLOT_ID_0		SCC Slot ID
SCC_A_SLOT_ID_1	STRAP			SLOT_ID_1		SCC Slot ID
SCC_A_STBY_PGOOD	GPIO	(expander)		SCC_STBY_PGOOD		
SCC_A_STBY_PWR_EN	GPIO	SCC_LOC_STBY_PWR_EN		SCC_STBY_PWR_EN		
SCC_A_TYPE_0	GPIO	(expander)	SCC_RMT_TYPE_0	SCC_TYPE_0		SCC Type Identifier output (JBOD indicator bit)
SCC_A_TYPE_1	GPIO	(expander)		SCC_TYPE_1		SCC Type Identifier output
SCC_A_TYPE_2	GPIO	(expander)		SCC_TYPE_2		SCC Type Identifier output
SCC_A_TYPE_3	GPIO	(expander)		SCC_TYPE_3		SCC Type Identifier output
SCC_B_FULL_PGOOD	GPIO		(expander)		SCC_FULL_PGOOD	
SCC_B_FULL_PWR_EN	GPIO	SCC_RMT_FULL_PWR_EN	SCC_LOC_FULL_PWR_EN		SCC_FULL_PWR_EN	
SCC_B_HEARTBEAT	PWM	SCC_RMT_HEARTBEAT	SCC_LOC_HEARTBEAT	SCC_RMT_HEARTBEAT	SCC_LOC_HEARTBEAT	SCC_B Heartbeat output
SCC_B_INS_N	GPIO	(expander)	(expander)	(expander)	SCC_LOC_INS_N	SCC_B insertion signal
SCC_B_SLOT_ID_0	STRAP				SLOT_ID_0	SCC Slot ID
SCC_B_SLOT_ID_1	STRAP				SLOT_ID_1	SCC Slot ID
SCC_B_STBY_PGOOD	GPIO		(expander)		SCC_STBY_PGOOD	
SCC_B_STBY_PWR_EN	GPIO		SCC_LOC_STBY_PWR_EN		SCC_STBY_PWR_EN	
SCC_B_TYPE_0	GPIO	SCC_RMT_TYPE_0	(expander)		SCC_TYPE_0	SCC Type Identifier output (JBOD indicator bit)
SCC_B_TYPE_1	GPIO		(expander)		SCC_TYPE_1	SCC Type Identifier output

Signal Name (DPB Ref)	Signal Type	IOM-A	IOM-B	SCC-A	SCC-B	Notes
SCC_B_TYPE_2	GPIO		(expander)		SCC_TYPE_2	SCC Type Identifier output
SCC_B_TYPE_3	GPIO		(expander)		SCC_TYPE_3	SCC Type Identifier output
SYS_A_RESET_N	GPIO	SYS_RESET_N		SYS_RESET_N		Release all devices from RESET
SYS_B_RESET_N	GPIO		SYS_RESET_N		SYS_RESET_N	Release all devices from RESET
SYS_PWR_LED_A		SYS_PWR_LED		SYS_PWR_LED		
SYS_PWR_LED_B			SYS_PWR_LED		SYS_PWR_LED	
UART_COMP_A	GPIO	UART_COMP				UART from IOM_A to COMP_A
UART_COMP_B	GPIO		UART_COMP			UART from IOM_B to COMP_B
UART_EXP_A	GPIO			UART_EXP		UART from EXP_A to USB 3.0 debug header
UART_EXP_B	GPIO				UART_EXP	UART from EXP_B to USB 3.0 debug header
UART_IOC_A	GPIO			UART_IOC		UART from IOC_A to USB 3.0 debug header
UART_IOC_B	GPIO				UART_IOC	UART from IOC_B to USB 3.0 debug header
UART_SDB_A	GPIO	UART_SDB		UART_SDB		
UART_SDB_B	GPIO		UART_SDB		UART_SDB	
USB_COMP_A	GPIO	USB_COMP				COMP_A USB for USB 3.0 connector
USB_COMP_B	GPIO		USB_COMP			COMP_B USB for USB 3.0 connector

6.2.11.4 High-speed signal naming reference

The table below shows all signal names for SAS- and PCIe-related signal on a per-board basis.

Table 15. PCIe and SAS signal naming

Board Name	Function	Source	Destination	Net Name
SCC	SAS	SCC_EXP	HDD	PHY_SCC_TO_DPB_[0:35]_DP/N [TX] PHY_DPB_TO_SCC_[0:35]_DP/N [RX]
		SCC_EXP	Internal Connector	PHY_EXP_TO_CONN_[0:3]_DP/N [TX] PHY_CONN_TO_EXP_[0:3]_DP/N [RX]
	PCIe	COMP_A/B	SCC_IOC	PCIE_SCC_TO_COMP_[0:7]_DP/N [TX] PCIE_COMP_TO_SCC_[0:7]_DP/N [RX]
	PCIe Clock	COMP_A/B	SCC_IOC	PCIE_COMP_TO_SCC_CLK_0_DP/N
	PCIe Reset	COMP_A/B	SCC_IOC	PCIE_COMP_TO_SCC_RST_0
DPB-A (Front DPB)	SAS	SCC_A_EXP	HDD_A	PHY_DRV_A_TO_SCC_A_[0:35]_DP/N [TX] PHY_SCC_A_TO_DRV_A_[0:35]_DP/N [RX]
	PCIe	COMP_A/B	SCC_A/B_IOC	PCIE_COMP_A/B_TO_SCC_A/B_[0:7]_DP/N [TX] PCIE_SCC_A/B_TO_COMP_A/B_[0:7]_DP/N [RX]
		COMP_A/B	IOM_A/B_IOC/M.2	PCIE_COMP_A/B_TO_IOM_A/B_[8:15]_DP/N [TX] PCIE_IOM_A/B_TO_COMP_A/B_[8:15]_DP/N [RX]
		COMP_A/B	IOM_A/B_OCP	PCIE_COMP_A/B_TO_IOM_A/B_[16:23]_DP/N [TX] PCIE_IOM_A/B_TO_COMP_A/B_[16:23]_DP/N [RX]
	PCIe Clock	COMP_A/B	SCC_A/B_IOC	PCIE_COMP_A/B_TO_SCC_A/B_CLK_0_DP/N
		COMP_A/B	IOM_A/B_IOC/M.2	PCIE_COMP_A/B_TO_IOM_A/B_CLK_[2:3]_DP/N
		COMP_A/B	IOM_A/B_OCP	PCIE_COMP_A/B_TO_IOM_A/B_CLK_4_DP/N
	PCIe Reset	COMP_A/B	SCC_A/B_IOC	PCIE_COMP_A/B_TO_SCC_A/B_RST_0
		COMP_A/B	IOM_A/B_IOC/M.2	PCIE_COMP_A/B_TO_IOM_A/B_RST_[2:3]
		COMP_A/B	IOM_A/B_OCP	PCIE_COMP_A/B_TO_IOM_A/B_RST_4
DPB-B (Rear DPB)	SAS	SCC_B_EXP	HDD_B	PHY_SCC_B_TO_DRV_B_[0:35]_DP/N [RX] PHY_DRV_B_TO_SCC_B_[0:35]_DP/N [TX]
	PCIe	COMP_B	SCC_B_IOC	PCIE_COMP_B_TO_SCC_B_[0:7]_DP/N [TX] PCIE_SCC_B_TO_COMP_B_[0:7]_DP/N [RX]
	PCIe Clock	COMP_B	SCC_B_IOC	PCIE_COMP_B_TO_SCC_B_CLK_0_DP/N
	PCIe Reset	COMP_B	SCC_B_IOC	PCIE_COMP_B_TO_SCC_B_RST_0
IOM	SAS	IOM_IOC	External Connector A	PHY_IOC_TO_CON_A_[0:3]_DP/N [TX] PHY_CON_A_TO_IOC_[0:3]_DP/N [RX]
			External Connector B	PHY_IOC_TO_CON_B_[0:3]_DP/N [TX] PHY_CON_B_TO_IOC_[0:3]_DP/N [RX]
	PCIe	COMP_A/B	IOM_IOC/M.2	PCIE_COMP_TO_IOM_[8:15]_DP/N [RX] PCIE_IOM_TO_COMP_[8:15]_DP/N [TX]
		COMP_A/B	IOM_OCP	PCIE_COMP_TO_IOM_[16:23]_DP/N [RX] PCIE_IOM_TO_COMP_[16:23]_DP/N [TX]
	PCIe Clock	COMP_A/B	IOM_IOC/M.2	PCIE_COMP_TO_IOM_CLK_[2:3]_DP/N
		COMP_A/B	IOM_OCP	PCIE_COMP_TO_IOM_CLK_4_DP/N
	PCIe Reset	COMP_A/B	IOM_IOC/M.2	PCIE_COMP_TO_IOM_RST_[2:3]
		COMP_A/B	IOM_OCP	PCIE_COMP_TO_IOM_RST_4

6.3 Signal integrity requirements

6.3.1 SAS/SATA

All drive slots must be capable of 12Gb and 6Gb SAS, and tested to a BER of 1 in 10^{-15}. When testing SATA 6Gb, the BER compliance should be tested to a BER of 1 in 10^{-14}.

6.3.2 PCIe

All drive slots must be capable of PCIe Gen 3, and tested to a BER of 1 in $10^{-15.}$

6.4   ESD compliance

The Bryce Canyon Chassis shall be designed such that all ESD events that may occur while interacting with the buttons, LEDs and connectors accessible from the front of the chassis, will be handled gracefully. This will be implemented with appropriate ESD protection devices. This includes but is not limited to the nets interfacing with the power and reset buttons, the USB and UART signals on the debug headers, as well as all externally interfaced LEDs that do not go through a long light pipe that would isolate them from ESD events. These ESD protection devices must be placed on the PCB as close to the component as feasible, with the ground path to dissipate the ESD event routed as short as possible to the ground plane.

7 Power

7.1 Power topology
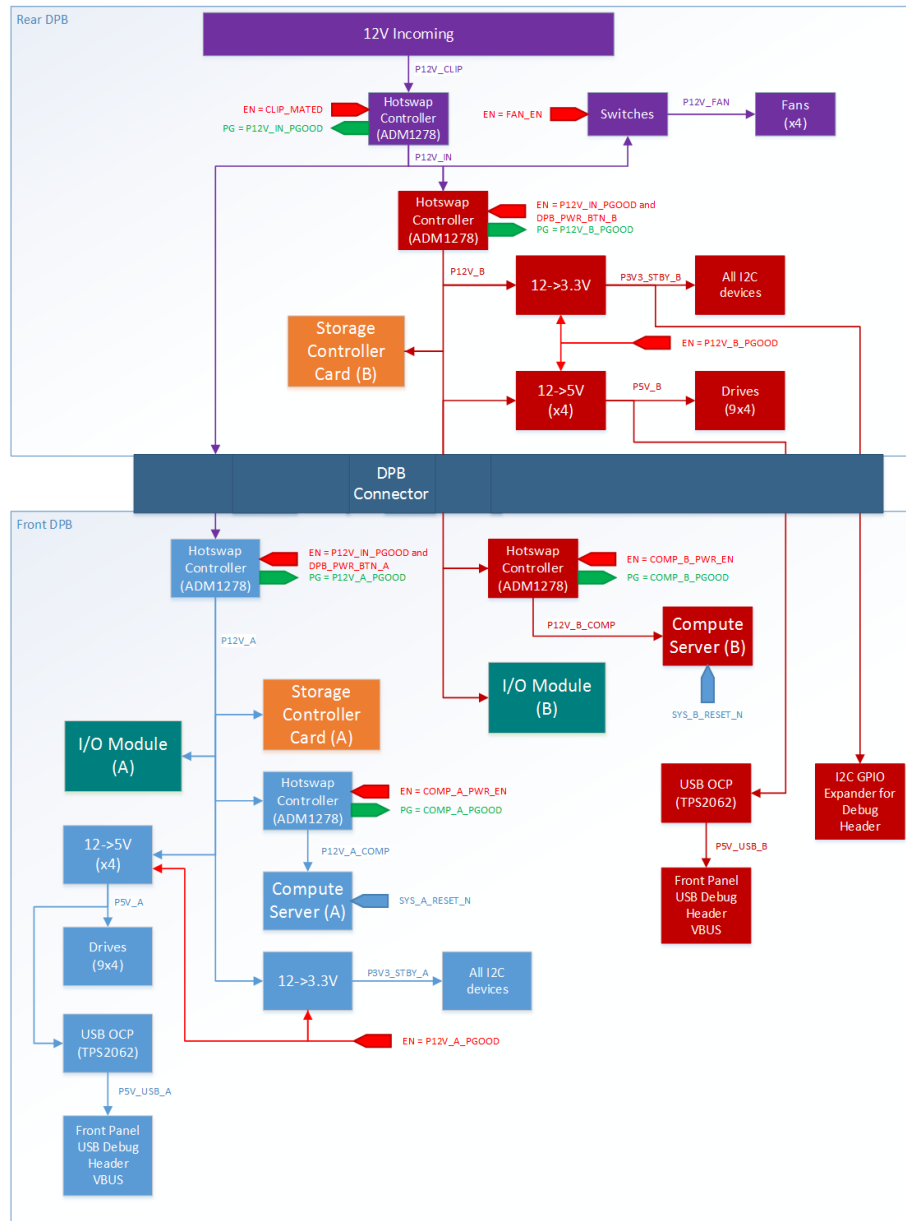
Figure 32. System power block diagram

Figure 32 shows the overall power topology of the system. The specific implementation in the SCC and IOM will be covered in later sections.

The power topology breaks the two logical domains into separate power domains, each of which are protected by a hot-swap controller. Isolating the "A" side power from the "B" side power reduces the chance of failures on one side propagating to the other.

Because the fans are supplied by a voltage rail common to both A/B sides, care must be taken such that hot-swap of the fans will not bring down the voltage to either A/B side.

7.2 System grounding topology

The grounding topology of the system shall be implemented in such a way that there is a singular signal ground entry and exit point from the entirety of the PCB assembly to chassis ground. This is done to prevent any possible ground loops from forming. This will be accomplished by electrically isolating all PCBs from connection points to the chassis. This includes all screw down points, clamped metal features, support walls, etc. The topology of this proposal is demonstrated below in Figure 33.
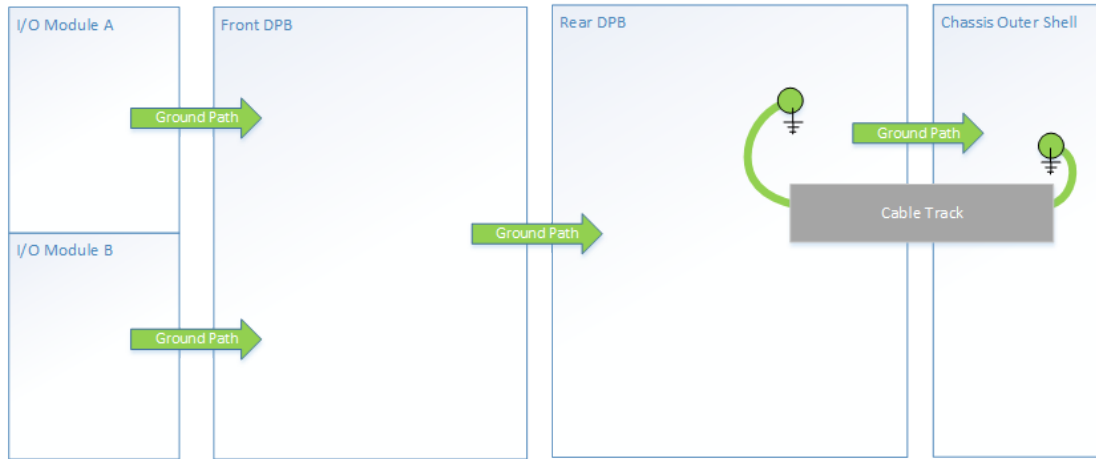
Figure 33 - System Grounding Topology

In order to have a good ground reference connection for the Bryce Canyon sliding drawer assembly, the grounding connection point will be implemented as a green 8 AWG wire screwed down to the Rear DPB, next to the power entry cable. (*In DVT, the power entry cable will be modified to allow the addition of the separate grounding wire to the connector.*) This ground wire will run through the cable track, and be connected to the outer shell of the Bryce Canyon chassis through a solidly connected bolt. The ground path will then travel through the chassis shell, into the support knives and into the rack. This additional grounding wire is necessary to provide a direct ground connection from the Bryce Canyon drawer to the outer chassis shell, and then to the Earth grounded rack. This is needed because although there are metal rails attaching the drawer to the shell of the chassis, the rails are an electrically and mechanically dynamic system that will not provide a consistent or continuous ground path due to the rolling ball bearings, nylon bearing ball carriers and insulating grease coating all contact points.

7.2.1 Mechanical Interface Isolation Distance

Robust grounding isolation must be maintained between the PCB assembly signal ground, and all mechanical interfaces between the PCB assembly and the chassis. This restriction applies to all *non-electrically connected* screw and bolt holes, key-hole features, PEM nuts and mounting points. In order to achieve this, a standard gap of 2mm, and an absolute minimum gap of 1mm, is necessary for all nets and planes on all layers of the PCB.

This gap extends radially from anywhere there will be an interface between mounting hardware and the PCBs. For anything contacting the top and/or bottom of the PCB, such as the maximum contact area of bolt head, brackets, nuts, etc., there shall be a 2mm isolation gap extending out of this maximum contact area. For any mechanical holes penetrating the PCB assemblies, the 2mm isolation gap extends outward radially from the hole on all layers of the PCB. These restrictions are illustrated in Figure 34.

White – Maximum Mechanical Contact / Hole Area
Red – No Routing Zone – 2mm
Green – Unrestricted PCB Area
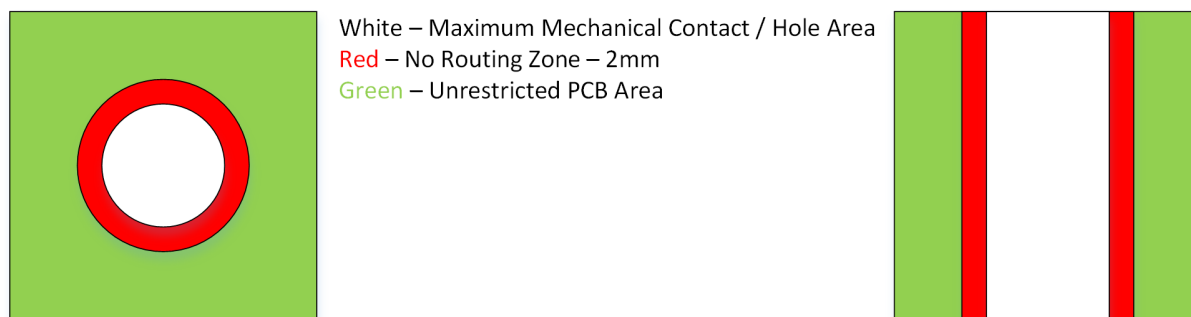
Figure 34 - Mechanical Isolation Keep-Out Area

7.2.2 Connector Housing Ground Topology

In order to further ensure that there is a singular signal ground connection point to the system/chassis ground, the outer shells off all connectors on the front of the Bryce Canyon chassis must be isolated from signal ground on all PCBs through the connection of an RC filter network. This network serves two purposes: first to electrically isolate the shells from chassis ground, second to provide a tuning mechanism in order to optimize and reduce EM emissions from the connectors. This will be implemented similar to Figure 35 below.
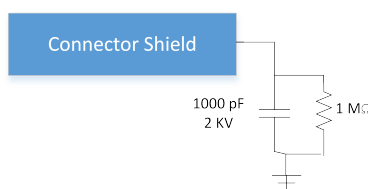
Figure 35 - Connector Shield Isolation

The values of the resistor used should be 1 MΩ, and the parallel capacitor should have a value of 1000 pF with a voltage rating on the order of 2 KV.

7.3   12V busbar cable input

To enable the drawer to remain powered while the drawer is extended, a power cable is routed between a busbar clip and the drive plane board. One end of this cable has an Open Rack v2 busbar clip, as detailed in the "Cubby: Three-bay shelf for Open Rack V2" specification[1]. The cables leading from the clip are to be terminated into a squeeze-to-release receptacle (P/N: TE 1600798-1, or equivalent), which mates with a vertical plug on the Rear Drive Plane Board. The cable construction should contain six (6) 8AWG high-flex wires, three used for 12V, and 3 for GND.

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[1] http://files.opencompute.org/oc/public.php?service=files&t=db28490bdd3afbff048dbcceae8d9f44
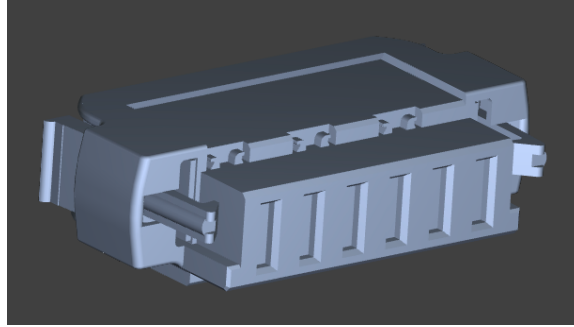
Figure 36. Squeeze-to-release receptacle for power

7.4 Drive power requirements

This section outlines the requirements of power supplies to the hard drives.

7.4.1 Staggered spin up requirements

The system must implement a staggered spin up of the hard drives. The spin up algorithm should spin up the drives as fast as possible, while keeping the total chassis power under 1200W. To do this, the drives will need to be spun up in groups. The first group can have many drives, due to plenty of power being available, but care needs to be taken not to draw too much from the onboard regulators.

7.4.2 Hot-swap requirements

The drives must be capable of being electrically hot-swapped.

7.4.3 5V conversion failure domains

To maintain failure domains at an acceptable size, no more than nine HDDs shall be present behind a single 5V conversion, unless there is evidence of a better cost model by having fewer HDDs per converter.

7.4.4 5V conversion loading requirements

The 5V conversion should be able to maintain regulation at both full-load, as well as no-load (when all drives are powered off, or not inserted; this is distinctly separate from idle).

7.5 Hot-swap requirements

In addition to drives, all compute servers, IOMs, and SCCs should be capable of electrical hot-swap. That is, each of these components should be able to remove without bringing down any voltage rails in the chassis. Furthermore, the overall chassis should be able to be plugged into a live busbar without drooping the main 12V rail of the rack. To achieve this, each hot-swappable component is protected by a hot-swap controller.

All hot-swap controllers must support the following features:

- Over current protection (OCP), and short circuit protection
- Over voltage protection (OVP)
- Under voltage protection (UVP)
- Power monitoring over I2C

As a reference, the ADM1278 part satisfies all of these requirements.

7.6 Fuses

<< TBD >>

7.7 I/O Module power topology
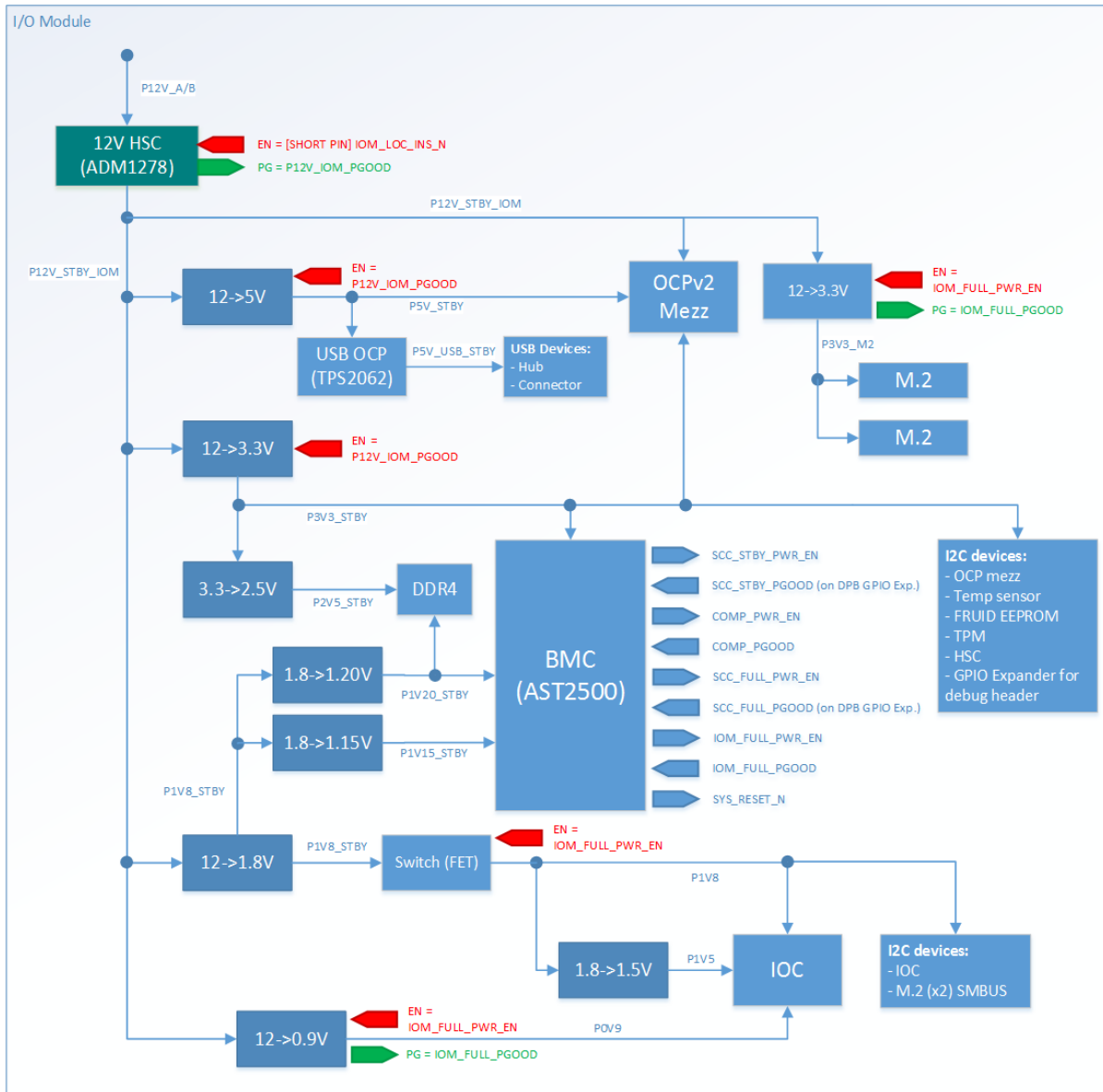
Figure 37. I/O Module power block diagram

The I/O Module power topology is designed such that the necessary standby devices (BMC, OCP Mezz) are always powered. Additionally, the necessary connected devices that support the BMC and OCP Mezz (e.g., FRUID EEPROM, TPM, etc.) must also be powered. This is why the majority of the voltage rails shown above are listed as standby. Low-side switches allow for the M.2s and the normal P3V3 to the OCP Mezz to be turned off in standby mode, despite being supplied by a standby rail.

Due to the partial power on scenarios introduced by standby mode, all I2C lines and GPIOs that are connected to a device that is not supplied by a standby rail (i.e., a device that is off while the system is in standby) must be disconnected from the system via a FET switch / CBT. This eliminates the possibility of leakage or erroneous logic levels being introduced by the unpowered device. In the above diagram, the IOC and the SMBUS lines of the M.2 are examples of such devices that would require this disconnection.

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7.8 Storage Controller Card power topology
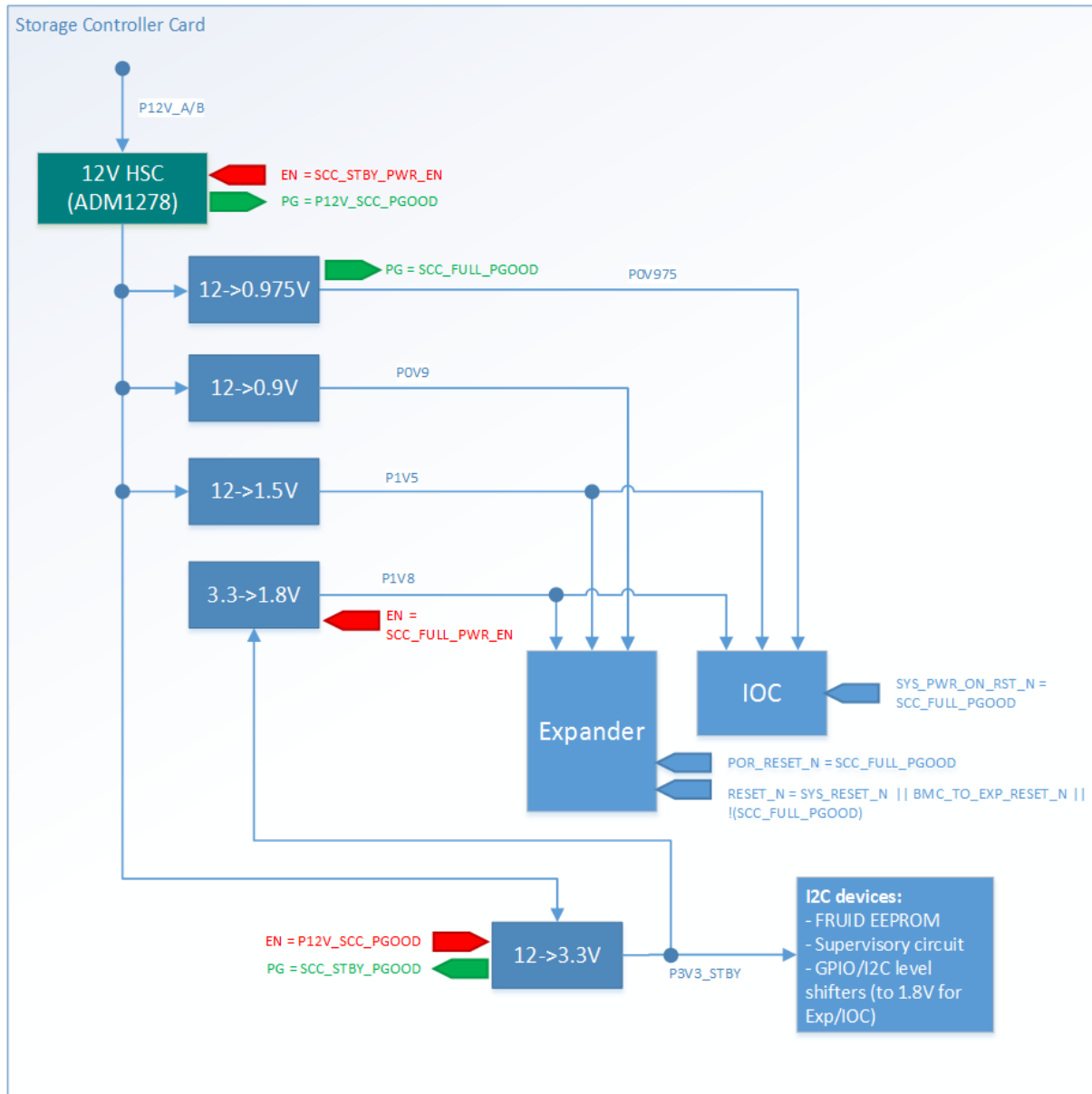
Figure 38. Storage Controller Card power block diagram

The Storage Controller Card power topology is designed similarly to that of the IO Module. In this case, the majority of the devices do not receive standby power; only the I2C devices that need to support the BMC in standby are powered (e.g., FRUID EEPROM).

Due to the partial power on scenarios introduced by standby mode, all I2C lines and GPIOs that are connected to a device that is not supplied by a standby rail (i.e., a device that is off while the system is in standby) must be disconnected from the system via a FET switch/CBT. This eliminates the possibility of leakage or erroneous logic levels being introduced by the unpowered device. In the above diagram, all I2C level shifters supplying the expander (which would also be unpowered) are examples of such devices that would require this disconnection.

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7.9 Power budget

7.9.1 System power budget

The system power budget is limited by the busbar clip ampacity rating, which is 150A.

7.9.2 SCC connector power budget

The power budget of the SCC connector is driven by the worst-case draw of the IOC and SAS Expanders, and the connector should be sized to support 5.5 A @ 12V.

7.9.3 IOM connector power budget

The power budget of the IOM connector is driven by the worst-case draw of M.2, BMC, and NIC, and the connector should be sized to support 3.7 A @ 12V.

7.9.4 DPB connector power budget

The DPB connector must support the A/B split power planes. The pins to support this split shall be allotted as per Table 16.

Table 16. DPB connector power requirements

DPB Connector	A Side	B Side
Power Requirement [W]	705.89	178.42
Current Requirement [A]	58.82	14.87

The power estimations that drive these requirements are shown in Table 17. Fans are not included as part of this estimation because they do not contribute to the DPB connector power requirement.

Table 17. Worst-case power per component

Component	A Side [W]	B Side [W]
Mono Lake	134.68	134.68
Drives	461.628	461.628
SCC	65.85	65.85
IOM	43.73	43.73
Fans	0	0
Total	705.89	705.89

7.10 Power sequencing

Refer to Section 6.2.10, "Reset and Power Enable," for the power sequence and reset signal coordination across the entire system.

8   Storage Controller Card

The function of the Storage Controller Card (SCC) is to connect the server module to the drives inside the chassis. The SCC is comprised of two main ASICS: the SAS IOC and SAS expander. The SCC is designed to function under directives from the BMC on the IOM, or in certain configurations, autonomously using the SAS expander.

8.1   Storage Controller Card configuration diagram
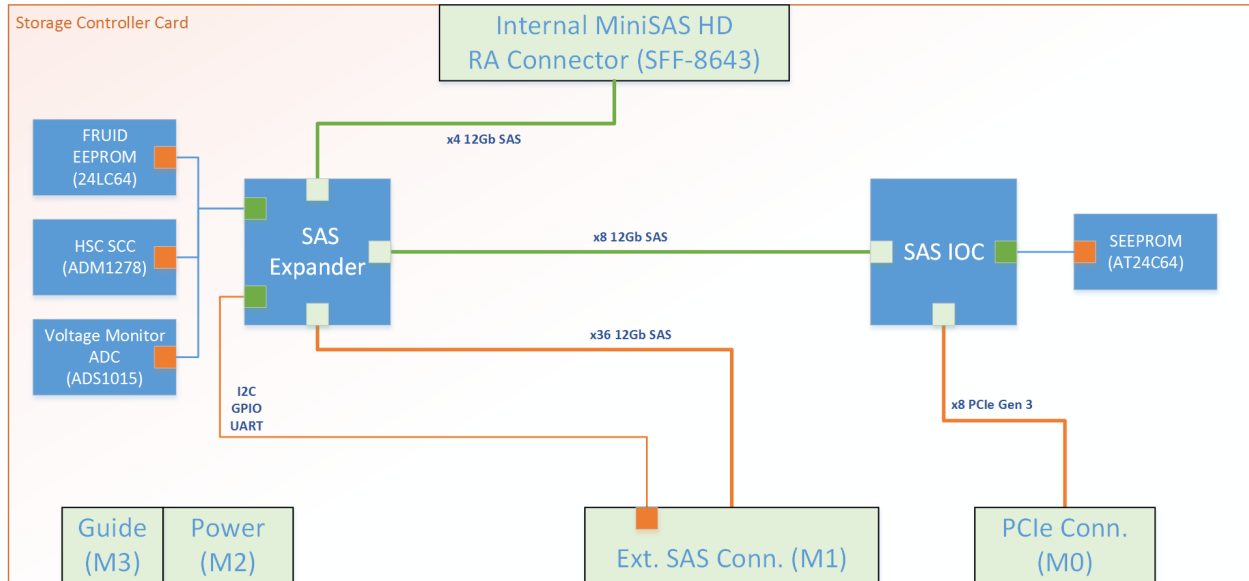
Figure 39. Storage Controller Card Integrated configuration block diagram
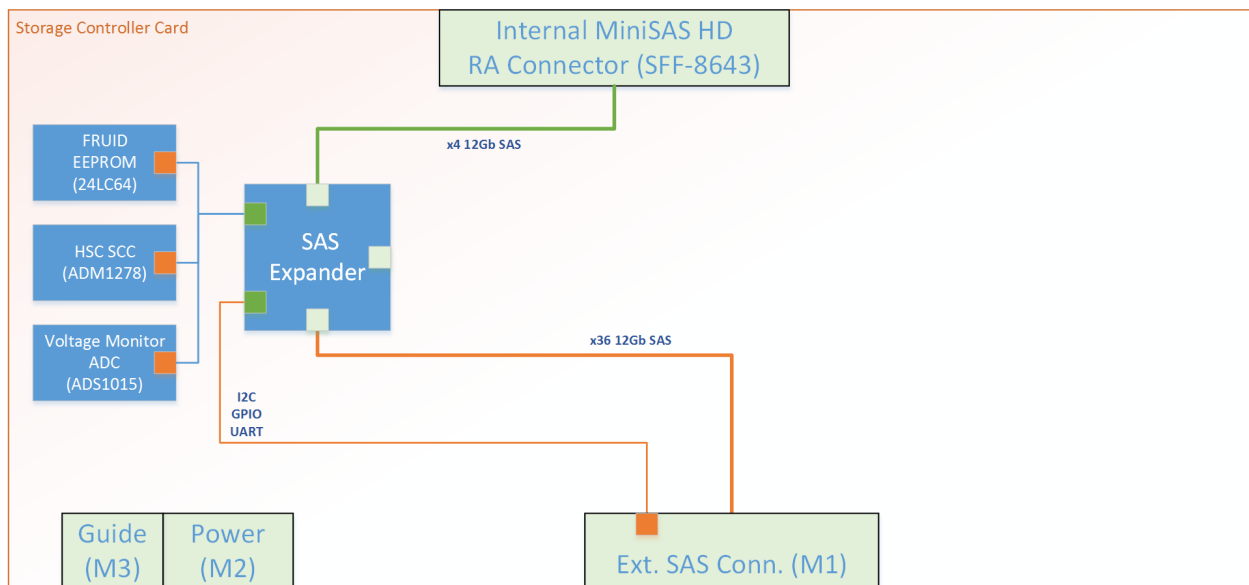
Figure 40. Storage Controller Card JBOD configuration block diagram

<show connector modules, M0 through M3 with descriptions. Put the detailed connector pinouts in a section at the end of spec to keep spec clean (see 10.1.3 below)>

8.2 Storage Controller Card configurations

The Storage Controller Card has different configurations options built into the design to accommodate the various Rack Types Bryce Canyon can serve. There are two main configurations of the SCC; in the first, the "Integrated" variant, the SCC is populated with the SAS expander and I/O Controller, as well as various sensors and chips throughout the board. In the second, the "JBOD" configuration, the IOC and PCIe connector are removed, as well as all IOC-related logic and chips (including the IOC SEEPROM). Power and Reset signaling is also modified; additional information on Reset and Power Enable differences between card variants can be found in section 6.2.10.

The SAS expander will also function as the main systems management controller in the JBOD configuration; additionally, in all configurations the expander will assume control of the chassis in the event of an I/O Module (BMC) failure. The health and present condition of the IOM BMC is determined from both a presence detector as well as a "Heartbeat" signal emanating from the BMC (see section 6.2.1).

It should be noted that any signals necessary for the SCC to function in the JBOD or Single configurations of Bryce Canyon should be routed through the SAS connector, not the PCIe connector, as the latter connector will be absent from the JBOD variant of the SCC. This includes all signals routed to the Remote-side IOM, SCC_FULL_PWR_EN (for fan switch enable), and any other relevant System Management signals; see sections 23.5, 23.6, and 6.2 for details. For reference, the reason the remote IOM signals are routed through the SAS connector is that the local IOM only ever utilizes the PCIe connector, as there is no Bryce Canyon configuration where a local IOM is installed for an SCC operating in JBOD mode, but there is a configuration with solely a remote IOM installed (Single config.; see section 3.4.2).

For each of the different configurations (Integrated and JBOD), four TYPE pins are strapped on the SCC to indicate to the system which variant (BOM population) of the SCC is inserted. Of the four pins, pin 0 is the JBOD-variant indicator pin. A table of the TYPE bit configurations can be found below.

Table 18. SCC TYPE bits

Variant	TYPE 0	TYPE 1	TYPE 2	TYPE 3
Integrated (Broadcom)	0	0	0	1
Integrated (Microsemi)	0	0	1	0
JBOD (Broadcom)	1	0	0	1
JBOD (Microsemi)	1	0	1	0

8.2.1 Connector Configurations

The SCC has multiple connector configurations, which allow the card to be used in all system configurations. The connectors populated are dependent on the system Type (IV/V/VII). For different connector configurations, refer to the table below.

Table 19. Storage Controller Card connector configuration

Configuration	Connectors on SCC-A	Connectors on SCC-B
Integrated SCC	M0, M1, M2, M3, INT	M0, M1, M2, M3, INT
JBOD SCC	M1, M2, M3, INT	M1, M2, M3, INT

8.2.2   Supplier variants

There is a Broadcom and a Microsemi version of the SCC, with the key component part numbers identified below.

Table 20. SCC IOC/EXP variants (by supplier)

Supplier	IOC P/N	Expander P/N
Broadcom	LSISAS3008 (Fury)	LSISAS3x48 (Cobra)
Microsemi	PM8068	PM8055 SXP 48x12G

8.3   Storage Controller Card Design

The SCC is designed to function in multiple Bryce Canyon configurations (Dual, Single, and JBOD), and thus the two different SCC variants (Integrated and JBOD) are designed with this in mind. These variant differences are seen heavily in the Reset and Power Enable and Device management signaling sections, but also in the Systems management section as a whole. As an example of the adaptability of the system, there are dedicated I2C lines from both IOMs to each SCC (so that both BMCs can communicate with either expander if necessary), as well as spare GPIO connections from both the BMC and Compute server.

8.3.1   Drive Management

Communication with all 36 drives occurs through the SAS expander; drive control signals are sent and received through 9 GPIO expanders (Insert, Power, and Fault), as well as directly by the SAS expander through the SAS connector (in the case of Drive Activity); refer to section 10.7 for additional details.

8.4   Storage Controller Card SAS PHY Mapping

The SAS PHY mapping is found in Table 21; the table will be fully updated once the boards are routed and optimal placement has been determined.

Table 21. SCC SAS PHY mapping

SCC SAS	Front DPB	LED	Rear DPB	LED	SCC SAS	Front DPB	LED	Rear DPB	LED
SAS-0	Drive-28	LED32	Drive-28	LED32	SAS-22	Drive-7	LED7	Drive-10	LED14
SAS-1	Drive-29	LED33	Drive-29	LED33	SAS-23	Drive-6	LED6	Drive-11	LED15
SAS-2	Drive-35	LED39	Drive-35	LED39	SAS-24	Drive-12	LED16	Drive-12	LED16
SAS-3	Drive-34	LED38	Drive-34	LED38	SAS-25	Drive-13	LED17	Drive-13	LED17
SAS-4	Drive-33	LED37	Drive-33	LED37	SAS-26	Drive-14	LED18	Drive-14	LED18
SAS-5	Drive-32	LED36	Drive-32	LED36	SAS-27	Drive-15	LED19	Drive-15	LED19
SAS-6	Drive-31	LED35	Drive-31	LED35	SAS-28	Drive-24	LED28	Drive-24	LED28
SAS-7	Drive-30	LED34	Drive-30	LED34	SAS-29	Drive-25	LED29	Drive-25	LED29
SAS-12	Drive-0	LED0	Drive-5	LED5	SAS-30	Drive-26	LED30	Drive-26	LED30
SAS-13	Drive-1	LED1	Drive-4	LED4	SAS-31	Drive-27	LED31	Drive-27	LED31
SAS-14	Drive-2	LED2	Drive-3	LED3	SAS-32	Drive-16	LED20	Drive-16	LED20
SAS-15	Drive-3	LED3	Drive-2	LED2	SAS-33	Drive-17	LED21	Drive-17	LED21
SAS-16	Drive-4	LED4	Drive-1	LED1	SAS-34	Drive-23	LED27	Drive-23	LED27
SAS-17	Drive-5	LED5	Drive-0	LED0	SAS-35	Drive-22	LED26	Drive-22	LED26
SAS-18	Drive-11	LED15	Drive-6	LED6	SAS-36	Drive-21	LED25	Drive-21	LED25
SAS-19	Drive-10	LED14	Drive-7	LED7	SAS-37	Drive-20	LED24	Drive-20	LED24
SAS-20	Drive-9	LED13	Drive-8	LED12	SAS-38	Drive-19	LED23	Drive-19	LED23
SAS-21	Drive-8	LED12	Drive-9	LED13	SAS-39	Drive-18	LED22	Drive-18	LED22

8.5   Storage Controller Card PCB

8.5.1   Important Components & Interfaces

The following figures detail the major functional blocks of the SCC, and their placement on the PCBs. This is detailed for both versions of the SCC, the Type 5 version with expander and IOC, as well as the JBOD version with just the expander – the IOC being un-populated on the PCB.
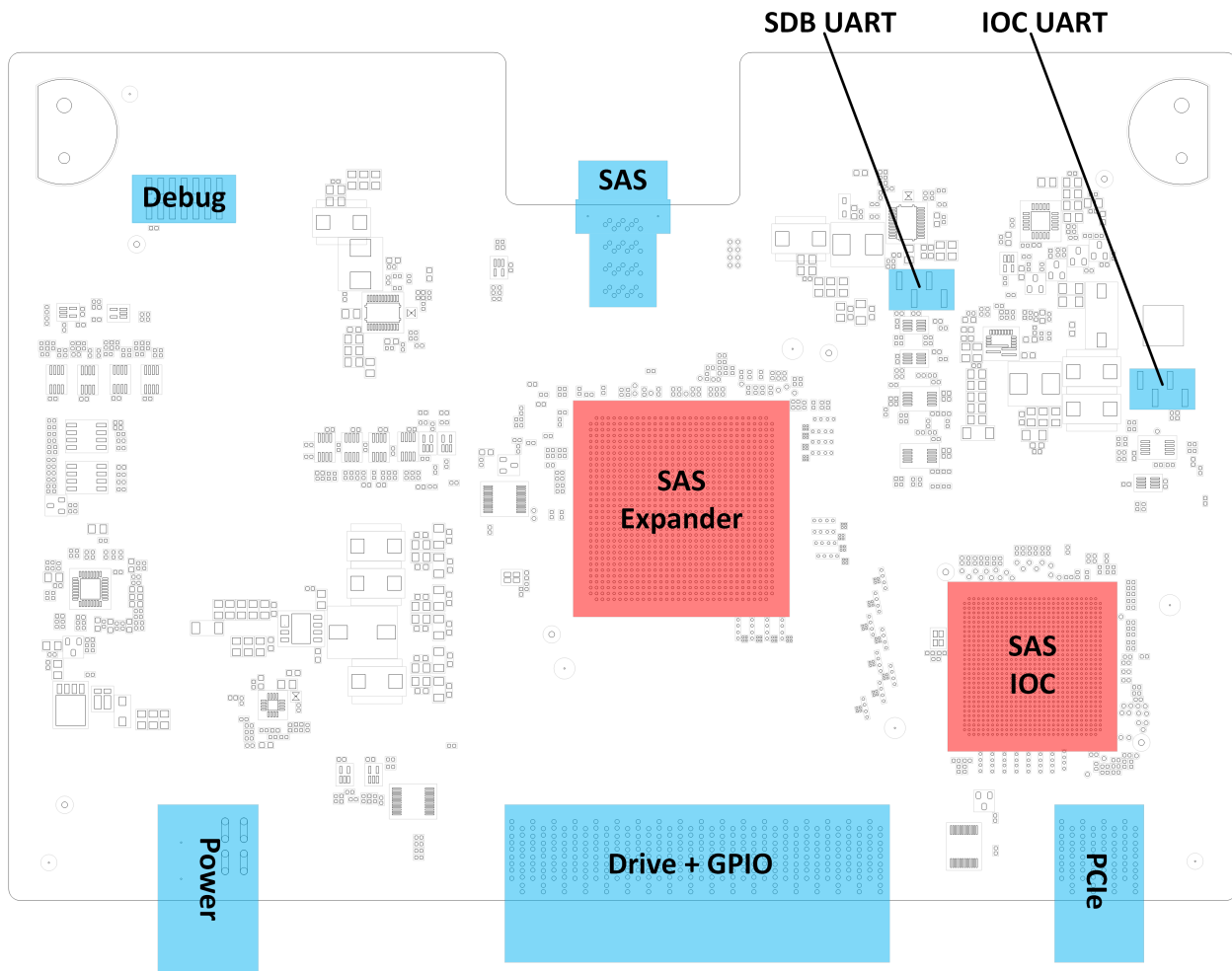
Figure 41 - SCC Type 5
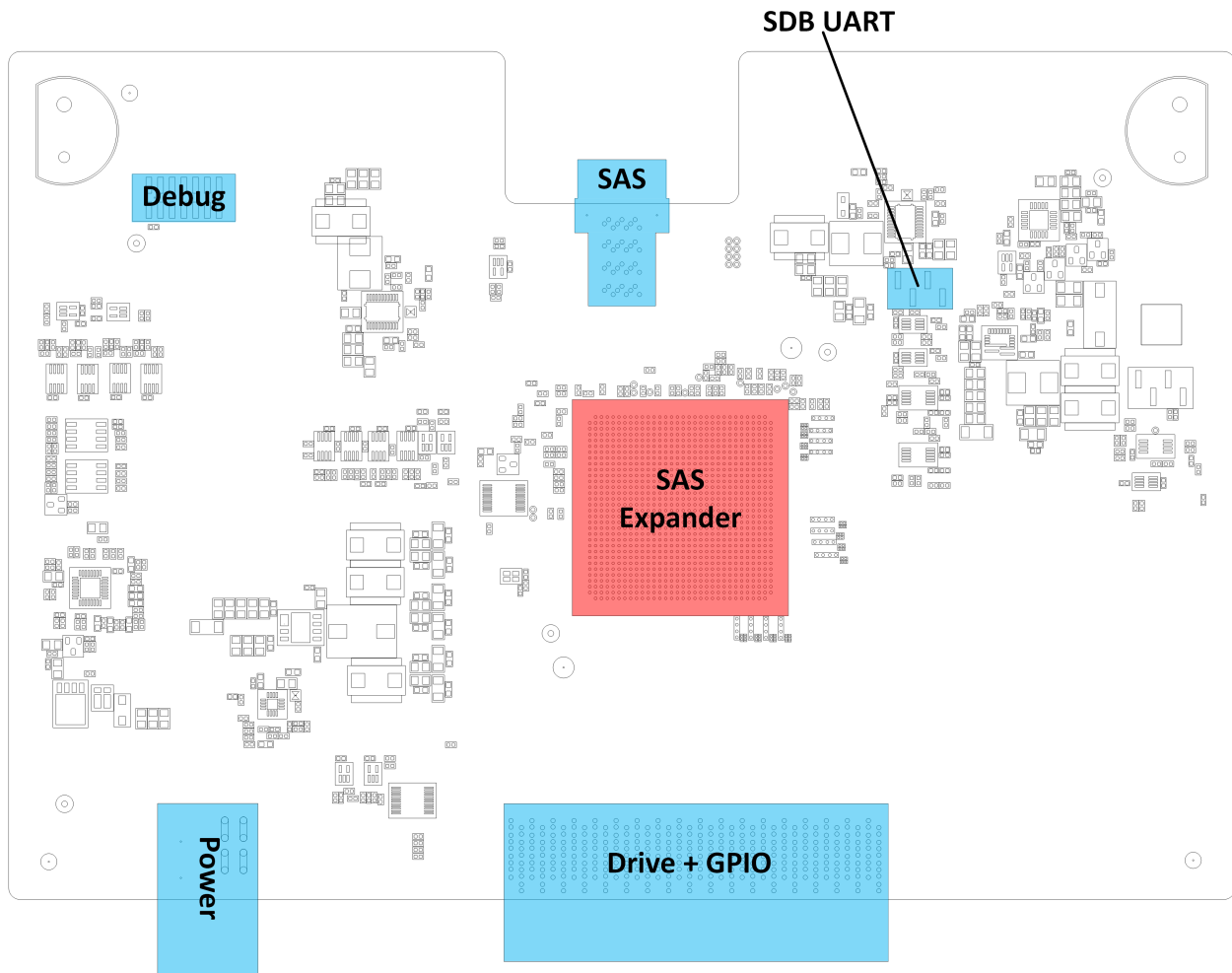
Figure 42 - SCC Type 7

8.5.2   PCB Key dimensions

The figure below shows the PCBA outline for the SCC.
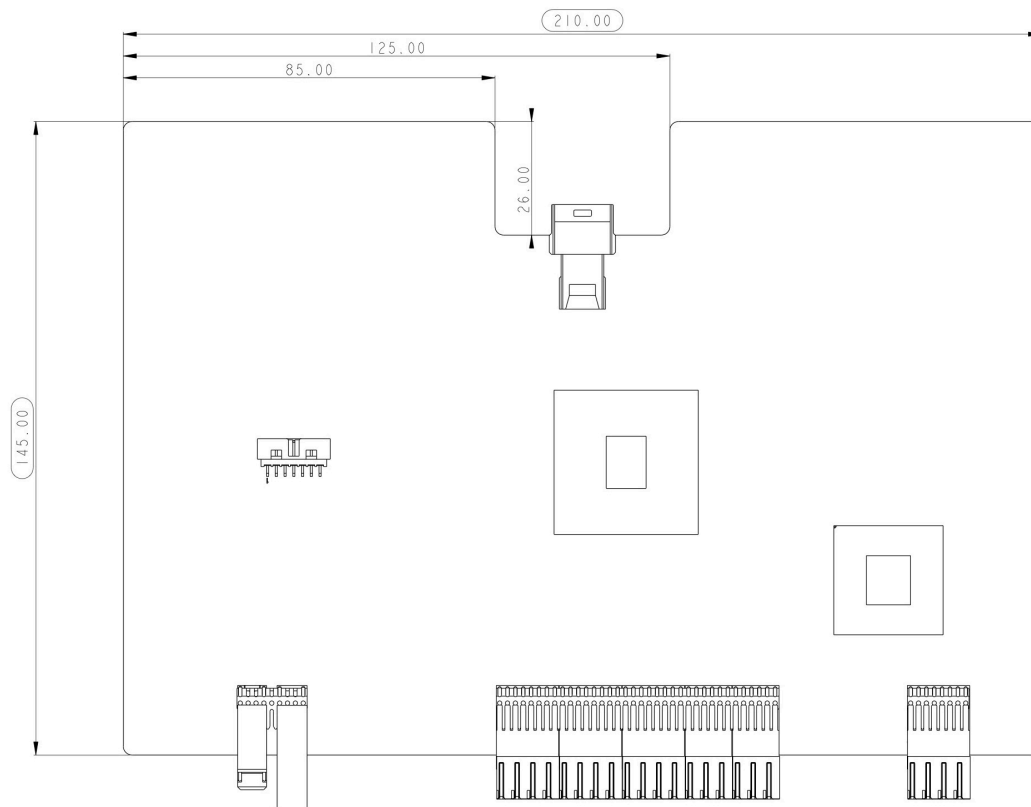
Figure 43. SCC PCBA outline

8.5.3   PCB Stack up

The following table details the physical construction of the PCB, including layer count, layer designation, thicknesses, material choice, material performance, and material finishes as design specific controls for trace impedance.

Board Number:	16316-SA					Version													
Project name:	**Bryce Canyon**					09													
Model Name:	Storage Controller Card																		
Layer Count:	8 Layer																		
Date:	2016/9/8																		
Material:	TU863+VLP / NPG171+VLP								Single Ended Type(mil)										
Gold Finger(Y/N):	Y						Imp	50				Imp	85						
Customer:	Fiona						Variation	Inner/Outer+/-5ohm				Variation	Inner/Outer+/-10%						
EE engineer	Jeff Huang						Bus	MISC./I2C				Bus	PCIe/Clock/USB						
SI Engineer	Eason YS Chen																		

Layer		Cu oz	Thickness Wiwynn	Glass/Copper Style	Er Wiwynn	Df(1G)	Type Layers	SE 1,3,6,8				Type Layers	DP 1,3,6,8					
								Wiwynn					Wiwynn					
	Mask		0.5		3.4			Width	Imp	Width	Imp		Width	Space	Imp	Width	Space	Imp
Top	Signal	3/8 oz+plating	1.7				S1	5(L2)	50.08			S1	5.75(L2)	6.5	85.36			
	Prepreg		3		3.9		P2	reference layer				P2	reference layer					
L2	GND	1 oz	1.3															
	Core		4		3.9													
L3	Signal	1 oz	1.3				S3	5(L2/L4)	49.28			S3	5.5(L2/L4)	7.5	84.9			
	Prepreg		16.4		4.2		P4	reference layer				P4	reference layer					
L4	POWER	1 oz	1.3															
	Core		4		3.8	0	0											
L5	POWER	1 oz	1.3	0.0	0		P5	reference layer				P5	reference layer					
	Prepreg		16.4	0	4.2	0	0											
L6	Signal	1 oz	1.3	0	3.9	0	0	S6	5(L5/L7)	49.28		S6	5.5(L5/L7)	7.5	84.9		
	Core		4	0														
L7	GND	1 oz	1.3	0	3.9	0	0	P7	reference layer			P7	reference layer				
	Prepreg		3	0														
Bottom	Signal	3/8 oz+plating	1.7	0	3.9	0	0	S8	5(L7)	50.08		S8	5.75(L7)	6.5	85.36		
	Mask		0.5	0	3.4	0	0											
Thickness requirement: 1.6 ± 10% mm		mil	63															
		mm	1.60															

Differential Type(mil)

100						97						88						92					83
Inner/Outer+/-10%						Outer+/-10%						Inner+/-10%						Outer+/-10%					Inner+/-10%
Clock/SATA						BGA Break out(SAS.SATA)						BGA Break out(SAS.SATA)						BGA Break out(PCIE)					BGA Break out(PCIE)
DP 1,3,6,8						DP 1,8						DP 3,6						DP 1,8					DP 3,6

Width	Space	Imp	Width	Space	Imp	Width	Space	Imp	Width	Space	Imp	Width	Space	Imp	Width	Space	Imp	Width	Space	Imp	Width	Space	Imp
4.9(L2)	11.1	96.82				3.5(L2)	4											3.75(L2)	3.5				
reference layer						reference layer			reference layer						reference layer						reference layer		
4(L2/L4)	8	97.59							3.5(L2/L4)	4											3.75(L2/L4	3.5	
reference layer						reference layer			reference layer						reference layer						reference layer		
reference layer						reference layer			reference layer						reference layer						reference layer		
4(L5/L7)	8	97.59							3.5(L5/L7)	4											3.75(L5/L7	3.5	
reference layer						reference layer			reference layer						reference layer						reference layer		
4.9(L7)	11.1	96.82				3.5(L7)	4											3.75(L7)	3.5				

Figure 44 - SCC Stack Up

9   I/O Module

The I/O Module is designed to provide connectivity to the storage servers inside the Bryce Canyon system. There are two I/O Modules planned for the launch of Bryce Canyon; one for the main storage sever application, and one for a cold storage configuration. The IOM also contains the BMC, which manages the system, including the compute cards, Storage Controller Cards, and fans.

9.1   BMC

The BMC used on the Bryce Canyon IOMs is an Aspeed AST2500 running an OpenBMC software stack.

The following firmware upgrade paths should be supported: I2C, USB, and UART. The UART path must be supported even when the BMC firmware is non-functional.

9.2   IOM Variants

9.2.1   NIC & Flash

The NIC & Flash IOM will provide connectivity for an OCP NIC via eight lanes of PCIe Gen 3 as well as 2x M.2 connectors routed with four lanes of PCIe Gen 3 for future growth. The OCP NIC supports 10/25/50 Gb NICs using the 5mm stack height connector option.
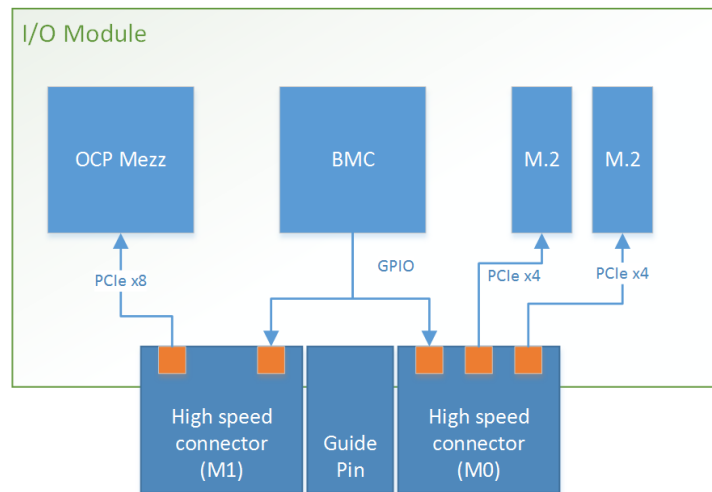
Figure 45. I/O Module block diagram (NIC & Flash variant)

9.2.1.1   M.2 & NVM enablement
The IOM supports two M.2 slots, which support both 2280 and 22110 modules.

Connector: The connectors are socket 3 type, M key, with a 5.8mm stack height.

Power Support: The M.2 slots should have the ability to draw up to 4.5A each, in order to support high powered modules and/or charging of super caps/batteries for an NVM device.

Super Cap/Battery: The IOM must have a cutout to allow for a later addition of a super capacitor or battery to enable NVM modules to be used in the M.2 slots. Only one place for this module needs to be supported. The mechanical envelope for the module is shown in Figure 46.
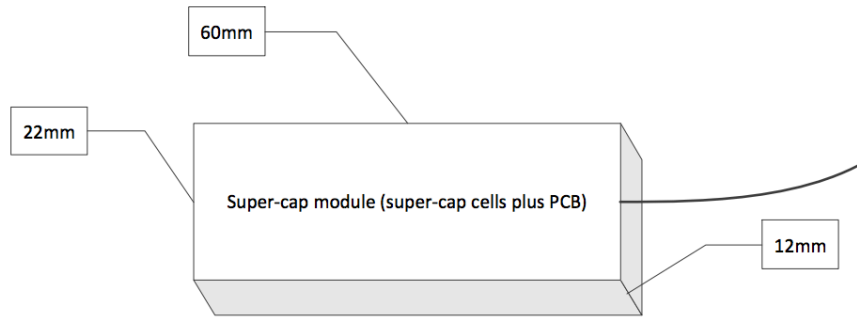
Figure 46. IOM super-cap envelope

9.2.2 NIC & SAS Expansion

The NIC & SAS Expansion IOM will provide connectivity for an OCP NIC via eight lanes of PCIe Gen 3, and a SAS IOC also connected via eight lanes of PCIe Gen 3. There will be two variants of this module to allow multi-vendor support. The boards will be otherwise identical, with the exception of the IOC chip and its support logic.

Table 22. NIC & SAS Expansion IOM variants

Variant	Supplier	NIC P/N
A	Mellanox	MCX4411B-ACAN_FB
B	Broadcom	BCM957302M3021CBK

There are two MiniSAS HD external (SFF-8644) connectors present on the IOM. There shall be at least two footprint-compatible connector options.
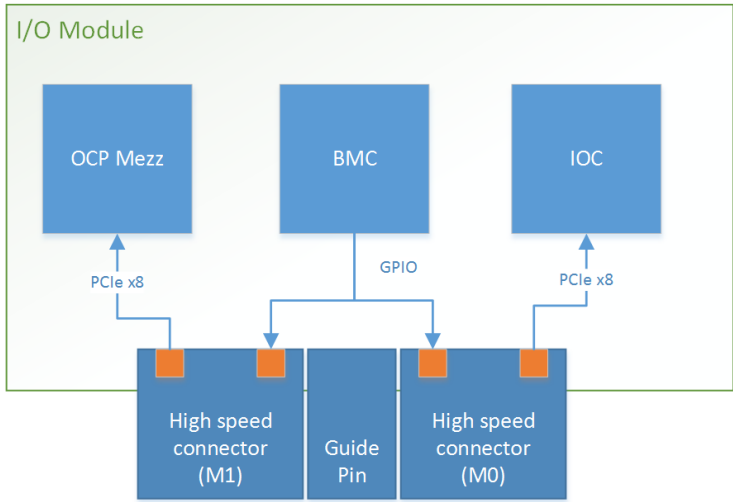
Figure 47. I/O module block diagram (NIC & SAS Expansion variant)

9.2.3 IOM Type Bits

To identify the different IOM variants to the BMC, dedicated GPIs on the BMC shall be strapped up/down depending on the BOM population of the IOM. This is done so that the BMC does not have to query the attached devices on the IOM to self-identify. The type bits are defined as follows:

Table 23. IOM type bits

Variant	TYPE 0	TYPE 1	TYPE 2	TYPE 3
M.2 Variant	0	0	0	1
IOC Variant	0	0	1	0

9.3 Connectors

9.3.1 OCP Mezzanine

The IOM supports "Connector A" from the OCP Mezzanine NIC specification. This connector routes x8 lanes of PCIe Gen 3. The part number used on the IOM is FCI 61082-121402LF. The IOM does not populate connectors B or C, but may reserve the footprints for future use.

The Bryce Canyon IOM only supports 5mm stack height OCP NICs, as opposed to the more common 8mm stack height. The mechanical retention mechanism must ensure that an 8mm OCP NIC will not seat in correctly.

9.3.2 USB Debug

The IOM will have a USB 3.0 debug port, which re-maps pins provided by a standard USB 3.0 Type-A connector. The pin mapping is shown in Section 23.12. This debug header will connect the USB 2.0 portion of the connector to the compute server USB lanes. The UARTs that will route to the debug mux selection come from the BMC and compute server.

The debug header requires a few circuits on the IOM board to allow the UART selection, port 80 codes, etc.
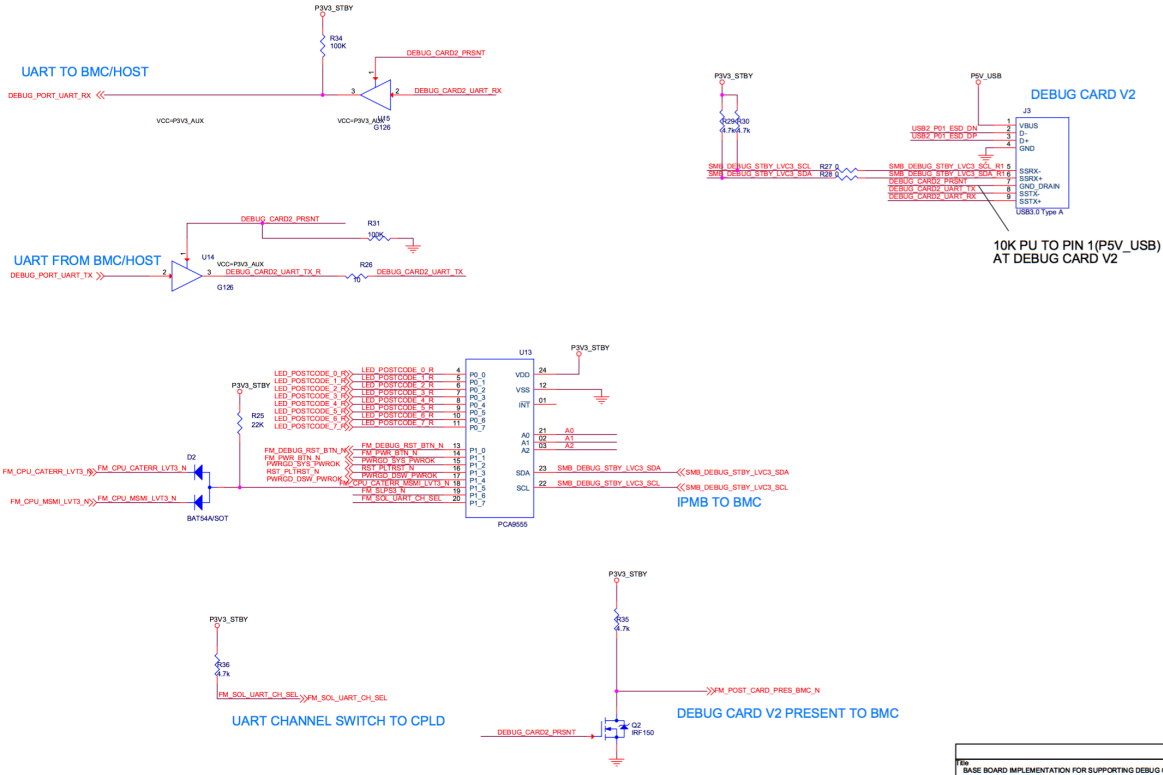
Figure 48. Baseboard reference schematic for USB 3.0 debug card

9.4   TPM

The IOM must support the same TPM implementation as used in Tioga Pass. For reference, the part number is SLB9645TT1-2FW133-32.

9.5   LEDs & Buttons

9.5.1   SAS Link LED

There shall be blue/yellow link status LEDs for the MiniSAS HD ports. There will be one LED per connector. The yellow fault/indicator LED is connected to the BMC to allow this to be turned on. When the yellow is illuminated, the blue should be gated off via hardware. See section LEDs and for more information on LED behaviors.

9.5.2   Graceful Shutdown Button

The reset button shall be a right angle, momentary-on pushbutton switch with a red plunger. This button is routed to the BMC to allow the system to perform a graceful shutdown of the system.

9.6   USB Connectivity

The IOM features a two or four port USB hub to connect the compute server to the BMC and the external USB connector. The topology is shown in Section 6.2.6.

9.7   I/O Module PCB

9.7.1   Important Components & Interfaces

The following figures detail the major functional blocks of the IOM, and their placement on the PCBs. This is detailed for both versions of the IOM, the Type 5 version with BMC and M.2 flash cards, as well as the JBOD version with just the BMC in addition to the IOC for downstream JBOD chassis.
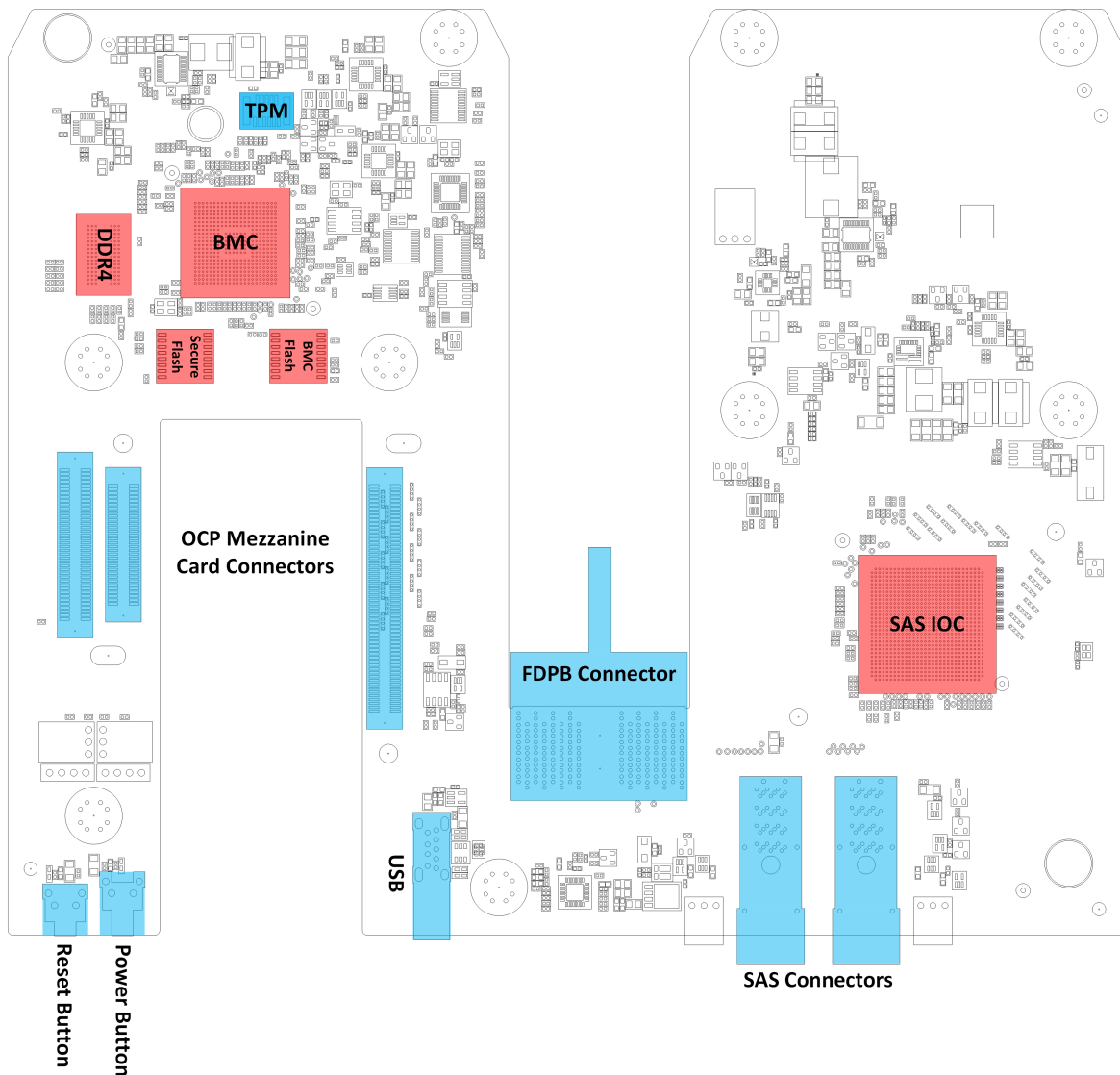
Figure 49. I/O Module placement (Dual Storage Server configuration)
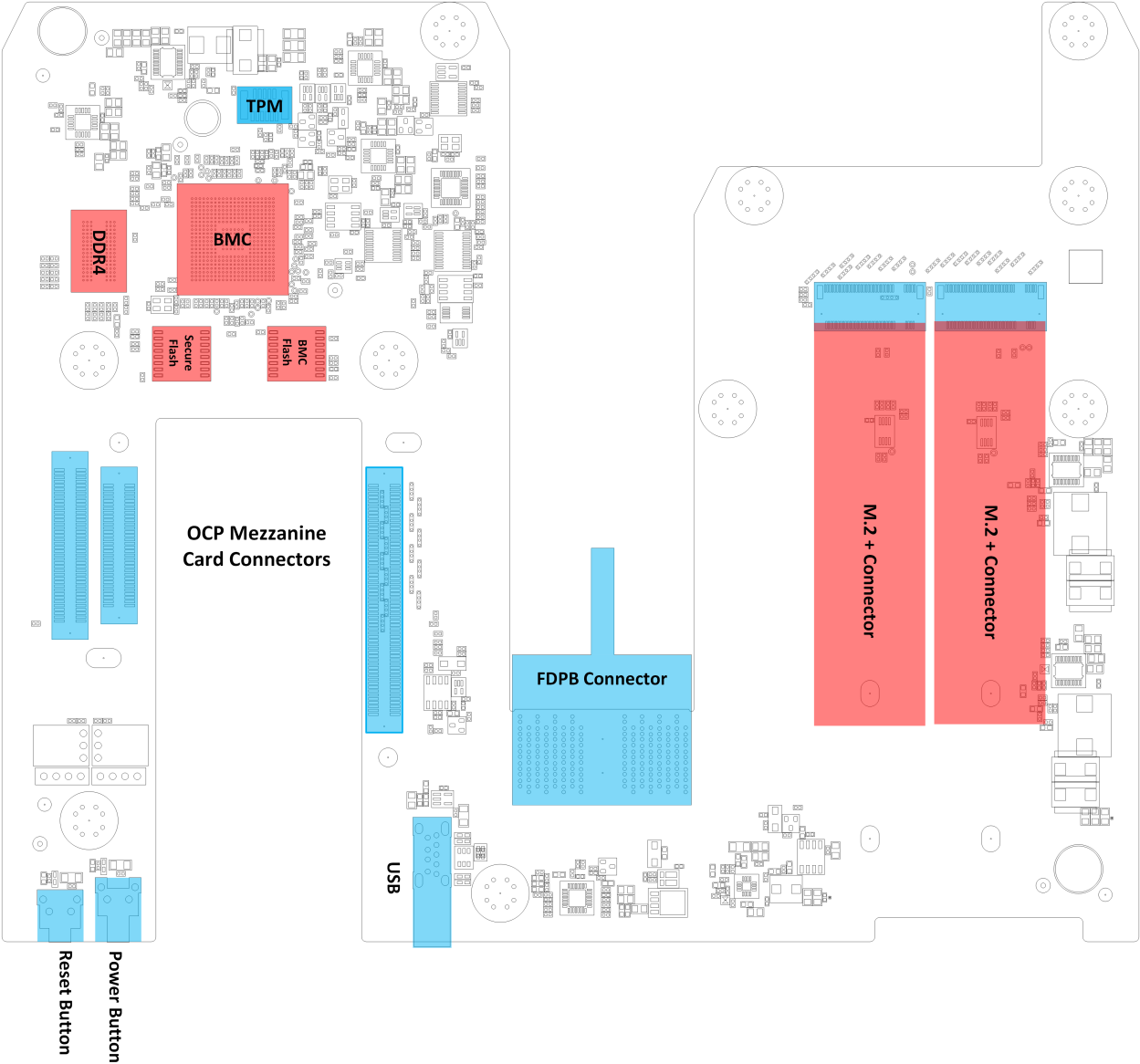
Figure 50. I/O Module placement (Single Storage Server configuration)

9.7.2   PCB Key dimensions

The figures below show the PCBA outline for the IOM (both NIC & SAS Expansion and NIC & Flash variants).
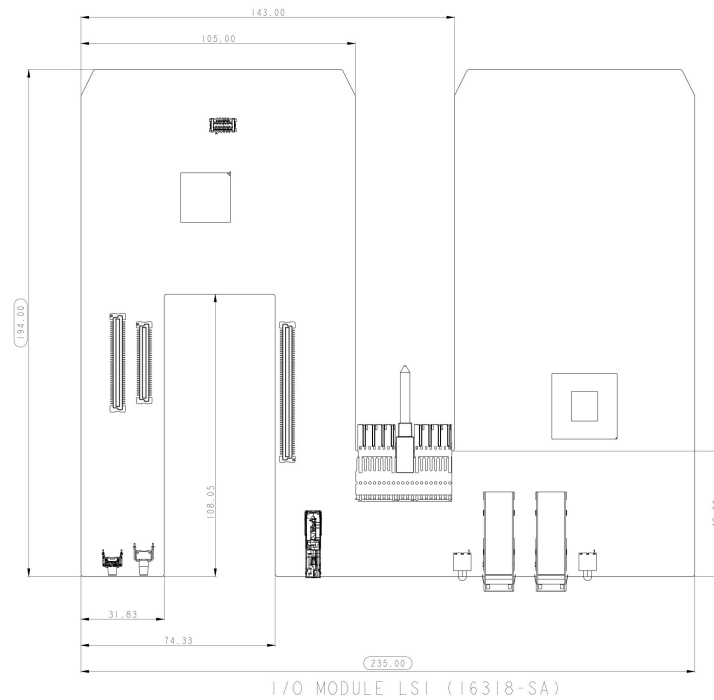
Figure 51. IOM PCBA outline (NIC & SAS Expansion)
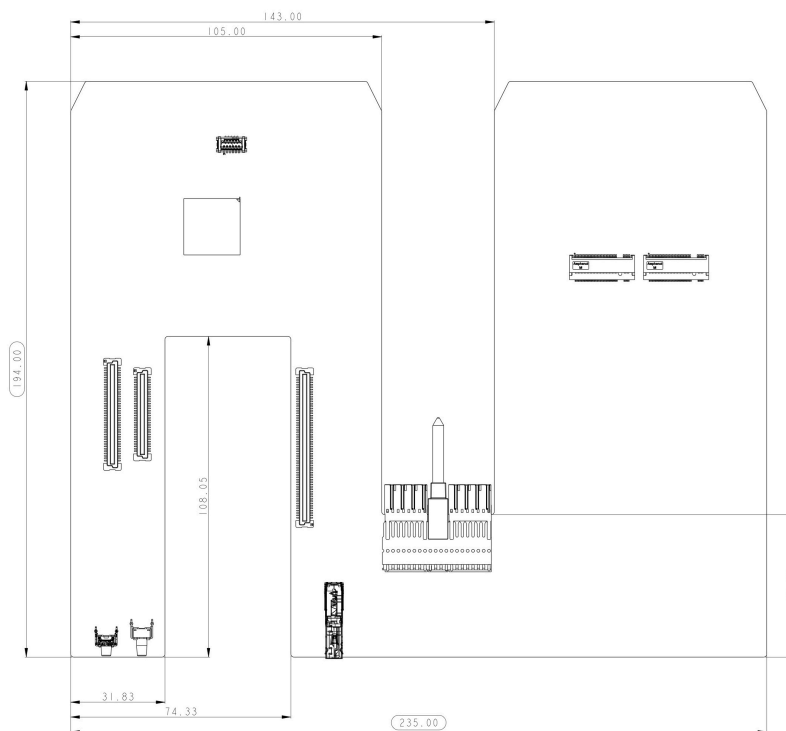
Figure 52. IOM PCBA outline (NIC & Flash)

9.7.3   PCB Stack up

The following table details the physical construction of the PCB, including layer count, layer designation, thicknesses, material choice, material performance, and material finishes as design specific controls for trace impedance.

Figure 53 - IOM Type 5 Stack Up

Figure 54 - IOM Type 7 Stack Up

10 Drive Plane Boards

The Drive Plane Boards serve to connect all the PCBs in the system to create the platform. The boards are divided into a Rear Drive Plane Board and a Front Drive Plane Board, joined with a coplanar board connector. This is to allow the DPB PCBs to be small enough to easily manufacture. The division of components between the boards is shown in Figure 55.
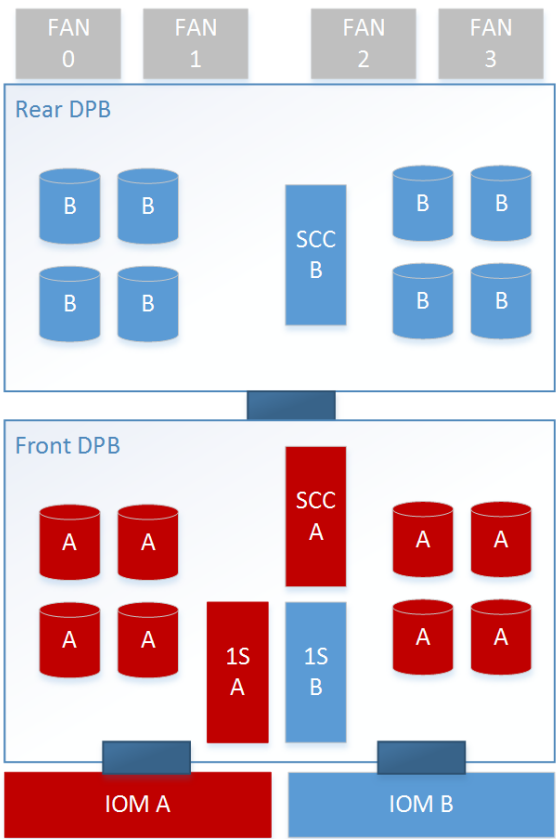
Figure 55. Division of components between Rear and Front Drive Plane Boards

The key components list for both the Front and Rear DPBs can be found below.

Table 24. Drive Plane Board key components list

Front DPB	Rear DPB
36x 12Gb SAS 29-pin SMT connectors	36x 12Gb SAS 29-pin SMT connectors
1x SCC Connector Set	1x SCC Connector Set
4x PCIe Gen 3 PCIe x16 connectors	1x 12V Input connector
2x IOM connectors	4x 10-pin fan connectors
	Drawer Detection Sensor set

10.1 Connectors

10.1.1 Compute Slots

There are two compute slots in the Bryce Canyon chassis. These comply with the pinouts in the 1S Microserver specification, and are referenced in the Connector Pinouts section. Each microserver is connected via two x16 PCIe Gen 3 connectors, which must be press fit or SMT connectors.

10.1.2 IOM Connectors

[Placeholder]

10.1.3   SCC Connectors

The SCC connectors are comprised of several modules. These include an 85 Ohm impedance module for PCIe, a 100 Ohm module for the SAS and GPIO signals, a power module, and a guide pin.

See sections 23.15 and 23.16 for Front and Rear DPB SCC SAS and PCIe connector pinouts.

10.1.4   Hard Drive Connectors

There are 36 SAS drive connectors used on each DPB. These connectors shall be surface mount, 29-pin 12Gb SAS connectors. The contacts must be plated with a minimum of 30µ" of gold. There shall be at least two sources for this connector that are fully footprint-compatible.

10.1.5   12V System power input

The 12V cable from the busbar clip terminates into the Rear DPB with a squeeze-to-release connector that plugs into a receptacle (P/N: TE 1-6450824-2, or equivalent).
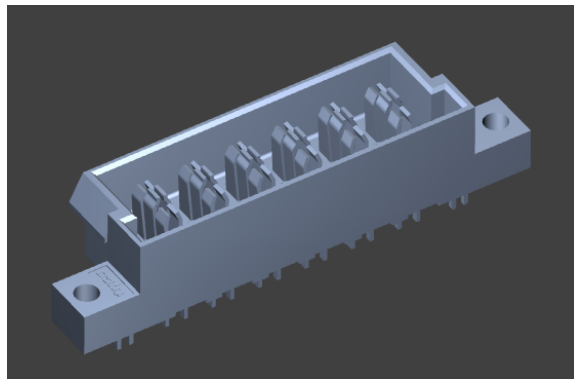
Figure 56. Vertical mating plug for power

10.1.6   DPB to DPB Power connectors

There are two 12V power rails that connect through the DPB to DPB power connectors. To minimize the power loss, and ensure the best routing, the following pinout is used as shown in Figure 57. This illustrates the front DPB, as viewed from the top. The blue section is P12V_A, and the red section is P12V_B. P12V_A; they should be routed on both 2oz power planes. P12V_B should route on a single 2oz power layer only.
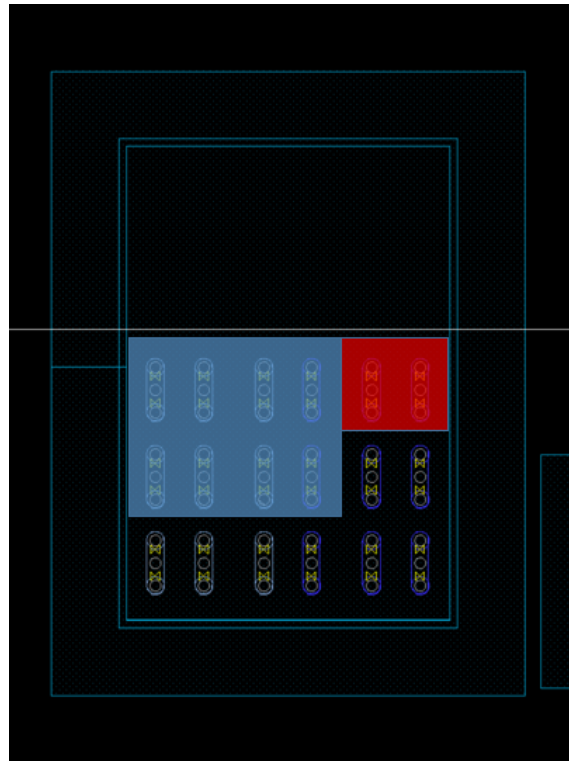
Figure 57. DPB-to-DPB power connector pinout

10.1.7 DPB to DPB Signal Connectors

[Placeholder]

10.1.8 Fan Connectors

There are four connectors to support dual counter-rotating fans in the back of the chassis. These connectors are only on the Rear DPB. These should be Molex Mini-fit 0438100279 or 0438100059, or equivalent. The pinouts for the connectors are located in Section 23.12. <confirm drawing below>
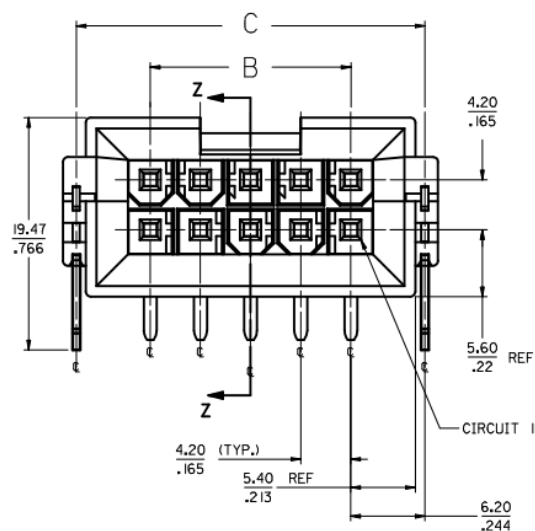
Figure 58. Fan connector drawing

10.1.9 Front Panel Board Connector

The front-panel functionality outlined in Section 4.2.1 should be supported by a separate daughter card, which plugs vertically into the DPB. The functionality for this Front Panel Board is outlined in Figure 59, which shows the circuitry required to support one logical side of the system (i.e., Side "A" or "B"). The complete pinout of the connector is shown in Section 23.13.
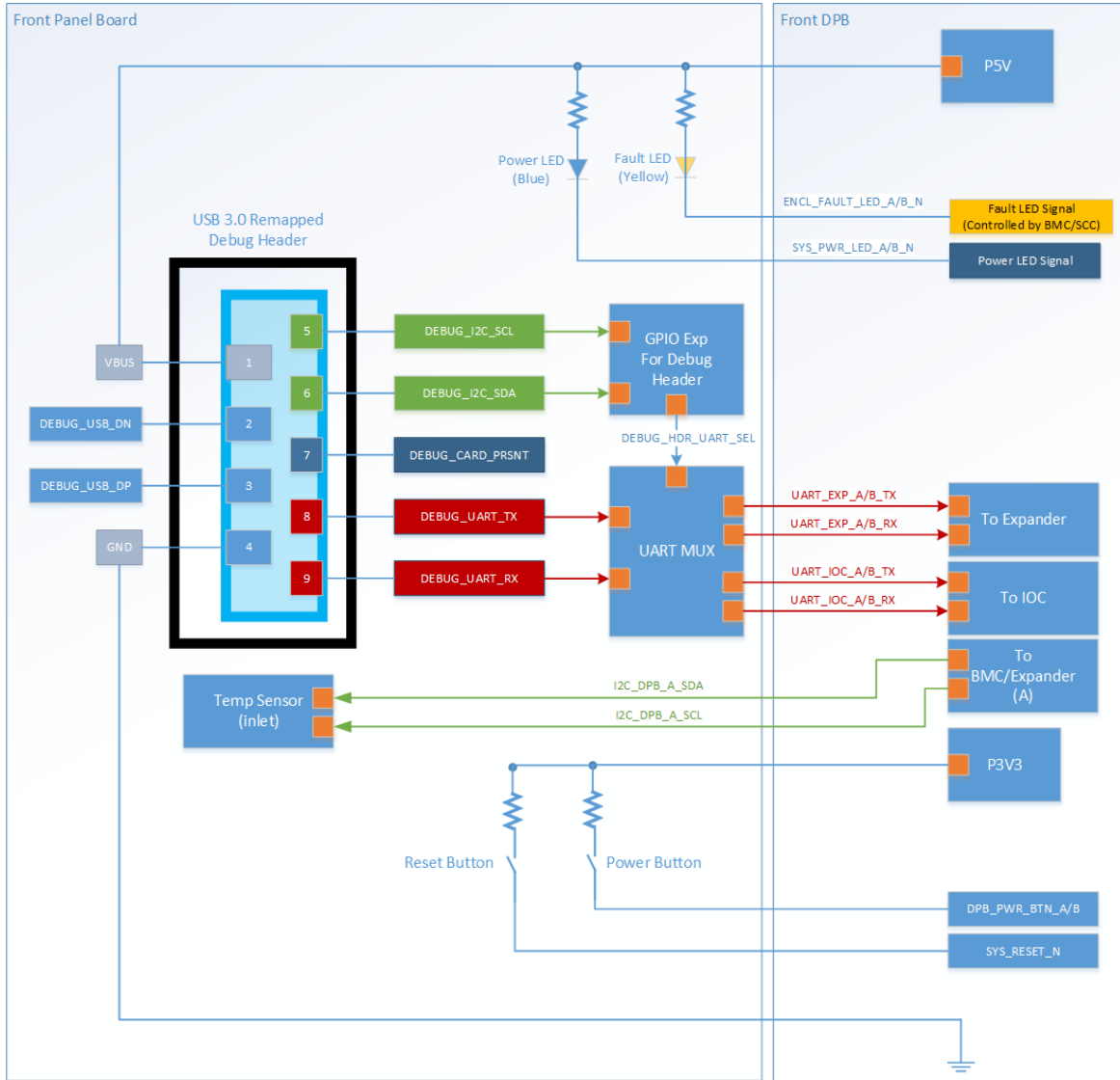
Figure 59. Front Panel Board block diagram

10.2 LEDs

Each drive slot has two LEDs that will illuminate a light pipe to allow the user easy identification of the drive status.

10.2.1 Drive Activity

The drive activity LED is a blue LED, and is controlled by the SAS expander on the SCC. The LED will be illuminated when the PHY link is established with the HDD. The expander should turn off the LED if the drive is not linked, spun down, etc.

In the future, if there is a requirement to blink the LED to indicate activity, the expander can emulate this behavior.

In order to save power, the activity LED should only be illuminated when the drawer is pulled out for service. This is possible due to the drawer insertion signal that alerts the SCC that the drawer is open.

10.2.2 Drive Fault/Identification

The drive fault indicator is a yellow LED. This is controlled by the SAS expander on the SCC via I2C GPIO devices located on the DPB. The DPB must implement a circuit to ensure that when the fault LED is illuminated, the drive activity LED is not illuminated.

10.3 Routing Requirements

To mitigate the impact of fiber weave, all high speed traces routed parallel to the X or Y axis of the PCB within five degrees must implement a weaving pattern every 2" or less.

10.3.1 SAS

The SAS lines shall be routed at a nominal 100 Ohm differential impedance. There should be a minimum spacing of 5x to the nearest high speed trace. Due to the length of the traces, routing on external layers is preferable.

All SAS lines shall be simulated and tested to comply with SAS 12Gb channel requirements, as well as SATA 6Gb.

10.3.2 PCIe

The PCIe lanes shall be routed at a nominal 85 Ohm differential impedance. There should be a minimum spacing of 5x to the nearest high speed trace.

The PCIe clocks shall be routed at a nominal 85 Ohm differential impedance. There should be a minimum spacing of 5x to the nearest high speed trace.

The longest PCIe path is from the B side server slot to the Rear DPB into the SCC. Thus, on the Front DPB, this bus should be routed first and given preference for the best routing layers.

10.4 Thermal Sensor Placement

There shall be four temperature sensors on each of the DPBs. These should be placed roughly as shown in Figure 60.
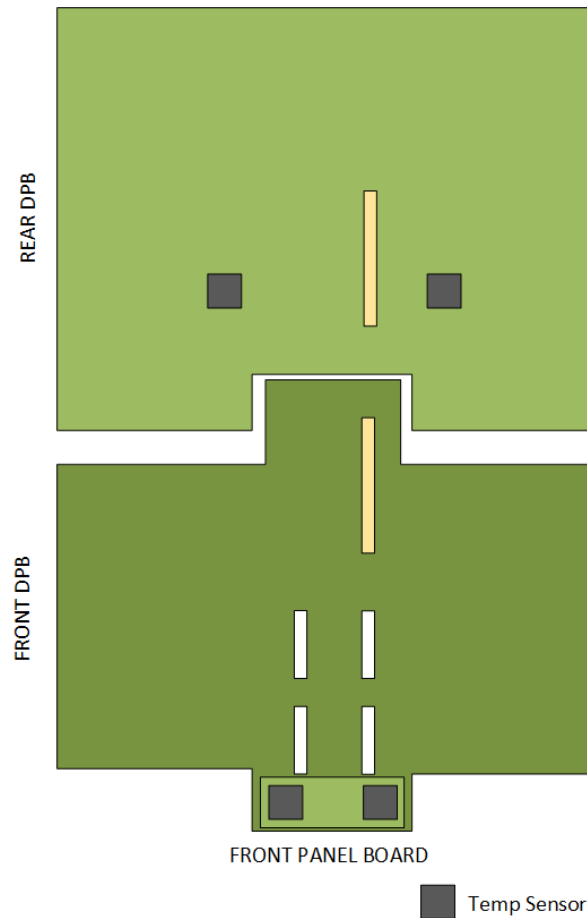
Figure 60. DPB temperature sensor placement guideline

10.5 I2C Component Placement

Due to the large number of I2C devices on the DPB, care should be taken when placing the components to reduce the overall bus capacitance. For the drive related I2C components, such as the drive insert, drive fault, and drive power control GPIO expanders, it would be preferable to group these close to the SCC connector to reduce etch length and capacitance. Care should also be taken to reduce branches in the routing that add to overall capacitance and reflections.

10.6 Drawer Detection Sensor

The Rear DPB must implement a drawer detection sensor. One state from this sensor should indicate that the drawer is completely closed, and the other state should indicate that it is somewhere between fully open and almost closed. This signal will go to the BMCs and SAS expanders to allow the chassis to understand that the drawer is open. The system is unable to cool drives adequately indefinitely if the drawer is left open, and there might need to be a thermal throttling or emergency shutdown if left open too long.

10.7 Drive Control Signals

There are four different HDD control signals routed through the DPB (Drive Insert, Fault LED, Drive Power, and Drive Activity). The first three of these signals (Insert, Fault, and Power) are routed through three GPIO

expander ICs each to accommodate 36 individual channels per signal. The latter, Drive Activity, is routed directly through the SCC connector and does not go through an expander.

Additionally, there is a DRIVE_INSERT_ALERT_N signal, which represents a wired-OR configuration (open-drain) of the interrupt outputs from the three Drive Insert GPIO expanders. This Alert signal is routed through the SCC connector to the SAS expander. See Figure 61 for an example of this configuration, as it would appear in the Front or "A" side of the box.
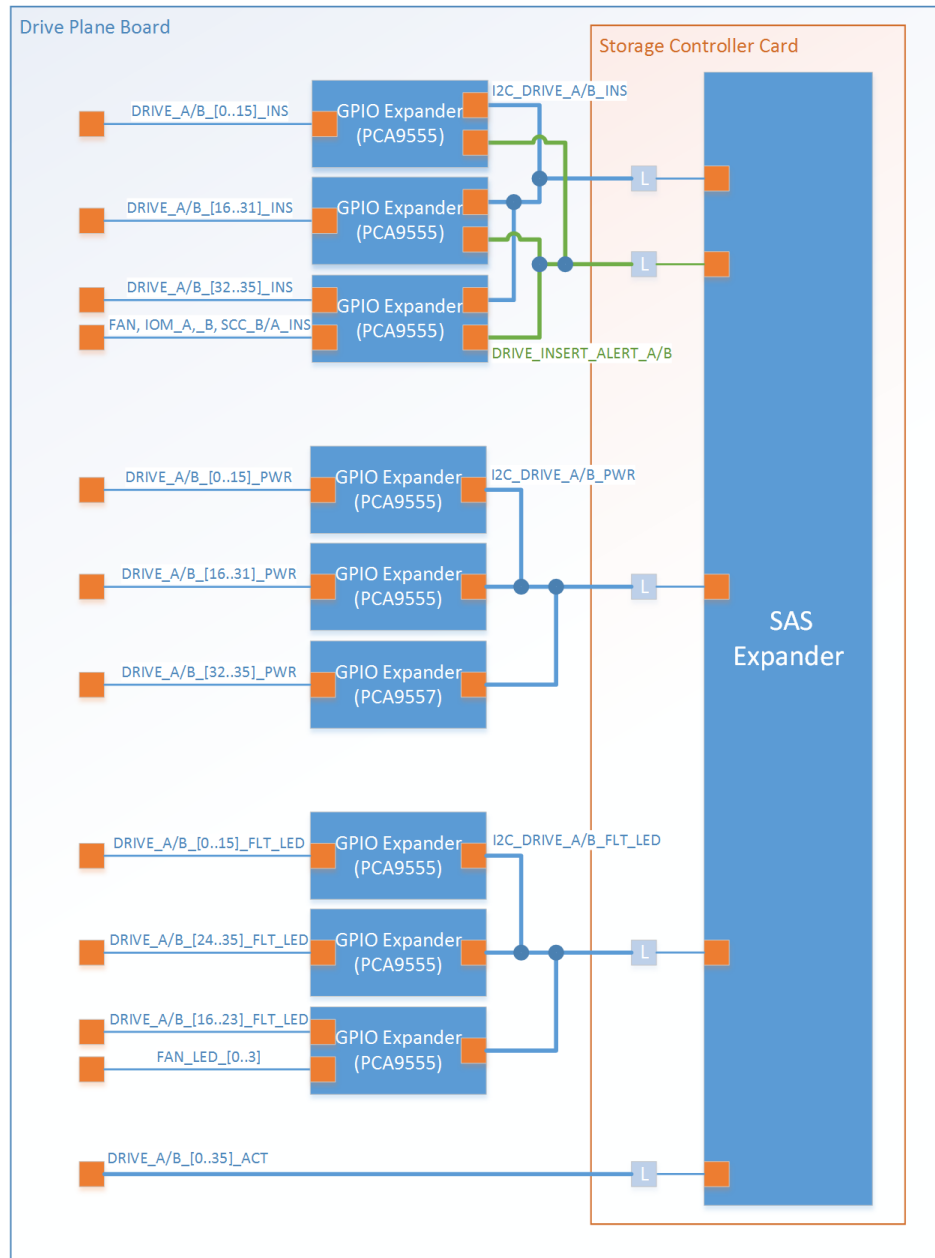
Figure 61. Drive control signal block diagram

10.8 PCB Details

10.8.1   Front DPB

10.8.1.1   Important Components & Features

The following figure details the major functional blocks of the Front DPB, and their placement on the PCB. More detailed information on the specific functional blocks can be found in the schematics as well as the descriptions in the documentation above.
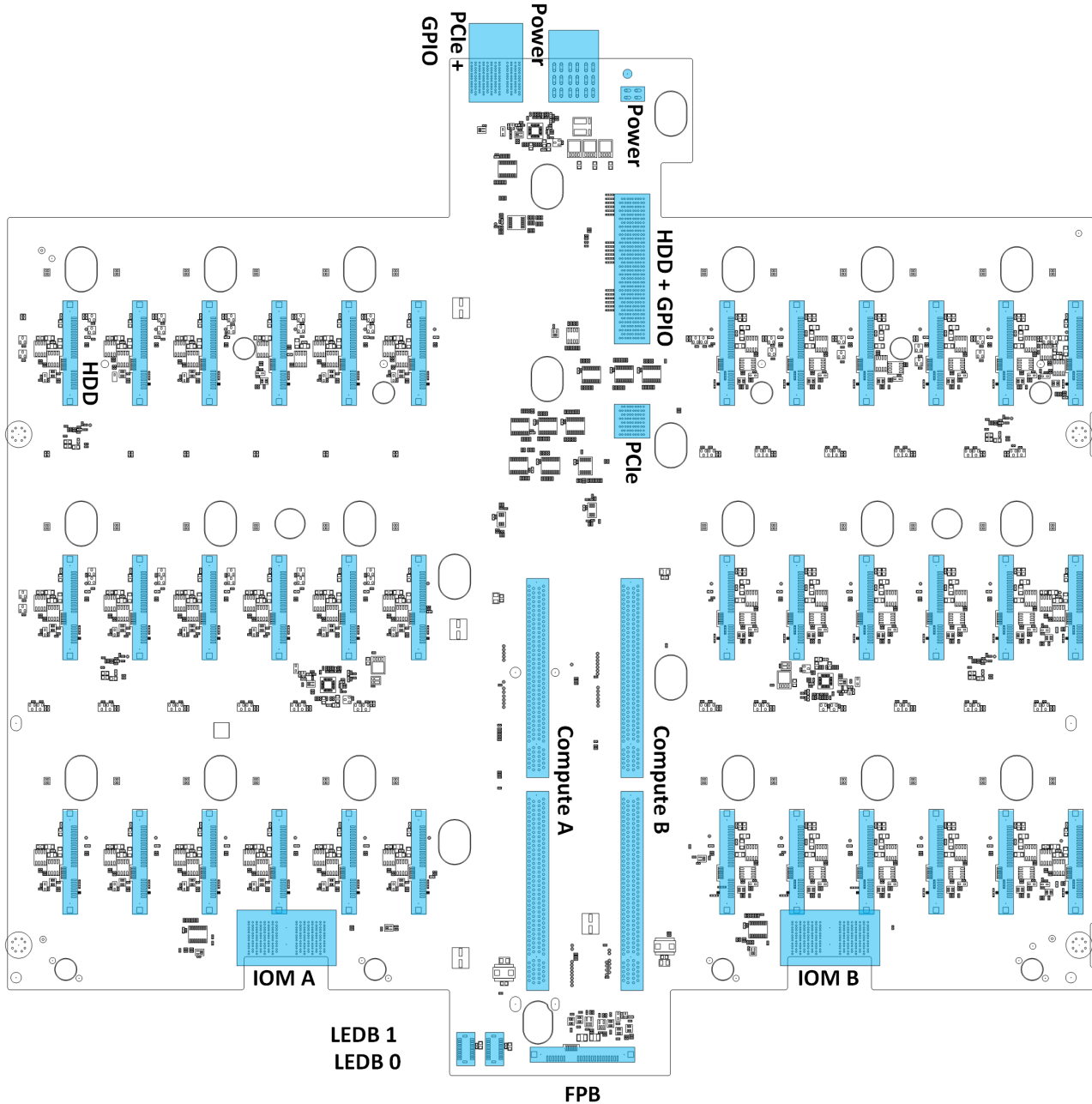
Figure 62 - Front Drive Plane Board

10.8.1.2   PCB Key dimensions

Facebook

The figure below shows the PCBA outline for the Front DPB.
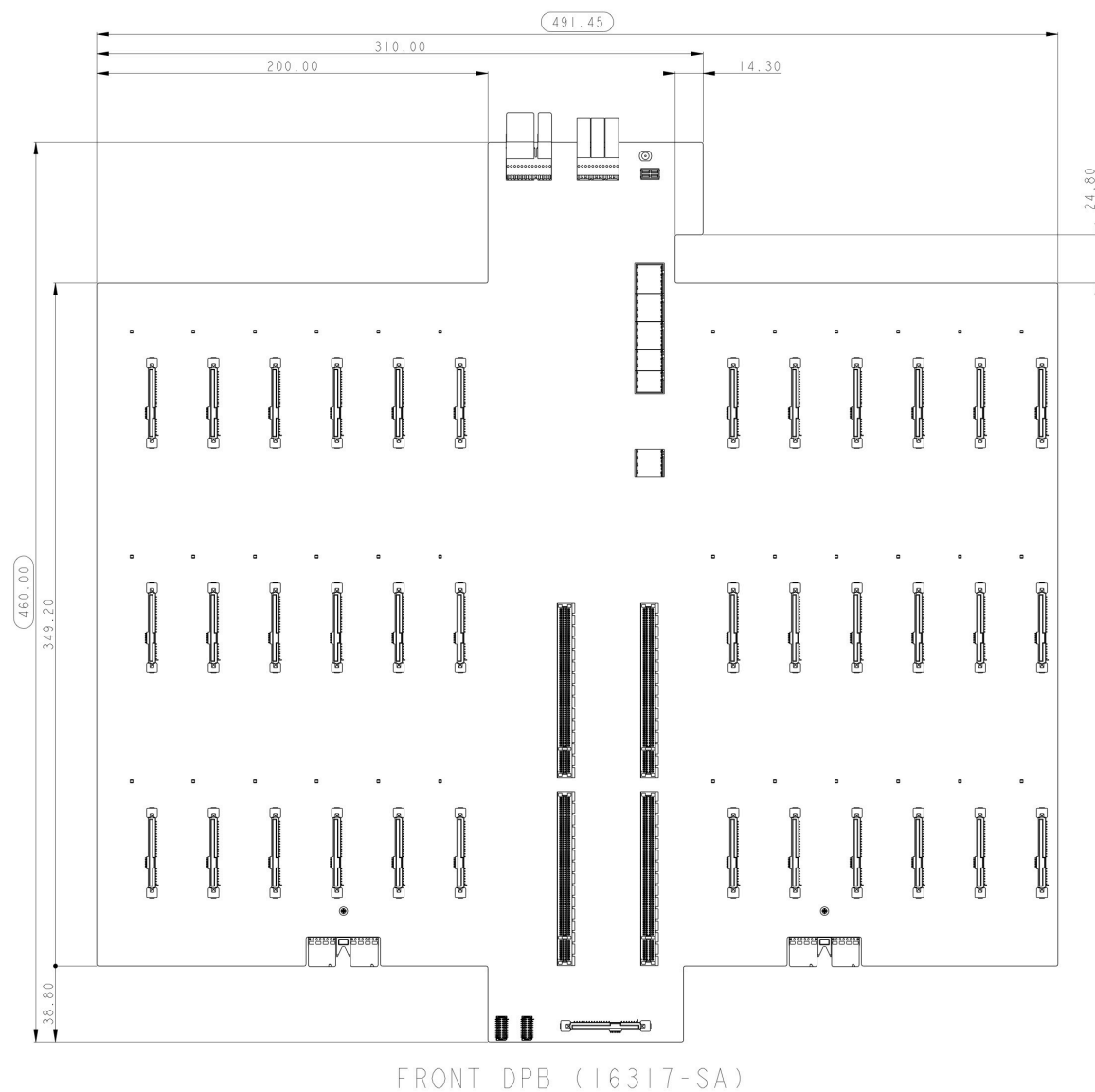
Figure 63. Front DPB PCBA outline

10.8.1.3   PCB Stack up

The following table details the physical construction of the PCB, including layer count, layer designation, thicknesses, material choice, material performance, and material finishes as design specific controls for trace impedance.

Figure 64 - Front DPB Stack Up

10.8.2 Rear DPB

10.8.2.1 Important Components & Interfaces

The following figure details the major functional blocks of the Rear DPB, and their placement on the PCB. More detailed information on the specific functional blocks can be found in the schematics as well as the descriptions in the documentation above.

Figure 65 - Rear Drive Plane Board

10.8.2.2   PCB Key dimensions

The figure below shows the PCBA outline for the Rear DPB.
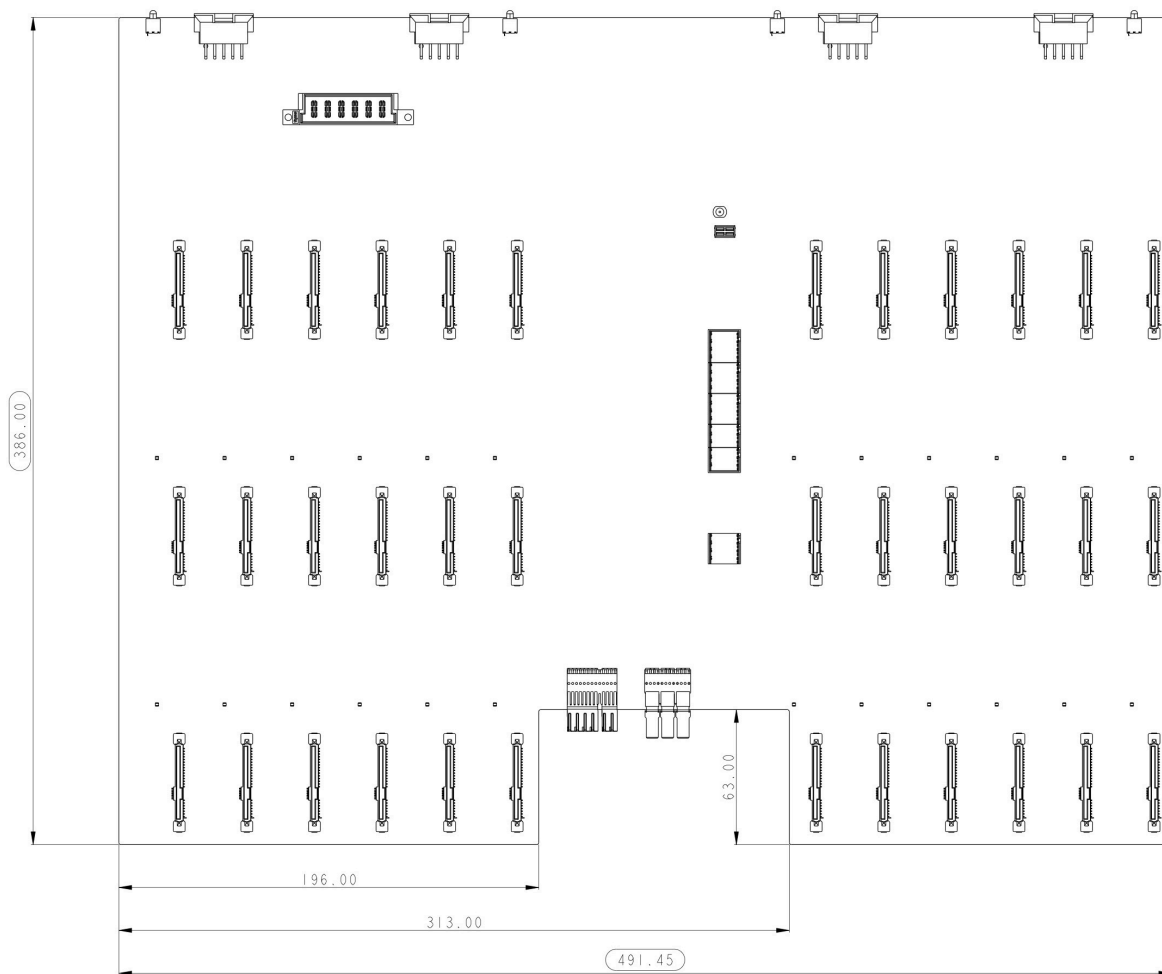
Figure 66. Rear DPB PCBA outline

10.8.2.3 PCB Stack up

The following table details the physical construction of the PCB, including layer count, layer designation, thicknesses, material choice, material performance, and material finishes as design specific controls for trace impedance.

Figure 67 - Rear DPB Stack Up

11 Front Panel Board

11.1 Important Components & Interfaces

The following figure details the major functional blocks of the Front Panel Board, and their placement on the PCB. More detailed information on the specific functional blocks can be found in the schematics as well as the descriptions in the documentation above.
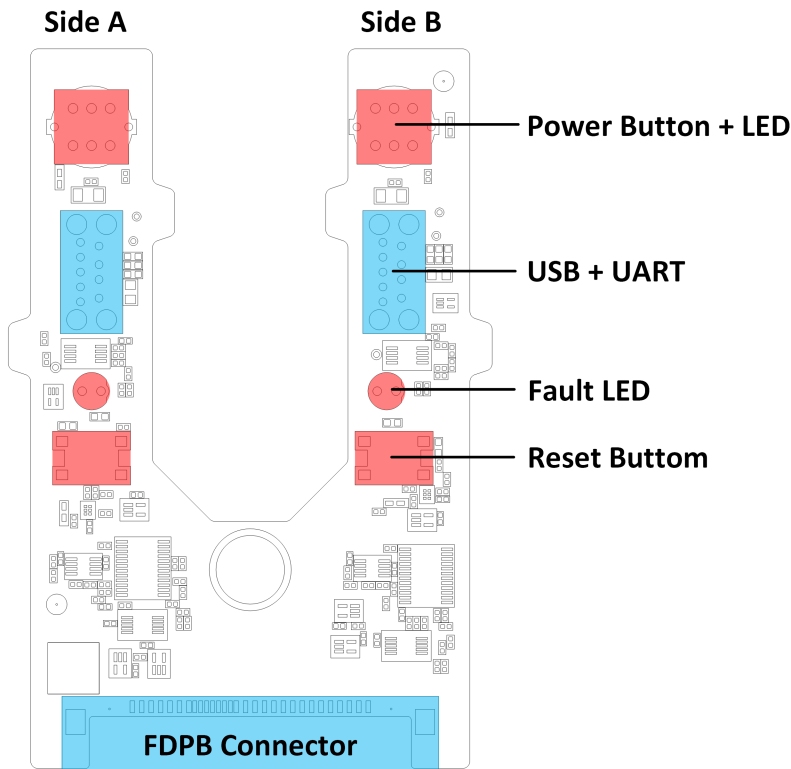
Figure 68 - Front Panel Board

11.2 PCB Stack up

The following table details the physical construction of the PCB, including layer count, layer designation, thicknesses, material choice, material performance, and material finishes as design specific controls for trace impedance.

Board Number:	16369-SA		Version 01
Project name:	Bryce Canyon		
Model Name:	Front Panel Board		
Layer Count:	4 Layer		
Date:	2016/8/11		
Material:	IT150G / NPG150N		
Golden Finger(Y/N):	N		
Customer:	Fiona		
EE engineer:	Kent Tsai		
SI Engineer:	Eason YS Chen		

						Single Ended Type(mil)			
					Imp Variation	50			
						Inner/Outer+/-5ohm			
					Bus	MISC./I2C			

	Layer	Cu oz	Thickness Wiwynn	Glass/Copper Style	Er Wiwynn	Df(1G)	Type Layers	SE 1,4			
								Width Wiwynn	Imp	Width	Imp
	Mask		0.5		3.4						
Top	Signal	0.5 oz+plating	1.9				S1	6.75(L2)	49.96		
	Prepreg		4		4						
L2	POWER/GND	1 oz	1.3				P2	reference layer			
	Core		47.6		4.5						
L3	POWER/GND	1 oz	1.3	0	0		P3	reference layer			
	Prepreg		4	0	4	0	0				
Bottom	Signal	0.5 oz+plating	1.9	0	0		S4	6.75(L3)	49.96		
	Mask		0.5	0	3.4	0	0				
Thickness requirement: 1.6 ± 10% mm		mil	63								
		mm	1.60								

Figure 69 - Front Panel Board Stack Up

12 LED Board

12.1 Important Components & Interfaces

The following figure details the major functional blocks of the LED Board, and their placement on the PCB. More detailed information on the specific functional blocks can be found in the schematics as well as the descriptions in the documentation above.
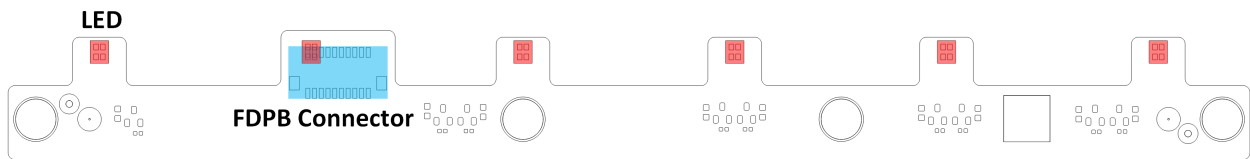
Figure 70 - LED Board

12.2 PCB Stack up

The following table details the physical construction of the PCB, including layer count, layer designation, thicknesses, material choice, material performance, and material finishes as design specific controls for trace impedance.

Board Number:	16347-SA		Version 03
Project name:	Bryce Canyon		
Model Name:	LED Board		
Layer Count:	2 Layer		
Date:	2016/8/11		
Material:	IT150G / NPG150N		
Golden Finger(Y/N):	N		
Customer:	Fiona		
EE engineer:	Kent Tsai		
SI Engineer:	Scott Lee		

						Single Ended Type(mil)			
					Imp Variation	50			
						Inner/Outer+/-10%			
					Bus	MISC.			

	Layer	Cu oz	Thickness Wiwynn	Glass/Copper Style	Er Wiwynn	Df(1G)	Type Layers	SE 1,2			
								Width Wiwynn	Imp	Width	Imp
	Mask		0.5		3.4						
Top	Signal/GND	0.5 oz+plating	1.9				S1	20(L1)	49.57		
	Core		34.5		4.5						
Bottom	Signal/GND	0.5 oz+plating	1.9	0	0		S2	20(L2)	49.57		
	Mask		0.5	0	3.4	0	0				
Thickness requirement: 1.0 ± 10% mm		mil	39.3								
		mm	1.00								

Figure 71 - LED Board Stack Up

13 **BMC Overview**

[Placeholder]

14 Expander Firmware Overview

The expander should have the following functionalities:

1. Sensor readings (per SES standards);
2. Calculate and report full chassis power consumption (in SCSI buffer or OEM SES pages);
3. HDD power control;
4. HDD LED control (see section 14.1);
5. Generate PWM for 2 sets of fans;
6. Read and clear of PHY error counters;
7. Read and write of FRUIDs;
8. Report status of GPIOs;
9. Provide configurable variables (see section 14.2);
10. Triggers chassis identify LED.

Please refer to "Facebook SCSI Enclosure Processor (SEP) Firmware Specification" for details of SES interface.

14.1 Drive LEDs

14.1.1 Drive Link LED

The drive Link LED is a blue LED, and is controlled by the SAS expander on the SCC. The LED will be illuminated when the PHY link is established with the HDD. The expander should turn off the LED if the drive is not linked, spun down, etc.

In the future, if there is a requirement to blink the LED to indicate activity, the expander can emulate this behavior.

14.1.2 Drive Fault/Identification LED

The drive fault indicator is a yellow LED. This is controlled by the SAS expander on the SCC via I2C GPIO devices located on the DPB. The DPB must implement a circuit to ensure that when the fault LED is illuminated, the drive activity LED is not illuminated.

The fault LED implements the following patterns:

1. Fault bit is set in SES page: on;
2. Ident bit is set in SES page: blink three seconds on, one second off.

14.1.3 Drive LED Behavior when drawer is inserted

In order to save power, the activity LEDs should only be illuminated when the drawer is pulled out for service. This is possible due to the drawer insertion signal that alerts the SCC that the drawer is open.

14.2 Runtime system configuration

The following parameters of the system must be configurable at runtime:

1. Current fan profile;
2. Time window of power calculation;
3. HDD temperature polling interval.

15 System Firmware Behaviors

15.1 Drawer Open Thermal Warning Behavior

The Bryce Canyon system is required to keep all of the components in the system within the nominal temperatures. Both the expander firmware and BMC need to monitor when the drawer is opened for service, and must provide a visual indication to the user when one or more components in the system is about to hit a thermal trip points. This indication must start a minimum of 30 seconds before the expected trip point is hit.

The behavior should be implemented as shown below. The fault LEDs in the first row should all illuminate, followed by the second row 1 second later, and the third row 1 second after that, and continuing until the 6th row is reached. At this point, the behavior should start again from the first step.

If one or more drives has previously been marked faulted (the reason for the drawer was opened) then the fault LED for this drive should be blink at 2Hz continuously during this mode so it is still easily identified.
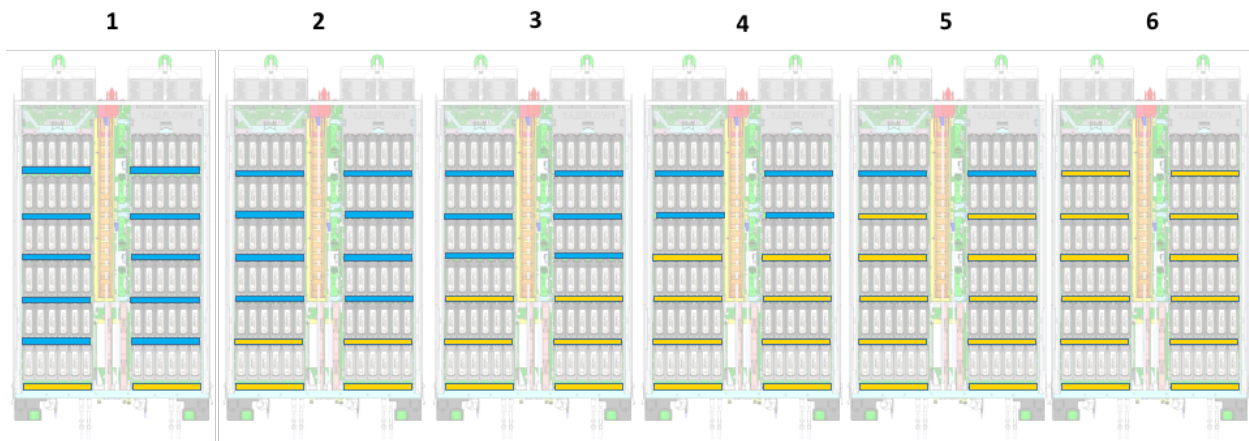
16 Internal Cables

16.1 JBOD Connection Bracket

When the Bryce Canyon system is used as a JBOD, a bracket is installed with external MiniSAS HD connectors that route into the Storage Controller Cards. An image of this connector is shown below.
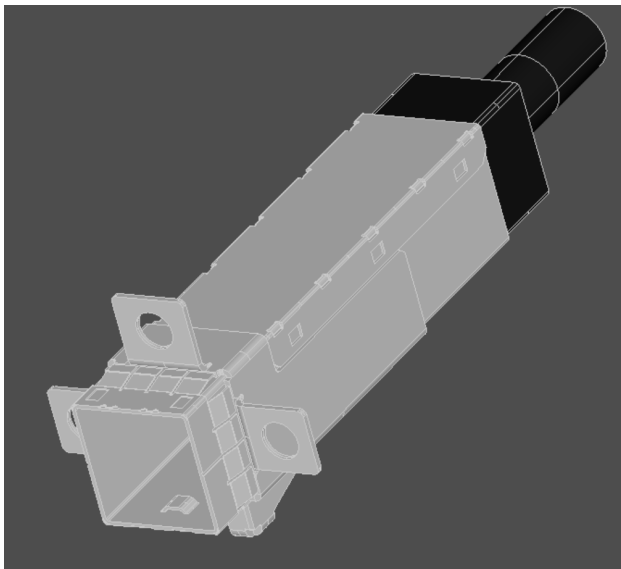
Figure 72. MiniSAS HD cable connector CAD model

This connector will terminate to an internal MiniSAS HD that plugs into the SCC. There will be two cable lengths, one that routes to the front SCC, and one that routes to the rear SCC. A cable rendering is shown below. (Cable length TBD, internal side changed to right angle)
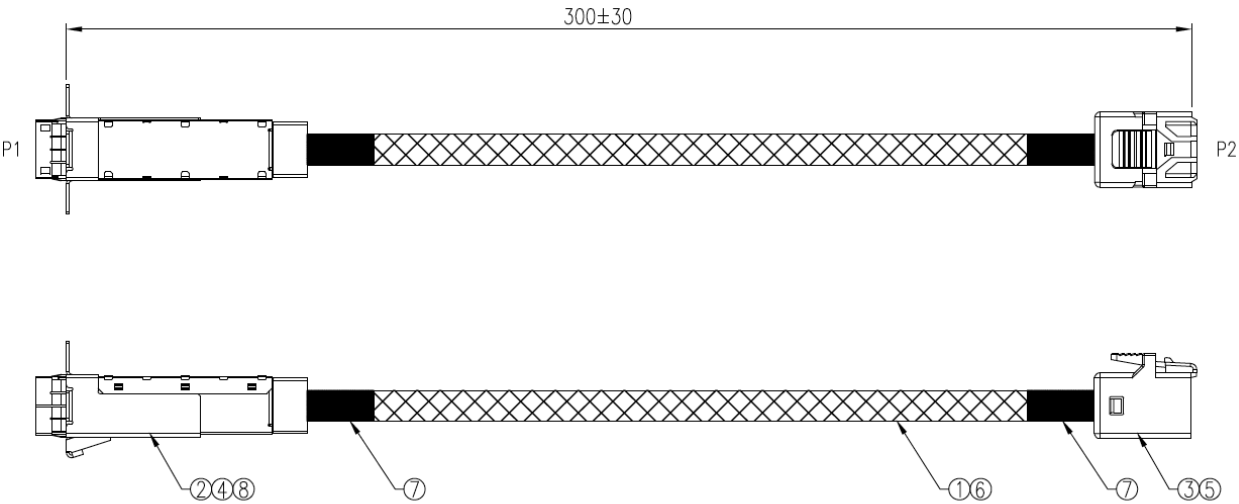
Figure 73. MiniSAS HD Cable drawing

The image below shows a side view of the Bryce Canyon system and how this will be used in the JBOD configuration.
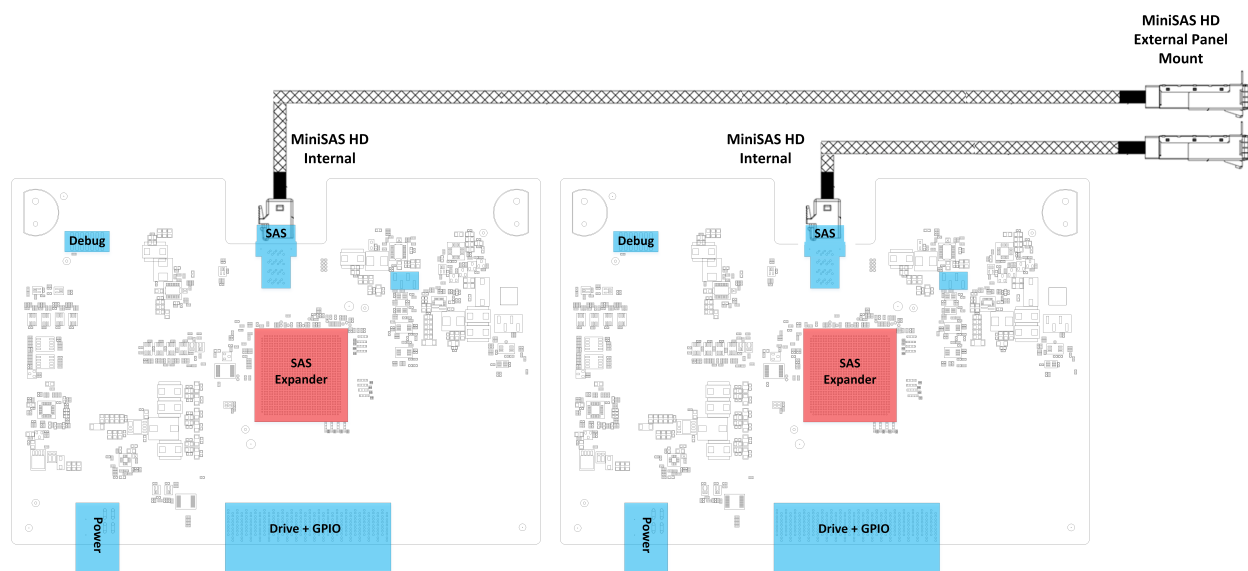
Figure 74. MiniSAS cabling drawing (side view)

16.2 Single Server SAS cable

When Bryce Canyon is used as a single storage server, the compute module needs to access all 72 drive slots. To do this, there will be an internal x4 SAS cable connecting the two SCCs. In order to make the cabling easier, this cable should have a 90-degree angle on both ends of the cable assembly, oriented as shown in the image below.
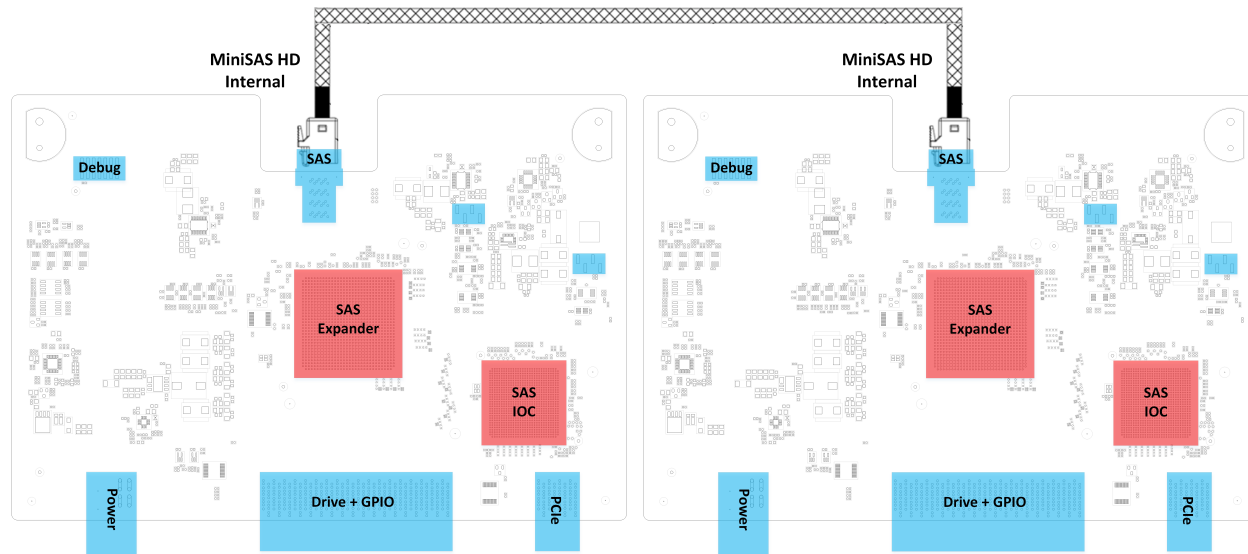
Figure 75. MiniSAS Single server cable drawing

17 Mechanical

This section outlines the mechanical design requirements of the system.

17.1 Overview

[Placeholder for pictures demonstrating top-down view, labeling of components]

Component Details

Thermal	4x dual rotor 92 mm fans
Power	ORv2 bus bar clip
Storage Protocol	2x Storage Controller Card
Serviceability	Cable track for hot swap
	Sliding rails
Compute	2x 1S Server Slot (MonoLake + Next Gen)
Network + extensibility	Personality module
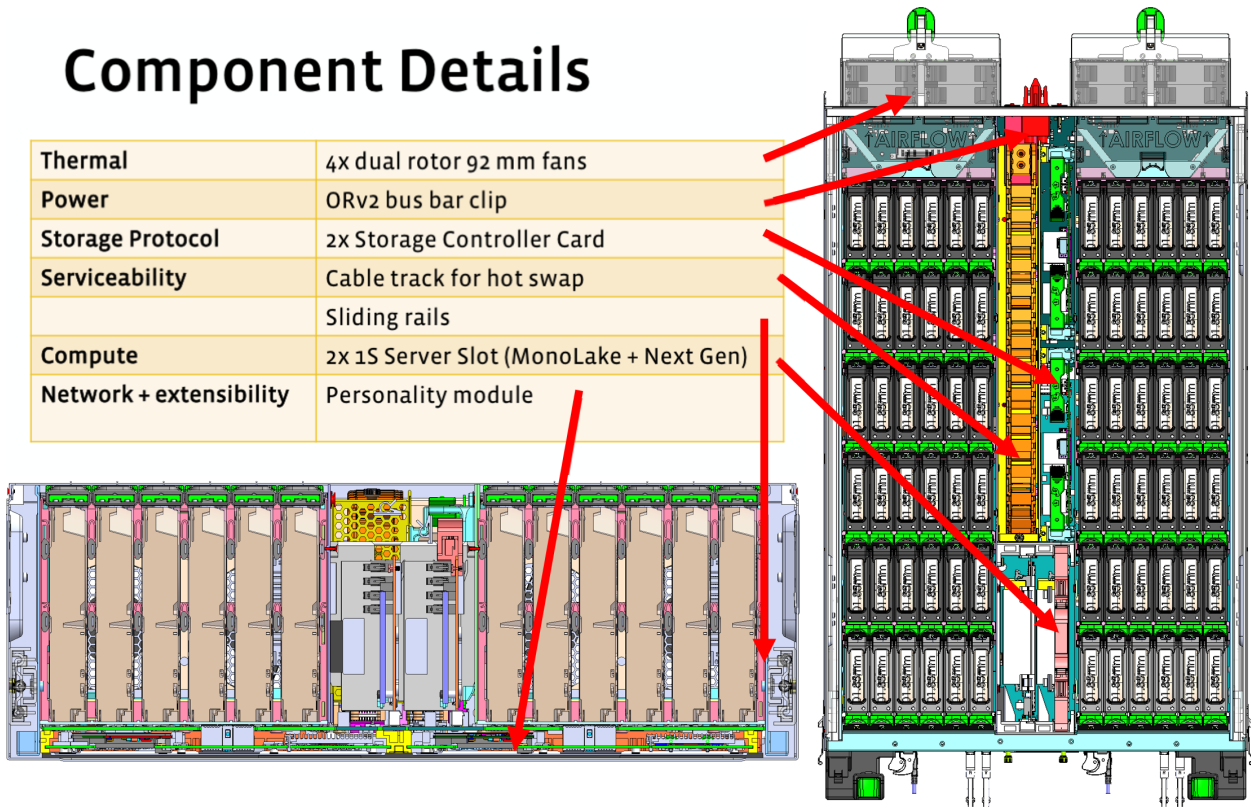
Figure 76. System mechanical layout

17.2 Overall dimensions

The system shall fit into the OCP rack V2.0 without any modifications.
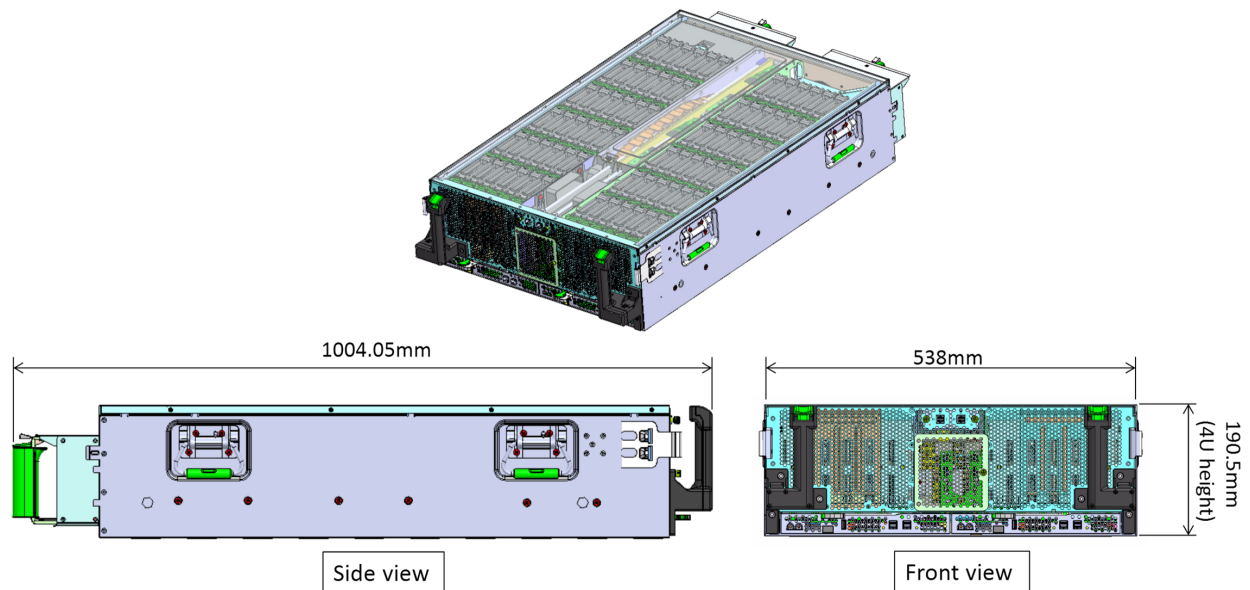
Figure 77. Overall dimensions
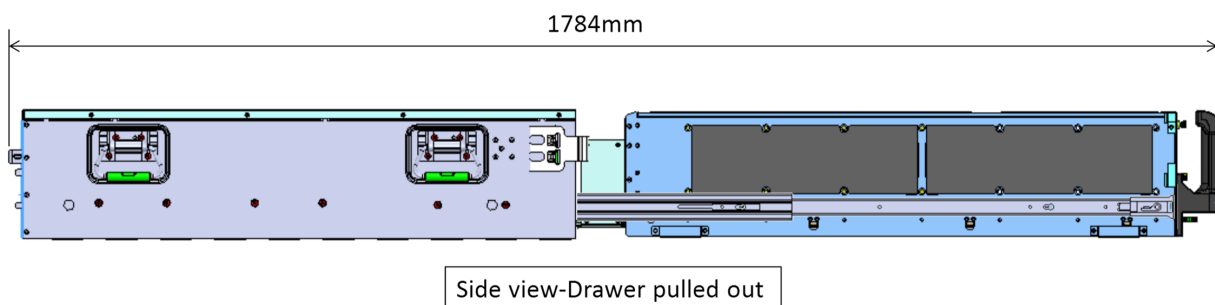
Figure 78. Dimensions with drawer pulled out

17.3 Rotational vibration requirements

The system must be designed so that there is minimal degradation due to the system design. Several areas contribute to negative drive performance impact, such as surrounding disk drives and the fans. The system must be designed so that over the operating conditions, all drives are able to perform at >= 90% of their ideal throughput/IOPS as tested on a bench.

The only exception to the requirements above are during drawer removal and insertion operations for service. During these events, it is acceptable for the drive performance to be affected, but there must be no damage to the drives themselves (for example, head touchdown, etc.).

[Placeholder for isolating material, contact points on drive, minimizing of metal-to-metal contact, dampening of slide rails on inner/outer X mm of engagement]

Fans shall be held against the chassis with rubber isolating material to minimize the vibration induced on the drive from the fan rotation.

17.4 Weight requirements

In order to not exceed the max fully loaded of 1134kg for elevated floor requirements, max weight of the chassis shall not be more than 42kg (not including hard drives). Further weight reductions shall be introduced to keep the rack as lightweight as possible to ease transportation and loading.

CG (304.4, 412.3,1047.4)   CG (304.4, 497.7,1058.2)   CG (304.3, 405.3,1072.9)

Total≈ 1111.73 kg   Total≈1129.73 kg   Total≈ 1148.83 kg
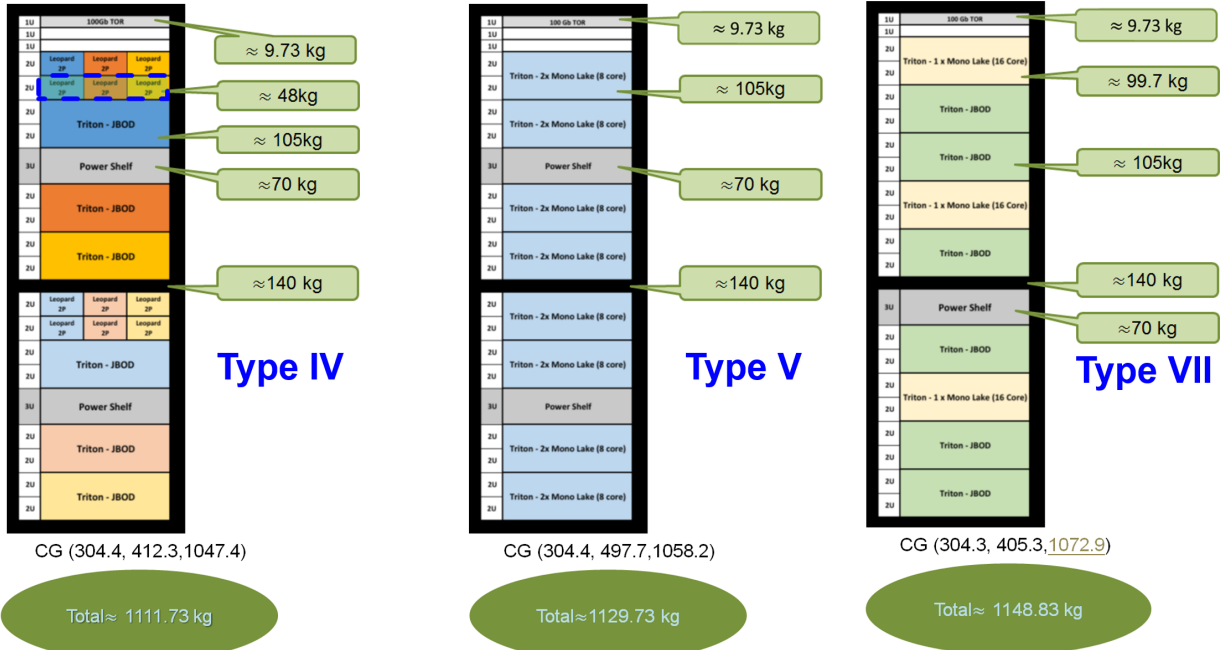
Figure 79. Current weights for different rack types

17.5 Drawer structural walls

To minimize weight requirements, sheet metal in inner structural walls is cored out to reduce weights; subcomponents that do not contribute to structural rigidity are replaced with thinner sheet metal or plastic materials.

Front ISO view   Back ISO view
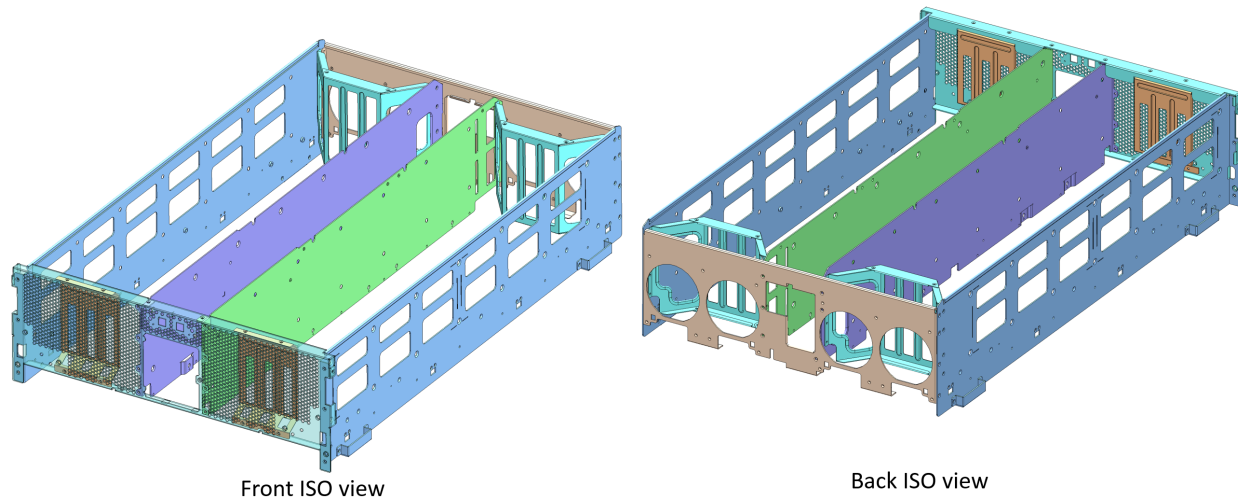
Figure 80. Drawer structural wall undergoes weight savings

17.6 Sliding rail

[Placeholder for sliding rail requirements, e.g., extension length, dampening of slide rails on inner/outer X mm of engagement]

17.7 Cable track

The cable track is present to control the 12V input power cables. This shall be a plastic material with the appropriate length to allow the drawer to fully extend. Cable tracks shall rotate freely and be able to fold and unfold themselves without any resistance.
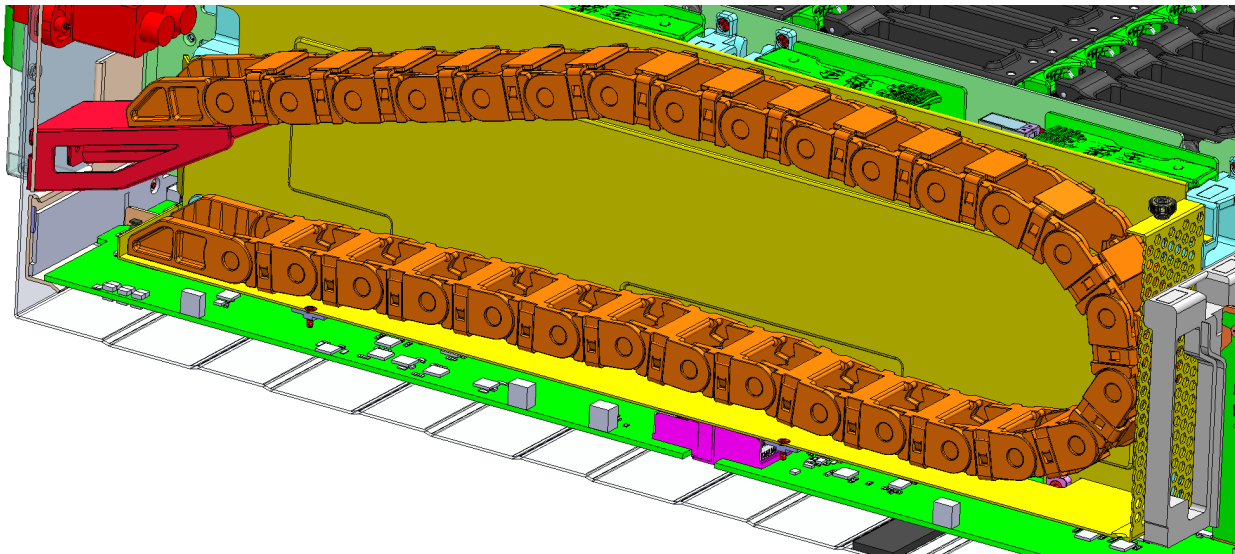
Figure 81. Cable track inside the system

17.8 Drawer Release handles and latching

TBD

17.9 Rack retention latch

The chassis implements a latch to be able to withstand minimum of 50kg. The chassis shall be folded away all the time to ensure the system slides freely into the rack. The handle shall be rubberized and green in color for easy handling.
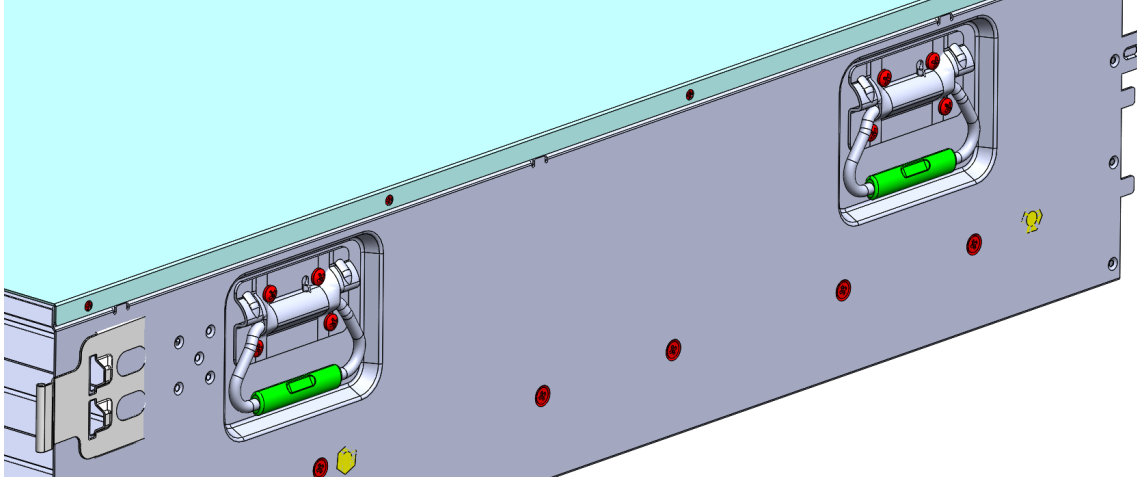
Figure 82. Chassis latches

17.10 Drive retention

Drive retention shall be designed around the form factor outlined in SFF-8301 specification, rather than a specific drive model. The latching mechanism must support all SFF compliant 3.5" HDDs adhering to the 26.1mm max height.
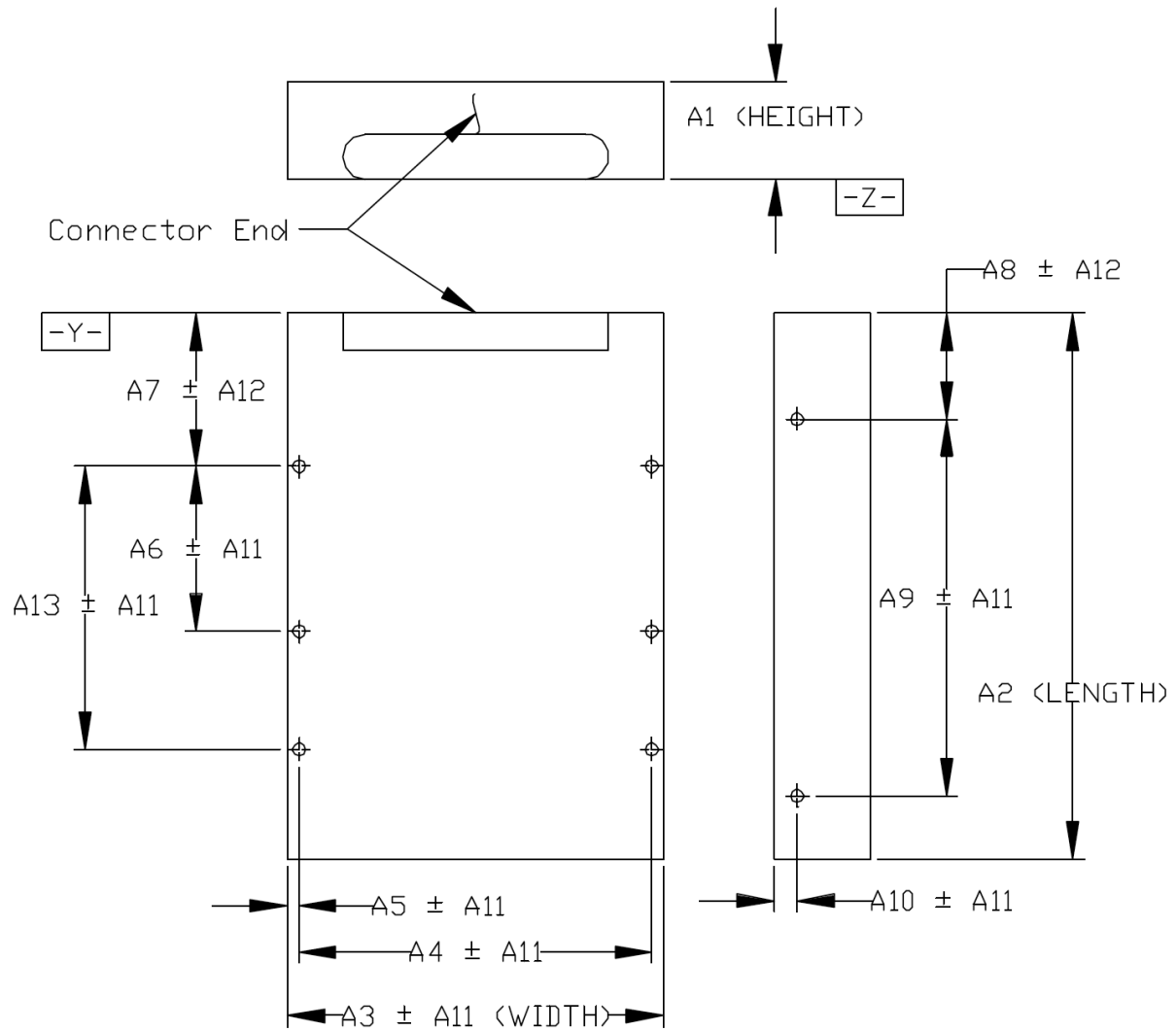
Figure 83. Drive retention drawing

Table 25. Drive retention HDD dimension table

```
TABLE 4-1 3.5" DISK DRIVE DIMENSIONS
+----------+----------+----------+
| Dimension |Millimeters|  Inches  |
+----------+----------+----------+
| A 1      |   17.80 * |   0.700 * |
| A 1      |   26.10 * |   1.028 * |
| A 1      |   42.00 * |   1.654 * |
|     A 2  |  147.00 * |   5.787 * |
|     A 3  |  101.60   |   4.000   |
|     A 4  |   95.25   |   3.750   |
|     A 5  |    3.18   |   0.125   |
|     A 6  |   44.45   |   1.750   |
|     A 7  |   41.28   |   1.625   |
|     A 8  |   28.50   |   1.122   |
|     A 9  |  101.60   |   4.000   |
|    A10   |    6.35   |   0.250   |
|      A11 |    0.25   |   0.010   |
|      A12 |    0.50   |   0.020   |
|    A 13  |   76.20   |   3.000   |
+----------+----------+----------+
         * = maximum
```

The hard drive latch should be designed in such a way as to allow for the barcode of an installed hard drive to be scanned without unseating the drive, thereby providing a means to verify the identity of a drive prior to removing it for service. In addition, the latching feature must be able to lift the drive a minimum of 20mm above the adjacent drive slots and/or any other obstructions to make the removal and insertion of the drive easier.

[Placeholder for drive latching]

17.11 I/O Module

[Placeholder]

17.12 Storage Controller Card

[Placeholder]

17.13 Front I/O Panel

17.13.1 PCB Details

17.13.1.1 PCB Key dimensions
The figure below shows the PCBA outline for Front I/O panel.
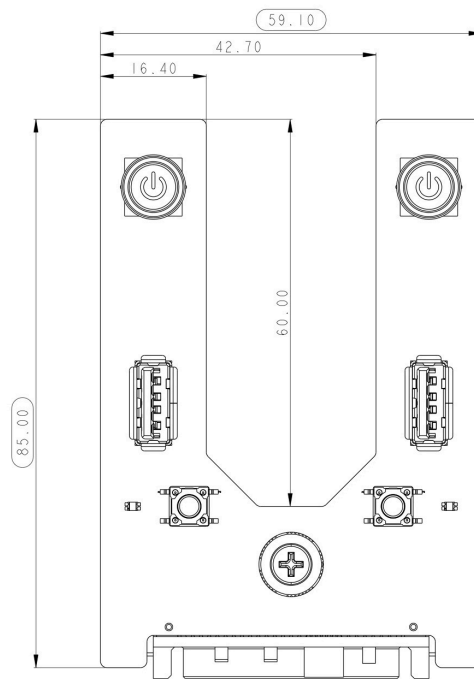
Figure 84. Front I/O panel PCBA outline

17.14 LED Board

17.14.1 PCB Details

17.14.1.1 PCB Key dimensions
The figure below shows the PCBA outline for the LED board.
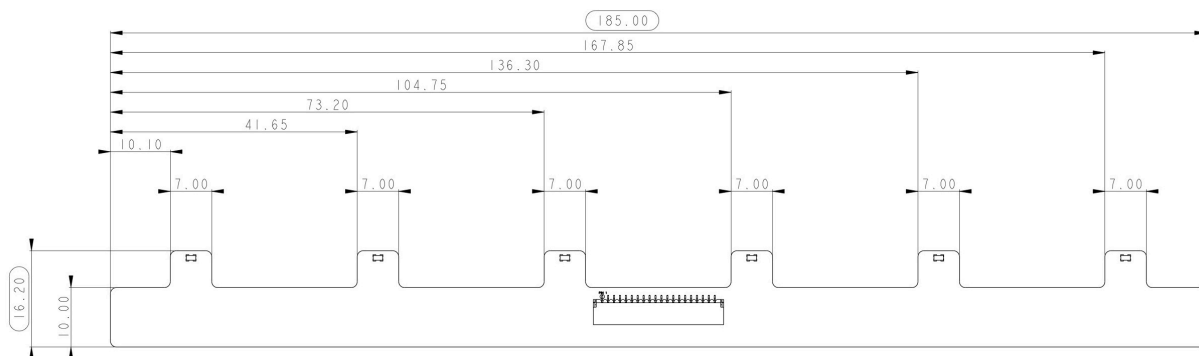
Figure 85. LED board PCBA outline

18 Thermal

This section outlines the thermal design of the Bryce Canyon platform.

18.1 Fans

The main configuration of Bryce Canyon shall use four (4) 92mm dual-rotor counter-rotating fans. For the cold storage configuration of Bryce Canyon, there will be two (2) 92mm options to reduce the airflow and power of the system.

The diagram below shows the fan curves under the various duty cycles, which are required to meet for Bryce Canyon.
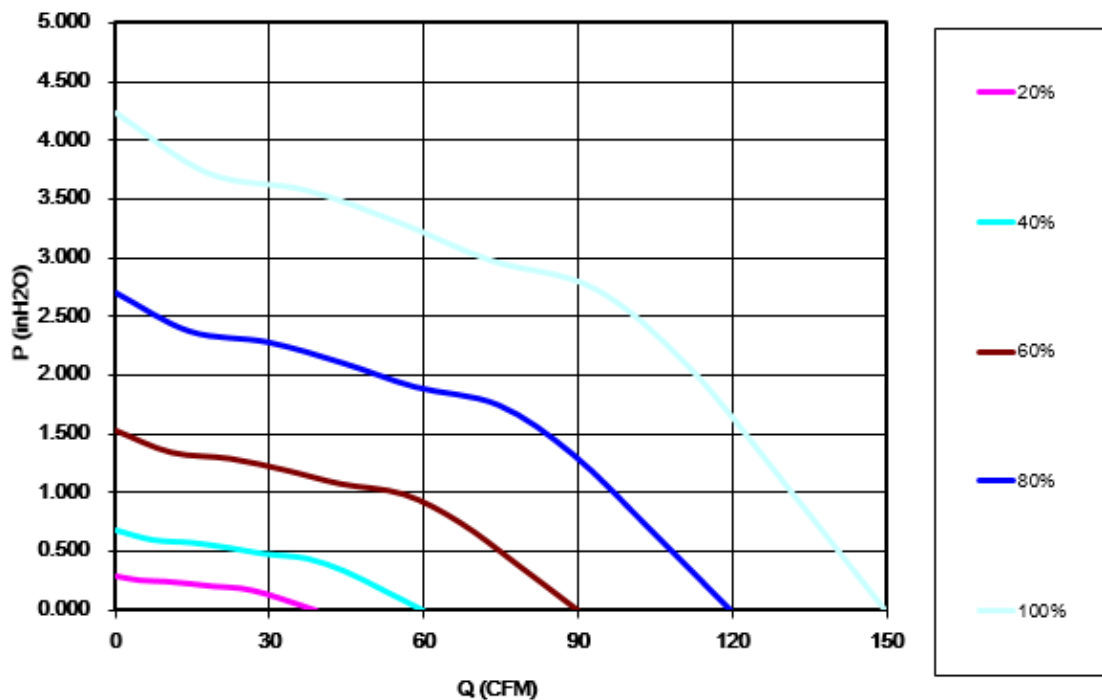
Figure 86 - Bryce Canyon Fan Curves

18.2 Cooling Zones

The Bryce Canyon system has two zones to control the PWM to the fans. These are referred to as Zone C for the center compute section, and Zone D for the drive areas. There are two fans connected to each zone. The BMC on the IOM only outputs PWM to Zone C, and the SCC controls both Zones C & D. In the cold storage configuration, the fans in Zone D are not populated. Due to the plenum design, the system can still be effectively cooled by using the Zone C fans.
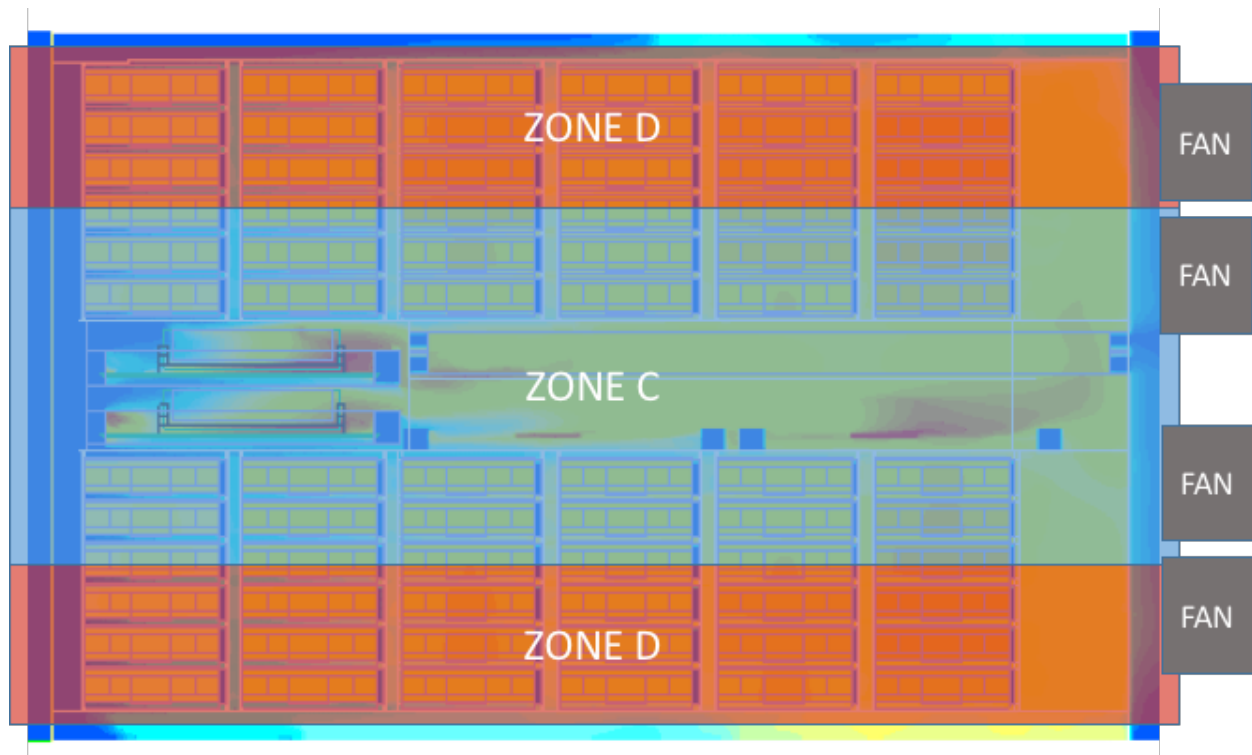
18.3 92mm Fan Module

The fan module shall have ergonomic handles to ease replacement. Fans shall overhang on rubber material to isolate fan rotational vibrations that affect hard drive performance. To further isolate the fan module from the system, the interface surfaces with the surface shall have a layer of dampening material. The fan cage shall protect the fan blades from the operator to avoid cut injuries.
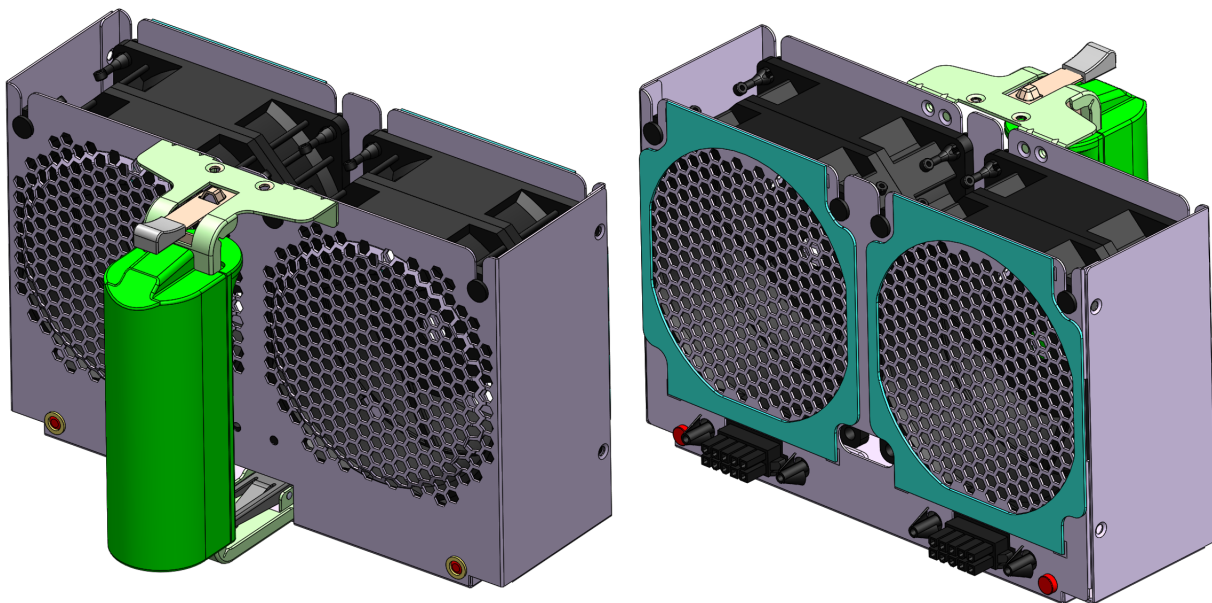
Figure 87. Fan module Front and Back ISO views
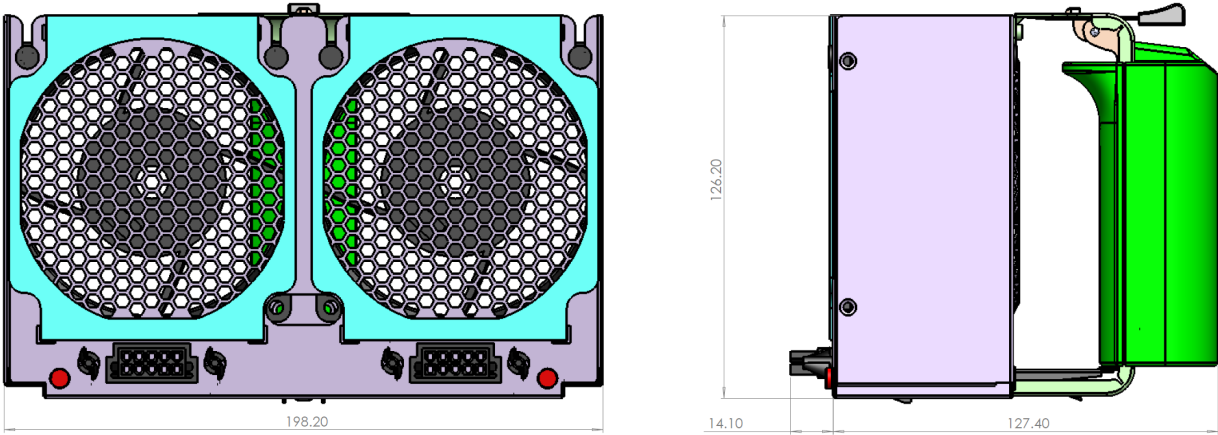
Figure 88. Fan Module Dimensions

18.4 Air baffles

One of the most important aspects of the thermal design is to keep the drives cool. To assist this, ducting may be implemented to redirect fresh (cold) air from the front of the chassis to help cool the back three rows of drives. Channels would be cut out of the PCB and an air baffle would be installed in the base of the chassis, as shown in Figure 89.
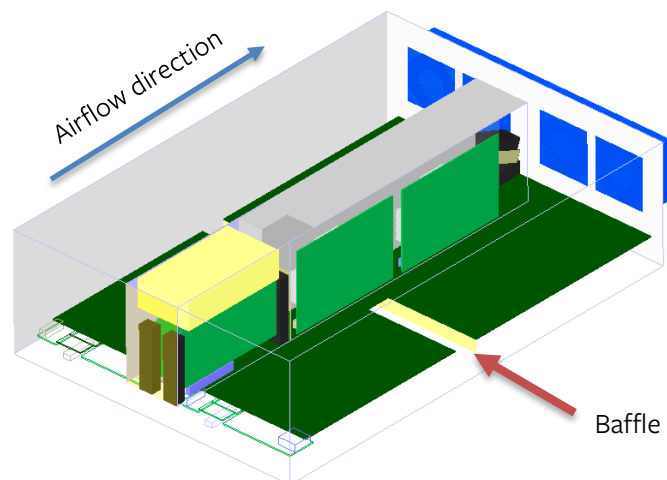
Figure 89. Air baffle for drive cooling

The effect of this is shown in Figure 90, which is a side profile of the system showing the cold air mixing with warm air at the bottom of the chassis.
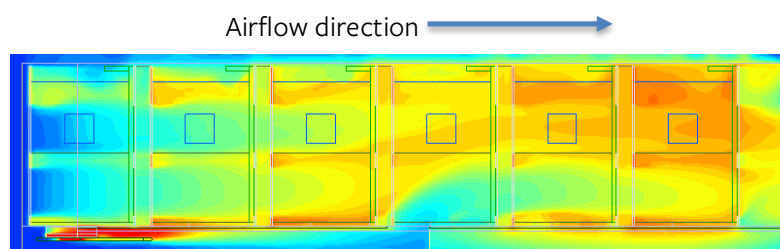
Figure 90. Effect of thermal baffle on drive temperature

To optimize the cooling in Zone C, the air baffles are required to minimize the air bypass and increase approaching velocity for the higher heat transfer rate. The red color in Figure 90 and Figure 91 are showing the placements of the SCC and server air baffles.
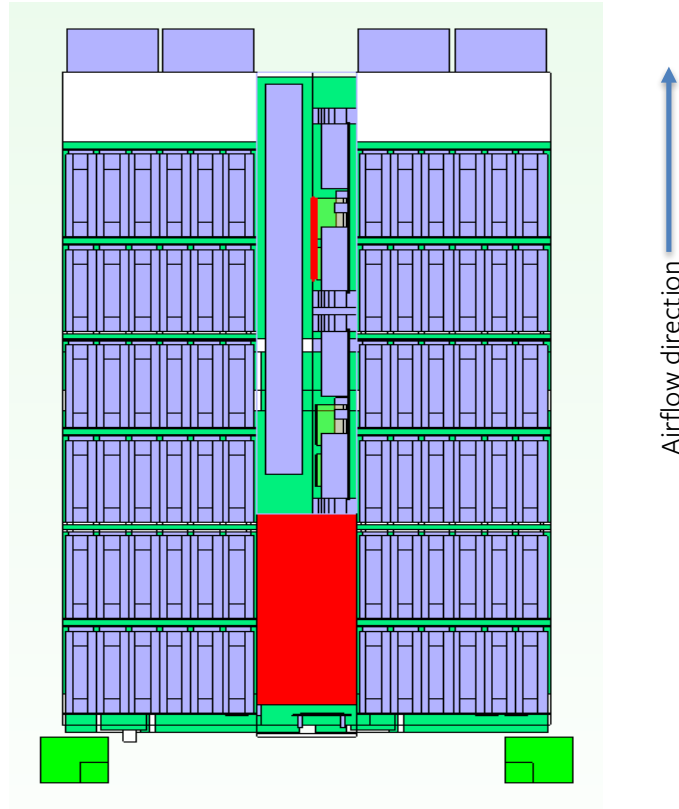
Figure 91: Red color indicates the SCC and Server baffle placements
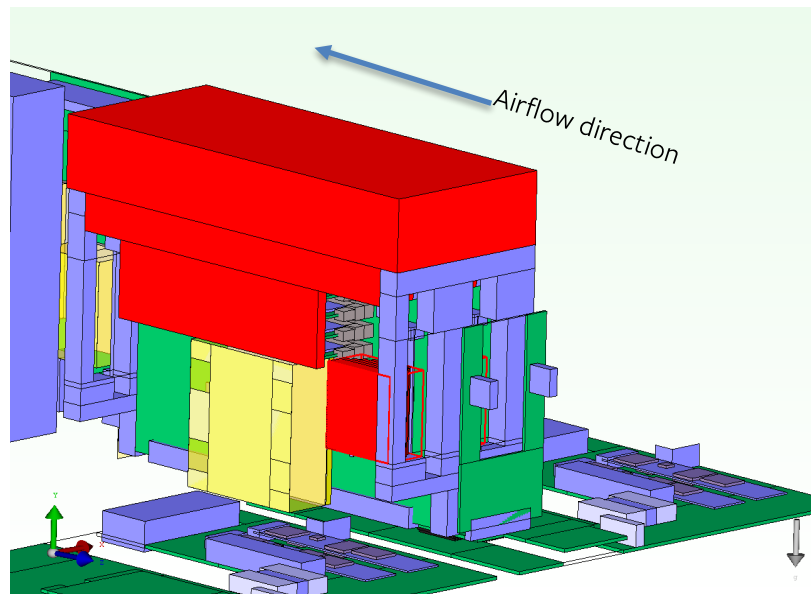
Figure 92: Detail baffle placement in server cards

For Coldstorage Bryce Canyon Type VII or single server configuration, the dummy server will be required to limit the air bypass through the empty slot.
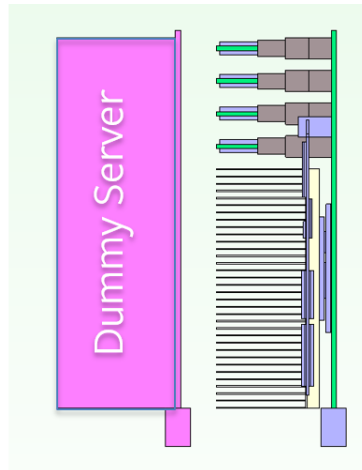
To enhance the cooling for M.2 drives or the super-cap in IOM modules, the proper air baffles will be needed to guide the airflow into M.2 drives. Figure 92 shows the possible location for the air baffle in red.
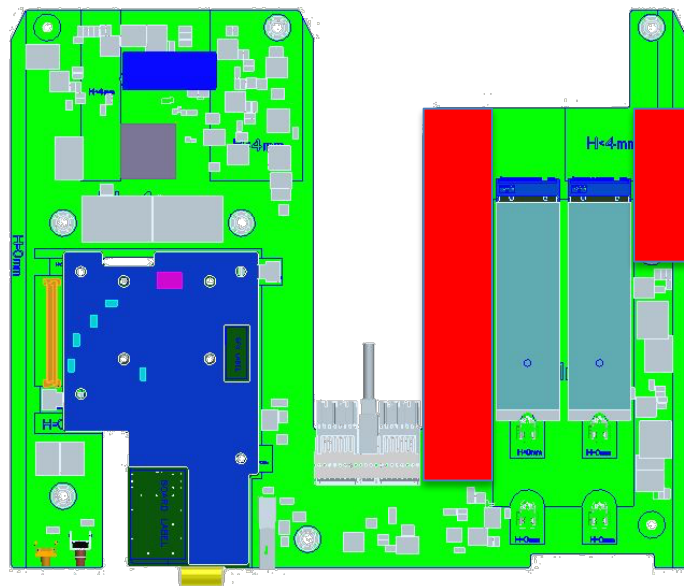
Figure 93 : The possible location for Air baffles in IOM Module

19 Thermal Design Requirements

To meet thermal reliability requirements, the cooling solution should dissipate heat from the components when the system is operating up to its maximum thermal power. The final thermal solution of the system should be most optimized and energy efficient under data center environmental conditions with the lowest capital and operating costs. Thermal solution should not allow any overheating issue for any components in the system.

19.1 Data Center Environmental Conditions

This section outlines Facebook data center operational conditions.

19.1.1 Location of Data Center/Altitude

Maximum altitude is 6,000 feet above sea level. Any variation of air properties or environmental difference due to the high altitude needs to be deliberated into the thermal design.

19.1.2 Cold-Aisle Temperature

Data centers generally maintain cold aisle temperatures between 18°C and 30°C (65°F to 85°F). The mean temperature in the cold aisle is usually 25°C with 3°C standard deviation. The cold aisle temperature in a data center may fluctuate minutely depending on the outside air temperature. Every component must be cooled and must maintain a temperature below its maximum specification temperature in the cold aisle.

19.1.3 Cold-Aisle Pressurization

Data centers generally maintain cold aisle pressure between 0 inches H_2O and 0.005 inches H_2O. The thermal solution of the system should consider the worst operational pressurization possible, which generally is 0 inches H_2O and 0.005 inches H_2O with a single fan (or rotor) failure.

19.1.4 Relative Humidity

Data centers generally maintain a relative humidity between 20% and 90%.

19.2 Server Operational Conditions

19.2.1 Inlet Temperature

The inlet air temperature will vary. The cooling system should cover inlet temperatures 20°C, 25°C, 30°C, and 35°C. Cooling above 30°C is beyond the Facebook operational condition, but used during validation to demonstrate the thermal reliability and design margin. Any degraded performance is not allowed over the validation range 0°C-35°C.

19.2.2 Pressurization

Except for the condition when one rotor in a server fan fails, the thermal solution should not consider extra airflow from data center cooling fans. If and only if one rotor in a server fan fails, the negative or positive DC pressurization can be considered in the thermal solution in the hot aisle or the cold aisle, respectively.

19.2.3 Fan Redundancy

The server fans at N+1 redundancy should be sufficient for cooling server components to temperatures below their maximum specification to prevent server shut down or to avoid any defect of failure.

19.2.4 Delta T

The Delta T is the air temperature difference across the system, or the temperature difference between the outlet air temperature and the inlet air temperature. The Delta T must be greater than 12.2°C (54°F) when the server is running within the data center operational condition. The desired Delta T is greater than 13.9°C (57°F).

19.2.5 System Airflow or Volumetric Flow

The unit of airflow (or volumetric flow) used for this spec is cubic feet per minute (CFM). The CFM can be used to determine the thermal expenditure or to calculate the Delta T of system in approximation. The thermal expenditure is quantified by the metric CFM/W, which is calculated by the following formula:

$$\text{Thermal Expenditure} = \frac{\text{System airflow}}{\text{Total system power consumption, including fans}} \ [\text{CFM/W}]$$

At sea level, the maximum allowable airflow per watt in Bryce Canyon rack is 0.1625 at 30°C inlet temperature under the normal load or 9kW rack power. As the rack power increases, the maximum allowable airflow decrease up to 0.145.

The allowable CFM/W for Bryce Canyon server can vary by the system SKU or system loading. Please see the curves below for the maximum allowable CFM/W in Bryce Canyon under the different system power.

Note: Bryce Canyon without Mono Lake cards is the approximation curve, which can vary by up to 10%.
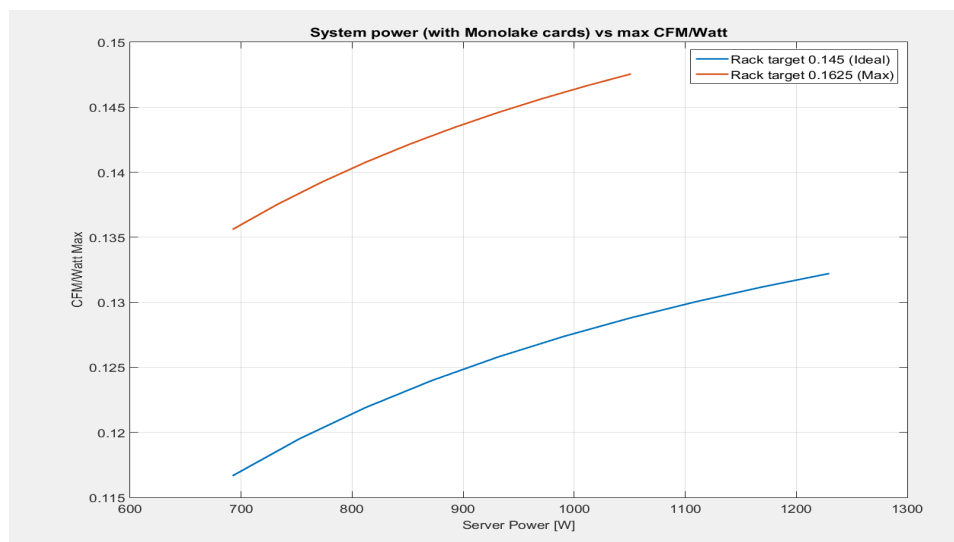
Figure 94. System power vs. CFM/W (with Mono Lake)
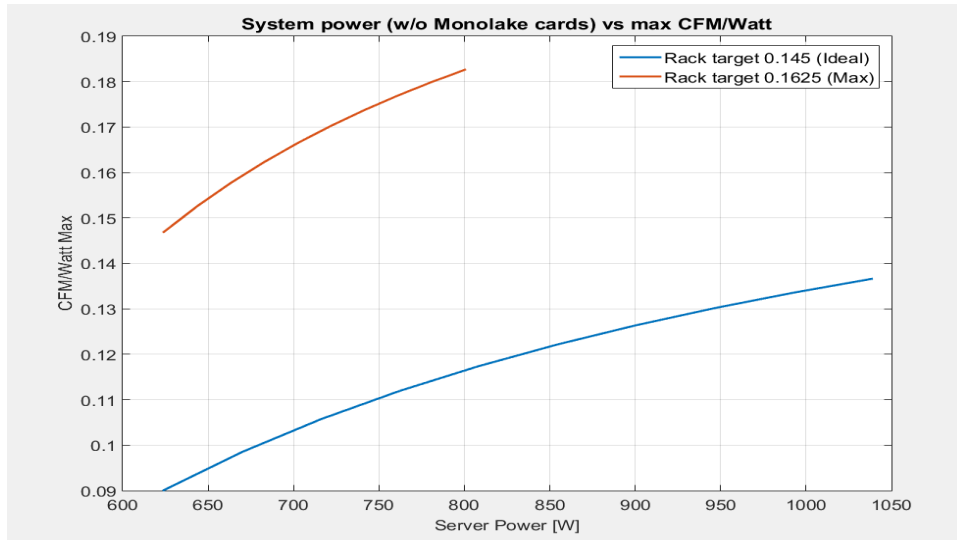
Figure 95. System power vs CFM/W (without Mono Lake)

19.2.6   Thermal Margin

The thermal margin is the difference between the maximum theoretical safe temperature and the actual temperature. Unless specified, the system should operate at an inlet temperature of 35°C (95°F) outside of the system with a minimum 4% thermal margin or 7% thermal margin for inlet temperatures up to 30°C.

Table 26. Thermal margin by component

Component	Minimum Thermal Margin required in degrees C
HDD	5
Broadwell-DE CPU	10
DIMM	5
NIC main chip	15
M.2 NAND	3

19.2.7   Thermal Sensor

The maximum allowable tolerance of thermal sensors is ±2°C.

19.2.8   DDR DIMM DRAM Operation

The thermal design should meet the DIMM (or DRAM) max operating temperature (85°C with a single refresh rate). Thermal test should be done based on a DIMM module's AVL (Approved Vendor List). The Vendor should implement BIOS and memory subsystem to have optimized refresh rate and utilize optional DIMM Auto-Self-Refresh (ASR) based on DIMM temperature. The implementation should follow updated DDR3/DDR4 memory controller and DIMM vendor's specification.

20 Serviceability

20.1 Service touch points

All user touchpoints (latches, thumbscrews, etc.) shall be colored Pantone PMS 375C.

20.2 Drawer Opening Procedure

Two green buttons, one on each handle, need to be pressed down to eject the drawer out for servicing.

1. Push button for releasing latch

2. Pull the drawer out
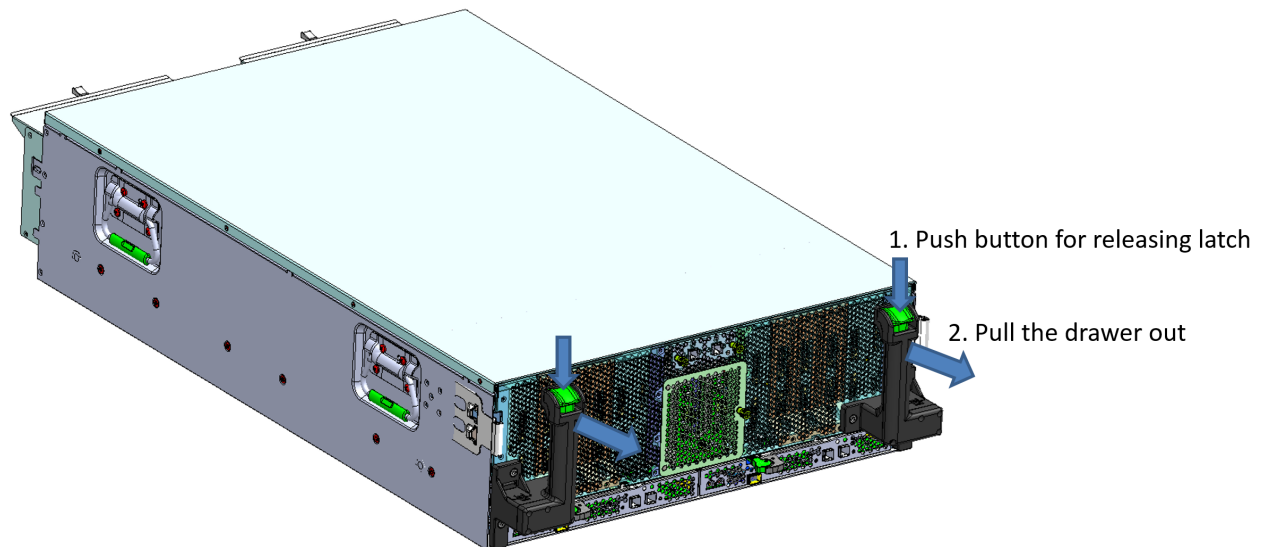
Figure 96. Drawer handles and release buttons

20.3 Drawer release backup mechanism

In the case that the handle latch fails to disengage to remove the drawer, there's a small hinged cover that can be flipped up. Insert a flat head screwdriver to disengage the drawer lock.

If handle lock mechanism is stuck.

1.Open the small cover

2.Use a tool(screwdriver) to push release mechanism to unlock rail.
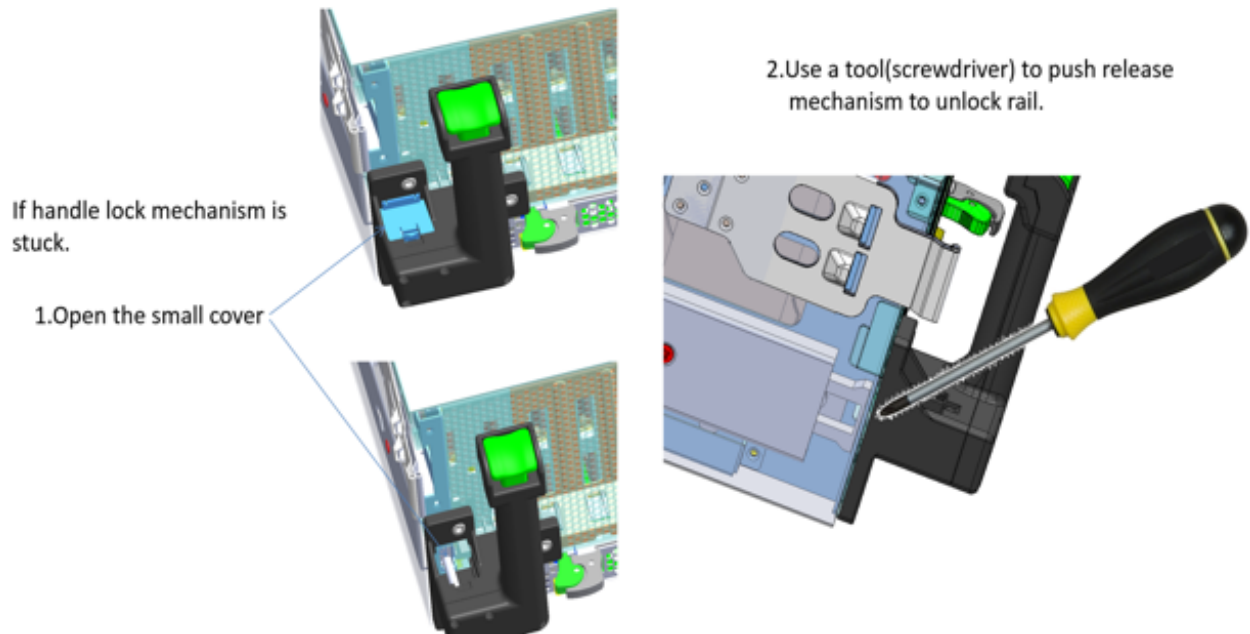
Figure 97. In the event pullout handle failure

20.4 IOM Servicing

In the event that the IOM or one of its components is required to be removed, there are simple latches that hold the module in. The green latch can be compressed to disengage the lock, pulling the latch out will disengage the IOM from the system.

Push green part and rotate the latches to release IOM.

Figure 98. IOM servicing

20.5 Front panel board access or removal

When the front panel board requires access, loosen the green thumbscrew to open the front faceplate cover. This exposes the system's power button and the SCC reset button. If the board needs replacement, the front IO board can be removed by loosening the thumb screw and pulling the board up to disengage from the connector.

1.Loosen the thumb screw of cover to remove the cover

2.Loosen the thumb screw of front board
   to maintain the front board
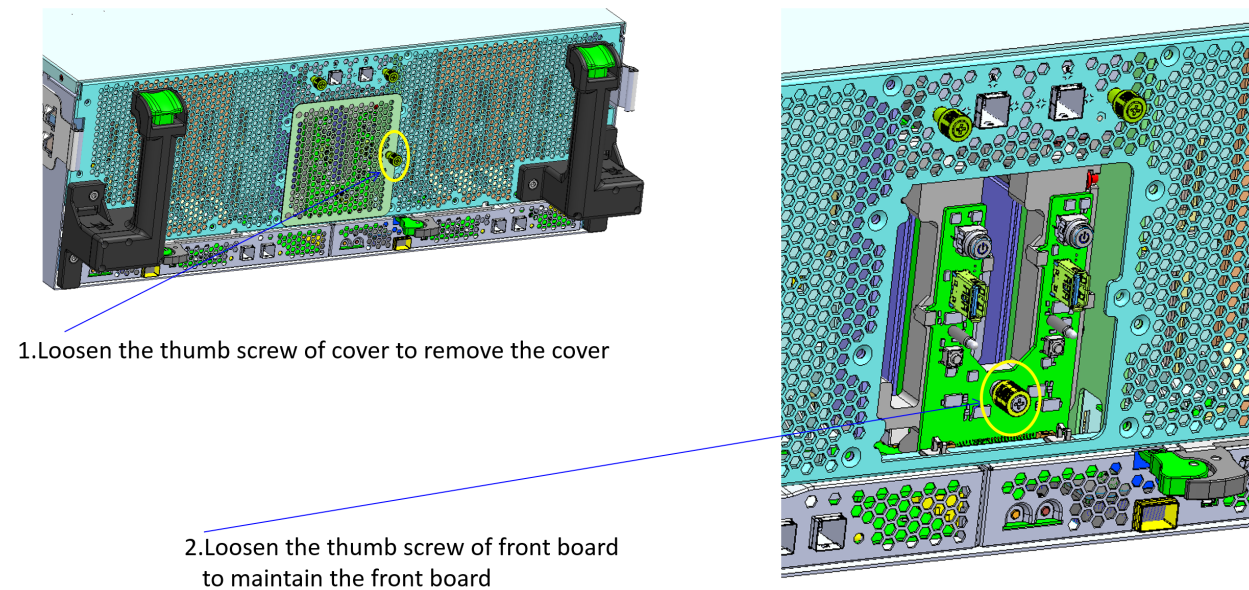
Figure 99. Front IO board access or removal

20.6 Fan cage replacement

In the event of fan failure, the fan module can be replaced by pushing the green button down and pulling the fan module out. Installing a new fan module can be done by reversing the removal steps.

1.Push the button to release the fan tray
2.Pull the fan cge out
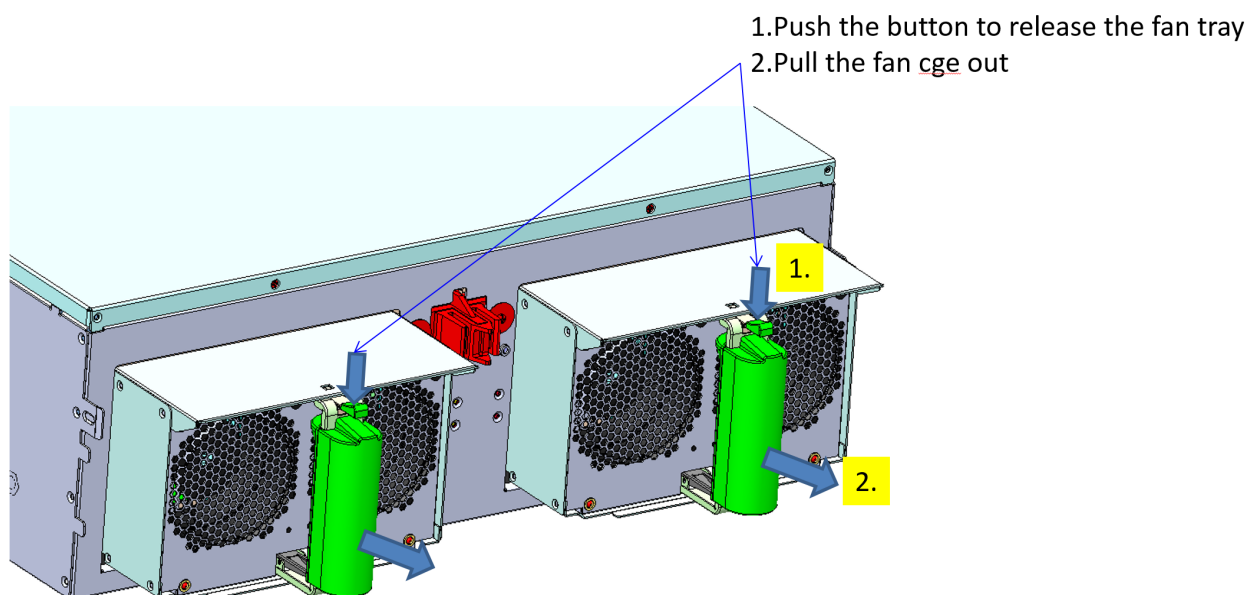
Figure 100. Fan Module replacement

20.7 CPU module replacement

If the CPU module needs to be replaced or serviced, the air baffle needs to be removed from the system to gain access. Next, the CPU module can be removed by pinching and pulling on the CPU module latch.

1.Take Mono lake air baffle off

2.Release Mono lake latch and pull Mono lake up.
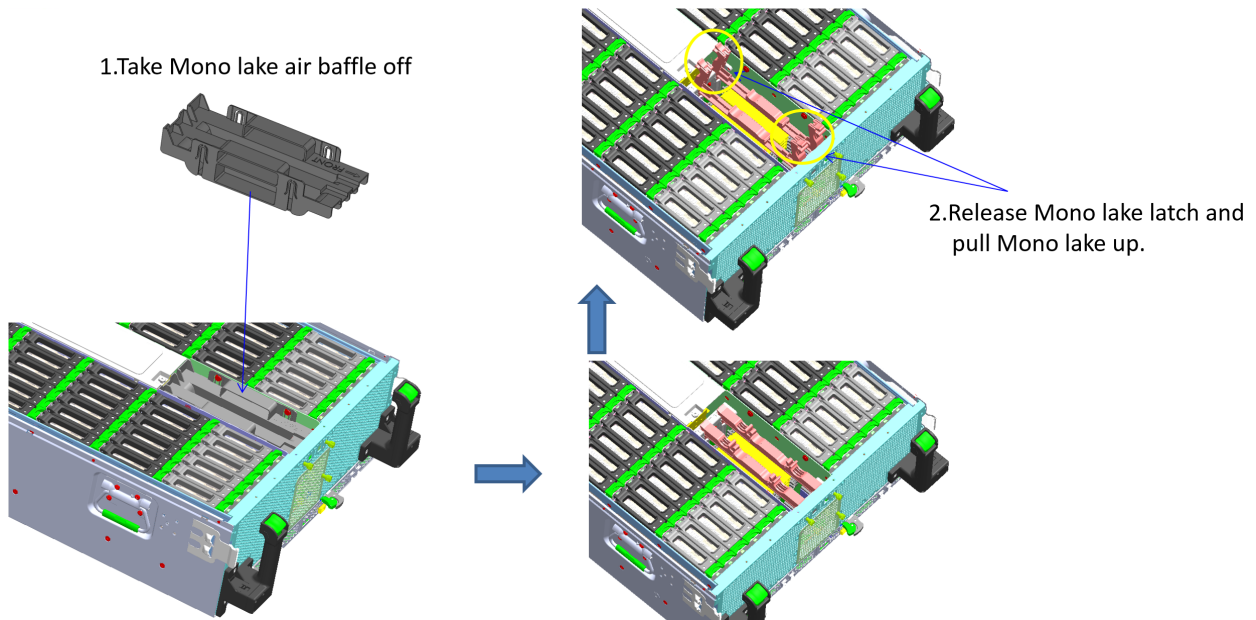
Figure 101. CPU module replacement

20.8 Storage Controller Card replacement

In the event the Storage Controller Card needs to be replaced, the top cover needs to be removed by loosening the green thumbscrew and taking off the cover. Next, pull the green latches on the expander card forward, and rotate the latches up to disengage the module from the system.

2.Release SCC latch and pull SCC up.

1.Loosen the thumb screw of drawer rear top cover to remove the it.
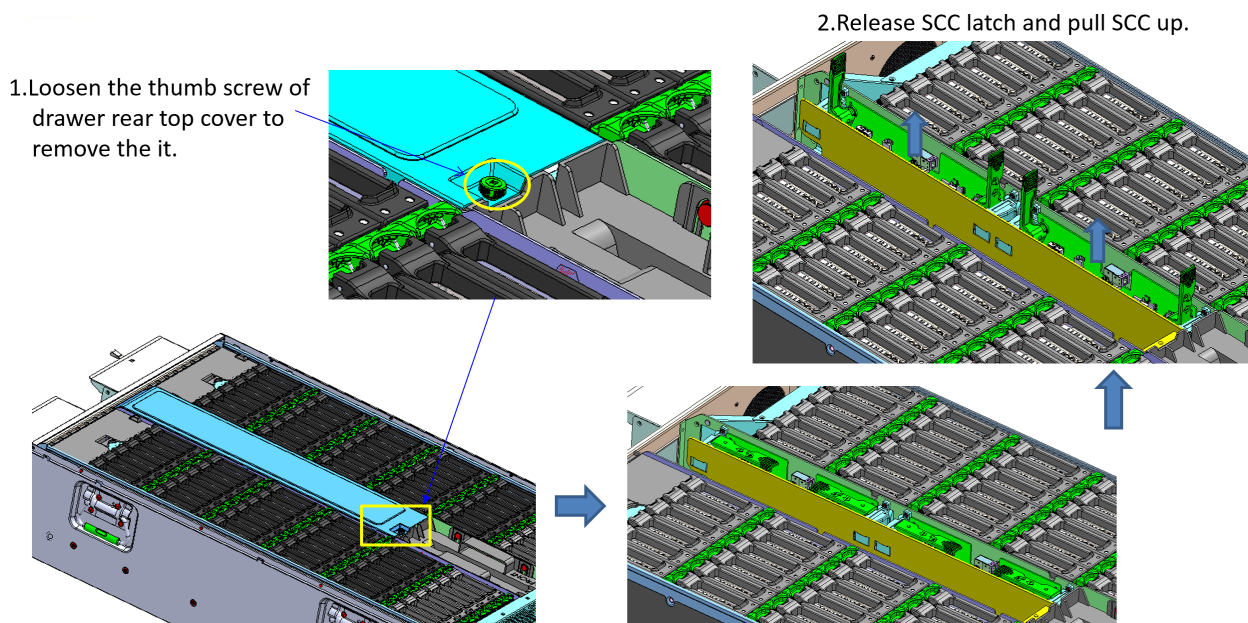
Figure 102. Expander card module replacement

21 System Reliability and Longevity

[Placeholder]

22 Manufacturing and Testability

22.1 JTAG Requirements

Any board that contains an ASIC that has JTAG boundary scan capabilities should implement the XDP JTAG header support, or make the necessary JTAG signals available via test points on the PCB, which are accessible to the ICT test fixture. The test points should also be large enough to enable wired connection if debug becomes necessary.

The PCBs that have JTAG test points include the SCC as well as the IOM. The SCC has JTAG available for the SAS Expander IC as well as the SAS IOC. The Type 7 IOM PCB has JTAG test points available for the SAS IOC.

22.2 Test Point Coverage

Please reference the Facebook manufacturing and DFM guidelines for test point coverage guidelines and criteria.

23 Connector Pinouts

This section outlines the pin definitions for all connectors used in Bryce Canyon.

23.1 Busbar
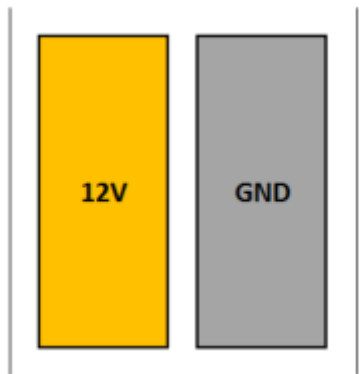
Figure 103: Bus Bar connector pinout looking from the front of the rack

23.2 12V input connector
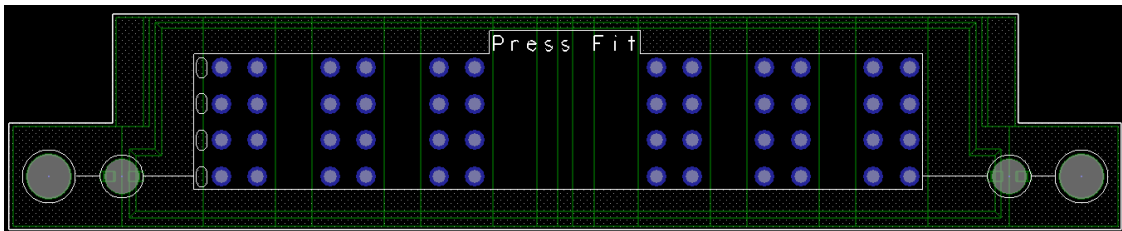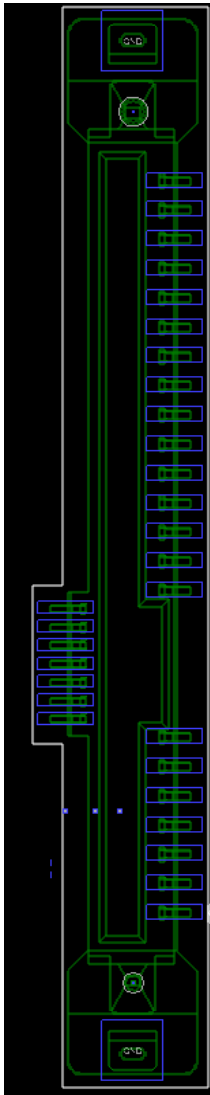
Figure 104: 12V input connector to RDPB

Table 27: 12V input connecctor pinout

P1		P2		P3			P4		P5		P6		Pin# Decoder	
GND	GND	GND	GND	GND	GND		P12V_CLIP	P12V_CLIP	P12V_CLIP	P12V_CLIP	P12V_CLIP	P12V_CLIP	1	8
GND	GND	GND	GND	GND	GND		P12V_CLIP	P12V_CLIP	P12V_CLIP	P12V_CLIP	P12V_CLIP	P12V_CLIP	2	7
GND	GND	GND	GND	GND	GND		P12V_CLIP	P12V_CLIP	P12V_CLIP	P12V_CLIP	P12V_CLIP	P12V_CLIP	3	6
GND	GND	GND	GND	GND	GND		P12V_CLIP	P12V_CLIP	P12V_CLIP	P12V_CLIP	P12V_CLIP	P12V_CLIP	4	5

23.3 Hard drive connector

Table 28: HDD connector pinout

Pin Name	Pin#		Pin Name
		P15	P12V_HDD0
		P14	P12V_HDD0
		P13	12V_PRE_0
		P12	GND
		P11	ACT_HDD_0
		P10	GND
		P9	P5V_HDD0
		P8	P5V_HDD0
		P7	5V_PRE_0
		P6	GND
		P5	HDD_PRSNT_0
		P4	GND
		P3	
		P2	
		P1	
GND	S14		
	S13		
	S12		
GND	S11		
	S10		
	S9		
GND	S8		
		S1	GND
		S2	SAS_HDD_RX_P0
		S3	SAS_HDD_RX_N0
		S4	GND
		S5	PHY_DRV_B_TO_SCC_B_0_DN
		S6	PHY_DRV_B_TO_SCC_B_0_DP
		S7	GND

23.4 Storage Controller Card power connector

Table 29: Storage Controller Card power connector pinout

Pin Name	Pin#	Pin Name
P12V_MAIN	A6 B6	GND
P12V_MAIN	A5 B5	GND
P12V_MAIN	A4 B4	GND
P12V_MAIN	A3 B3	GND
P12V_MAIN	A2 B2	GND
P12V_MAIN	A1 B1	GND
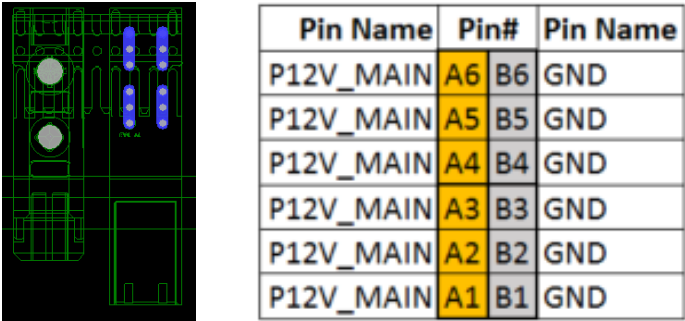
23.5 Storage Controller Card PCIe connector
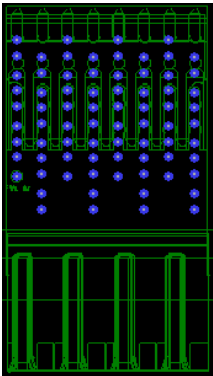
Figure 105: SCC PCIe Connector

Table 30. SCC PCIe Connector (M0) pinout

M0									Decoder	
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**			
PCIE_SCC_TO_COMP_0_DN		PCIE_SCC_TO_COMP_2_DN		PCIE_SCC_TO_COMP_4_DN		PCIE_SCC_TO_COMP_6_DN			F	
PCIE_SCC_TO_COMP_0_DP	PCIE_SCC_TO_COMP_1_DN	PCIE_SCC_TO_COMP_2_DP	PCIE_SCC_TO_COMP_3_DN	PCIE_SCC_TO_COMP_4_DP	PCIE_SCC_TO_COMP_5_DN	PCIE_SCC_TO_COMP_6_DP	PCIE_SCC_TO_COMP_7_DN		E	F
	PCIE_SCC_TO_COMP_1_DP		PCIE_SCC_TO_COMP_3_DP		PCIE_SCC_TO_COMP_5_DP		PCIE_SCC_TO_COMP_7_DP			E
PCIE_COMP_TO_SCC_CLK_0_DN		I2C_SCC_SDA2		UART_IOC_RX		BMC_RMT_HEARTBEAT			D	
PCIE_COMP_TO_SCC_CLK_0_DP	I2C_BMC_RMT_SDA1	I2C_SCC_SCL2	COMP_SPARE_0	UART_IOC_TX	BMC_SPARE_1	PCIE_COMP_TO_SCC_RST_0	I2C_BMC_LOC_SDA0		C	D
	I2C_BMC_RMT_SCL1		COMP_SPARE_0		BMC_SPARE_0		I2C_BMC_LOC_SCL0			C
PCIE_COMP_TO_SCC_0_DN		PCIE_COMP_TO_SCC_2_DN		PCIE_COMP_TO_SCC_4_DN		PCIE_COMP_TO_SCC_6_DN			B	
PCIE_COMP_TO_SCC_0_DP	PCIE_COMP_TO_SCC_1_DN	PCIE_COMP_TO_SCC_2_DP	PCIE_COMP_TO_SCC_3_DN	PCIE_COMP_TO_SCC_4_DP	PCIE_COMP_TO_SCC_5_DN	PCIE_COMP_TO_SCC_6_DP	PCIE_COMP_TO_SCC_7_DN		A	B
	PCIE_COMP_TO_SCC_1_DP		PCIE_COMP_TO_SCC_3_DP		PCIE_COMP_TO_SCC_5_DP		PCIE_COMP_TO_SCC_7_DP			A

Note: Pinout view is looking into the top side of the SCC PCBA, going left to right, with the power, SAS, PCIe connectors on the lower corner.

23.6 Storage Controller Card SAS connector
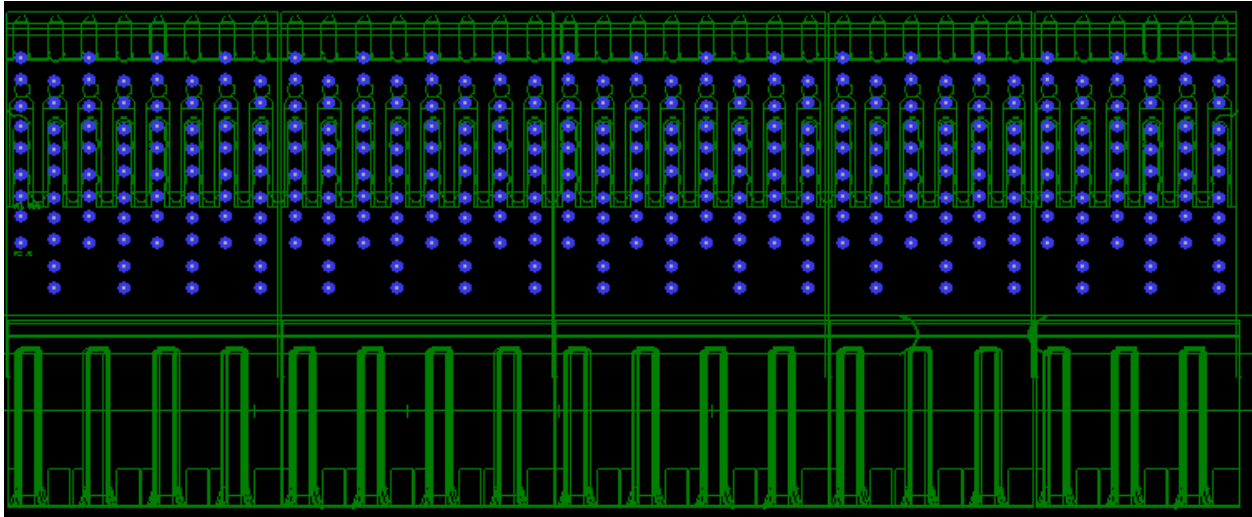
Figure 106: SCC SAS Connector

Table 31. SCC SAS Connector (M2) pinout

M2.1

	1	2	3	4	5	6	Decoder	
	PHY_SCC_TO_DPB_12_DN		PHY_SCC_TO_DPB_14_DN		PHY_SCC_TO_DPB_16_DN		F	
	PHY_SCC_TO_DPB_12_DP	PHY_SCC_TO_DPB_13_DN	PHY_SCC_TO_DPB_14_DP	PHY_SCC_TO_DPB_15_DN	PHY_SCC_TO_DPB_16_DP	PHY_SCC_TO_DPB_17_DN	E	F
		PHY_SCC_TO_DPB_13_DP		PHY_SCC_TO_DPB_15_DP		PHY_SCC_TO_DPB_17_DP		E
	BMC_LOC_HEARTBEAT		SCC_RMT_HEARTBEAT		SCC_TYPE_1		D	
	SCC_STBY_PGOOD	SCC_STBY_PWR_EN	SCC_LOC_HEARTBEAT	SLOT_ID_1	SCC_TYPE_0	SCC_TYPE_3	C	D
		P3V3_DPB		SLOT_ID_0		SCC_TYPE_2		C
	PHY_DPB_TO_SCC_12_DP		PHY_DPB_TO_SCC_14_DP		PHY_DPB_TO_SCC_16_DP		B	
	PHY_DPB_TO_SCC_12_DN	PHY_DPB_TO_SCC_13_DP	PHY_DPB_TO_SCC_14_DN	PHY_DPB_TO_SCC_15_DP	PHY_DPB_TO_SCC_16_DN	PHY_DPB_TO_SCC_17_DP	A	B
		PHY_DPB_TO_SCC_13_DN		PHY_DPB_TO_SCC_15_DN		PHY_DPB_TO_SCC_17_DN		A

M2.2

7	8	9	10	11	12	Decoder	
PHY_SCC_TO_DPB_18_DN		PHY_SCC_TO_DPB_20_DN		PHY_SCC_TO_DPB_22_DN		F	
PHY_SCC_TO_DPB_18_DP	PHY_SCC_TO_DPB_19_DN	PHY_SCC_TO_DPB_20_DP	PHY_SCC_TO_DPB_21_DN	PHY_SCC_TO_DPB_22_DP	PHY_SCC_TO_DPB_23_DN	E	F
	PHY_SCC_TO_DPB_19_DP		PHY_SCC_TO_DPB_21_DP		PHY_SCC_TO_DPB_23_DP		E
UART_SDB_RX		SCC_FULL_PWR_EN		SCC_LOC_INS_N		D	
UART_SDB_TX	PWM_OUT_ZONE_D	SYS_PWR_LED_N	SCC_RESET_N	DRIVE_INSERT_ALERT_N	I2C_CLIP_SDA7	C	D
	PWM_OUT_ZONE_C		ENCL_FAULT_LED		I2C_CLIP_SCL7		C
PHY_DPB_TO_SCC_18_DP		PHY_DPB_TO_SCC_20_DP		PHY_DPB_TO_SCC_22_DP		B	
PHY_DPB_TO_SCC_18_DN	PHY_DPB_TO_SCC_19_DP	PHY_DPB_TO_SCC_20_DN	PHY_DPB_TO_SCC_21_DP	PHY_DPB_TO_SCC_22_DN	PHY_DPB_TO_SCC_23_DP	A	B
	PHY_DPB_TO_SCC_19_DN		PHY_DPB_TO_SCC_21_DN		PHY_DPB_TO_SCC_23_DN		A

M2.3

13	14	15	16	17	18	Decoder	
PHY_SCC_TO_DPB_24_DN		PHY_SCC_TO_DPB_26_DN		PHY_SCC_TO_DPB_32_DN		F	
PHY_SCC_TO_DPB_24_DP	PHY_SCC_TO_DPB_25_DN	PHY_SCC_TO_DPB_26_DP	PHY_SCC_TO_DPB_27_DN	PHY_SCC_TO_DPB_32_DP	PHY_SCC_TO_DPB_33_DN	E	F
	PHY_SCC_TO_DPB_25_DP		PHY_SCC_TO_DPB_27_DP		PHY_SCC_TO_DPB_33_DP		E
UART_EXP_RX		I2C_DRIVE_PWR_SDA4		I2C_DRIVE_FLT_LED_SDA6		D	
UART_EXP_TX	I2C_DPB_SDA3	I2C_DRIVE_PWR_SCL4	I2C_DRIVE_INS_SDA5	I2C_DRIVE_FLT_LED_SCL6	DRIVE_1_ACT	C	D
	I2C_DPB_SCL3		I2C_DRIVE_INS_SCL5		DRIVE_0_ACT		C
PHY_DPB_TO_SCC_24_DP		PHY_DPB_TO_SCC_26_DP		PHY_DPB_TO_SCC_32_DP		B	
PHY_DPB_TO_SCC_24_DN	PHY_DPB_TO_SCC_25_DP	PHY_DPB_TO_SCC_26_DN	PHY_DPB_TO_SCC_27_DP	PHY_DPB_TO_SCC_32_DN	PHY_DPB_TO_SCC_33_DP	A	B
	PHY_DPB_TO_SCC_25_DN		PHY_DPB_TO_SCC_27_DN		PHY_DPB_TO_SCC_33_DN		A

M2.4

19	20	21	22	23	24	Decoder	
PHY_SCC_TO_DPB_34_DN		PHY_SCC_TO_DPB_36_DN		PHY_SCC_TO_DPB_38_DN		F	
PHY_SCC_TO_DPB_34_DP	PHY_SCC_TO_DPB_35_DN	PHY_SCC_TO_DPB_36_DP	PHY_SCC_TO_DPB_37_DN	PHY_SCC_TO_DPB_38_DP	PHY_SCC_TO_DPB_39_DN	E	F
	PHY_SCC_TO_DPB_35_DP		PHY_SCC_TO_DPB_37_DP		PHY_SCC_TO_DPB_39_DP		E
DRIVE_3_ACT		DRIVE_7_ACT		DRIVE_15_ACT		D	
DRIVE_2_ACT	DRIVE_5_ACT	DRIVE_6_ACT	DRIVE_13_ACT	DRIVE_14_ACT	DRIVE_17_ACT	C	D
	DRIVE_4_ACT		DRIVE_12_ACT		DRIVE_16_ACT		C
PHY_DPB_TO_SCC_34_DP		PHY_DPB_TO_SCC_36_DP		PHY_DPB_TO_SCC_38_DP		B	
PHY_DPB_TO_SCC_34_DN	PHY_DPB_TO_SCC_35_DP	PHY_DPB_TO_SCC_36_DN	PHY_DPB_TO_SCC_37_DP	PHY_DPB_TO_SCC_38_DN	PHY_DPB_TO_SCC_39_DP	A	B
	PHY_DPB_TO_SCC_35_DN		PHY_DPB_TO_SCC_37_DN		PHY_DPB_TO_SCC_39_DN		A

M2.5

25	26	27	28	29	30	Decoder	
PHY_SCC_TO_DPB_28_DN		PHY_SCC_TO_DPB_30_DN		PHY_SCC_TO_DPB_0_DN		F	
PHY_SCC_TO_DPB_28_DP	PHY_SCC_TO_DPB_29_DN	PHY_SCC_TO_DPB_30_DP	PHY_SCC_TO_DPB_31_DN	PHY_SCC_TO_DPB_0_DP	PHY_SCC_TO_DPB_1_DN	E	F
	PHY_SCC_TO_DPB_29_DP		PHY_SCC_TO_DPB_31_DP		PHY_SCC_TO_DPB_1_DP		E
DRIVE_19_ACT		DRIVE_23_ACT		DRIVE_27_ACT		D	
DRIVE_18_ACT	DRIVE_21_ACT	DRIVE_22_ACT	DRIVE_25_ACT	DRIVE_26_ACT	DRIVE_29_ACT	C	D
	DRIVE_20_ACT		DRIVE_24_ACT		DRIVE_28_ACT		C
PHY_DPB_TO_SCC_28_DP		PHY_DPB_TO_SCC_30_DP		PHY_DPB_TO_SCC_0_DP		B	
PHY_DPB_TO_SCC_28_DN	PHY_DPB_TO_SCC_29_DP	PHY_DPB_TO_SCC_30_DN	PHY_DPB_TO_SCC_31_DP	PHY_DPB_TO_SCC_0_DN	PHY_DPB_TO_SCC_1_DP	A	B
	PHY_DPB_TO_SCC_29_DN		PHY_DPB_TO_SCC_31_DN		PHY_DPB_TO_SCC_1_DN		A

M2.6

31	32	33	34	35	36	Decoder	
PHY_SCC_TO_DPB_2_DN		PHY_SCC_TO_DPB_4_DN		PHY_SCC_TO_DPB_6_DN		F	
PHY_SCC_TO_DPB_2_DP	PHY_SCC_TO_DPB_3_DN	PHY_SCC_TO_DPB_4_DP	PHY_SCC_TO_DPB_5_DN	PHY_SCC_TO_DPB_6_DP	PHY_SCC_TO_DPB_7_DN	E	F
	PHY_SCC_TO_DPB_3_DP		PHY_SCC_TO_DPB_5_DP		PHY_SCC_TO_DPB_7_DP		E
DRIVE_31_ACT		DRIVE_35_ACT		DRIVE_39_ACT		D	
DRIVE_30_ACT	DRIVE_33_ACT	DRIVE_34_ACT	DRIVE_37_ACT	DRIVE_38_ACT	SCC_FULL_PGOOD_BUF	C	D
	DRIVE_32_ACT		DRIVE_36_ACT		SCC_HSC_N		C
PHY_DPB_TO_SCC_2_DP		PHY_DPB_TO_SCC_4_DP		PHY_DPB_TO_SCC_6_DP		B	
PHY_DPB_TO_SCC_2_DN	PHY_DPB_TO_SCC_3_DP	PHY_DPB_TO_SCC_4_DN	PHY_DPB_TO_SCC_5_DP	PHY_DPB_TO_SCC_6_DN	PHY_DPB_TO_SCC_7_DP	A	B
	PHY_DPB_TO_SCC_3_DN		PHY_DPB_TO_SCC_5_DN		PHY_DPB_TO_SCC_7_DN		A

Note: Pinout view is looking into the top side of the SCC PCBA, going left to right, with the power, SAS, PCIe connectors on the lower corner.

23.7 Compute Module edge connector

The Mono Lake 1S server leverages an x16 edge connector pin assignments as defined in OCP microserver specification with a few exceptions, such as newly defined FAST_THROTTLE_N and 10GBase-KR signals. This mandatory primary x16 edge connector is referred to as Connector A. The secondary x16 edge connector is referred to as Connector B. [Placeholder]

Table 32. Mono Lake 1S Server Primary X16 OCP Edge Connector A Pinout

Pin Name	B Side	A Side	Pin Name	Pin Name	B Side	A Side	Pin Name
P12V	1	1	PRSNT_A#	GND	42	42	NIC_SMBUS_ALERT#
P12V	2	2	P12V	NIC_SMBUS_SCL	43	43	GND
P12V	3	3	P12V	NIC_SMBUS_SDA	44	44	GND
GND	4	4	GND	GND	45	45	KR0_RX_P
I2C_SCL	5	5	SVR_ID0/GPIO0	GND	46	46	KR0_RX_N
I2C_DATA	6	6	SVR_ID1/GPIO1	KR0_TX_P	47	47	GND
GND	7	7	COM_TX	KR0_TX_N	48	48	GND

Pin Name	B Side	A Side	Pin Name		Pin Name	B Side	A Side	Pin Name
PWR_BTN#	8	8	COM_RX		GND	49	49	PCIE1_RX0_P
USB_P	9	9	SVR_ID2/GPIO2		GND	50	50	PCIE1_RX0_N
USB_N	10	10	SVR_ID3/GPIO3		PCIE1_TX0_P	51	51	GND
SYS_RESET#	11	11	PCIE0_RESET#		PCIE1_TX0_N	52	52	GND
					GND	53	53	PCIE1_RX1_P
I2C_ALERT#	12	12	GND		GND	54	54	PCIE1_RX1_N
GND	13	13	PCIE0_REFCLK_P		PCIE1_TX1_P	55	55	GND
GND	14	14	PCIE0_REFCLK_N		PCIE1_TX1_N	56	56	GND
PCIE0_TX0_P	15	15	GND		GND	57	57	PCIE1_RX2_P
PCIE0_TX0_N	16	16	GND		GND	58	58	PCIE1_RX2_N
GND	17	17	PCIE0_RX0_P		PCIE1_TX2_P	59	59	GND
GND	18	18	PCIE0_RX0_N		PCIE1_TX2_N	60	60	GND
PCIE0_TX1_P	19	19	GND		GND	61	61	PCIE1_RX3_P
PCIE0_TX1_N	20	20	GND		GND	62	62	PCIE1_RX3_N
GND	21	21	PCIE0_RX1_P		PCIE1_TX3_P	63	63	GND
GND	22	22	PCIE0_RX1_N		PCIE1_TX3_N	64	64	GND
PCIE0_TX2_P	23	23	GND		GND	65	65	PCIE2_RX0_P
PCIE0_TX2_N	24	24	GND		GND	66	66	PCIE2_RX0_N
GND	25	25	PCIE0_RX2_P		PCIE2_TX0_P	67	67	GND
GND	26	26	PCIE0_RX2_N		PCIE2_TX0_N	68	68	GND
PCIE0_TX3_P	27	27	GND		GND	69	69	PCIE2_RX1_P
PCIE0_TX3_N	28	28	GND		GND	70	70	PCIE2_RX1_N
GND	29	29	PCIE0_RX3_P		PCIE2_TX1_P	71	71	GND
GND	30	30	PCIE0_RX3_N		PCIE2_TX1_N	72	72	GND
SATA0_TX_P	31	31	GND		GND	73	73	PCIE2_RX2_P
SATA0_TX_N	32	32	GND		GND	74	74	PCIE2_RX2_N
GND	33	33	SATA0_RX_P		PCIE2_TX2_P	75	75	GND
GND	34	34	SATA0_RX_N		PCIE2_TX2_N	76	76	GND
PCIE1_REFCLK_P	35	35	GND		GND	77	77	PCIE2_RX3_P
PCIE1_REFCLK_N	36	36	GND		GND	78	78	PCIE2_RX3_N
GND	37	37	PCIE2_REFCLK_P		PCIE2_TX3_P	79	79	GND
GND	38	38	PCIE2_REFCLK_N		PCIE2_TX3_N	80	80	GND
PCIE1_RESET#	39	39	GND		GND	81	81	P12V
PCIE2_RESET#	40	40	GND		GND	82	82	P12V
GND	41	41	FAST_THROTTLE_N					

Table 33. Mono Lake 1S Server Primary x16 OCP Edge Connector B Pinout

Pin Name	B Side	A Side	Pin Name		Pin Name	B Side	A Side	Pin Name
P12V	1	1	PRSNT_B#		GND	42	42	PCIE3_RX2_N
P12V	2	2	P12V		PCIE3_TX2_P	43	43	GND
P12V	3	3	P12V		PCIE3_TX2_N	44	44	GND
GND	4	4	GND		GND	45	45	PCIE3_RX3_P
NCSI_TXEN	5	5	NCSI_RCLK		GND	46	46	PCIE3_RX3_N
NCSI_TXD0	6	6	NCSI_RXD0		PCIE3_TX3_P	47	47	GND
NCSI_TXD1	7	7	NCSI_RXD1		PCIE3_TX3_N	48	48	GND
NCSI_CRSDV	8	8	GND		GND	49	49	PCIE4_RX0_P
NCSI_RXER	9	9	PCIE4_REFCLK_P		GND	50	50	PCIE4_RX0_N
GND	10	10	PCIE4_REFCLK_N		PCIE4_TX0_P	51	51	GND
PCIE3_RESET#	11	11	GND		PCIE4_TX0_N	52	52	GND
					GND	53	53	PCIE4_RX1_P
PCIE4_RESET#	12	12	GND		GND	54	54	PCIE4_RX1_N
PCIE5_RESET#	13	13	PCIE5_REFCLK_P		PCIE4_TX1_P	55	55	GND

Signal	Pin	Pin	Signal		Signal	Pin	Pin	Signal
GND	14	14	PCIE5_REFCLK_N		PCIE4_TX1_N	56	56	GND
KR4_TX0_P	15	15	GND		GND	57	57	PCIE4_RX2_P
KR4_TX0_N	16	16	GND		GND	58	58	PCIE4_RX2_N
GND	17	17	KR1_RX0_P		PCIE4_TX2_P	59	59	GND
GND	18	18	KR1_RX0_N		PCIE4_TX2_N	60	60	GND
KR1_TX1_P	19	19	GND		GND	61	61	PCIE4_RX3_P
KR1_TX1_N	20	20	GND		GND	62	62	PCIE4_RX3_N
GND	21	21	N/A		PCIE4_TX3_P	63	63	GND
GND	22	22	N/A		PCIE4_TX3_N	64	64	GND
N/A	23	23	GND		GND	65	65	PCIE5_RX0_P
N/A	24	24	GND		GND	66	66	PCIE5_RX0_N
GND	25	25	N/A		PCIE5_TX0_P	67	67	GND
GND	26	26	N/A		PCIE5_TX0_N	68	68	GND
N/A	27	27	GND		GND	69	69	PCIE5_RX1_P
N/A	28	28	GND		GND	70	70	PCIE5_RX1_N
GND	29	29	N/A		PCIE5_TX1_P	71	71	GND
GND	30	30	N/A		PCIE5_TX1_N	72	72	GND
PCIE3_REFCLK_P	31	31	GND		GND	73	73	PCIE5_RX2_P
PCIE3_REFCLK_N	32	32	GND		GND	74	74	PCIE5_RX2_N
GND	33	33	PCIE3_RX0_P		PCIE5_TX2_P	75	75	GND
GND	34	34	PCIE3_RX0_N		PCIE5_TX2_N	76	76	GND
PCIE3_TX0_P	35	35	GND		GND	77	77	PCIE5_RX3_P
PCIE3_TX0_N	36	36	GND		GND	78	78	PCIE5_RX3_N
GND	37	37	PCIE3_RX1_P		PCIE5_TX3_P	79	79	GND
GND	38	38	PCIE3_RX1_N		PCIE5_TX3_N	80	80	GND
PCIE3_TX1_P	39	39	GND		GND	81	81	P12V
PCIE3_TX1_N	40	40	GND		POWER_FAIL_N	82	82	P12V
GND	41	41	PCIE3_RX2_P					

23.8 I/O Module coplanar connector

Figure 107: IOM coplanar connector

Table 34: IOM coplanar connector pinout

16	15	14	13	12	11	10	9	GUIDE PIN	8	7	6	5	4	3	2	1
A		A		A		A			A		A		A		A	
B	A	B	A	B	A	B	A		B	A	B	A	B	A	B	A
	B		B		B		B			B		B		B		B
C		C		C		C			C		C		C		C	
D	C	D	C	D	C	D	C		D	C	D	C	D	C	D	C
	D		D		D		D			D		D		D		D
E		E		E		E			E		E		E		E	
F	E	F	E	F	E	F	E		F	E	F	E	F	E	F	E
	F		F		F		F			F		F		F		F
G		G		G		G			G		G		G		G	
H	G	H	G	H	G	H	G		H	G	H	G	H	G	H	G
	H		H		H		H			H		H		H		H

16	15	14	13	12	11	10	9	Decoder	
COMP_SPARE_1		I2C_DPB_SDA		USB_COMP_DN		SLOTID_1		A	
COMP_SPARE_0	EXP_SPARE_1	I2C_DPB_SCL	COMP_TO_BMC_RESET	USB_COMP_DP	BMC_TO_EXP_RESET_N	SLOTID_0	PCIE_COMP_TO_IOM_CLK_4_DN	B	A
	EXP_SPARE_0		SYS_RESET_N		DPB_MISC_ALERT		PCIE_COMP_TO_IOM_CLK_4_DP		B
PWM_OUT_ZONE_C				COMP_PWR_EN		I2C_BMC_COMP_SDA		C	
PWM_OUT_ZONE_D		COMP_PWR_BTN_N	COMP_POWER_FAIL_N	SCC_RMT_TYPE_0	UART_COMP_RX	I2C_BMC_COMP_SCL	I2C_BMC_COMP_ALERT_N	D	C
	ENCL_FAULT_LED		COMP_FAST_THROTTLE_N		UART_COMP_TX		PCIE_COMP_TO_IOM_RST_4		D
PCIE_IOM_TO_COMP_23_DN	PCIE_IOM_TO_COMP_21_DN			PCIE_IOM_TO_COMP_19_DN		PCIE_IOM_TO_COMP_17_DN		E	
PCIE_IOM_TO_COMP_23_DP	PCIE_IOM_TO_COMP_22_DN	PCIE_IOM_TO_COMP_21_DP	PCIE_IOM_TO_COMP_20_DN	PCIE_IOM_TO_COMP_19_DP	PCIE_IOM_TO_COMP_18_DN	PCIE_IOM_TO_COMP_17_DP	PCIE_IOM_TO_COMP_16_DN	F	E
	PCIE_IOM_TO_COMP_22_DP		PCIE_IOM_TO_COMP_20_DP		PCIE_IOM_TO_COMP_18_DP		PCIE_IOM_TO_COMP_16_DP		F
PCIE_COMP_TO_IOM_23_DN	PCIE_COMP_TO_IOM_21_DN			PCIE_COMP_TO_IOM_19_DN		PCIE_COMP_TO_IOM_17_DN		G	
PCIE_COMP_TO_IOM_23_DP	PCIE_COMP_TO_IOM_22_DN	PCIE_COMP_TO_IOM_21_DP	PCIE_COMP_TO_IOM_20_DN	PCIE_COMP_TO_IOM_19_DP	PCIE_COMP_TO_IOM_18_DN	PCIE_COMP_TO_IOM_17_DP	PCIE_COMP_TO_IOM_16_DN	H	G
	PCIE_COMP_TO_IOM_22_DP		PCIE_COMP_TO_IOM_20_DP		PCIE_COMP_TO_IOM_18_DP		PCIE_COMP_TO_IOM_16_DP		H

8	7	6	5	4	3	2	1	Decoder	
P12V_IOM		I2C_EXP_LOC_SDA		SCC_RMT_FULL_PWR_EN		I2C_DPB_MISC_SDA		A	
P12V_IOM	P12V_IOM	I2C_EXP_LOC_SCL	PCIE_COMP_TO_IOM_CLK_3_DN	SCC_LOC_FULL_PWR_EN	BMC_LOC_HEARTBEAT	I2C_DPB_MISC_SCL	PCIE_COMP_TO_IOM_CLK_2_DN	B	A
	P12V_A_PGOOD		PCIE_COMP_TO_IOM_CLK_3_DP		BMC_RMT_HEARTBEAT		PCIE_COMP_TO_IOM_CLK_2_DP		B
P12V_IOM		I2C_EXP_RMT_SDA		SYS_PWR_LED		I2C_SCC_SDA		C	
P12V_IOM	UART_SDB_RX	I2C_EXP_RMT_SCL	IOM_LOC_INS_N	SCC_STBY_PWR_EN	SCC_RMT_HEARTBEAT	I2C_SCC_SCL	IOM_MATED_N	D	C
	UART_SDB_TX		PCIE_COMP_TO_IOM_RST_3		SCC_LOC_HEARTBEAT		PCIE_COMP_TO_IOM_RST_2		D
PCIE_IOM_TO_COMP_15_DN		PCIE_IOM_TO_COMP_13_DN		PCIE_IOM_TO_COMP_11_DN		PCIE_IOM_TO_COMP_9_DN		E	
PCIE_IOM_TO_COMP_15_DP	PCIE_IOM_TO_COMP_14_DN	PCIE_IOM_TO_COMP_13_DP	PCIE_IOM_TO_COMP_12_DN	PCIE_IOM_TO_COMP_11_DP	PCIE_IOM_TO_COMP_10_DN	PCIE_IOM_TO_COMP_9_DP	PCIE_IOM_TO_COMP_8_DN	F	E
	PCIE_IOM_TO_COMP_14_DP		PCIE_IOM_TO_COMP_12_DP		PCIE_IOM_TO_COMP_10_DP		PCIE_IOM_TO_COMP_8_DP		F
PCIE_COMP_TO_IOM_15_DN		PCIE_COMP_TO_IOM_13_DN		PCIE_COMP_TO_IOM_11_DN		PCIE_COMP_TO_IOM_9_DN		G	
PCIE_COMP_TO_IOM_15_DP	PCIE_COMP_TO_IOM_14_DN	PCIE_COMP_TO_IOM_13_DP	PCIE_COMP_TO_IOM_12_DN	PCIE_COMP_TO_IOM_11_DP	PCIE_COMP_TO_IOM_10_DN	PCIE_COMP_TO_IOM_9_DP	PCIE_COMP_TO_IOM_8_DN	H	G
	PCIE_COMP_TO_IOM_14_DP		PCIE_COMP_TO_IOM_12_DP		PCIE_COMP_TO_IOM_10_DP		PCIE_COMP_TO_IOM_8_DP		H

23.9 NIC mezzanine connector

Table 35: NIC Mezzanine connector pinout

Pin Name	Pin #		Pin Name
	○		
MEZZ_A_PRSNT_120_N	120	60	GND
GND	119	59	PCIE_IOM_TO_COMP_23_DN
GND	118	58	PCIE_IOM_TO_COMP_23_DP
PCIE_COMP_TO_IOM_23_DN	117	57	GND
PCIE_COMP_TO_IOM_23_DP	116	56	GND
GND	115	55	PCIE_IOM_TO_COMP_22_DN
GND	114	54	PCIE_IOM_TO_COMP_22_DP

PCIE_COMP_TO_IOM_22_DN	113	53	GND
PCIE_COMP_TO_IOM_22_DP	112	52	GND
GND	111	51	PCIE_IOM_TO_COMP_21_DN
GND	110	50	PCIE_IOM_TO_COMP_21_DP
PCIE_COMP_TO_IOM_21_DN	109	49	GND
PCIE_COMP_TO_IOM_21_DP	108	48	GND
GND	107	47	PCIE_IOM_TO_COMP_20_DN
GND	106	46	PCIE_IOM_TO_COMP_20_DP
PCIE_COMP_TO_IOM_20_DN	105	45	GND
PCIE_COMP_TO_IOM_20_DP	104	44	GND
GND	103	43	PCIE_IOM_TO_COMP_19_DN
GND	102	42	PCIE_IOM_TO_COMP_19_DP
PCIE_COMP_TO_IOM_19_DN	101	41	GND
PCIE_COMP_TO_IOM_19_DP	100	40	GND
GND	99	39	PCIE_IOM_TO_COMP_18_DN
GND	98	38	PCIE_IOM_TO_COMP_18_DP
PCIE_COMP_TO_IOM_18_DN	97	37	GND
PCIE_COMP_TO_IOM_18_DP	96	36	GND
GND	95	35	PCIE_IOM_TO_COMP_17_DN
GND	94	34	PCIE_IOM_TO_COMP_17_DP
PCIE_COMP_TO_IOM_17_DN	93	33	GND
PCIE_COMP_TO_IOM_17_DP	92	32	GND
GND	91	31	PCIE_IOM_TO_COMP_16_DN
GND	90	30	PCIE_IOM_TO_COMP_16_DP
PCIE_COMP_TO_IOM_16_DN	89	29	GND
PCIE_COMP_TO_IOM_16_DP	88	28	GND
GND	87	27	
GND	86	26	
PCIE_COMP_TO_IOM_CLK_4_DN	85	25	GND
PCIE_COMP_TO_IOM_CLK_4_DP	84	24	GND
GND	83	23	NCSI_RXD1_R
GND	82	22	NCSI_RXD0_R
NCSI_TXD1	81	21	GND
NCSI_TXD0	80	20	GND
GND	79	19	I2C_MEZZ_OOB_SDA
NCSI_RX_ER_R	78	18	I2C_MEZZ_OOB_SCL
PCIE_WAKE_N	77	17	PCIE_COMP_TO_IOM_RST_4_R
I2C_MEZZ_FRU_SENSOR_SDA	76	16	NCSI_TXEN_R
I2C_MEZZ_FRU_SENSOR_SCL	75	15	NCSI_RCLK
I2C_MEZZ_ALERT_R_N	74	14	NCSI_RCSDV_R
GND	73	13	P3V3
P3V3	72	12	P3V3
P3V3	71	11	P3V3

P3V3	70		10	P3V3
P3V3	69		9	GND
GND	68		8	GND
GND	67		7	P3V3_STBY
P3V3_STBY	66		6	GND
GND	65		5	GND
GND	64		4	P5V_STBY
P12V_STBY	63		3	P5V_STBY
P12V_STBY	62		2	P5V_STBY
P12V_STBY	61		1	MEZZA_PRSNT1_N
		○		

23.10 M.2 connector

Table 36: PCIe M.2 connector
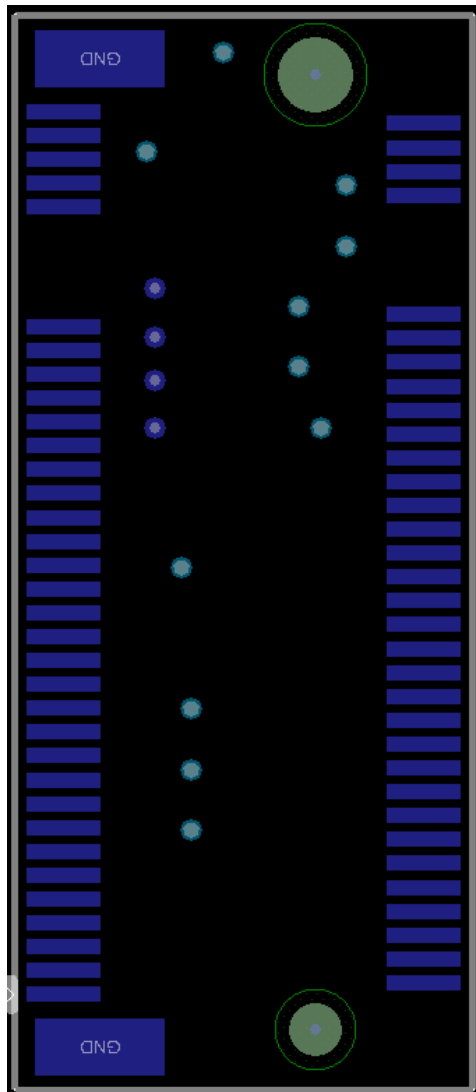
Pin Name	Pin #		Pin Name
GND	77	○	
	75	75	GND
P3V3_M2	73	73	GND
P3V3_M2	71	71	GND
P3V3_M2	69	69	
	67	67	
GND	57	58	TP_M2_2_MFG_CLK
PCIE_COMP_TO_IOM_CLK_3_DP	55	56	TP_M2_2_MFG_DAT
PCIE_COMP_TO_IOM_CLK_3_DN	53	54	
GND	51	52	M2_2_CLKREQ#
PCIE_COMP_TO_IOM_12_DP	49	50	PCIE_COMP_TO_IOM_RST_3
PCIE_COMP_TO_IOM_12_DN	47	48	
GND	45	46	
PCIE_IOM_TO_COMP_12_DP	43	44	M2_2_ALERT#
PCIE_IOM_TO_COMP_12_DN	41	42	I2C_M2_2_1V8_SDA
GND	39	40	I2C_M2_2_1V8_SCL
PCIE_COMP_TO_IOM_13_DP	37	38	
PCIE_COMP_TO_IOM_13_DN	35	36	
GND	33	34	
PCIE_IOM_TO_COMP_13_DP	31	32	
PCIE_IOM_TO_COMP_13_DN	29	30	
GND	27	28	
PCIE_COMP_TO_IOM_14_DP	25	26	
PCIE_COMP_TO_IOM_14_DN	23	24	
GND	21	22	
PCIE_IOM_TO_COMP_14_DP	19	20	
PCIE_IOM_TO_COMP_14_DN	17	18	P3V3_M2
GND	15	16	P3V3_M2
PCIE_COMP_TO_IOM_15_DP	13	14	P3V3_M2
PCIE_COMP_TO_IOM_15_DN	11	12	P3V3_M2
GND	9	10	M2_2_ACTIVE_N
PCIE_IOM_TO_COMP_15_DP	7	8	
PCIE_IOM_TO_COMP_15_DN	5	6	
GND	3	4	P3V3_M2
M2_2_PRESENT_N_R	1	2	P3V3_M2
GND	76	○	

23.11 DPB to DPB coplanar connector
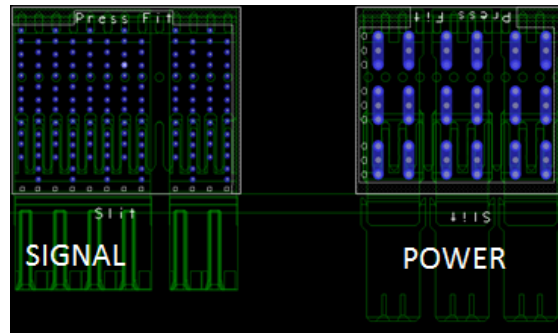
Figure 108: DPb to DPB coplanar connectors

Table 37: DPB to DPB signal connector pinout

1	2	3	4	5	6	7	8	Decoder	
PCIE_SCC_B_TO_COMP_B_0_DN		PCIE_SCC_B_TO_COMP_B_2_DN		PCIE_SCC_B_TO_COMP_B_4_DN		PCIE_SCC_B_TO_COMP_B_6_DN		H	
PCIE_SCC_B_TO_COMP_B_0_DP	PCIE_SCC_B_TO_COMP_B_1_DN	PCIE_SCC_B_TO_COMP_B_2_DP	PCIE_SCC_B_TO_COMP_B_3_DN	PCIE_SCC_B_TO_COMP_B_4_DP	PCIE_SCC_B_TO_COMP_B_5_DN	PCIE_SCC_B_TO_COMP_B_6_DP	PCIE_SCC_B_TO_COMP_B_7_DN	G	H
	PCIE_SCC_B_TO_COMP_B_1_DP		PCIE_SCC_B_TO_COMP_B_3_DP		PCIE_SCC_B_TO_COMP_B_5_DP		PCIE_SCC_B_TO_COMP_B_7_DP		G
PCIE_COMP_B_TO_SCC_B_CLK_0_DN		I2C_CLIP_A_SDA		I2C_BMC_B_EXP_B_SDA		UART_SDB_B_RX		F	
PCIE_COMP_B_TO_SCC_B_CLK_0_DP	I2C_DPB_A_SDA_BUF	I2C_CLIP_A_SCL	PCIE_COMP_B_TO_SCC_B_RST_0	I2C_BMC_B_EXP_B_SCL	SCC_B_RESET_N	UART_SDB_B_TX	PWM_SCC_A_ZONE_D	E	F
	I2C_DPB_A_SCL_BUF		COMP_B_EXP_B_SPARE_0				PWM_SCC_A_ZONE_C		E
PCIE_COMP_B_TO_SCC_B_0_DN		PCIE_COMP_B_TO_SCC_B_2_DN		PCIE_COMP_B_TO_SCC_B_4_DN		PCIE_COMP_B_TO_SCC_B_6_DN		D	
PCIE_COMP_B_TO_SCC_B_0_DP	I2C_SCC_B_SDA	PCIE_COMP_B_TO_SCC_B_2_DP	PWM_BMC_A_ZONE_D	PCIE_COMP_B_TO_SCC_B_4_DP	I2C_DRIVE_B_FLT_LED_SCL	PCIE_COMP_B_TO_SCC_B_6_DP	UART_IOC_B_RX	C	D
	I2C_SCC_B_SCL		PWM_BMC_A_ZONE_C		I2C_DRIVE_B_FLT_LED_SDA		UART_IOC_B_TX		C
PWM_BMC_B_ZONE_D		I2C_DPB_B_SDA		I2C_BMC_A_EXP_B_SDA		UART_EXP_B_RX		B	
PWM_BMC_B_ZONE_C	PCIE_COMP_B_TO_SCC_B_1_DN	I2C_DPB_B_SCL	PCIE_COMP_B_TO_SCC_B_3_DN	I2C_BMC_A_EXP_B_SCL	PCIE_COMP_B_TO_SCC_B_5_DN	UART_EXP_B_TX	PCIE_COMP_B_TO_SCC_B_7_DN	A	B
	PCIE_COMP_B_TO_SCC_B_1_DP		PCIE_COMP_B_TO_SCC_B_3_DP		PCIE_COMP_B_TO_SCC_B_5_DP		PCIE_COMP_B_TO_SCC_B_7_DP		A

9	10	11	12	Decoder	
GND		DRIVE_B_35_ACT		M	
SCC_B_TYPE_3	GND	DRIVE_B_34_ACT	P5V_B_2	L	N
SCC_B_FAULT_LED	SCC_B_TYPE_2	DRIVE_B_33_ACT	P3V3_STBY_B	K	M
DPB_PWR_BTN_BUF_B	SCC_B_TYPE_1	DRIVE_B_32_ACT	P3V3_STBY_A	J	L
SCC_B_STBY_PWR_EN	SCC_B_TYPE_0	DRIVE_B_31_ACT	FDPB_FAN_LED3	H	K
P12V_B_PGOOD	SCC_B_INS_N	DRIVE_B_30_ACT	FDPB_FAN_LED2	G	J
P12V_IN_PGOOD	SCC_A_INS_N	DRIVE_B_29_ACT	FDPB_FAN_LED1	F	H
DRAWER_CLOSED_N	IOM_B_INS_N	DRIVE_B_28_ACT	FDPB_FAN_LED0	E	G
SCC_B_FULL_PGOOD	IOM_A_INS_N	DRIVE_B_27_ACT	SCC_B_HEARTBEAT	D	F
SCC_B_FULL_PWR_EN	FAN_3_INS_N	DRIVE_B_26_ACT	SCC_A_HEARTBEAT	C	E
SCC_A_FULL_PWR_EN	FAN_2_INS_N	DRIVE_B_25_ACT	BMC_B_HEARTBEAT	B	D
SCC_B_STBY_PGOOD	FAN_1_INS_N	DRIVE_B_24_ACT	BMC_A_HEARTBEAT	A	C
	FAN_0_INS_N		BMC_B_EXP_B_SPARE_1		B
	SCC_B_PWR_LED		BMC_B_EXP_B_SPARE_0		A

Table 38: DPB to DPB power connector pinout

6	5	4	3	2	1	Decoder
GND	GND	GND	GND	GND	GND	J
GND	GND	GND	GND	GND	GND	H
GND	GND	GND	GND	GND	GND	G
GND	GND	P12V_IN	P12V_IN	P12V_IN	P12V_IN	F
GND	GND	P12V_IN	P12V_IN	P12V_IN	P12V_IN	E
GND	GND	P12V_IN	P12V_IN	P12V_IN	P12V_IN	D
P12V_B	P12V_B	P12V_IN	P12V_IN	P12V_IN	P12V_IN	C
P12V_B	P12V_B	P12V_IN	P12V_IN	P12V_IN	P12V_IN	B
P12V_B	P12V_B	P12V_IN	P12V_IN	P12V_IN	P12V_IN	A

23.12 Debug header (USB 3.0 remapped) connector

Pin Name	Pin#		Pin Name
USB_CONN_A_GND	10	12	USB_CONN_A_GND
		9	UART_DEBUG_A_RX
P5V_VBUS_A	1		
		8	UART_DEBUG_A_TX
DEBUG_USB_A_DN	2		
		7	DEBUG_CARD_A_PRSNT
DEBUG_USB_A_DP	3		
		6	I2C_DEBUG_A_SDA
GND	4		
		5	I2C_DEBUG_A_SCL
USB_CONN_A_GND	11	13	USB_CONN_A_GND
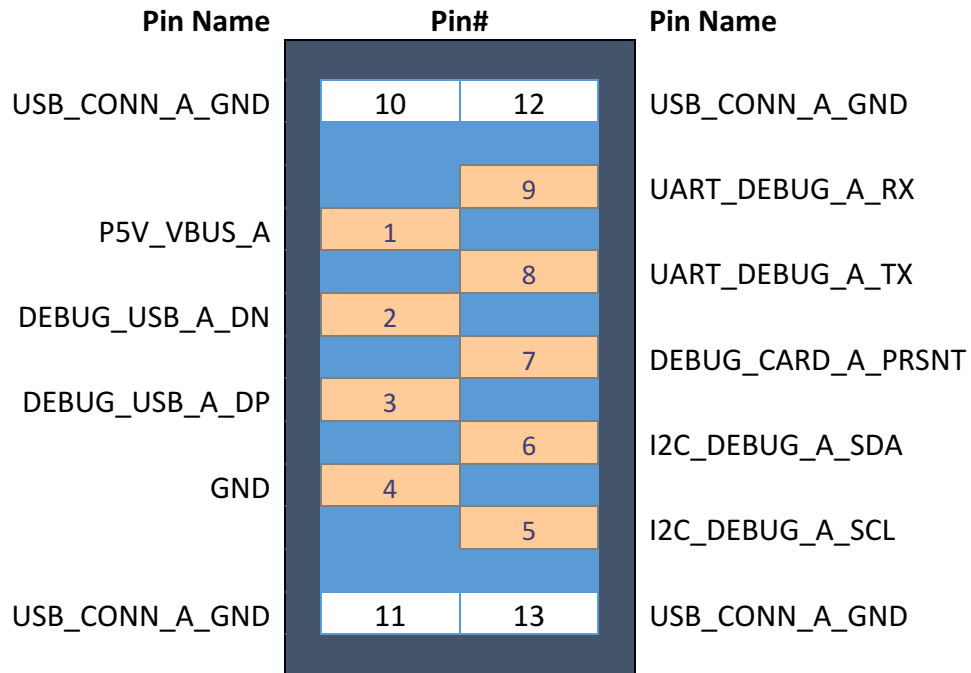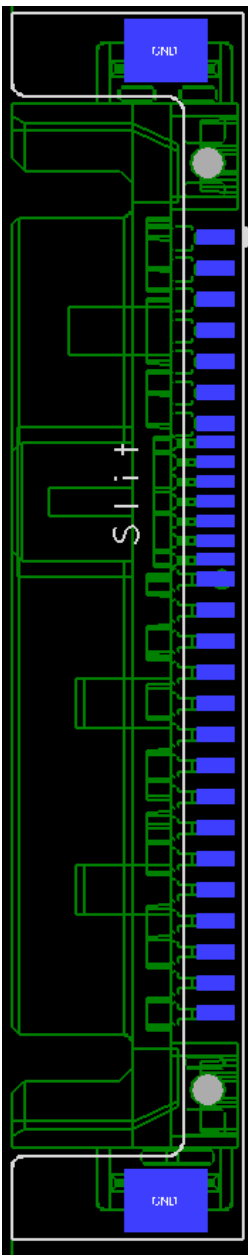
Figure 109. Debug header connector pin definitions

23.13 Front panel connector

Table 39: Front Panel board connector pinout

Pin	Signal
GND	
S1	UART_EXP_A_TX
S2	UART_EXP_A_RX
S3	GND
S4	UART_IOC_A_TX
S5	UART_IOC_A_RX
S6	GND
S7	DPB_PWR_BTN_A
S8	I2C_DPB_A_SCL_BUF
S9	I2C_DPB_A_SDA_BUF
S10	RST_BTN_A_N
S11	P3V3_STBY_A
S12	SYS_PWR_LED_A
S13	ENCL_FAULT_LED_A
S14	
P1	P5V_USB_A
P2	P5V_USB_B
P3	ENCL_FAULT_LED_B
P4	SYS_PWR_LED_B
P5	P3V3_STBY_B
P6	RST_BTN_B_N
P7	GND
P8	I2C_DPB_B_SCL
P9	I2C_DPB_B_SDA
P10	DPB_PWR_BTN_B
P11	UART_IOC_B_TX
P12	UART_IOC_B_RX
P13	GND
P14	UART_EXP_B_TX
P15	UART_EXP_B_RX
GND	

23.14 Fan Connector

Table 40. Fan Connector pinout
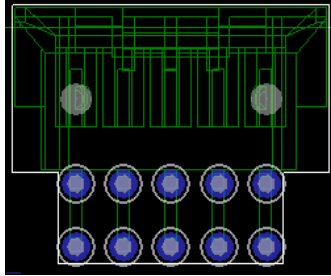
Pin Name	FAN_0_TACH0	FAN_0_PWM	FAN_0_INS_N	P12V_FAN0	GND
Pin #	1	3	5	7	9
	2	4	6	8	10
Pin Name	FAN_0_TACH1	FAN_0_PWM		P12V_FAN0	GND

23.15 Front Drive Plane Board SAS Connector (to SCC)
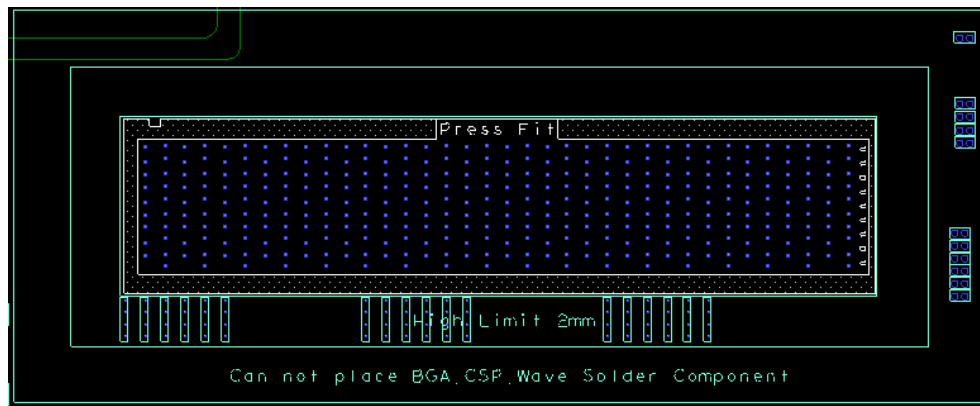
Figure 110: Front DPB SAS Connector to SCC

Table 41. SCC FDPB SAS Connector (M2) pinout

M2.1							
1	**2**	**3**	**4**	**5**	**6**	**Decoder**	
PHY_DRV_A_TO_SCC_A_0_DN		PHY_DRV_A_TO_SCC_A_2_DN		PHY_DRV_A_TO_SCC_A_4_DN		A	
PHY_DRV_A_TO_SCC_A_0_DP	PHY_DRV_A_TO_SCC_A_1_DN	PHY_DRV_A_TO_SCC_A_2_DP	PHY_DRV_A_TO_SCC_A_3_DN	PHY_DRV_A_TO_SCC_A_4_DP	PHY_DRV_A_TO_SCC_A_5_DN	B	A
	PHY_DRV_A_TO_SCC_A_1_DP		PHY_DRV_A_TO_SCC_A_3_DP		PHY_DRV_A_TO_SCC_A_5_DP		B
SCC_A_STBY_PGOOD		SCC_A_HEARTBEAT		SCC_A_TYPE_0		C	
BMC_A_HEARTBEAT	P3V3_STBY_A	SCC_B_HEARTBEAT	SCC_A_SLOT_ID_0	SCC_A_TYPE_1	SCC_A_TYPE_2	D	C
	SCC_A_STBY_PWR_EN		SCC_A_SLOT_ID_1		SCC_A_TYPE_3		D
PHY_SCC_A_TO_DRV_A_0_DP		PHY_SCC_A_TO_DRV_A_2_DP		PHY_SCC_A_TO_DRV_A_4_DP		E	
PHY_SCC_A_TO_DRV_A_0_DN	PHY_SCC_A_TO_DRV_A_1_DP	PHY_SCC_A_TO_DRV_A_2_DN	PHY_SCC_A_TO_DRV_A_3_DP	PHY_SCC_A_TO_DRV_A_4_DN	PHY_SCC_A_TO_DRV_A_5_DP	F	E
	PHY_SCC_A_TO_DRV_A_1_DN		PHY_SCC_A_TO_DRV_A_3_DN		PHY_SCC_A_TO_DRV_A_5_DN		F

M2.2

7	8	9	10	11	12	Decoder	
PHY_DRV_A_TO_SCC_A_11_DN		PHY_DRV_A_TO_SCC_A_9_DN		PHY_DRV_A_TO_SCC_A_7_DN		A	
PHY_DRV_A_TO_SCC_A_11_DP	PHY_DRV_A_TO_SCC_A_10_DN	PHY_DRV_A_TO_SCC_A_9_DP	PHY_DRV_A_TO_SCC_A_8_DN	PHY_DRV_A_TO_SCC_A_7_DP	PHY_DRV_A_TO_SCC_A_6_DN	B	A
	PHY_DRV_A_TO_SCC_A_10_DP		PHY_DRV_A_TO_SCC_A_8_DP		PHY_DRV_A_TO_SCC_A_6_DP		B
UART_SDB_A_TX		SCC_A_PWR_LED		DRIVE_INSERT_ALERT_A_N		C	
UART_SDB_A_RX	PWM_SCC_A_ZONE_C	SCC_A_FULL_PWR_EN	SCC_A_FAULT_LED	SCC_A_INS_N	I2C_CLIP_A_SCL	D	C
	PWM_SCC_A_ZONE_D		SCC_A_RESET_N		I2C_CLIP_A_SDA		D
PHY_SCC_A_TO_DRV_A_11_DP		PHY_SCC_A_TO_DRV_A_9_DP		PHY_SCC_A_TO_DRV_A_7_DP		E	
PHY_SCC_A_TO_DRV_A_11_DN	PHY_SCC_A_TO_DRV_A_10_DP	PHY_SCC_A_TO_DRV_A_9_DN	PHY_SCC_A_TO_DRV_A_8_DP	PHY_SCC_A_TO_DRV_A_7_DN	PHY_SCC_A_TO_DRV_A_6_DP	F	E
	PHY_SCC_A_TO_DRV_A_10_DN		PHY_SCC_A_TO_DRV_A_8_DN		PHY_SCC_A_TO_DRV_A_6_DN		F

M2.3

13	14	15	16	17	18	Decoder	
PHY_DRV_A_TO_SCC_A_12_DN		PHY_DRV_A_TO_SCC_A_14_DN		PHY_DRV_A_TO_SCC_A_16_DN		A	
PHY_DRV_A_TO_SCC_A_12_DP	PHY_DRV_A_TO_SCC_A_13_DN	PHY_DRV_A_TO_SCC_A_14_DP	PHY_DRV_A_TO_SCC_A_15_DN	PHY_DRV_A_TO_SCC_A_16_DP	PHY_DRV_A_TO_SCC_A_17_DN	B	A
	PHY_DRV_A_TO_SCC_A_13_DP		PHY_DRV_A_TO_SCC_A_15_DP		PHY_DRV_A_TO_SCC_A_17_DP		B
UART_EXP_A_TX		I2C_DRIVE_A_PWR_SCL		I2C_DRIVE_A_FLT_LED_SCL		C	
UART_EXP_A_RX	I2C_DPB_A_SCL_BUF	I2C_DRIVE_A_PWR_SDA	I2C_DRIVE_A_INS_SCL	I2C_DRIVE_A_FLT_LED_SDA	DRIVE_A_0_ACT	D	C
	I2C_DPB_A_SDA_BUF		I2C_DRIVE_A_INS_SDA		DRIVE_A_1_ACT		D
PHY_SCC_A_TO_DRV_A_12_DP		PHY_SCC_A_TO_DRV_A_14_DP		PHY_SCC_A_TO_DRV_A_16_DP		E	
PHY_SCC_A_TO_DRV_A_12_DN	PHY_SCC_A_TO_DRV_A_13_DP	PHY_SCC_A_TO_DRV_A_14_DN	PHY_SCC_A_TO_DRV_A_15_DP	PHY_SCC_A_TO_DRV_A_16_DN	PHY_SCC_A_TO_DRV_A_17_DP	F	E
	PHY_SCC_A_TO_DRV_A_13_DN		PHY_SCC_A_TO_DRV_A_15_DN		PHY_SCC_A_TO_DRV_A_17_DN		F

M2.4

19	20	21	22	23	24	Decoder	
PHY_DRV_A_TO_SCC_A_23_DN		PHY_DRV_A_TO_SCC_A_21_DN		PHY_DRV_A_TO_SCC_A_19_DN		A	
PHY_DRV_A_TO_SCC_A_23_DP	PHY_DRV_A_TO_SCC_A_22_DN	PHY_DRV_A_TO_SCC_A_21_DP	PHY_DRV_A_TO_SCC_A_20_DN	PHY_DRV_A_TO_SCC_A_19_DP	PHY_DRV_A_TO_SCC_A_18_DN	B	A
	PHY_DRV_A_TO_SCC_A_22_DP		PHY_DRV_A_TO_SCC_A_20_DP		PHY_DRV_A_TO_SCC_A_18_DP		B
DRIVE_A_2_ACT		DRIVE_A_6_ACT		DRIVE_A_10_ACT		C	
DRIVE_A_3_ACT	DRIVE_A_4_ACT	DRIVE_A_7_ACT	DRIVE_A_8_ACT	DRIVE_A_11_ACT	DRIVE_A_12_ACT	D	C
	DRIVE_A_5_ACT		DRIVE_A_9_ACT		DRIVE_A_13_ACT		D
PHY_SCC_A_TO_DRV_A_23_DP		PHY_SCC_A_TO_DRV_A_21_DP		PHY_SCC_A_TO_DRV_A_19_DP		E	
PHY_SCC_A_TO_DRV_A_23_DN	PHY_SCC_A_TO_DRV_A_22_DP	PHY_SCC_A_TO_DRV_A_21_DN	PHY_SCC_A_TO_DRV_A_20_DP	PHY_SCC_A_TO_DRV_A_19_DN	PHY_SCC_A_TO_DRV_A_18_DP	F	E
	PHY_SCC_A_TO_DRV_A_22_DN		PHY_SCC_A_TO_DRV_A_20_DN		PHY_SCC_A_TO_DRV_A_18_DN		F

M2.5

25	26	27	28	29	30	Decoder	
PHY_DRV_A_TO_SCC_A_24_DN		PHY_DRV_A_TO_SCC_A_26_DN		PHY_DRV_A_TO_SCC_A_28_DN		A	
PHY_DRV_A_TO_SCC_A_24_DP	PHY_DRV_A_TO_SCC_A_25_DN	PHY_DRV_A_TO_SCC_A_26_DP	PHY_DRV_A_TO_SCC_A_27_DN	PHY_DRV_A_TO_SCC_A_28_DP	PHY_DRV_A_TO_SCC_A_29_DN	B	A
	PHY_DRV_A_TO_SCC_A_25_DP		PHY_DRV_A_TO_SCC_A_27_DP		PHY_DRV_A_TO_SCC_A_29_DP		B
DRIVE_A_14_ACT		DRIVE_A_18_ACT		DRIVE_A_22_ACT		C	
DRIVE_A_15_ACT	DRIVE_A_16_ACT	DRIVE_A_19_ACT	DRIVE_A_20_ACT	DRIVE_A_23_ACT	DRIVE_A_24_ACT	D	C
	DRIVE_A_17_ACT		DRIVE_A_21_ACT		DRIVE_A_25_ACT		D
PHY_SCC_A_TO_DRV_A_24_DP		PHY_SCC_A_TO_DRV_A_26_DP		PHY_SCC_A_TO_DRV_A_28_DP		E	
PHY_SCC_A_TO_DRV_A_24_DN	PHY_SCC_A_TO_DRV_A_25_DP	PHY_SCC_A_TO_DRV_A_26_DN	PHY_SCC_A_TO_DRV_A_27_DP	PHY_SCC_A_TO_DRV_A_28_DN	PHY_SCC_A_TO_DRV_A_29_DP	F	E
	PHY_SCC_A_TO_DRV_A_25_DN		PHY_SCC_A_TO_DRV_A_27_DN		PHY_SCC_A_TO_DRV_A_29_DN		F

M2.6

31	32	33	34	35	36	Decoder	
PHY_DRV_A_TO_SCC_A_35_DN		PHY_DRV_A_TO_SCC_A_33_DN		PHY_DRV_A_TO_SCC_A_31_DN		A	
PHY_DRV_A_TO_SCC_A_35_DP	PHY_DRV_A_TO_SCC_A_34_DN	PHY_DRV_A_TO_SCC_A_33_DP	PHY_DRV_A_TO_SCC_A_32_DN	PHY_DRV_A_TO_SCC_A_31_DP	PHY_DRV_A_TO_SCC_A_30_DN	B	A
	PHY_DRV_A_TO_SCC_A_34_DP		PHY_DRV_A_TO_SCC_A_32_DP		PHY_DRV_A_TO_SCC_A_30_DP		B
DRIVE_A_26_ACT		DRIVE_A_30_ACT		DRIVE_A_34_ACT		C	
DRIVE_A_27_ACT	DRIVE_A_28_ACT	DRIVE_A_31_ACT	DRIVE_A_32_ACT	DRIVE_A_35_ACT	SCC_A_HS_EN	D	C
	DRIVE_A_29_ACT		DRIVE_A_33_ACT		SCC_A_FULL_PGOOD		D
PHY_SCC_A_TO_DRV_A_35_DP		PHY_SCC_A_TO_DRV_A_33_DP		PHY_SCC_A_TO_DRV_A_31_DP		E	
PHY_SCC_A_TO_DRV_A_35_DN	PHY_SCC_A_TO_DRV_A_34_DP	PHY_SCC_A_TO_DRV_A_33_DN	PHY_SCC_A_TO_DRV_A_32_DP	PHY_SCC_A_TO_DRV_A_31_DN	PHY_SCC_A_TO_DRV_A_30_DP	F	E
	PHY_SCC_A_TO_DRV_A_34_DN		PHY_SCC_A_TO_DRV_A_32_DN		PHY_SCC_A_TO_DRV_A_30_DN		F

23.16 Rear Drive Plane Board SAS Connector (to SCC)
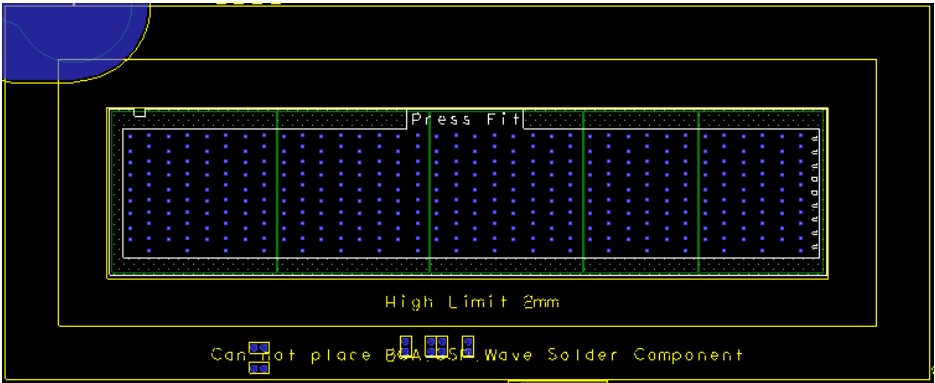
Figure 111: Rear DPB SAS Connector to SCC

Table 42. SCC RDPB SAS Connector (M2) pinout

M2.1

	1	2	3	4	5	6	Decoder	
	PHY_DRV_B_TO_SCC_B_5_DN		PHY_DRV_B_TO_SCC_B_3_DN		PHY_DRV_B_TO_SCC_B_1_DN		A	
	PHY_DRV_B_TO_SCC_B_5_DP	PHY_DRV_B_TO_SCC_B_4_DN	PHY_DRV_B_TO_SCC_B_3_DP	PHY_DRV_B_TO_SCC_B_2_DN	PHY_DRV_B_TO_SCC_B_1_DP	PHY_DRV_B_TO_SCC_B_0_DN	B	A
		PHY_DRV_B_TO_SCC_B_4_DP		PHY_DRV_B_TO_SCC_B_2_DP		PHY_DRV_B_TO_SCC_B_0_DP		B
	SCC_B_STBY_PGOOD		SCC_B_HEARTBEAT		SCC_B_TYPE_0		C	
	BMC_B_HEARTBEAT	P3V3_STBY_B	SCC_A_HEARTBEAT	SCC_B_SLOT_ID_0	SCC_B_TYPE_1	SCC_B_TYPE_2	D	C
		SCC_B_STBY_PWR_EN		SCC_B_SLOT_ID_1		SCC_B_TYPE_3		D
	PHY_SCC_B_TO_DRV_B_5_DP		PHY_SCC_B_TO_DRV_B_3_DP		PHY_SCC_B_TO_DRV_B_1_DP		E	
	PHY_SCC_B_TO_DRV_B_5_DN	PHY_SCC_B_TO_DRV_B_4_DP	PHY_SCC_B_TO_DRV_B_3_DN	PHY_SCC_B_TO_DRV_B_2_DP	PHY_SCC_B_TO_DRV_B_1_DN	PHY_SCC_B_TO_DRV_B_0_DP	F	E
		PHY_SCC_B_TO_DRV_B_4_DN		PHY_SCC_B_TO_DRV_B_2_DN		PHY_SCC_B_TO_DRV_B_0_DN		F

M2.2

7	8	9	10	11	12	Decoder	
PHY_DRV_B_TO_SCC_B_6_DN		PHY_DRV_B_TO_SCC_B_8_DN		PHY_DRV_B_TO_SCC_B_10_DN		A	
PHY_DRV_B_TO_SCC_B_6_DP	PHY_DRV_B_TO_SCC_B_7_DN	PHY_DRV_B_TO_SCC_B_8_DP	PHY_DRV_B_TO_SCC_B_9_DN	PHY_DRV_B_TO_SCC_B_10_DP	PHY_DRV_B_TO_SCC_B_11_DN	B	A
	PHY_DRV_B_TO_SCC_B_7_DP		PHY_DRV_B_TO_SCC_B_9_DP		PHY_DRV_B_TO_SCC_B_11_DP		B
UART_SDB_B_TX		SCC_B_PWR_LED		DRIVE_INSERT_ALERT_B_N		C	
UART_SDB_B_RX	PWM_SCC_B_ZONE_C	SCC_B_FULL_PWR_EN	SCC_B_FAULT_LED	SCC_B_INS_N	I2C_CLIP_B_SCL	D	C
	PWM_SCC_B_ZONE_D		SCC_B_RESET_N		I2C_CLIP_B_SDA		D
PHY_SCC_B_TO_DRV_B_6_DP		PHY_SCC_B_TO_DRV_B_8_DP		PHY_SCC_B_TO_DRV_B_10_DP		E	
PHY_SCC_B_TO_DRV_B_6_DN	PHY_SCC_B_TO_DRV_B_7_DP	PHY_SCC_B_TO_DRV_B_8_DN	PHY_SCC_B_TO_DRV_B_9_DP	PHY_SCC_B_TO_DRV_B_10_DN	PHY_SCC_B_TO_DRV_B_11_DP	F	E
	PHY_SCC_B_TO_DRV_B_7_DN		PHY_SCC_B_TO_DRV_B_9_DN		PHY_SCC_B_TO_DRV_B_11_DN		F

M2.3

13	14	15	16	17	18	Decoder	
PHY_DRV_B_TO_SCC_B_12_DN		PHY_DRV_B_TO_SCC_B_14_DN		PHY_DRV_B_TO_SCC_B_16_DN		A	
PHY_DRV_B_TO_SCC_B_12_DP	PHY_DRV_B_TO_SCC_B_13_DN	PHY_DRV_B_TO_SCC_B_14_DP	PHY_DRV_B_TO_SCC_B_15_DN	PHY_DRV_B_TO_SCC_B_16_DP	PHY_DRV_B_TO_SCC_B_17_DN	B	A
	PHY_DRV_B_TO_SCC_B_13_DP		PHY_DRV_B_TO_SCC_B_15_DP		PHY_DRV_B_TO_SCC_B_17_DP		B
UART_EXP_B_TX		I2C_DRIVE_B_PWR_SCL		I2C_DRIVE_B_FLT_LED_SCL		C	
UART_EXP_B_RX	I2C_DPB_B_SCL_BUF	I2C_DRIVE_B_PWR_SDA	I2C_DRIVE_B_INS_SCL	I2C_DRIVE_B_FLT_LED_SDA	DRIVE_B_0_ACT	D	C
	I2C_DPB_B_SDA_BUF		I2C_DRIVE_B_INS_SDA		DRIVE_B_1_ACT		D
PHY_SCC_B_TO_DRV_B_12_DP		PHY_SCC_B_TO_DRV_B_14_DP		PHY_SCC_B_TO_DRV_B_16_DP		E	
PHY_SCC_B_TO_DRV_B_12_DN	PHY_SCC_B_TO_DRV_B_13_DP	PHY_SCC_B_TO_DRV_B_14_DN	PHY_SCC_B_TO_DRV_B_15_DP	PHY_SCC_B_TO_DRV_B_16_DN	PHY_SCC_B_TO_DRV_B_17_DP	F	E
	PHY_SCC_B_TO_DRV_B_13_DN		PHY_SCC_B_TO_DRV_B_15_DN		PHY_SCC_B_TO_DRV_B_17_DN		F

M2.4

19	20	21	22	23	24	Decoder	
PHY_DRV_B_TO_SCC_B_23_DN		PHY_DRV_B_TO_SCC_B_21_DN		PHY_DRV_B_TO_SCC_B_19_DN		A	
PHY_DRV_B_TO_SCC_B_23_DP	PHY_DRV_B_TO_SCC_B_22_DN	PHY_DRV_B_TO_SCC_B_21_DP	PHY_DRV_B_TO_SCC_B_20_DN	PHY_DRV_B_TO_SCC_B_19_DP	PHY_DRV_B_TO_SCC_B_18_DN	B	A
	PHY_DRV_B_TO_SCC_B_22_DP		PHY_DRV_B_TO_SCC_B_20_DP		PHY_DRV_B_TO_SCC_B_18_DP		B
DRIVE_B_2_ACT		DRIVE_B_6_ACT		DRIVE_B_10_ACT		C	
DRIVE_B_3_ACT	DRIVE_B_4_ACT	DRIVE_B_7_ACT	DRIVE_B_8_ACT	DRIVE_B_11_ACT	DRIVE_B_12_ACT	D	C
	DRIVE_B_5_ACT		DRIVE_B_9_ACT		DRIVE_B_13_ACT		D
PHY_SCC_B_TO_DRV_B_23_DP		PHY_SCC_B_TO_DRV_B_21_DP		PHY_SCC_B_TO_DRV_B_19_DP		E	
PHY_SCC_B_TO_DRV_B_23_DN	PHY_SCC_B_TO_DRV_B_22_DP	PHY_SCC_B_TO_DRV_B_21_DN	PHY_SCC_B_TO_DRV_B_20_DP	PHY_SCC_B_TO_DRV_B_19_DN	PHY_SCC_B_TO_DRV_B_18_DP	F	E
	PHY_SCC_B_TO_DRV_B_22_DN		PHY_SCC_B_TO_DRV_B_20_DN		PHY_SCC_B_TO_DRV_B_18_DN		F

M2.5

25	26	27	28	29	30	Decoder	
PHY_DRV_B_TO_SCC_B_24_DN		PHY_DRV_B_TO_SCC_B_26_DN		PHY_DRV_B_TO_SCC_B_28_DN		A	
PHY_DRV_B_TO_SCC_B_24_DP	PHY_DRV_B_TO_SCC_B_25_DN	PHY_DRV_B_TO_SCC_B_26_DP	PHY_DRV_B_TO_SCC_B_27_DN	PHY_DRV_B_TO_SCC_B_28_DP	PHY_DRV_B_TO_SCC_B_29_DN	B	A
	PHY_DRV_B_TO_SCC_B_25_DP		PHY_DRV_B_TO_SCC_B_27_DP		PHY_DRV_B_TO_SCC_B_29_DP		B
DRIVE_B_14_ACT		DRIVE_B_18_ACT		DRIVE_B_22_ACT		C	
DRIVE_B_15_ACT	DRIVE_B_16_ACT	DRIVE_B_19_ACT	DRIVE_B_20_ACT	DRIVE_B_23_ACT	DRIVE_B_24_ACT	D	C
	DRIVE_B_17_ACT		DRIVE_B_21_ACT		DRIVE_B_25_ACT		D
PHY_SCC_B_TO_DRV_B_24_DP		PHY_SCC_B_TO_DRV_B_26_DP		PHY_SCC_B_TO_DRV_B_28_DP		E	
PHY_SCC_B_TO_DRV_B_24_DN	PHY_SCC_B_TO_DRV_B_25_DP	PHY_SCC_B_TO_DRV_B_26_DN	PHY_SCC_B_TO_DRV_B_27_DP	PHY_SCC_B_TO_DRV_B_28_DN	PHY_SCC_B_TO_DRV_B_29_DP	F	E
	PHY_SCC_B_TO_DRV_B_25_DN		PHY_SCC_B_TO_DRV_B_27_DN		PHY_SCC_B_TO_DRV_B_29_DN		F

M2.6

31	32	33	34	35	36	Decoder	
PHY_DRV_B_TO_SCC_B_35_DN		PHY_DRV_B_TO_SCC_B_33_DN		PHY_DRV_B_TO_SCC_B_31_DN		A	
PHY_DRV_B_TO_SCC_B_35_DP	PHY_DRV_B_TO_SCC_B_34_DN	PHY_DRV_B_TO_SCC_B_33_DP	PHY_DRV_B_TO_SCC_B_32_DN	PHY_DRV_B_TO_SCC_B_31_DP	PHY_DRV_B_TO_SCC_B_30_DN	B	A
	PHY_DRV_B_TO_SCC_B_34_DP		PHY_DRV_B_TO_SCC_B_32_DP		PHY_DRV_B_TO_SCC_B_30_DP		B
DRIVE_B_26_ACT		DRIVE_B_30_ACT		DRIVE_B_34_ACT		C	
DRIVE_B_27_ACT	DRIVE_B_28_ACT	DRIVE_B_31_ACT	DRIVE_B_32_ACT	DRIVE_B_35_ACT	SCC_B_HS_EN	D	C
	DRIVE_B_29_ACT		DRIVE_B_33_ACT		SCC_B_FULL_PGOOD		D
PHY_SCC_B_TO_DRV_B_35_DP		PHY_SCC_B_TO_DRV_B_33_DP		PHY_SCC_B_TO_DRV_B_31_DP		E	
PHY_SCC_B_TO_DRV_B_35_DN	PHY_SCC_B_TO_DRV_B_34_DP	PHY_SCC_B_TO_DRV_B_33_DN	PHY_SCC_B_TO_DRV_B_32_DP	PHY_SCC_B_TO_DRV_B_31_DN	PHY_SCC_B_TO_DRV_B_30_DP	F	E
	PHY_SCC_B_TO_DRV_B_34_DN		PHY_SCC_B_TO_DRV_B_32_DN		PHY_SCC_B_TO_DRV_B_30_DN		F

24 Labels and Markings

24.1 PCBA labels and markings

All PCBAs shall include the following labels, summarized in Table 43. The labels shall not be placed in such a way that may cause them to disrupt the functionality or airflow to the system.

Table 43. PCBA label requirements

Description	Type	Barcode Required?
Safety markings	Silkscreen	No
Vendor P/N, S/N, REV (revision would increment for any approved changes)	Adhesive label	Yes
Vendor logo, name & country of origin	Silkscreen	No
PCB vendor logo, name	Silkscreen	No
Facebook P/N	Adhesive label	Yes
Date code (industry standard: WEEK/YEAR)	Adhesive label	Yes
DC input ratings	Silkscreen	No
RoHS compliance	Silkscreen	No
WEEE symbol: ⌦ The motherboard will have the crossed out wheeled bin symbol to indicate that it will be taken back by the manufacturer for recycling at the end of its useful life. This is defined in the European Union Directive 2002/96/EC of January 27, 2003 on Waste Electrical and Electronic Equipment (WEEE) and any subsequent amendments.	Silkscreen	No

24.2 Chassis labels and markings

The chassis shall carry the following adhesive barcoded labels in locations that can easily be scanned during integration:

- Vendor P/N, S/N, REV (revision would increment for any approved changes)

- Facebook P/N (or OCP customer P/N)

- Date code (industry standard: WEEK/YEAR)

- The assembly shall be marked "THIS SIDE UP," "TOP SIDE," "UP ^," or other approved marking in bright, large characters in a color to be defined by ODM and Facebook (or OCP customer). This printing may be on the PCB itself, or on an installed component such as an air baffle. The label should be clear and easy to read in low light conditions, when viewed from above or below from two feet away, and at an angle of approximately 60 degrees off horizontal.

The exact label location will be agreed upon between the Vendor and Facebook.

24.3 Environmental & design requirements

Bryce Canyon must meet the following environmental requirements:

- Gaseous Contamination: Severity Level G1 per ANSI/ISA 71.04-1985

- Ambient operating temperature range: +5°C to +35°C

- Operating and storage relative humidity: 10% to 90% (non-condensing)

- Storage temperature range: -40°C to +70°C (long-term storage)

- Transportation temperature range: -55°C to +85°C (short-term storage)

- Operating altitude with no de-rating to 1000m (3300 feet)

24.4 Vibration and shock

Bryce Canyon must meet shock and vibration requirements according to the following IEC specifications: IEC78-2-(*) and IEC721-3-(*) Standard and Levels. The testing requirements are summarized in Table 44.

Table 44. Shock and vibration requirements

	Operating	Non-Operating
Vibration	0.4g acceleration, 5 to 500 Hz, 10 sweeps at 1 octave / minute per each of the three axes (one sweep is 5 to 500 to 5 Hz)	1g acceleration, 5 to 500 Hz, 10 sweeps at 1 octave / minute per each of the three axes (one sweep is 5 to 500 to 5 Hz)
Shock	6g, half-sine 11mS, 5 shocks per each of the three axes	12g, half-sine 11mS, 10 shocks per each of the three axes

24.5 Data center design requirements

- Seismic tie downs – GR63

- All casters will swivel

- Push / tilt / angle ramp testing – see OCP spec at www.opencompute.org

- Rack shall have entry and exit angle of 15 degrees minimum.

- Rack force (kgw) required to push the rack from a non-moving position along a smooth, flat cement floor shall be less than 5% the total combined weight (kgw) of the rack and IT Gear (note: this is a goal, not a hard requirement).

- The following tests will be performed with the rack loaded at the maximum rated IT load.

    o Roll over a 6mm vertical step with each caster independently at 0.5m/s

    o Transitioning a 1" wide gap in the floor while fully loaded at 0.5m/s

    o Transition a 5-degree ramp

    o Roll a minimum of 800m on a concrete floor at 0.8m/s

- Transportation shock/vibration testing per ASTM D4169-09, Assurance Level II, Mechanized handling, truck, no stacking, distribution cycle 2. Alternative testing may be acceptable, with Facebook approval.

- Seismic testing: NEBS GR63 zone 2 with the rack levelling feet lowered. Racks may be ganged together prior to test. NEBS GR63 zone 4 with the rack levelling feet lowered. Racks may be ganged together prior to test.

- Levelling feet requirements: The rack will provide four levelling feet to remove the weight off of the casters once deployed in the data center. The feet shall:

  o Be delivered from the rack supplier in the raised condition and stay in that condition under ASTM D4169-09 as defined in 17.4 <confirm this reference>.

  o Be capable of raising and lowering the feet to their maximum height using only an electric driver from the front and/or rear (side access not allowed)

  o Be capable of cycling three times up and down under maximum cabinet load without damage to the rack or the leveler.

  o Be capable of supporting the rack under maximum weight under the GR63 zone 4 as defined in 17.4 <confirm this reference>.

  o Have a swivel base to prevent the rack from "walking" when the feet are deployed.

  o Be capable of raising the rack a minimum of 35mm off of the floor.

- Cabinet life: Rack should be designed for an expected life of 10 years under the following environmental conditions:

  o Humidity: 85% max, 42°F dew point minimum

- Cabling and grounding: Cables should be retained out of the path of the FRUs so service events will not damage cables during installation and removal.

- Cables can be added and removed from the cable retention without tools.

- No sharp edges, and burrs must be removed around cable routing areas to prevent damage.

24.6 Mean Time Between Failure (MTBF) requirements

[Placeholder]

24.7 Certifications

The Vendor needs to provide CB reports of the Bryce Canyon system at the component level.

25 Compliance Engineering

25.1 Vendor Responsibilities

Responsible for successful completion and demonstration of compliance to the FCC Authorization Program Requirements, EU Directive requirements, and NRTL Product Safety requirements specified below for L10 product.

25.2 Vendor Deliverables

- **FCC Compliance:** The product shall comply with FCC sub-part 15 b class A. Characterization documentation and test data shall be provided.
- **CE Compliance:** The Product shall comply with the EU Directives noted below. Facebook shall be provided with a CE Declaration of Conformity and complete technical reports and other documentation files for:
  a. The Low Voltage Directive; 2014/35/EU
  b. The EMC Directive; 2014/30/EU
  c. RoHS 2 Directive; 2011/65/EU, unless there are legal exemptions allowed
  d. REACH Regulation; 1907/2006

25.3 Product Safety Compliance

NRTL Certificate and complete technical report(s) per EN 60950-1, UL 60950-1, CAN/CSA-C22.2 No. 60950-1; Safety of Information Technology Equipment, General Requirements per Edition 2 and Amendment 2.

26 Prescribed Materials

26.1 Disallowed components

The following components are not to be used in the design of the system:
- Components disallowed by the European Union's Restriction of Hazardous Substances directive (RoHS 6)

- Trimmers and/or potentiometers

- Dip switches

26.2 Capacitors and inductors

The following limitations apply to the use of capacitors:
- Only aluminum organic polymer capacitors made by high quality manufacturers are used; they must be rated 105°C

- All capacitors have a predicted life of at least 50,000 hours at 45°C inlet air temperature, under worst conditions

- Tantalum capacitors using manganese dioxide cathodes are forbidden

- SMT ceramic capacitors with case size >1206 are forbidden (size 1206 are still allowed when installed far from the PCB edge and with a correct orientation that minimizes risk of cracks)

- Ceramic material for SMT capacitors must be X7R or better material (COG or NP0 type are used in critical portions of the design).

- Only SMT inductors may be used. The use of through hole inductors is disallowed.

26.3 Component de-rating

For inductors, capacitors, and FETs, de-rating analysis is based on at least 20% de-rating.

26.4 Sustainable materials

Materials and finishes that reduce the life cycle impact of servers should be used where cost and performance are not compromised. This includes the use of non-hexavalent metal finishes, recycled and recyclable base materials and materials made from renewable resources, with associated material certifications.

Facebook identified plastic alternatives including polypropylene plus natural fiber (PP+NF) compounds that meet functionality requirements while reducing cradle-to-gate environmental impact when compared to PC/ABS. GreenGranF023T is one acceptable alternate material. JPSECO also offers a PP+NF material that is acceptable; the model number will be available at a later date. It is strongly preferred that such alternatives are identified and used. If vendor is unable to use this, or a similar alternate material, vendor will provide a list of materials that were considered and why they were not successfully incorporated.

The supplier shall use Halogen Free (IEC 61249-2-21), arsenic-free (less than 1000 ppm, or 0.1% by weight) and phthalate-free (less than 1000 ppm, or 0.1% by weight) material by default and discuss with Facebook and get written approval if there is difficulty with sourcing in L10.