LSI® Nytro™ XP6209 Application Acceleration Card Datasheet

1 Scope

This document defines the technical specifications for the LSI Nytro XP6209 Application Acceleration Card used in Open Compute Project servers.

2 Contents

3 Document Overview

3.1 License

As of January 28, 2014, the following persons or entities have made this Specification available under the Open Web Foundation Contributor License Agreement, which is available at http://www.dmarc.org/OWF_CLA_1-0_Copyright_Patent.pdf

LSI Corporation

You can review the signed copies of the Open Web Foundation Contributor License Agreement for this Specification at http://opencompute.org/licensing/, which may also include additional parties to those listed above.

Your use of this Specification may be subject to other third party rights. THIS SPECIFICATION IS PROVIDED "AS IS." The contributors expressly disclaim any warranties (express, implied, or otherwise), including implied warranties of merchantability, non-infringement, fitness for a particular purpose, or title, related to the Specification. The entire risk as to implementing or otherwise using the Specification is assumed by the Specification implementer and user. IN NO EVENT WILL ANY PARTY BE LIABLE TO ANY OTHER PARTY FOR LOST PROFITS OR ANY FORM OF INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES OF ANY CHARACTER FROM ANY CAUSES OF ACTION OF ANY KIND WITH RESPECT TO THIS SPECIFICATION OR ITS GOVERNING AGREEMENT, WHETHER BASED ON BREACH OF CONTRACT, TORT (INCLUDING NEGLIGENCE), OR OTHERWISE, AND WHETHER OR NOT THE OTHER PARTY HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

4 Introduction

This document describes the functional requirements for the **LSI® Nytro™** XP6209 PCI Express® (PCIe®) flash storage card.

5 Features

The **LSI Nytro** XP6209 Application Acceleration Card acts as a PCIe-based block storage device and presents itself to the operating system (OS) through a **Fusion-MPT™** interface.

This device uses an LSISAS2008 controller with firmware running on the LSISAS2008 I/O controller processor. Four of the LSISAS2008 ports are connected to each of the four Flash Storage Processors (FSPs), and each FSP is connected to 256-GB MLC NAND. Additional features include the following:

- Card dimensions are 68.9 mm × 167.65 mm, *PCI Express Local Bus Specification, Revision 2.0* low-profile, half-length card.
- Current support for *PCI Express Local Bus Specification, Revision 2.0*.
- Eight full-duplex PCIe lanes.
- Four FSPs.
- LSISAS2008 core voltages are 1.0 V, 1.8 V derived from PCI 3.3 V, and 3.3 V, derived from 12.0 V through switching regulators.
- Embedded Drive Voltages are 1.0 V, 1.8 V, 2.8 V, and 3.3 V are derived from 12.0 V.
- Capacitance backup on the embedded drives provides 15-ms uptime after a power failure.
- 8-MB NOR Flash.
- 32-KB NVSRAM.
- Debug LEDs: Heartbeat LED for the LSISAS2008 controller, Status and Fault LEDs for each of the four FSPs.
- ICE connector pads and hot-pluggable UART debug/diagnostic ports.
- PCIe half-height and full-height brackets, which contain three holes (one for each LED).
- Bracket LEDS: LEDs are visible through the PCIe bracket:
  - One green/yellow/red LED indicates drive life remaining.
  - One green/yellow/red LED indicates status.
  - One green/yellow/red LED indicates data activity.
- The following table shows capacity points for the **LSI Nytro** XP6209 Application Acceleration Card:

Card Number	SKU Identifier	Usable Capacity (Factory GB setting)	NAND Type
6209	NWD-6209-4A1024	930	MLC

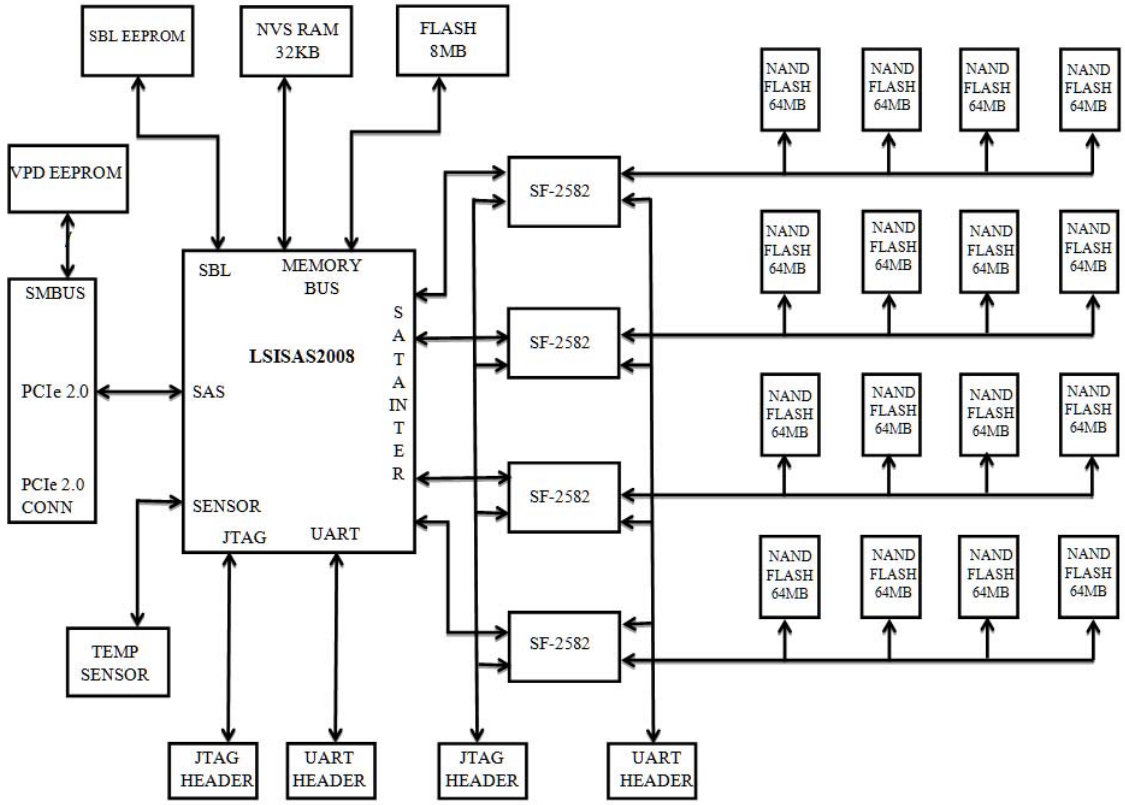
Table 1 Capacity Point for LSI Nytro XP6209 Application Acceleration Card

6 Functional Description

6.1 Block Diagram

The following figure shows the block diagram for the

Figure 1 LSI Nytro XP6209 Application Acceleration Card Block Diagram



6.2 PCIe Host Interface

PCIe is a high-speed standard local bus for point-to-point interfacing of I/O components to the processor and memory subsystems in a high-end PC. The PCIe functionality for the **LSI Nytro** XP6209 Application Acceleration Card is contained in the LSISAS2008 controller chip. The LSISAS2008 controller connects directly to the PCIe bus and generates timing and protocol in compliance with the PCIe specifications. The *LSISAS2008 PCI Express to SAS Technical Manual* provides a complete functional description of the PCIe interface as used on the **LSI Nytro** XP6209 Application Acceleration Card. The LSISAS2008 JTAG signals are not connected to the corresponding signals in the PCIe connector.

6.3 Flash Memory

The **LSI Nytro** XP6209 Application Acceleration Card provides an 8-Mb × 8-bit NOR Flash memory device and a 32-KB NVRAM device that

provides access to nonvolatile parameter storage for the LSI SAS 2008 device. A 4-KB Serial bootstrap ROM configures the PCIe settings, such as the PCIe device ID, vendor ID, subsystem device ID, and subsystem vendor ID. Additional EEPROMs store product-related data and key encryption codes. With the correct software utilities, you can reprogram most of these devices on the card when installed in a PCIe slot.

6.4 LEDs and GPIO Usage

The LSISAS2008 controller interfaces with the FSPs on the **LSI Nytro** XP6209 Application Acceleration Card. This interface has control pins that are attached to the LSISAS2008 GPIO. The following table shows how to connect the GPIO pins.

GPIO	Use	Direction	Polarity
0	–	–	–
1	–	–	–
2	–	–	–
3	–	–	–
4	RAID Key	Bi	N/A
5	–	–	–
6	–	–	–
7	–	–	–
8	–	–	–
9	DM DATASAFE	Input	1: Safe
10	–	–	–
11	–	–	–
12	–	–	–
13	–	–	–
14	Temp Sensor Alert	Input	1: Safe
15	–	–	–
16	Phy 0 Activity	Output	0: Active
17	–	–	–
18	–	–	–
19	LED1 Red	Output	0: On
20	Phy 4 Activity	Output	0: Active
21	12-V Monitor	Input	0: Fail
22	SBL Write Protect (Provisioned)	Output	1: Protect
23	LED1 Green	Output	0: On
24	Backup Monitor	Input	1: Fail
25	–	–	–

Table 2 LSI Nytro XP6209 Application Acceleration Card GPIO Usage

26	LED2 Red	Output	0: On
27	–	–	–
28	LED2 Green	Output	0: On
29	–	–	–
30	–	–	–
31	–	–	–
32	–	–	–
33	–	–	–
34	–	–	–
35	–	–	–

Table 2 LSI Nytro XP6209 Application Acceleration Card GPIO Usage (Continued)

6.4.1 Troubleshooting the LSI Nytro XP6209 Application Acceleration Card

The bracket LEDs provide key status information to diagnose any troubleshooting issues with the **LSI Nytro** XP6209 Application Acceleration Card.

LED Name	LED Color	Troubleshooting Issue
Activity	Green	On, blinking – Indicates data activity on the card. No action required.
Life	Green	On, steady – The card has sufficient life remaining for programming and erasing the Flash memory. No action is required.
	Yellow	On, steady – The card has approximately 10% or less life remaining for programming and erasing the Flash memory. Plan for replacements.
	Red	On, steady – The card has no program or erase cycles left, and data can be read, but not written. Back up data, and copy to a new card.

Table 3 Troubleshooting Issues

Status	Green	On, steady – Normal.
		On, blinking – This LED lets the user locate a specific card in a rack of servers.
	Yellow	On, steady – Warning. This warning includes: • Incorrect operating system driver. Make sure that the card OS driver is installed. • Temperature warning. • Other component issues: Run the list and health commands in the `ddcli` utility to determine which component has an issue.
	Red	On, blinking – Firmware fault code: • Run the `ddcli` utility to determine which component has an issue. • If no information appears, reboot the system and retry. • If no information appears, call your field application engineer (FAE).
		On, steady – One of the following conditions applies: • One or more of the embedded drives has failed (IT mode). • At least one of the embedded drives has exceeded its temperature. Check that server fans are working. To reset this LED, reboot the server. • Other component issues: Run the list and health commands in the `ddcli` utility to determine which component has an issue. • The RAID volume has failed. • No RAID volume is configured.

Table 3 Troubleshooting Issues (Continued)

6.5 Input Voltage Monitors

The Flash controllers on the embedded drives require advance warning of power failure to prevent data corruption. This warning comes from the onboard input voltage monitors, which trip the power failure signal to the flash controllers.

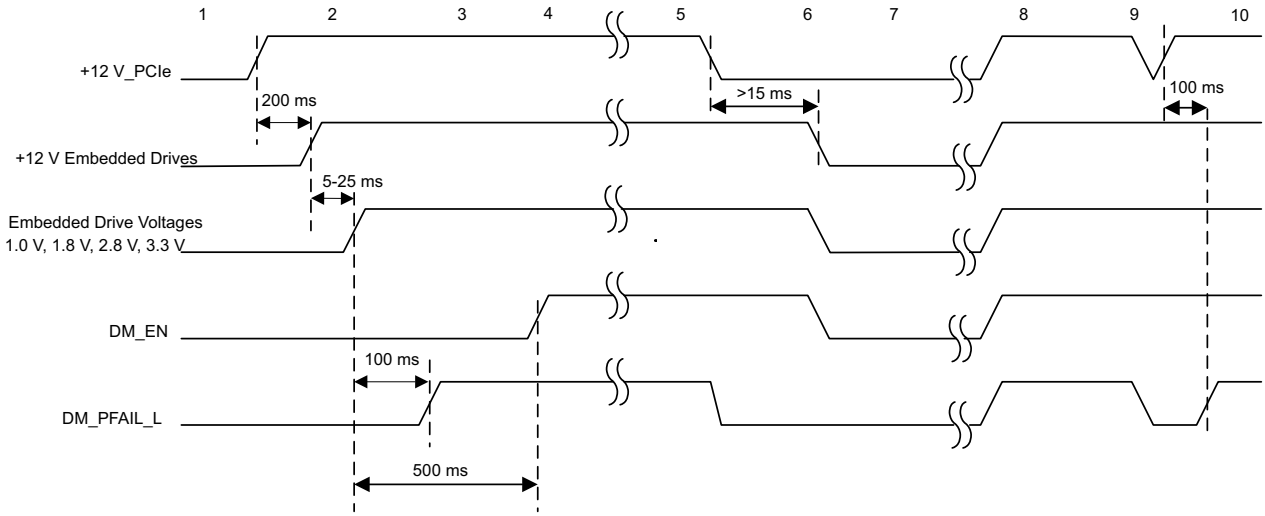
6.6 Holdup Capacitance

After the input rail voltage causes the power fail signal to trip, the bulk holdup capacitance holds up the drive rail power supply for a minimum of 15 ms to permit the embedded drives to complete any required shutdown tasks before power-off. This capacitance has a monitoring circuit to verify that no capacitor has shorted and caused a physical issue.

6.7 LSISAS2008 Board Power Sequencing and Monitoring

The following figure shows how the control signals on the **LSI Nytro** XP6209 Application Acceleration Card works. Time units 1 through 4 apply to startup. Units 5 through 7 apply to shutdown or a power failure. Units 8 through 10 show the behavior if a glitch occurs on input power; the same glitch can also occur on the 3.3-V PCIe rail.

Figure 2 LSI Nytro XP6209 Application Acceleration Card Control Signals



6.7.1 Startup

During startup, the 12.0-V embedded drive rail powers up and permits limited current to flow to the capacitor array charging the 12.0-V embedded drive rail. The delays involved plus the charging take less than 200 ms. When the 12.0-V embedded drive rail reaches 6.0 V to 7.0 V, the regulator starts to switch on. When the regulator is switched on, the voltage monitors that control the DM_Enable signal and the DM_PFAIL_L signal perform their function.

The DM_PFAIL_L signal alerts the drives if an input power supply (12.0-V PCIe rail or 3.3-V-PCIe rail) falls below an acceptable level, and maintains the signal for at least 100 ms. The 100-ms delay makes sure that no case exists where the drives have not safeguarded all data, because they are designed to complete saves in 15 ms. The DM_Enable signal permits drives to be enabled at all times, but because the DM_PFAIL_L signal is not in the required state at start of day, the DM_Enable signal delays 500 ms to permit the DM_PFAIL_L signal to attain the correct state.

6.7.2 Shutdown or Power Failure

If a power failure or shutdown occurs, the voltage monitor controlling the DM_PFAIL_L signal detects the drop in voltage. This drop in voltage trips the signal to alert the FSPs to prepare for shutdown. The **LSI Nytro** XP6209 Application Acceleration Card provides at least 15 ms for the devices to prepare for power-off. After 15 ms, the regulator turns off after the 12.0-V rail decays to below 6.5 V.

6.7.3 Out-of-Spec Input Rail Glitch Handling

If the input power supply (12.0-V PCIe rail or 3.3-V-PCIe rail) has a glitch that drops the voltage below the trip point, the PFAIL_L signal alerts the drives to prepare for shutdown. If this occurs, the PFAIL_L signal returns to normal after 100 ms. This return permits the devices to be used again, but the firmware might need to disable and re-enable the drives. If this action occurs, the system asserts the PCIe reset signal because it is out of specification on the input rails.

7 Related Documents

This section lists related documents.

7.1 National, International, and Industry Standards

- IEEE Std 1149.1-1990, *IEEE® Standard Test Access Port and Boundary-Scan Architecture*
- *PCI Express Local Bus Specification, Revision 2.0*
- *INCITS T10 SAS Specifications*
- SAS
- SATA protocol defined by the *ATA/AtAPI-7 Serial STA standard*
- *PCI Express Card Electromechanical Specification, Revision 2.0*
- *SMBus Specification*

7.2 Other Normative References

LSISAS2008 PCI Express to SAS Technical Manual

Fusion-MPT Interface

Ddcli Utility

7.3 Clarification

The documents identified in this Section 7 are normative references. As such, they are merely referenced in this datasheet and therefore fall within the exception set forth in the Granted Claims definition of Section 10.5 of the Open Web Foundation Contributor License Agreement. Additionally, hardware components (such as, but not limited to, those depicted in the Figure 1 Block Diagram of Section 6.1 of this datasheet), and their associated functionality, fall within the exception set forth in the Granted Claims definition. Therefore, to be clear, the definition of Granted Claims excludes the content of Sections 1 through 7 of this datasheet. Only the content set forth beginning in Section 8 of this datasheet is eligible for consideration as being Granted Claims (and even though eligible for consideration, portions of the content beginning in Section 8 of this datasheet that are merely referenced will not include Granted Claims.)

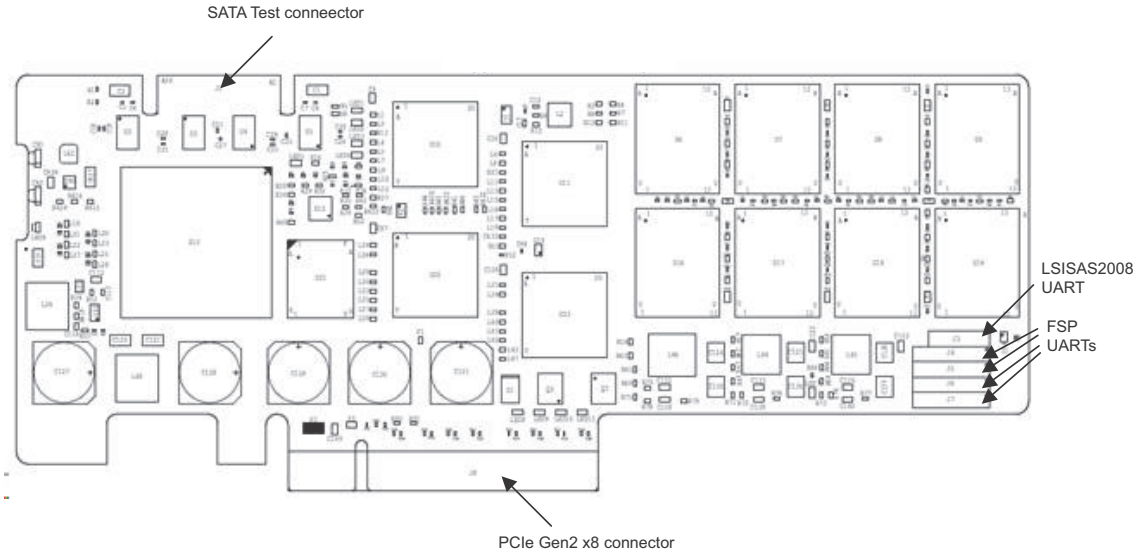
8 Physical Characteristics

The **LSI Nytro** XP6209 Application Acceleration Card has the following physical characteristics:

- The card has dimensions of 68.9 mm × 167.65 mm.
- The card makes the PCIe connection through the edge connector.
- The component height on the top and the bottom of the card follows the PCIe specifications.

The following figure shows the layout of the card.

Figure 3 LSI Nytro XP6209 Application Acceleration Card Connectors



8.1 Electrical Characteristics

The **LSI Nytro** XP6209 Application Acceleration Card consumes power from the PCIe 12.0-V and 3.3-V rails.

Use the following data for power consumption measured with the 16-KB I/O size:

- 12.0-V DC at 1.12 Amps (13.44W)
- 3.3-V DC at 1.57 Amps (5.18 W)
- 3.3-Vaux DC at 0.03 A (0.1 W)

8.2 Thermal Characteristics

The board is designed to operate in an environment defined by the following parameters:

- Temperature range: 0 °C to 50 °C
- Relative humidity range: noncondensing 5% to 90%
- Maximum wet bulb temperature: 28 °C
- Minimum airflow: 250 LFM

The board is designed for the following storage and transit environmental parameters:

- Temperature range: –20 °C to 75 °C
- Relative humidity range: noncondensing 5% to 95%

NOTE Because of system design and cooling capacity variations, which can affect the actual airflow delivered to the **LSI Nytro** XP6209 Application Acceleration Card card, the system-level fan speeds might require adjustment to make sure that the **LSI Nytro** XP6209 Application Acceleration Card sensor temperature does not exceed 74 °C.

8.3 Weight

The **LSI Nytro** XP6209 Application Acceleration Card weighs 0.23 lb.

9 Connectors

9.1 PCIe Edge Connector

PCIe implements through a ×8 edge connector, EC1, which provides connections on both the top (EC1B) and bottom (EC1A) of the card. The signal definitions and pin numbers conform to the *PCI Express Card Electromechanical Specification, Revision 2.0*. The following tables show the signal assignments. Card functions are powered from the host system PCIe 12.0-V power rail and the 3.3-V power rail. The 3.3-Vaux rail is used for one SEEPROM IC.

EC1B (Top Side)	
Signal Name	Pin
+12 V	1
+12 V	2
+12 V	3
GND	4
SMLK	5
SMDAT	6
GND	7
+3.3 V	8
TRST	9
3.3 Vaux	10
WAKE	11
Mechanical	Key
Reserved	12
GND	13
PETp0	14

EC1A (Bottom Side)	
Signal Name	Pin
PRSNT1	1
+12 V	2
+12 V	3
GND	4
TCK	5
TDI	6
TDO	7
TMS	8
+3.3 V	9
+3.3 V	10
PERST	11
Mechanical	Key
GND	12
REFCLK	13
REFCLK	14

Table 4 LSI Nytro XP6209 Application Acceleration Card PCI Express Connector EC1

PETn0	15	GND	15
GND	16	PETp0	16
PRSNT2#	17	PETn0	17
GND	18	GND	18
PETp1	19	Reserved	19
PETn1	20	GND	20
GND	21	PERp1	21
GND	22	PERn1	22
PETp2	23	GND	23
PETn2	24	GND	24
GND	25	PERp2	25
GND	26	PERn2	26
PETp3	27	GND	27
PETn3	28	GND	28
GND	29	PERp3	29
Reserved	30	PERn3	30
PRSNT2	31	GND	31
GND	32	Reserved	32
PETp4	33	Reserved	33
PETn4	34	GND	34
GND	35	PERp4	35
GND	36	PERn4	36
PETp5	37	GND	37
PETn5	38	GND	38
GND	39	PERp5	39
GND	40	PERn5	40
PETp6	41	GND	41
PETn6	42	GND	42
GND	43	PERp6	43
GND	44	PERn6	44
PETp7	45	GND	45
PETn7	46	GND	46
GND	47	PERp7	47
PRSNT2	48	PERn7	48
GND	49	GND	49

NOTE Shaded cells are optional sideband signals and do not have to be implemented on the targeted system.

Table 4 LSI Nytro XP6209 Application Acceleration Card PCI Express Connector EC1 (Continued)

9.2 LSISAS2008 UART Debug Header

The LSISAS2008 controller provides one industry-standard UART implementation for test and debug purposes. The firmware can use the LSISAS2008 serial interface to send debug information to an external terminal. The following table shows the signal assignments of the 1x4, J3, UART connector.

Signal Name	Pin
UART0_RX	1
GND	2
UART0_TX	3
3.3V	4

Table 5 LSI Nytro XP6209 Application Acceleration Card UART Header Signals

9.3 FSPs UART Debug Headers

The **LSI Nytro** XP6209 Application Acceleration Card has four 1x5 debug UARTs, one for each of the four FSPs present on the card. This sends debug information from the FSPs to an external terminal.

Signal Name	Pin
SFx_RX	1
Ground	2
SFx_TX	3
GPIO1	4
FLASH_WP	5

Table 6 LSI Nytro XP6209 Application Acceleration Card FSP UART Header Signals

10 Compatibility

The PCIe interface is compatible with the appropriate sections in the *PCI Express Local Bus Specification, Revision 2.0*. The embedded drive interfaces are compatible with the SATA protocol defined by the ATA/ATAPI-7 Serial ATA standard.

11 Constraints

The **LSI Nytro** XP6209 Application Acceleration Card must be installed in a half-height or full-height, PCIe bus-based machine with standard PCIe mounting bracket hardware.

12 Data Integrity

The **LSI Nytro** XP6209 Application Acceleration Card supports cyclic redundancy check (CRC) generation and checking on PCIe and on SATA buses. The flash controllers support up to 55-bit ECC and RAISE™ technology to ensure data integrity for the data written into or read from the NAND media.

13 Design for Testability

The LSISAS2008 controller incorporates 1149.1 to test pin continuity during board manufacturing test. The SATA test connector is for LSI internal testing purposes only.

14 Human Factors

All component and optional designators, such as the following features, are labeled on the [1]**LSI Nytro** XP6209 Application Acceleration Card:

- Card name
- LEDs
- Barcode
- Assembly label locations

1. **LSI**, **Nytro**, **Fusion-MPT** and **RAISE** are trademarks or registered trademarks of LSI Corporation in the United States and/or other countries. Other trademarks mentioned herein are the trademarks of their respective owners