Modern Design Methodologies for Next-Gen Multi-Chip(let) Packaging

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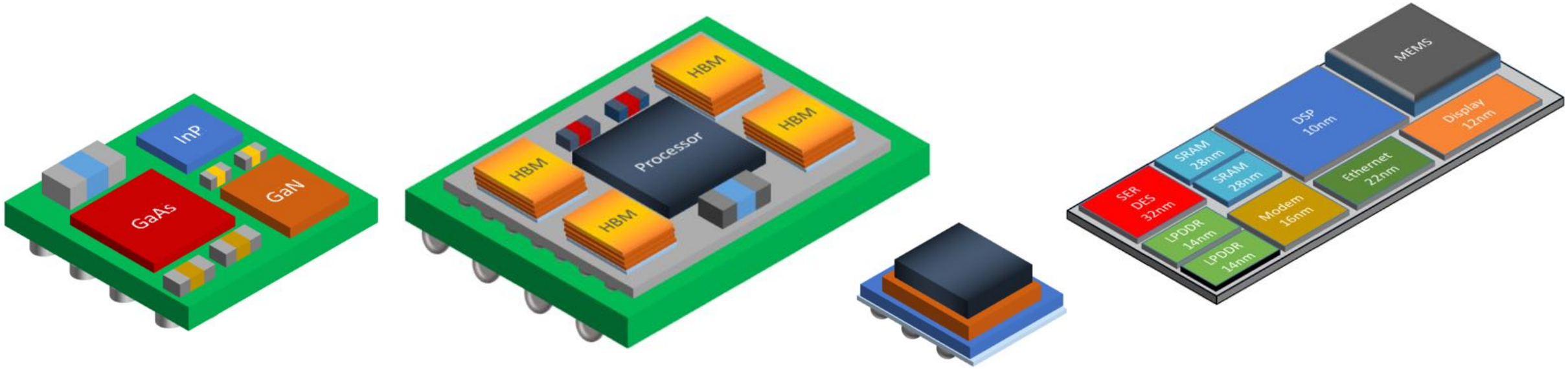
Outline

- Advanced Multi-Chip(let) Packaging Technology Trends
- The Big Picture: Cadence Multi-Chip(let) Advanced Packaging
- Example: Multi-Chip(let) Flow

The Evolution of Multi-Chip(let) Packaging…Heterogenous Integration

PCB Style Design Flows — IC Style Design Flows



Multi-Chip Module (MCM) — 1980

System in a Package (SiP) RF Module — 2005

Heterogeneous Integration — 2008 — Now

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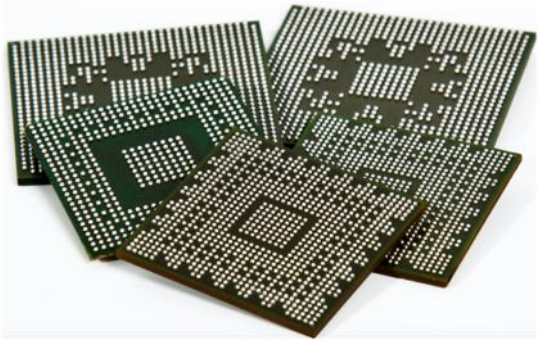
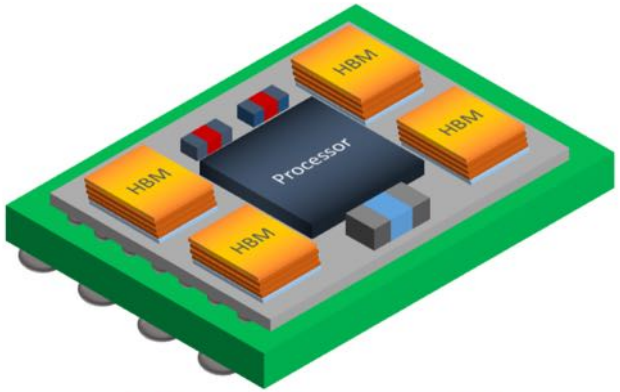
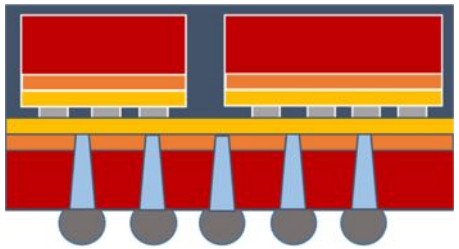
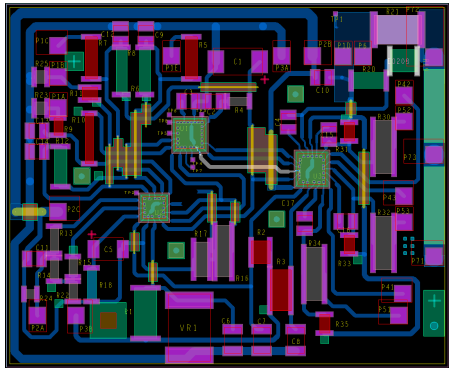
The Next Packaging Paradigm Change is Here…

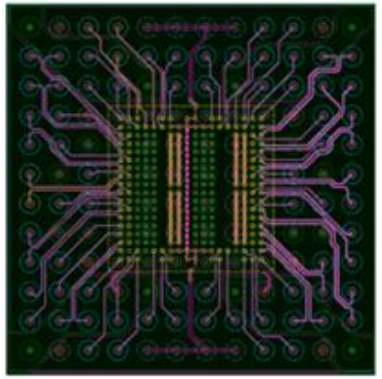
Mechanical Design Tools	PCB-Like Design Flows	Hybrid Design Flows	IC-Like Design Flows
Mechanical Leadframe	Routable Substrates Organic & Ceramic	2.5D-IC/Silicon Interposer, Embedded Bridges & FOWLP	3D-IC

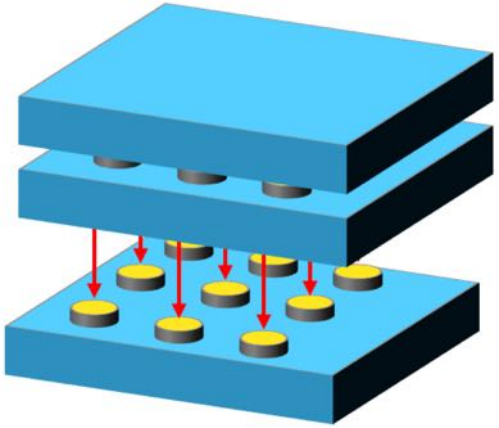












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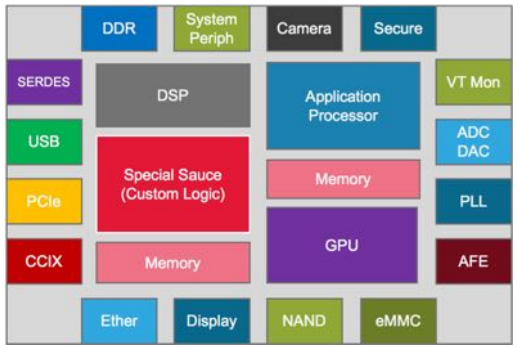
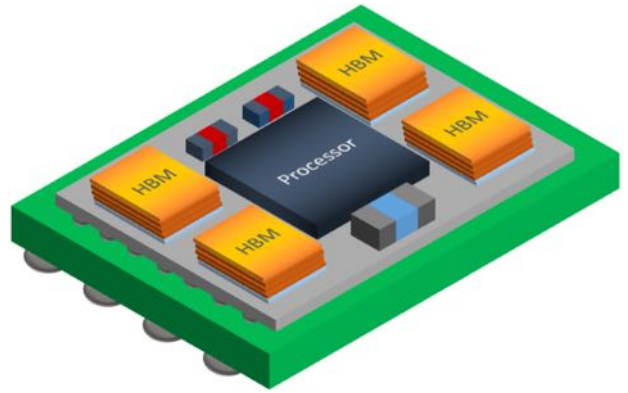
More Than Moore…What Does It Mean?

- Three major paradigm shifts changing the dynamics of the advanced packaging industry

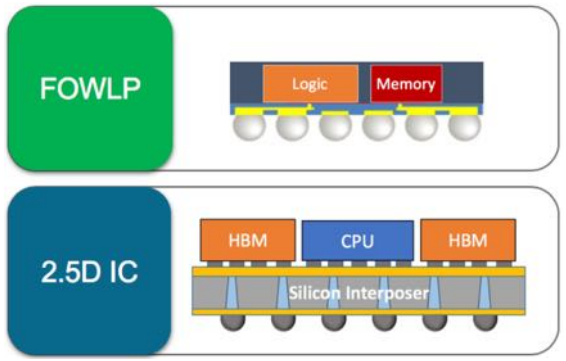


1) Heterogenous integration
   - New methods (chiplets) for SoC logical partitioning
   - SiP becoming the new SoC?



2) TSVs and FOWLP driving more silicon content in packages
   - 2.5D/3D IC wafer and chip stacking technologies

3) Semiconductor foundries offering advanced packaging solutions
   - Cadence continues to work with major semiconductor foundries and OSATs to develop advanced packaging certified reference flows



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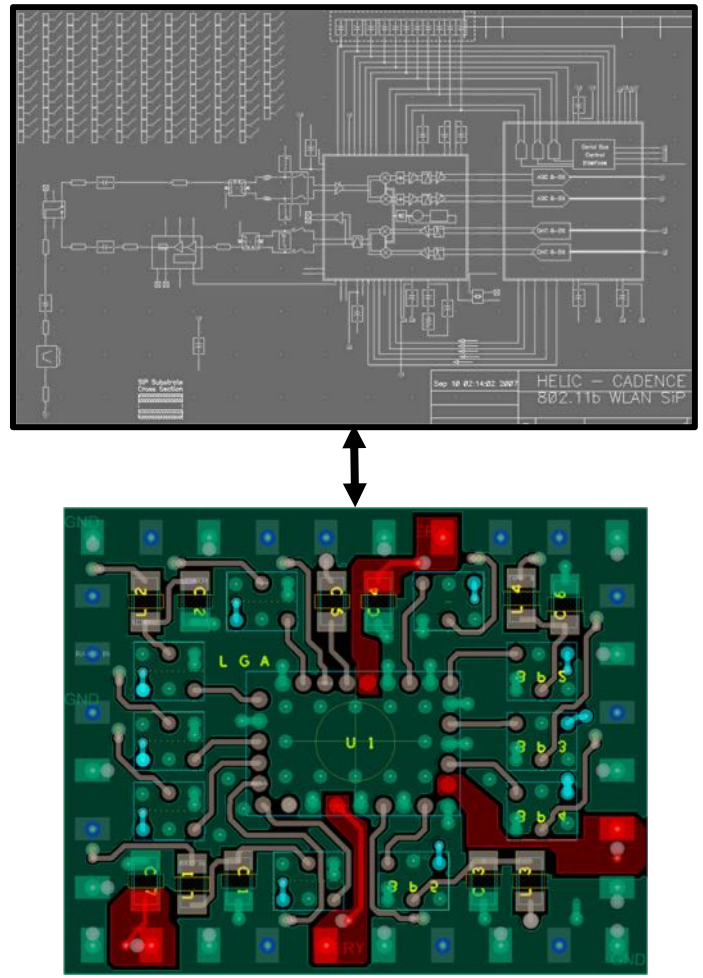
Design Tool/Flow Challenges for Next-Gen Heterogeneously Integrated Designs…Is It a Chip or a Package or a PCB?

- Packaging technology – silicon interposer, thin-film laminate, FOWLP – play an important role in determining the right tools/flow
  - Cross-domain planning and optimization (path finding)
    - How do you determine then optimize the right system-level solution?
  - What is the “right” level of chip(let) abstraction/representation in layout?
    - Simple (extents & pin locations), Complex (Full chip(let))
  - Connectivity definition
    - Schematic driven? HDL driven? Spreadsheet driven? Mixed?
  - Packages with silicon content require specialized verification steps
    - Layout vs schematic (LVS) connectivity validation
    - Mask-level physical DRC
    - Specialized metal fill and balancing
  - Cross-domain electrical modeling
    - How do you model the coupling effects between domains?
    - Linking different extraction tools for IC, package, and PCB?
  - Multi-PDK netlisting and simulation
    - How to handle namespace conflicts?



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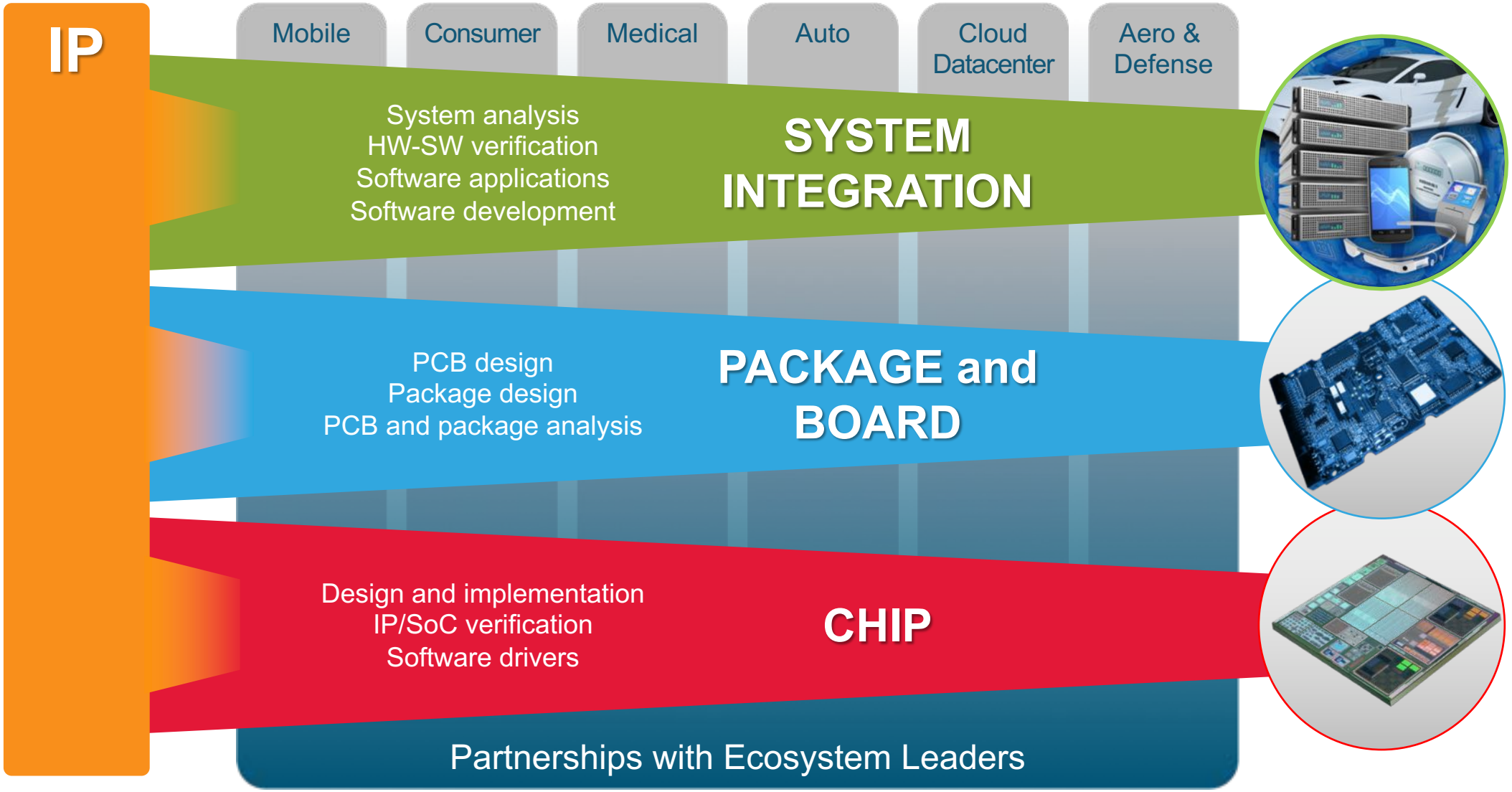
System Design Enablement (SDE)…Thinking Outside The Chip



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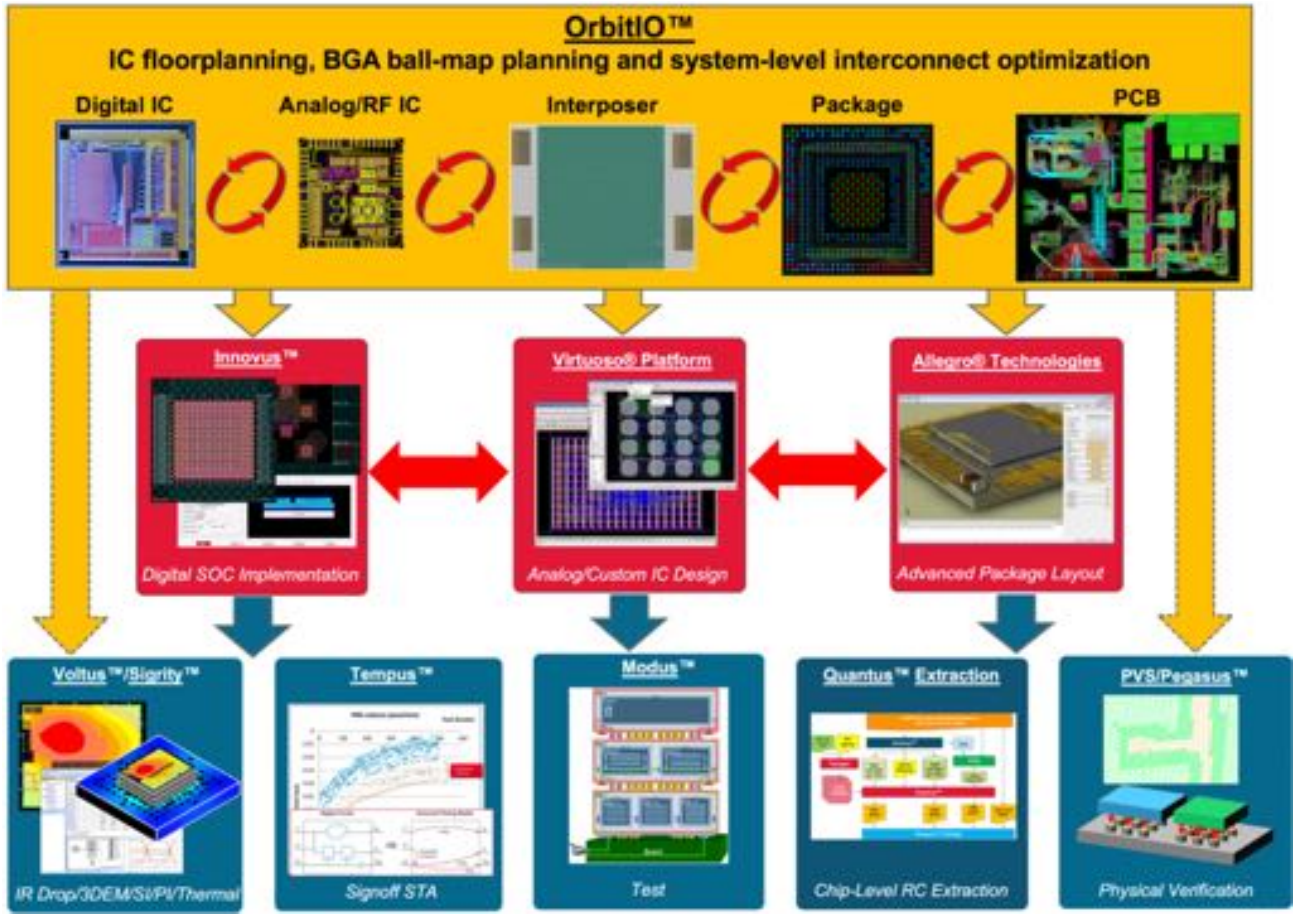
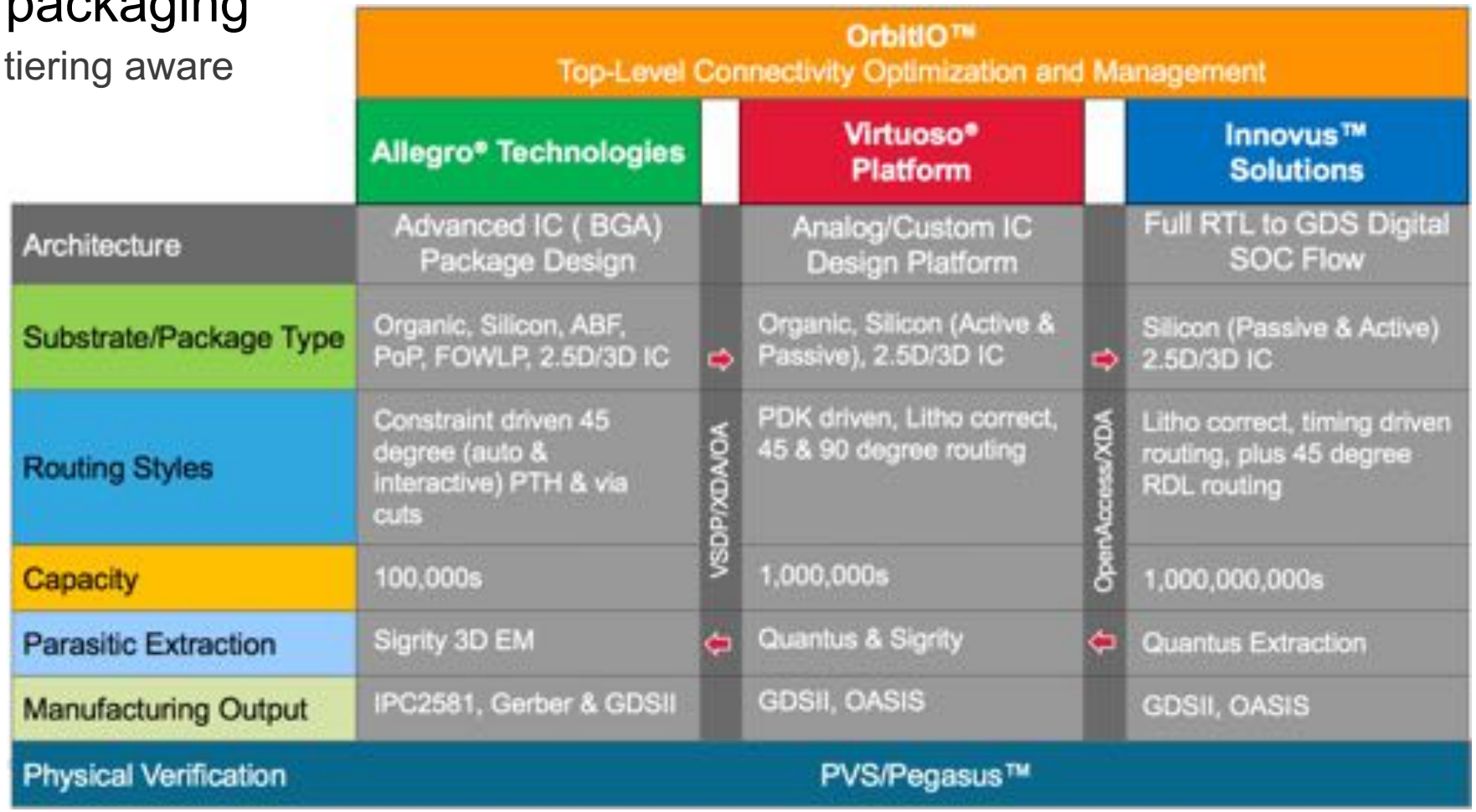
Multi-Chip(let) Packaging – Planning, Implementation and SignOff

- Top-Level cross-domain design management and optimization platform
  - Provides single canvas for planning and optimizing chip(let)s, interposers, packages and boards
  - Provides top-level data to aggregate complete design for signoff
    - Cross-domain connectivity
    - Chip(let) orientation
- Signoff and Test tools – Sigrity/Voltus, Quantus, PVS, Tempus, Xcelium and Modus – all support multi-chip(let) design
  - 3DEM/EM-IR/Thermal, RC extraction, physical DRC/LVS, STA, EM/IR, functional sim and test
- Cross-platform flows developed to streamline the interaction between IC, package and PCB design



Cadence-Wide Solutions for Next-Gen IC Packaging

- All three Cadence implementation platforms have been enabled to support next-gen advanced IC packaging
  - Multi-chip, TSV, MB, chip tiering aware
  - Usually flow type (digital IC, analog IC or core adv. packaging), routing style and manufacturing outputs determine platform of choice
  - Capacity often a driving factor
  - Two or more platforms may be required to create optimal design



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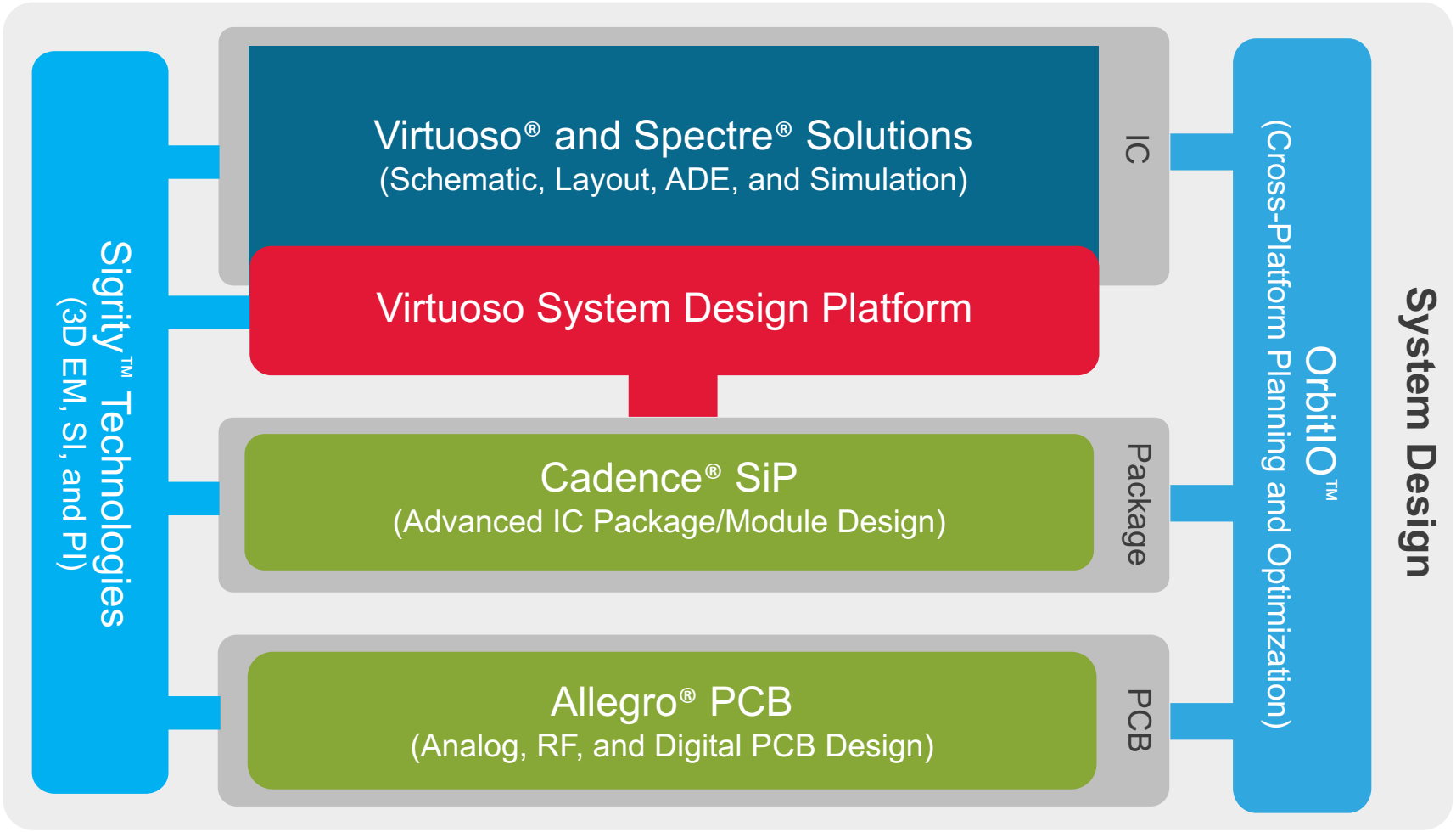
- Related Projects

Virtuoso® System Design Platform

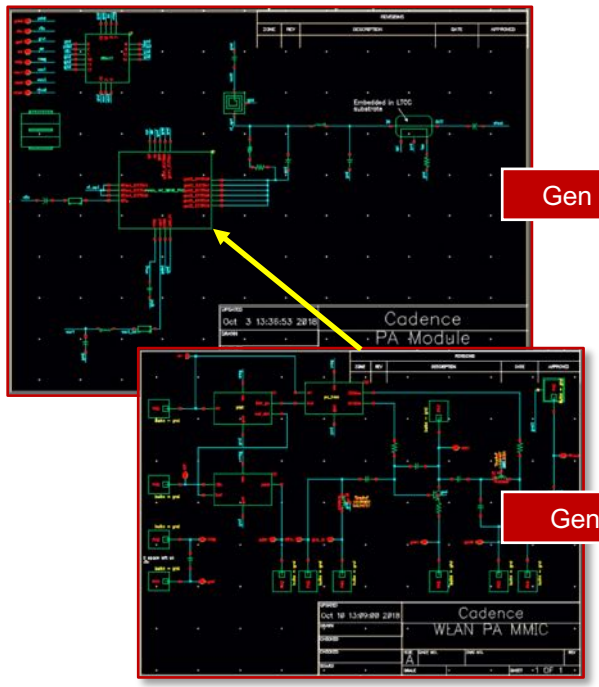
Extending IC design into multi-chip(let) system-level design



Virtuoso® for Intelligent System Design

- Cross-platform solution that integrates Virtuoso, Allegro and Sigrity technologies
- Industries first multi-chip(let) (multi-PDK) solution that provides system-level connectivity validation, automated layout parasitic feedback loop and true concurrent chip/package co-design

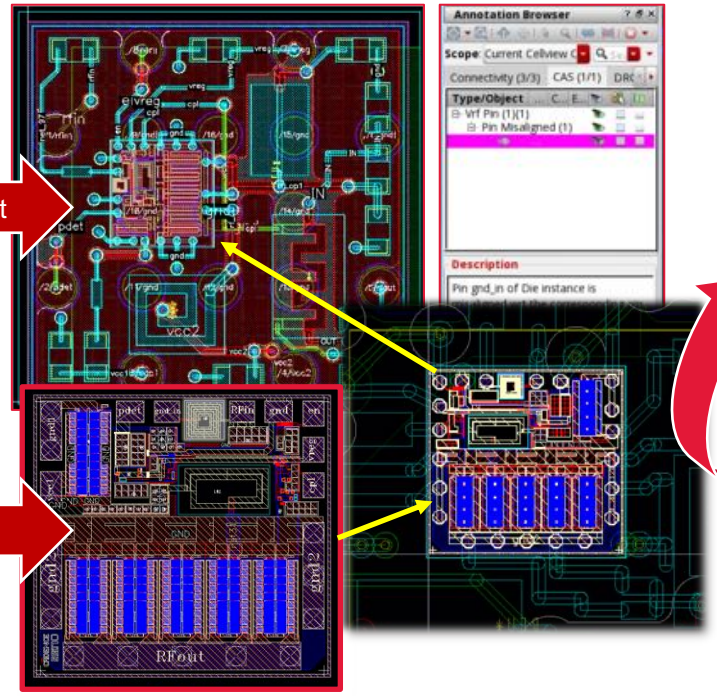
System Schematic Design & Capture
Capture "golden" schematics for RFIC & SIP using **Virtuoso Schematic** Editor



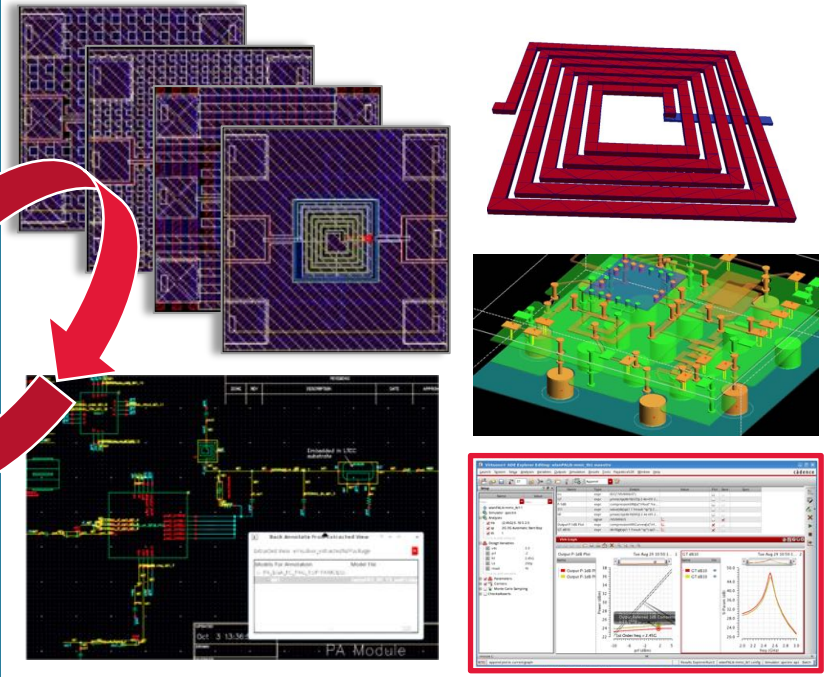
Gen SIP Layout

Gen IC Layout

Edit-in-Concert™
Edit SIP & RFIC in a single layout environment with multi-technology using **Virtuoso Layout Suite**

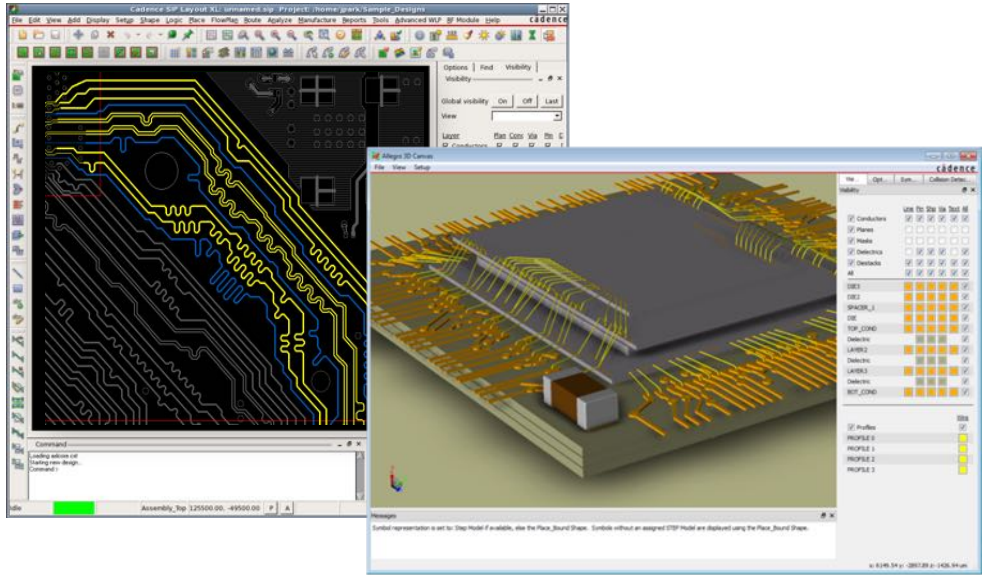


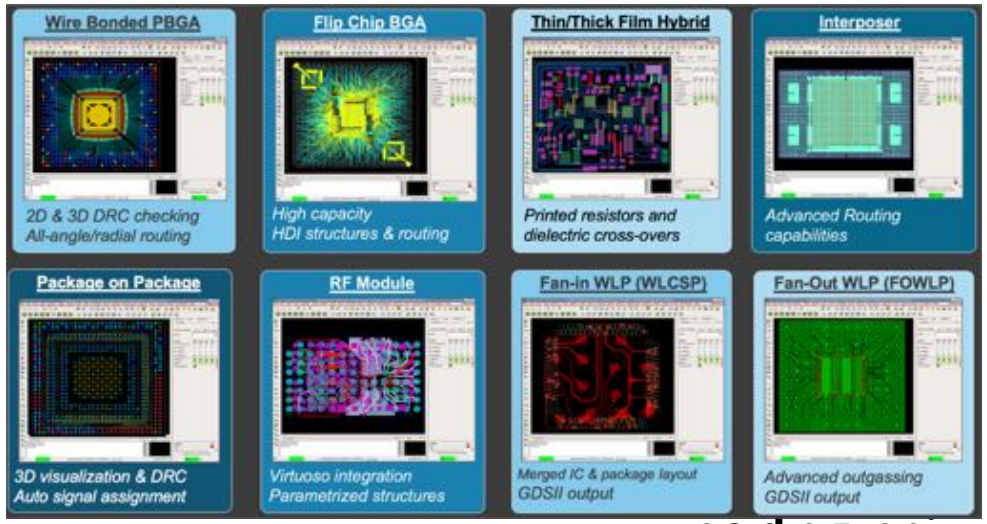
Smart EM Integration
Layout conditioning, Extraction, EM Analysis, back-annotation & simulate using **Virtuoso ADE**



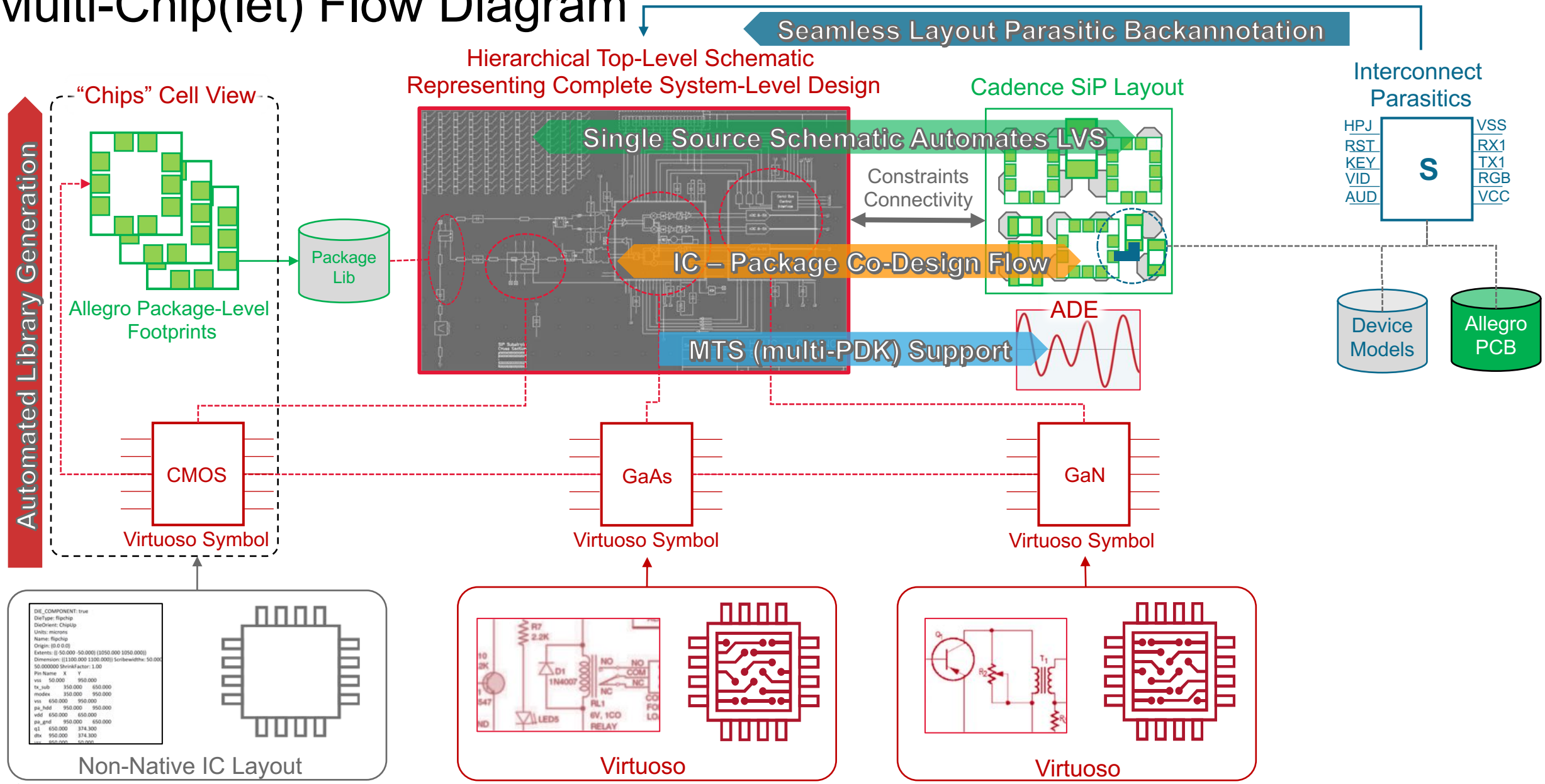
Multi-Chip(let) Capabilities of (Allegro®) Cadence SiP Layout

- Architected as a package/module design solution
  - Correct-by-construction with real-time DRC
  - Support for all chip(let) attach methods
    - Bond wire, flip-chip, stacking, embedded, etc.
  - Incredibly flexible connectivity use model
    - Schematic and/or table and/or spreadsheet
    - Connectivity on-the-fly
  - Technology file-driven package substrate style stack-up
    - Unlimited substrate material types
      - Laminates, Ceramics, Glass, Flex, etc.
  - Advanced package-specific push/shove and automatic routing styles
    - Radial, all angle, flip-chip
  - Package-specific manufacturing outputs
    - BGA ball-maps, bond wire diagrams
  - Integration with IC-level DRC, LVS and metal fill tools
  - PCB and IC manufacturing outputs
    - IPC-2581, Gerber, GDSII, etc.



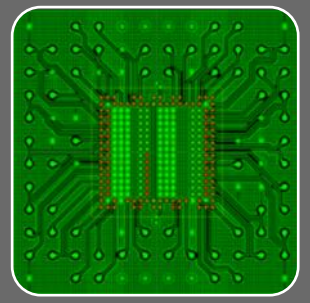


Multi-Chip(let) Flow Diagram



Summary

Cadence Cross-Platform Solutions for Advanced Packaging

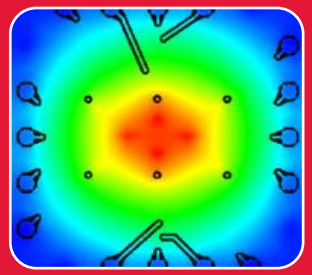


Complete Implementation Platforms

Support flexible entry point and seamless cross-platform co-design

Allegro®, Innovus™, and Virtuoso® technologies Each platform has unique and dedicated functionality and cross-platform capability for multi-chip(let) advanced packaging

Early-stage system-level exploration and top-level connectivity management with OrbitIO™



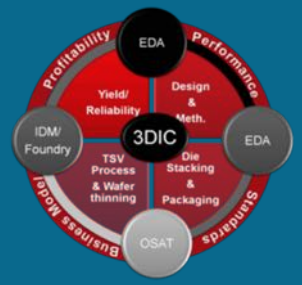
Robust Signoff Capabilities

Modus™ DFT and ATPG for 3D IC

Voltus™/Tempus™/Quantus™ digital analysis tools

Sigrity and Voltus for chip/package thermal analysis
Sigrity™ 3D EM Extraction, SI, and PI provides system-level analysis

PVS/Pegasus™ for LVS, DRC and metal-fill



Ecosystem Partnership and Real Tape-out Experiences

Cadence has been working with ecosystem partners since 2007 on 3D IC

Over 10 test chips completed and multiple production chip tape-outs

Several ongoing projects