# Modern Design Methodologies for Next-Gen Multi-Chip(let) Packaging

John Park

Product Management Director – IC Packaging & Cross-Platform Solutions

### cādence<sup>®</sup>

#### Outline

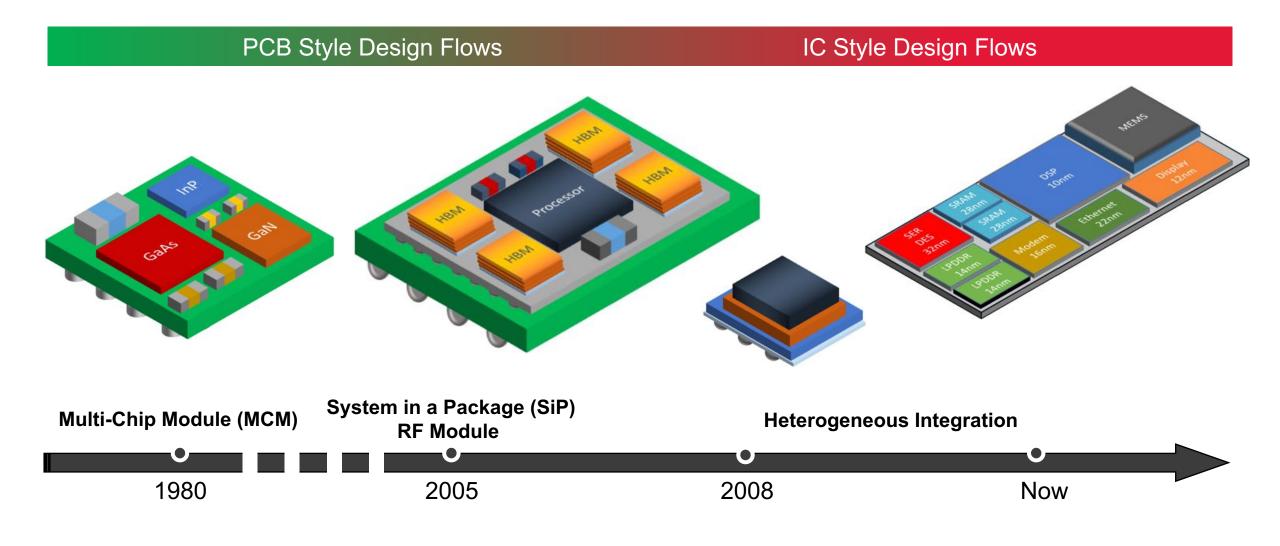
Advanced Multi-Chip(let) Packaging Technology Trends

The Big Picture: Cadence Multi-Chip(let) Advanced Packaging

Example: Multi-Chip(let) Flow



#### The Evolution of Multi-Chip(let) Packaging...Heterogenous Integration



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## The Next Packaging Paradigm Change is Here...

Mechanical Design Tools	PCB-Like Design Flows	Hybrid Design Flows	IC-Like Design Flows			
Mechanical Leadframe	Routable Substrates Organic & Ceramic	2.5D-IC/Silicon Interposer, Embedded Bridges & FOWLP	3D-IC			
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### More Than Moore...What Does It Mean?

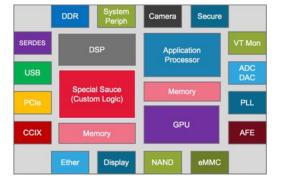
 Three major paradigm shifts changing the dynamics of the advanced packaging industry

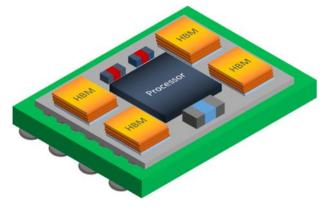
#### 1) Heterogenous integration

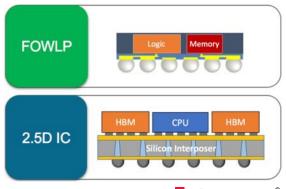
- New methods (chiplets) for SoC logical partitioning
- SiP becoming the new SoC?
- 2) TSVs and FOWLP driving more silicon content in packages

– 2.5D/3D IC wafer and chip stacking technologies

- 3) Semiconductor foundries offering advanced packaging solutions
  - Cadence continues to work with major semiconductor foundries and OSATs to develop advanced packaging certified reference flows



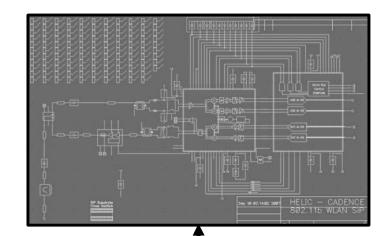


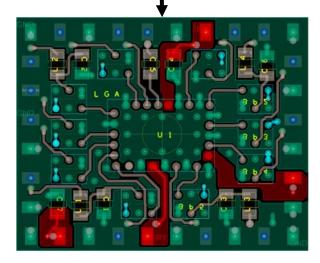


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#### Design Tool/Flow Challenges for Next-Gen Heterogeneously Integrated Designs...Is It a Chip or a Package or a PCB?

- Packaging technology silicon interposer, thin-film laminate, FOWLP – play an important role in determining the right tools/flow
  - Cross-domain planning and optimization (path finding)
    - How do you determine then optimize the right system-level solution?
  - What is the "right" level of chip(let) abstraction/representation in layout?
    - Simple (extents & pin locations), Complex (Full chip(let))
  - Connectivity definition
    - Schematic driven? HDL driven? Spreadsheet driven? Mixed?
  - Packages with silicon content require specialized verification steps
    - Layout vs schematic (LVS) connectivity validation
    - Mask-level physical DRC
    - Specialized metal fill and balancing
  - Cross-domain electrical modeling
    - How do you model the coupling effects between domains?
    - Linking different extraction tools for IC, package, and PCB?
  - Multi-PDK netlisting and simulation
    - How to handle namespace conflicts?







#### Outline

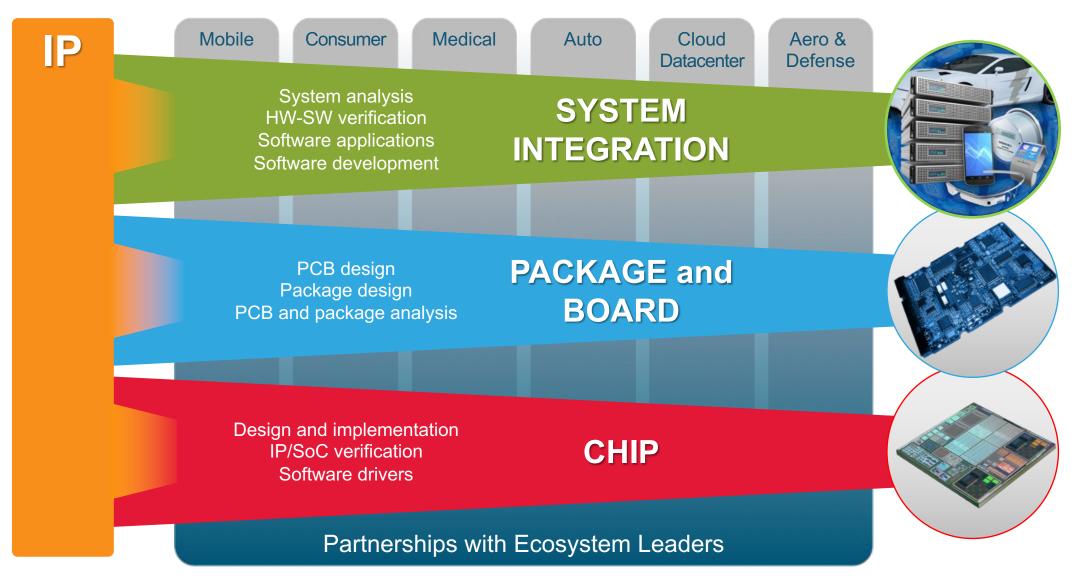
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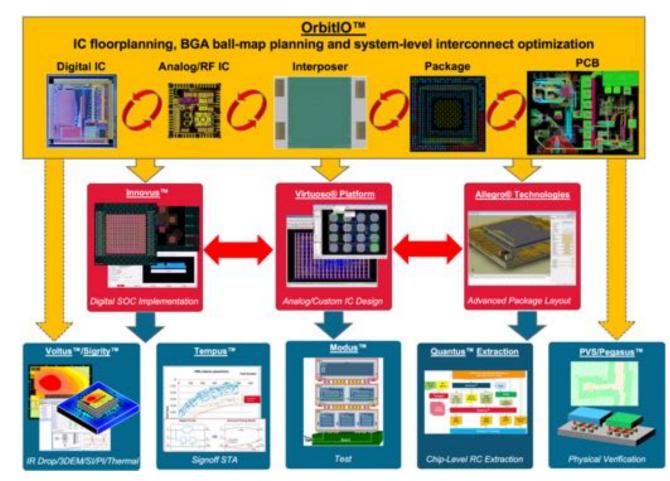
### System Design Enablement (SDE)...Thinking Outside The Chip





### Multi-Chip(let) Packaging – Planning, Implementation and SignOff

- Top-Level cross-domain design management and optimization platform
  - Provides single canvas for planning and optimizing chip(let)s, interposers, packages and boards
  - Provides top-level data to aggregate complete design for signoff
    - Cross-domain connectivity
    - Chip(let) orientation
- Signoff and Test tools Sigrity/Voltus, Quantus, PVS, Tempus, Xcelium and Modus – all support multi-chip(let) design
  - 3DEM/EM-IR/Thermal, RC extraction, physical DRC/LVS, STA, EM/IR, functional sim and test
- Cross-platform flows developed to streamline the interaction between IC, package and PCB design





### Cadence-Wide Solutions for Next-Gen IC Packaging

- All three Cadence implementation platforms have been enabled to support next-gen advanced IC packaging
  - Multi-chip, TSV, MB, chip tiering aware
  - Usually flow type (digital IC, analog IC or core adv. packaging), routing style and manufacturing outputs determine platform of choice
  - Capacity often a driving factor
  - Two or more platforms may be required to create optimal design

ering aware	OrbitIO™ Top-Level Connectivity Optimization and Management					
	Allegro <sup>®</sup> Technologies		Virtuoso* Platform		Innovus™ Solutions	
Architecture	Advanced IC ( BGA) Package Design		Analog/Custom IC Design Platform		Full RTL to GDS Digital SOC Flow	
Substrate/Package Type	Organic, Silicon, ABF, PoP, FOWLP, 2.5D/3D IC	٠	Organic, Silicon (Active & Passive), 2.5D/3D IC		Silicon (Passive & Active) 2.5D/3D IC	
Routing Styles	Constraint driven 45 degree (auto & interactive) PTH & via cuts	<b>NP/XDAOA</b>	PDK driven, Litho correct, 45 & 90 degree routing	Access/XDA	Litho correct, timing driven routing, plus 45 degree RDL routing	
Capacity	100,000s	NSI	1,000,000s	Open	1,000,000,000s	
Parasitic Extraction	Sigrity 3D EM	¢	Quantus & Sigrity	¢	Quantus Extraction	
Manufacturing Output	IPC2581, Gerber & GDSII		GDSII, OASIS		GDSII, OASIS	
Physical Verification			PVS/Pegasus™			

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**Related Projects** 

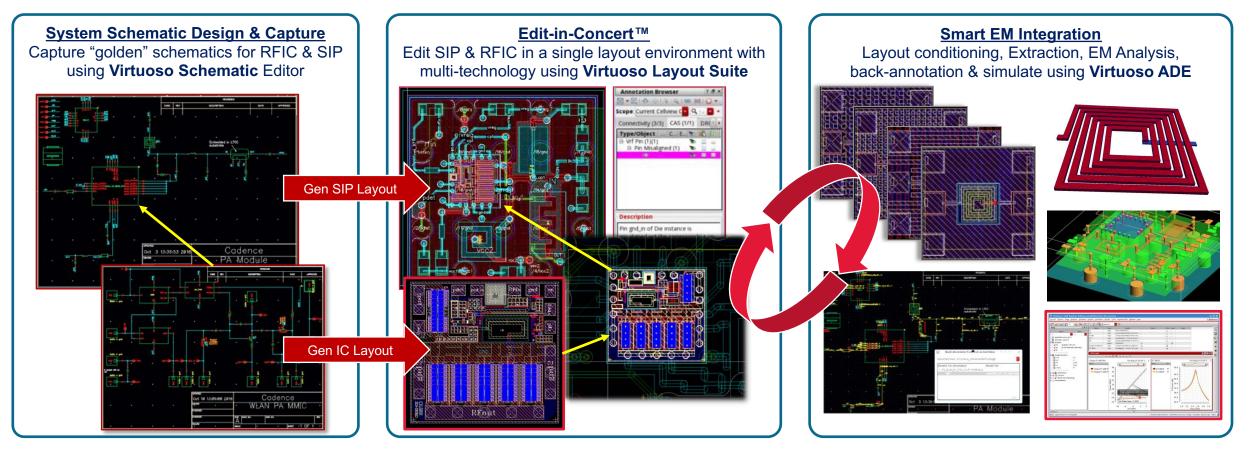




#### Virtuoso<sup>®</sup> System Design Platform Extending IC design into multi-chip(let) system-level design of the YEAH AWARD Virtuoso<sup>®</sup> and Spectre<sup>®</sup> Solutions (Cross-Platform Planning and Optimization) $\overline{O}$ (Schematic, Layout, ADE, and Simulation) Sigrity (3D System Virtuoso System Design Platform OrbitIO<sup>™</sup> ΕM, M, SI, and PI) Package Design Cadence<sup>®</sup> SiP (Advanced IC Package/Module Design) ies Allegro<sup>®</sup> PCB PCB (Analog, RF, and Digital PCB Design)

### Virtuoso® for Intelligent System Design

- Cross-platform solution that integrates Virtuoso, Allegro and Sigrity technologies
- Industries first multi-chip(let) (multi-PDK) solution that provides system-level connectivity validation, automated layout parasitic feedback loop and true concurrent chip/package co-design

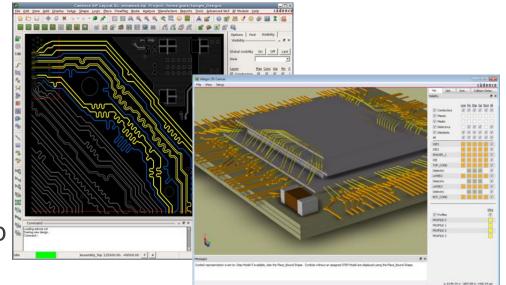


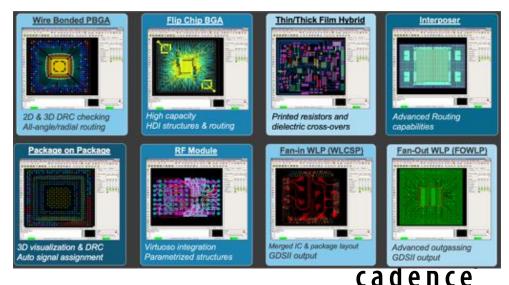
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### Multi-Chip(let) Capabilities of (Allegro®) Cadence SiP Layout

#### Architected as a package/module design solution

- Correct-by-construction with real-time DRC
- Support for all chip(let) attach methods
  - Bond wire, flip-chip, stacking, embedded, etc.
- Incredibly flexible connectivity use model
  - Schematic and/or table and/or spreadsheet
  - Connectivity on-the-fly
- Technology file-driven package substrate style stack-up
  - Unlimited substrate material types
    - Laminates, Ceramics, Glass, Flex, etc.
- Advanced package-specific push/shove and automatic routing styles
  - Radial, all angle, flip-chip
- Package-specific manufacturing outputs
  - BGA ball-maps, bond wire diagrams
- Integration with IC-level DRC, LVS and metal fill tools
- PCB and IC manufacturing outputs
  - IPC-2581, Gerber, GDSII, etc.





#### Multi-Chip(let) Flow Diagram Seamless Layout Parasitic Backannotation **Hierarchical Top-Level Schematic** Interconnect **Representing Complete System-Level Design** Cadence SiP Layout -"Chips" Cell View--**Parasitics** VSS HPJ Single Source Schematic Automates LVS RX1 RST eneration **KEY** <u>TX1</u> S Constraints RGB VID VCC Connectivity AUD IC – Package Co-Design Flow Package 3 Lib ibrary Allegro Package-Level ADE Allegro Device **Footprints** MTS (multi-PDK) Support PCB **Models** Automated **CMOS** GaN GaAs Virtuoso Symbol Virtuoso Symbol Virtuoso Symbol пппп пппп пппп Orient: ChipU Nts: micror ma finch rigin: (0.00 nts: (1-50.000 -50.000) (1050.000 105) 6V, 1CO Non-Native IC Layout Virtuoso Virtuoso

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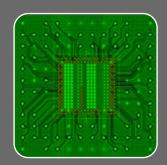
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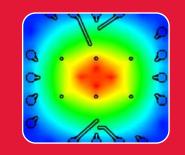


#### Cadence Cross-Platform Solutions for Advanced Packaging



#### Complete Implementation Platforms Support flexible entry point and seamless cross-platform co-design

Allegro<sup>®</sup>, Innovus<sup>™</sup>, and Virtuoso<sup>®</sup> technologies Each platform has unique and dedicated functionality and cross-platform capability for multi-chip(let) advanced packaging Early-stage system-level exploration and top-level connectivity management with OrbitIO<sup>™</sup>



#### **Robust Signoff Capabilities**

Modus<sup>™</sup> DFT and ATPG for 3D IC Voltus<sup>™</sup>/Tempus<sup>™</sup>/Quantus<sup>™</sup> digital analysis tools Sigrity and Voltus for chip/package thermal analysis Sigrity<sup>™</sup> 3D EM Extraction, SI, and PI provides system-level analysis PVS/Pegasus<sup>™</sup> for LVS, DRC and metal-fill



#### **Ecosystem Partnership and Real Tape-out Experiences**

Cadence has been working with ecosystem partners since 2007 on 3D IC Over 10 test chips completed and multiple production chip tape-outs Several ongoing projects



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