OPEN

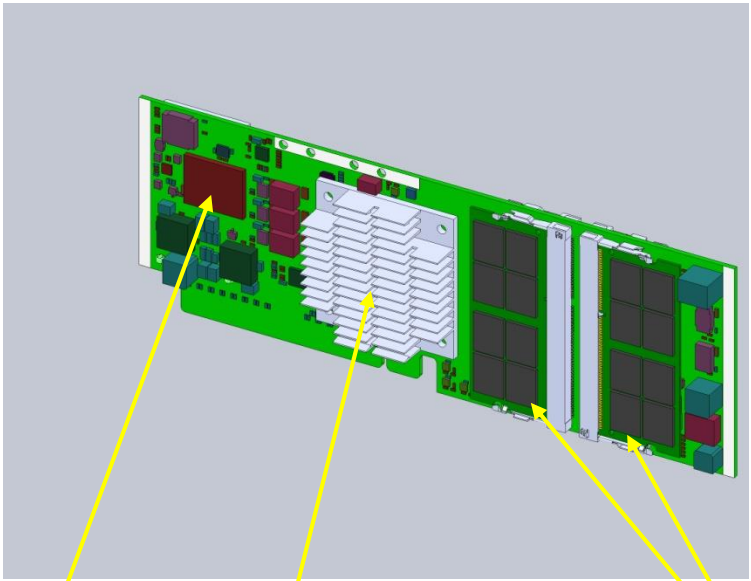
Compute Project

AMD Open CS 1.0

Bob Ogrey

1/29/14

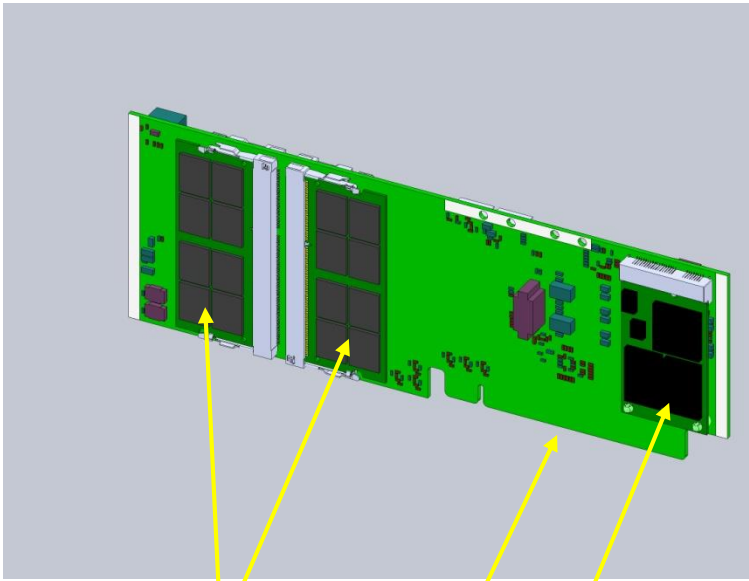
Open CS 1.0 details



iSSD

Seattle Proc with passive Heatsink

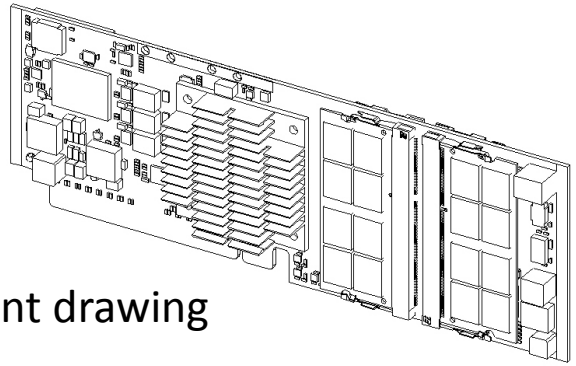
2of 4 ECC SODIMM's
(Front side)



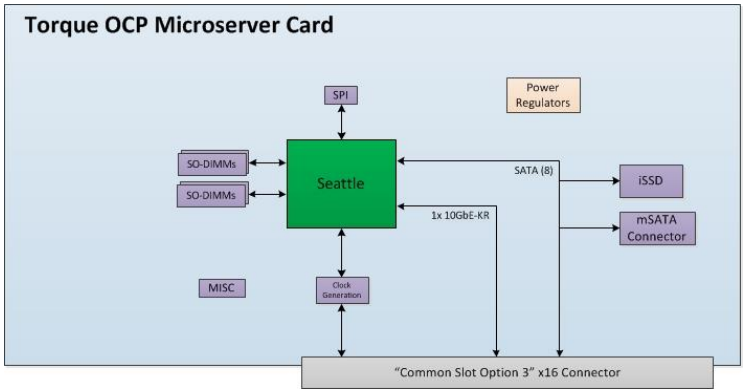
2of 4 ECC SODIMM's
(Back side)

mSATA option

x16 Common slot interface



Placement drawing



Option 3 pinout from ver 0.7 Spec

Option 3: 6x SATA + 1x 10GbE			
Pin Name	Side B	Side A	Pin Name
P12V	1	1	PRSNT#
P12V	2	2	P12V
P12V	3	3	P12V
GND	4	4	GND
I2C_SCL	5	5	SVR_ID0
I2C_SDA	6	6	SVR_ID1
GND	7	7	COM_TX
PWR_BTN#	8	8	COM_RX
USB_P	9	9	SVR_ID2
USB_N	10	10	SVR_ID3
SYS_RESET#	11	11	Reserved
I2C_ALERT#	12	12	GND
GND	13	13	RSVD
GND	14	14	RSVD
SATA5_TX_P	15	15	GND
SATA5_TX_N	16	16	GND
GND	17	17	SATA5_RX_P
GND	18	18	SATA5_RX_N
SATA4_TX_P	19	19	GND
SATA4_TX_N	20	20	GND
GND	21	21	SATA4_RX_P
GND	22	22	SATA4_RX_N
SATA3_TX_P	23	23	GND
SATA3_TX_N	24	24	GND
GND	25	25	SATA3_RX_P
GND	26	26	SATA3_RX_N
SATA2_TX_P	27	27	GND
SATA2_TX_N	28	28	GND
GND	29	29	SATA2_RX_P
GND	30	30	SATA2_RX_N
SATA1_TX_P	31	31	GND

OPEN

SATA1_TX_N	32	32	GND
GND	33	33	SATA1_RX_P
GND	34	34	SATA1_RX_N
SATA0_TX_P	35	35	GND
SATA0_TX_N	36	36	GND
GND	37	37	SATA0_RX_P
GND	38	38	SATA0_RX_N
RFU	39	39	GND
RFU	40	40	GND
GND	41	41	RFU
GND	42	42	NIC_SMBUS_ALERT#
NIC_SMBUS_SCL	43	43	GND
NIC_SMBUS_SDA	44	44	GND
GND	45	45	GE0_RX_P
GND	46	46	GE0_RX_N
GE0_TX_P	47	47	GND
GE0_TX_N	48	48	GND
GND	49	49	RFU

Figure 6-8 Pin Assignment Option 3, which Provides SATA and Ethernet Ports

- Spec to be submitted to Incubation committee in the March timeframe
- Will contribute schematics and gerbers

Board Shots