

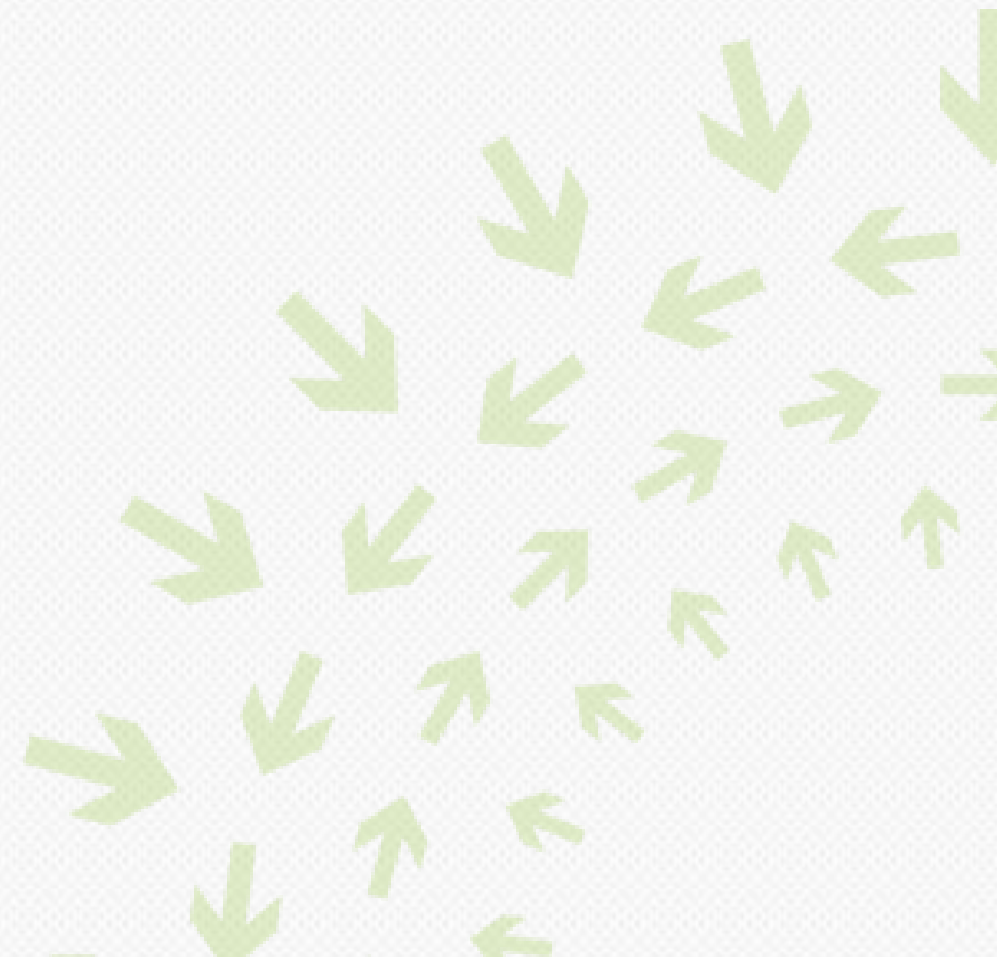


OCP Mezzanine Card Update

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Compute Server Design



Agenda

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Overview – Where we are now

- 10G NIC Mezzanine Card widely available
 - Mellanox ConnectX-3
 - Intel 82599
 - Others
- Specification 1.0
 - Common Form Factor
 - I2C sideband connection between NIC and BMC
 - PCIe x8 defined in connector
 - 8mm stacking height is considered
 - 2x SFP+ ports



Enhancement – RMII support

- **I2C Sideband Limitation**

- Low speed as 100Kbps, with low throughput
- Challenges for features as firmware update by OOB

- **New 10G Mezzanine Card with RMII**

- **Backward compatible**

- Use RSVD pins in current 10G Mezzanine Card

- **Requirement for New/Refreshed 10G Mezzanine Card**

- Support both I2C and RMII as sideband channels, select/enable by BMC

- **Requirement for Management Controller**

- Support both I2C and RMII as sideband channels, discover RMII support first, then fall back to I2C



Enhancement – RMII support

Pin Changes

Pin	Current 10G Mezz	New with RMII
14	RSVD(MEZZ_CPRSNT1_N)	NCSI_RCSDV
15	RSVD(MEZZ_CPRSNT2_N)	NCSI_RCLK
16	RSVD (SSD_PRSNT_N)	NCSI_TXEN
22	RSVD (SATA_RX+)	NCSI_RXD0
23	RSVD (SATA_RX-)	NCSI_RXD1
78	RSVD (DA_DSS)	NCSI_RXER
80	RSVD (SATA_TX+)	NCSI_TXD0
81	RSVD (SATA_TX-)	NCSI_TXD1



Plan for Next – 2.0

Features in Consideration

- QSFP+ port support
- Wider high speed bus to host, such as PCIe x16
- Flexible stacking height choices and placement guidance
 - High chip power needs extra space for Heatsink



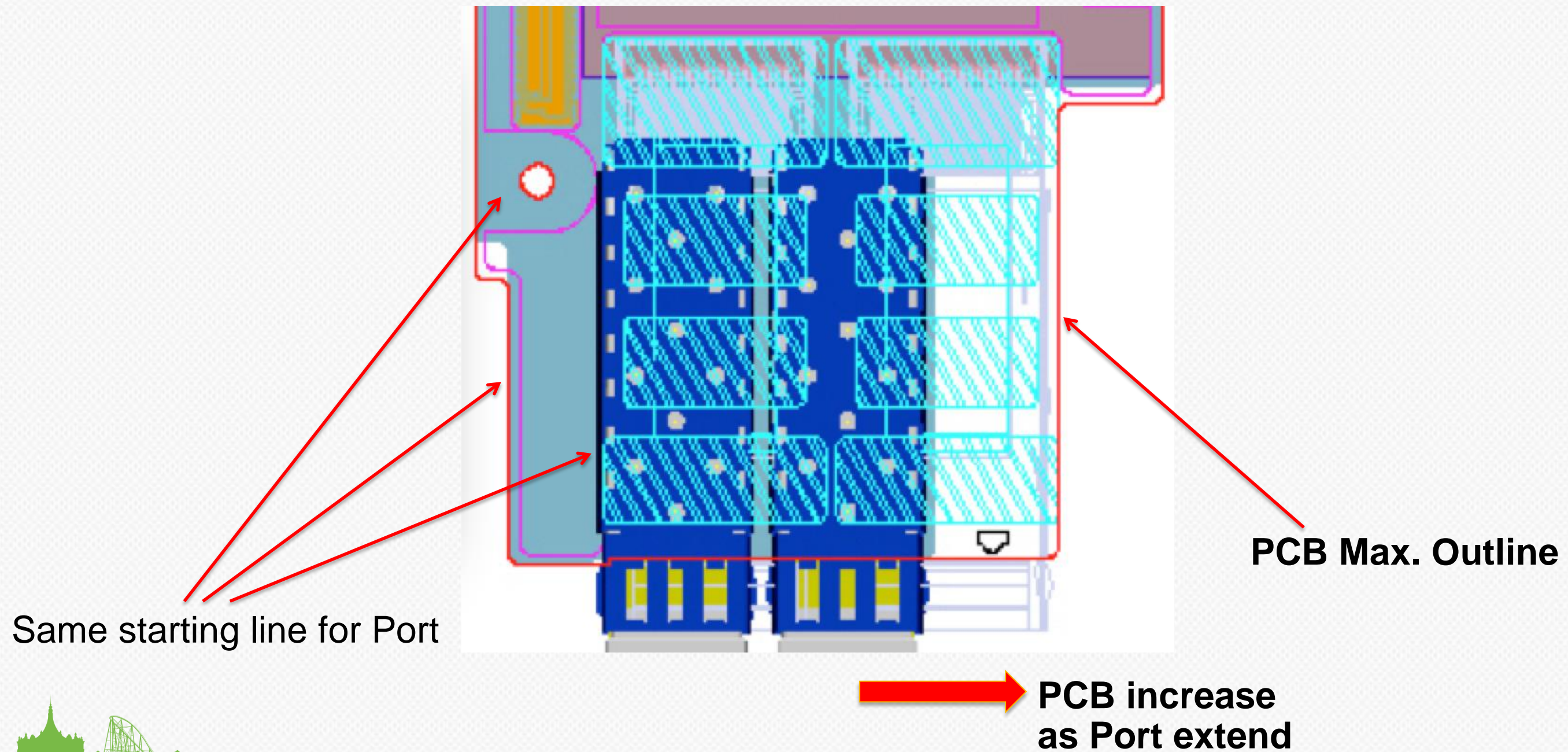
2.0 – QSFP+

- **2x QSFP+ ports with Port 0 required**
 - PCB maximum outline on I/O portion, to accommodate up to 2x QSFP+ ports
 - For Single QSFP+ Port implementation, only Port 0 is required, so extra PCB space is available for design solution
- **Server Design Compatibility Consideration**
 - **Facebook Server Motherboard Spec 2.0**
 - No plan for support
 - It is possible to use taller Mezzanine connector on MB side
 - **Facebook Server Motherboard Spec 3.0**
 - MB PCB has additional cut-out to accommodate QSFP+, to maintain same stacking height as SFP+ version



2.0 – QSFP+

I/O Comparison between 1.0 and 2.0



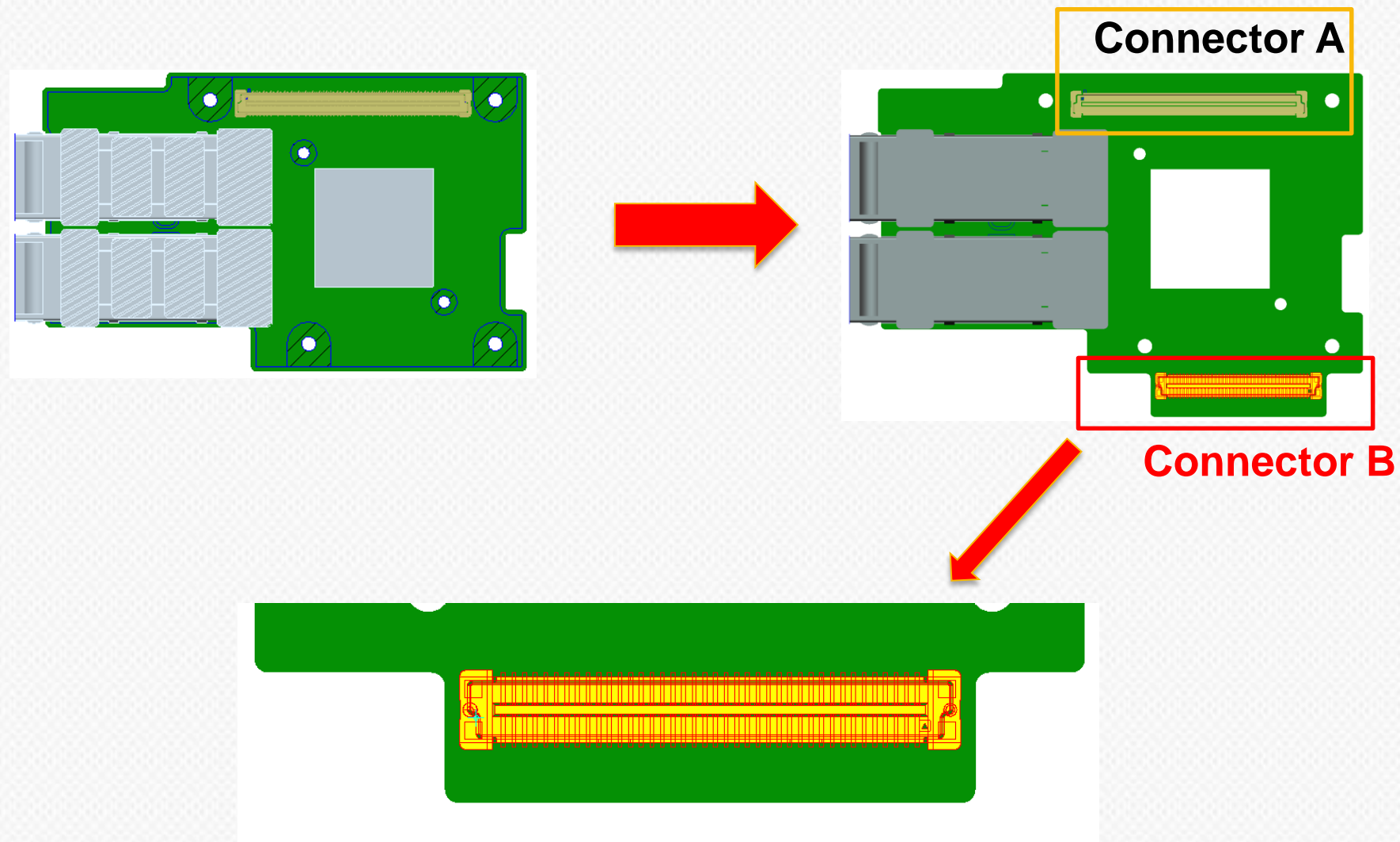
2.0 – PCIe x16

- **Add Connector B for additional PCIe x8**
 - Current Mezzanine connector is referred as Connector A
 - Connector B is optional, together with PCB extension for it.
- **Compatibility Consideration**
 - Same mounting hole and Connector A location as 10G Mezzanine Card, best effort for backward compatibility
 - Card supporting PCIe x16 can DEPOP connector B and be installed on MB which only supports Connector A
 - Current 10G Mezzanine Card can fit into MB which supports both Connector A and B



2.0 – PCIe x16

Connector B Location



2.0 – PCIe x16

- **Pin Definitions**

- **Connector B**

- 2x pins for P12V_AUX
- 8x TX/RX pairs for x8 PCIe
- 1x pairs for Mezz present detection
- 2x pairs of 100MHz Clock

- **Connector A**

- Same as 10G Mezz with RMII support



2.0 – Summary

Status on NIC Mezzanine Card SKUs

	I/O Port	Connector A	Connector B	Vendors
10G Mezz. Card (Today)	SFP+, Single/Dual ports	Yes	No	Mellanox ConnectX-3 Intel 82599 Others
10G Mezz. Card (RMII)	SFP+, Single/Dual ports	Yes	No	Mellanox ConnectX-3 (sample) Intel 82599 (sample)
40G Mezz. Card (RMII)	QSFP+, Single/Dual ports	Yes	No	Mellanox ConnectX-3 pro (sample)
Others?				

2.0 Spec is still working in progress



Q & A



