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Compute Summit

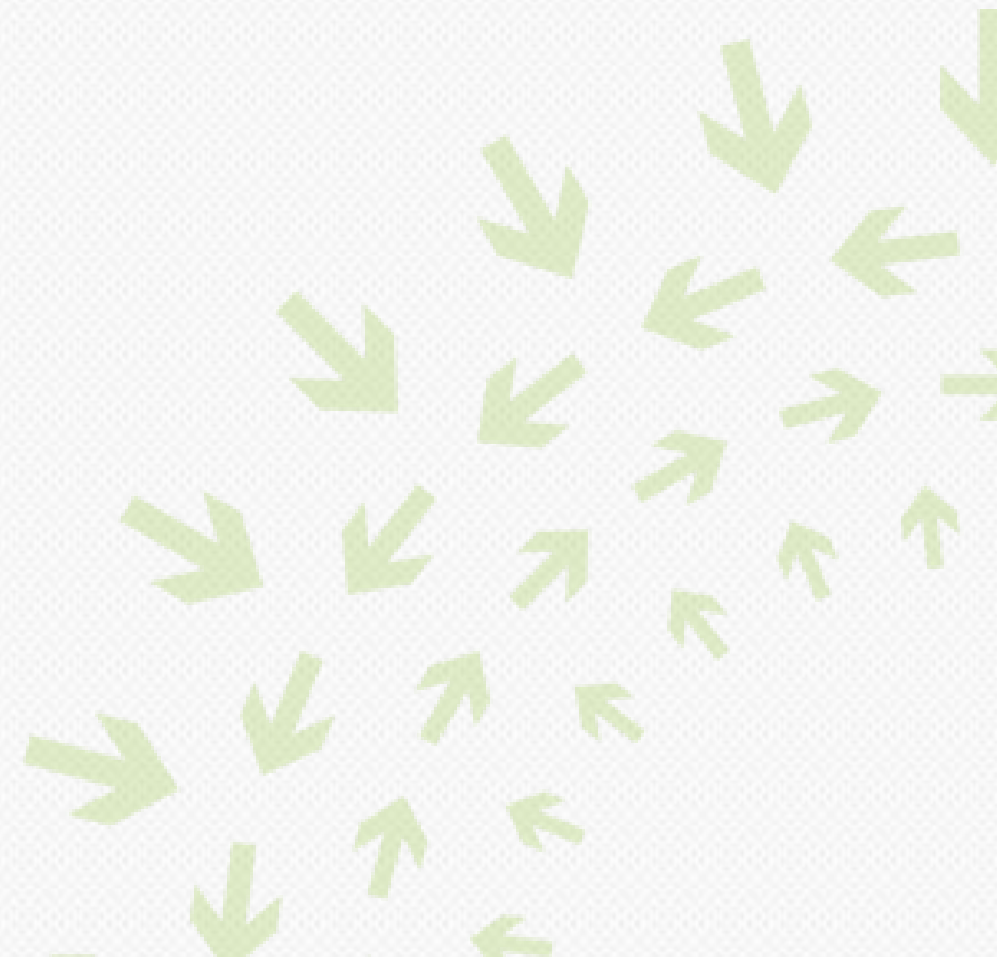
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Santa Clara



Micro-server spec update

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Agenda

- 1 Overview
- 2 x16 Mechanical details
- 3 x8 pin-out updates
- 4 x16 pin-out updates
- 5 Other updates
- 8 Q&A

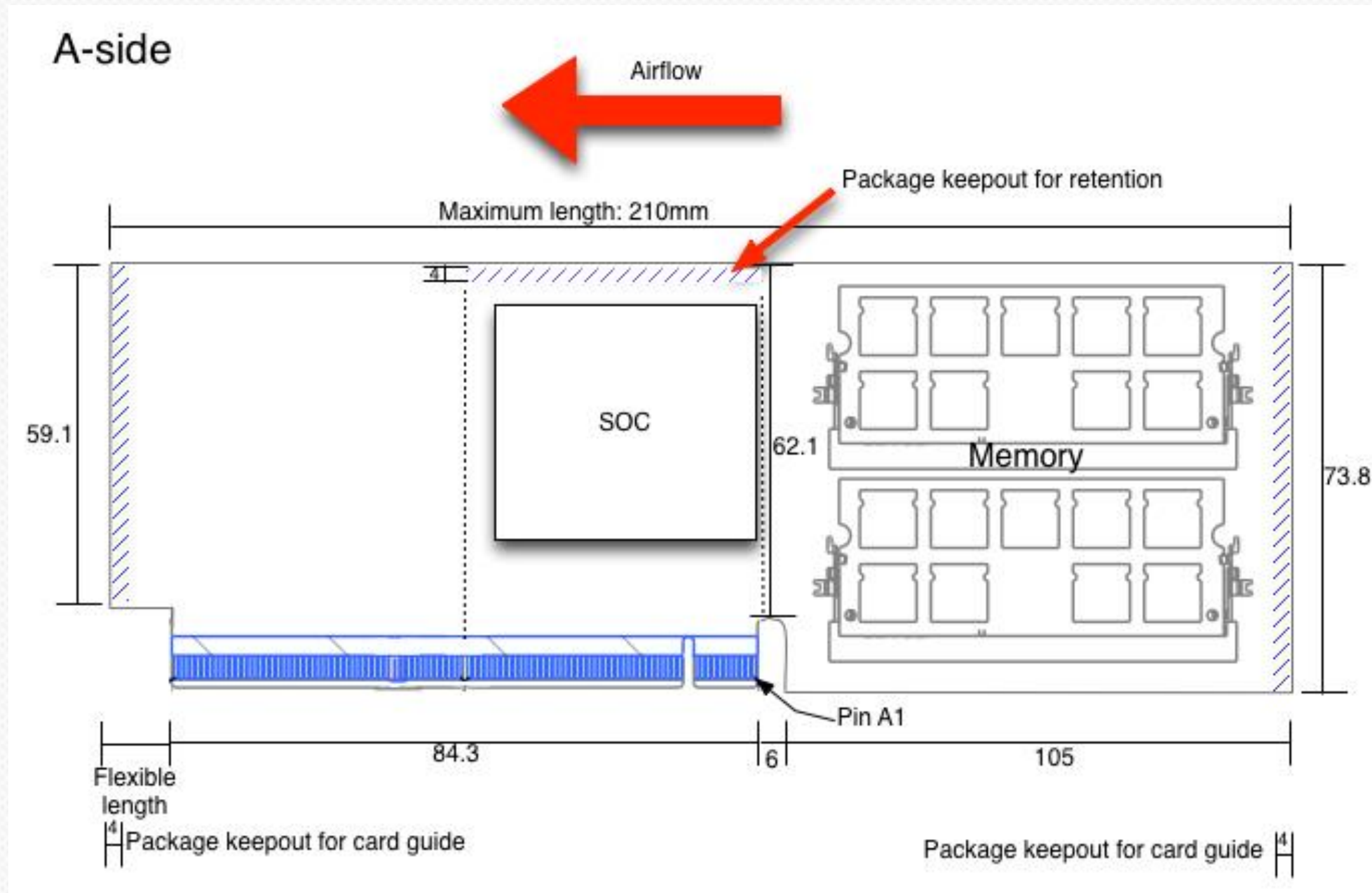


Micro-server spec updated to version 0.7

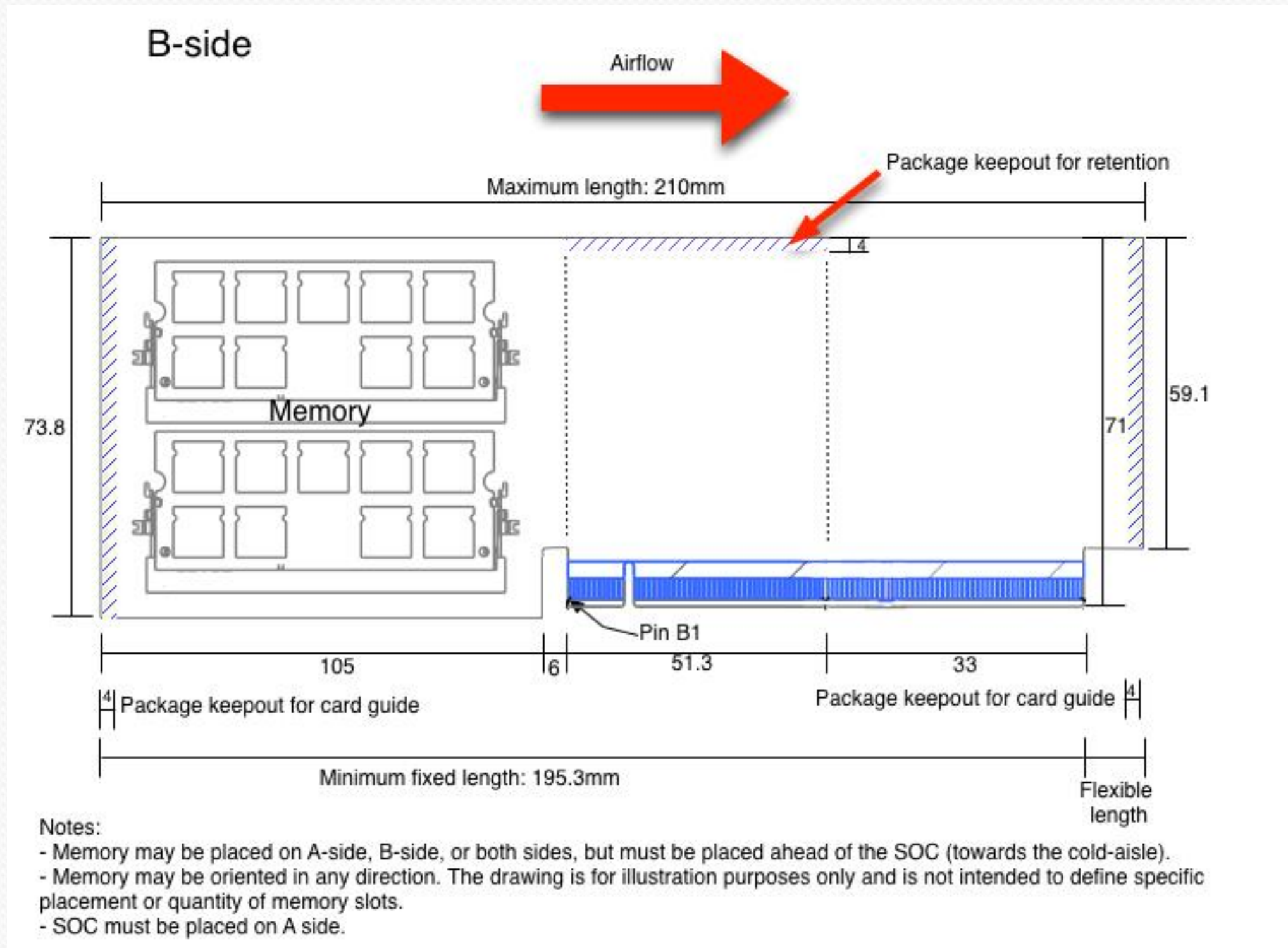
- Mechanical updates
 - Added additional retention keep-outs
 - Decreased card pitch
- Added x16 pin-out and form factor
- Added NIC SMBUS connection
- Misc. updates



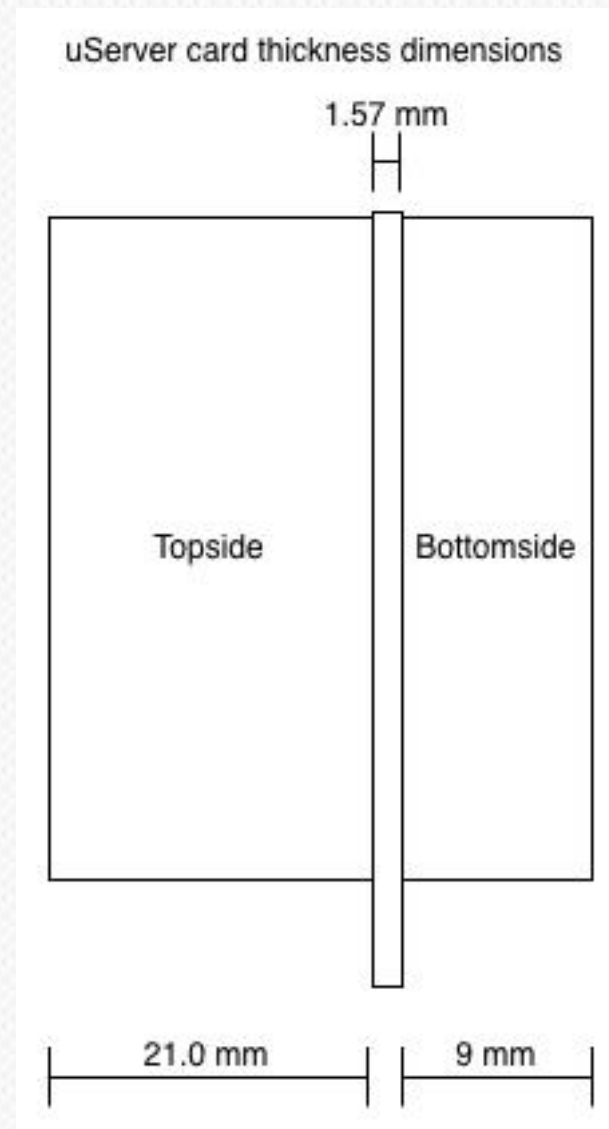
Micro-server mechanical details



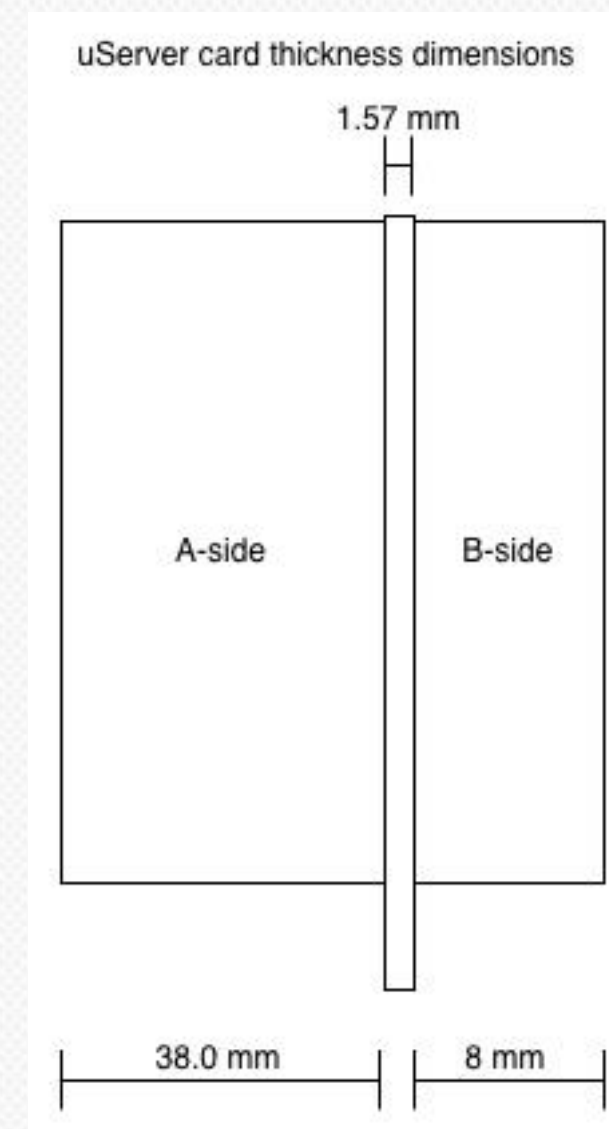
Micro-server mechanical details



Micro-server mechanical details



Single-width



Double-width



Micro-server updated x8 connector pin-out

Pin Name	Side B	Side A	Pin Name
P12V	1	1	PRSNT#
P12V	2	2	P12V
P12V	3	3	P12V
GND	4	4	GND
I2C_SCL	5	5	SVR_ID0
I2C_DATA	6	6	SVR_ID1
GND	7	7	COM_TX
PWR_BTN#	8	8	COM_RX
USB_P	9	9	SVR_ID2
USB_N	10	10	SVR_ID3
SYS_RESET#	11	11	PCIE_RESET#
I2C_ALERT#	12	12	GND
GND	13	13	PCIE_REFCLK_P
GND	14	14	PCIE_REFCLK_N
PCIE_TX0_P	15	15	GND
PCIE_TX0_N	16	16	GND
GND	17	17	PCIE_RX0_P
GND	18	18	PCIE_RX0_N
PCIE_TX1_P	19	19	GND
PCIE_TX1_N	20	20	GND
GND	21	21	PCIE_RX1_P
GND	22	22	PCIE_RX1_N
PCIE_TX2_P	23	23	GND
PCIE_TX2_N	24	24	GND
GND	25	25	PCIE_RX2_P
GND	26	26	PCIE_RX2_N
PCIE_TX3_P	27	27	GND
PCIE_TX3_N	28	28	GND
GND	29	29	PCIE_RX3_P
GND	30	30	PCIE_RX3_N
SATAo_TX_P	31	31	GND
SATAo_TX_N	32	32	GND
GND	33	33	SATAo_RX_P
GND	34	34	SATAo_RX_N
RSVD	35	35	GND
RSVD	36	36	GND
GND	37	37	RSVD
GND	38	38	RSVD
RFU	39	39	GND
RFU	40	40	GND
GND	41	41	RSVD
GND	42	42	NIC_SMBUS_ALERT#
NIC_SMBUS_SCL	43	43	GND
NIC_SMBUS_SDA	44	44	GND
GND	45	45	GEo_RX_P
GND	46	46	GEo_RX_N
GEo_TX_P	47	47	GND
GEo_TX_N	48	48	GND
GND	49	49	RFU

Required connection
Configurable connection
Reserved for future use



Micro-server x16 connector pin-out

X8

SATAo_TX_P	31	GND	31
SATAo_TX_N	32	GND	32
GND	33	SATAo_RX_P	33
GND	34	SATAo_RX_N	34
PCIE1_REFCLK_P	35	GND	35
PCIE1_REFCLK_N	36	GND	36
GND	37	PCIE2_REFCLK_P	37
GND	38	PCIE2_REFCLK_N	38
PCIE1_RESET#	39	GND	39
PCIE2_RESET#	40	GND	40
GND	41	RSVD	41
GND	42	NIC_SMBUS_ALERT#	42
NIC_SMBUS_SCL	43	GND	43
NIC_SMBUS_SDA	44	GND	44
GND	45	GEo_RX_P	45
GND	46	GEo_RX_N	46
GEo_TX_P	47	GND	47
GEo_TX_N	48	GND	48
GND	49	PCIE1_RX0_P	49
GND	50	PCIE1_RX0_N	50
PCIE1_TX0_P	51	GND	51
PCIE1_TX0_N	52	GND	52
GND	53	PCIE1_RX1_P	53
GND	54	PCIE1_RX1_N	54
PCIE1_TX1_P	55	GND	55
PCIE1_TX1_N	56	GND	56
GND	57	PCIE1_RX2_P	57
GND	58	PCIE1_RX2_N	58
PCIE1_TX2_P	59	GND	59
PCIE1_TX2_N	60	GND	60
GND	61	PCIE1_RX3_P	61
GND	62	PCIE1_RX3_N	62
PCIE1_TX3_P	63	GND	63
PCIE1_TX3_N	64	GND	64
GND	65	PCIE2_RX0_P	65
GND	66	PCIE2_RX0_N	66
PCIE2_TX0_P	67	GND	67
PCIE2_TX0_N	68	GND	68
GND	69	PCIE2_RX1_P	69
GND	70	PCIE2_RX1_N	70
PCIE2_TX1_P	71	GND	71
PCIE2_TX1_N	72	GND	72
GND	73	PCIE2_RX2_P	73
GND	74	PCIE2_RX2_N	74
PCIE2_TX2_P	75	GND	75
PCIE2_TX2_N	76	GND	76
GND	77	PCIE2_RX3_P	77
GND	78	PCIE2_RX3_N	78
PCIE2_TX3_P	79	GND	79
PCIE2_TX3_N	80	GND	80
GND	81	P12V	81
GND	82	P12V	82

Required connection
Configurable connection
Reserved for future use



Micro-server x8 changes

Added 2nd SMBUS connection

- Provides connection from BMC to an SOC with an integrated NIC
- Enables “shared” BMC connection

Removed 2nd SATA connection

- Changed pins to RSVD to enable x8 cards in x16 slots

GND	33	33	SATAo_RX_P
GND	34	34	SATAo_RX_N
RSVD	35	35	GND
RSVD	36	36	GND
GND	37	37	RSVD
GND	38	38	RSVD
RFU	39	39	GND
RFU	40	40	GND
GND	41	41	RSVD
GND	42	42	NIC_SMBUS_ALERT#
NIC_SMBUS_SCL	43	43	GND
NIC_SMBUS_SDA	44	44	GND
GND	45	45	GEo_RX_P
GND	46	46	GEo_RX_N
GEo_TX_P	47	47	GND
GEo_TX_N	48	48	GND
GND	49	49	RFU

Micro-server x16 additions

More PCIe

- Support for 3x x4 connections (12 lanes total)
- 3x clocks
- 3x resets

GND	34	34	PCIE1_TX0_P
PCIE1_REFCLK_P	35	35	GND
PCIE1_REFCLK_N	36	36	GND
GND	37	37	PCIE2_REFCLK_P
GND	38	38	PCIE2_REFCLK_N
PCIE1_RESET#	39	39	GND
PCIE2_RESET#	40	40	GND
GND	41	41	RSVD

More power pins

- 2x more 12V pins
- Supports up to 80W cards

GND	49	49	PCIE1_RX0_P
GND	50	50	PCIE1_RX0_N
PCIE1_TX0_P	51	51	GND
PCIE1_TX0_N	52	52	GND
GND	53	53	PCIE1_RX1_P
GND	54	54	PCIE1_RX1_N
PCIE1_TX1_P	55	55	GND
PCIE1_TX1_N	56	56	GND
GND	57	57	PCIE1_RX2_P
GND	58	58	PCIE1_RX2_N
PCIE1_TX2_P	59	59	GND
PCIE1_TX2_N	60	60	GND
GND	61	61	PCIE1_RX3_P
GND	62	62	PCIE1_RX3_N
PCIE1_TX3_P	63	63	GND
PCIE1_TX3_N	64	64	GND
GND	65	65	PCIE2_RX0_P
GND	66	66	PCIE2_RX0_N
PCIE2_TX0_P	67	67	GND
PCIE2_TX0_N	68	68	GND
GND	69	69	PCIE2_RX1_P
GND	70	70	PCIE2_RX1_N
PCIE2_TX1_P	71	71	GND
PCIE2_TX1_N	72	72	GND
GND	73	73	PCIE2_RX2_P
GND	74	74	PCIE2_RX2_N
PCIE2_TX2_P	75	75	GND
PCIE2_TX2_N	76	76	GND
GND	77	77	PCIE2_RX3_P
GND	78	78	PCIE2_RX3_N
PCIE2_TX3_P	79	79	GND
PCIE2_TX3_N	80	80	GND
GND	81	81	P12V
GND	82	82	P12V



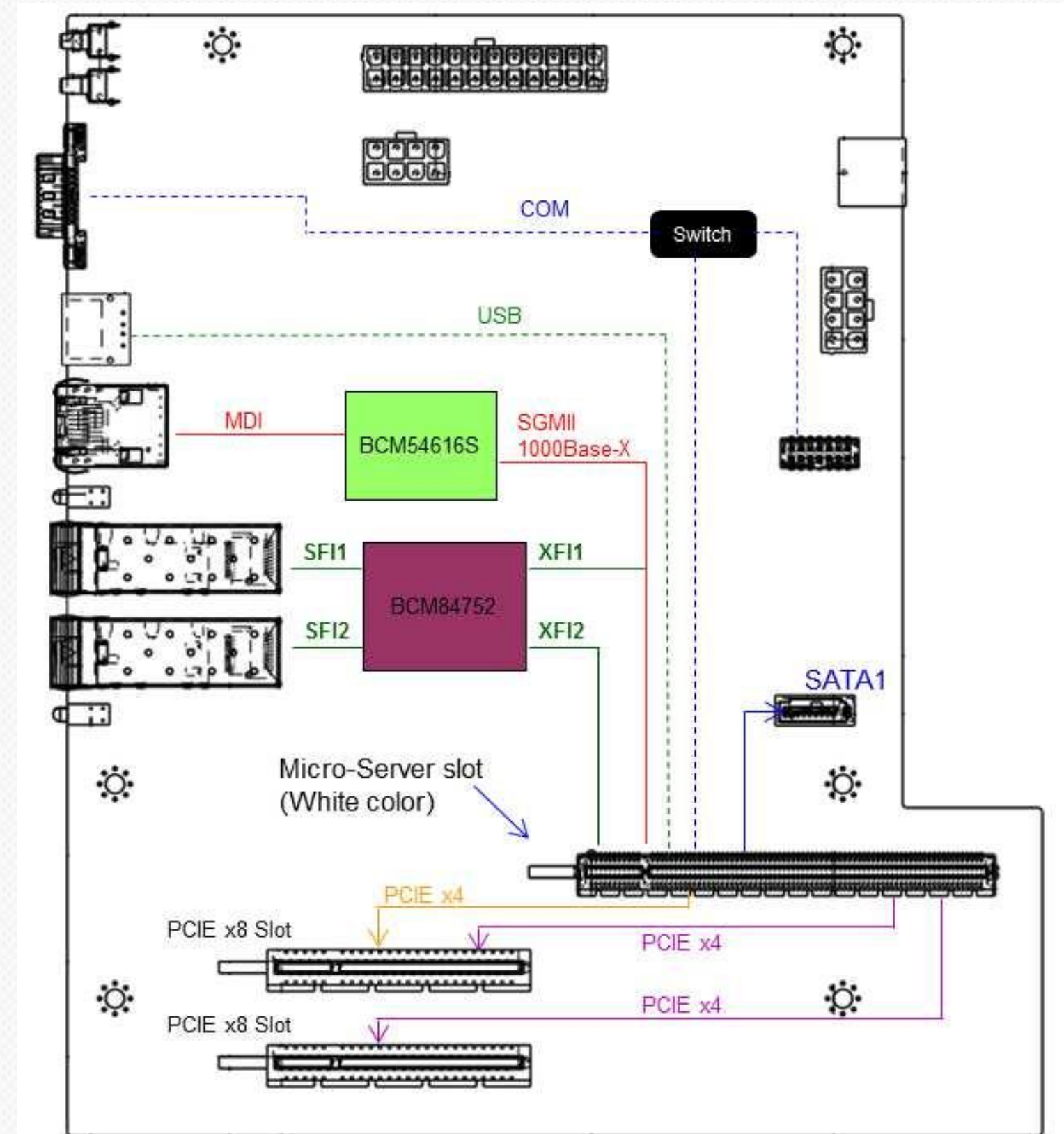
Other updates

- Added requirement for IPv6 support
- Added requirement for UEFI firmware
- Added BIOS ECC error code table
- Removed “Chassis” FRU information



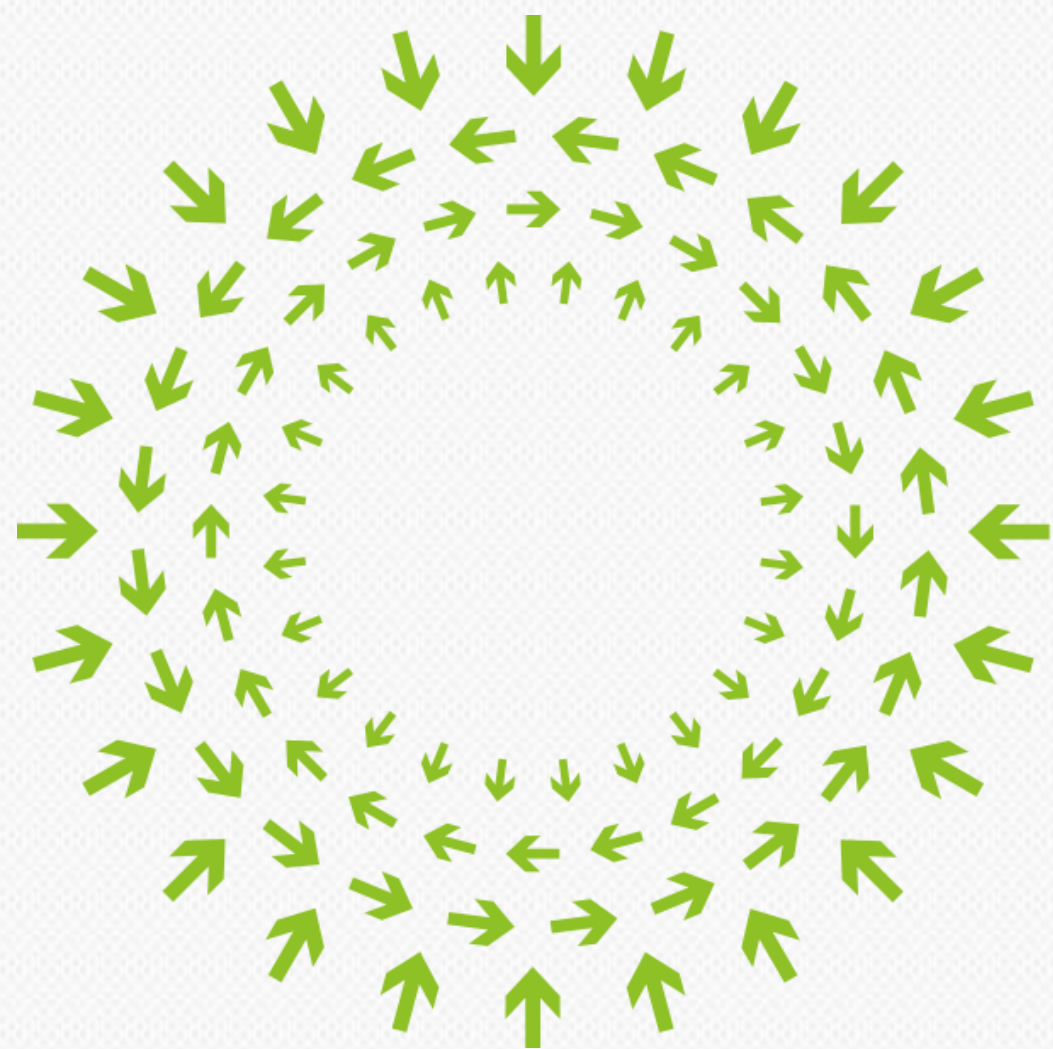
Test system

- Micro-ATX form factor test board is available now



Q & A





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