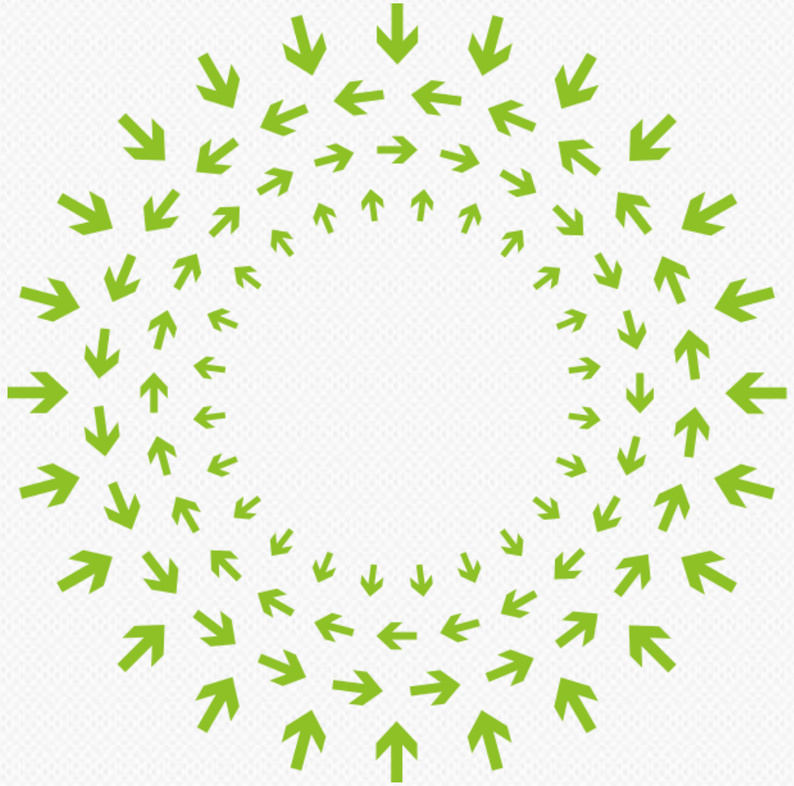


OPEN Compute Summit

January 16-17, 2013

Santa Clara

OPEN
Compute Summit

Micro-server spec update

Chris Petersen
Facebook
Hardware System Engineer

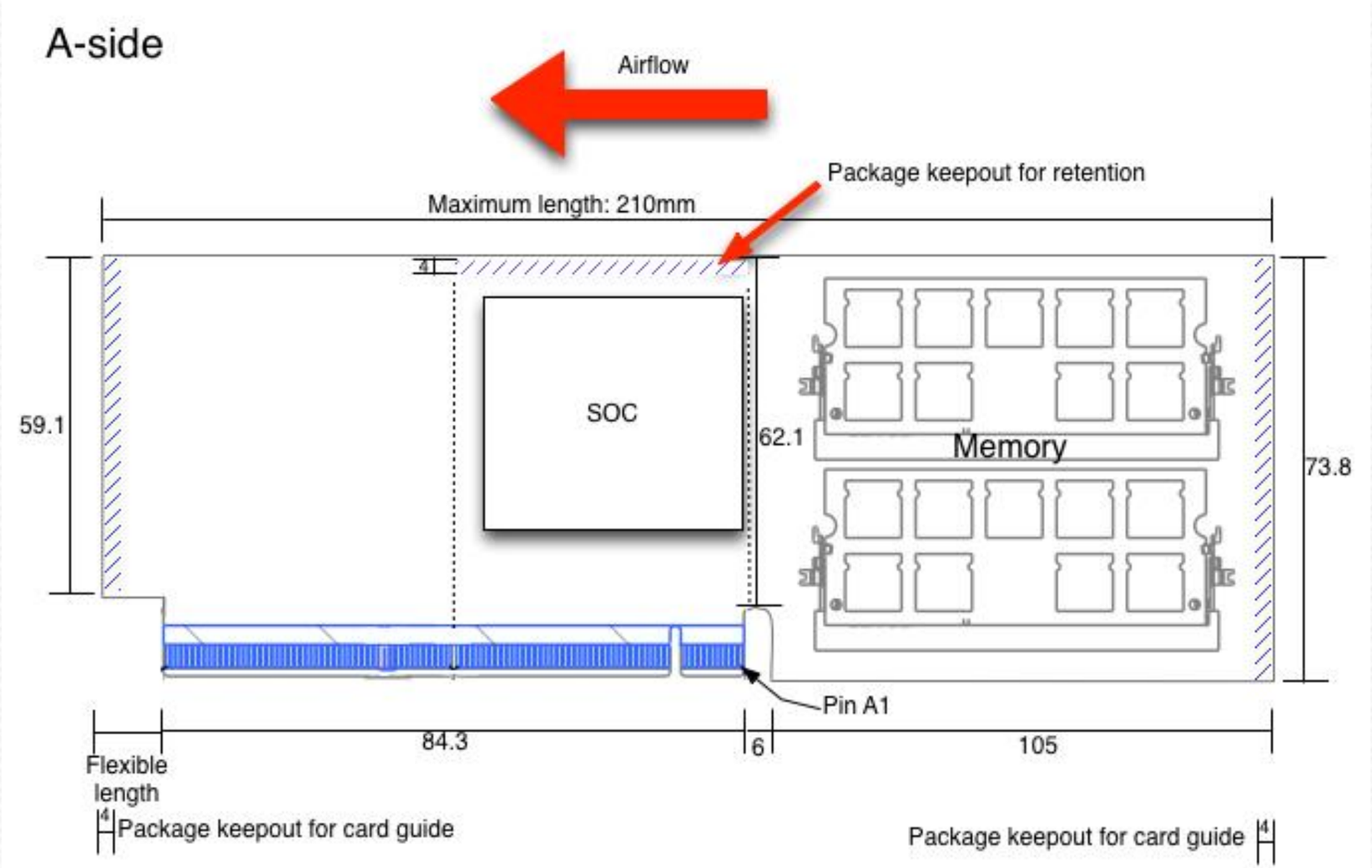
Agenda

1	Overview
2	x16 Mechanical details
3	x8 pin-out updates
4	x16 pin-out updates
5	Other updates
8	Q&A

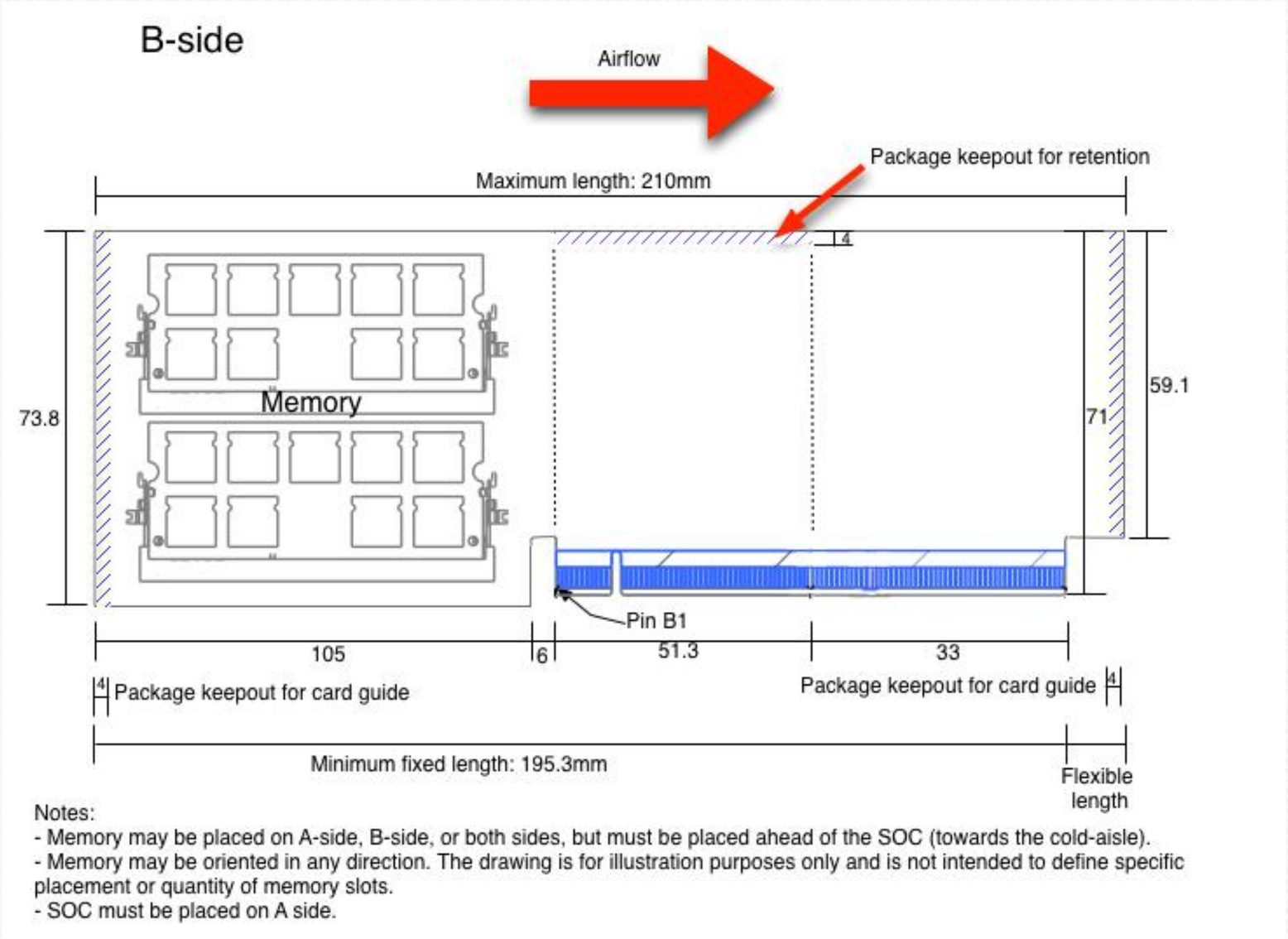
Micro-server spec updated to version 0.7

- Mechanical updates
  - Added additional retention keep-outs
  - Decreased card pitch
- Added x16 pin-out and form factor
- Added NIC SMBUS connection
- Misc. updates

Micro-server mechanical details

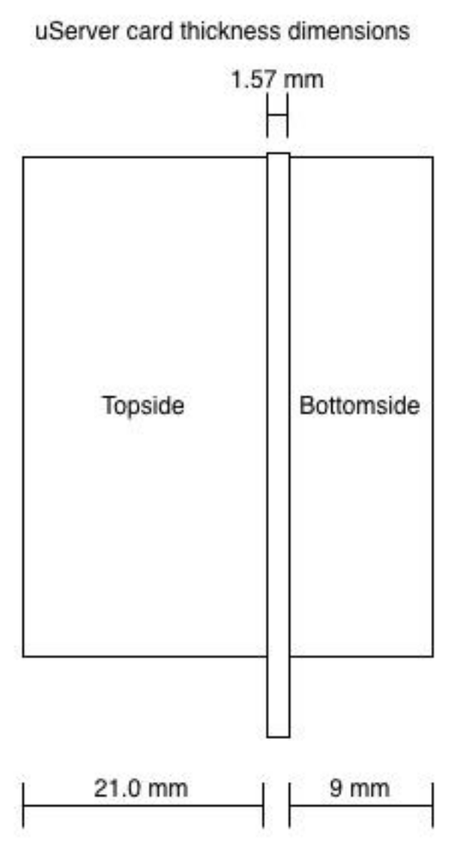


Micro-server mechanical details

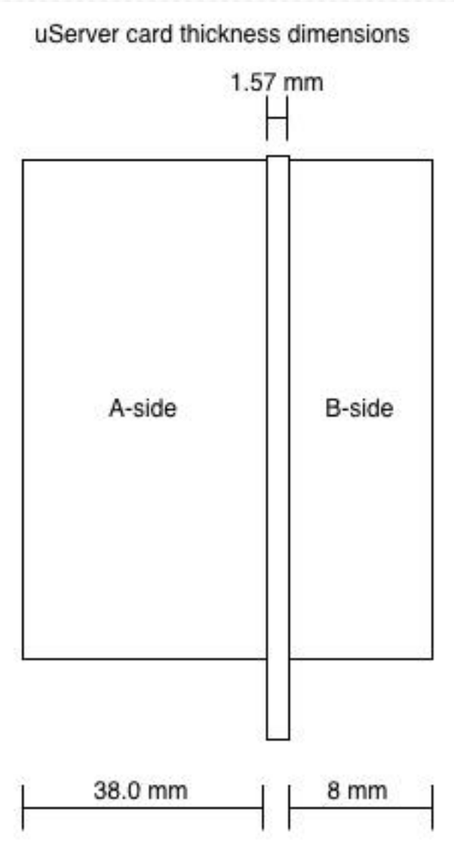


Notes:
- Memory may be placed on A-side, B-side, or both sides, but must be placed ahead of the SOC (towards the cold-aisle).
- Memory may be oriented in any direction. The drawing is for illustration purposes only and is not intended to define specific placement or quantity of memory slots.
- SOC must be placed on A side.

Micro-server mechanical details

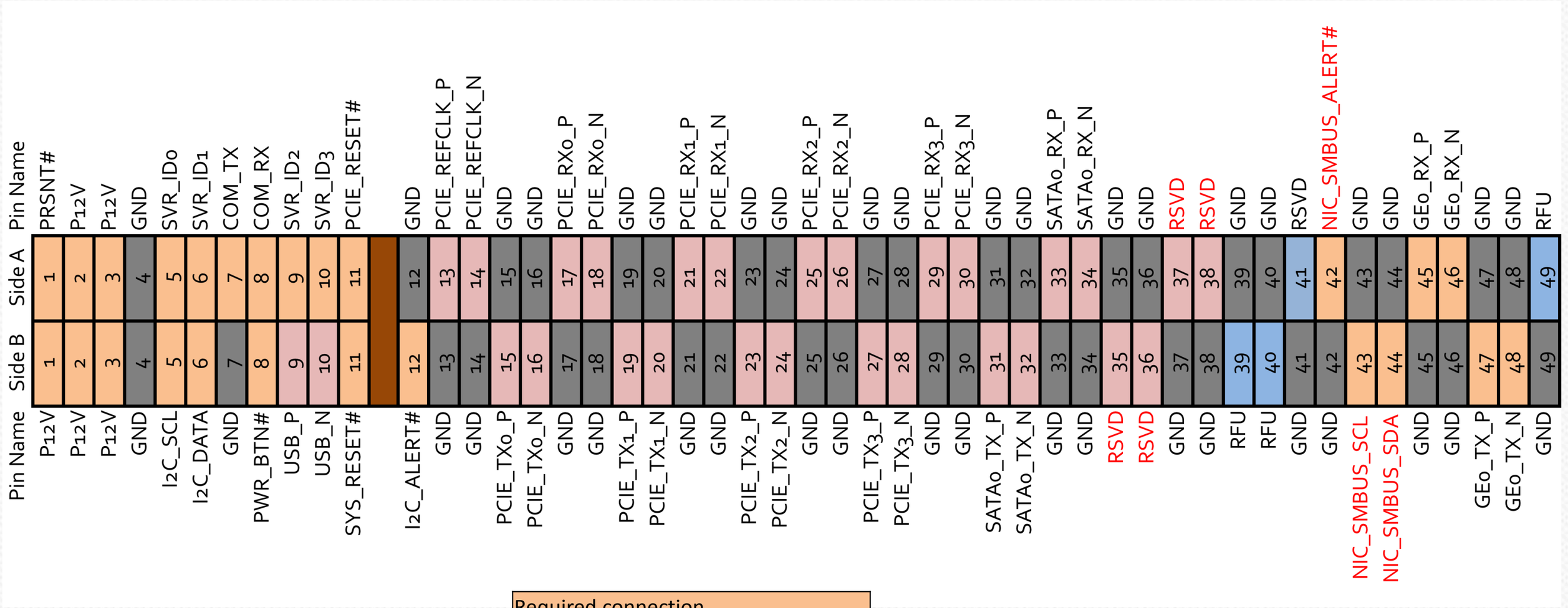


Single-width



Double-width

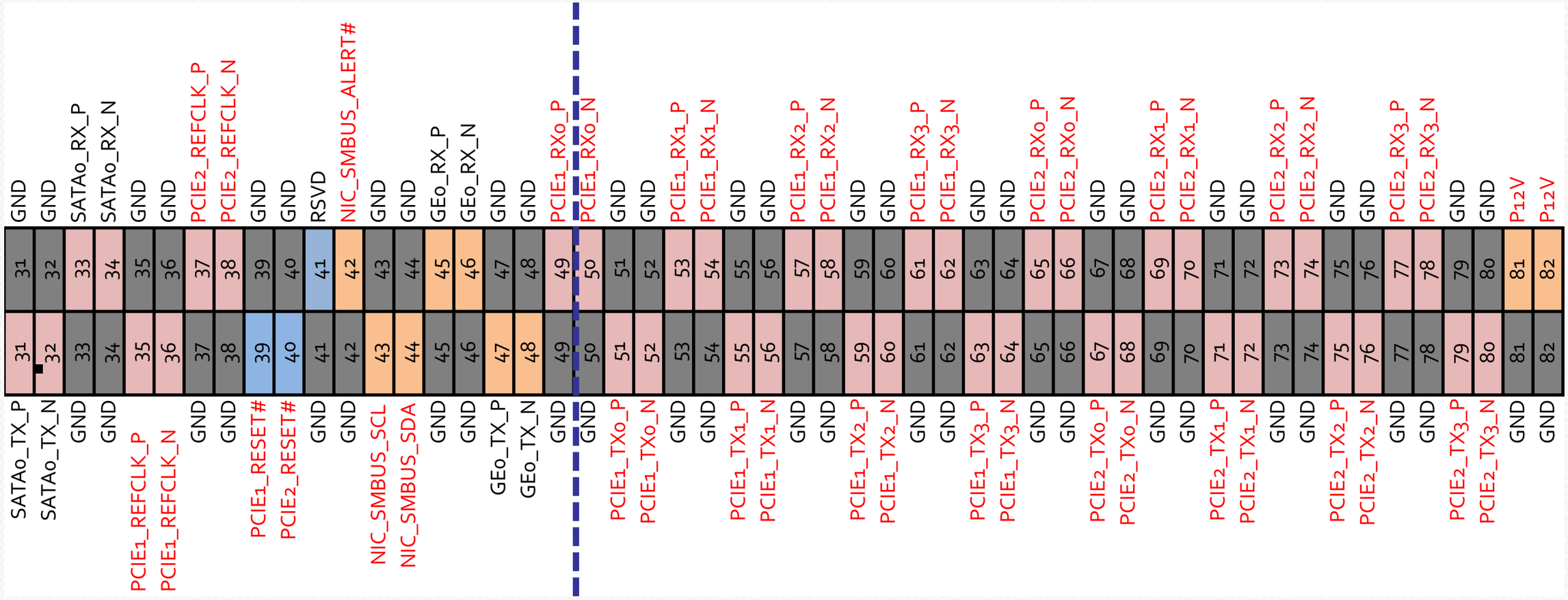
Micro-server updated x8 connector pin-out



Required connection
Configurable connection
Reserved for future use

Micro-server x16 connector pin-out

x8 . .



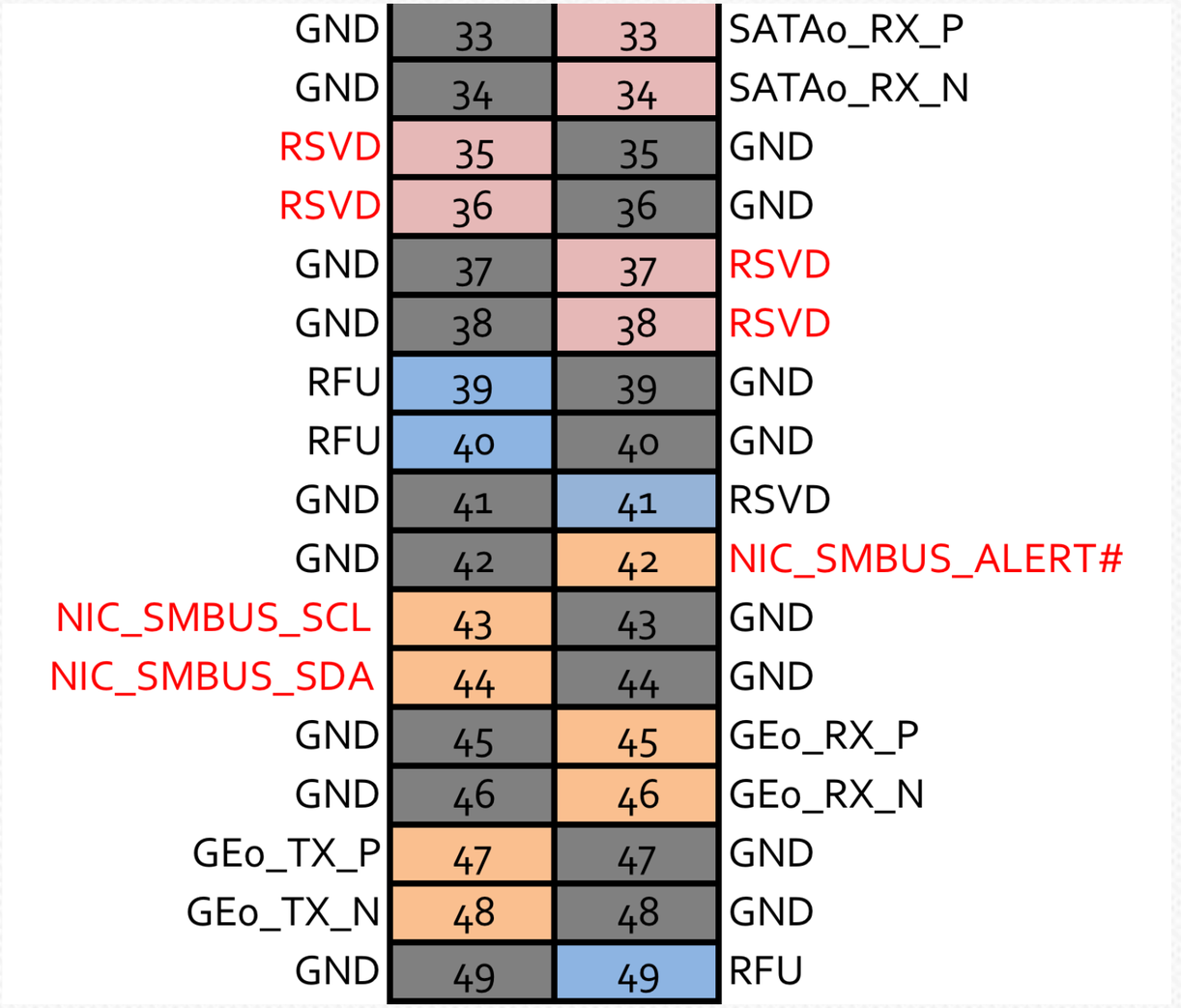
Micro-server x8 changes

Added 2nd SMBUS connection

- Provides connection from BMC to an SOC with an integrated NIC
- Enables “shared” BMC connection

Removed 2nd SATA connection

- Changed pins to RSVD to enable x8 cards in x16 slots



Micro-server x16 additions

More PCIe

- Support for 3x x4 connections (12 lanes total)
- 3x clocks
- 3x resets

	34	34	SATA0_RX_N
PCIE1_REFCLK_P	35	35	GND
PCIE1_REFCLK_N	36	36	GND
GND	37	37	PCIE2_REFCLK_P
GND	38	38	PCIE2_REFCLK_N
PCIE1_RESET#	39	39	GND
PCIE2_RESET#	40	40	GND
GND	41	41	RSVD

More power pins

- 2x more 12V pins
- Supports up to 80W cards

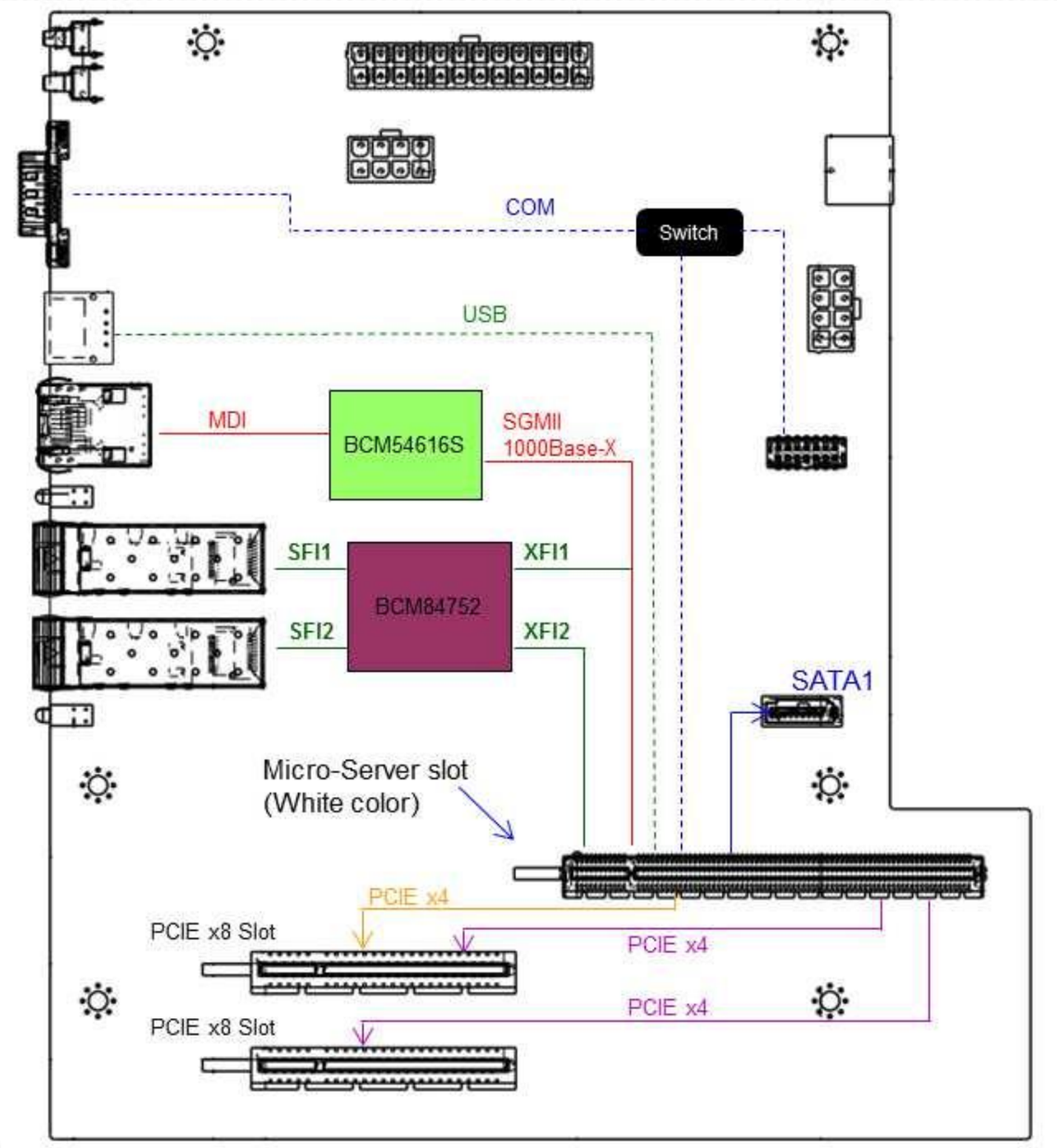
GND	49	49	PCIE1_RX0_P
GND	50	50	PCIE1_RX0_N
PCIE1_TX0_P	51	51	GND
PCIE1_TX0_N	52	52	GND
GND	53	53	PCIE1_RX1_P
GND	54	54	PCIE1_RX1_N
PCIE1_TX1_P	55	55	GND
PCIE1_TX1_N	56	56	GND
GND	57	57	PCIE1_RX2_P
GND	58	58	PCIE1_RX2_N
PCIE1_TX2_P	59	59	GND
PCIE1_TX2_N	60	60	GND
GND	61	61	PCIE1_RX3_P
GND	62	62	PCIE1_RX3_N
PCIE1_TX3_P	63	63	GND
PCIE1_TX3_N	64	64	GND
GND	65	65	PCIE2_RX0_P
GND	66	66	PCIE2_RX0_N
PCIE2_TX0_P	67	67	GND
PCIE2_TX0_N	68	68	GND
GND	69	69	PCIE2_RX1_P
GND	70	70	PCIE2_RX1_N
PCIE2_TX1_P	71	71	GND
PCIE2_TX1_N	72	72	GND
GND	73	73	PCIE2_RX2_P
GND	74	74	PCIE2_RX2_N
PCIE2_TX2_P	75	75	GND
PCIE2_TX2_N	76	76	GND
GND	77	77	PCIE2_RX3_P
GND	78	78	PCIE2_RX3_N
PCIE2_TX3_P	79	79	GND
PCIE2_TX3_N	80	80	GND
GND	81	81	P12V
GND	82	82	P12V

Other updates

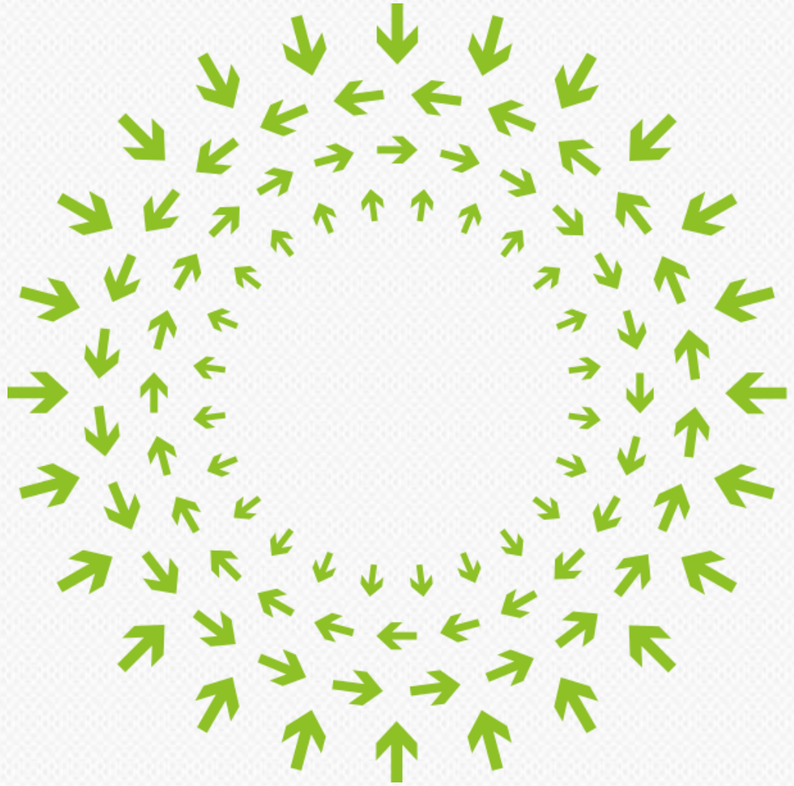
- Added requirement for IPv6 support
- Added requirement for UEFI firmware
- Added BIOS ECC error code table
- Removed “Chassis” FRU information

Test system

- Micro-ATX form factor test board is available now



Q & A



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