

OPEN
Compute Project

QCT Rackgo X Yosemite V2

Product Marketing Specification

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Revision History

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1. Overview

“Rackgo X Yosemite V2” is new generation platform that enables with Intel Xeon Processor Skylake-D Product Family. Each Yosemite V2 sled hosts up to “4x OCP compliant 1P server cards” or “2x 1P server cards & 2x device cards”. And each vCubby chassis can hold up to 4x Yosemite V2 sleds.

The system communicates with external world via an OCP 2.0 50Gb Mellanox CX4-LX mezzanine card, or a 100Gb Mellanox CX4 mezzanine card. A Baseband Management Controller is used to manage all 1P servers and the sled itself. The system is single-socket compute system compatible with Open Rack V2.

1.1 Yosemite V2 Sled

Yosemite V2 contains one primary board as the baseboard to hold all of the connectors and common infrastructure pieces, including the 1P server card connectors, OCP V2 mezzanine card connectors, a 12.5V inlet power connector (from the Cubby chassis). BMC section, fan connectors, and a hot-swap controller.

Yosemite V2 baseboard is installed horizontally on the side of a Cubby chassis. OCP complaint 1P server cards with height of 160mm can be installed vertically to the baseboard in new v-cubby.



Figure 1 Yosemite V2 Sled

Table 1 High Level Features- Yosemite V2 Sled

Function	Description
Processor	<ul style="list-style-type: none"> Intel Skylake-D, Xeon processor, up to 18 cores, TDP up to 110W. Twin Lakes only support 86W
Memory	<ul style="list-style-type: none"> Up to 4 DDR4 channels (2DIMMs / channel) Max Memory capacity of Twin Lakes: 128GB. 16GB*8 or 32GB*4
External I/O Connections	<ul style="list-style-type: none"> 32 x PCIe Gen3 Lanes (CPU) <ul style="list-style-type: none"> (6) X4 to gold finger (2) X4 to high-speed storage drive M.2 connector on Twin Lakes. 20 x Gen3 over HSIO (PCH) <ul style="list-style-type: none"> (1) X4 PCIe for Mellanox CX-4 LX mezzanine (1) USB 3.0 for DCI (1) PCIe X1 for VGA (1) USB 2.0 to baseboard (1) Serial connection(Tx/Rx only) I2C Management connection Power On/Off, Reset control
Storage	<ul style="list-style-type: none"> (3) M.2 connectors. One for boot drive(Pcie or SATA). Two for high-speed storage drive(Pcie).

1.2 Yosemite V2 Functional Block Diagram

High level functional block diagram of Yosemite V2 is shown

Yosemite V2 Block Diagram V0.04

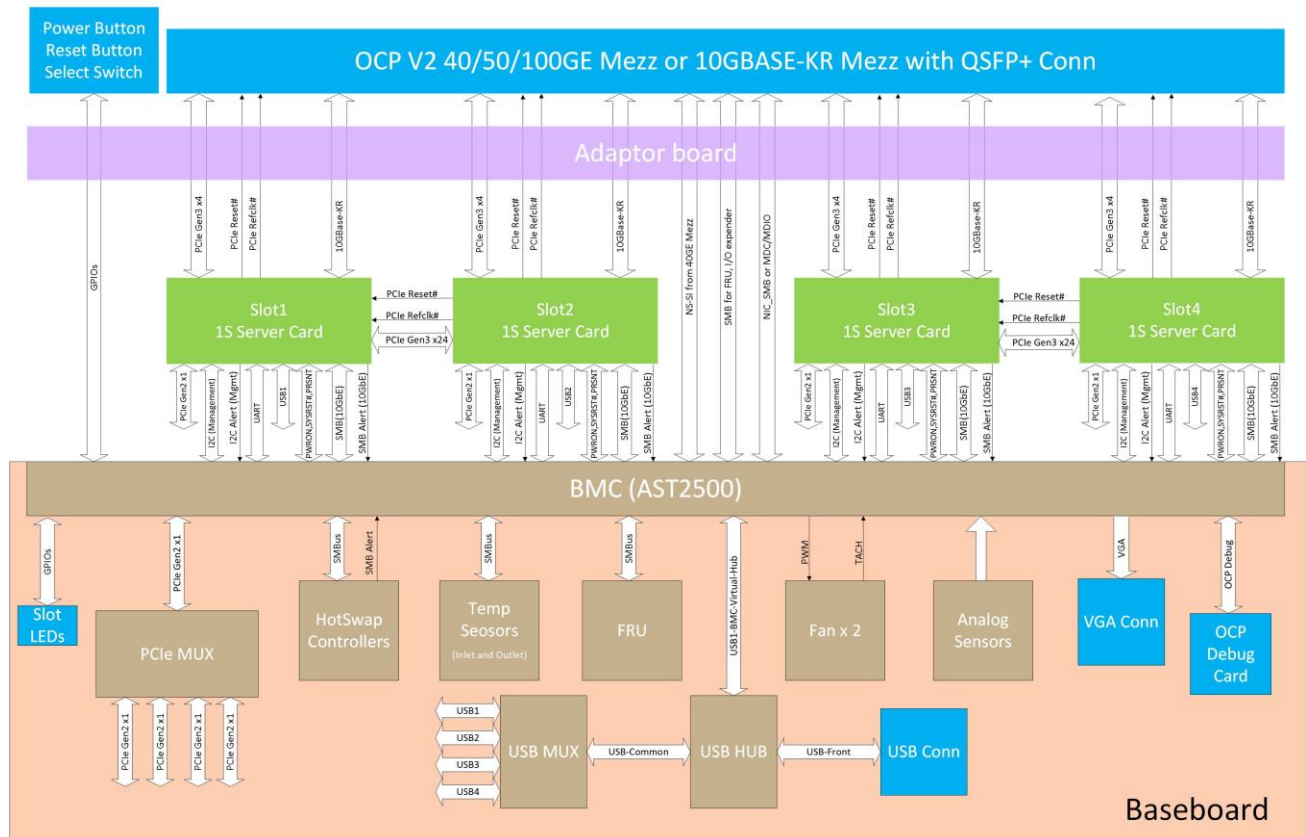


Figure 2 Yosemite V2 Functional Block Diagram

2. Mechanical View





Figure 3 Mechanical View-System Level





Figure 4 Mechanical View-Sled Level



Figure 5 Mechanical View-Server Card Level

3. Motherboard (Twin Lakes)

Twin Lakes is a PCIe card like 1P server, particularly designed for Yosemite V2 platform. Twin Lakes uses Intel's next-generation Skylake-D SOC, which supports up to 18 Xeon cores, up to Up to 4 DDR4 channels, x32 PCIe Gen3 lanes, 20 High-Speed Flexible Lanes configured as PCIe or SATA or USB3, X6 SATA3 ports, Up to 4 USB 2.0, eSPI/LPC, SMBus, Integrated Clocking and other advanced features.

Twin Lakes supports 8 DDR4 RDIMMs, 2 RDIMM per memory channel. The maximum memory capacity of Twin Lakes is 128GB, or 32GB per DIMM each channel. Three M.2 SSD drives are connected to Skylake-D on Twin Lakes. The boot drive's bus lanes come through a SATA or PCIe interface from PCH with BOM option. The other two high-speed storage drives are connected from CPU PCIe port.

A Bridge IC is used to connect BMC and Skylake-D together for server management through an I2C interface. The BMC on Yosemite V2 can access FRU and temperature sensors through the Bridge IC.

3.1 Twin Lakes Block Diagram

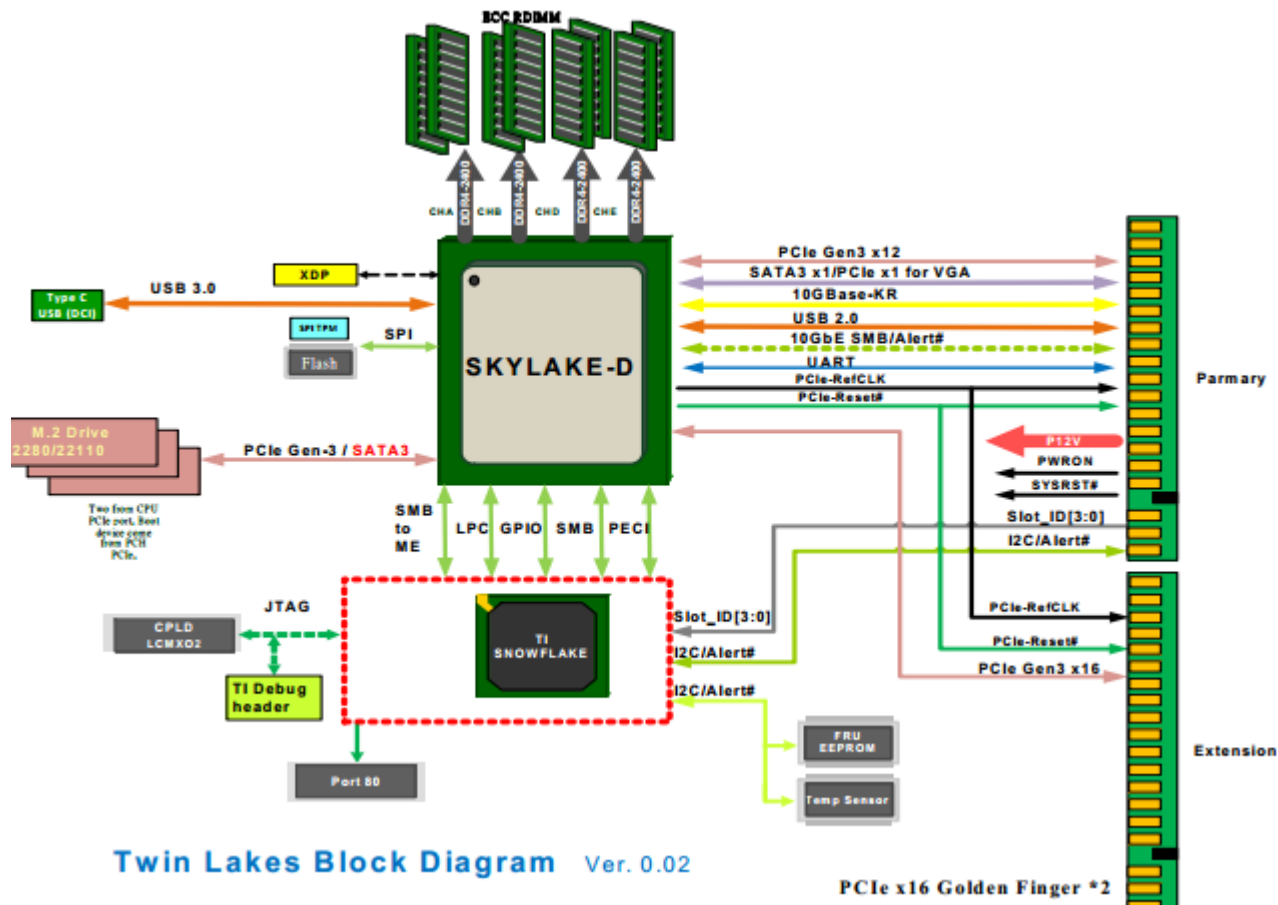


Figure 6 Twin Lakes Block Diagram

3.2 Twin Lakes Outline & Placement

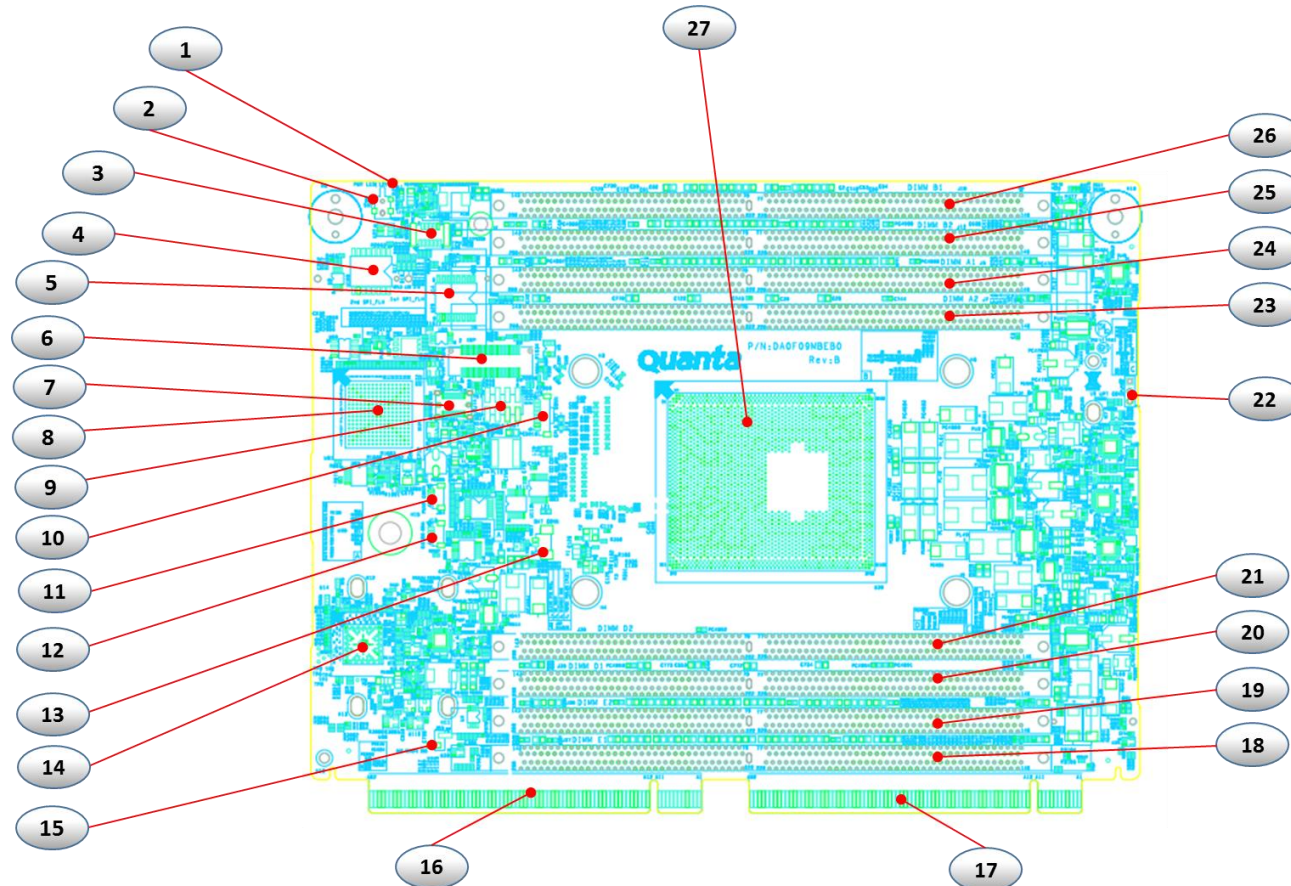


Figure 7 Twin Lakes placement- Top Side

Table 2 Function Description-Top Side

Item	Ref Designator / function	Description	Note
1	D12 / PWR LED (12V)	Power Led will light on when power on.	It is indicated P12V_STBY is ready.
2	SW1 / Detect switch	It will open when ejector release.	
3	J33 / TPM Conn	For TPM module.	
4	U109 / 2nd SPI flash	2 nd BIOS SPI flash	
5	U29(J14)/1st SPI flash	1 st BIOS SPI flash	
6	J41 / XDP header	XDP header for debugging.	
7	J74 / USB DCI conn	USB type C connector for the DCI feature only.	No plan to support other device.
8	U81 / CPLD	CPLD chip	
9	J83 / Jumper header	CMOS clear jumper : pin 1-2	

		open : Normal (default) short : Clear RTC register. ME recovery mode jumper : pin3-4 open : Normal (default) short: ME recovery mode Disable BIC jumper : pin5-6 open : Normal (default) short: Disable BIC. Force CPLD to power-on : pin7-8 open : Normal (default) short: Force power-on.	
10	J76 / CPLD update conn	CPLD in system programming header	
11	J84 / Liquid cooler pump conn	Liquid cooler pump connector	
12	J13 / BIC debug conn	Bridge IC debug connector	
13	BT1 / Coin battery conn	Coin battery connector	
14	U14 / Bridge IC	Bridge IC	
15	J85 / Remote debug disable jumper	Disable remote debugging.	
16	J26 / Primary gold finger	Primary gold finger	
17	J25 / Extension gold finger	Extension gold finger	
18	J37 / DIMM CH E0	DDR4 DIMM connector channel 3 DIMM0	
19	J38 / DIMM CH E1	DDR4 DIMM connector channel 3 DIMM1	
20	J35 / DIMM CH D0	DDR4 DIMM connector channel 2 DIMM0	
21	J36 / DIMM CH D1	DDR4 DIMM connector channel 2 DIMM1	
22	PIP2 / VR update Conn	The connector for VR firmware update	
23	J7 / DIMM CH A1	DDR4 DIMM connector channel 0 DIMM1	
24	J5 / DIMM CH A0	DDR4 DIMM connector channel 0 DIMM0	
25	J12 / DIMM CH B1	DDR4 DIMM connector channel 1 DIMM1	
26	J10 / DIMM CH B0	DDR4 DIMM connector channel 1 DIMM0	
27	U30 / SOC	Includes CPU and PCH.	

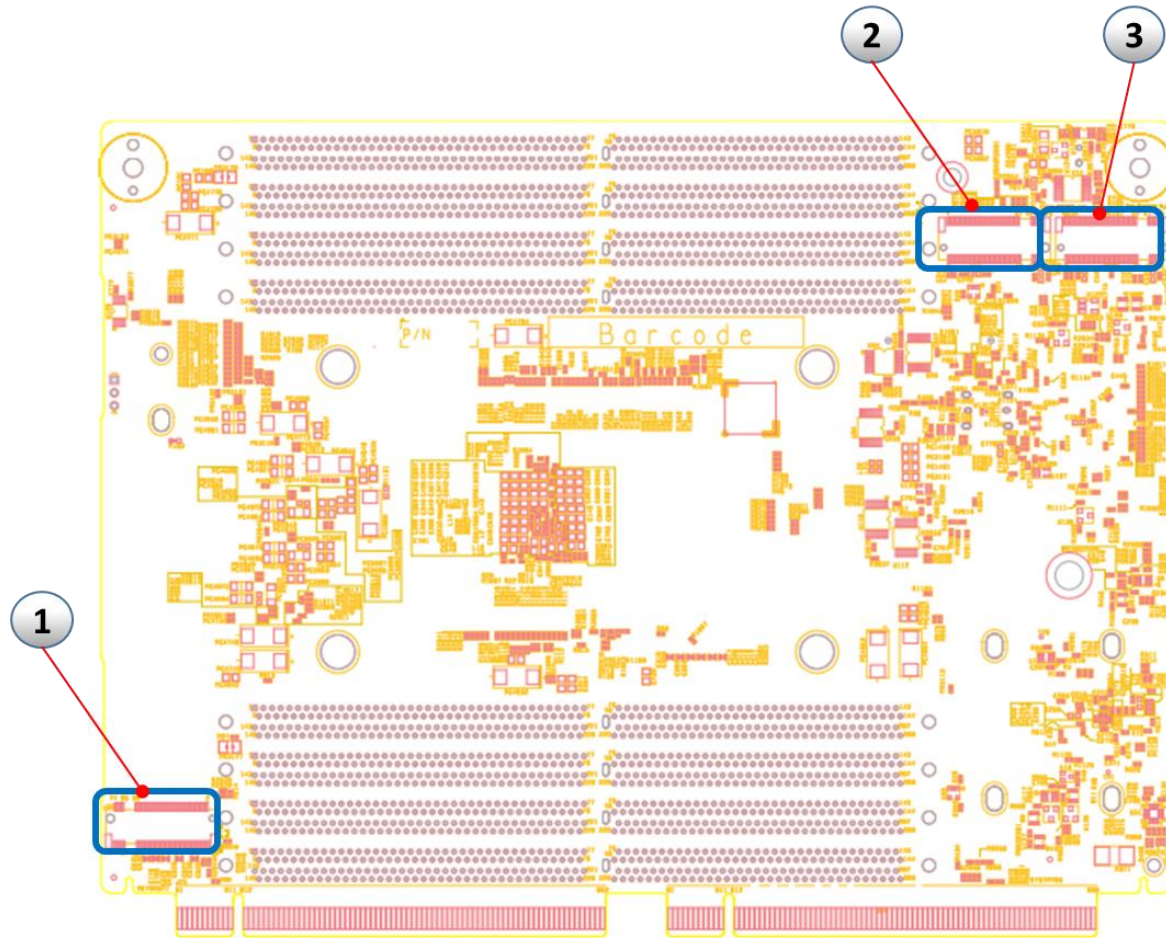


Figure 8 Twin Lakes placement- Bottom Side

Table 3 Function Description-Bottom Side

Item	Ref Designator @PCB	Description	Note
1	J40 / 0 th boot drive M.2 conn	M.2 connector for boot drive. From PCH	PCIe or SATA selection with BOM option.
2	J9 / 1 st storage M.2	1 st M.2 storage connector.	PCIe interface from CPU
3	J34 / 2 nd storage M.2	2 nd M.2 storage connector.	PCIe interface from CPU

4. OCP Tenets/Principles

- Efficiency
 - Modularized design for user to easily allocate the compute/storage/accelerator ratio according to different workload
- Scalability
 - Define a new 1S server card form factor for different modularized compute, storage or accelerator application
- Openness
 - Comply with ORv2 standard
- Impact
 - Provide high efficiency & modularized design to extend the different possible applications

5. Reference

- Facebook Multi-Node Server Platform: Yosemite V2 Design Specification v1.0 spec