



OPEN

Compute Project

MSX1710-OCP

Rev. 1.1

SwitchX®-2 based 40GbE, 1U Open Ethernet Switch
with 36 QSFP+ ports



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Rev 1.1

Revision History

Revision	Date	Description of Change
1.1	April 2015	Added Section 2.1.1, 2.1.2, 17.1, 17.2
1.0	January 2015	Initial release

Scope

This document defines the technical specifications for the MSX1710-OCP switch used in the Open Compute Project

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Overview

The MSX1710-OCF Ethernet system provides the highest performing fabric solution by delivering high bandwidth and low latency to Enterprise Data Centers (EDC), High-Performance Computing (HPC) and Embedded environments.

The SX1710 Ethernet system switch family delivers up to 2.88Tb/s of non-blocking throughput to HPCs, high frequency trading and EDCs, with ultra-low-latency. It has 36 40GbE ports, that when connected to Mellanox NICs with Mellanox cables and adapters, give you the optimal end-to-end solution for Ethernet Data-Centers.

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Manufacturer	Description
Mellanox	SwitchX-2, 36 Port 40GbE Switch IC MT51136A2-CLCR-B
Lattice	CPLD 4320LUT 3.3V LCMXO2-4000HC-4BG332CCA2
Intel	C QM77 EXPRESS CHIPSET BD82QM77-SLJ8A
Intel	IC CPU 1047UE 2M 1.40GHZ AV8063801116300-SR10E
Intel	IC GIGABIT ETHERNET CONTROLLER 82583 WG82583V-SLGVD
Windbond	MEMORY FLASH SPI SERIAL 32MBIT 4KBYTEX1024 W25Q32FVSSIGT
Windbond	MEMORY FLASH SPI SERIAL 64MBIT 4KBYTEX2048 W25Q64FVSSIGT
Windbond	SUPER IO LPC INTERFACE WITH UART NCT5577D
Intel	LHA5 "LEWISVILLE" GIGABIT ETHERNET LAN CONTROLLER HURON WG82579LM-SLHA6
INNODISK	MODULE MSATA SSD 16GB MLC 0..70 DEMSR-16GD07SC2DC-92
APACER	MODULE SO-DIMM DDR3 ECC 4GB 1600MBS 800MHZ SDRAM 204PIN 78.B2GCS.AT00C

1 **Abbreviations**

ToR – Top of Rack Switch

MNG – Management

SWB – Switch Board

FRU – Field Replaceable Unit

PWR – Power

HS – High Speed

SE – Single Ended

OCP – Open Compute Project

WD – Watch Dog

2 Mechanical Drawings

2.1 Mechanical System Overview

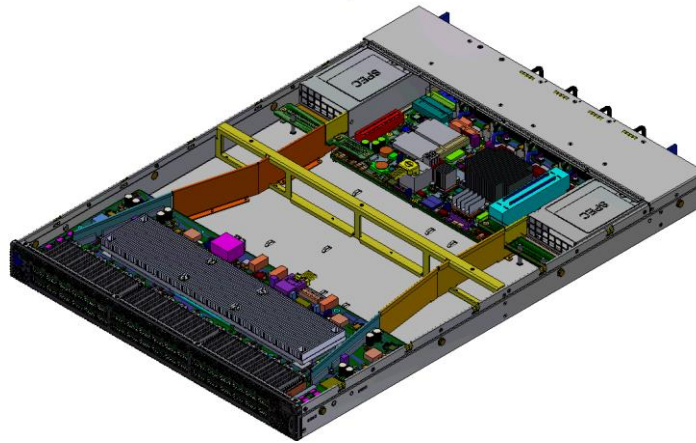


Figure 1 - Mechanical System Overview

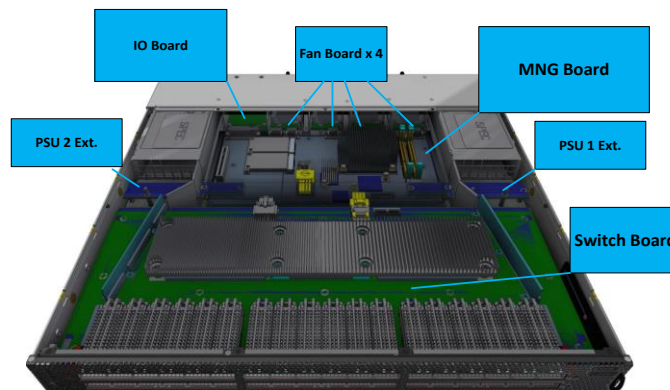


Figure 2 – Main Components

PCB Function	PCB Layer #	Dimensions
Switch Board	18	413 x 186
MNG Board	16	250 x 134
IO Board	4	51 x 80.7
FAN Board	2	40.2 x 18.7
PSU Extender	4	127 x 25

Table 1: PCB Layer Dimensions

2.2 Switch Dimensions (in mm)

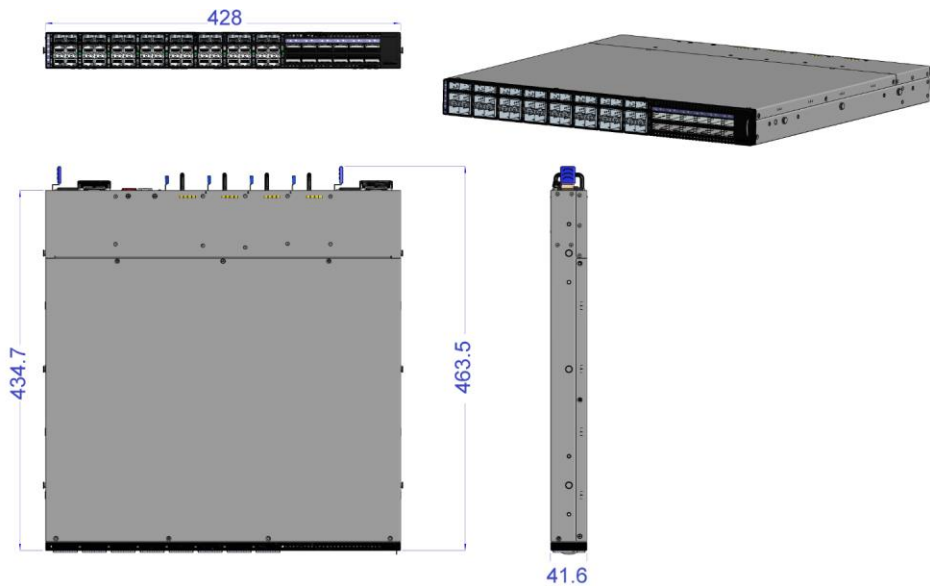


Figure 3 – Short Depth 17" Switch Dimensions

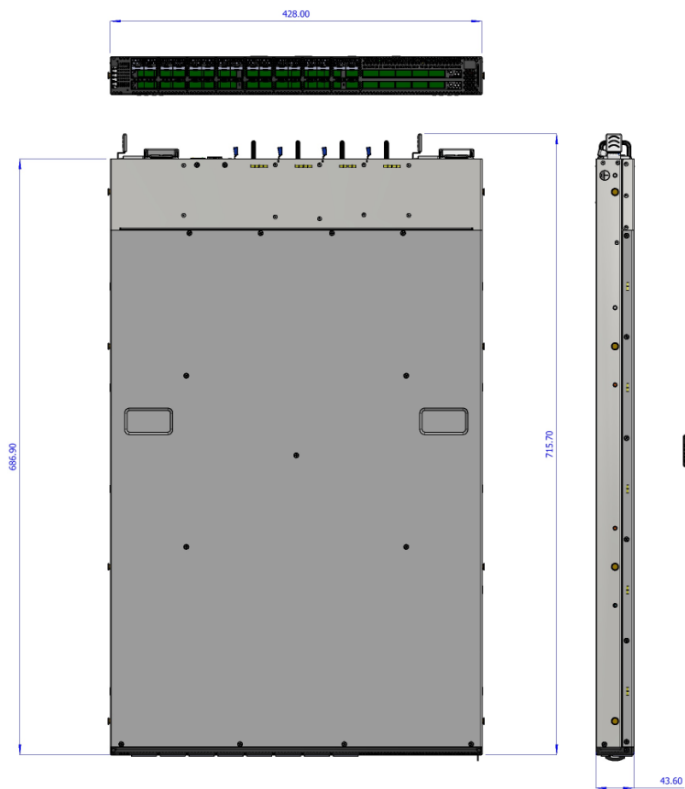


Figure 4 – Long Depth 27" Switch Dimensions

Fan Unit Dimensions (in mm)

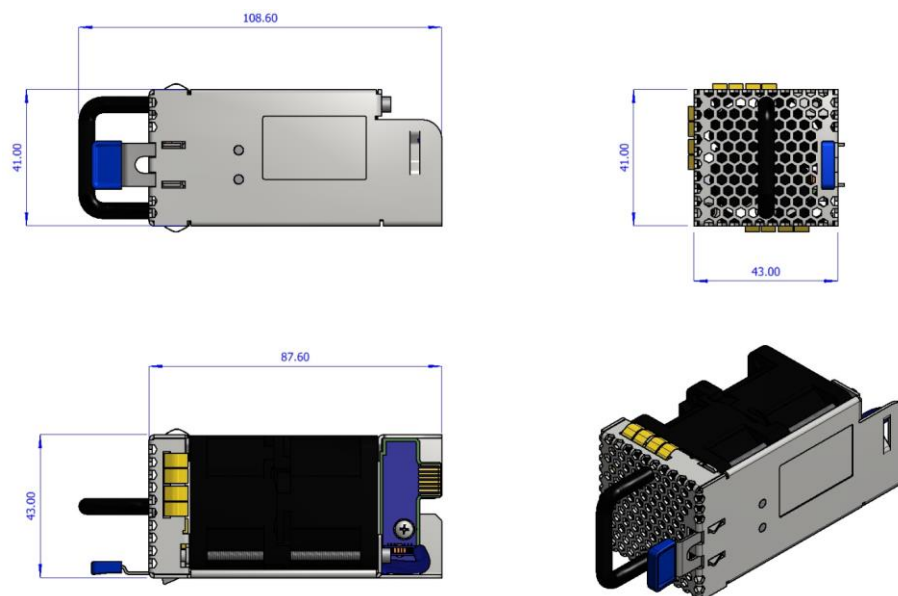


Figure 5: Fan Unit Dimensions

2.2.2 Power Supply Dimensions (in mm)

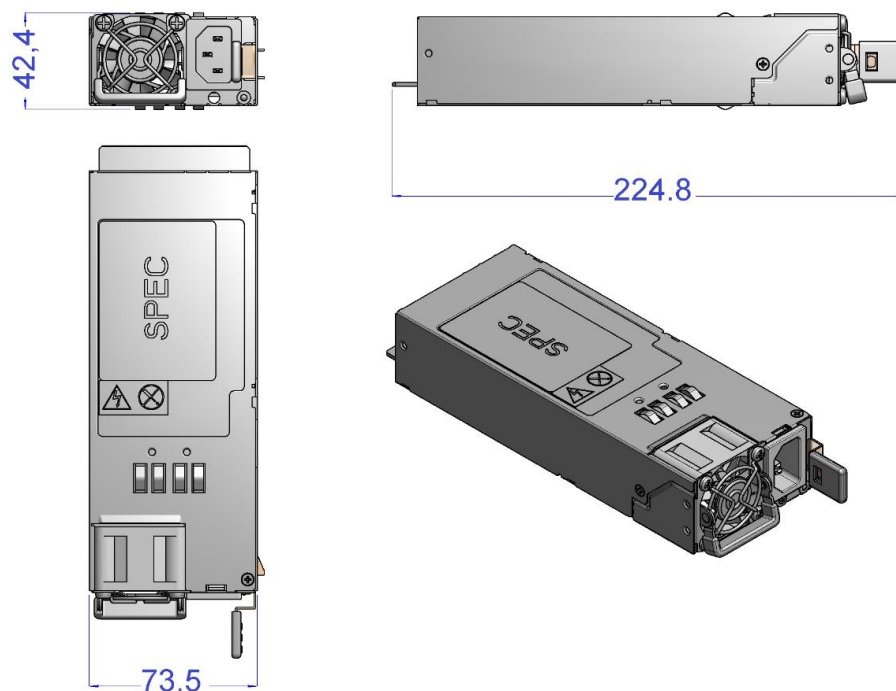


Figure 6: Power Supply Dimensions

3 System Feature List

The SX1710 system supports the following features:

Managed and Unmanaged Systems

- 1 + 1 redundant 460W AC/DC hot swappable power supplies
- 3 + 1 redundant dual fan units (supports IN/OUT Airflow)
- External I²C connector (shard with RS232 connector in managed systems)
- Reset Push button on front & back panel (only FRU PB side will be assembled)
- Front/back panel indication LEDs
- FRU EEPROM on:
 - All FRUs
 - MNG Board
 - Switch board
- JTAG support in fully assembled system

Managed Systems Only

- 2 x 10/100/1000BASE-T RJ-45 Ethernet external ports
- 1 x USB external connector
- RS-232 external connector
- 4X PCIE up to Gen2 interface between MNG and switch board

3.1 Management Board Feature List

Managed Systems Only

- CPU: Intel Ivy Bridge (1047UE in the basic version)
- Chipset: Intel QM77 (Panther Point)
- X8 PCIe GEN3 from CPU to PCIe slot connector** (not supported in the basic version)
- Up to two 1333MTs, 8GB (Each), DDR3, ECC SO-DIMM modules (1X4G in the basic version)
- Supports up to 2 mSATA 4/8/16/64GB SLC or MLC SSD modules (1X16G MLC in the basic version)
- 2 SPI flash memory chips, 64Mb each, for BIOS code
- 2 additional SPI flash chips, 64Mb each, for BIOS FU fail safe support
- BIOS field upgrade
- Real Time clock 24H-SuperCap (optional battery)
- Assembly option for Connect-X3 as bridge between the CPU and SwitchX-2 (not supported in the basic version)
- Super cap for SSD surprise power off (not supported in the basic version)
- No internal graphic core

**Gen3 is supported only with i5 or i7 CPU

Managed and Unmanaged Systems

- CPLD with field upgrade and Fail Safe capabilities
- Fan control
- AC/DC power supplies control

3.2 Switch Board Feature List

- Supports 36 SR4\LR4\ACC\DAC QSFP ports up to 56Gbps
- Based on Mellanox SwitchX-2
- 2 SPI flash chips – 32Mbit, for SwitchX-2 image
- 2 CPLDs with field upgrade and fail safe capabilities

4 Block Diagram

SX1710 is a SwitchX-2 based system with 36 QSFP ports (40GbE). The SwitchX-2 firmware image is stored in 2 SPI flash modules. All QSFP I/Os are controlled by CPLD on the switch board. SwitchX-2 is connected to the CPU via a 4-lane PCIe bus (in managed systems). Most of the control signals on the MGMT board and switch board are controlled by on board CPLD.

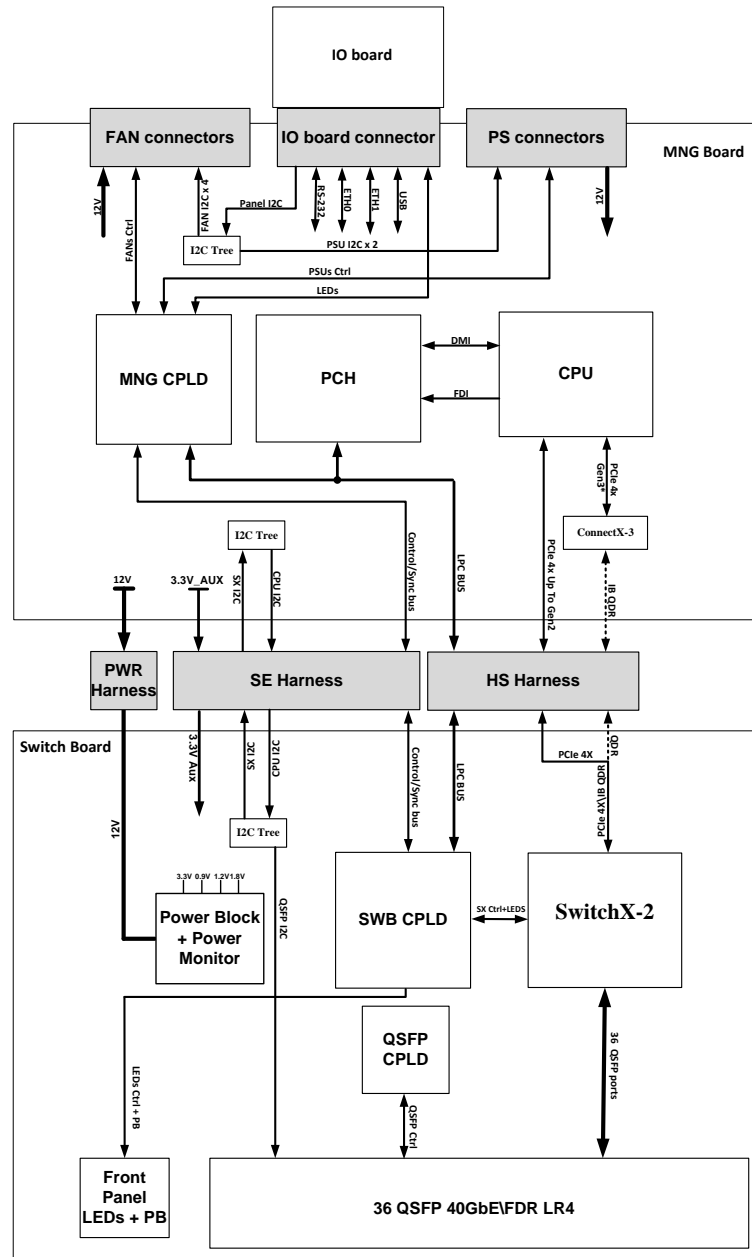


Figure 7: System Block Diagram

5 Ethernet interface

5.1 SwitchX-2

SwitchX-2 is Mellanox's fifth generation switch device, supporting Mellanox's Virtual Protocol Interconnect® (VPI) technology, and enabling converged and virtualized I/O over Ethernet. SwitchX-2 provides 144 network SerDes that can be configured in various combinations of network ports, running multiple standards at several speed options, such as 10, 20, 40 GbE (1X/2X/4X lanes) and 10, 20, 40 Gb/s (1X/4X lanes).

5.2 Port Mapping

The SX1710 switch system includes 36 ports of 40GbE that are reaching towards the panel from the SwitchX-2. The switch supports up to 64 different MACs in different combinations, enabled by the use of split cables.

[Figure 8](#) shows the split options marked in different colors, while each split-4 (green) port is blocking the port above it (gray ports). [Figure 8](#) also shows the general fan-out of the high speed signals on the SX1710 board.

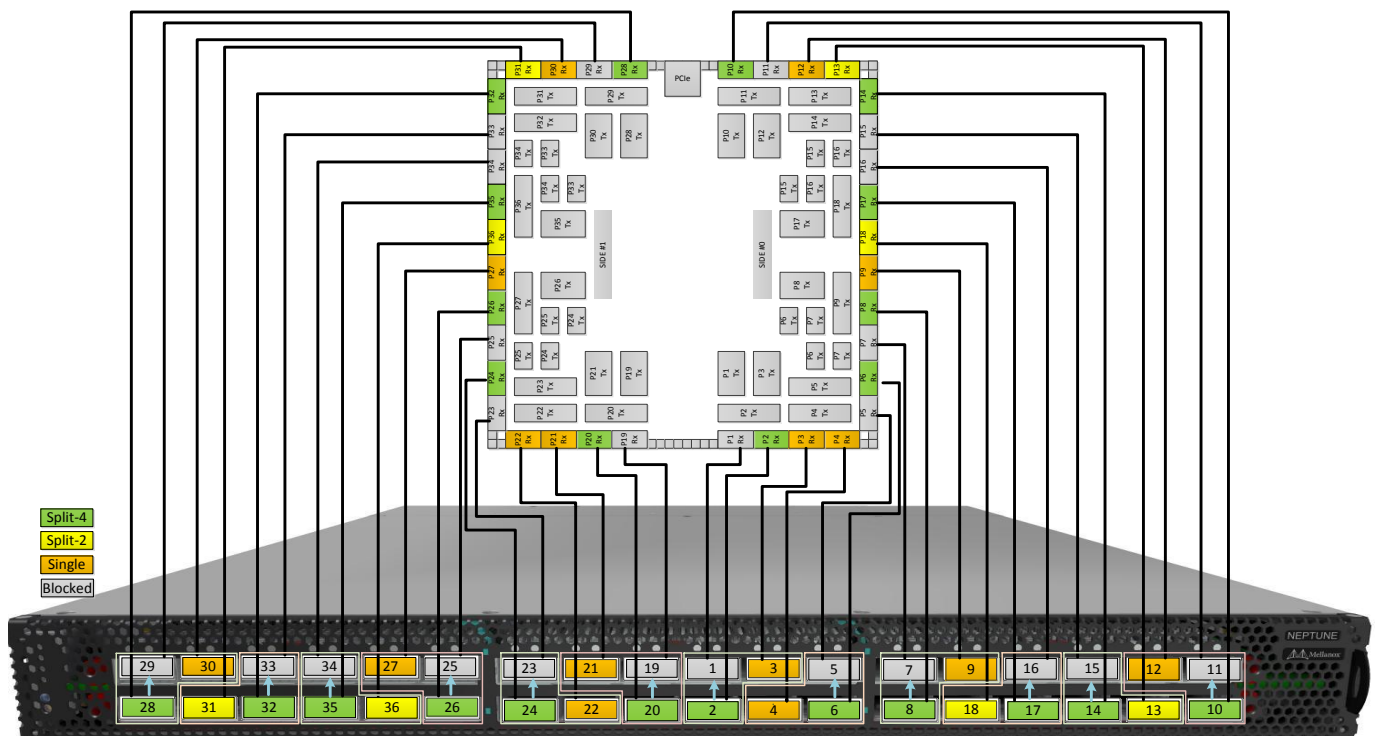


Figure 8: Ports Mapping

Table 2 specifies the SX1710 4X port mapping.

Panel Port	HW Port	Panel Port	HW Port
1	29	19	1
2	28	20	2
3	30	21	3
4	31	22	4
5	33	23	5
6	32	24	6
7	34	25	7
8	35	26	8
9	27	27	9
10	36	28	18
11	25	29	16
12	26	30	17
13	23	31	15
14	24	32	14
15	21	33	12
16	22	34	13
17	19	35	11
18	20	36	10

Table 2: SX1710 Port Mapping

6 QSFP Interface

The SX1710 system has 36 ports of QSFP connectors. Each QSFP connector supports the following:

Signal Name	Description	Type
TD+/TD-	High Speed Transmission pairs (x4)	CML from SwitchX-2 to connector
RD+/RD-	High Speed Receive pairs (x4)	CML from connector to SwitchX-2
SCL/SDA	I ² C slave interface address 0x50	Open Drain from SwitchX-2 to connector
ModSel	Module select for I ² C communication to prevent bus conflicts	In module: short to GND MOD_SEL register in CPLD selects between the ports
ResetL	Module reset use to reset all user module settings to their default state	LVTTTL from CPLD to connector
IntL	Used to indicate the host for a fault or critical status	OC from Connector to CPLD
ModPrsL	Module present	Shorted to GND in module
LPMMod	When the module is in a low power mode it has a maximum power consumption of 1.5W	This signal is floating in the board

Table 3: QSFP Interface

A single QSFP interface in the MSX1410-OCP board is presented in the figure below.

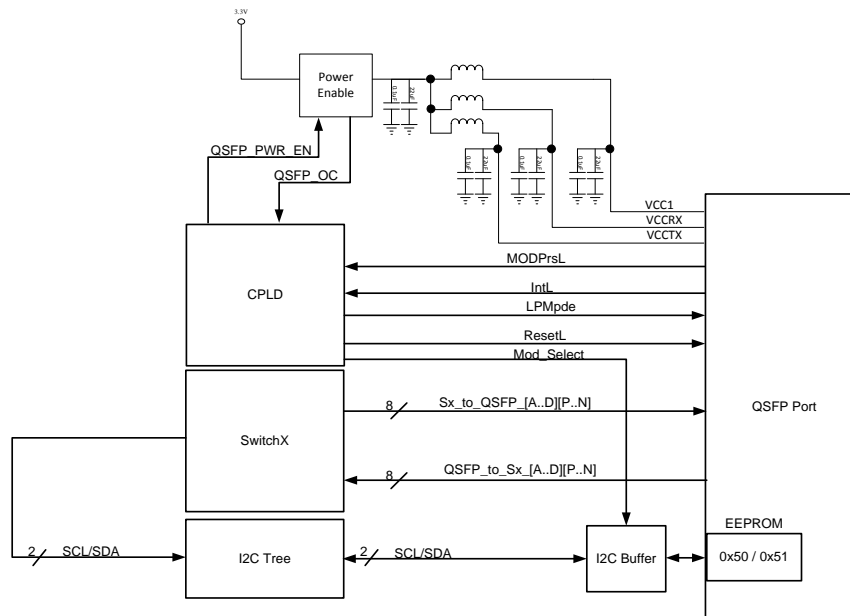


Figure 9 : QSFP Interface

6.1.1 Port over Current Protection

The power for all 4 QSFP modules is controlled by a 5.4 Amperes current, limited power distribution switch. All of these power limiting switches are controlled by QSFP_PWR_EN[1..9] signals (default enabled), originated from the CPLD.

When the output load exceeds the current limit threshold, the power switch limits the current to a safe level. In addition, the QSFP_OVER_CURRENT[1..9] signals are asserted low, in order to notify of the condition to the CPU interrupt registers and to the SwitchX-2 interrupt register. [Figure 10](#) describes a single QSFP interface in the SX1710 board.

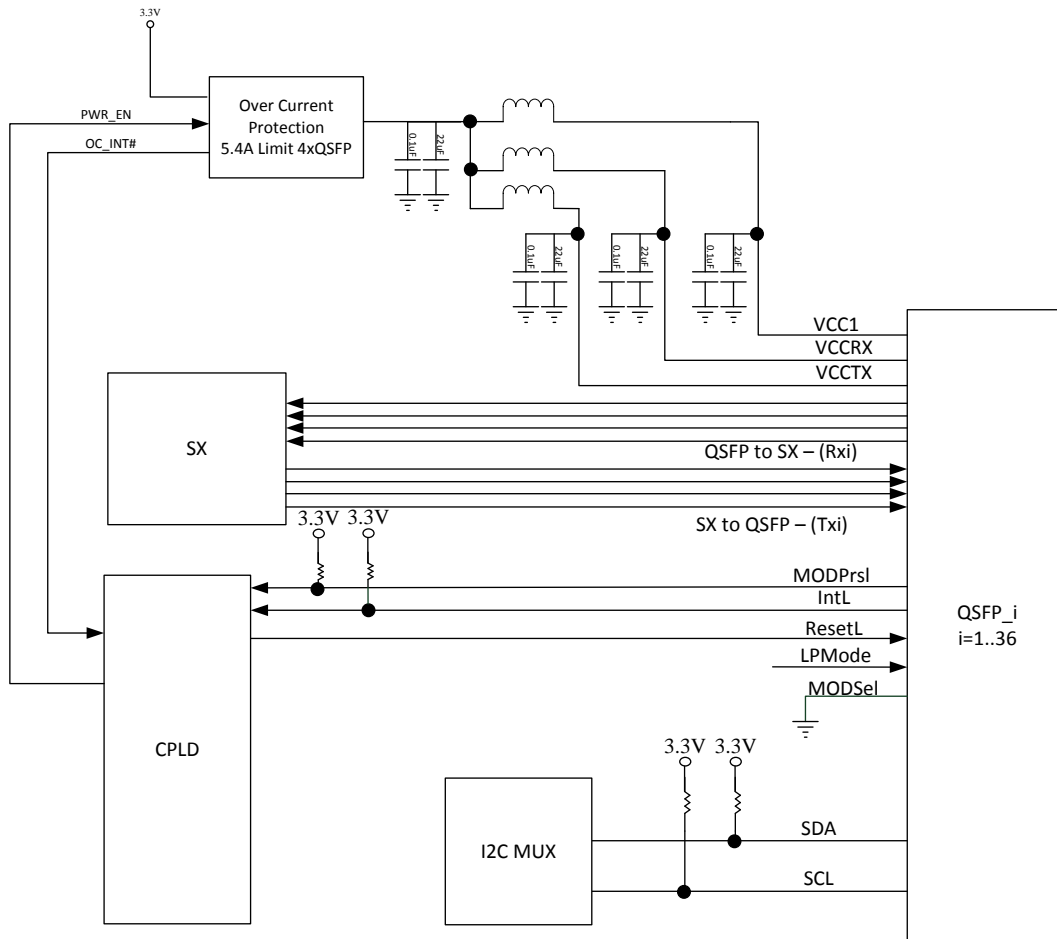


Figure 10: Port over Current Protection

6.1.2Port I²C Interface

CPLD controls the I²C switch and connected to SwitchX-2 secondary I²C bus. 60 different I²C buses are connected from I²C switch to the 60 MSX1410-OCP ports. MOD_SEL register selects which I²C bus will be open– each time only one bus can be open.

The main reason for using this CPLD buffering method is that all the QSFP modules have the same address (0x50). By separating the buses in the CPLD, Switch-X2 can select a specific module to communicate with. Another reason for selecting a different bus for each port is to isolate problematic modules from the others. This way, if a specific port is corrupted, it does not affect the other ports.

6.1.3I²C

- The SX1710 I²C tree contains 4 masters:
 1. SW (LPC to I²C module)
 2. FW (SwitchX-2)
 3. External connector for testing/FAE
 4. BIOS (SMBus)
- The PCH does not support I²C. Therefore, an LPC to I²C module was implemented in the MGMT CPLD.
- I²C switching is done by external analog MUX devices. These devices are controlled by I²C/LPC registers inside the CPLD.
- FW general I²C switching is controlled via 0x61 and 0x63 by writing the channel number into the relevant register. FW ports' I²C switching is controlled via 0x64 by writing "1" to the relevant "ModSel" bit. There is one "ModSel" bit per port and only one can be "1".
- SW I²C switching is controlled via LPC through dedicated registers in the SW reg. map
- The SW master and the connector master share the same MUX and the same head of tree.
- The I²C connector is not connected directly to the head of the SW tree. When connection between the connector and the head of the tree is required, it must be opened via the 0X80 device inside the CPLD.
- When connection between the connector and the head of the tree is enabled, the SW I²C connection to the head of the tree is disabled.
- In case of collision between masters, the following hierarchy will be implemented (decreasing order):
 1. Connector
 2. SW I²C register

3. SW LPC register
 4. FW
- The I²C and the RS232 share the same RJ45 connector on the I/O board.
 - CPLD I²C slave modules 0x61, 0x63 and 0x64 are “Two Byte Address” modules. The rest of the CPLD modules are “One Byte Address modules”.
 - Sequential read and write modes are supported by all CPLD I²C modules.



7 CPLD

Three CPLD devices on the SX1710 provide monitoring and controlling capabilities:

1. MGMT CPLD (CPLD1): located on the MGMT board, controls most of the board's SE signals, fans, PS, power sequence, most of the SW registers, a few FW registers, SW interrupt, FW interrupt, reset, I²C switching, safe BIOS etc.
2. Switch board MGMT CPLD (CPLD2): located on the switch board, responsible for all board peripherals such as LEDs, reset logic, power monitor, I²C switching, SW registers, FW registers etc.
3. QSFP CPLD (CPLD3): located on the switch board, controls and monitors the QSFP ports – this CPLD is mainly controlled by the SwitchX-2. LPC is not connected to this CPLD and therefore, it cannot contain SW registers.

The CPLD codes contain various modules for board control. One of the main modules is the R/W registers for SW and FW control. The registers list with their functionality is presented in the register map documents.

For CPLD registers that are controlled via SW (CPU controlled via LPC), please refer to SX1710 CPLD SW registers map document.

For CPLD registers that are controlled via FW (SwitchX controlled via I²C), please refer to SX1710 CPLD FW registers map document.

CPLD 1 and 2 are connected via a 3-signal sync serial bus. The CPLDs are syncing data using this bus, which was implemented in order to reduce signals connectivity between the two CPLDs. Instead of connecting signal per bit, the bits are synced via a serial bus.

All CPLDs are powered by the auxiliary power; therefore, they still function during main 12V rail shutdown.

7.1 CPLD Features

- Lattice XO2 CABGA332 device
- 4320 Logic elements
- 271 I/Os in four banks
- 96K bit UFM user flash memory
- 332-Pin FineLine BGA
- Field upgrade with Fail-Safe mechanism using SPI flash memory

7.2 CPLD Field Upgrade

All three CPLD devices can be field upgraded through SX JTAG emulation. Fail Safe feature is supported in case of field upgrade failure for all CPLDs.

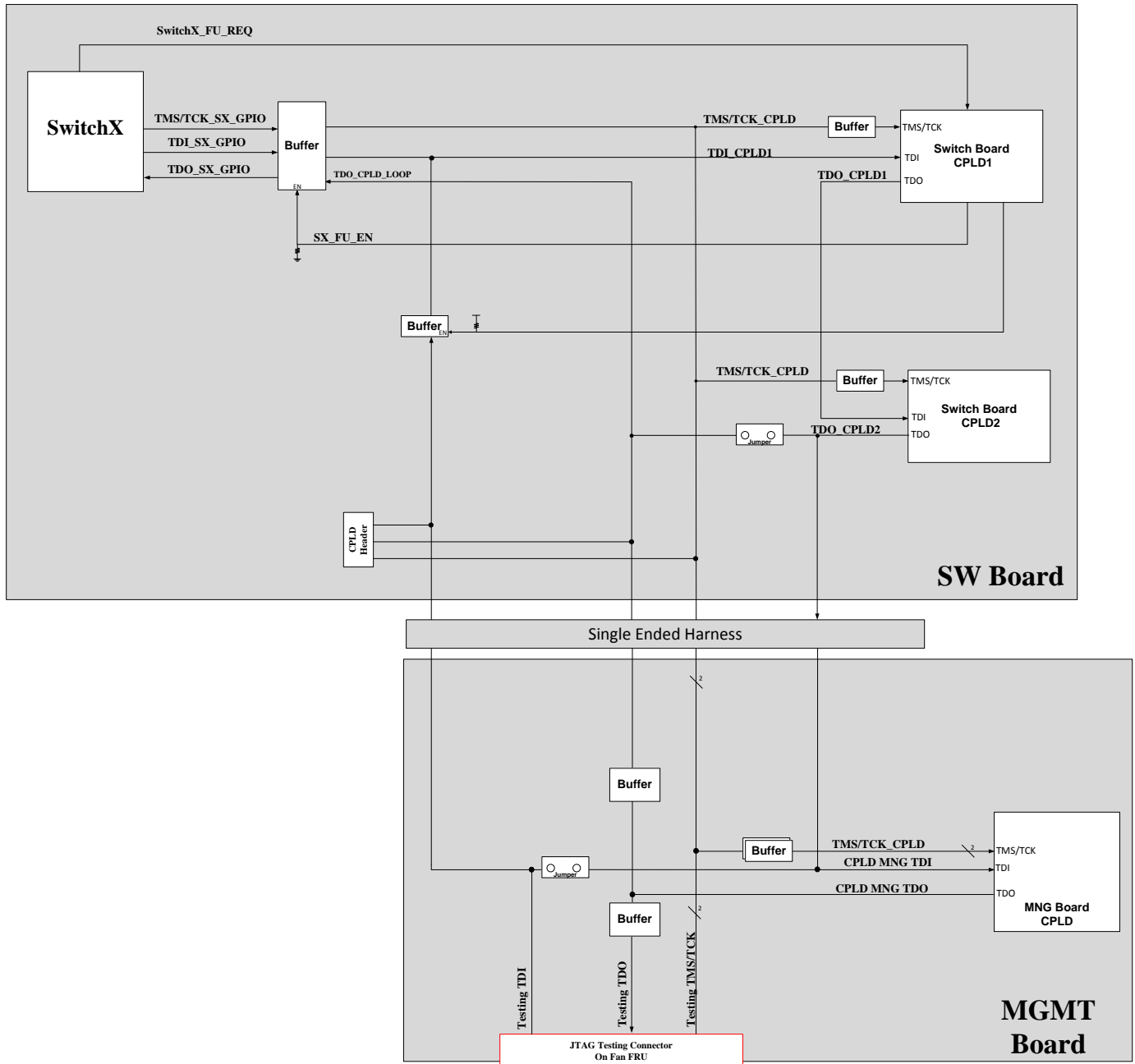


Figure 12: CPLD Field Upgrade and JTAG

8 SPI and Safe BIOS Mechanism



NOTE: This section is relevant to managed systems only.

The Serial Peripheral Interface on the chipset supports two 64MB flash devices (each), storing a Unified BIOS Code.

The MGMT board has two pairs of SPI flash chips: one serves as the default pair, and the other serves as the safe BIOS pair.

The following figure describes the BIOS SPI interface.

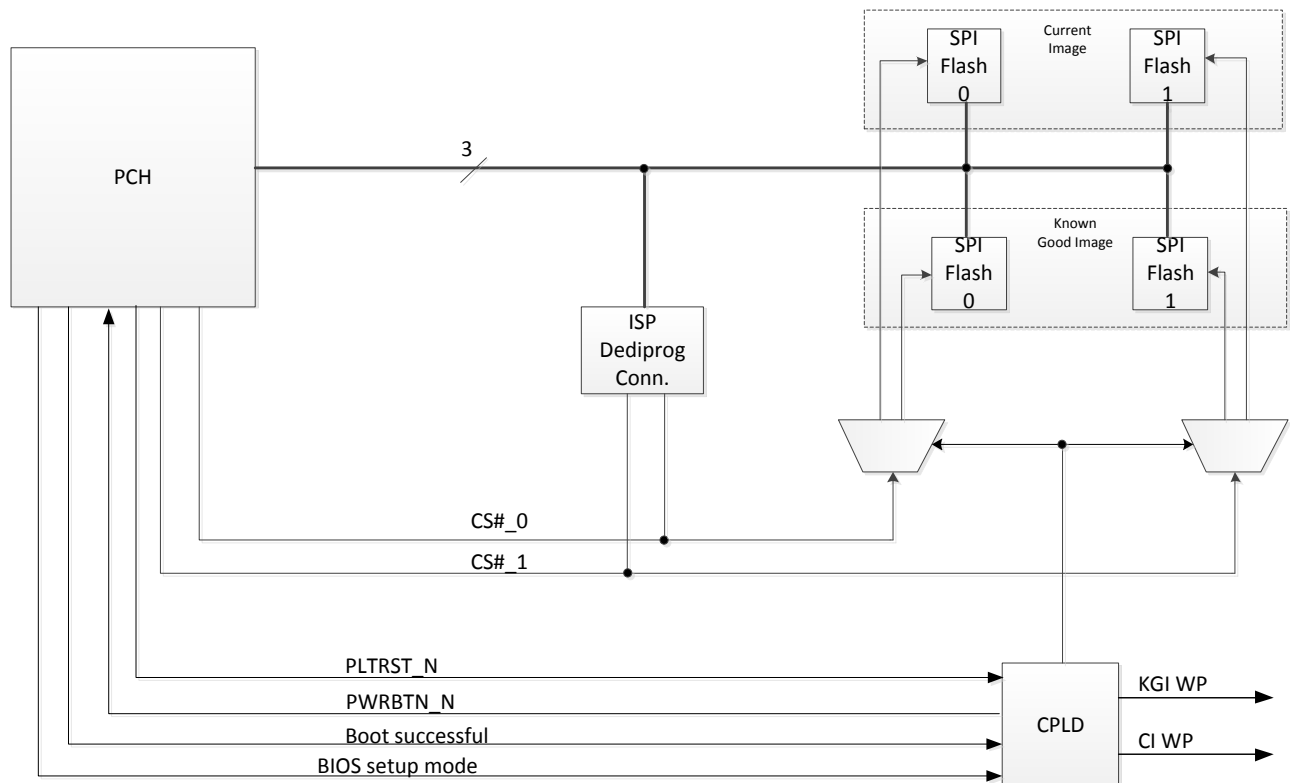


Figure 13: Safe BIOS Mechanism

The system includes two SPI Flash pairs:

- Known Good Image (KGI) pair
- Current Image (CI) pair

Both of these pairs are loaded with identical images at the factory. The factory programmed images are the KGI images, which are not intended for update. The KGI provides an image to allow recovery of the system at any point.

The system always selects the CI as the default boot device after power up. This selection is made by the CPLD.

Safe BIOS events flow:

1. Initial boot: the default is CI.
2. When PLTRST_N is asserted (logic low) and then de-asserted, a timer starts inside the CPLD (this timer's value can vary based upon boot time of the system).
3. The CPLD then waits for "Boot Successful" bit driven by the BIOS.
4. If "Boot Successful" is high before the timer runs out, everything functions properly - normal boot. If not, the mechanism starts working:
5. CPLD selects the KGI pair.
6. Then PWRBTN_N is asserted for 6 seconds, then de-asserted for 5 seconds, asserted for 1 second and then released. This will power cycle the platform (PCH and CPU).
7. The system then boots from KGI.
8. After a successful boot, the CPLD selects the CI again
9. At this point, it is possible to recover the CI using the BIOS FU mechanism.

Note that the CPU has no indication of which image it was uploaded from. Therefore, on every boot, the SW should check a special bit in CPLD (via LPC) that tells which image was uploaded.

In addition to the BOOT_SUCCESS signals, two other signals are connected from the PCH to the CPLD:

- i. BIOS_SETUP_MODE - Asserted high by the PCH, in case the user entered the setup menu. As long as this signal is high, the CPLD counter for boot success is paused.
- ii. BIOS_STARTED - Asserted high by the PCH once the BIOS load is started.

BOOT_SUCCESS and BIOS_STARTED are used for status LED control.

9 Ethernet



NOTE: This section is relevant to managed systems only.

The MNG board provides two Ethernet MDI 10/100/1000MB/s port to the I/O board. One port is connected through internal PCH MAC and Intel 82579 PHY (port 1). The other port is connected through Intel 82583 MAC/PHY (port 2).

These two MDI ports are routed to two RJ45 ports on the I/O board.

The following figure describes the Ethernet interface.

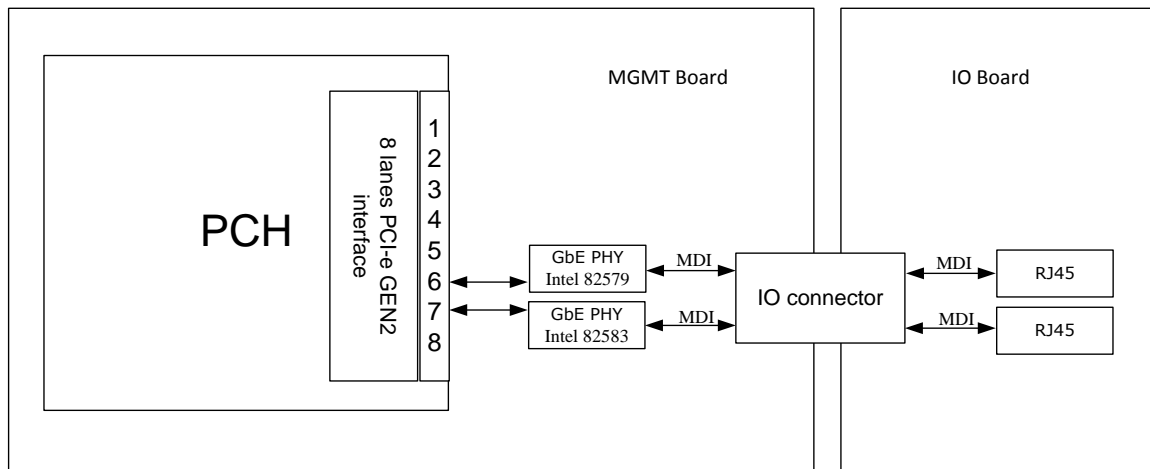


Figure 14: SX1710 Ethernet Interface

10 RS232 Interface



NOTE: This section is relevant to managed systems only.

An 8-pin RJ-45 connector is located on the I/O board and provides CLI connectivity (RS-232) to the CPU. The I²C and the RS232 share the same RJ45 connector.

The following figure describes the RS-232 interface.

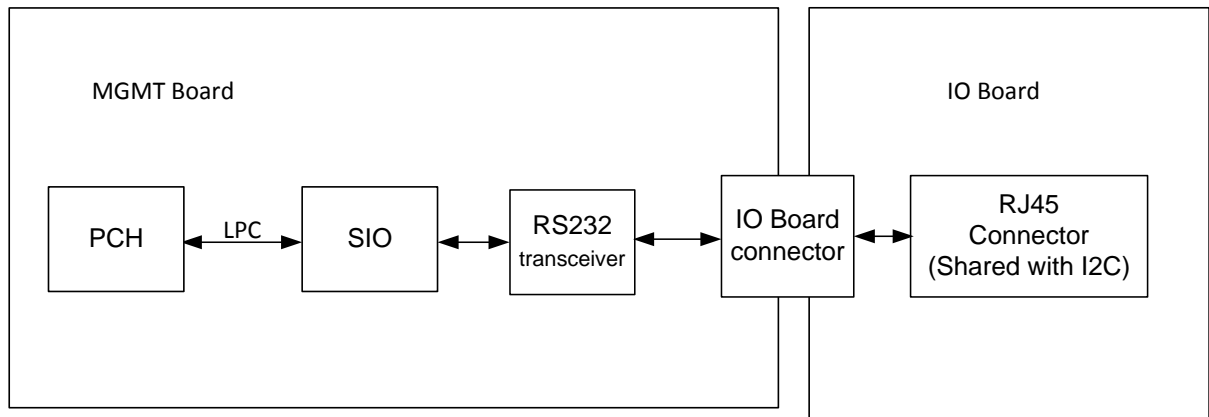


Figure 15: RS-232 Interface

11 USB



NOTE: This section is relevant to managed systems only.

The system has one external USB 2.0 Host interface for general use. The USB port can supply 500mA @ 5V and has internal current limiter with fault signal.

[Figure 16](#) describes the USB interface.

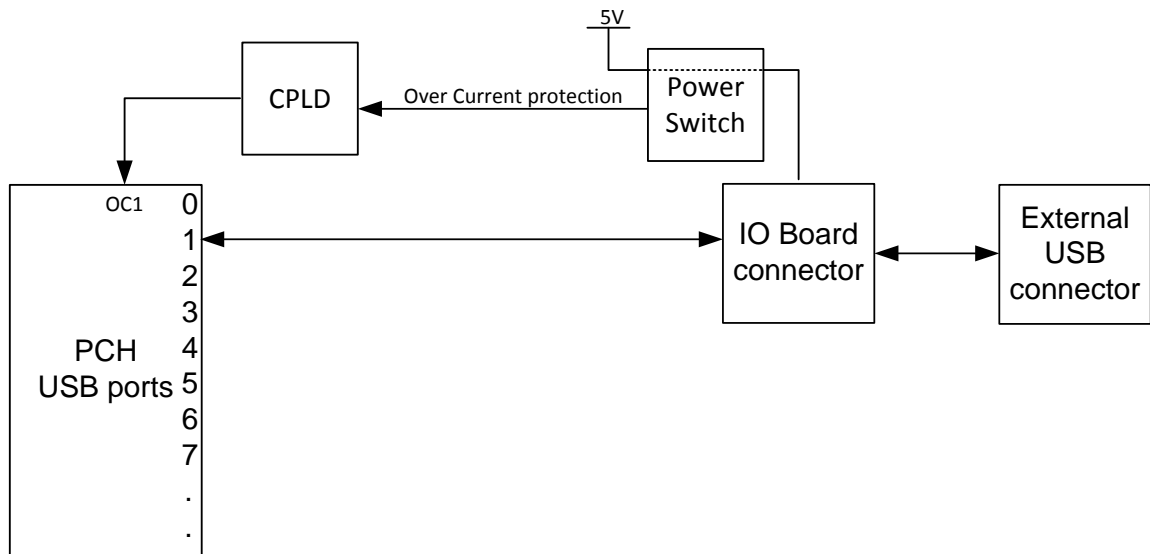


Figure 16: USB Interface

12 LPC



NOTE: This section is relevant to managed systems only.

The PCH implements an LPC interface, as described in the Low Pin Count Interface Specification, Revision 1.1. The LPC interface from the PCH is shown in [Figure 17](#).

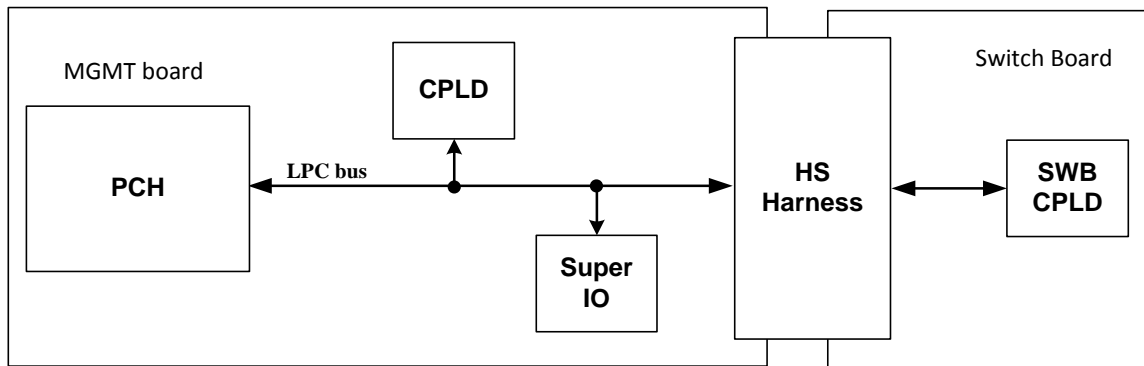


Figure 17: LPC Interface

13 SATA



NOTE: This section is relevant to managed systems only.

Up to two mSATA SSD (Solid State Drive) modules are supported by the system. Each one of them supports 4-64GB SLC or MLC. By default, only one 16GB MLC module is assembled on slot 0.

On power down sequence, both of the SSD modules are powered by a super capacitor, in order to perform a graceful shutdown. The super capacitors provide power to the SSD modules, while the rest of the board parts are already shut down.

[Figure 18](#) describes the SATA interface.

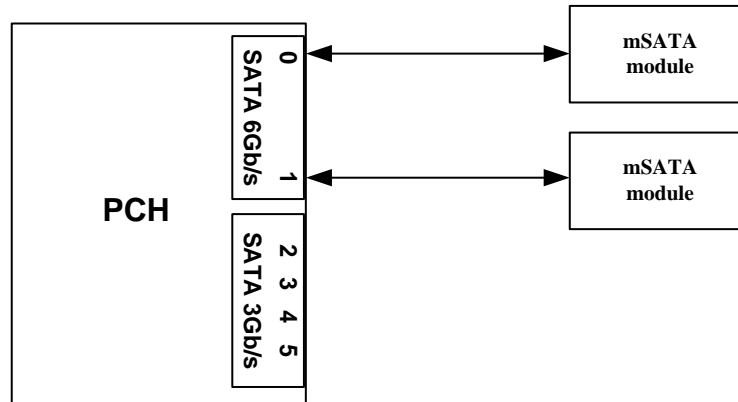


Figure 18: SATA Interface

14 PCIe



NOTE: This section is relevant to managed systems only.

The SX1710 contains 4 PCIe interfaces:

1. 1X from PCH to 82579
2. 1X from PCH to 82583
3. 8X (gen 2 for Celeron/i3, Gen3 for i5/i7) from CPU to 8X slot
4. Connection between the MGMT board and the switch board:

Direct 4X (gen 2 for Celeron/i3, Gen3 for i5/i7) connection between the CPU and SwitchX. The gen is also depended in SwitchX capabilities, currently only Gen1 is supported by SwitchX.

[Figure 19](#) describes the PCIe interface.

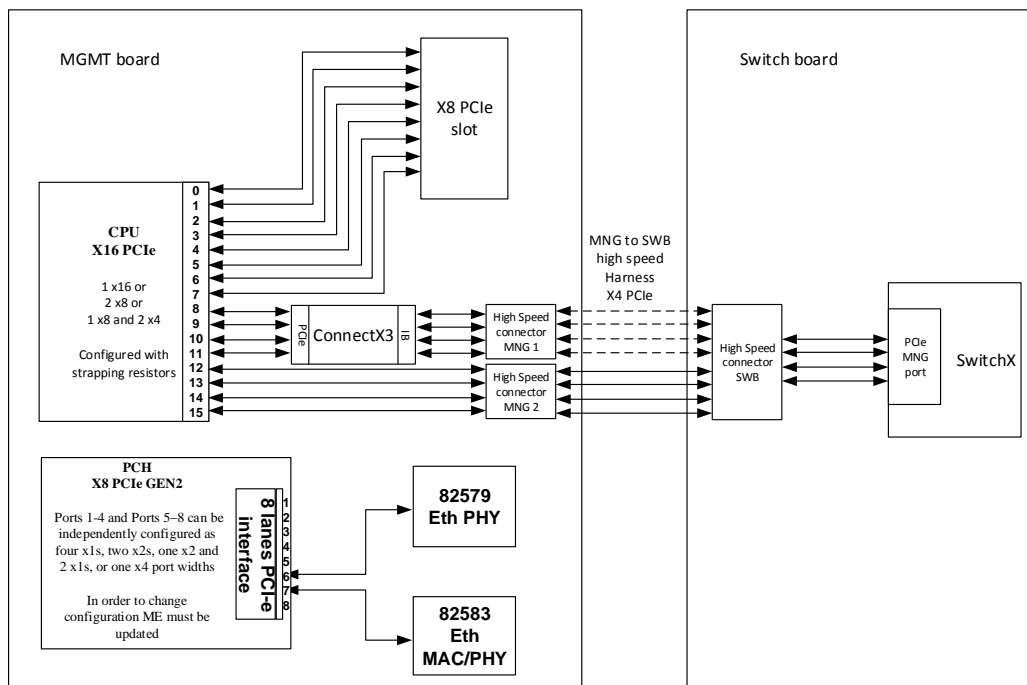


Figure 19: PCIe Interface

15 Power

15.1 Power Consumption

15.1.1 Switch Board Max Power Consumption

Configuration	3.3_SX (3.3V)[W]	1.8_SX (1.8V) [W]	1.2_SX (1.2V) [W]	VCORE_SX (0.9V) [W]	Total 12v Including DC/DC Efficiency
36 Copper (0W per port)	5.9	9.5	20.6	41.2	85.8
36 SR4 (3.5W per port)	77.9	9.5	20.6	41.2	165.8
36 LR4 (2W per port)	131.9	9.5	20.6	41.2	225.8
36 Active cables (1.5W per port)	59.9	9.5	20.6	41.2	145.8

Table 4: Switch Board Max Power Consumption

15.1.2 MGMT Board Power Consumption

Current (Amp)		Power[Watt]															Total power consumption per part
Device	Qty.	0.90	1.23	1.05	1.05	1.35	0.675	0.85	5.00	3.30	1.90	1.05	1.80	0.90	1.20	1.80	
Device	Qty.	CPU Core	CPU GFX	CPU VCCIO	PCH Vtt	Vddq DDR3	Vtt DDR3	VCCSA	5V	3.3V	1.9V	1.05	CPU PLL	ADIR Core	ADIR	ADIR	
CPU	1	47.700	0.000	8.925	0.000	6.750	0.000	5.400	0.000	0.000	0.000	0.000	2.160	0.000	0.000	0.000	35.000
PCH	1	0.000	0.000	0.000	6.152	0.225	0.000	0.000	0.010	0.878	0.000	0.000	0.004	0.000	0.000	0.000	4.000
82583	1	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.017	0.505	0.205	0.000	0.000	0.000	0.000	0.727
82579	1	0.000	0.000	0.000	0.320	0.000	0.000	0.000	0.000	0.310	0.000	0.000	0.000	0.000	0.000	0.000	0.630
CPD	1	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.330	0.000	0.000	0.000	0.000	0.000	0.000	0.330
SODIMM	1	0.000	0.000	0.000	0.000	4.050	0.506	0.000	0.000	0.017	0.000	0.000	0.000	0.000	0.000	0.000	4.573
mSATA	1	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.990	0.000	0.000	0.000	0.000	0.000	0.000	0.990
ConnectX-3	1	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.957	0.000	0.000	0.000	2.124	1.032	0.504	4.617
PCIe slot	0	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000
USB	1	0.000	0.000	0.000	0.000	0.000	0.000	0.000	2.500	0.000	0.000	0.000	0.000	0.000	0.000	0.000	2.500
CRT	0	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000
SP flash	2	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.132	0.000	0.000	0.000	0.000	0.000	0.000	0.132
SIO	1	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.132	0.000	0.000	0.000	0.000	0.000	0.000	0.132
OSC	4	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.264	0.000	0.000	0.000	0.000	0.000	0.000	0.264
LEDs	15	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.594	0.000	0.000	0.000	0.000	0.000	0.000	0.594
3.3->1.9V (Integrated in 82583)	1	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.878	0.000	0.000	0.000	0.000	0.000	0.000	0.878
3.3->1.05V (Integrated in 82583)	1	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.644	0.000	0.000	0.000	0.000	0.000	0.000	0.644
3.3->1.8V CPU	1	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	3.967	0.000	0.000	0.000	0.000	0.000	0.000	3.967
3.3V->1.8V ADIR	1	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.924	0.000	0.000	0.000	0.000	0.000	0.000	0.924
Total		47.70	0.00	8.93	6.47	11.03	0.51	5.40	2.51	11.03	0.51	0.20	2.16	2.12	1.03	0.50	
Power[W]																	
12V (including 90% efficiency)	51.66																
12V_AUX (including 90% efficiency)	12.26																
12V PCIe slot	0.00																
Total	63.91																
CPU power [W]																	
t> 2sec	35																
10ms<t<2s	45																
t<10mS	71																

Table 5: MGMT Board Power Consumption

15.1.3 System Power Consumption

Part	Power	Current	Comments
Fans	92.2	7.7	---
MNG Board	51.7	4.3	---
SWB	225.8 (with 36 LR4)	18.8	---
12V Total	369.6	30.8	From 460W
12V AUX MNG	12.3	1.0	---
12V AUX SWB	3.5	0.3	---
12 AUX Total	15.7	1.3	From 24W

Table 6: System Max Power Consumption

15.2 Power Monitoring and Distribution

15.2.1 Switch Board Power Monitoring and Distribution

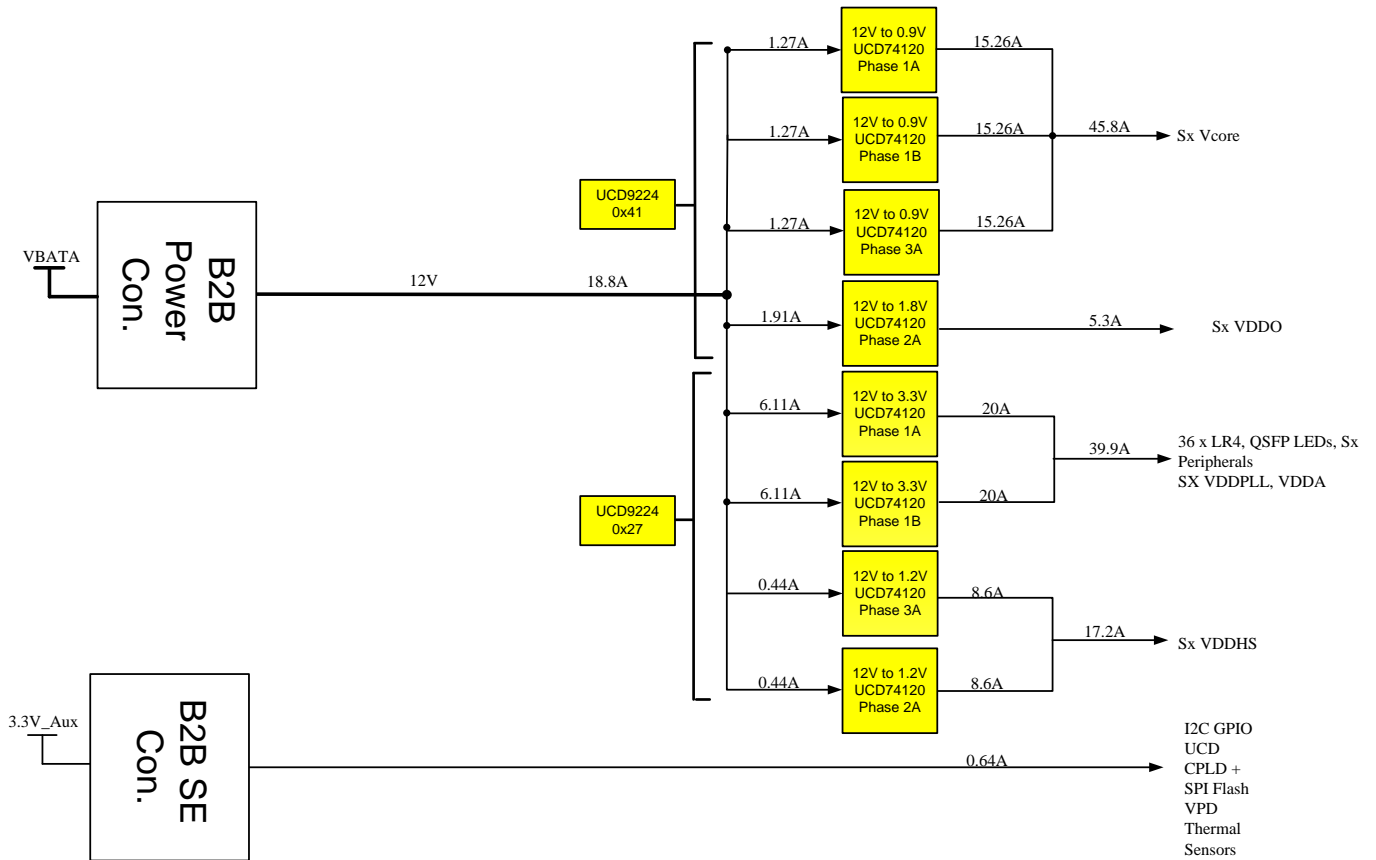


Figure 20: Switch Board Power Distribution

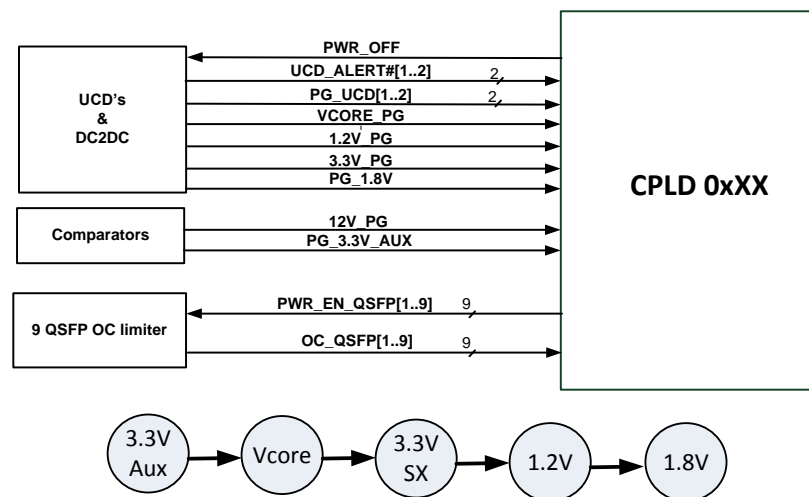


Figure 21: Switch Board Power Monitor and Power Sequence

15.2.2 MGMT Board Power Monitoring and Distribution

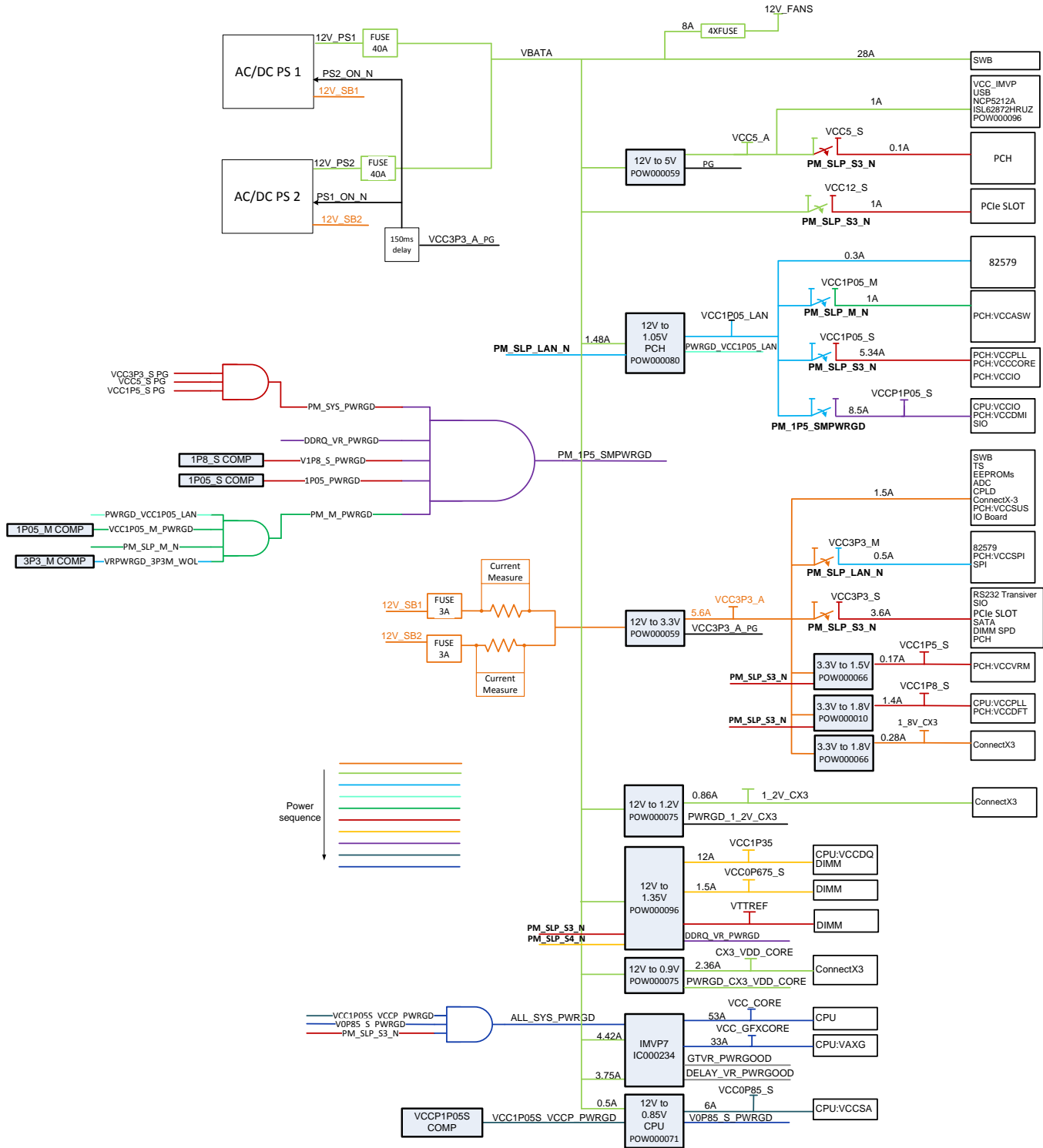


Figure 22: System and MGMT Board Power Distribution, Monitoring and Sequence

15.2.3 System and MGMT Board Voltages and Currents Sensing

Certain voltages and currents in the system can be read by SW/FW via an 8-channel I²C analog to digital converter. Voltage/current inputs to the A2D channels 2-7 are MUXed by 1:2 MUX. Therefore, two values can be read per channel. The MUX select signal is derived by the CPLD and can be controlled by SW and FW. The main 12V voltages and currents can be read directly from the AC/DC PS.

The following table describes the voltage rail in each channel and the expected reading.

The acceptable range for each rail is +/-10% from nominal value.

A/D Channel	MUX Select Signal	Monitored Voltage/Current		"B" Parameter
0	NA	DDR3 VTT 0.675V (VCC0P675_S)		0.008 (See note 2)
1	NA VCC0P85_S (See Note 1)	Rail Level	[VID0,VID1]	0.008 (See note 2)
		0.675	[1,1]	
		0.725	[1,0]	
		0.8	[0,1]	
		0.9	[0,0]	
2	0	12V_AUX1 (12VSB1 current)		0.008 (See note 2)
	1	12V_AUX2 (12VSB2 current)		0.008 (See note 2)
3	0	3.3V (VCC3P3_A)		0.016 (See note 2,3)
	1	5V (VCC5_A)		0.024 (See note 2,3)
4	0	CPU 1.8V (VCC1P8_S)		0.008 (See note 2)
	1	CX3 1.2V (1_2V_CX3)		0.008 (See note 2)
5	0	CPU/PCH 1.05V (VCC1P05_LAN)		0.008 (See note 2)
	1	CPU 1.5V (VCC1P5_S)		0.008 (See note 2)
6	0	CPU 1.05V (VCCP1P05_S)		0.008 (See note 2)
	1	CX3 1.8V (1_8V_CX3)		0.008 (See note 2)
7	0	DDR3 1.35V (VCC1P35)		0.008 (See note 2)
	1	CX3 0.9V (CX3_VDD_CORE)		0.008 (See note 2)

Table 7: A/D Channels

Notes:

1. This rail has 4 valid values controlled by the CPU, using 2 lines which are connected to the voltage regulator - VCCSA_SEL[0:1].
In order to allow the testing of all 4 levels in JTAG tests, these two controls are routed through the CPLD (CPLD_VCCSA_SEL[0:1]).
2. The B parameter is used to calculate the real voltage/current from I²C reading, using the following formula: $V=B \cdot R$, where V is the real voltage and R is the I²C reading.
3. This voltage is divided by voltage divider before it is sampled; therefore its B parameter contains the divider value as well.

16 FRUs

16.1 Power Supply Units

The system contains 2 power supplies – AC version (DPS-460KBJ_REV.03) with the following features:

- Input voltage: 100 to 240 VAC
- Frequency: 50 to 60 Hz
- Efficiency: 89 to 91% at 220V

[Table 8](#) describes the power supply connector pinout.

Pin #	Description	Pin #	Description
A1~9	GND	B1~9	GND
A10~18	+12V	B10~18	+12V
A19	PMBus SDA	B19	A0 (SMBus Address)
A20	PMBus SCL	B20	N/A
A21	PSON	B21	12VSB
A22	SMBAAlert#	B22	Smart)on
A23	Return Sense	B23	12VLS
A24	+12V Remote Sense	B24	No Connect
A25	PWOK	B25	N/A

Table 8: Power Supply Connector Pinout

16.2 Fan Units

The fan FRU is Delta Module P/N FA121A04-D40. [Table 9](#) describes the fan unit connector pinout. Figure 18 is a mechanical drawing of the unit.

Pin #	Description	Pin #	Description
1	12V	9	12V
2	12V	10	12V
3	Fan PWM	11	FAN TACH
4	Fan PWM	12	FAN TACH
5	GND	13	GND
6	GND	14	GND
7	FAN Present	15	I2C SCL
8	3.3V	16	I2C SDA

Table 9: Fan Unit Connector Pinout

16.3 FRU Control

The following figure describes the SX1710 FRU control.

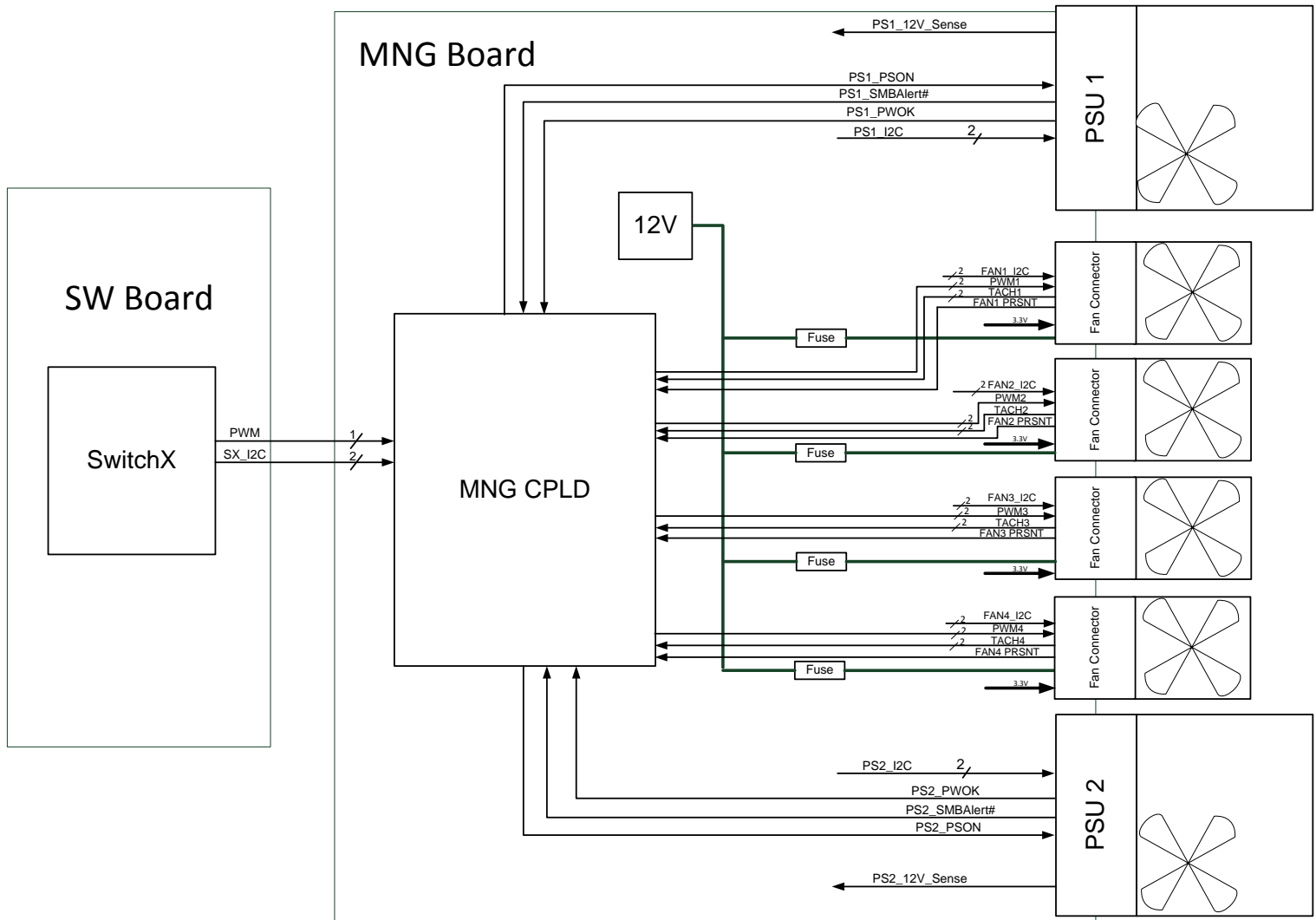


Figure 23: SX1710 FRU Control

16.3.1 Fan Control

The MGMT CPLD includes a fan controller that is controlled by the SwitchX FW. The fans' speed is controlled by 8 PWM signals from the MGMT CPLD to the fans, and they are monitored by 8 Tacho signals from the fans towards the CPLD.

PWM:

- One PWM output signal from SX is connected to the MGMT CPLD. This signal is reflected to all 8 fans by default.

Tacho:

- 8 Tacho RO registers are available via FW I²C (part of the FW register map)

Fan present signal can be monitored by SW and FW via FW and SW registers maps.

Inside the FRU the I²C is connected only to one EEPROM. FW and SW can access the fans I²C buses. For more info regarding the I²C connection to the fans FRUs, see I²C chapter.

16.3.2 PS Control

The PS is controlled via PMbus and a few signals. SW and FW can access the PMbus. For more information regarding the I²C connection to the PS, see [I²C](#).

PS fans can be controlled via the PMbus. As default, PS fans are controlled automatically by the PS. PS fans speed can be increased by FW/SW, but never reduced.

All other PS control signals can be controlled (for PS inputs) and monitored (for PS outputs) via FW and SW register maps.

17 Reset

The following table specifies the reset scenarios in the SX1710 system:

#	Cause	Source	Target	Description
1.	Power monitor circuit indication	CPLD	Entire board.	Power monitor circuit monitors that the local voltages are in the range of $\pm 10\%$ of the nominal value.
2.	External push button Short assertion	Push Button	Entire board.	User reset from panel. Assertion of more than $\frac{1}{2}$ sec and less than 12sec.
3.	External push button Long assertion	Push Button	Entire board.	User reset from panel. Restores CPU factory defaults. Assertion of more than 12sec. Supported only on managed systems.
4.	SW RST	SW	Entire board. The SW has the ability to reset specific components via its registers map.	SW request RST. Supported only on managed systems.
5.	FW RST	FW	Entire board. The FW has the ability to reset specific components via its registers map.	FW request RST
6.	WD expired	CPLD	Entire board. WD is disabled as default.	WD mechanism is implemented in the CPLD device. The CPU periodically writes counter value via LPC to 4 WD registers in the SW board 0xXX CPLD – if the CPLD does not recognize a counter value, change board reset is initiated. Supported only on managed systems.
7.	I ² C Reset request	FW	FW I ² C tree	FW request from CPLD to reset the internal I ² C switches. Asserted by dedicated GPIO from SwitchX.

Table 10: SX1710 Reset Matrix

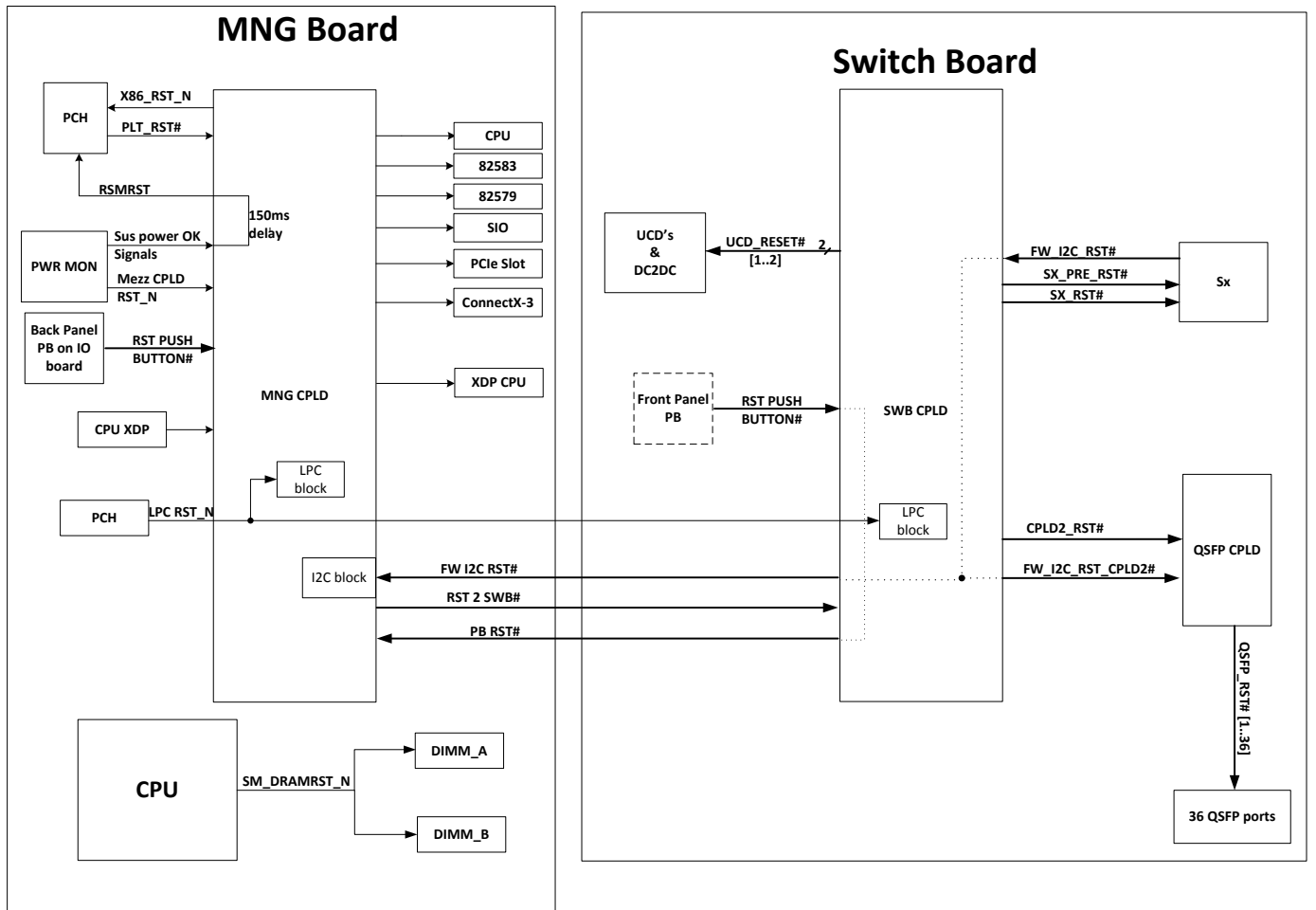


Figure 24: SX1710 Reset Mechanism

18 Temperature Monitor

The following temperature sensors can be read by SW or FW, or both:

- Two external sensors provide temperature sensing:
 - In front of the fan FRUs: sense the ambient temperature when fans are pushing air into the system (Air In system)
 - In front of the front panel: sense the ambient temperature when fans are sucking air from the system (Air Out system)
- SwitchX-2 has an internal temperature sensing diode. The temperature sensed by the diode is processed, and according to it, two signals may be asserted: Over Thermal Warning and Over Thermal Shutdown. The temperature above / below which these signals are activated /deactivated is controlled by firmware via the INI file, and it must be within the operational temperature range of the device.
- The CPU has an internal sensor that can be monitored only by SW. The CPU can reduce its power (the performance might be reduced as well) in order to prevent from reaching the maximum T_j value.
- The PCH has an internal sensor that can be monitored only by SW.
- Each SODIMM has on module thermal sensor that can be monitored only by SW.

19 Clocks

19.1 Switch Board Clocks

[Figure 25](#) describes the switch board clock distribution.

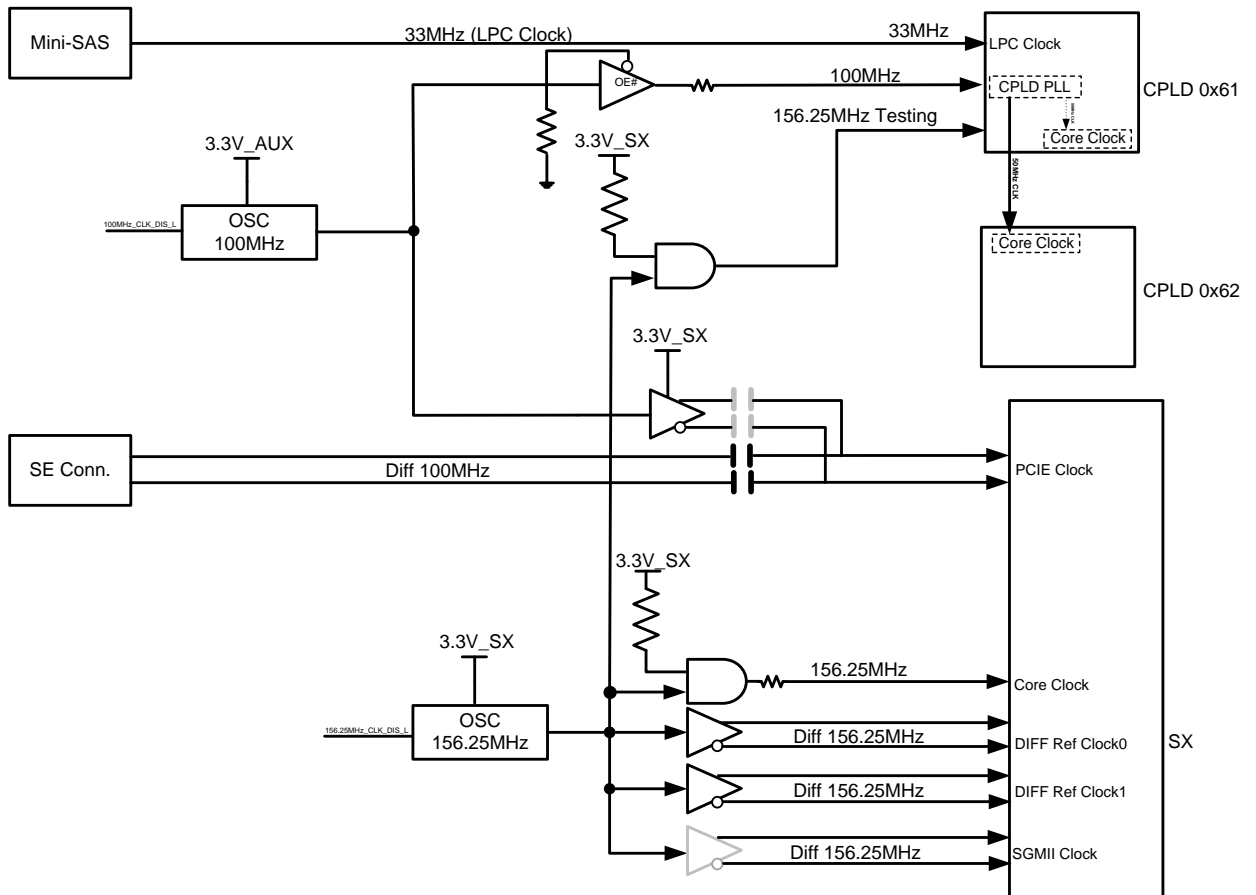


Figure 25: Switch Board Clock Distribution

19.2MGMT Board Clocks

Most of the MGMT board clocks are generated from two crystals and distributed by the PCH. In addition, one 25MHz oscillator is buffered and distributed to the ETH PHYs and to the CPLD. The ConnectX3 156.25MHz is generated by additional oscillator.

The ConnectX3 and the PCIe slot are connected to GEN3 supported clocks (PCIe clocks A and B). The rest of the PCIe components are connected to GEN2 clocks. In case a GEN3 connection with the switch board is required, a GEN 3 clock source on the switch board will be needed.

[Figure 26](#) describes the clock distribution in the MGMT board.

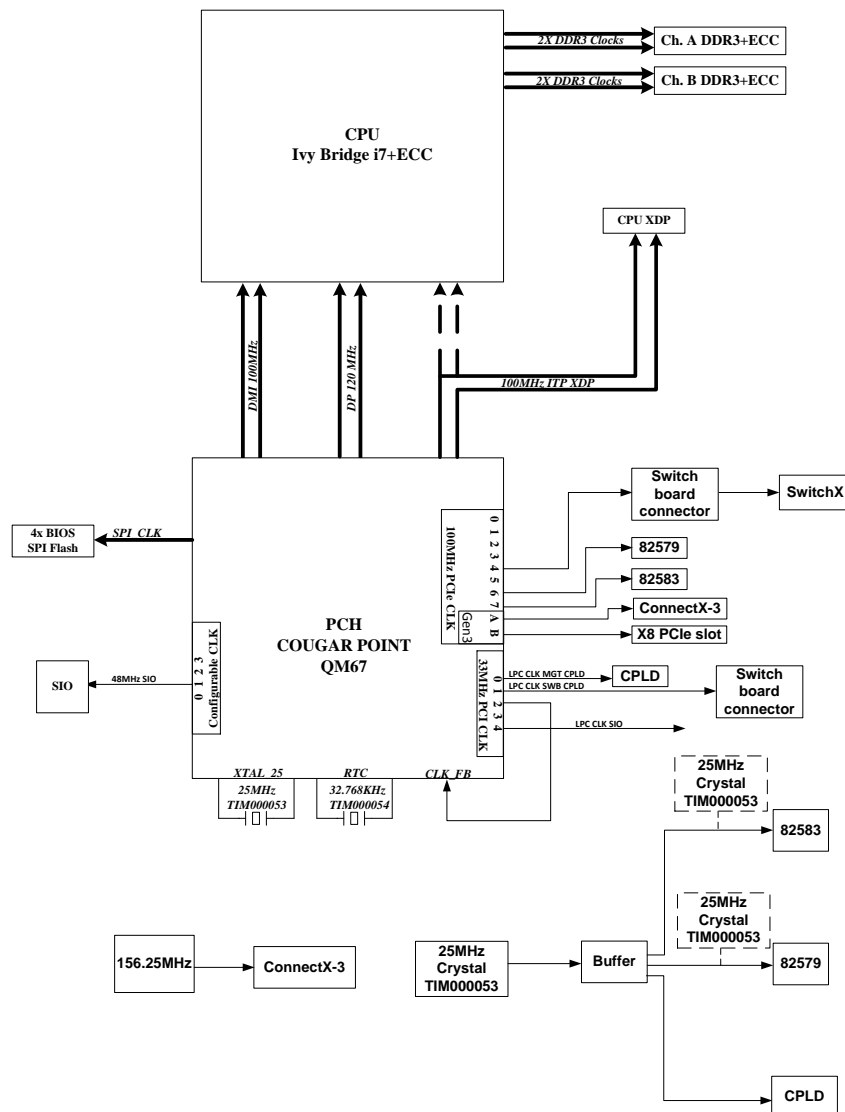


Figure 26: MGMT Board Clock Distribution

20 LEDs

The following table describes the SX1710 indication LEDs.

LED	Qty.	Color	Description		Originator	Driver	Location
Status LED	1	Red/ Green/ Yellow	Off – No power Solid Red – Fault Solid Green – Normal operation Blinking Green – Boot Solid Yellow – Error		CPU via LPC I/F towards MNG Board CPLD or SW Board 0xXX CPLD or MNG Board CPLD	MNG Board CPLD	On Ports Side and on IO Board
General Fans LED	1	Red/ Green	Off – No power Green – All fans operating Red – Fan failure		MNG Board CPLD	SW Board CPLD	On Ports Side
Fans 1-4 LEDs	4	Red/ Green	Off – No power Green – Fan# is operating Red – Fan failure		MNG Board CPLD	MNG Board CPLD	IO Board
UID LED	1	Blue	Static – The operator has activated this LED to identify this module. Blinking – The Operator is instructing to replace this module		CPU via LPC I/F toward SW Board CPLD	SW Board CPLD	Ports Side LED Board
Bad Port indication	1	Green / Yellow	Blinking yellow – Bad port indication		SwitchX-2	SW Board CPLD	Ports Side LED Board
PSU LED	1	Green/ Red	Green – Both PSU OK Red –PSU is Faulty		MNG Board CPLD according to PSU indications	SW Board CPLD	Ports Side LED Board
PSU LED	1 per PS FRU	Green / Amber	Output ON and OK	GREEN	PS	PS	PS FRU
			No AC power to all power supplies	OFF			
			AC present / Only 12VSB on (PS off) or PS in Smart on state	1Hz Blink GREEN			
			AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input	AMBER			

			power.				
			Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink Amber			
			Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	AMBER			
			Power Supply FW updating	2Hz Blink GREEN			

Table 11: SX1710 LEDs

21 JTAG

The system's MGMT board has standalone JTAG support; in addition, the system allows JTAG support via a special fan FRU, while the top cover is assembled.

In order to connect to the MGMT JTAG chain, a special extension card is required (no on-board connectors).

For lab CPLD burning, a few jumpers might have to be assembled, depending on the board and on the system structure. For CPLD JTAG chain, please refer to [CPLD](#).

The SwitchX chain and the MGMT board chain are described in the following figure.

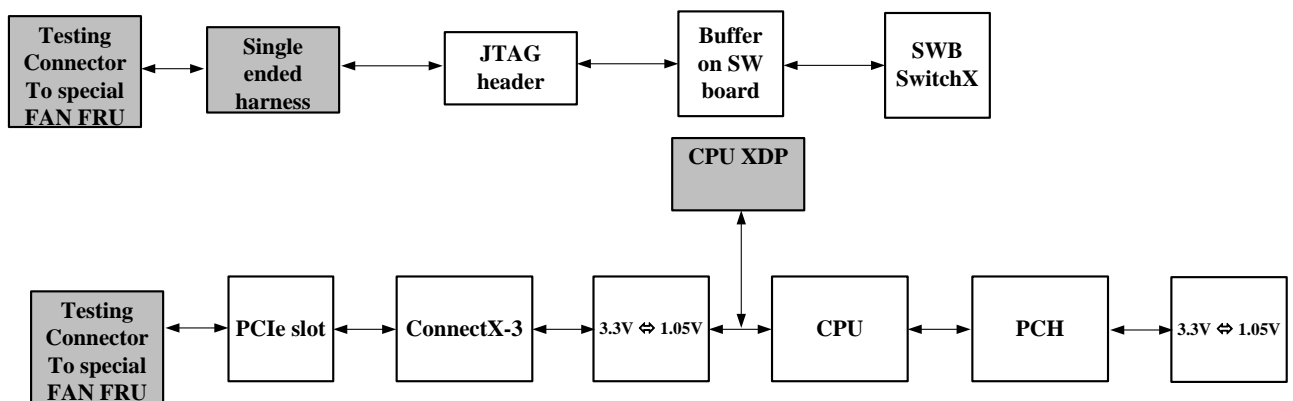


Figure 27: MGMT Board and Switch Board JTAG Chains

21.1 Testing I²C GPIO

Each of the two boards has a dedicated I²C GPIOs for testing. This GPIO is for use only during JTAG tests. The CPLD emulates I²C (using JTAG) to control this GPIO.

The GPIO allows control on critical signals during the JTAG test.

In addition, the I²C GPIO on the MGMT board is connected to the "Safe BIOS" mechanism. This will allow switching between the 2 sets of SPI flash (Know Good Image and Current Image) without the need of a jumper during the burning process.

22 Compliance

- Shock & Vibration: ETSI EN 300 019-2-2: 1999-09
- Humidity operating: 5% - 95% non-condensing
- Operating temperature 0C-45C
- Safety:
 - US/Canada: cTUVus
 - EU: IEC60950
 - International: CB
 - CCC
- EMC (Emissions):
 - USA: FCC, Class A
 - Canada: ICES, Class A
 - EU: EN55022, Class A
 - EU: EN55024, Class A
 - EU: EN61000-3-2, Class A
 - EU: EN61000-3-3, Class A
 - Japan: VCCI, Class A
- Environmental
 - EU: IEC 60068-2-64: Random Vibration
 - EU: IEC 60068-2-29: Shocks Type I /II
 - EU: IEC 60068-2-32: Fall Test
- Acoustics:
 - ISO 7779
 - ETS 300 753