

|  |
| --- |
| QuantaGrid D51B-1U |
| *Revision 1.0* |
| ***2015/11/4*** |

Contributed by : Alan Chang. Quanta Computer Inc.

**Revision History:**

|  |  |  |
| --- | --- | --- |
| **Revision** | **Date** | **Description** |
| 1.0 | 2015-11-04 | Release for Open Compute Project |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

**Table of Contents**

[1 INTRODUCTION 4](#_Toc434430722)

[2 PRODUCT ARCHITECTURE OVERVIEW 5](#_Toc434430723)

[2.1 PRODUCT ARCHITECTURE BLOCK DIAGRAM 7](#_Toc434430724)

[2.2 BASEBOARD PLACEMENT 8](#_Toc434430725)

[2.3 BASEBOARD Diemesion 9](#_Toc434430726)

[3 PRODUCT FEATURES 10](#_Toc434430728)

[3.1 PROCESSOR 10](#_Toc434430729)

[3.2 MEMORY 10](#_Toc434430730)

[3.2.1 DIMM NOMENCLATURE 10](#_Toc434430731)

[3.3 PCH 11](#_Toc434430732)

[3.3.1 PCH GPIOs 12](#_Toc434430733)

[3.4 BMC 18](#_Toc434430734)

[3.4.1 AST2400 (Default) 18](#_Toc434430735)

[3.5 CLOCKS 18](#_Toc434430736)

[3.6 SATA 19](#_Toc434430737)

[3.6.1 SATA PORT CONNECTIVITY 19](#_Toc434430738)

[3.7 USB 20](#_Toc434430739)

[3.8 PCIe BUS 21](#_Toc434430740)

[3.8.1 PCIe PORT CONNECTIVITY 21](#_Toc434430741)

[3.9 PCIe Interface 22](#_Toc434430742)

[3.9.1 Riser Slot PINOUT 23](#_Toc434430743)

[3.10 LAN ON MOTHERBOARD (LOM) 34](#_Toc434430744)

[3.10.1 DEDICATED NIC (MANAGEMENT RJ45 Port) 34](#_Toc434430745)

[3.11 LPC BUS 34](#_Toc434430746)

[3.12 TPM 34](#_Toc434430747)

[3.13 SERIAL PORT 34](#_Toc434430748)

[3.14 FANs 35](#_Toc434430749)

[3.15 Jumper Definition 36](#_Toc434430750)

[3.16 DEBUG header Information 40](#_Toc434430758)

[3.16.1 XDP SUPPORT 40](#_Toc434430759)

[3.16.2 SMB Debug Header (JP7) 40](#_Toc434430760)

[3.16.3 BMC Debug Header (JP2 and J19) 40](#_Toc434430761)

[3.17 PRODUCT SENSORS 41](#_Toc434430762)

[3.18 SMBUS 42](#_Toc434430763)

[3.18.1 SMBUS ARCHITECTURE 42](#_Toc434430764)

[3.19 POWER 43](#_Toc434430765)

[3.19.2 Power supply PINOUT 44](#_Toc434430766)

[4 PRODUCT SYSTEM REQUIREMENTS 47](#_Toc434430767)

[4.1 Chassis Overview 47](#_Toc434430768)

[4.2 LED behavior 49](#_Toc434430769)

[4.2.1 Front Panel LED Function and Behavior 49](#_Toc434430770)

# INTRODUCTION

The S2B will be IA-64 based dual-socket servers that support the Grantley –EP processors in combination with the Wellsburg PCH (PCH) to provide a balanced feature set between technology leadership and cost. Quanta Grantley will be 24 DIMM and three x16 risers,

The intended audiences for this document are the Grantley platform technical leads, software team, validation team, and board design engineers that need to utilize a comprehensive package. This document will provide the S2B Design Teams the product specific features that are required to be implemented on the boards. Product feature requirements and block diagrams will be provided.

Links to reference documents that dive into the implementation for the software stack, common-core solution, server management architecture, fan-speed control architecture, chassis, power budget, and thermal requirements are provided.

# PRODUCT ARCHITECTURE OVERVIEW

The S2B 24 DIMMs Server board will be Quanta Grantley server product. The silicon ingredients and features are as follows list:

**Table 2‑1. Grantley Enterprise Server S2B Feature List**

|  |  |
| --- | --- |
| **Board Name** | **Grantley Server Baseboard** |
| Form Factor | 2U Rack (X2M chassis)/ 720mm x 430mm x 87.5mm/ 28.34" x 16.92" x 3.4"  1U Rack (X1S chassis) / 720mm x 430mm x 43.5mm/ 28.34" x 16.92" x 1.7" |
| Baseboard size | 16.7” x 16”, 8 layer, 2.4mm, 24 DIMMs |
| CPU | Intel Haswell E5-2600V3, -R3 Socket |
| Max Processor Wattage | 145W, Optimized power delivery for 95W, VRD 12.5 |
| QPI Speed | 9.6 GT/s, 8.0GT/s, 6.4GT/s |
| Chipset | Intel (R) C610 series chipset (Wellsburg) |
| Memory | ECC RDIMM/ LRDIMM slots Up to 768GB (32Gx24) of memory for LRDIMM Up to 768GB (32Gx24) of memory for RDIMM |
| PCIe Expansion Slot | **1U Chassis**  (1) PCIe x16 G3 riser slot for low-profile card (By Riser1) (1) PCIe x16 G3 riser slot for full height card (By Riser2) (1) PCIe x8 G3 OCP mezzanine card slot  **2U Chassis**   1. PCIe x8 G3 riser slot for low-profile card + (1) PCIe x8 G3 Linking slot for   low-profile card (By Riser1, Default)   1. PCIe x16 G3 riser slot for low-profile card + (1) PCIe x8 G3 riser slot for   low-profile card (By Riser1, Option)   1. PCIe x16 G3 riser slot for full height card + (1) PCIe x8 G3 riser slot for   Full height card (By Riser2) (1) PCIe x8 G3 OCP mezzanine card slot |
| Rear IO | (2) USB 3.0 ports (1) VGA port (BMC AST2400 SKU only) (1) RS232 serial port (2) GbE or 10G BASE-T RJ45 ports (1) GbE RJ45 management port (1) ID LED  (1) Port80 Debug Port (option) |
| Front IO | Power/ID/Reset Buttons, LEDs  (2) USB 2.0 ports |
| Network | Powerville Dual GbE: (2 MACs and 2 PHYs Integrated)  Twinville Dule 10GbE (Option)  PHY RTL8211 to BMC for delicate management NIC port. |
| Storage | (24) 2.5" or (12) 3.5" SATA/SAS hot-plug drives (2U Chassis) (10) 2.5" or (4) 3.5" SATA/SAS hot-plug drives (1U Chassis)  (2) SATADOM (optional) (2) 2.5" hot-plug SAS or PCIe SSDs (optional) |
| USB | Two USB3.0 ports on Rear  Two USB2.0 ports on Front panel (Option) |
| Video | ASPEED AST2400 8MB DDR3 video memory |
| Series Port | One external serial port on Rear  One internal serial port (Option) |
| FAN | 1U 6 dual-rotor FAN connectors from HDD backplane.  2U 4 dual-rotor FAN connectors on motherboard |
| ACPI | ACPI compliance, S0, S5 support. (\* No S1 and S3 support.) |
| TPM | Yes (Option) |
| Power-Supply | (2) 1100W high efficiency redundant PSU, 100-240VAC 50/60Hz (2U Chassis)  Or (2) 750W high efficiency redundant PSU, 100-240VAC 50/60Hz (1U Chassis) |
| Chassis | 1U system / 2U system |

## PRODUCT ARCHITECTURE BLOCK DIAGRAM

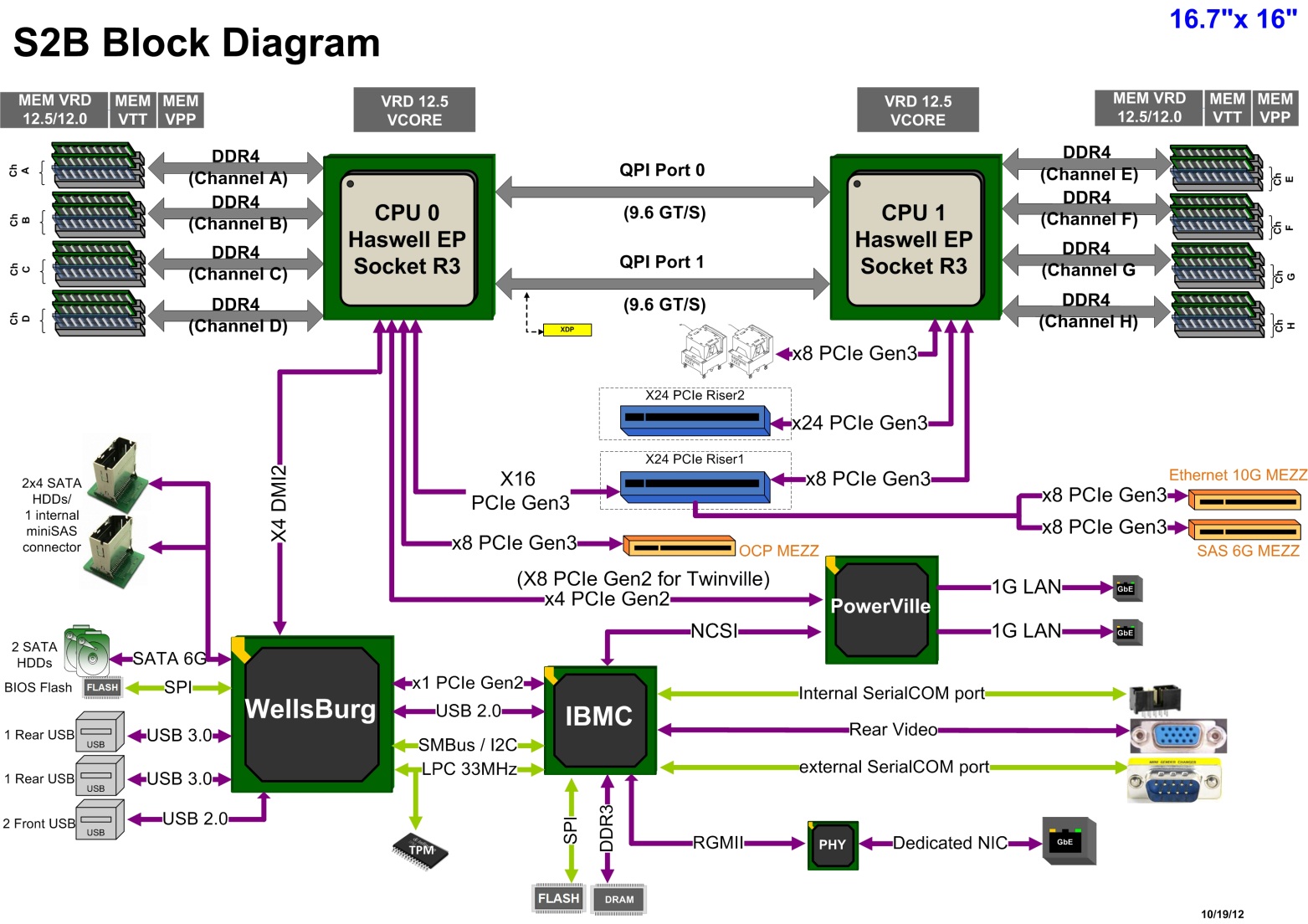


Figure 2-1 Grantley Enterprise Rack S2B Configuration

## BASEBOARD PLACEMENT

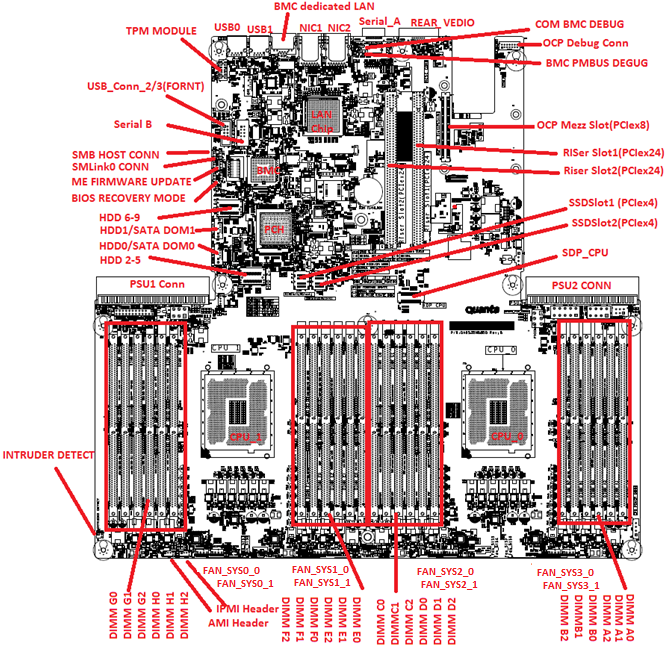


Figure 2-2: Quanta Grantley 2S 24-DIMM S2B Baseboard Placement

## BASEBOARD Diemesion

W 425mm (16.7 “) x L 406mm (16”)

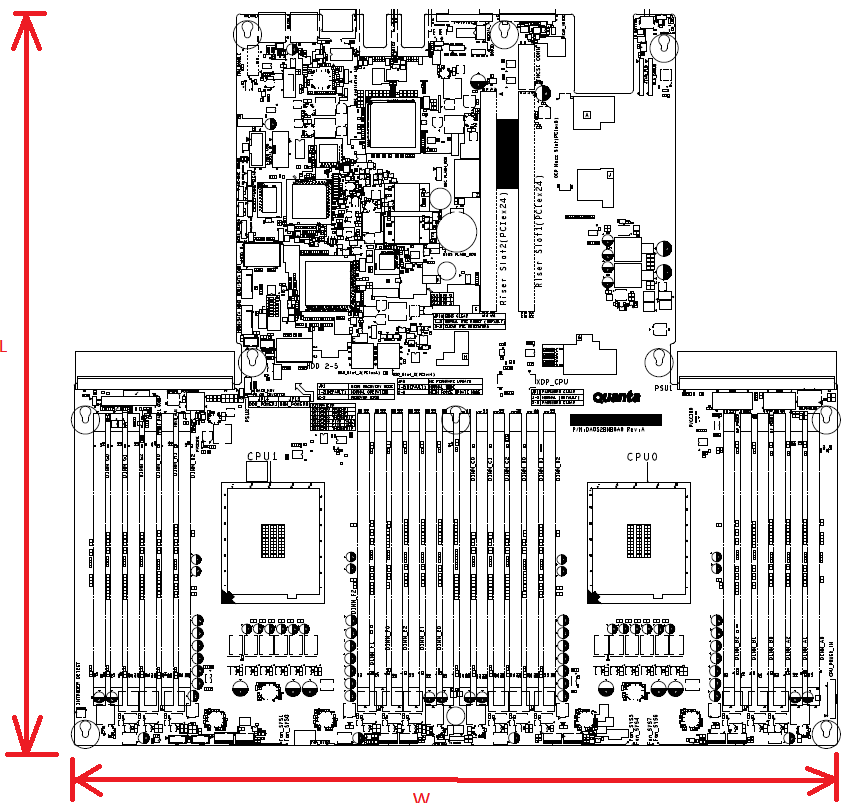


Figure 2-3: Quanta Grantley 2S 24-DIMM S2B BaseBoard Dimension

# PRODUCT FEATURES

## PROCESSOR

The Processor’s core name of Grantley platform is named “Haswell EP Processor- E5-2600V3”. It is 22nm process Processor with new Microarchitecture and New Instructions (including AVX 2.0). And the processor supports 4 DDR4 Memory channels. The QPI bus speed has improved up to 9.6GT/s. In this generation, the processor has internal voltage regulator (IVR), IVR integrates legacy power delivery onto processor package/die. So IVR enables power management benefits and simplified platform power design.

## MEMORY

Quanta Grantley Server board S2B support total 24 DDR4 DIMMs.

### DIMM NOMENCLATURE

DIMMs are organized into physical slots on DDR4 memory channels that belong to processor sockets. The memory channels from Socket 0 (CPU-0) are identified as Channel A, B, C, D. The memory channels from Socket 1 (CPU-1) are identified as Channel E, F, G and H.

The DIMM identifiers on the silkscreen on the board provide information about the channel, and therefore the processor, to which they belong. For example, DIMM\_A0 is the first slot on Channel A of processor 0; DIMM\_E0 is the first DIMM socket on Channel A of processor 1.

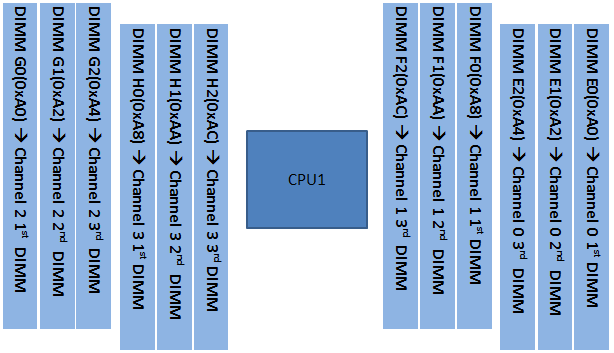
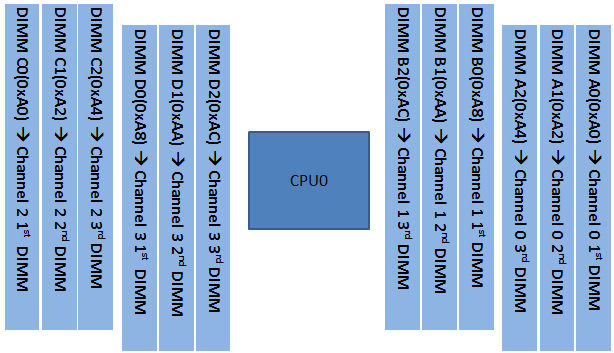
 

Figure 3-1 processor SKU list

## PCH

The PCH’s core name of Grantley platform is named “Wellsburg”.

**Wellsburg Key Features**:

* + Optimized and Validated to work with Haswell Server CPUs
  + Integrated system clocks w/ support for ext. clock buffers
  + Reduced TDP / Average Power/ Package (vs. Patsburg)
  + Intel® SVT / Dengate\* support capable
  + USB3 XHCI Debug Device required for Windows8
  + Flexible Management Infrastructure focused on Run Time
  + Support for MCTP Protocol and End Points
  + Support for Management traffic over DMI
  + Embedded Platform SW Services capability
  + 6x SMBus; 1@ 1MHz bus support for LAN or BMC
  + SPI Enhancements (large enough address space for 2 BIOS)
  + Continued support for GSX (GPIO Expansion slots)
  + 10 SATA ports capable of 6Gb/s
  + Up to 6 ports of USB3; 8 ports of USB2
  + Up to 8 x1 PCIe G2
  + Intel ® Node Manager 3.0 (with BE, EE options)
  + vPro/AMT
  + RSTe SW RAID (optional DSS SSD caching capability)

### PCH GPIOs

**Table 3‑3. PCH GPIOs List**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Item** | **Pin Name** | **Signal Name** | **Usage** | **Strapping** | **In/Out** |
| GPIO0 | BMBUSY\_N\_GPIO0 | PU\_PCH\_GPIO0 | No used and PU to P3V3 |  | In |
| GPIO1 | TACH1\_GPIO1 | REVISION\_ID1 | REVISION\_ID1 |  | In |
| GPIO2 | PIRQE\_N\_GPIO2 | FM\_CPU\_ERR0\_CO\_N | Error seen signaling from CPU |  | In |
| GPIO3 | PIRQF\_N\_GPIO3 | FM\_ERR1\_DLY\_N | Error seen signaling from CPLD (Delay) |  | In |
| GPIO4 | PIRQG\_N\_GPIO4 | PU\_PIRQG\_N | No used and PU to P3V3 |  | In |
| GPIO5 | PIRQH\_N\_GPIO5 | IRQ\_CPU\_CATERR\_DLY | CATERR\_N RC delay |  | In |
| GPIO6 | TACH2\_GPIO6 | TP\_BOARD\_ID0 | NA |  | In |
| GPIO7 | TACH3\_GPIO7 | TP\_BOARD\_ID1 | NA |  | In |
| GPIO8 | GPIO8 | IRQ\_BMC\_PCH\_NMI\_N\_MUX | NMI form BMC | **Integrated Clock Chip Enable / Disable**  0 = Enable Integrated Clock Chip mode. 1 = Disable Integrated Clock Chip mode.[Default] | In |
| GPIO9 | OC5\_N\_GPIO9 | FP\_PWR\_LED\_N | Turn on PWR LED on FP |  | Out |
| GPIO10 | OC6\_N\_GPIO10 | FM\_TPM\_PRSNT\_N | Detect TPM |  | In |
| GPIO11 | SMBALERT\_N\_GPIO11 | RST\_PCIE\_CPU\_N |  |  | Out |
| GPIO12 | LAN\_PHY\_PWR\_CTRL\_GPIO12 | IRQ\_IBMC\_PCH\_SMI\_LPC\_N | SMI from BMC |  | In |
| GPIO13 | GPIO13 | FM\_IBMC\_PCH\_SCI\_LPC\_N | SCI from BMC |  | In |
| GPIO14 | OC7\_N\_GPIO14 | PU\_USB\_OC7\_R\_N | No used and PU to P3V3\_AUX |  | In |
| GPIO15 | GPIO15 | FM\_PCH\_SATA\_RAID\_KEY | SATA RAID KEY |  | In |
| GPIO16 | SATA4GP\_GPIO16\_MGPIO9 | FM\_THROTTLE\_N | THROTTLE |  | Out |
| GPIO17 | TACH0\_GPIO17 | REVISION\_ID0 | REVISION\_ID0 |  | In |
| GPIO18 | GPIO18 | PU\_PCH\_GPIO18 | No used and PU to P3V3 |  | In |
| GPIO19 | SATA1GP\_GPIO19 | RST\_PCIE\_PCH\_N | Reset PCIE | **Boot BIOS Strap bit 0** Bit1 Bit0 Boot BIOS Destination 0 1 Reserved 1 0 RSVD 1 1 SPI [Default] 0 0 LPC | In |
| GPIO20 | GPIO20\_SMI\_N | PU\_PCH\_GPIO20 | No used and PU to P3V3 |  | Out |
| GPIO21 | SATA0GP\_GPIO21 | PD\_SATA0GP\_GPIO21 | No used and PD to GND |  | In |
| GPIO22 | SCLOCK\_GPIO22 | SGPIO\_SATA\_CLOCK\_R | SGPIO SATA CLOCK |  | Out |
| GPIO23 | LDRQ1\_N\_GPIO23 | TP\_PCH\_LDRQ1\_N | No used and TP |  | In |
| GPIO24 | GPIO24\_MGPIO0 | PU\_PCH\_GPIO24 | No used and PU to P3V3\_AUX |  | In |
| GPIO25 | GPIO25 | FM\_PCH\_LAN0\_DISABLE\_N | DISABLE LAN |  | Out |
| GPIO26 | GPIO26 | PU\_PCH\_GPIO26 | No used and PU to P3V3\_AUX |  | In |
| GPIO27 | GPIO27\_MGPIO6 | FM\_VIDEO\_DISABLE\_N | Video output enable/disable  indicate from PCH |  | Out |
| GPIO28 | GPIO28\_MGPIO7 | FM\_USB\_EN\_N | Enable USB PWR |  | Out |
| GPIO29 | SLP\_WLAN\_N\_GPIO29\_MGPIO3 | PU\_PCH\_GPIO29 | No used and PU to P3V3\_AUX |  | In |
| GPIO30 | SUSWARN\_N\_GPIO30\_MGPIO1 | PU\_PCH\_GPIO30 | No used and PU to P3V3\_AUX |  | In |
| GPIO31 | GPIO31\_MGPIO2 | IRQ\_SML1\_PMBUS\_ALERT\_N | PMBus Alert from PSU1 and PSU2 |  | In |
| GPIO32 | GPIO32 | PU\_PCH\_GPIO32 | No used and PU to P3V3 |  | In |
| GPIO33 | GPIO33 | FM\_QPI\_SLOW\_MODE\_N | QPI SLOW MODE SELECT | **DMI TX Termination** 0 = DMI TX is terminated to VSS. 1 = DMI TX is terminated to VCC. [Default] | In |
| GPIO34 | GPIO34 | OCP\_MEZZA\_PRSNT\_N | Detect OCP MEZZA |  | In |
| GPIO35 | GPIO35\_NMI\_N | FM\_NMI\_EVENT\_2\_N | Inform BMC NMI EVENT |  | In |
| GPIO36 | SATA2GP\_GPIO36 | FM\_BIOS\_ADV\_FUNCTIONS | BIOS ADVANCED FUNCTIONS | **DMI RX Termination** 0 = DMI RX is terminated to VSS.  1 = DMI RX is terminated to common mode. [Default] | In |
| GPIO37 | SATA3GP\_GPIO37 | PU\_ADR\_TRIGGER\_N | TLS CONFIDENTIALITY ENABLE | **TLS Confidentiality** 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality) [Default] | In |
| GPIO38 | SLOAD\_GPIO38 | SGPIO\_SATA\_LOAD\_R | SGPIO SATA LOAD |  | Out |
| GPIO39 | SDATAOUT0\_GPIO39 | SGPIO\_SATA\_DATAOUT0\_R | SGPIO SATA DATAOUT0 |  | Out |
| GPIO40 | OC1\_N\_GPIO40 | FM\_USB\_OC1\_BP\_R\_N | USB OVER CURRENT |  | In |
| GPIO41 | OC2\_N\_GPIO41 | PU\_USB\_OC2\_R\_N | No used and PU to P3V3\_AUX |  | In |
| GPIO42 | OC4\_N\_GPIO42 | ROMA<0> | Disable BMC |  | Out |
| GPIO43 | OC4\_N\_GPIO43 | FM\_USB\_OC4\_FP\_R\_N | USB OVER CURRENT |  | In |
| GPIO44 | GPIO44 | FM\_PCH\_LAN1\_DISABLE\_N | DISABLE LAN |  | Out |
| GPIO45 | GPIO45 | RST\_PCH\_IBMC\_N | RST BMC |  | Out |
| GPIO46 | GPIO46 | FM\_BIOS\_POST\_CMPLT\_N | For BIOS to indicate POST status to BMC |  | In |
| GPIO47 | GPIO47 | FM\_BMC\_READY\_N | BMC ready indicate to PCH |  | In |
| GPIO48 | SDATAOUT1\_GPIO48 | SGPIO\_SATA\_DATAOUT1\_R | SGPIO SATA DATAOUT1 |  | Out |
| GPIO49 | SATA5GP\_GPIO49\_MGPIO10 | FM\_CPU\_PROCHOT\_N | Detect CPU PROCHOT |  | In |
| GPIO50 | GPIO50\_GSXCLK | FM\_RISER2\_CFG1 | Riser2 PCIE configuration |  | In |
| GPIO51 | GPIO51\_GSXDOUT | PD\_SGPIO\_GSX\_DOUT | No used and PD to GND | **Boot BIOS Strap bit 1** Bit1 Bit0 Boot BIOS Destination 0 1 Reserved 1 0 RSVD 1 1 SPI [Default] 0 0 LPC | In |
| GPIO52 | GPIO52\_GSXSLOAD | FM\_RISER2\_CFG0 | Riser2 PCIE configuration |  | In |
| GPIO53 | GPIO53\_GSXDIN | PD\_SGPIO\_GSX\_MUX\_DIN | No used and PD to GND | **DMI AC Coupling** 0= Configures DMI for AC coupling mode.  1 = Configures DMI for DC coupling mode. [Default] | In |
| GPIO54 | GPIO54\_GSXSRESET\_N | FM\_RISER1\_CFG0 | Riser1 PCIE configuration |  | In |
| GPIO55 | GPIO55 | PU\_PCH\_GPIO55 | No used and PU to P3V3 | **Top-Block Swap Override** 0 = Enable “Top-Block Swap” mode - PCH will invert A16 for cycles going to the upper two 64 KB blocks in the FWH or appropriate address lines (A16, A17, A18, A19 or A20) as selected in BIOS Boot-Block size soft strap for SPI. 1 = Disable “Top-Block Swap” mode.. [Default] | In |
| GPIO56 | GPIO56 | FM\_BIOS\_RCVR\_BOOT\_N | BIOS RECOVERY MODE |  | In |
| GPIO57 | GPIO57\_MGPIO5 | FM\_ME\_RCVR\_N | ME FIRMWARE UPDATE |  | in |
| GPIO58 | SML1CLK\_GPIO58\_MGPIO11 | SMB\_3V3SB\_PMBUS\_CLK\_R | SM bus CLK |  | Out |
| GPIO59 | OC0\_N\_GPIO59 | PU\_USB\_OC0\_R\_N | No used and PU to P3V3 |  | In |
| GPIO60 | SML0ALERT\_N\_GPIO60\_MGPIO4 | IRQ\_SML0ALERT\_N | SM bus Alert to BMC |  | Out |
| GPIO61 | SUS\_STAT\_N\_GPIO61 | PU\_PCH\_GPIO61 | CPLD JTAG TDI |  | Out |
| GPIO62 | SUSCLK\_GPIO62 | CLK\_33K\_SUSCLK | CLK 33MHZ | **PLL On-Die Voltage Regulator Enable** 0 = Disable PLL On-Die voltage regulator. 1 = Enable PLL On-Die voltage regulator.[Default] | Out |
| GPIO63 | SLP\_S5\_N\_GPIO63 | PU\_SLP\_S5\_N | No used and reserve a PU to P3V3\_AUX |  | Float |
| GPIO64 | CLKOUTFLEX0\_GPIO64 | FM\_RISER1\_CFG1 | Riser1 PCIE configuration |  | In |
| GPIO65 | CLKOUTFLEX1\_GPIO65 | SLOT3\_PRESENT\_N | Detect SLOT3 |  | In |
| GPIO66 | CLKOUTFLEX2\_GPIO66 | SLOT2\_PRESENT\_N | Detect SLOT2 |  | In |
| GPIO67 | CLKOUTFLEX3\_GPIO67 | SLOT1\_PRESENT\_N | Detect SLOT1 |  | In |
| GPIO68 | TACH4\_GPIO68 | TP\_BOARD\_ID2 | NA |  | In |
| GPIO69 | TACH5\_GPIO69 | TP\_BOARD\_ID3 | NA |  | In |
| GPIO70 | TACH6\_GPIO70 | TP\_BOARD\_ID4 | NA |  | In |
| GPIO71 | TACH7\_GPIO71 | TP\_BOARD\_ID5 | NA |  | In |
| GPIO72 | GPIO72 | PU\_PCH\_GPIO72 | No used and PU to P3V3\_AUX |  | In |
| GPIO73 | GPIO73 | PU\_PCH\_GPIO73 | No used and PU to P3V3\_AUX |  | In |
| GPIO74 | SML1ALERT\_N\_PCHHOT\_N\_GPIO74\_MGPIO8 | FM\_PCH\_BMC\_THERMTRIP\_N | PCH HOT indicate |  | Out |
| GPIO75 | SML1DATA\_GPIO75\_MGPIO12 | SMB\_3V3SB\_PMBUS\_DAT\_R | SM bus DATA |  | Bi |
| HDA\_SDO | HDA\_SDO | AUD\_AZA\_SDO | Reserve PU to P3V3\_AUX | **Flash Descriptor Security Override** 0 = Enable security measures defined in the Flash Descriptor. [default] 1 = Disable Flash Descriptor Security (override). | Out |
| INTVRMEN | INTVRMEN | PU\_PCH\_INTVRMEN | Enable internal VRM | Integrated VRM Enable 0 = Disable 1 = Enable [Default] | In |
| DSWVRMEN | DSWVRMEN | PU\_PCH\_DSWODVREN | Deep Sx Well On-Die Voltage Regulator Enable | **Deep Sx Well On-Die Voltage Regulator Enable** 0 = Disable Integrated DeepSx Well (DSW) On-Die Voltage  Regulator.  1 = Enable DSW 3.3V-to-1.05V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. [Default] | In |
| SPKR | SPKR | SPEAKER\_PCH | Control speaker | **No Reboot** 0 = Disable “No Reboot” mode. 1 = Enable “No Reboot” mode. [Default] | Out |
| MEXP\_SMBDATA0 | MEXP\_SMBDATA\_0 | SMB\_MEXP\_SMBDATA\_0 | SMB SDA | **ADR Timer Hold off** 0 = Enable 1 = Disable [Default] | I/OD |
| MEXP\_SMBDATA1 | MEXP\_SMBDATA\_1 | PU\_MEXP\_SMBDATA\_1 | SMB SDA | **LT Key Downgrade** 0 = Enable 1 = Disable [Default] | I/OD |

## BMC

There are 2 BMC options on the S2B Mainboard – AST2400 which include VGA interface.

### AST2400 (Default)

The Server’s Board Management Controller (**AST2400**) is a highly integrated single-chip solution, integrating several devices typically found on servers.

## CLOCKS

The Grantley platform has two different clock architectures, external clock architecture (exCLK) and integrated system clock (isCLK) architecture. The Wellsburg PCH is capable of providing both exCLK and isCLK. S2B will use Hybrid clock mode. The external clock generator is not needed. There is a clock generator is from PCH internal and an external clock buffer.



Figure 3-4: Grantley Product System Clock Diagram

## SATA

The Wellsburg PCH supports total 10 SATA-III 6Gbs ports. The PCH contains three SATA controller modes, while IDE, ACHI and Raid mode.

The project supports 6 SATAIII ports, while two 7 pins SATA ports on baseboard, 4 SATA ports connect to internal miniSAS Connector for system HDD backplane connection.

### SATA PORT CONNECTIVITY



Figure 3-6: S2B SATA Diagram

## USB

The Wellsburg PCH supports total 14 USB ports, 6 USB 2.0 ports and 8 USB 3.0 ports. The USB port distribution of Quanta Grantley product is as follows:

* ASPEED BMC AST2400 consumes 2 USB 2.0 ports (one 1.1 and one 2.0)
* 2 Rear USB3.0 ports are needed for this project
* 2 Front-panel USB2.0 ports are needed for 1U 3.5” SKU and 2U chassis

The USB ports on the products are not required to be powered from STBY.

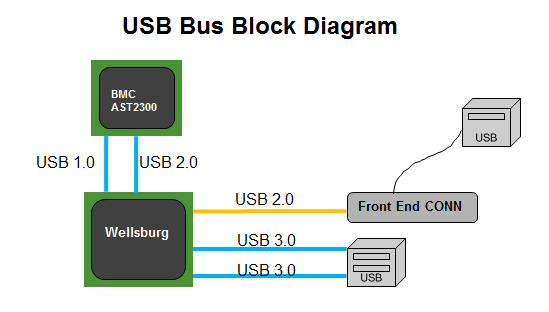


Figure 3-7: Grantley USB Ports

## PCIe BUS

PCI Express\* Gen1, Gen2 and Gen 3 are dual-simplex point-to point serial differential low-voltage interconnects. The signaling bit rate is 2.5 Gb/s one direction per lane for Gen1 (8b/10b encoding), 5.0 Gbit/s one direction per lane for Gen2 (8b/10b encoding) and 8.0 Gb/s one direction per lane for Gen3 (128b/130b encoding). Each port consists of a transmitter and receiver pair. A link between the ports of two devices is a collection of lanes (x1, x2, x4, x8, x16, etc.).

### PCIe PORT CONNECTIVITY

The following diagram lists the usage of the Grantley-EP and Wellsburg PCIe bus segments in S2B project.



Figure 3-8 Quanta Grantley S2B PCIe block diagram

## PCIe Interface

There are multi types of Riser boards and Mezzanine boards for this project. Also we will have PCIe SSD Backplane connected to motherboard via Cable. The follow table lists the detail request of this project.

**Table 3‑8. Riser and Mezzanine list**

|  |  |  |
| --- | --- | --- |
| Description | | |
| 1U | 1 Slot Riser1 | Support (1) PCIe Gen3 x8 Add-on Card |
| 1 Slot Riser2 | Support (1) PCIe GEN3 x16 Add-on Card |
| Linking Riser1 | Support (1) PCIe Gen3 x8  Link to Quanta LAN MEZZ Card (NCSI interface support) |
| 2U | Riser1 – (2) Slot | Support  (1) PCIe Gen3 x16 Add-on Card  (1) PCIe Gen3 x8 Add-on Card |
| Riser1 - (2) Slot +(1) linking | Support   1. PCIe Gen3 x8 linking slot (NCSI interface support) 2. PCIe Gen3 x8 Add-on Card |
| Riser2 - (2) Slot | Support   1. PCIe Gen3 x16 slot 2. PCIe Gen3 x8 Add-on Card |
| OCP  Mezz |  | PCIe x8 Connector  NCSI interface support |
| PCIe SSD |  | Support  (2) PCIe Gen3 x4 port for PCIe SSD Drive |

### Riser Slot PINOUT

#### Riser 1 PINOUT Definition

**Table 3‑9. PIN definition of PCIe Riser 1**

|  |  |  |  |
| --- | --- | --- | --- |
| Riser 1 | | | |
| Name | PIN | | Name |
| P12V | B1 | A1 | GND |
| P12V | B2 | A2 | P12V |
| P12V | B3 | A3 | P12V |
| GND | B4 | A4 | P12V |
| P3V3 | B5 | A5 | GND |
| P3V3 | B6 | A6 | P3V3 |
| P3V3 | B7 | A7 | P3V3 |
| P3V3 | B8 | A8 | P3V3 |
| GND | B9 | A9 | P3V3 |
| P3V3\_AUX | B10 | A10 | P3V3 |
| IRQ\_LVC3\_WAKE\_N | B11 | A11 | GND |
| P12V\_STBY | B12 | A12 | RST\_PERST0\_N |
| SMB\_PCI\_3V3SB\_CLK | B13 | A13 | SLOT1\_PRESENT\_N |
| SM B\_PCI\_3V3SB\_DAT\_SLOT1 | B14 | A14 | FM\_RISER1\_CFG0 |
| GND | B15 | A15 | FM\_RISER1\_CFG1 |
| CLK\_100M\_PE1\_DP | B16 | A16 | GND |
| CLK\_100M\_PE1\_DN | B17 | A17 | CLK\_100M\_PE2\_DP |
| GND | B18 | A18 | CLK\_100M\_PE2\_DN |
| CLK\_100M\_PE3\_DP | B19 | A19 | GND |
| CLK\_100M\_PE3\_DN | B20 | A20 | P3E\_CPU1\_PCIE3\_RX\_DP7 |
| GND | B21 | A21 | P3E\_CPU1\_PCIE3\_RX\_DN7 |
| P3E\_CPU1\_PCIE3\_TX\_C\_DP7 | B22 | A22 | GND |
| P3E\_CPU1\_PCIE3\_TX\_C\_DN7 | B23 | A23 | GND |
| GND | B24 | A24 | P3E\_CPU1\_PCIE3\_RX\_DP6 |
| GND | B25 | A25 | P3E\_CPU1\_PCIE3\_RX\_DN6 |
| P3E\_CPU1\_PCIE3\_TX\_C\_DP6 | B26 | A26 | GND |
| P3E\_CPU1\_PCIE3\_TX\_C\_DN6 | B27 | A27 | GND |
| GND | B28 | A28 | P3E\_CPU1\_PCIE3\_RX\_DP5 |
| GND | B29 | A29 | P3E\_CPU1\_PCIE3\_RX\_DN5 |
| P3E\_CPU1\_PCIE3\_TX\_C\_DP5 | B30 | A30 | GND |
| P3E\_CPU1\_PCIE3\_TX\_C\_DN5 | B31 | A31 | GND |
| GND | B32 | A32 | P3E\_CPU1\_PCIE3\_RX\_DP4 |
| GND | B33 | A33 | P3E\_CPU1\_PCIE3\_RX\_DN4 |
| P3E\_CPU1\_PCIE3\_TX\_C\_DP4 | B34 | A34 | GND |
| P3E\_CPU1\_PCIE3\_TX\_C\_DN4 | B35 | A35 | GND |
| GND | B36 | A36 | P3E\_CPU1\_PCIE3\_RX\_DP3 |
| GND | B37 | A37 | P3E\_CPU1\_PCIE3\_RX\_DN3 |
| P3E\_CPU1\_PCIE3\_TX\_C\_DP3 | B38 | A38 | GND |
| P3E\_CPU1\_PCIE3\_TX\_C\_DN6 | B39 | A39 | GND |
| GND | B40 | A40 | P3E\_CPU1\_PCIE3\_RX\_DP2 |
| GND | B41 | A41 | P3E\_CPU1\_PCIE3\_RX\_DN2 |
| P3E\_CPU1\_PCIE3\_TX\_C\_DP2 | B42 | A42 | GND |
| P3E\_CPU1\_PCIE3\_TX\_C\_DN2 | B43 | A43 | GND |
| GND | B44 | A44 | P3E\_CPU1\_PCIE3\_RX\_DP1 |
| GND | B45 | A45 | P3E\_CPU1\_PCIE3\_RX\_DN1 |
| P3E\_CPU1\_PCIE3\_TX\_C\_DP1 | B46 | A46 | GND |
| P3E\_CPU1\_PCIE3\_TX\_C\_DN1 | B47 | A47 | GND |
| GND | B48 | A48 | P3E\_CPU1\_PCIE3\_RX\_DP0 |
| GND | B49 | A49 | P3E\_CPU1\_PCIE3\_RX\_DN0 |
| P3E\_CPU1\_PCIE3\_TX\_C\_DP0 | B50 | A50 | GND |
| P3E\_CPU1\_PCIE3\_TX\_C\_DN0 | B51 | A51 | GND |
| GND | B52 | A52 | P3E\_CPU0\_PCIE2\_RX\_DP15 |
| GND | B53 | A53 | P3E\_CPU0\_PCIE2\_RX\_DN15 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP15 | B54 | A54 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN15 | B55 | A55 | GND |
| GND | B56 | A56 | P3E\_CPU0\_PCIE2\_RX\_DP14 |
| GND | B57 | A57 | P3E\_CPU0\_PCIE2\_RX\_DN14 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP14 | B58 | A58 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN14 | B59 | A59 | GND |
| GND | B60 | A60 | P3E\_CPU0\_PCIE2\_RX\_DP13 |
| GND | B61 | A61 | P3E\_CPU0\_PCIE2\_RX\_DN13 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP13 | B62 | A62 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN13 | B63 | A63 | GND |
| GND | B64 | A64 | P3E\_CPU0\_PCIE2\_RX\_DP12 |
| GND | B65 | A65 | P3E\_CPU0\_PCIE2\_RX\_DN12 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP12 | B66 | A66 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN12 | B67 | A67 | GND |
| GND | B68 | A68 | P3E\_CPU0\_PCIE2\_RX\_DP11 |
| GND | B69 | A69 | P3E\_CPU0\_PCIE2\_RX\_DN11 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP11 | B70 | A70 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN11 | B71 | A71 | GND |
| GND | B72 | A72 | P3E\_CPU0\_PCIE2\_RX\_DP10 |
| GND | B73 | A73 | P3E\_CPU0\_PCIE2\_RX\_DN10 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP10 | B74 | A74 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN10 | B75 | A75 | GND |
| GND | B76 | A76 | P3E\_CPU0\_PCIE2\_RX\_DP9 |
| GND | B77 | A77 | P3E\_CPU0\_PCIE2\_RX\_DN9 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP9 | B78 | A78 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN9 | B79 | A79 | GND |
| GND | B80 | A80 | P3E\_CPU0\_PCIE2\_RX\_DP8 |
| GND | B81 | A81 | P3E\_CPU0\_PCIE2\_RX\_DN8 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP8 | B82 | A82 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN8 | B83 | A83 | GND |
| GND | B84 | A84 | P3E\_CPU0\_PCIE2\_RX\_DP7 |
| GND | B85 | A85 | P3E\_CPU0\_PCIE2\_RX\_DN7 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP7 | B86 | A86 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN7 | B87 | A87 | GND |
| GND | B88 | A88 | P3E\_CPU0\_PCIE2\_RX\_DP6 |
| GND | B89 | A89 | P3E\_CPU0\_PCIE2\_RX\_DN6 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP6 | B90 | A90 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN6 | B91 | A91 | GND |
| GND | B92 | A92 | P3E\_CPU0\_PCIE2\_RX\_DP5 |
| GND | B93 | A93 | P3E\_CPU0\_PCIE2\_RX\_DN5 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP5 | B94 | A94 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN5 | B95 | A95 | GND |
| GND | B96 | A96 | P3E\_CPU0\_PCIE2\_RX\_DP4 |
| GND | B97 | A97 | P3E\_CPU0\_PCIE2\_RX\_DN4 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP4 | B98 | A98 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN4 | B99 | A99 | GND |
| GND | B100 | A100 | P3E\_CPU0\_PCIE2\_RX\_DP3 |
| GND | B101 | A101 | P3E\_CPU0\_PCIE2\_RX\_DN3 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP3 | B102 | A102 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN3 | B103 | A103 | GND |
| GND | B104 | A104 | P3E\_CPU0\_PCIE2\_RX\_DP2 |
| GND | B105 | A105 | P3E\_CPU0\_PCIE2\_RX\_DN2 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP2 | B106 | A106 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN2 | B107 | A107 | GND |
| GND | B108 | A108 | P3E\_CPU0\_PCIE2\_RX\_DP1 |
| GND | B109 | A109 | P3E\_CPU0\_PCIE2\_RX\_DN1 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP1 | B110 | A110 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN1 | B111 | A111 | GND |
| GND | B112 | A112 | P3E\_CPU0\_PCIE2\_RX\_DP0 |
| GND | B113 | A113 | P3E\_CPU0\_PCIE2\_RX\_DN0 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP0 | B114 | A114 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN0 | B115 | A115 | GND |

#### Riser 2 PINOUT Definition

**Table 3‑10. PIN definition of PCIe Riser 2**

|  |  |  |  |
| --- | --- | --- | --- |
| Riser 2 | | | |
| Name | PIN | | Name |
| P12V | B1 | A1 | GND |
| P12V | B2 | A2 | P12V |
| P12V | B3 | A3 | P12V |
| GND | B4 | A4 | P12V |
| P3V3 | B5 | A5 | GND |
| P3V3 | B6 | A6 | P3V3 |
| P3V3 | B7 | A7 | P3V3 |
| P3V3 | B8 | A8 | P3V3 |
| GND | B9 | A9 | P3V3 |
| P3V3\_AUX | B10 | A10 | P3V3 |
| IRQ\_LVC3\_WAKE\_N | B11 | A11 | GND |
| TP\_SLOT2\_B12 | B12 | A12 | RST\_PERST1\_N |
| SMB\_PCI\_3V3SB\_CLK | B13 | A13 | SLOT2\_PRESENT\_N |
| SM B\_PCI\_3V3SB\_DAT\_SLOT2 | B14 | A14 | FM\_RISER2\_CFG0 |
| GND | B15 | A15 | FM\_RISER2\_CFG1 |
| CLK\_100M\_PE4\_DP | B16 | A16 | GND |
| CLK\_100M\_PE4\_DN | B17 | A17 | CLK\_100M\_PE5\_DP |
| GND | B18 | A18 | CLK\_100M\_PE5\_DN |
| CLK\_100M\_PE6\_DP | B19 | A19 | GND |
| CLK\_100M\_PE6\_DN | B20 | A20 | P3E\_CPU1\_PCIE3\_RX\_DP8 |
| GND | B21 | A21 | P3E\_CPU1\_PCIE3\_RX\_DN8 |
| P3E\_CPU1\_PCIE3\_TX\_C\_DP8 | B22 | A22 | GND |
| P3E\_CPU1\_PCIE3\_TX\_C\_DN8 | B23 | A23 | GND |
| GND | B24 | A24 | P3E\_CPU1\_PCIE3\_RX\_DP9 |
| GND | B25 | A25 | P3E\_CPU1\_PCIE3\_RX\_DN9 |
| P3E\_CPU1\_PCIE3\_TX\_C\_DP9 | B26 | A26 | GND |
| P3E\_CPU1\_PCIE3\_TX\_C\_DN9 | B27 | A27 | GND |
| GND | B28 | A28 | P3E\_CPU1\_PCIE3\_RX\_DP10 |
| GND | B29 | A29 | P3E\_CPU1\_PCIE3\_RX\_DN10 |
| P3E\_CPU1\_PCIE3\_TX\_C\_DP10 | B30 | A30 | GND |
| P3E\_CPU1\_PCIE3\_TX\_C\_DN10 | B31 | A31 | GND |
| GND | B32 | A32 | P3E\_CPU1\_PCIE3\_RX\_DP11 |
| GND | B33 | A33 | P3E\_CPU1\_PCIE3\_RX\_DN11 |
| P3E\_CPU1\_PCIE3\_TX\_C\_DP11 | B34 | A34 | GND |
| P3E\_CPU1\_PCIE3\_TX\_C\_DN11 | B35 | A35 | GND |
| GND | B36 | A36 | P3E\_CPU1\_PCIE3\_RX\_DP12 |
| GND | B37 | A37 | P3E\_CPU1\_PCIE3\_RX\_DN12 |
| P3E\_CPU1\_PCIE3\_TX\_C\_DP12 | B38 | A38 | GND |
| P3E\_CPU1\_PCIE3\_TX\_C\_DN12 | B39 | A39 | GND |
| GND | B40 | A40 | P3E\_CPU1\_PCIE3\_RX\_DP13 |
| GND | B41 | A41 | P3E\_CPU1\_PCIE3\_RX\_DN13 |
| P3E\_CPU1\_PCIE3\_TX\_C\_DP13 | B42 | A42 | GND |
| P3E\_CPU1\_PCIE3\_TX\_C\_DN13 | B43 | A43 | GND |
| GND | B44 | A44 | P3E\_CPU1\_PCIE3\_RX\_DP14 |
| GND | B45 | A45 | P3E\_CPU1\_PCIE3\_RX\_DN14 |
| P3E\_CPU1\_PCIE3\_TX\_C\_DP14 | B46 | A46 | GND |
| P3E\_CPU1\_PCIE3\_TX\_C\_DN14 | B47 | A47 | GND |
| GND | B48 | A48 | P3E\_CPU1\_PCIE3\_RX\_DP15 |
| GND | B49 | A49 | P3E\_CPU1\_PCIE3\_RX\_DN15 |
| P3E\_CPU1\_PCIE3\_TX\_C\_DP15 | B50 | A50 | GND |
| P3E\_CPU1\_PCIE3\_TX\_C\_DN15 | B51 | A51 | GND |
| GND | B52 | A52 | P3E\_CPU1\_PCIE2\_RX\_DP0 |
| GND | B53 | A53 | P3E\_CPU1\_PCIE2\_RX\_DN0 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP0 | B54 | A54 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN0 | B55 | A55 | GND |
| GND | B56 | A56 | P3E\_CPU1\_PCIE2\_RX\_DP1 |
| GND | B57 | A57 | P3E\_CPU1\_PCIE2\_RX\_DN1 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP1 | B58 | A58 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN1 | B59 | A59 | GND |
| GND | B60 | A60 | P3E\_CPU1\_PCIE2\_RX\_DP2 |
| GND | B61 | A61 | P3E\_CPU1\_PCIE2\_RX\_DN2 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP2 | B62 | A62 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN2 | B63 | A63 | GND |
| GND | B64 | A64 | P3E\_CPU1\_PCIE2\_RX\_DP3 |
| GND | B65 | A65 | P3E\_CPU1\_PCIE2\_RX\_DN3 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP3 | B66 | A66 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN3 | B67 | A67 | GND |
| GND | B68 | A68 | P3E\_CPU1\_PCIE2\_RX\_DP4 |
| GND | B69 | A69 | P3E\_CPU1\_PCIE2\_RX\_DN4 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP4 | B70 | A70 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN4 | B71 | A71 | GND |
| GND | B72 | A72 | P3E\_CPU1\_PCIE2\_RX\_DP5 |
| GND | B73 | A73 | P3E\_CPU1\_PCIE2\_RX\_DN5 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP5 | B74 | A74 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN5 | B75 | A75 | GND |
| GND | B76 | A76 | P3E\_CPU1\_PCIE2\_RX\_DP6 |
| GND | B77 | A77 | P3E\_CPU1\_PCIE2\_RX\_DN6 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP6 | B78 | A78 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN6 | B79 | A79 | GND |
| GND | B80 | A80 | P3E\_CPU1\_PCIE2\_RX\_DP7 |
| GND | B81 | A81 | P3E\_CPU1\_PCIE2\_RX\_DN7 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP7 | B82 | A82 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN7 | B83 | A83 | GND |
| GND | B84 | A84 | P3E\_CPU1\_PCIE2\_RX\_DP8 |
| GND | B85 | A85 | P3E\_CPU1\_PCIE2\_RX\_DN8 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP8 | B86 | A86 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN8 | B87 | A87 | GND |
| GND | B88 | A88 | P3E\_CPU1\_PCIE2\_RX\_DP9 |
| GND | B89 | A89 | P3E\_CPU1\_PCIE2\_RX\_DN9 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP9 | B90 | A90 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN9 | B91 | A91 | GND |
| GND | B92 | A92 | P3E\_CPU1\_PCIE2\_RX\_DP10 |
| GND | B93 | A93 | P3E\_CPU1\_PCIE2\_RX\_DN10 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP10 | B94 | A94 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN10 | B95 | A95 | GND |
| GND | B96 | A96 | P3E\_CPU1\_PCIE2\_RX\_DP11 |
| GND | B97 | A97 | P3E\_CPU1\_PCIE2\_RX\_DN11 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP11 | B98 | A98 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN11 | B99 | A99 | GND |
| GND | B100 | A100 | P3E\_CPU1\_PCIE2\_RX\_DP12 |
| GND | B101 | A101 | P3E\_CPU1\_PCIE2\_RX\_DN12 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP12 | B102 | A102 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN12 | B103 | A103 | GND |
| GND | B104 | A104 | P3E\_CPU1\_PCIE2\_RX\_DP13 |
| GND | B105 | A105 | P3E\_CPU1\_PCIE2\_RX\_DN13 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP13 | B106 | A106 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN13 | B107 | A107 | GND |
| GND | B108 | A108 | P3E\_CPU1\_PCIE2\_RX\_DP14 |
| GND | B109 | A109 | P3E\_CPU1\_PCIE2\_RX\_DN14 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP14 | B110 | A110 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN14 | B111 | A111 | GND |
| GND | B112 | A112 | P3E\_CPU1\_PCIE2\_RX\_DP15 |
| GND | B113 | A113 | P3E\_CPU1\_PCIE2\_RX\_DN15 |
| P3E\_CPU0\_PCIE2\_TX\_C\_DP15 | B114 | A114 | GND |
| P3E\_CPU0\_PCIE2\_TX\_C\_DN15 | B115 | A115 | GND |

#### OCP MEZZ PINOUT Definition

**Table 3‑11. PIN definition of PCIe OCP Mezz connector**

|  |  |  |  |
| --- | --- | --- | --- |
| OCP Mezz | | | |
| PIN | Name | PIN | Name |
| 61 | P12V | 1 | MEZZ\_PRSNT1\_N |
| 62 | P12V | 2 | P5V\_AUX |
| 63 | P12V | 3 | P5V\_AUX |
| 64 | GND | 4 | P5V\_AUX |
| 65 | GND | 5 | GND |
| 66 | P3V3\_AUX | 6 | GND |
| 67 | GND | 7 | P3V3\_AUX |
| 68 | GND | 8 | GND |
| 69 | P3V3 | 9 | GND |
| 70 | P3V3 | 10 | P3V3 |
| 71 | P3V3 | 11 | P3V3 |
| 72 | P3V3 | 12 | P3V3 |
| 73 | GND | 13 | P3V3 |
| 74 | PU\_SMB\_LAN\_ALERT\_N\_MEZZ | 14 | NCSI\_OCP\_RCSDV |
| 75 | SMB\_PCI\_3V3SB\_CLK | 15 | NCSI\_OCP\_RCLK |
| 76 | SMB\_PCI\_3V3SB\_DAT\_MEZZ\_R | 16 | NCSI\_OCP\_TXEN |
| 77 | IRQ\_LVC3\_WAKE\_N | 17 | RST\_PERST0\_N |
| 78 | NCSI\_OCP\_RXER | 18 | TP\_OCP\_MEZZ\_18 |
| 79 | GND | 19 | TP\_OCP\_MEZZ\_19 |
| 80 | NCSI\_OCP\_TXD0 | 20 | GND |
| 81 | NCSI\_OCP\_TXD1 | 21 | GND |
| 82 | GND | 22 | NCSI\_OCP\_RXD0 |
| 83 | GND | 23 | NCSI\_OCP\_RXD1 |
| 84 | CLK\_100M\_OCP\_MEZZA\_DP | 24 | GND |
| 85 | CLK\_100M\_OCP\_MEZZA\_DN | 25 | GND |
| 86 | GND | 26 | CLK\_100M\_OCP\_MEZZB\_DP |
| 87 | GND | 27 | CLK\_100M\_OCP\_MEZZB\_DN |
| 88 | P3E\_CPU0\_PCIE3\_TX\_C\_DP7 | 28 | GND |
| 89 | P3E\_CPU0\_PCIE3\_TX\_C\_DN7 | 29 | GND |
| 90 | GND | 30 | P3E\_CPU0\_PCIE3\_RX\_DP7 |
| 91 | GND | 31 | P3E\_CPU0\_PCIE3\_RX\_DN7 |
| 92 | P3E\_CPU0\_PCIE3\_TX\_C\_DP6 | 32 | GND |
| 93 | P3E\_CPU0\_PCIE3\_TX\_C\_DN6 | 33 | GND |
| 94 | GND | 34 | P3E\_CPU0\_PCIE3\_RX\_DP6 |
| 95 | GND | 35 | P3E\_CPU0\_PCIE3\_RX\_DN6 |
| 96 | P3E\_CPU0\_PCIE3\_TX\_C\_DP5 | 36 | GND |
| 97 | P3E\_CPU0\_PCIE3\_TX\_C\_DN5 | 37 | GND |
| 98 | GND | 38 | P3E\_CPU0\_PCIE3\_RX\_DP5 |
| 99 | GND | 39 | P3E\_CPU0\_PCIE3\_RX\_DN5 |
| 100 | P3E\_CPU0\_PCIE3\_TX\_C\_DP4 | 40 | GND |
| 101 | P3E\_CPU0\_PCIE3\_TX\_C\_DN4 | 41 | GND |
| 102 | GND | 42 | P3E\_CPU0\_PCIE3\_RX\_DP4 |
| 103 | GND | 43 | P3E\_CPU0\_PCIE3\_RX\_DN4 |
| 104 | P3E\_CPU0\_PCIE3\_TX\_C\_DP3 | 44 | GND |
| 105 | P3E\_CPU0\_PCIE3\_TX\_C\_DN3 | 45 | GND |
| 106 | GND | 46 | P3E\_CPU0\_PCIE3\_RX\_DP3 |
| 107 | GND | 47 | P3E\_CPU0\_PCIE3\_RX\_DN3 |
| 108 | P3E\_CPU0\_PCIE3\_TX\_C\_DP2 | 48 | GND |
| 109 | P3E\_CPU0\_PCIE3\_TX\_C\_DN2 | 49 | GND |
| 110 | GND | 50 | P3E\_CPU0\_PCIE3\_RX\_DP2 |
| 111 | GND | 51 | P3E\_CPU0\_PCIE3\_RX\_DN2 |
| 112 | P3E\_CPU0\_PCIE3\_TX\_C\_DP1 | 52 | GND |
| 113 | P3E\_CPU0\_PCIE3\_TX\_C\_DN1 | 53 | GND |
| 114 | GND | 54 | P3E\_CPU0\_PCIE3\_RX\_DP1 |
| 115 | GND | 55 | P3E\_CPU0\_PCIE3\_RX\_DN1 |
| 116 | P3E\_CPU0\_PCIE3\_TX\_C\_DP0 | 56 | GND |
| 117 | P3E\_CPU0\_PCIE3\_TX\_C\_DN0 | 57 | GND |
| 118 | GND | 58 | P3E\_CPU0\_PCIE3\_RX\_DP0 |
| 119 | GND | 59 | P3E\_CPU0\_PCIE3\_RX\_DN0 |
| 120 | OCP\_MEZZA\_PRSNT\_N | 60 | GND |

#### PCIe SSD 0 Pinout Definition

**Table 3‑12. PIN definition of PCIe SSD0 Connector**

|  |  |  |  |
| --- | --- | --- | --- |
| **PCIe SSD0** | | | |
| PIN | Name | PIN | Name |
| A1 | SMB\_PCI\_3V3SB\_CLK | C1 | CLK\_100M\_PE7\_DP |
| A2 | SMB\_PCI\_3V3SB\_DAT\_PESSD0 | C2 | CLK\_100M\_PE7\_DN |
| A3 | GND | C3 | GND |
| A4 | P3E\_CPU1\_PCIE1\_RX\_DP1 | C4 | P3E\_CPU1\_PCIE1\_TX\_C\_DP1 |
| A5 | P3E\_CPU1\_PCIE1\_RX\_DN1 | C5 | P3E\_CPU1\_PCIE1\_TX\_C\_DN1 |
| A6 | GND | C6 | GND |
| A7 | P3E\_CPU1\_PCIE1\_RX\_DP3 | C7 | P3E\_CPU1\_PCIE1\_TX\_C\_DP3 |
| A8 | P3E\_CPU1\_PCIE1\_RX\_DN3 | C8 | P3E\_CPU1\_PCIE1\_TX\_C\_DN3 |
| A9 | GND | C9 | GND |
| B1 | RST\_PERST1\_N | D1 | SMB\_LVC3\_PE\_HP\_SCL\_R1 |
| B2 | HP\_LVC3\_PESSD0\_PWRGD | D2 | SMB\_LVC3\_PE\_HP\_SDA\_R1 |
| B3 | GND | D3 | GND |
| B4 | P3E\_CPU1\_PCIE1\_RX\_DP0 | D4 | P3E\_CPU1\_PCIE1\_TX\_C\_DP0 |
| B5 | P3E\_CPU1\_PCIE1\_RX\_DN0 | D5 | P3E\_CPU1\_PCIE1\_TX\_C\_DN0 |
| B6 | GND | D6 | GND |
| B7 | P3E\_CPU1\_PCIE1\_RX\_DP2 | D7 | P3E\_CPU1\_PCIE1\_TX\_C\_DP2 |
| B8 | P3E\_CPU1\_PCIE1\_RX\_DN2 | D8 | P3E\_CPU1\_PCIE1\_TX\_C\_DN2 |
| B9 | GND | D9 | GND |
| G1 | GND | G3 | GND |
| G2 | GND | G4 | GND |

#### PCIe SSD 1 Pinout Definition

**Table 3‑13. PIN definition of PCIe SSD1 Connector**

|  |  |  |  |
| --- | --- | --- | --- |
| **PCIe SSD0** | | | |
| PIN | Name | PIN | Name |
| A1 | SMB\_PCI\_3V3SB\_CLK | C1 | CLK\_100M\_PE8\_DP |
| A2 | SMB\_PCI\_3V3SB\_DAT\_PESSD1 | C2 | CLK\_100M\_PE8\_DN |
| A3 | GND | C3 | GND |
| A4 | P3E\_CPU1\_PCIE1\_RX\_DP5 | C4 | P3E\_CPU1\_PCIE1\_TX\_C\_DP5 |
| A5 | P3E\_CPU1\_PCIE1\_RX\_DN5 | C5 | P3E\_CPU1\_PCIE1\_TX\_C\_DN5 |
| A6 | GND | C6 | GND |
| A7 | P3E\_CPU1\_PCIE1\_RX\_DP7 | C7 | P3E\_CPU1\_PCIE1\_TX\_C\_DP7 |
| A8 | P3E\_CPU1\_PCIE1\_RX\_DN7 | C8 | P3E\_CPU1\_PCIE1\_TX\_C\_DN7 |
| A9 | GND | C9 | GND |
| B1 | RST\_PERST1\_N | D1 | SMB\_LVC3\_PE\_HP\_SCL\_R2 |
| B2 | HP\_LVC3\_PESSD1\_PWRGD | D2 | SMB\_LVC3\_PE\_HP\_SDA\_R2 |
| B3 | GND | D3 | GND |
| B4 | P3E\_CPU1\_PCIE1\_RX\_DP4 | D4 | P3E\_CPU1\_PCIE1\_TX\_C\_DP4 |
| B5 | P3E\_CPU1\_PCIE1\_RX\_DN4 | D5 | P3E\_CPU1\_PCIE1\_TX\_C\_DN4 |
| B6 | GND | D6 | GND |
| B7 | P3E\_CPU1\_PCIE1\_RX\_DP6 | D7 | P3E\_CPU1\_PCIE1 TX\_C\_DP6 |
| B8 | P3E\_CPU1\_PCIE1\_RX\_DN6 | D8 | P3E\_CPU1\_PCIE1 TX\_C\_DN6 |
| B9 | GND | D9 | GND |
| G1 | GND | G3 | GND |
| G2 | GND | G4 | GND |

## LAN ON MOTHERBOARD (LOM)

The baseboards will use the Intel® I350 code named Powerville Dual 10/100/1000 integrated MAC and PHY controller. The Powerville LAN controller requires a PCIe x4 Gen2 upstream interface. The Powerville controller also requires the use of the Wellsburg SMBus interface during Sleep states S5 as well as for ME Firmware. The Powerville LAN controller will be on standby power so that Wake on LAN and manageability functions can be supported. Powerville will be used in conjunction with the BMC for out of band Management traffic. The BMC will communicate with Powerville over a NC-SI interface (RMII physical). Powerville will be on standby power so that the BMC can send management traffic over the NC-SI interface to the network during sleep states S5.

### DEDICATED NIC (MANAGEMENT RJ45 Port)

Motherboards will support embedded version of the Dedicated NIC. The Dedicated NIC feature provides a dedicated 1G/100M/10Mb Ethernet interface for remote management features. The Dedicated NIC consists of a 1G/100M/10MbE PHY device which interfaces to the primary NC-SI port 0 (RGMII mode) out of the AST2400 integrated BMC, to offer a dedicated management 1G/100M/10MbE port. Because of the limited distance the RGMII signals can travel, the recommended placement for this connector is to be as close as possible to the AST2400 IBMC.

## LPC BUS

The PCH implements an LPC interface as described in the Low Pin Count Interface Specification, Revision 1.1. The PCH LPC bus is used to connect to the BMC and to an optional TPM device.

## TPM

The PCH supports TPM specification 1.2 level2 revisions 103. The Baseboard will not be populated with a TPM device except for special deals that require a TPM.

## SERIAL PORT

There are two serial ports provided. One is external serial port on rear. One is internal serial port. The usage is either debug or for a terminal concentrator. Since the serial port does not exist in the IO panel, the user will need to use a cable and chassis knock out for a DB9 connector. The cable will connect to a standard 10 pin serial port header. Note that the choice of RS232 transceivers is limited by the absence of a -12V rail.

## FANs

The board supports a total **8** FANs. Fan signals are made available via a consolidated header. The FAN control and FAN speed monitor are from BMC chip. BMC will have FAN Tachometer and PWM function. Note that all fans will operate at the same speed.

## Jumper Definition

Below table is Jumper definition of board.

**Table 4-7 BIOS/BMC Jumper Setting**

|  |  |  |  |
| --- | --- | --- | --- |
| JUMPER LOCATION |  | DEFAULT SETTING. | FUNCTION |
| PASSWORLD CLEAR | JP11 | 1-2 | 1-2 : HOLD (DEFAULT)  2-3 : CLEAR |
| RECOVER BIOS JUMPER | JP1 | 1-2 | 1-2 : HOLD (DEFAULT)  2-3 : RECOVER BIOS |
| CLR RTC\_RST | JP10 | 1-2 | 1-2 : HOLD (DEFAULT)  2-3 : CLR RTC\_RST |
| ME FIRMWARE UPDATE | JP8 | 1-2 | 1-2 : HOLD (DEFAULT)  2-3 : ME IN FORCE UPDATE MODE |
| BMC Disable/Enable | J19 | 1-2 | Open: HOLD (DEFAULT)  1-2: Disable BMC |
| SOL Enable | J7 | 1-2 | Open: HOLD (DEFAULT)  1-2: Enable BMC |
| Intruder Enable | J57 | 1-2 | Open: HOLD (DEFAULT)  1-2: Chassis Top Covered |
| SMB\_SML0 debug header | JP24 | Pin1  Pin3 | Pin1: Smb\_Sml0\_3V3sb\_Clk  Pin3: Smb\_Sml0\_3V3sb\_Dat |
| SMB Host debug header | JP7 | Pin1  Pin3 | Pin1: Smb\_Host\_3V3sb\_Clk  Pin3: Smb\_Host\_3V3sb\_Dat |
| SMB\_PMbus Debug Header | JP2 | Pin1  Pin3 | Pin1: Smb\_3V3sb\_Pmbus\_Clk  Pin3: Smb\_3V3sb\_Pmbus\_Dat |

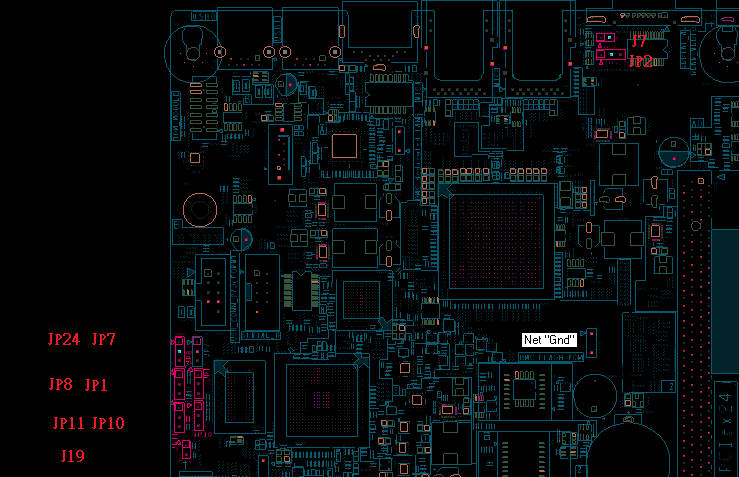


Figure 3-18: Jumper Location

### Password Clear

The user sets this 3-pin jumper to clear the password. The pin should be strapped LOW when the password needs to be reset.

**Table 4-8 Password Clear Jumper**

| **Jumper Position** | **Mode of Operation** | **Note** |
| --- | --- | --- |
| 1-2 | Normal | FM\_PASSWORD\_CLEAR\_N pin is pulled HIGH. Default position. |
| 2-3 | Clear Password | FM\_PASSWORD\_CLEAR\_N pin is pulled LOW. |

## DEBUG header Information

### XDP SUPPORT

Standard XDP header for Grantley-EP Processors (XDP 0) will be provided, the XDP connector will be depopulated in production, please indicate parts that can be safely removed for production in the schematic.

### SMB Debug Header (JP7)

SMB Debug Header is a SMB debug header which was connected to PCH’s HOST channel and BMC SMB channel 4.

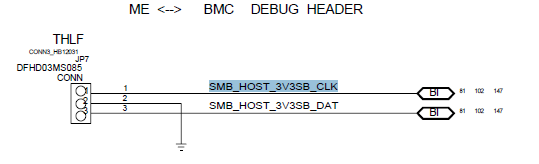


Figure 3-19: S2B SMB debug Header

### BMC Debug Header (JP2 and J19)

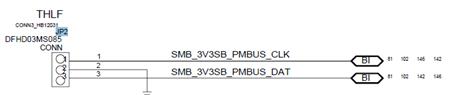


Figure 3-20: S2B PMBUS debug Header

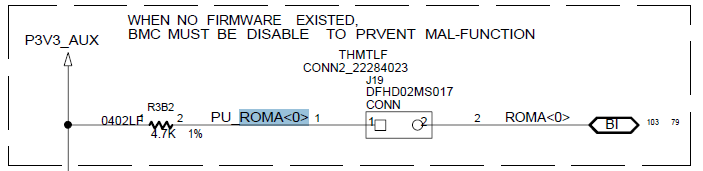


Figure 3-21: S2B BMC Desiable Header

## PRODUCT SENSORS

**Table 3‑15. Baseboard Sensor list**

|  |  |  |
| --- | --- | --- |
|  | Description |  |
| TMP75\_0 | Temperature sensor on middle of board | PCI\_Inlet\_Temp2 |
| TMP75\_1 | Temperature sensor close to OCP Mezz | PCI\_Inlet\_Temp1 |
| TMP75\_2 | Temperature sensor close to dedicated NIC | Exhaust\_Temp |
| AST2400 (BMC) | Monitor CPU core voltage and system voltage |  |

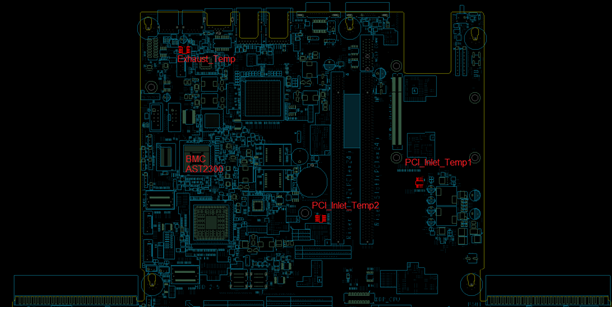


Figure 3-22: S2B Temperature sensor

## SMBUS

The products must comply with the Grantley Platform common-core SMBUS architecture in order to maximize BIOS, Wellsburg ME Firmware, and BMC firmware. This is a requirement in an order to minimize BIOS and Firmware code development efforts and improve validation and product board

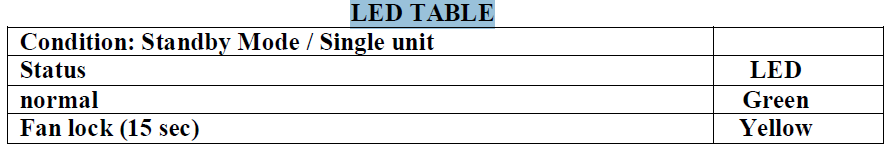
stability and debugging.

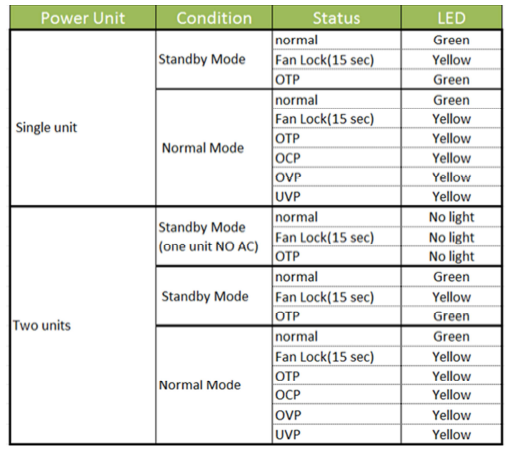
Figure 3-23: Grantley BMC SMBUS Block Diagram

## POWER

These are max values (where available) for board VR design purposes. From a system power supply budgeting or thermal standpoint it's recommended to apply a derating factor. TDP power estimate for the main components are provided in below table as well.

#### LED Behavior of POWER SUPPLY





**Table 3‑17. LED Behavior of PSU**

### Power supply PINOUT

**Table 3‑17. PIN definition of Power Supply 0**

|  |  |  |  |
| --- | --- | --- | --- |
| Power Supply 0 | | | |
| Name | PIN | | Name |
| P12V | 64 | 1 | P12V |
| P12V | 63 | 2 | P12V |
| P12V | 62 | 3 | P12V |
| P12V | 61 | 4 | P12V |
| P12V | 60 | 5 | P12V |
| P12V | 59 | 6 | P12V |
| P12V | 58 | 7 | P12V |
| P12V | 57 | 8 | P12V |
| P12V | 56 | 9 | P12V |
| P12V | 55 | 10 | P12V |
| P12V | 54 | 11 | P12V |
| P12V | 53 | 12 | P12V |
| GND | 52 | 13 | GND |
| GND | 51 | 14 | GND |
| GND | 50 | 15 | GND |
| GND | 49 | 16 | GND |
| GND | 48 | 17 | GND |
| GND | 47 | 18 | GND |
| GND | 46 | 19 | GND |
| GND | 45 | 20 | GND |
| GND | 44 | 21 | GND |
| GND | 43 | 22 | GND |
| GND | 42 | 23 | GND |
| GND | 41 | 24 | GND |
| PSU\_REMOTE\_SENSE\_P | 40 | 25 | TP\_TACH |
| P12V\_STBY | 39 | 26 | PSU\_REMOTE\_SENSE\_N |
| PSU\_A0 | 38 | 27 | TP\_VIN\_GOOD |
| PWROK0 | 37 | 28 | CSHARE |
| GND | 36 | 29 | FM\_PS\_EN\_PSU\_N |
| SMB\_3V3SB\_PMBUS\_CLK | 35 | 30 | PS\_KILL\_0 |
| PSU\_PRESENT0\_N | 34 | 31 | RESET\_PS\_0 |
| SMB\_3V3SB\_PMBUS\_DAT | 33 | 32 | IRQ\_SML1\_PMBUS\_ALERT\_N |

**Table 3‑18. PIN definition of Power Supply 1**

|  |  |  |  |
| --- | --- | --- | --- |
| Power Supply 1 | | | |
| Name | PIN | | Name |
| P12V | 64 | 1 | P12V |
| P12V | 63 | 2 | P12V |
| P12V | 62 | 3 | P12V |
| P12V | 61 | 4 | P12V |
| P12V | 60 | 5 | P12V |
| P12V | 59 | 6 | P12V |
| P12V | 58 | 7 | P12V |
| P12V | 57 | 8 | P12V |
| P12V | 56 | 9 | P12V |
| P12V | 55 | 10 | P12V |
| P12V | 54 | 11 | P12V |
| P12V | 53 | 12 | P12V |
| GND | 52 | 13 | GND |
| GND | 51 | 14 | GND |
| GND | 50 | 15 | GND |
| GND | 49 | 16 | GND |
| GND | 48 | 17 | GND |
| GND | 47 | 18 | GND |
| GND | 46 | 19 | GND |
| GND | 45 | 20 | GND |
| GND | 44 | 21 | GND |
| GND | 43 | 22 | GND |
| GND | 42 | 23 | GND |
| GND | 41 | 24 | GND |
| PSU\_REMOTE\_SENSE\_P | 40 | 25 | TP\_TACH |
| P12V\_STBY | 39 | 26 | PSU\_REMOTE\_SENSE\_N |
| PSU\_A1 | 38 | 27 | TP\_VIN\_GOOD |
| PWROK1 | 37 | 28 | CSHARE |
| GND | 36 | 29 | FM\_PS\_EN\_PSU\_N |
| SMB\_3V3SB\_PMBUS\_CLK | 35 | 30 | PS\_KILL\_1 |
| PSU\_PRESENT1\_N | 34 | 31 | RESET\_PS\_1 |
| SMB\_3V3SB\_PMBUS\_DAT | 33 | 32 | IRQ\_SML1\_PMBUS\_ALERT\_N |

# PRODUCT SYSTEM REQUIREMENTS

1U and 2U chassis will be enabled to complement the board offering. A new chassis development is expected in order to accommodate the marketing requirements of a spread-core form factor and the docking power supplies.

## Chassis Overview

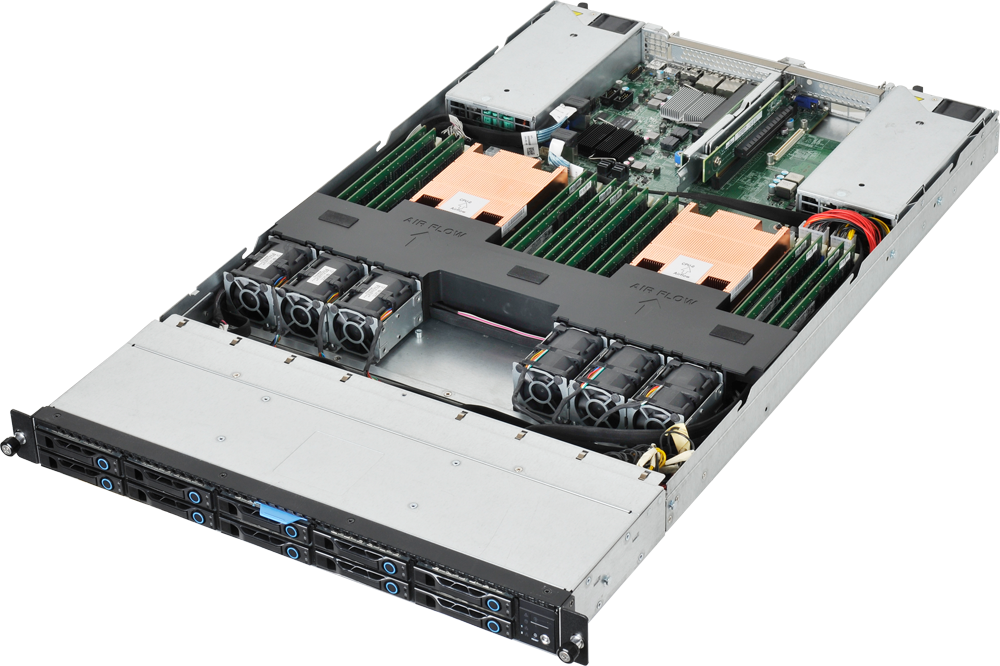


Figure 4-1 1U Chassis







Figure 4-2 1U Chassis Front and Rear View

## LED behavior

### Front Panel LED Function and Behavior

#### 2U System

**Table 4‑1. LED behavior of 2U system**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Mark** | **Name** | **Color** | **Condition** | **Behavior** | **Voltage** | **Owner** |
|  | **Power LED** | **Blue** | **On** | **S0 System Power On** | **5VSB** | **BMC** |
|  | **OFF** | **S5 System Power Off** |
|  | **ID LED** | **Blue** | **Blinking** | **Unit selected for Identification** | **5VSB** | **BMC** |
|  | **OFF** | **No Identificaiton requested** |
|  | **Fault LED** | **Amber** | **Blinking** | **Critical Failure: FAN /Temp/ Voltage** | **5VSB** | **BMC** |
| **Non Critical Failure:** |
|  | **OFF** | **SEL Cleared** |
| **Last pending warning or Error has been deleted** |
|  | **HDD Activity** | **Blue** | **Blinking** | **HDD access (SATA Onboard Only)** | **5V** | **PCH** |
|  | **OFF** |  |
|  | **LAN1 LED** | **Blue** | **ON** | **Link** | **3V3AUX** | **LAN1** |
| **Blue** | **Blinking** | **LAN Access** |
|  | **LAN2 LED** | **Blue** | **ON** | **Link** | **3V3AUX** | **Lan2** |
| **Blue** | **Blinking** | **LAN Access** |