

Barreleye 1.0 Draft Specification

Chassis, Motherboard, IO Board, Lunchbox Power Supply  
Revision 0.8.2

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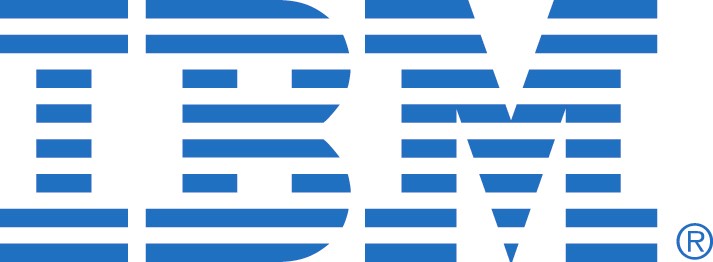
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# Recognition & Logos

This specification and its associated first implementations in hardware were developed and tested by engineers and software developers at Ingrasys (a Foxconn / Hon Hai Industries subsidiary), Rackspace, and IBM, basedin part upon material made available through the OpenPOWER Foundation and community members.

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# Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| Revision | Date | Name | Description |
| 0.1 | 04/28/2015 |  | Preliminary Release |
| 0.2 | 05/12/2015 |  | Update POWER8 DIMM Support |
| 0.3 | 07/18/2015 |  | 1. Update Sled Block Diagram  2. Update PCB information |
| 0.4 | 08/20/2015 |  | 1. Add PEB and BP placement  2. Update Chapter 9 Mechanical |
| 0.5 | 08/25/2015 |  | Add 9.9 Rack and 9.10 Rack Knife section |
| 0.6 | 08/25/2015 |  | Edits for grammar and flow |
| 0.7 | 08/28/2015 |  | 1. Add MB and IO stack-up  2. Add board to board connector section  3. Add Lunch Box Chapter |
| 0.7.1 | 09/08/2015 |  | Additional edits for grammar and flow |
| 0.7.2 | 09/18/2015 |  | Additional edits for grammar and flow |
| 0.8 | 11/23/2015 |  | 1. Add 9.9 HDD tray dimension  2. Correct the number of CPU pin to 2296 pins  3. Update mSATA to M.2 SATA due to design change  4. Update APSS function description  5. Correct the location of fan connectors which are all on MB  6. BMC firmware update methoed  7. Add connector pin define  8. Update Lunch Box picture  9. Remove original section, 7.3.2 and 7.4.2 for VR optimiztions, since VR doesn’t support auto-phase dropping for light loading |
| 0.8.2 | 01/25/2015 |  | Numerous Edits:   1. Added IBM / OpenPOWER notice page 2. Added recognition & logos page 3. Added OCP-HL-P license information 4. Updated authors information |

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# Scope

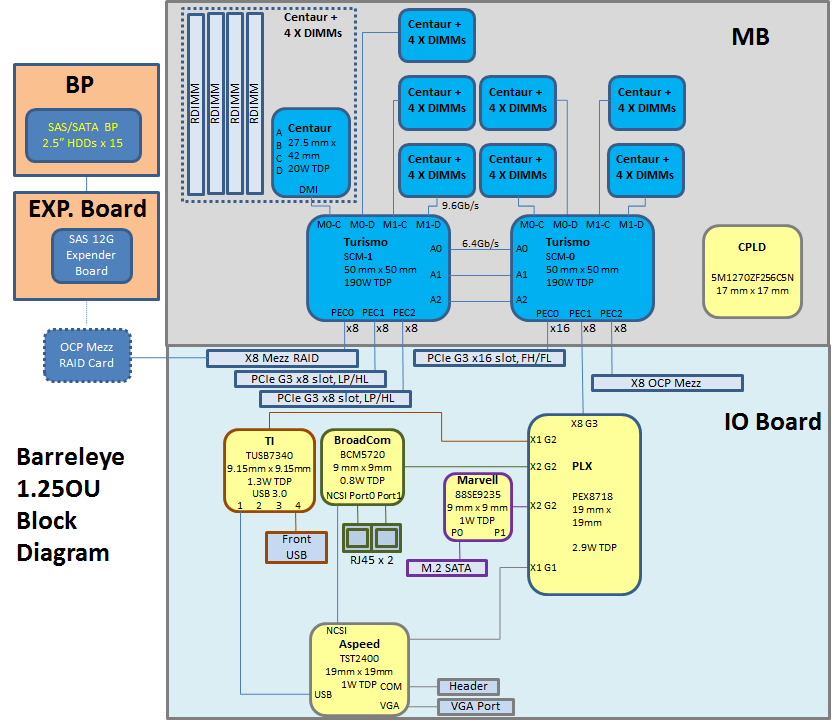
This document describes the specification of Barreleye, an OpenPOWER-based Open Compute server, with a mechanical & electrical package designed for OpenRack.

The hardware engineering specification provides technical details for the server board’s functional architecture and feature set, and some mechanical design details.

# System Block Diagram

The Barreleye platform consists of IBM POWER8 “Turismo” SCM (Single Chip Module) Processor with IBM “Centaur” Memory Buffers, with PCI-E Gen 3 integrated on chip. Additional details follow.

* IBM POWER8 “Turismo” SCM Processors connects directly to Memory Buffers through a DMI interface operating at 9.6 GTs x 3B.
  + Each processor is directly connected to four buffers, with 8 total buffers on board.
  + Each buffer connects to 4 DIMM slots
  + Each buffer also functions as a 16MiB L4 cache (128 MiB of cache, total)
  + Each buffer provides an additional 9.6 GTs x 3B of memory bandwidth, to the system
  + In this configuration, maximum bandwidth to DRAM is 115.2 GiBps, per socket, and 230.4 GiBps per system.
* The communication between each CPU is A-Bus, operating at 6.4 GTs x 2B.
  + There are three A-Bus links between the CPUs, providing a total bandwidth of 38.4 GiBps
* POWER8 “Turismo” includes an integrated PCI Gen 3 interface, with a total of 56 lanes spread between processors.



# Product Features

* 1. Feature List

|  |  |
| --- | --- |
| **Project name** | Barreleye |
| **Chassis Size** | 1.25OU |
| **CPU** | IBM POWER8 “Turismo” SCM Processor x 2, 2296 pins Socket  (support up to 12-core, 190W CPU) |
| **Memory Buffer** | IBM Centaur, 4 Memory buffers per Processor, total 8 memory buffer |
| **Memory** | 4 DDR3 Memory channels per memory buffer; total 32 DDR3 RDIMMs,1333 MHz(1DPC), 8/16/32GB |
| **Storage** | 15x 12Gb/s SAS or 6Gb/s SATA 2.5” drive slots, up to 15mm thickness, connected via SEB, to an onboard HBA. One M.2 SATA slot, also on board. |
| **Graphic** | Integrated in iBMC (ASPEED AST2400) chip |
| **Onboard Network** | BroadCom BCM5720, GbE Controller, dual ports |
| **PCIE Bridge** | PLX PEX 8718 |
| **USB Controller** | TI TUSB 7340, support USB 3.0 |
| **SATA Controller** | Marvell 88SE9235, support for M.2 SATA |
| **Front I/O** | VGA, 2x RJ45 connector, 1x USB3.0(Front side),  Power/Reset button, Power/ID LED, M.2 SATA HDD LED, BEEP LED |
| **Management** | iBMC ASPEED AST2400 with a share NIC 1GbE LAN port(BroadCom BCM5720) |
| **PCI-e Slot** | 1 x 16 Gen3 FH/FL, 2 x8 Gen3 LP/HL, 1 x8 OCP Mez with front Panel access, 1 x8 PCIe OCP Mez in a non-front-accessible internal slot to support SAS HBA or Raid-on-Chip with SuperCap. |
| **Board Size** | MB : 600mm x380mm(20-Layer);  I/O Board : 367.5mm x 161.74mm(14-Layer);  BPx15 : 485.5mmx50mm(14-Layer);  Power Expander Board : 130mmx120mm(10-Layer);  PCIEx16 Riser : 137.9mm x 40.3 mm(4-Layer);  PCIEx8 Right Riser: 98.09mm x 44.10mm(6-Layer);  PCIEx8 Left Riser : 97.65 x 44.0 mm(4-Layer);  Mez RAID Card : 110.5 mm x 68mm(10-Layer)  RMC : 358.3 mm x 76 mm (6-Layer) |

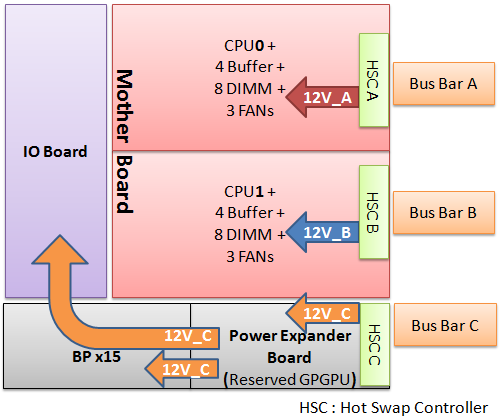
* 1. Power Distribution from Each Bus Bar

Bus Bar A : Max. 522.36W, Typical 464.62W, Usage Power 394.73W

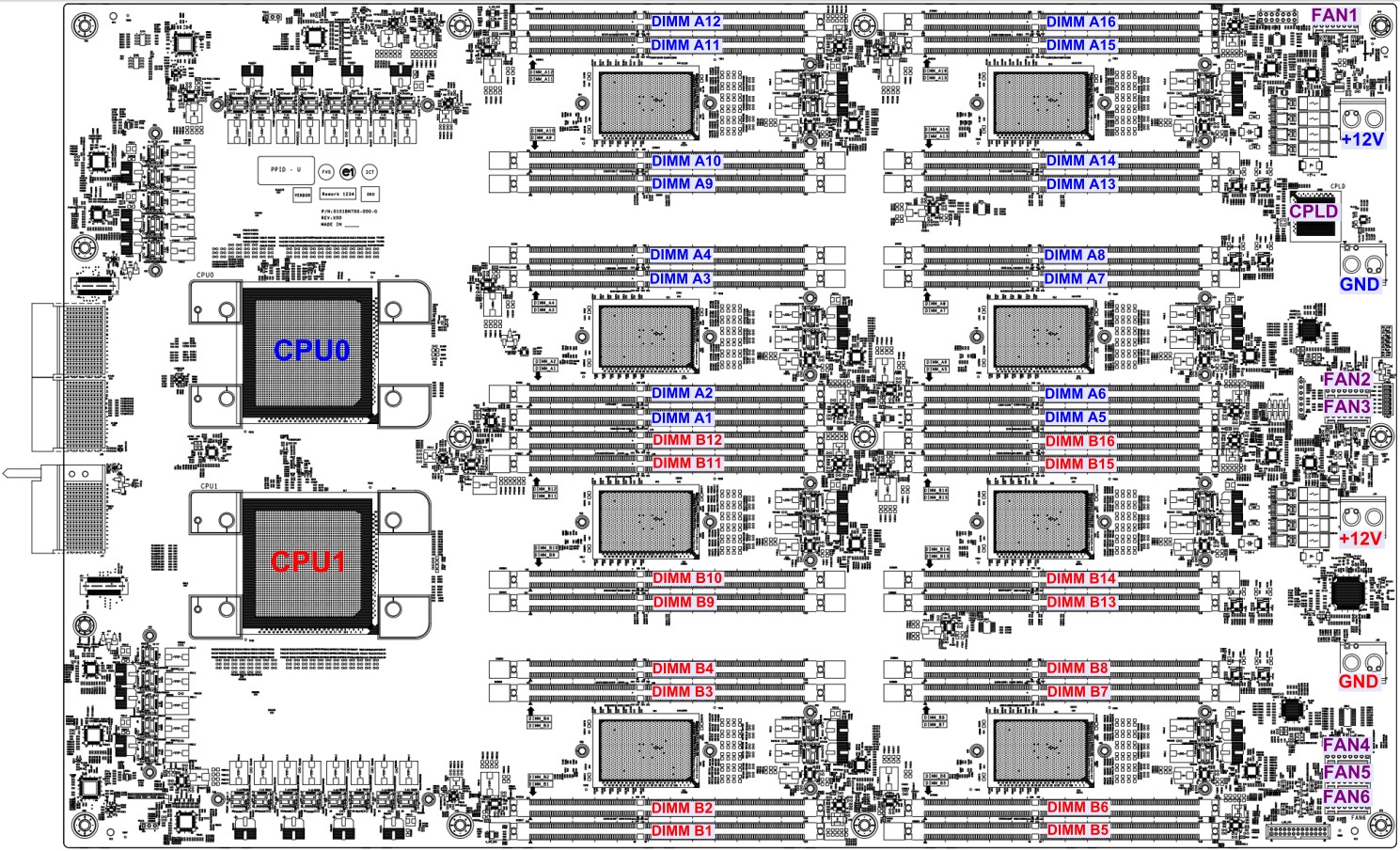
Bus Bar B : Max. 522.36W, Typical 464.62W, Usage Power 394.73W

Bus Bar C : Max. 516.07W, Typical 490.22W, Usage Power 336.52W

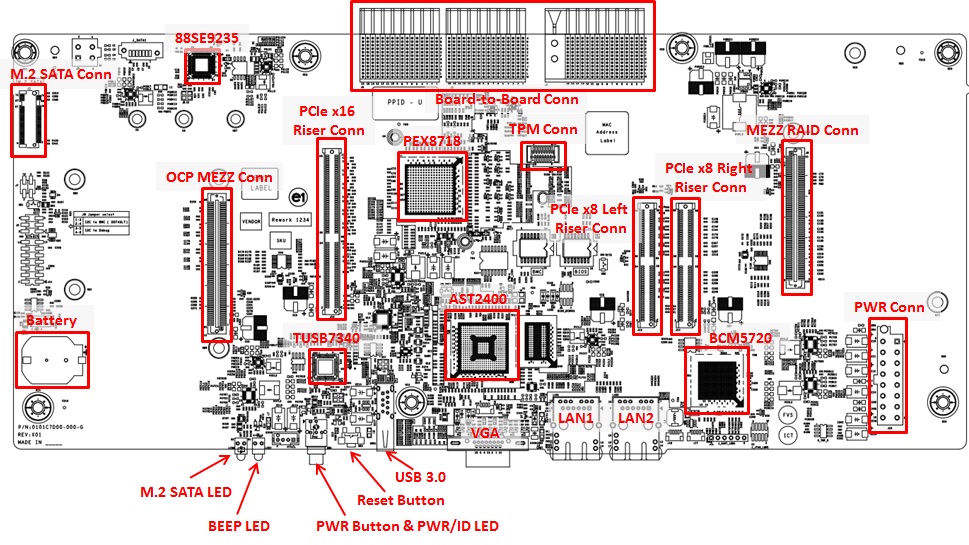
Total usage power : ~1.2KW, attachment is power budget.



* 1. MB Placement



* 1. I/O Board Placement



* 1. Processor and Memory
     1. Processor Feature Set

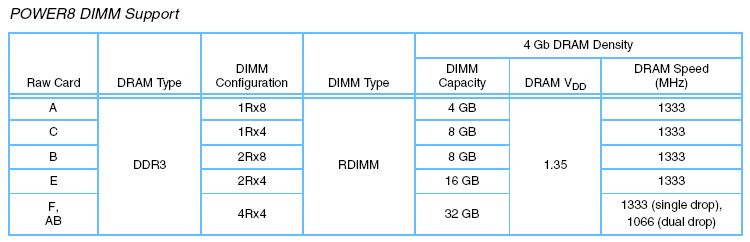
IBM POWER8 “Turismo” SCM Processor x 2, 2296 pins Socket, support up to 12-core, 190W CPU.

* + 1. Memory Buffer

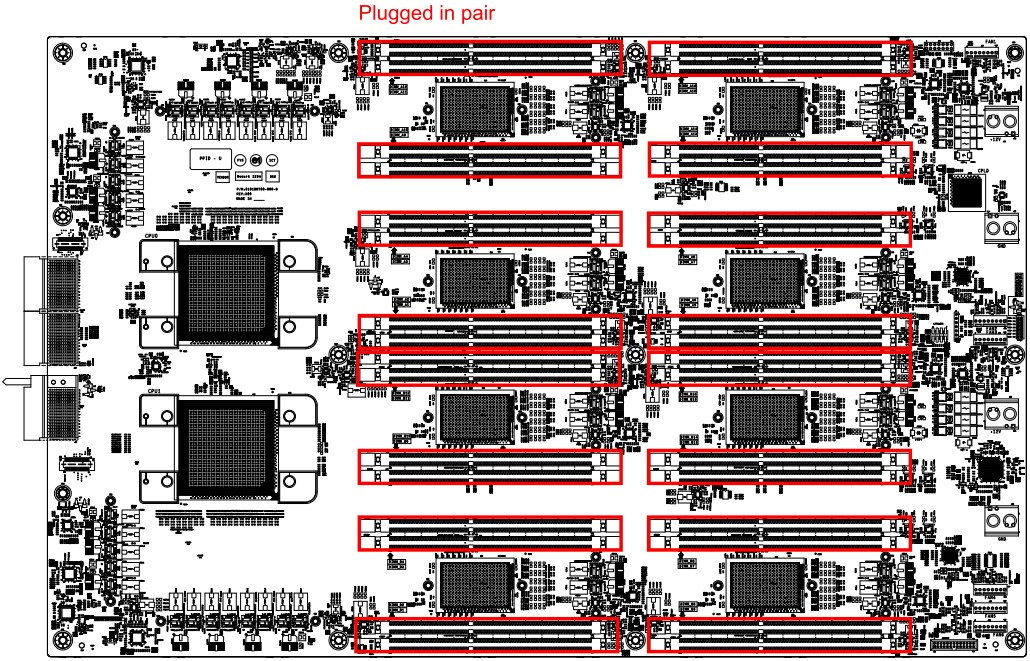
IBM Centaur, 4 Memory buffers per Processor, total 8 memory buffer connect to CPU0/1 through DMI interface.

* + 1. Memory Support

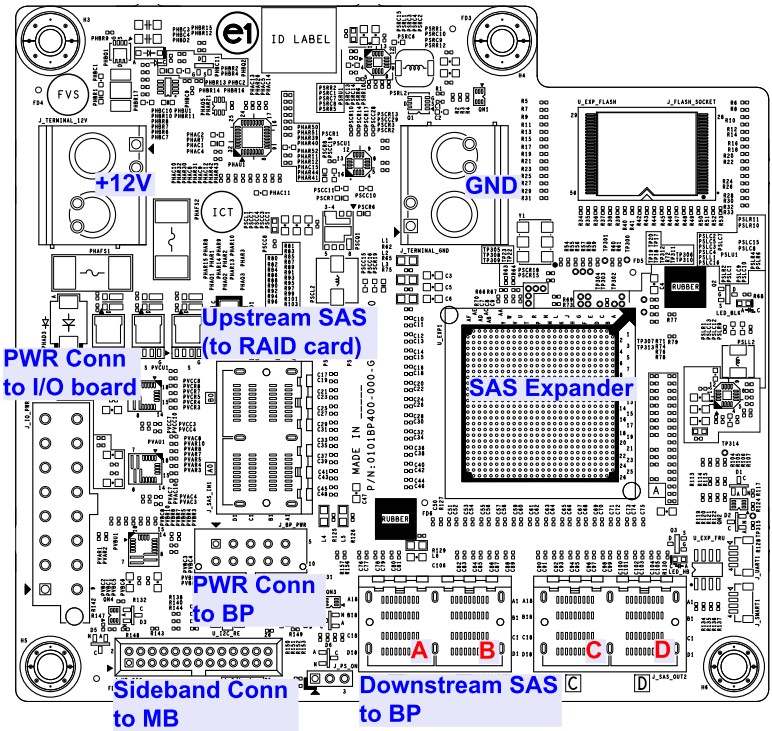
The OpenPOWER memory subsystem supports IS RDIMM DDR3 memory of sizes 4 GB, 8 GB, 16 GB, and 32 GB. All memory configurations run at 1333 Mbps with the exception of the 4-rank dual-drop configuration which runs at 1066 Mbps. Below table shows the configuration of the supported DIMMs.



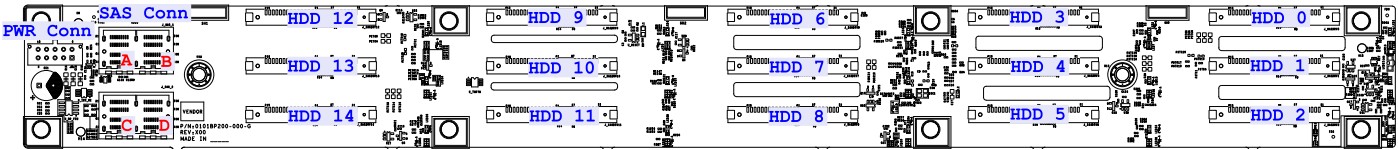
DIMMs must be populated, in pairs on each Centaur, or if memory interleave functions are enabled in system firmware, it quads on each Centaur.



* 1. Storage
     1. Power Expander board Placement



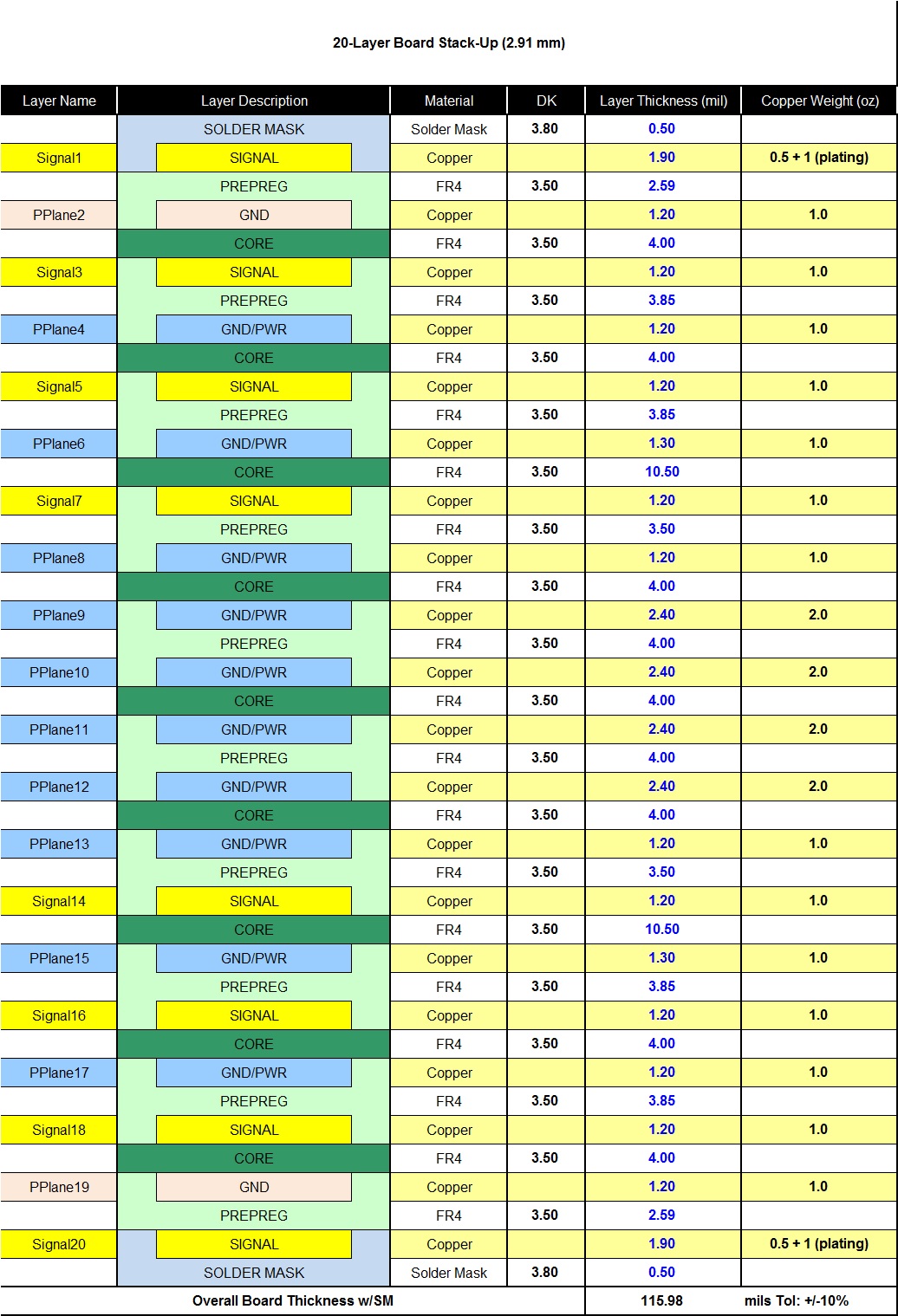
* + 1. BPX15 Placement

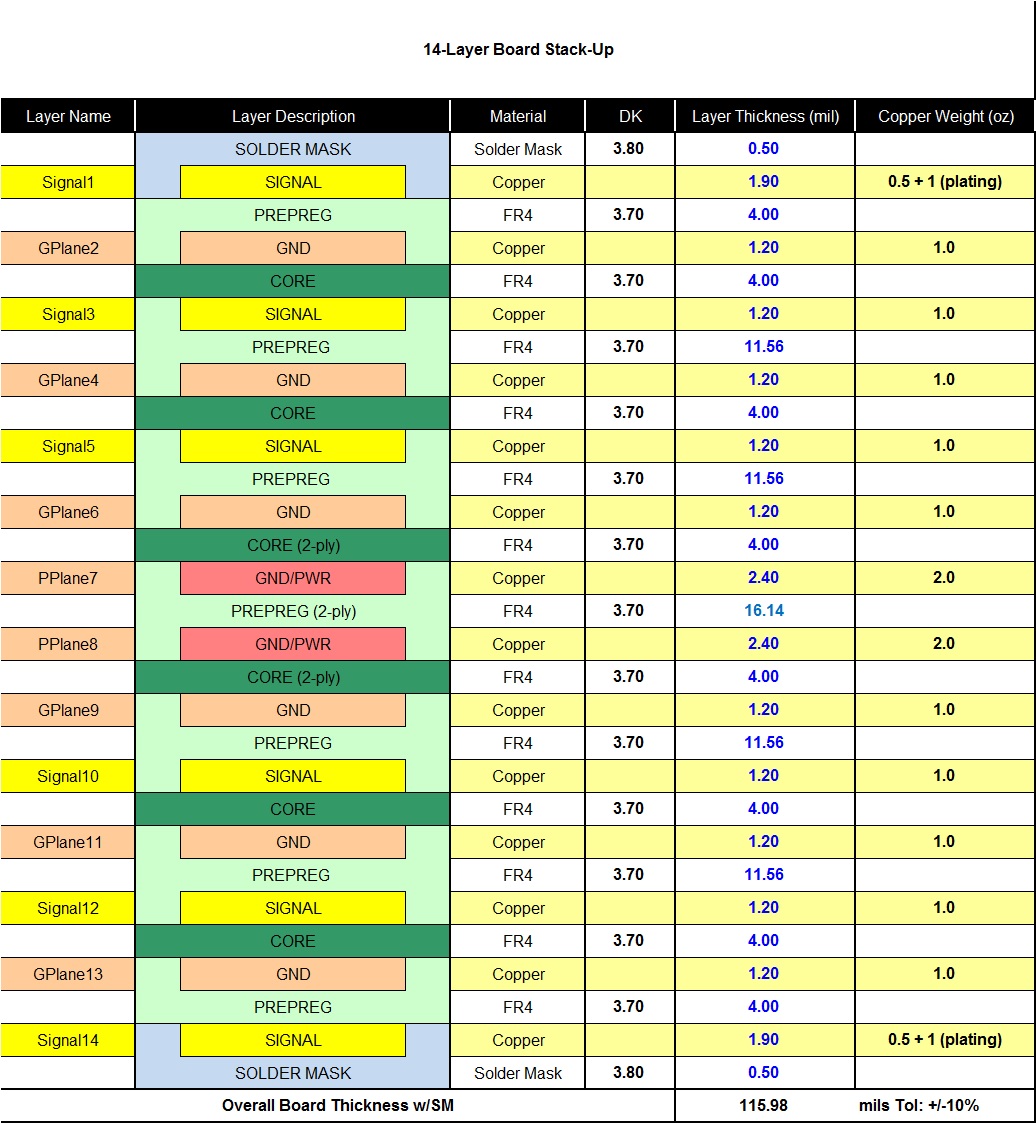


* 1. Printed Circuit Board Information

Each PCB material and stack-up are defined in the figure below.

|  |  |  |
| --- | --- | --- |
| **Board** | **PCB Material** | **PCBA Dimension** |
| **(L\*W\*H)（mm)** |
| MB | IT-150DA (VLP + RTF copper) | 600\*380\*2.65 |
| IO Board | TU-862HF (RTF copper) | 367.5\*161.73\*2.65 |
| BPX15 | IT-150DA (VLP + RTF copper) | 485.5\*50 \*2.82 |
| Power Expander Board | TU-862HF (RTF + HTE copper) | 120 \*130\*2.37 |
| Power Fixture Board | Standard FR4 (HTE copper) | 208.45\*94\*1.59 |
| PCIEx16 Riser | TU-862HF (RTF copper) | 137.9\*40.3\*1.58 |
| PCIEx8 Right Riser | TU-862HF (RTF copper) | 98.09\*44.109\*1.58 |
| PCIEx8 Left Riser | TU-862HF (RTF copper) | 97.65\*44.0\*1.58 |
| Mez RAID | Standard FR4 | 110.05\*68\*1.57 |
| RMC board | Standard FR4 (HTE copper) | 358.3\*76 |

* + 1. MB 20-Layer Stack-up
    2. IO 14-layer Stack-up



# System Firmware (System BIOS )

Barreleye uses OpenPOWER’s open source system firmware, made available under open source licensing schemes, available at <https://github.com/open-power>.

Barreleye machine configuration data files are available here: <https://github.com/open-power/barreleye-xml>

# BMC

The motherboard uses a BMC for various platform management services and interfaces with hardware, BIOS.

The BMC should be a standalone system in parallel to the host. The health status of the host system should not affect the normal operation and network connectivity of the BMC. The BMC cannot share memory with the host system. BMC management connectivity should work independently from the host. If using a shared NIC, there should be no NIC driver dependency for out-of-band (OOB) communication.

* 1. Management Network Interface

The BMC should have both I2C port and RMII/NCSI port for OOB access.

Shared--NIC uses RMII/NCSI interfaces to pass management traffic on BroadCom BCM5720. BCM5720 has 10/100/1000 MDI interface to RJ45(LAN1).

* 1. Local Serial Console and Serial‐Over‐LAN(SOL)

The BMC needs to support two access paths to the serial console:

1. A local serial console on debug header, described in section 8.12.2.
2. A remote console, available via IPMI Serial‐Over‐LAN (IPMI-SOL), or Secure Shell (SSH), through the management network.
   1. Graphic and GUI

Graphic and GUI features integrated in BMC (ASPEED AST2400) chip.

* 1. Remote Power Control and Power Policy

BMC firmware to support remote system power on/off/cycle and warm reboot through the In‐Band or Out-of-Band IPMI, ReST, or SSH commands.

BMC firmware to support power on policy to be last-state, always-on and always-off. The default setting is Last-State. The change of power policy should be supported by IPMI, ReST, or SSH command and take effect without a BMC firmware cold reset or a system reboot.

It should take less than 3 seconds from AC on, for the BMC to process the power button signal and to power the system for POST. A long waiting period for the BMC firmware to get ready before allowing a system POST start is NOT allowed.

* 1. Power and System Identification LED

The motherboard must combine the Power LED and the System Identification LED into a single blue LED at the front side.

There are 4 states of Power/system identification LED depending on system power state, and chassis identify status.

Power off, Chassis identify off: LED consistently off

Power off, Chassis identify on: LED on for 0.1sec, off for 0.9sec, and loop

Power on, Chassis identify off: LED consistently on

Power on, Chassis identify on: LED on for 0.9sec, off for 0.1sec, and loop

Power LED on is defined by the readiness of all power rails

Blinking the Power LED blinking is used as a system identifier. The on time is different during power on and power off.

* 1. BMC Heartbeat LED

LED always Light: AUX PW OK

LED Blink: BMC ACTIVE(FW Ready)

* 1. Power and Thermal Monitoring and Power Limiting

BMC firmware supports platform power monitoring. Power limiting for processor, memory, and platform is required. Access to this function must be available through In-Band and Out-of-Band.

BMC FW supports thermal monitoring, including processor, memory, chipset, and Inlet/outlet air temperatures.

* 1. Sensors

This portion of the specification is still in development. See production files and BoM available alongside this specification for current implementation.

* 1. System Event Log (SEL)

This portion of the specification is still in development. See production files and BoM available alongside this specification for current implementation.

* 1. Fan Speed Control in BMC

BMC I2C connect to HW monitor1/2 to control FAN PWN and read FAN tach. Blue & Red LEDs show FAN status, and these 2 LEDs are controlled by BMC.

* 1. BMC Firmware

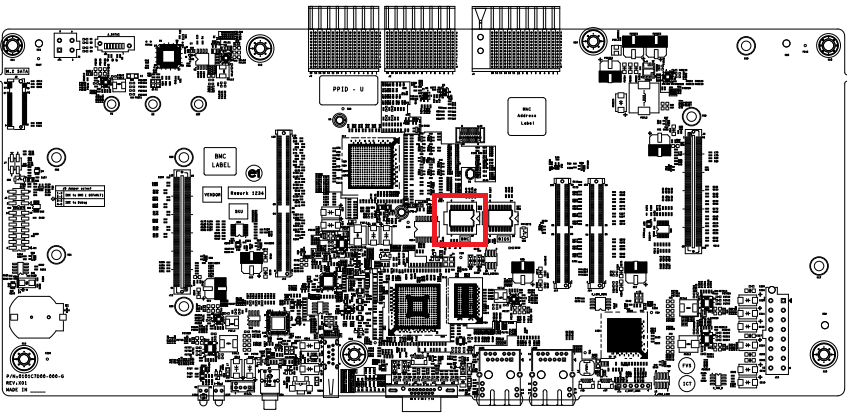
Barreleye can support a variety of BMC firmware solutions, including OpenBMC. OpenBMC is available primarily through two GitHub repositories:

1. The Facebook / OpenBMC repository: https://github.com/facebook/openbmc
2. The OpenBMC / OpenBMC repository: <https://github.com/openbmc/openbmc>
   1. This repository includes most OpenPOWER & Barreleye-specific contributions.
   2. Specific drivers for OpenPOWER machines were contributed here: <https://github.com/openbmc/openbmc/tree/master/meta-openbmc-machines/meta-openpower>

OpenBMC source code is available under its own license scheme.

* 1. BMC Firmware Update Methods
     1. Physical Method

Replace BMC ROM with the updated one. The following figure shows the location of BMC ROM socket on IO board.



* + 1. Host Operating System Method

Run ./socflashtool.sh to update BMC in OS.

When BMC finish updating, system will be shut down since BMC reset and Beep LED(amber) will be lighted. After Beep LED turning off, BMC becomes ready and it can be power on again by pushing power button

* + 1. Direct-to-BMC-Over-Network-Interface Method

This portion of the specification is still in development.

* 1. BMC Update Complex Programmable Logic Device (CPLD)

This portion of the specification is still in development.

* 1. BMC Update BIOS

This portion of the specification is still in development.

# Thermal Design Requirements

Thermal design can support 35degC ambient with two 190W Power8 in 1.25OU sled under one fan fail condition. Please refer to Barreleye Thermal Spec for more details.

# Motherboard Power system

* 1. Input Voltage

The motherboard can accept and operate normally at an input voltage tolerance range between 10.8V and

13.2V. The motherboard's main power under-voltage protection level is 9.5V (Typ.).

* 1. Hot Swap Controller (HSC) Circuit

In order to have better control of the 12.5VDC power input to motherboard.

The motherboard include three hot swap controllers, two for main power and one for stand-by power. The hot swap controller provides:

* Inrush current control when the motherboard is inserted and the server is powered on.
* Current limiting protection for short circuits.
* PMBUS interface to enable the BMC to report server input power.
  1. CPU Voltage Regulator (VR)
     1. CPU Maximum Power

The motherboard shall be designed to handle a processor with a maximum TDP of 190W CPU.

* + 1. CPU VRM Efficiency

The minimum efficiency for the CPU VRM efficiency is 82% over the 30% to 90% load range and 84% over the 50% to 70% load range for TDP power of CPU, measured from the 12.5V input to the VRM output.

* + 1. CPU Core VR Configuration

The guaranteed rewrite count of NVRAM should be equal to 8.

* 1. Memory Buffer Voltage Regulator
     1. DIMM Power Rails

The motherboard design should have DIMM Power Rails for DDR3.

* + 1. DIMM VR Configuration

The guaranteed rewrite count of NVRAM should be equal to 8.

* 1. Voltage Regulator Module Design Guideline

All regulators in the system response to an over-current event must be verified. A typical over-current set point is 25% or more above the maximum load current.

* 1. Hard Drive Power
  2. System VRM Efficiency

High-efficiency VRMs for all other voltage regulators over 20W and under 5W not defined in this specification. All other voltage regulation modules shall be 82% efficiency over the 30% to 90% load range.

* 1. Power On

The motherboard should be set to restore the last power state during AC on/off. This means when the AC cycles on/off, the motherboard should power on automatically without someone pressing the power button. When the motherboard is powered off on purpose, it should be kept off through AC on/off.

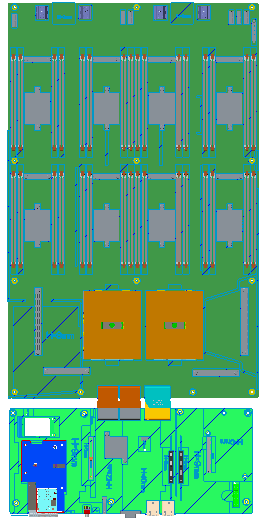
* 1. APSS

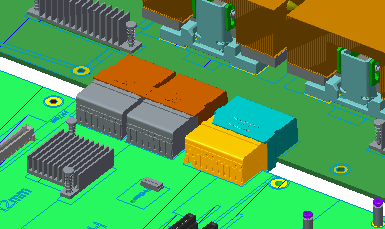
Use for current monitoring of all 240VA, and connect to CPU through SPI interface. On Chip Controller(OCC) of CPU communicates with APSS and calculates the total power consumption of system, then determines if the system needs to do the power capping. APSS also connects to BMC through I2C interface, so BMC can know the system load current as well.

# I/O System

* 1. Impact Board to Board Connector

The Impact board to board connectors are connected between MB and I/O board. There are 3 Impact connectors, refer to the attachment for more details.



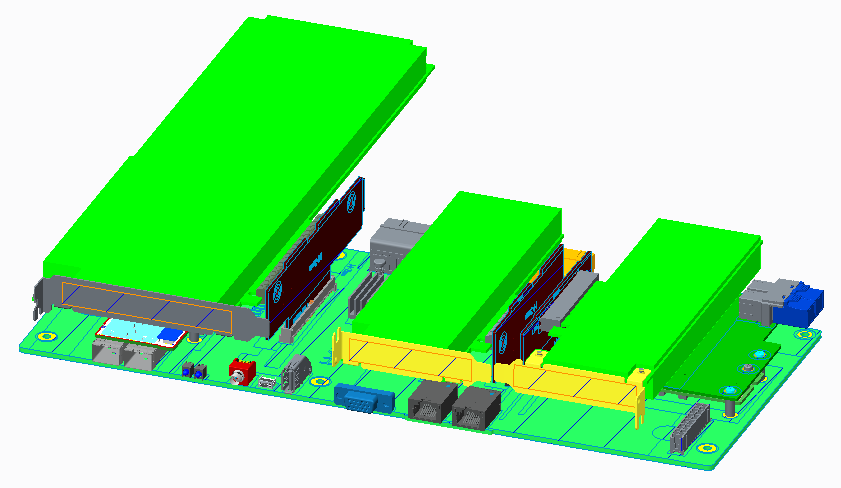
* 1. DIMM Connector

The DIMM connector is SMT type and support DDR3 DIMM. DIMM connectors must also include lubricant/sealant applied by the connector manufacturer which can remain intact after soldering and other manufacturing processes. The sealant is required to displace any voids in the connector gold plating.

* 1. PCIe Slot Connector/Riser Card

The mother board support 3 PCIE cards, but use non-standard PCIE connectors on mother board, need the corresponding riser cards to support standard PCIE cards. Can support 1 x 16 Gen3 FH/FL and 2 x8 Gen3 LP/HL.

See below for the figures of 3 riser cards.



I/O Board

1 x8 LP/HL Gen3

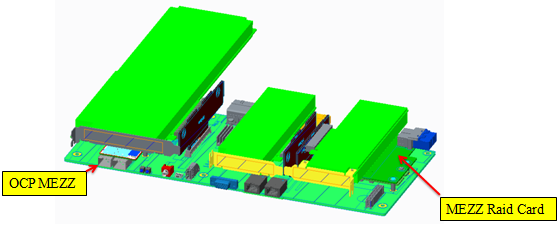
1 x8 LP/HL Gen3

1 x16 FH/FL Gen3

* 1. OCP PCI-E Mezzanine Card

Two OCP mezzanine connectors (support PCIE Gen3) are placed on the IO board to support 1 x8 OCP mez connector with front Panel access and 1 x8 mez connector for internal slot to support Raid-on-chip with battery backup or SuperCap.

1 x8 OCP mez connector with front Panel access supports standard OCP form factor card. Another 1 x8 OCP mez connector for internal slot loosely follows OCP mezzanine specifications, which is only for RAID function and built LSI 3108 on board.



OCP MEZ connector



|  |  |  |
| --- | --- | --- |
| **OCP MEZ Connector Signal Definitions** | | |
| **Signal** | **I/O** | **Definition** |
| PE\_BMC\_MEZZ0\_PRSNT\_N | O | OCP MEZ Connector present pin, connect to pin 120 on MEZ card with 0ohm |
| LAN\_2\_NCSI\_RXER | I | NC‐SI for OOB management |
| LAN\_2\_NCSI\_RXD[0:1] | I |
| LAN\_2\_NCSI\_CRSDV | I |
| LAN\_2\_NCSI\_TXEN | O |
| LAN\_2\_NCSI\_TXD[0:1] | O |
| LAN\_2\_NCSI\_TXEN | O |
| CK\_50M\_NCSI2 | I | NC-SI 50M input clock |
| MEZZ0\_I2C0\_SCL | I | PCIe I2C Clock for Mez slot/EEPROM; |
| MEZZ0\_I2C0\_SDA | I/O | PCIe I2C Data for Mez slot/EEPROM; |
| MEZZ0\_LAN\_3V3STB\_ALERT\_N | O | I2C Alert for OOB management |
| MEZZ0\_OOB\_I2C1\_SCL | I | I2C Clock for OOB management |
| MEZZ0\_OOB\_I2C1\_SDA | I/O | I2C Data for OOB management |
| BMC\_PE\_WAKE\_N | I | PCIe wake up signal |
| CK\_100M\_CP0\_PE\_MEZZ0\_DP/N | I | 1st MB clock output for PCIe devices |
| CLK\_100M\_MEZZ0\_DP/N | I | 2nd MB clock output for PCIe devices |
| PE\_CP0\_E1\_MEZZ0\_CK0\_DP/N[00:07] | I | PCIe Gen3 from CPU to OCP MEZ |
| PE\_MEZZ0\_E1\_CP0\_CK0\_DP/N[00:07] | O | PCIe Gen3 from OCP MEZ to CPU |
| P3V3\_IO | O | 3.3V input power |
| Ground | I/O | Ground pins |

MEZ RAID connector



|  |  |  |
| --- | --- | --- |
| **MEZ RAID Connector Signal Definitions** | | |
| **Signal** | **I/O** | **Definition** |
| PE\_BMC\_MEZZ1\_PRSNT\_N | O | OCP MEZ Connector present pin, connect to pin 120 on MEZ card with 0ohm |
| MEZZ1\_I2C0\_SCL | I | PCIe I2C Clock for Mez slot/EEPROM; |
| MEZZ1\_I2C0\_SDA | I/O | PCIe I2C Data for Mez slot/EEPROM; |
| MEZZ1\_LAN\_3V3STB\_ALERT\_N | O | I2C Alert for OOB management |
| MEZZ1\_OOB\_I2C1\_SCL | I | I2C Clock for OOB management |
| MEZZ1\_OOB\_I2C1\_SDA | I/O | I2C Data for OOB management |
| BMC\_PE\_WAKE\_N | I | PCIe wake up signal |
| CK\_100M\_CP1\_PE\_MEZZ1\_DP/N | I | 1st MB clock output for PCIe devices |
| CLK\_100M\_MEZZ1\_DP/N | I | 2nd MB clock output for PCIe devices |
| PE\_CP1\_E0\_MEZZ1\_CK0\_DP/N[00:07] | I | PCIe Gen3 from CPU to MEZ RAID |
| PE\_MEZZ1\_E0\_CP1\_CK0\_DP/N[00:07] | O | PCIe Gen3 from MEZ RAID to CPU |
| P3V3\_IO | O | 3.3V input power |
| Ground | I/O | Ground pins |

* 1. Network

Support two RJ-45 10/100/1000 LAN ports. NIC Indicators are shown below.



**Activity indicator**

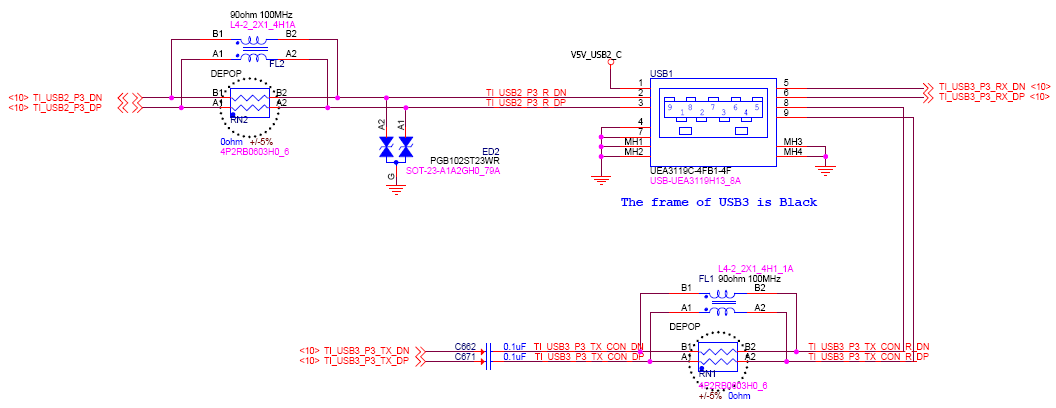
**Link indicator**

|  |  |
| --- | --- |
| **LAN LED Behavior** | |
| **Indicator** | **Indicator Code** |
| Link and activity indicators are off | The NIC is not connected to the network |
| Link indicator is green | The NIC is connected to a valid network at its maximum port speed (1Gbps or 10Gbps) |
| Link indicator is amber | The NIC is connected to a valid network at less than its maximum port speed |
| Activity indicator is green blinking | Network data is being sent or received |

* 1. USB

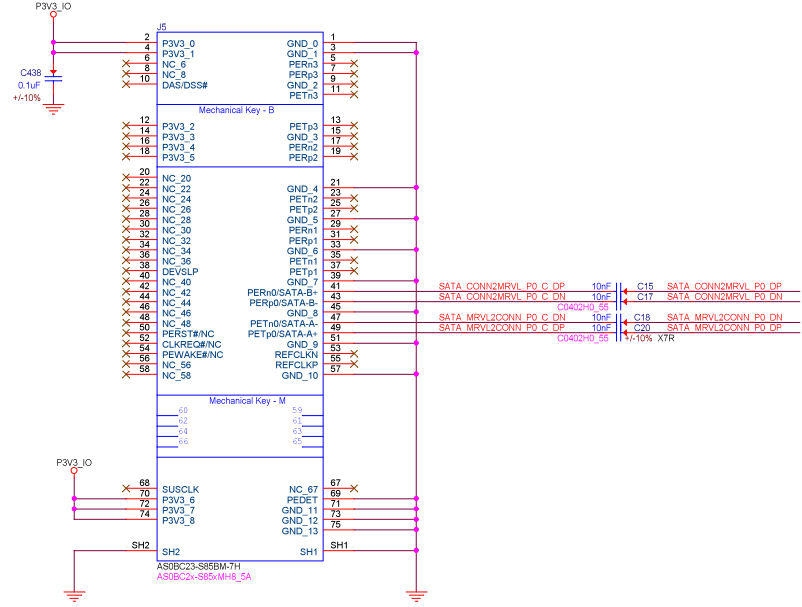
Support one USB3.0 connector put on front side for user used

USB 3.0 Circuit : USB1 is USB3.0 connector, can support USB3.0 device.



* 1. SATA

Support one M.2 connector on I/O board to support M.2 SATA device.

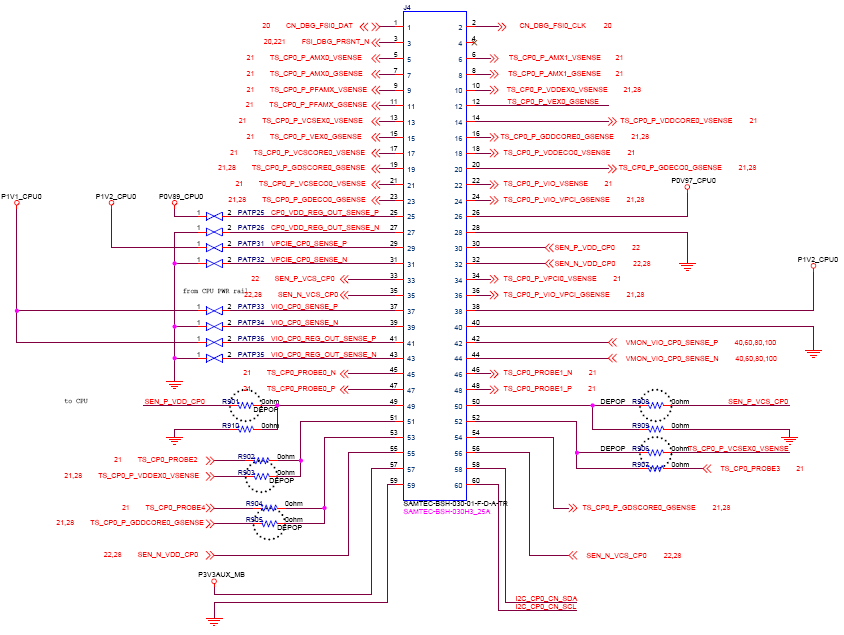


|  |  |  |
| --- | --- | --- |
| **M.2 Connector Signal Definitions** | | |
| **Signal** | **I/O** | **Definition** |
| SATA\_MRVL2CONN\_P0\_C\_DP/N | I | SATA signals from SATA controller to M.2 connector |
| SATA\_CONN2MRVL\_P0\_C\_DP/N | O | SATA signals from M.2 connector to SATA controller |
| P3V3\_IO | O | 3.3V input power |
| Ground | I/O | Ground pins |

* 1. Debug Header

There’s a debug header (J4 Connector), the function is CPU status monitoring and some Power sensor.

J4 Connector



* 1. Switches and LEDs

The motherboard shall include a power switch, a reset switch, a power LED(combine ID LED), an M.2 SATA HDD activity LED and a beep error LED on front side.

* + 1. Switches

Two switches put on front-side, one is POWER button and another is RESET button.

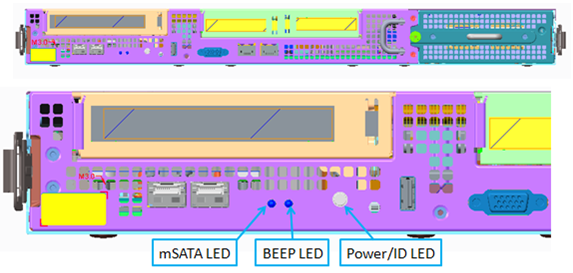
When the motherboard is powered off on purpose, need user to push POWER button to power on the system.

The RESET button is designed to generate a platform reset to reset BMC and TPM module.

* + 1. Power, M.2 SATA HDD & BEEP LEDs

The label describes the functionality of Power, M.2 SATA HDD & BEEP LED.

|  |  |  |  |
| --- | --- | --- | --- |
| **Front I/O LED Behavior** | | | |
| **LED Type** | **LED Color** | **Function** | **LED Pattern** |
| Power LED | Blue | Power LED on is defined by the readiness of all power rails | **Power off, 0Chassis identify off:**  LED consistently off  **Power off, Chassis identify on:**  LED on for 0.1sec, off for 0.9sec, and loop  **Power on, Chassis identify off:**  LED consistently on  **Power on, Chassis identify on:**  LED on for 0.9sec, off for 0.1sec, and loop |
| System Identifiction LED | Blinking the Power LED blinking is used as a system identifier.  The on time is different during power on and power off | Blinking |
| BEEP LED (Warning LED for fault) | Yellow | This LED replaces the functionality of the PC speaker. The motherboard causes the LED to illuminate for the same duration and sequence as the PC speaker would normally beep. The LED allows for easier diagnosis in a noisy data center environment | **TBD** |
| M.2 SATA LED | Green | SATA controller detected M.2 SATA HDD, but M.2 SATA hard drive no activity | Always light |
| M.2 SATA hard drive activity. This LED illuminates when M.2 SATA hard drive is activity | Blinking |
| Red | M.2 SATA failure / fault | Always light |

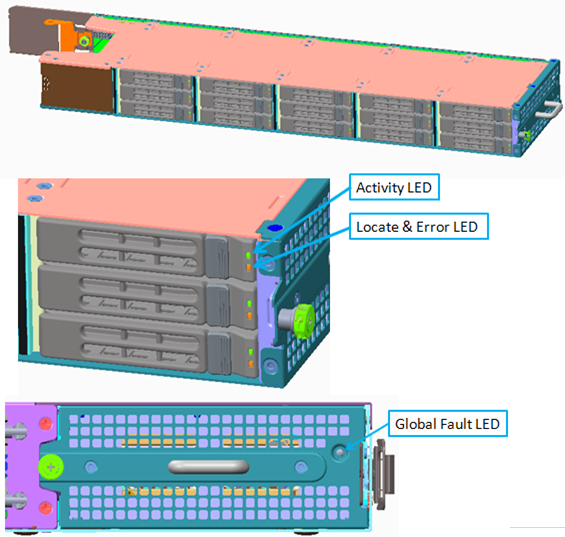


M.2 SATA LED

* + 1. HDD Carrier & Tray LEDs

Controlled by expander FW.

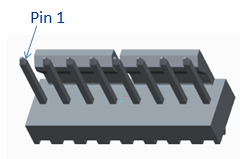
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **HDD Carrier and Tray LED Behavior** | | | | |
| **Location** | **LED Type** | **LED Color** | **Function** | **LED Pattern** |
| HDD Carrier | Locate LED | Green |  | |
| Error LED | Amber |
| Activity LED | Green |
| HDD Tray | Global Fault LED | Amber | “link” down errors between SEB and HDD drives – When HDDs occur “FAULT”, “PRD\_FAULT”, “PR\_ABORT” or “HOT\_SPARE” event | Always light |
| “link” down errors between the RoC & SEB | ON 500ms  OFF 500mS |



* 1. Fan Connector & LEDs
     1. Fan Connector

The motherboard has six fan connectors, and support one fan fail functionality.

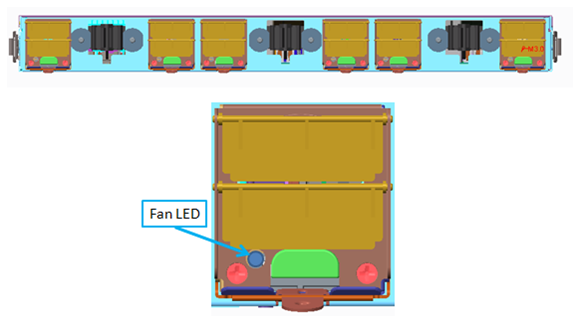
The fan connector pin definitions as below, support a dual rotor fan that shares a PWM control signal but has separate tachometer signals. And support two LED to show FAN status.



|  |  |  |
| --- | --- | --- |
| **Fan Connector Signal Definitions** | | |
| **Pin** | **Wire** | **Definition** |
| 1 | White Wire | LED Power, Connect to 3.3V AUX |
| 2 | Blue Wire | Blue LED - |
| 3 | Red Wire | Red LED - |
| 4 | Blue Wire | Fan Tach of Front Fan |
| 5 | White Wire  Green Wire | PWM of Front FAN  PWM of Rear FAN |
| 6 | Yellow Wire | Fan Tach of Rear Fan |
| 7 | Red Wire  Orange Wire | Main Power of Front Fan, Connect to 12V  Main Power of Rear Fan, Connect to 12V |
| 8 | Black Wire  Brown Wire | GND of Front Fan  GND of Rear Fan |

* + 1. Fan LEDs

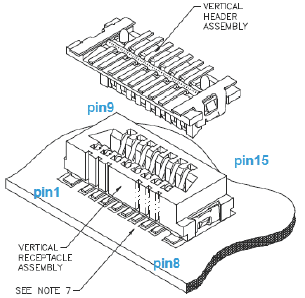
|  |  |  |  |
| --- | --- | --- | --- |
| **Fan LED Behavior** | | | |
| **LED Color** | **Function** | **LED Pattern** | **Comment** |
| Blue | Fan normal operation | Always light | Bi-color LED and integrated Fan modules |
| Red | Fan fault | Always light |



* 1. TPM Connector

A 15pin vertical receptacle connector (Figure 18) is defined on the motherboard for the LPC TPM module. The connector pin definition on the motherboard side is shown in the table below. Use an FCI 91911‐31115 receptacle or its equivalent on the motherboard.

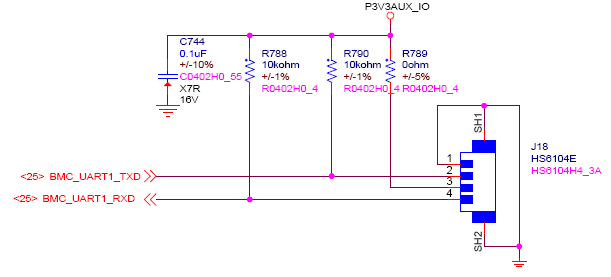
The TPM module is a 23mm(L)x 13mm(W) x 1.57mm(T) PCB with an FCI/91911-31515 header or its equivalent in the center of the module and a **TBD** TPM chip.



|  |  |  |  |
| --- | --- | --- | --- |
| **TPM Connector Signal Definitions** | | | |
| **Pin** | **Description** | **Pin** | **Description** |
| 1 | LPC\_CLK\_33M | 9 | P3V3 |
| 2 | LPC\_RST\_N | 10 | TPM\_PRSNT\_N |
| 3 | LPC\_LAD0 | 11 | NC |
| 4 | LPC\_LAD1 | 12 | LPC\_SERIRQ |
| 5 | LPC\_LAD2 | 13 | GND |
| 6 | LPC\_LAD3 | 14 | GND |
| 7 | LPC\_FRAME\_N | 15 | NC |
| 8 | NC |  |  |

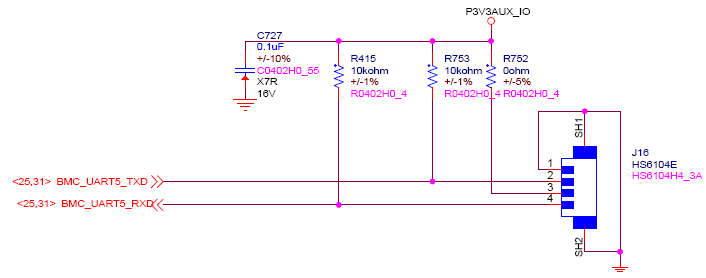
* 1. UART Connector
     1. System UART

There is a system UART connector J18, which can be redirected to be controlled by LPC bus as physical UARTs of host system.



* + 1. BMC Debug UART

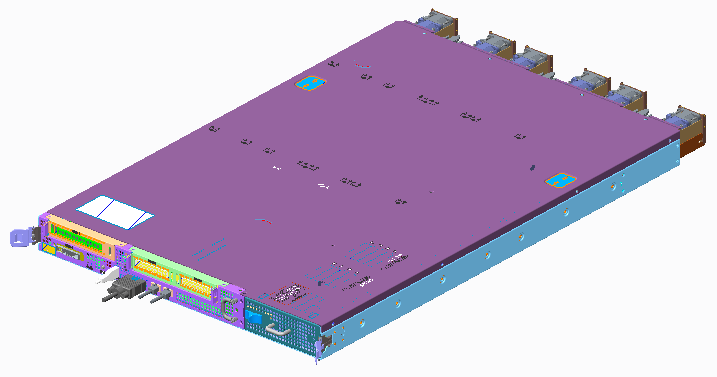
There is a debug UART connector J16 only for for BMC console, which is only for BMC designer debug used.



# Mechanical

* 1. Sled

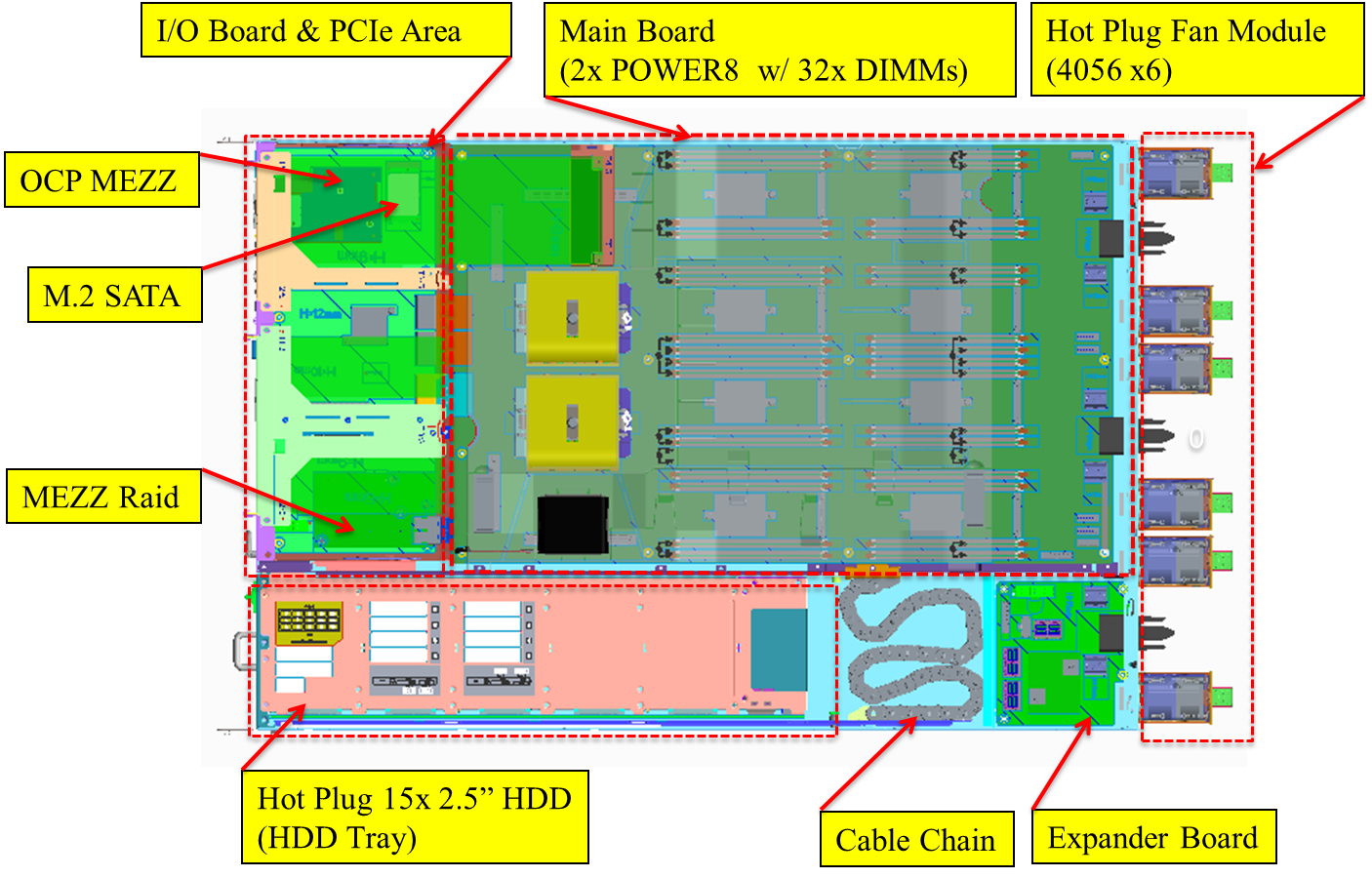
The 1.25OU sled has the dimensions, 537x897.1x56.8mm.



* 1. Top View

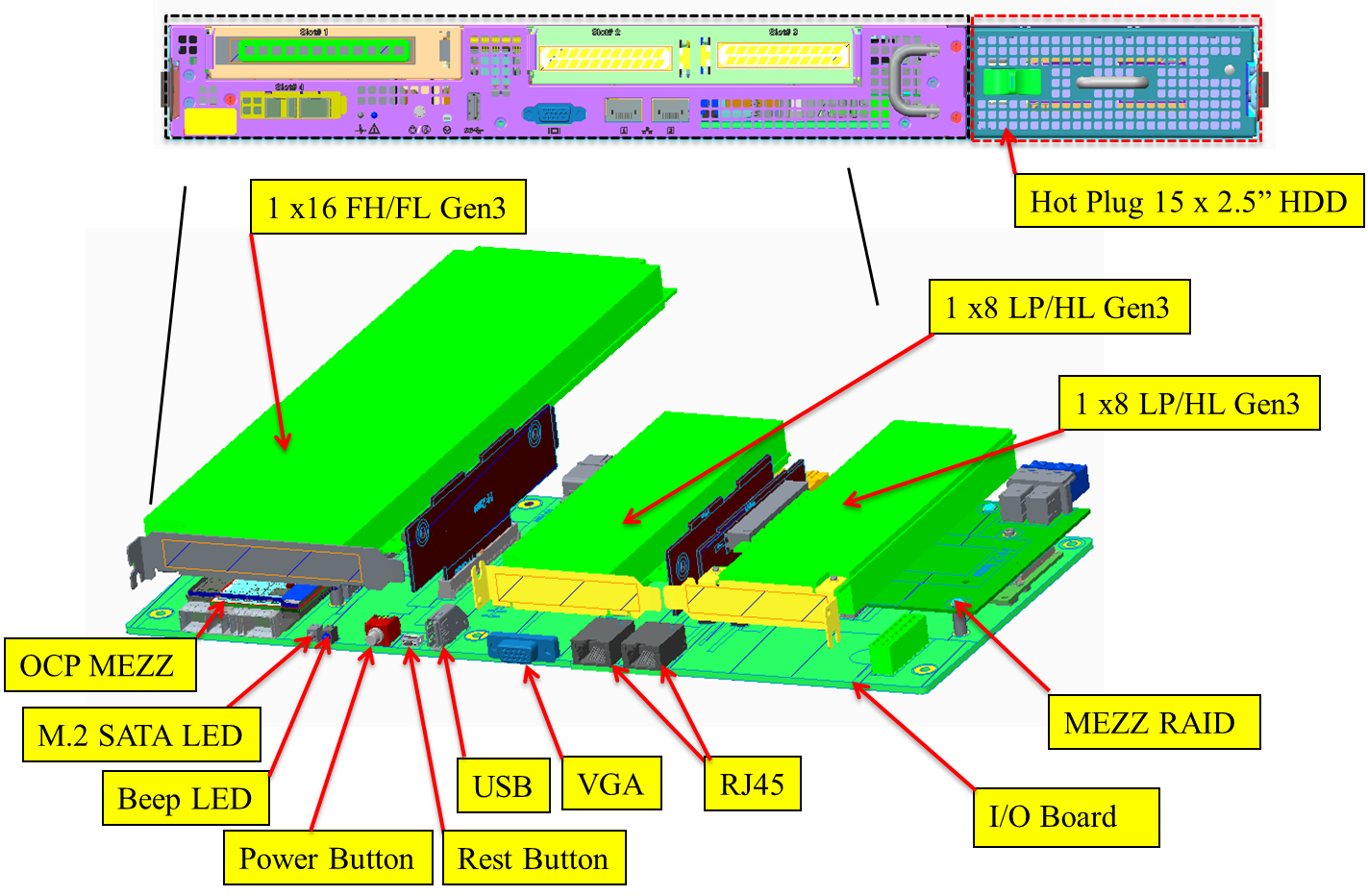
Barreleye supports hot-pluggable 2.5” HDD drives and Fan modules. There are 4 main boards in the system.

They are Main board, I/O board, Expander board and HDD BP.



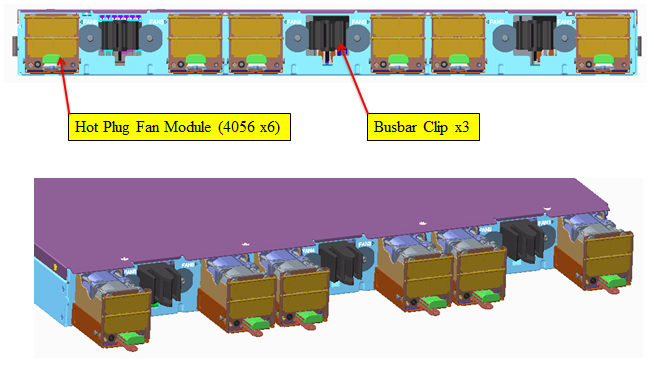
* 1. Front View

Barreleye supports two x8 LP/HL Gen 3, one x16 FH/FL Gen3 cards and one OCP MEZ Raid Card. The I/O connectors are located on the front. There is one HDD Tray on the right which contains 15pcs Hot-Pluggable 2.5” HDD drives.



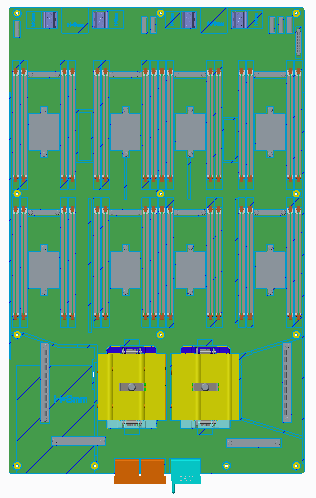
* 1. Rear View

There are three standard OCP Bus bar clips and 6 Hot-pluggable Fan Modules on the rear wall.



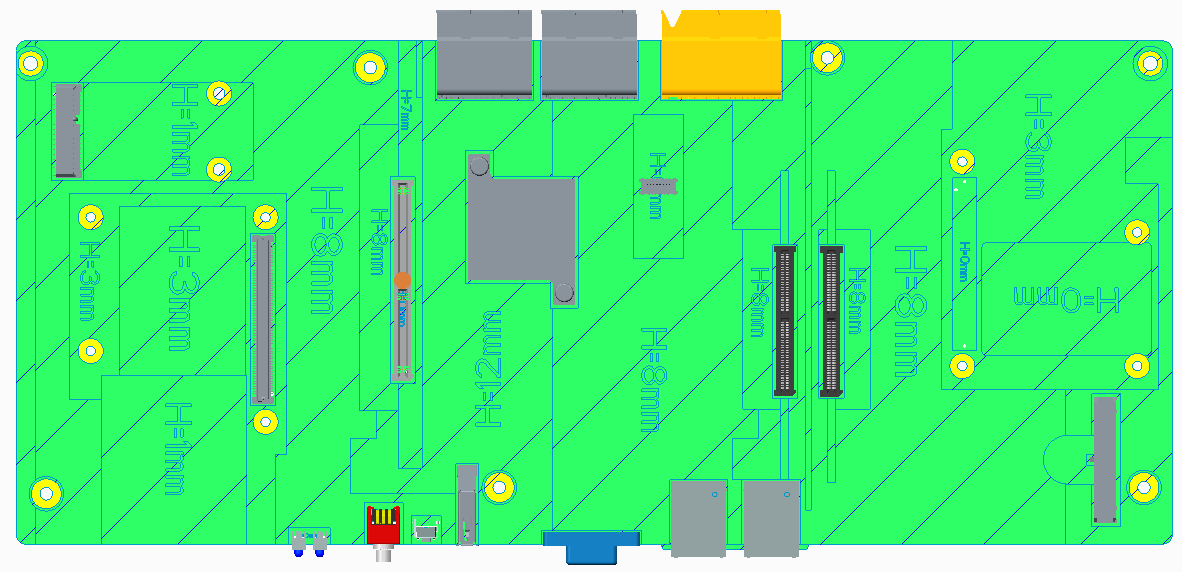
* 1. MB

The dimensions of Main board are 600x380mm. It supports two Power CPUs and 32 DIMMs.



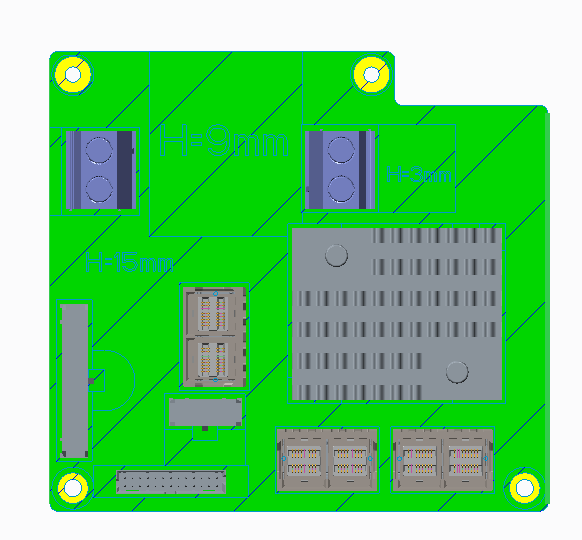
* 1. I/O Board

The dimensions of I/O board are 367.5x160mm. It contacts to Main board through the BTB connectors.



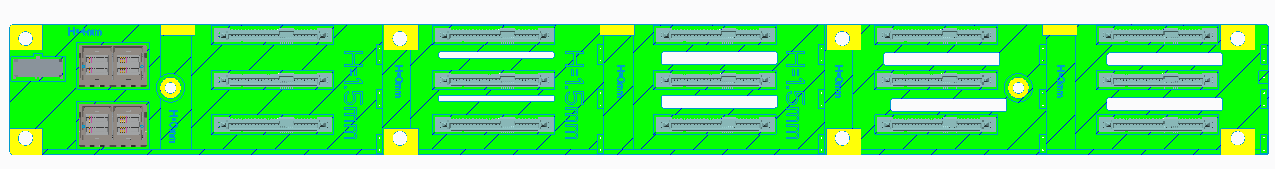
* 1. Power Expander Board

The dimensions of Power Expander board are 130x120mm. It conducts the SAS signal and Power to I/O board and HDD BP through the cables.



* 1. BPx15

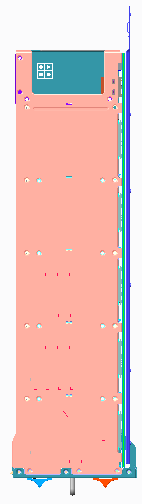
The dimensions of HDD BP are 485.5x50mm.



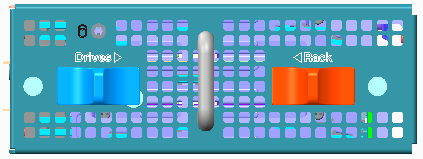
* 1. Hard Drive Tray

The dimension of Hard Drive Tray is 573.8mm (L) x 146.1mm (W) x 53.6mm (H).

* + 1. Top View



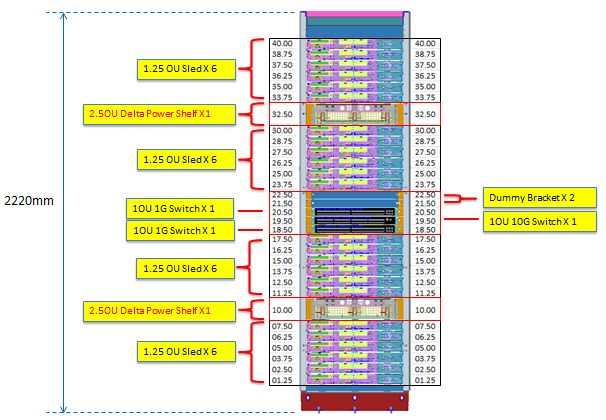
* + 1. Front View



* 1. Rack

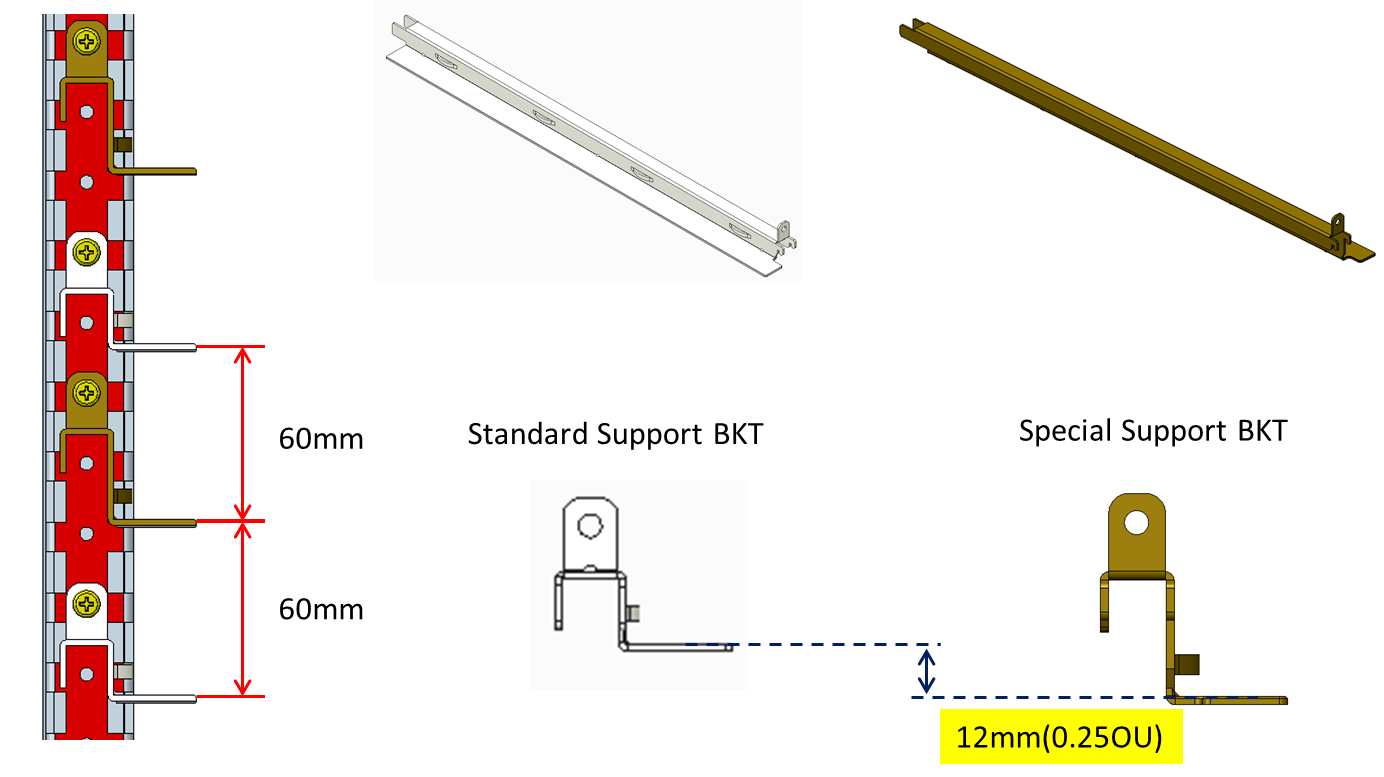
Barreleye Rack is one standard OCP rack. The configuration shows below. The Switch zone is in the middle.

One Powershelf to support 12 sleds is on the top and another Powershelf with 12 Sleds on the bottom.



* 1. Rack Knife

In order to accommodate the 1.25OU sled into this standard OCP rack, except the standard Support Bracket, we have one special Support Bracket which has 12mm gap from the standard one. These two kinds of brackets are assembled on the rack alternately.



# Lunch Box

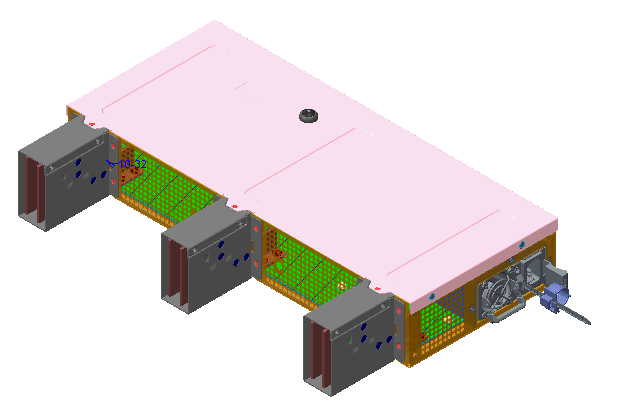
* 1. Lunch Box Feature

Lunch box is a power fixture which supports OCP 1U or 2U sled to power on without OpenRack.

* + 1. Top View

Power Supply

Power Button



**12V**

**GND**

**12V**

**GND**

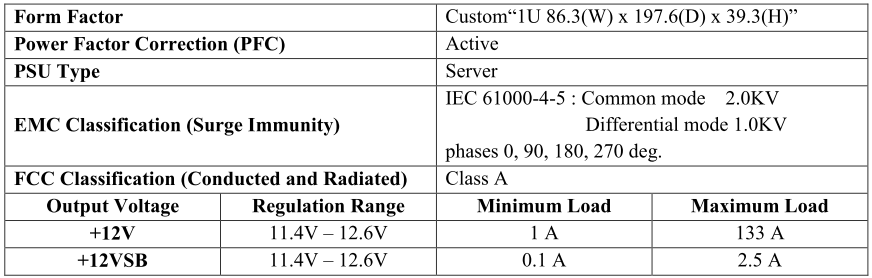
**12V**

**GND**

* 1. Power Supply Specification

The power supply resides in lunch box is Chicony R1K6A008L. Additional information is provided below.

* + 1. Power Supply Overview



AC Input Voltage Range

