

PROJECT NAME : MD90-FS0
PROJECT CODE : S14043-0
Major Chipsets : Haswell EP Processor + Wellsburg (PCH)
I/O Chipsets : I350 + ASPEED AST2400
Team Member List :

Members	Name	TEL Ext.	Email
PM			
HW Engineer			
Project Leader			
ME Engineer			
SI Engineer			
SW Engineer			
Layout Engineer			
FW Engineer			
DQA Engineer			
Thermal			
Validation Engineer			
CPE			
FAE Engineer			
Sales			

OCP identification Only

PCB part number

PCB1
PCB[10PMD90FS0-TN-S10B_10PMD90FS0-TX-S10B]

EC Key 入 *1 SMT 階

SERIAL Number part number

SFIS1
SFIS[12LB4-020004-0AR_12LB4-020004-00R]

EC Key 入 *1 SMT 階

MAC Label part number

MAC_LB1
MAC[12LB4-016006-2AR_12LB4-016006-20R]
DED_MAC
MAC[12LB4-016006-2AR_12LB4-016006-20R]

EC Key 入 *6 DIP階

MAC_LB2
MAC[12LB4-016006-2AR_12LB4-016006-20R]
SHA_MAC
MAC[12LB4-016006-2AR_12LB4-016006-20R]

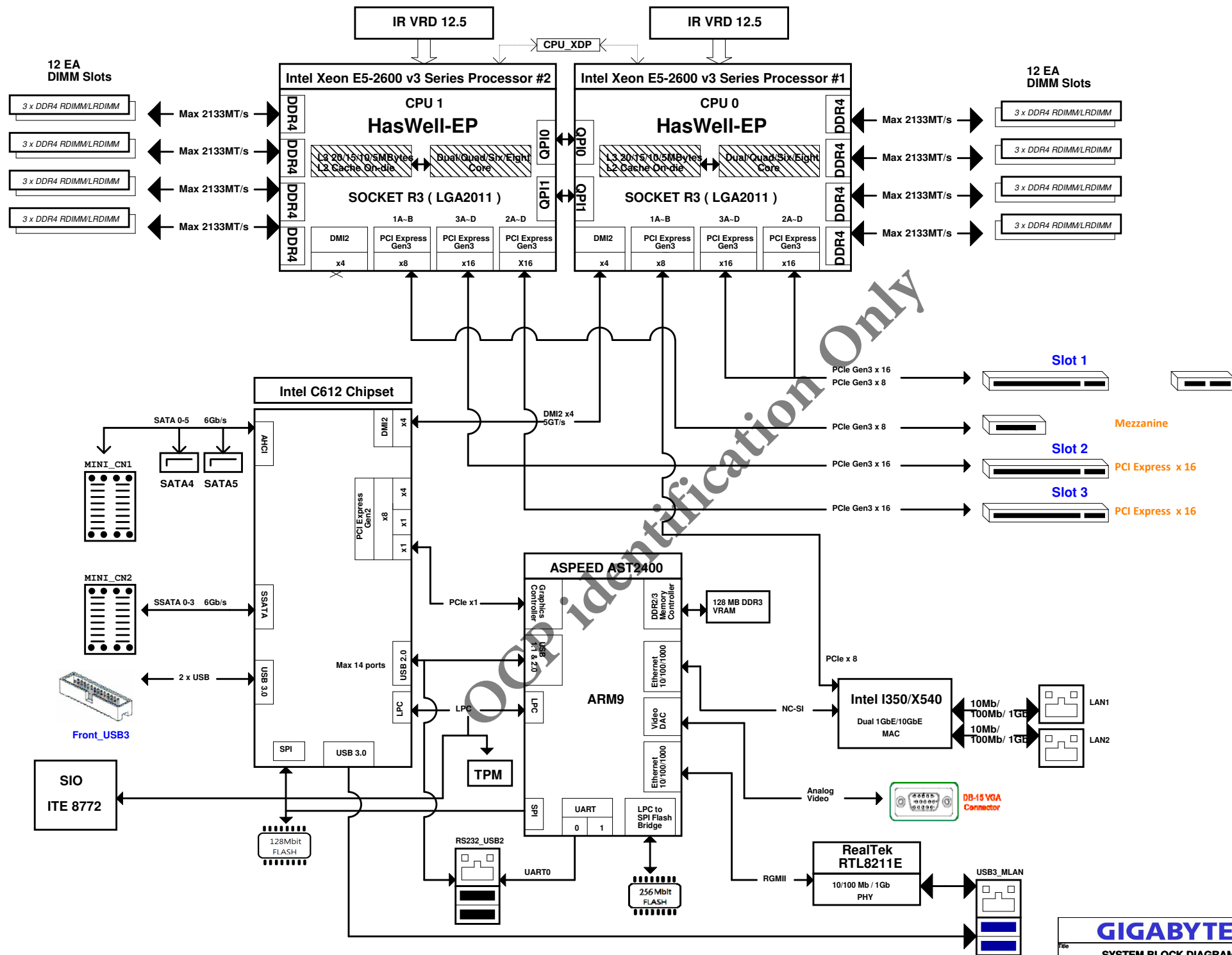
GIGABYTE™			
Title			
COVER			
Size	Document Number		Rev
Custom	MD90-FS0		1.0
Date:	Wednesday, July 29, 2015		Sheet 1 of 231

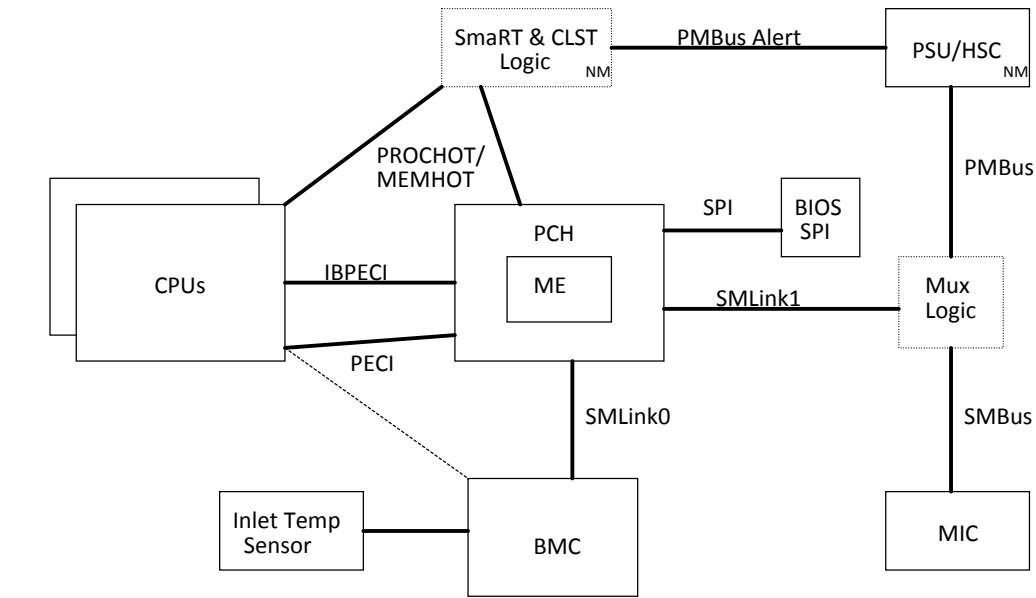
OCP identification Only

GIGABYTE™		
Title		
PAGE INDEX AND TITLE		
Size	Document Number	Rev
Custom	MD90-FS0	1.0
Date:	Tuesday, June 09, 2015	Sheet 2 of 231

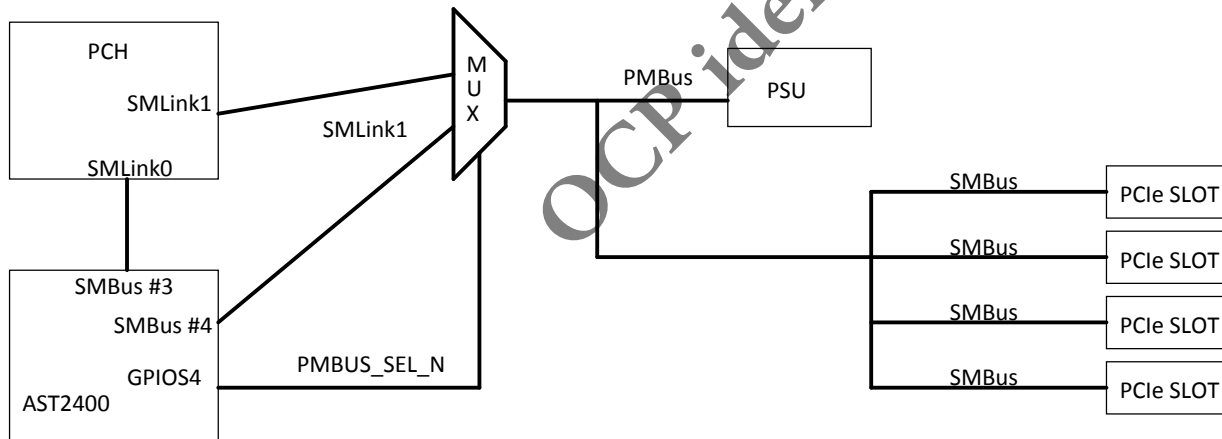
OCP identification Only

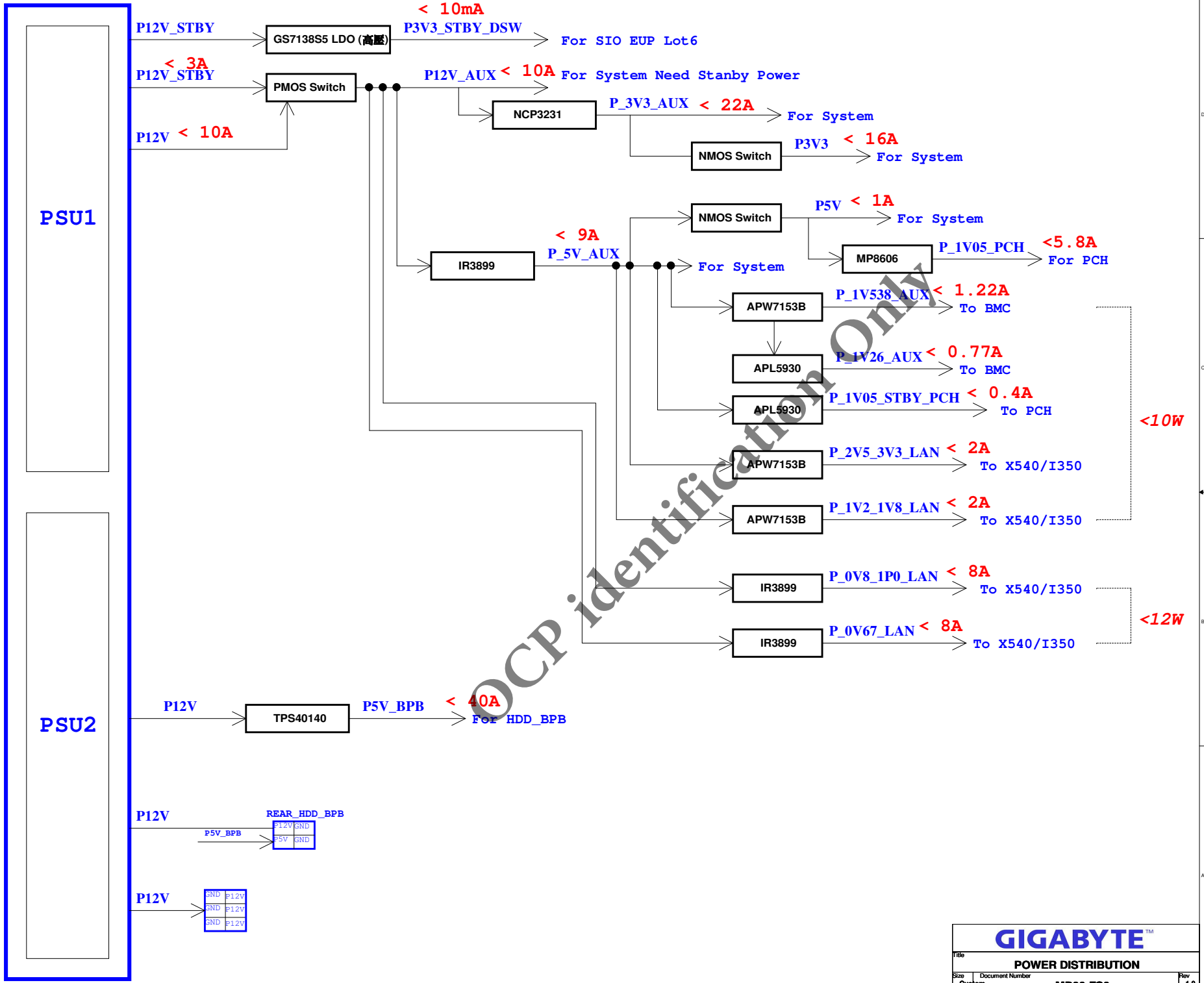
GIGABYTE™			
Title		MECHANICAL DRAWING	
Size	Document Number	Rev	
Custom	MD90-FS0	1.0	
Date:	Tuesday, June 09, 2015	Sheet	3 of 231



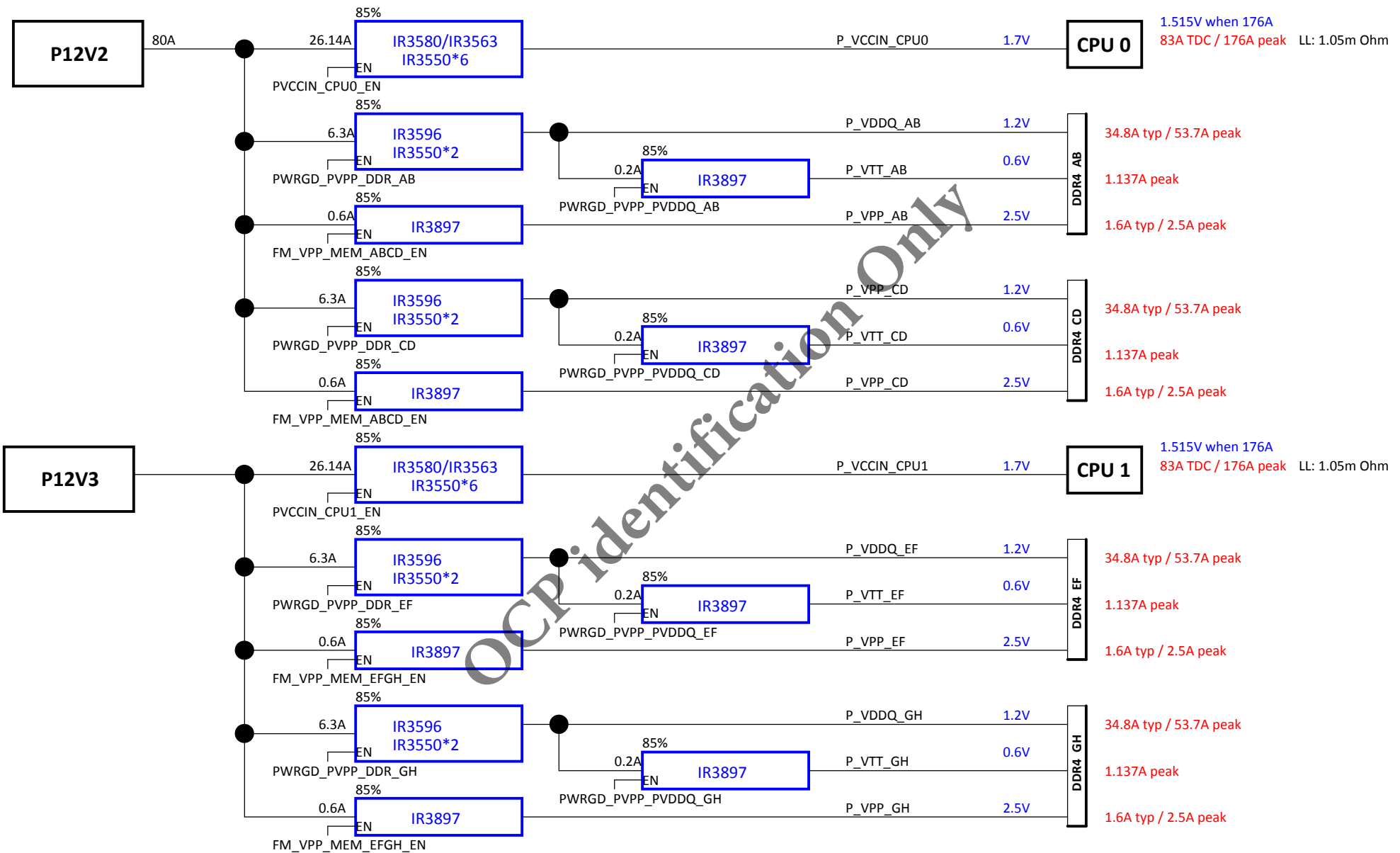


Mux Logic





VR BLOCK DIAGRAM-1



VR BLOCK DIAGRAM-2

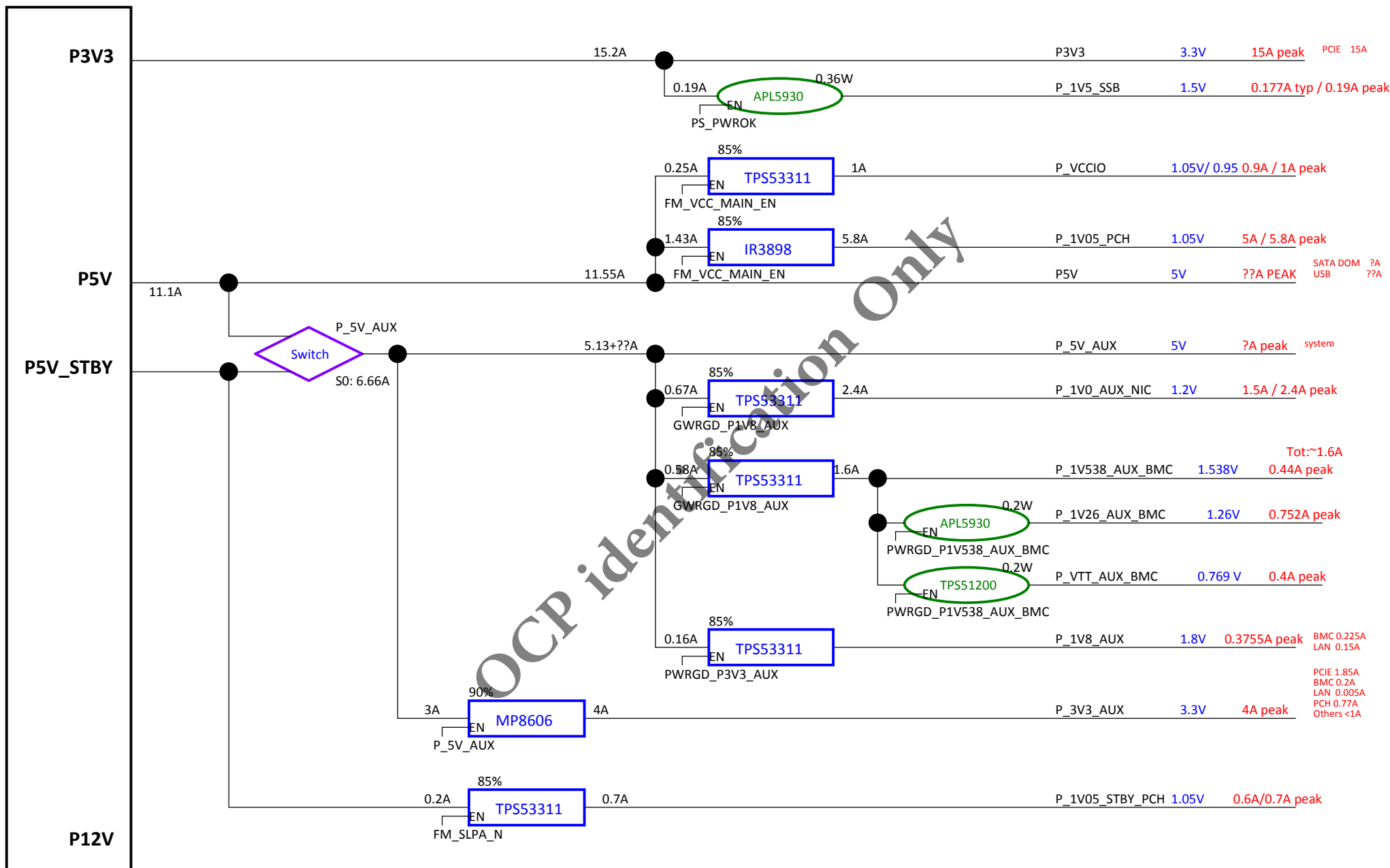
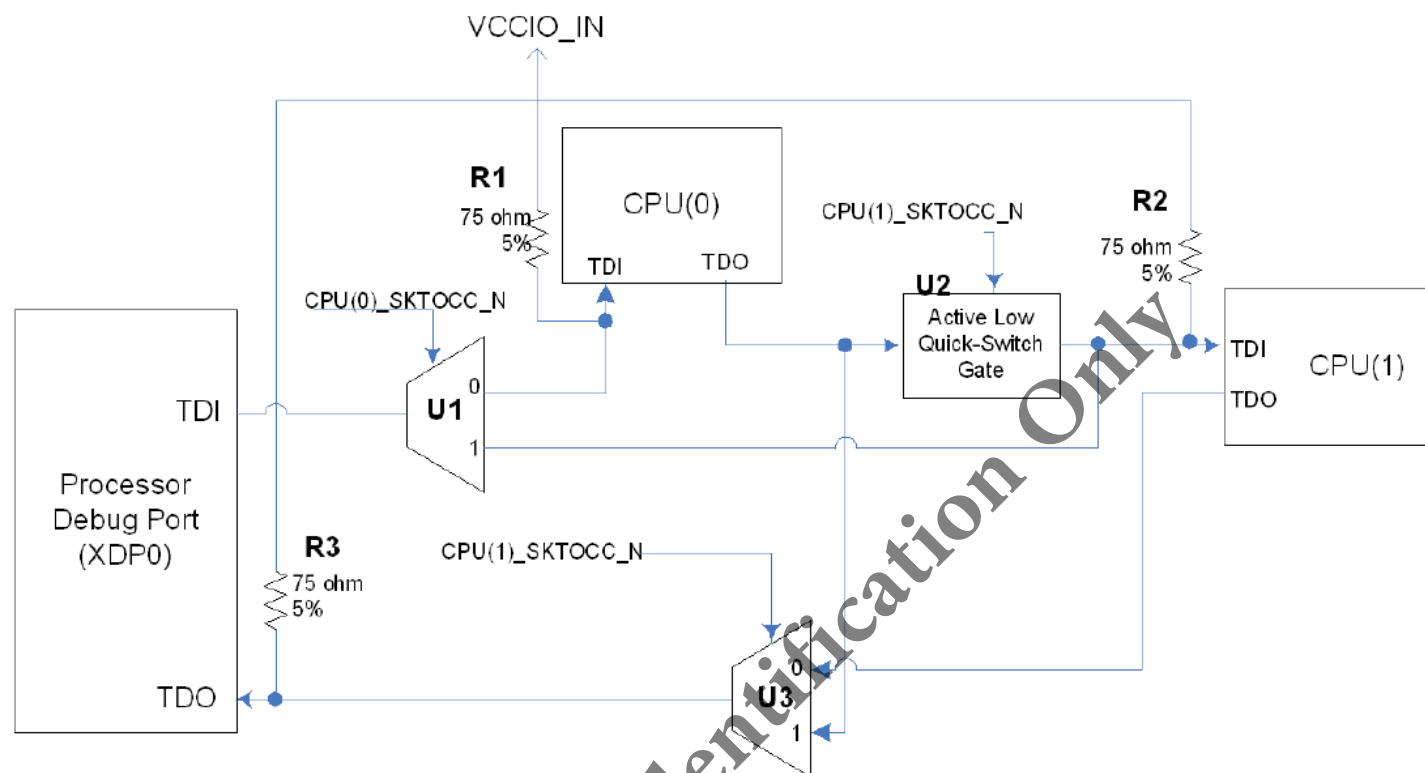


Figure 378. Processor XDP 2S TDI-TDO Topology with Automatic Bypass Quick Switches



CAD Notes:

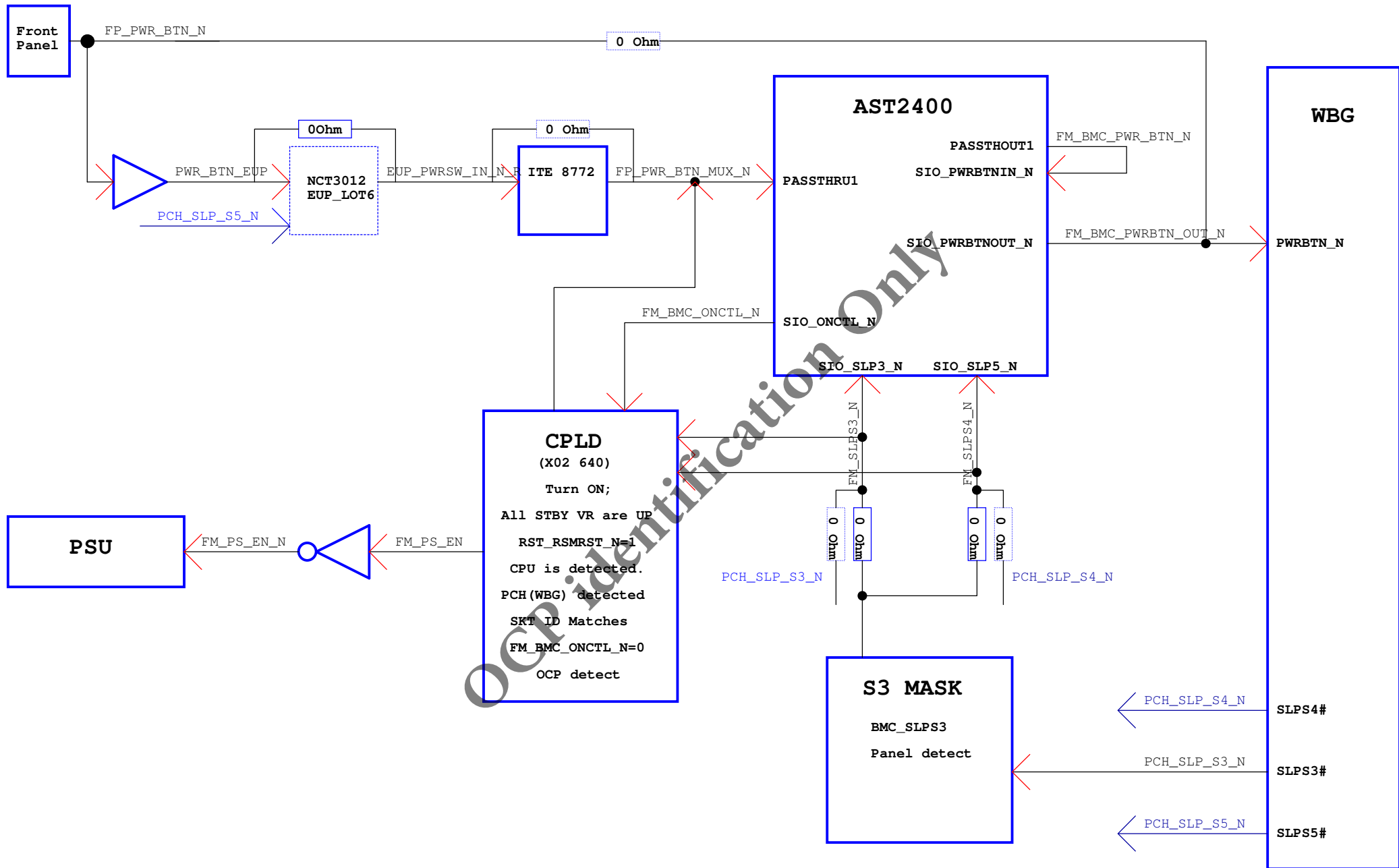
- Place R1 and R2 to within 200ps of the CPU(0) and CPU(1) TDI pin respectively
- Place R3 to within 50ps of XDP TDO pin
- Place U1 to within 1.1" of both U2 and U3.
- Stub length on TDI and TDO is 200ps.
- No trace length constraint for TDO and TDI traces

U1 and U3 = 2:1 Mux/Demux with Max Ron of 20ohm, Max Capitanace of 20pF (ex. NC7SB3157 or NC7SB3257)
 U2 = Active LOW enable 1-bit Bus Switch with Max Ron of 6 ohm, Max Capacitance of 20 pF (ex. 74CBTLV1G125)

Note: it is acceptable to replace R1 and R3 with 51ohm 5% resistor.

OCP identification Only

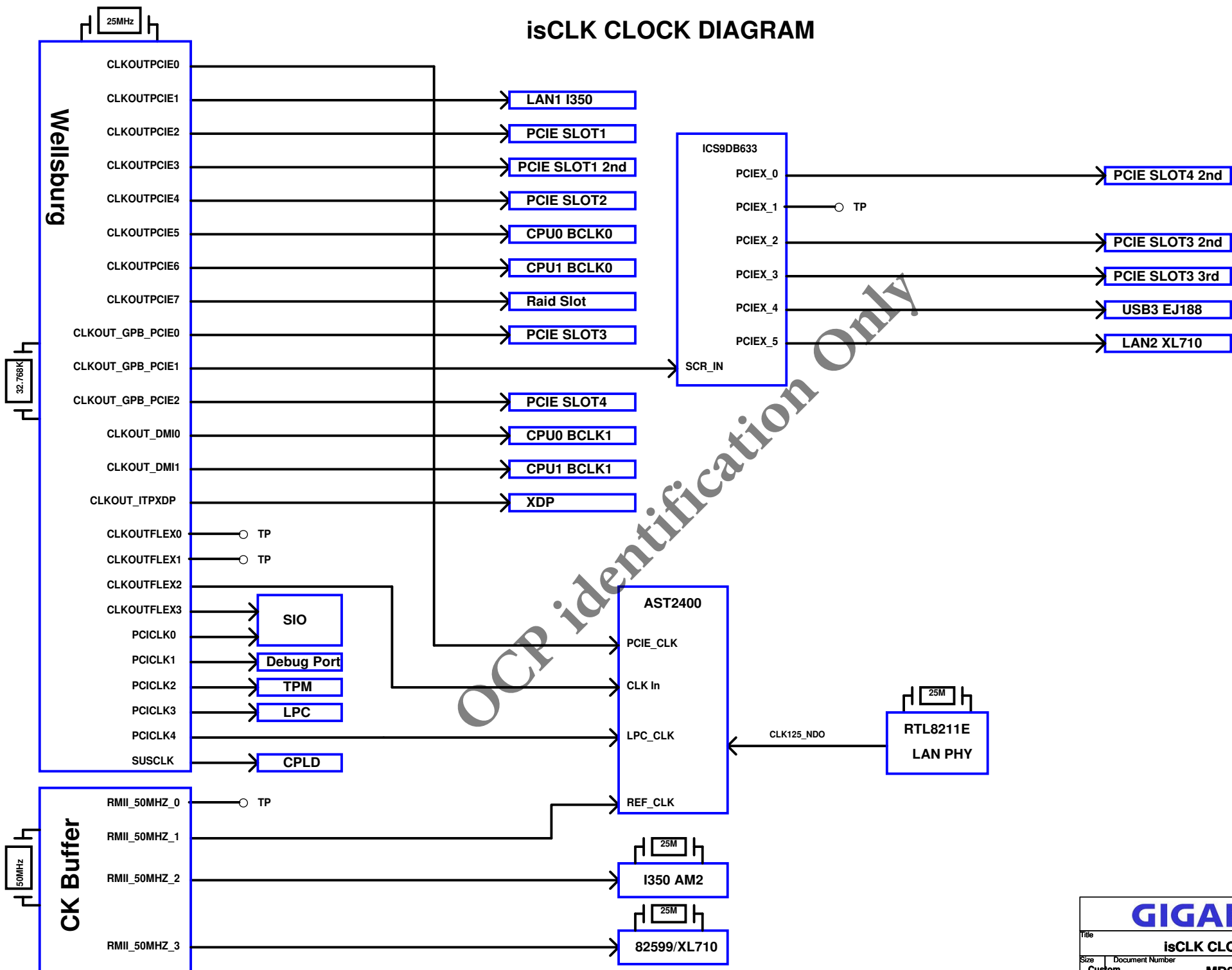
GIGABYTE™		
Title		
XDP/JTAG BLOCK DIAGRAM(PCH)		
Size	Document Number	Rev
Custom	MD90-FS0	1.0
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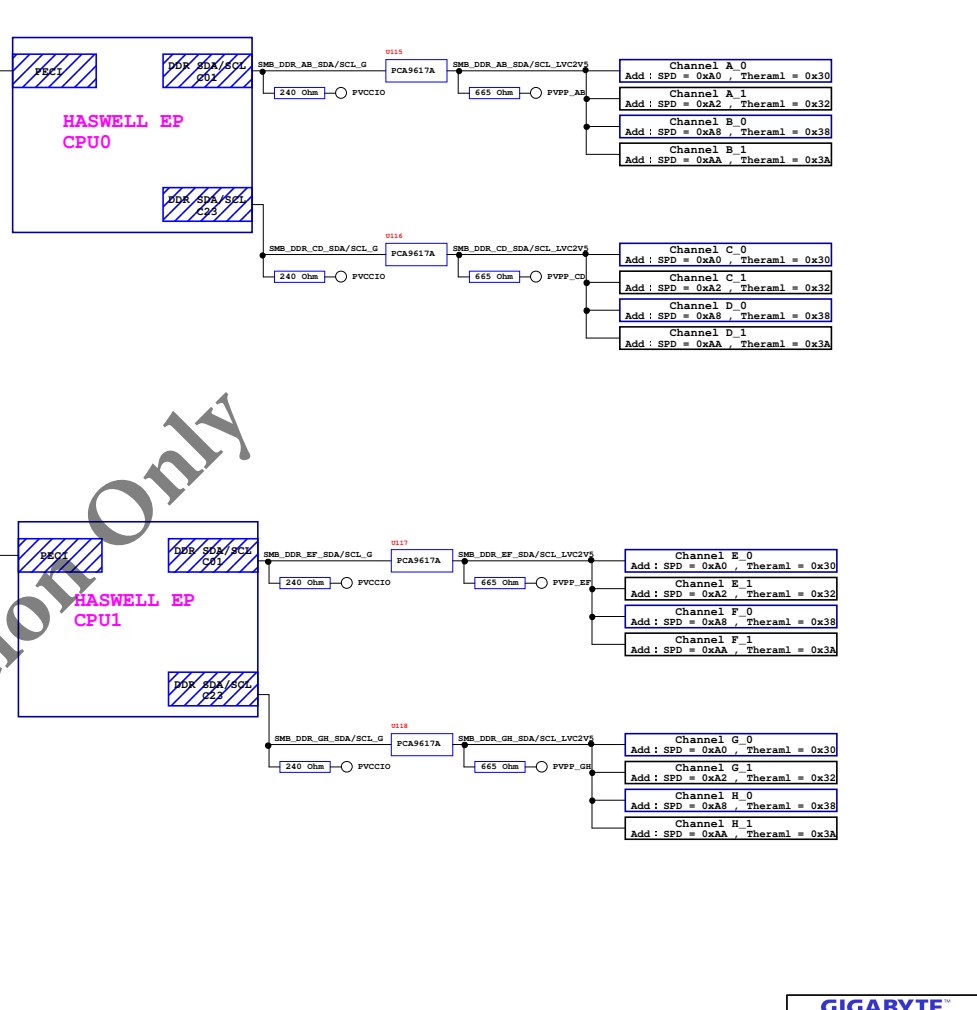


OCP identification Only

GIGABYTE™		
Title		
PWR GOOD/ RST DIAGRAM		
Size	Document Number	Rev
Custom	MD90-FS0	1.0
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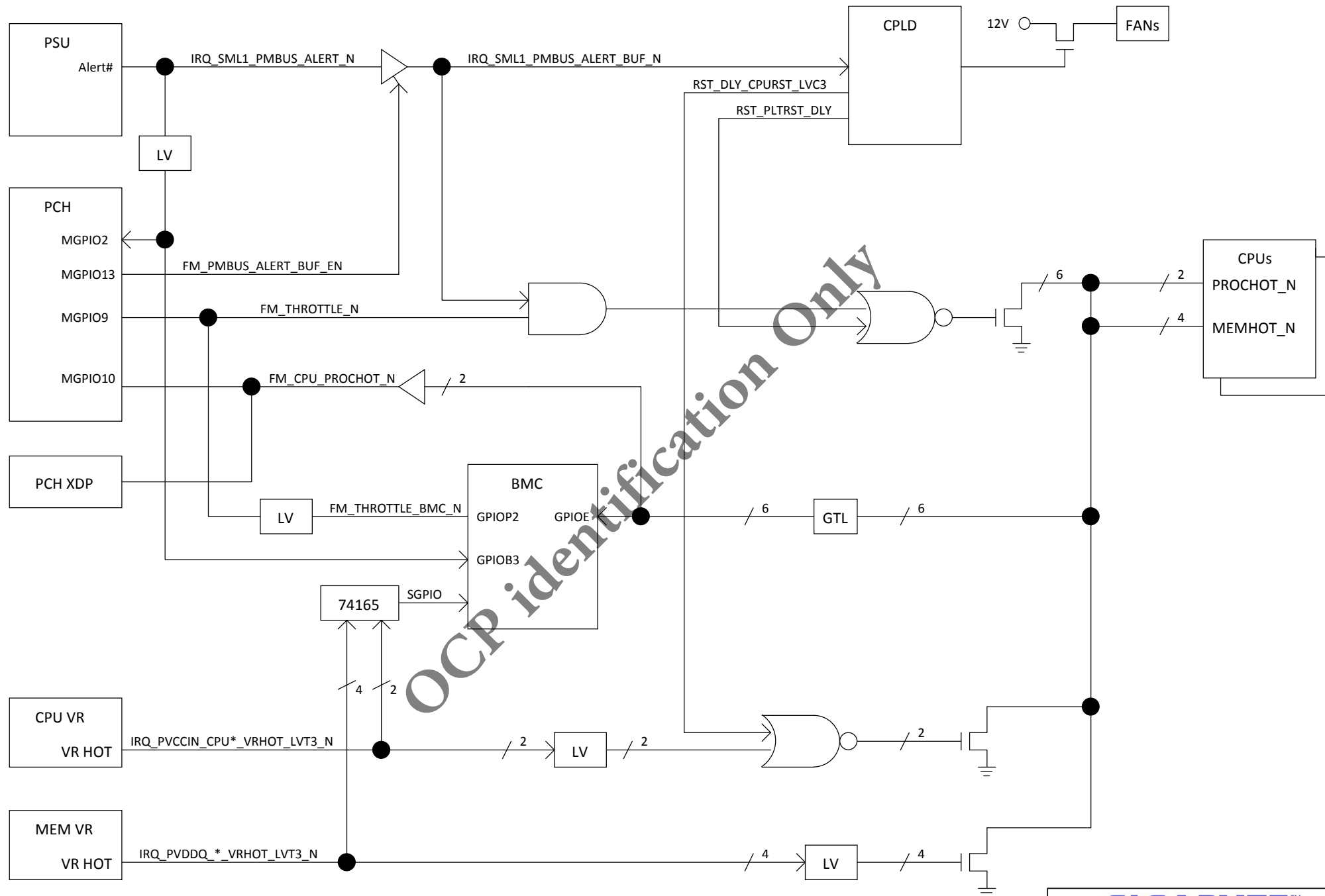
isCLK CLOCK DIAGRAM





OCP identification Only

GIGABYTE™		
Title		
POWER SEQUENCE DIAGRAM		
Size	Document Number	Rev
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OCP identification Only

GIGABYTE™		
Title =====CPU0, CPU1=====		
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231		

CPU0A

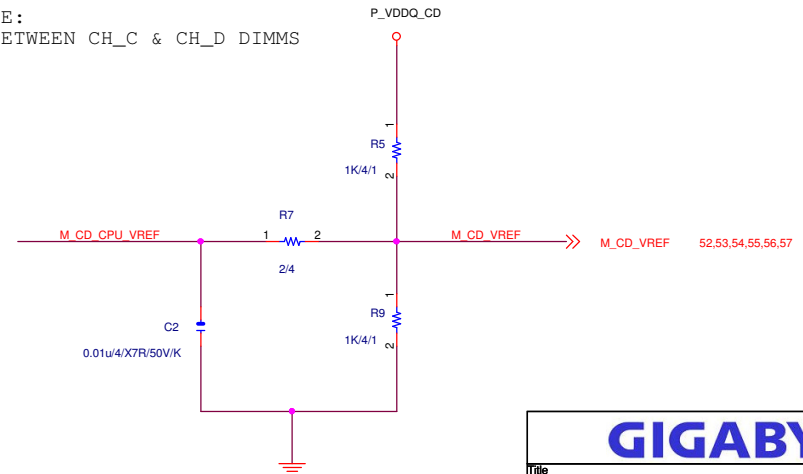
BCLK0_DP(I)
BCLK0_DN(I)

BCLK1_DP(I)
BCLK1_DN(I)

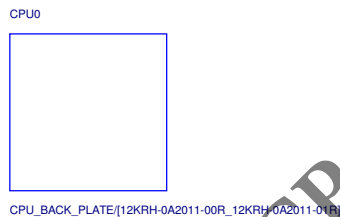
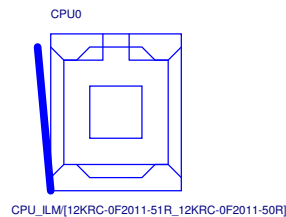
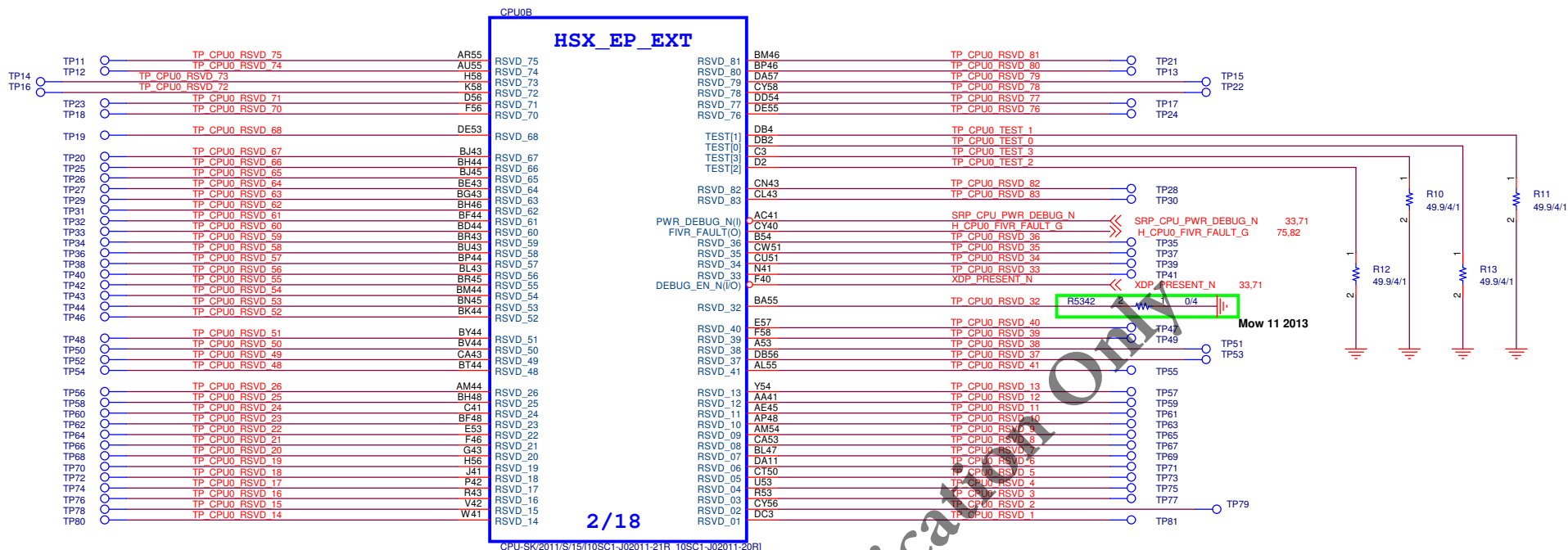
DRAM_PWR_OK_C01(I)
DRAM_PWR_OK_C23(I)
DDR_RESET_C01_N(O)
DDR_RESET_C23_N(O)
MEM_HOT_C01_N(I/O)
MEM_HOT_C23_N(I/O)



CPU-SK2011/S/15/(10SC1-J02011-21R_10SC1-J02011-20R)

[illegible]

Title			
CPU0_SOCKET(1/14)			
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Custom	MD90-FS0		1.0
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46,47,48 M_A_DQ[63:0] << >>

M_A_DQ[63:0]

46,47,48 M_A_ECC[7:0] << >>

M_A_ECC[7:0]

47 M_A_CLK_DP3
46,48 M_A_CLK_DP2
47 M_A_CLK_DP1
46 M_A_CLK_DP0
47 M_A_CLK_DN3
46,48 M_A_CLK_DN2
47 M_A_CLK_DN1
46 M_A_CLK_DN0

46,47,48 M_A_BG1
46,47,48 M_A_BG0
46,47,48 M_A_BA1
46,47,48 M_A_BA0

M_A_DQ63
M_A_DQ62
M_A_DQ61
M_A_DQ60
M_A_DQ59
M_A_DQ58
M_A_DQ57
M_A_DQ56
M_A_DQ55
M_A_DQ54
M_A_DQ53
M_A_DQ52
M_A_DQ51
M_A_DQ50
M_A_DQ49
M_A_DQ48
M_A_DQ47
M_A_DQ46
M_A_DQ45
M_A_DQ44
M_A_DQ43
M_A_DQ42
M_A_DQ41
M_A_DQ40
M_A_DQ39
M_A_DQ38
M_A_DQ37
M_A_DQ36
M_A_DQ35
M_A_DQ34
M_A_DQ33
M_A_DQ32
M_A_DQ31
M_A_DQ30
M_A_DQ29
M_A_DQ28
M_A_DQ27
M_A_DQ26
M_A_DQ25
M_A_DQ24
M_A_DQ23
M_A_DQ22
M_A_DQ21
M_A_DQ20
M_A_DQ19
M_A_DQ18
M_A_DQ17
M_A_DQ16
M_A_DQ15
M_A_DQ14
M_A_DQ13
M_A_DQ12
M_A_DQ11
M_A_DQ10
M_A_DQ9
M_A_DQ8
M_A_DQ7
M_A_DQ6
M_A_DQ5
M_A_DQ4
M_A_DQ3
M_A_DQ2
M_A_DQ1
M_A_DQ0

M_A_ECC7
M_A_ECC6
M_A_ECC5
M_A_ECC4
M_A_ECC3
M_A_ECC2
M_A_ECC1
M_A_ECC0

M_A_CLK_DP3
M_A_CLK_DP2
M_A_CLK_DP1
M_A_CLK_DP0
M_A_CLK_DN3
M_A_CLK_DN2
M_A_CLK_DN1
M_A_CLK_DN0

M_A_BG1
M_A_BG0
M_A_BA1
M_A_BA0

CK38
CM38
CK34
CM34
CL39
CL39
CJ35
CL35
CJ38
CF38
CD34
CF34
CC39
CE39
CC38
CE38
CC31
CE31
CC27
CE27
CB32
CD32
CB28
CD28
CJ31
CL31
CJ27
CL27
CH32
CK32
CH28
CK28
CL13
CM12
CD14
CC13
CH14
CM14
CG15
CE13
CJ9
CK8
CE11
CD10
CJ11
CK10
CF8
CE9
BY12
CA11
BU15
BT14
BY14
BW13
BU11
BT12
CB6
CA7
BU9
BT8
CB5
CA9
BT6
BU7
CR11
CP10
CN9
CP8
CU11
CW11
CV8
C18
CC19
CD20
CD18
CE21
CE19
CF20
CF18
CE21
CN17
CL17
CH20
CL21

CPU0C

HSX_EP_EXT

DDR0_DQ63(I/O)
DDR0_DQ62(I/O)
DDR0_DQ61(I/O)
DDR0_DQ60(I/O)
DDR0_DQ59(I/O)
DDR0_DQ58(I/O)
DDR0_DQ57(I/O)
DDR0_DQ56(I/O)
DDR0_DQ55(I/O)
DDR0_DQ54(I/O)
DDR0_DQ53(I/O)
DDR0_DQ52(I/O)
DDR0_DQ51(I/O)
DDR0_DQ50(I/O)
DDR0_DQ49(I/O)
DDR0_DQ48(I/O)
DDR0_DQ47(I/O)
DDR0_DQ46(I/O)
DDR0_DQ45(I/O)
DDR0_DQ44(I/O)
DDR0_DQ43(I/O)
DDR0_DQ42(I/O)
DDR0_DQ41(I/O)
DDR0_DQ40(I/O)
DDR0_DQ39(I/O)
DDR0_DQ38(I/O)
DDR0_DQ37(I/O)
DDR0_DQ36(I/O)
DDR0_DQ35(I/O)
DDR0_DQ34(I/O)
DDR0_DQ33(I/O)
DDR0_DQ32(I/O)
DDR0_DQ31(I/O)
DDR0_DQ30(I/O)
DDR0_DQ29(I/O)
DDR0_DQ28(I/O)
DDR0_DQ27(I/O)
DDR0_DQ26(I/O)
DDR0_DQ25(I/O)
DDR0_DQ24(I/O)
DDR0_DQ23(I/O)
DDR0_DQ22(I/O)
DDR0_DQ21(I/O)
DDR0_DQ20(I/O)
DDR0_DQ19(I/O)
DDR0_DQ18(I/O)
DDR0_DQ17(I/O)
DDR0_DQ16(I/O)
DDR0_DQ15(I/O)
DDR0_DQ14(I/O)
DDR0_DQ13(I/O)
DDR0_DQ12(I/O)
DDR0_DQ11(I/O)
DDR0_DQ10(I/O)
DDR0_DQ9(I/O)
DDR0_DQ8(I/O)
DDR0_DQ7(I/O)
DDR0_DQ6(I/O)
DDR0_DQ5(I/O)
DDR0_DQ4(I/O)
DDR0_DQ3(I/O)
DDR0_DQ2(I/O)
DDR0_DQ1(I/O)
DDR0_DQ0(I/O)
DDR0_ODT5(I/O)
DDR0_ODT4(I/O)
DDR0_ODT3(I/O)
DDR0_ODT2(I/O)
DDR0_ODT1(I/O)
DDR0_ODT0(I/O)
DDR0_CS_N9(I/O)
DDR0_CS_N8(I/O)
DDR0_CS_N7(CID4)
DDR0_CS_N6(CID3)
DDR0_CS_N5(I/O)
DDR0_CS_N4(I/O)
DDR0_CS_N3(CID1)
DDR0_CS_N2(CID0)
DDR0_CS_N1(I/O)
DDR0_CS_N0(I/O)
DDR0_C2D2(I/O)
DDR0_BG1(I/O)
DDR0_BG0(I/O)
DDR0_BA1(I/O)
DDR0_BA0(I/O)
DDR0_ACT_N(I/O)
DDR0_ALERT_N(I/O)
DDR0_PAR(I/O)
DDR0_DQS_DP17(I/O)
DDR0_DQS_DP16(I/O)
DDR0_DQS_DP15(I/O)
DDR0_DQS_DP14(I/O)
DDR0_DQS_DP13(I/O)
DDR0_DQS_DP12(I/O)
DDR0_DQS_DP11(I/O)
DDR0_DQS_DP10(I/O)
DDR0_DQS_DP9(I/O)
DDR0_DQS_DP8(I/O)
DDR0_DQS_DP7(I/O)
DDR0_DQS_DP6(I/O)
DDR0_DQS_DP5(I/O)
DDR0_DQS_DP4(I/O)
DDR0_DQS_DP3(I/O)
DDR0_DQS_DP2(I/O)
DDR0_DQS_DP1(I/O)
DDR0_DQS_DP0(I/O)
DDR0_DQS_DN17(I/O)
DDR0_DQS_DN16(I/O)
DDR0_DQS_DN15(I/O)
DDR0_DQS_DN14(I/O)
DDR0_DQS_DN13(I/O)
DDR0_DQS_DN12(I/O)
DDR0_DQS_DN11(I/O)
DDR0_DQS_DN10(I/O)
DDR0_DQS_DN9(I/O)
DDR0_DQS_DN8(I/O)
DDR0_DQS_DN7(I/O)
DDR0_DQS_DN6(I/O)
DDR0_DQS_DN5(I/O)
DDR0_DQS_DN4(I/O)
DDR0_DQS_DN3(I/O)
DDR0_DQS_DN2(I/O)
DDR0_DQS_DN1(I/O)
DDR0_DQS_DN0(I/O)
DDR0_MA17(I/O)
DDR0_MA16(I/O)
DDR0_MA15(I/O)
DDR0_MA14(I/O)
DDR0_MA13(I/O)
DDR0_MA12(I/O)
DDR0_MA11(I/O)
DDR0_MA10(I/O)
DDR0_MA9(I/O)
DDR0_MA8(I/O)
DDR0_MA7(I/O)
DDR0_MA6(I/O)
DDR0_MA5(I/O)
DDR0_MA4(I/O)
DDR0_MA3(I/O)
DDR0_MA2(I/O)
DDR0_MA1(I/O)
DDR0_MA0(I/O)
DDR0_CKE5(I/O)
DDR0_CKE4(I/O)
DDR0_CKE3(I/O)
DDR0_CKE2(I/O)
DDR0_CKE1(I/O)
DDR0_CKE0(I/O)
DDR0_ODT5(I/O)
DDR0_ODT4(I/O)
DDR0_ODT3(I/O)
DDR0_ODT2(I/O)
DDR0_ODT1(I/O)
DDR0_ODT0(I/O)
DDR0_CS_N9(I/O)
DDR0_CS_N8(I/O)
DDR0_CS_N7(CID4)
DDR0_CS_N6(CID3)
DDR0_CS_N5(I/O)
DDR0_CS_N4(I/O)
DDR0_CS_N3(CID1)
DDR0_CS_N2(CID0)
DDR0_CS_N1(I/O)
DDR0_CS_N0(I/O)
DDR0_C2D2(I/O)
DDR0_BG1(I/O)
DDR0_BG0(I/O)
DDR0_BA1(I/O)
DDR0_BA0(I/O)
DDR0_ACT_N(I/O)
DDR0_ALERT_N(I/O)
DDR0_PAR(I/O)
CU9
CM36
CF36
CE29
CL29
CG13
CG9
BU13
BV8
CV10
CJ37
CC37
CD30
CK30
CK14
CH10
BV12
BY6
CW9
CK36
CD36
CC29
CJ29
CF14
CH8
BV14
BW9
CT10
CL37
CE37
CG29
CK30
CJ13
CG11
BW11
BV6
CD24
CL23
CL25
CJ21
CE23
CR17
CP18
CP24
CK18
CJ19
CH18
CN19
CL19
CP20
CN21
CT22
CR21
CP22
CC15
CN15
CC17
CF16
CE17
CJ17
CE25
CF24
CC23
CJ23
CN25
CF22
CK26
CK24
CD26
CH26
CG22
CC25
CF26
CH22
CD22
CJ25
CK16
CD16
CK20

M_A_DQS_DP17
M_A_DQS_DP16
M_A_DQS_DP15
M_A_DQS_DP14
M_A_DQS_DP13
M_A_DQS_DP12
M_A_DQS_DP11
M_A_DQS_DP10
M_A_DQS_DP9
M_A_DQS_DP8
M_A_DQS_DP7
M_A_DQS_DP6
M_A_DQS_DP5
M_A_DQS_DP4
M_A_DQS_DP3
M_A_DQS_DP2
M_A_DQS_DP1
M_A_DQS_DP0
M_A_DQS_DN17
M_A_DQS_DN16
M_A_DQS_DN15
M_A_DQS_DN14
M_A_DQS_DN13
M_A_DQS_DN12
M_A_DQS_DN11
M_A_DQS_DN10
M_A_DQS_DN9
M_A_DQS_DN8
M_A_DQS_DN7
M_A_DQS_DN6
M_A_DQS_DN5
M_A_DQS_DN4
M_A_DQS_DN3
M_A_DQS_DN2
M_A_DQS_DN1
M_A_DQS_DN0
M_A_MA17
M_A_MA16
M_A_MA15
M_A_MA14
M_A_MA13
M_A_MA12
M_A_MA11
M_A_MA10
M_A_MA9
M_A_MA8
M_A_MA7
M_A_MA6
M_A_MA5
M_A_MA4
M_A_MA3
M_A_MA2
M_A_MA1
M_A_MA0
M_A_CKE5
M_A_CKE4
M_A_CKE3
M_A_CKE2
M_A_CKE1
M_A_CKE0
M_A_ODT5
M_A_ODT4
M_A_ODT3
M_A_ODT2
M_A_ODT1
M_A_ODT0
M_A_CS_N9
M_A_CS_N8
M_A_CS_N7
M_A_CS_N6
M_A_CS_N5
M_A_CS_N4
M_A_CS_N3
M_A_CS_N2
M_A_CS_N1
M_A_CS_N0
M_A_C2
M_A_ACT_N
M_A_ALERT_N
M_A_PAR

M_A_DQS_DP[17:0]

M_A_DQS_DP[17:0]

M_A_DQS_DN[17:0]

M_A_DQS_DN[17:0]

M_A_MA[17:0]

M_A_MA[17:0]

M_A_CKE5

48

M_A_CKE4

48

M_A_CKE3

47

M_A_CKE2

47

M_A_CKE1

46

M_A_CKE0

46

M_A_ODT5

48

M_A_ODT4

48

M_A_ODT3

47

M_A_ODT2

47

M_A_ODT1

46

M_A_ODT0

46

M_A_CS_N9

48

M_A_CS_N8

48

M_A_CS_N7

47

M_A_CS_N6

47

M_A_CS_N5

47

M_A_CS_N4

47

M_A_CS_N3

46,48

M_A_CS_N2

46,48

M_A_CS_N1

46

M_A_CS_N0

46

M_A_C2

46,47,48

M_A_ACT_N

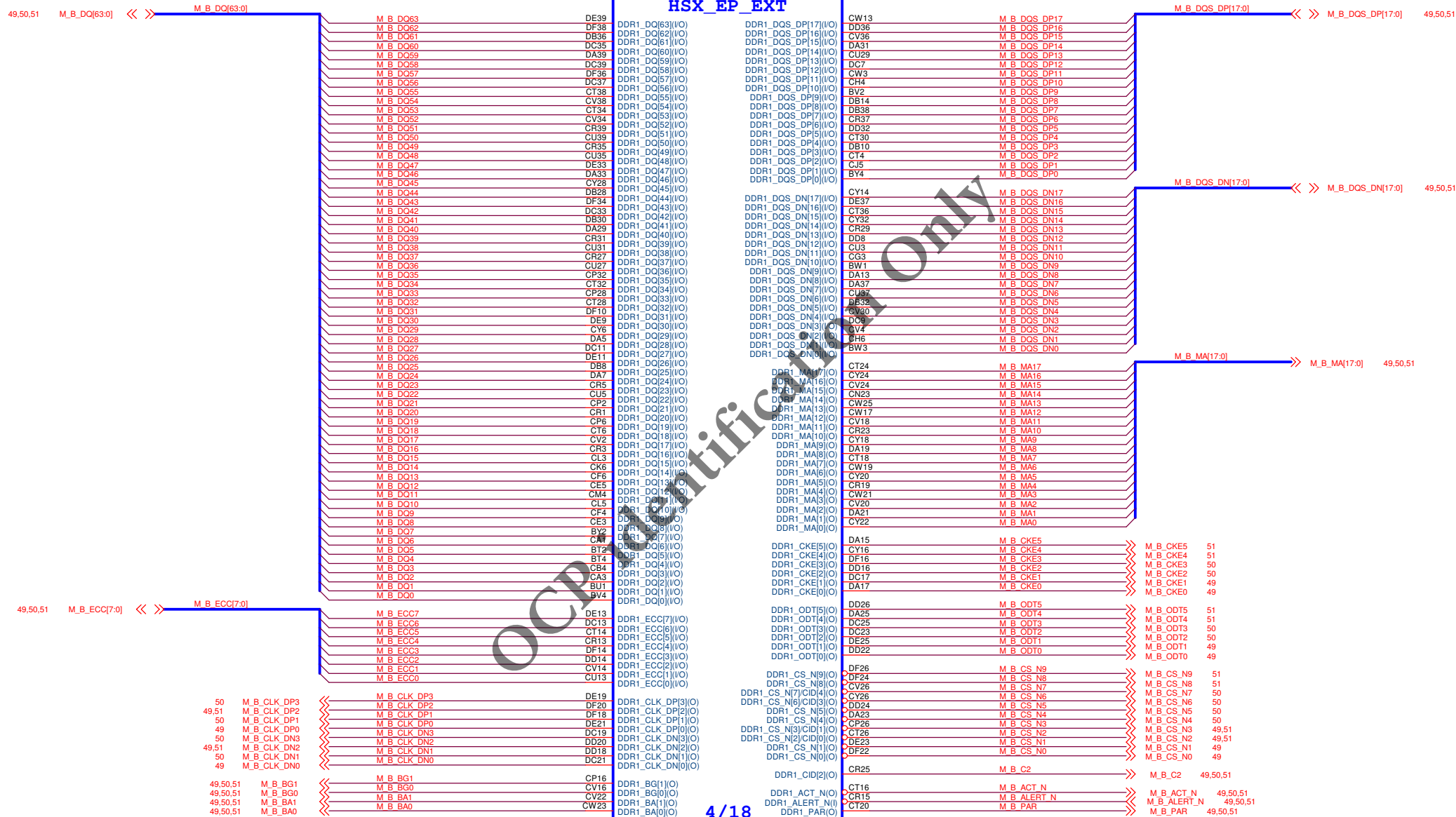
46,47,48

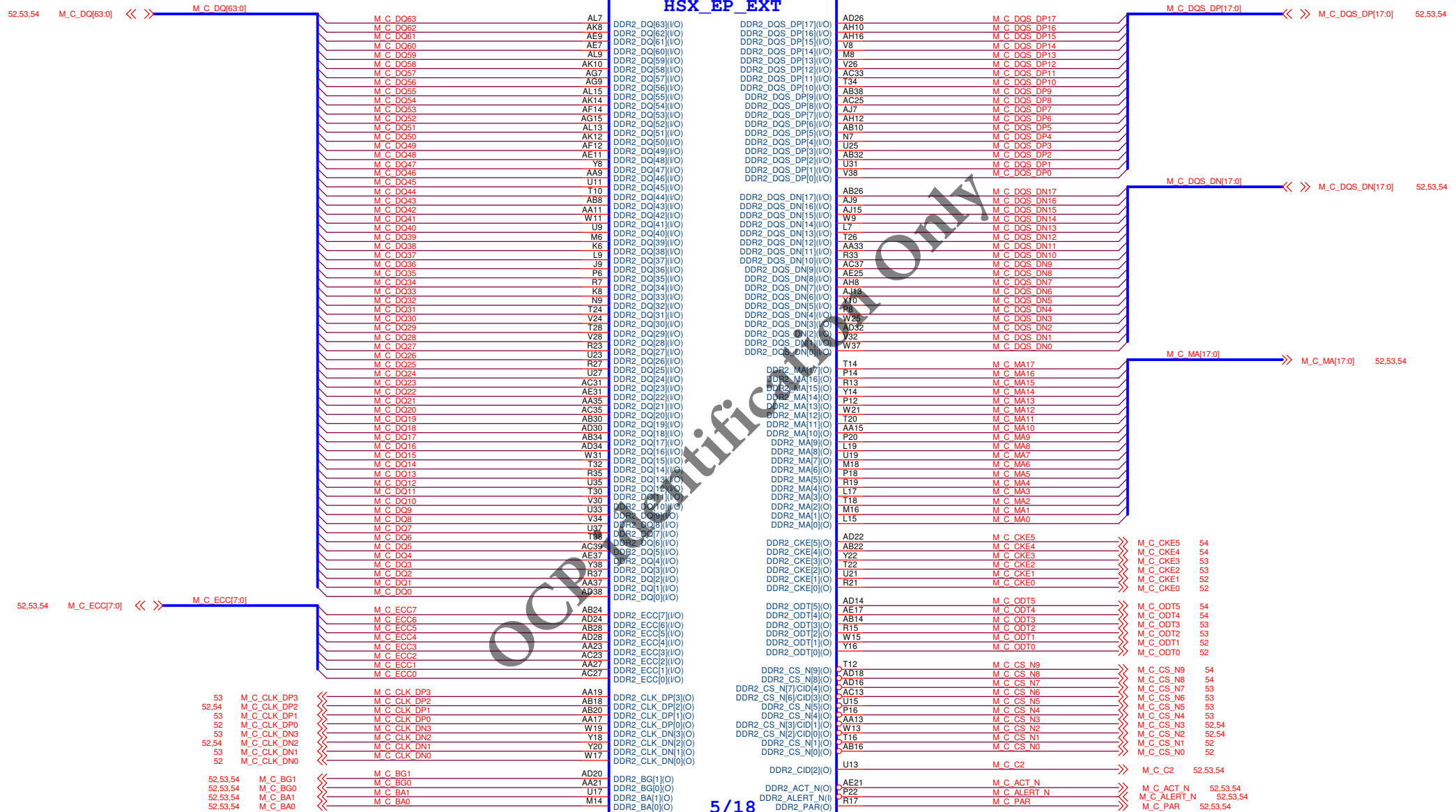
M_A_ALERT_N

46,47,48

M_A_PAR

46,47,48





90 DMI_CPU0_PCH_RX_C_DP[3:0] >> DMI_CPU0_PCH_RX_C_DP[3:0]
90 DMI_CPU0_PCH_RX_C_DN[3:0] >> DMI_CPU0_PCH_RX_C_DN[3:0]

DMI_CPU0_PCH_TX_C_DP[3:0] >> DMI_CPU0_PCH_TX_C_DP[3:0] 90
DMI_CPU0_PCH_TX_C_DN[3:0] >> DMI_CPU0_PCH_TX_C_DN[3:0] 90

Place AC CAP Close to CPU

Place AC CAP Close to CPU



142 P3E_CPU0_NIC_RX_C_DP[7:0] >> P3E_CPU0_NIC_RX_C_DP[7:0]
142 P3E_CPU0_NIC_RX_C_DN[7:0] >> P3E_CPU0_NIC_RX_C_DN[7:0]

P3E_CPU0_NIC_TX_DP[7:0] >> P3E_CPU0_NIC_TX_DP[7:0] 142
P3E_CPU0_NIC_TX_DN[7:0] >> P3E_CPU0_NIC_TX_DN[7:0] 142

CPU0H

HSX_EP_EXT

P3E_CPU0_PCIE1_1_RX_DP0	BB56	PE2D_RX_DP[15](I)	PE2D_TX_DP[15](O)	BA47	P3E_CPU0_PCIE1_1_TX_DP0
P3E_CPU0_PCIE1_1_RX_DP1	BA57	PE2D_RX_DP[14](I)	PE2D_TX_DP[14](O)	AY48	P3E_CPU0_PCIE1_1_TX_DP1
P3E_CPU0_PCIE1_1_RX_DP2	AT56	PE2D_RX_DP[13](I)	PE2D_TX_DP[13](O)	BA49	P3E_CPU0_PCIE1_1_TX_DP2
P3E_CPU0_PCIE1_1_RX_DP3	AV58	PE2D_RX_DP[12](I)	PE2D_TX_DP[12](O)	AY50	P3E_CPU0_PCIE1_1_TX_DP3
P3E_CPU0_PCIE1_1_RX_DN0	AY56	PE2D_RX_DN[15](I)	PE2D_TX_DN[15](O)	AW47	P3E_CPU0_PCIE1_1_TX_DN0
P3E_CPU0_PCIE1_1_RX_DN1	AY58	PE2D_RX_DN[14](I)	PE2D_TX_DN[14](O)	AV48	P3E_CPU0_PCIE1_1_TX_DN1
P3E_CPU0_PCIE1_1_RX_DN2	AP56	PE2D_RX_DN[13](I)	PE2D_TX_DN[13](O)	AW49	P3E_CPU0_PCIE1_1_TX_DN2
P3E_CPU0_PCIE1_1_RX_DN3	AT58	PE2D_RX_DN[12](I)	PE2D_TX_DN[12](O)	AV50	P3E_CPU0_PCIE1_1_TX_DN3
P3E_CPU0_PCIE1_1_RX_DP4	AU57	PE2C_RX_DP[11](I)	PE2C_TX_DP[11](O)	BA51	P3E_CPU0_PCIE1_1_TX_DP4
P3E_CPU0_PCIE1_1_RX_DP5	AL57	PE2C_RX_DP[10](I)	PE2C_TX_DP[10](O)	B554	P3E_CPU0_PCIE1_1_TX_DP5
P3E_CPU0_PCIE1_1_RX_DP6	AM59	PE2C_RX_DP[9](I)	PE2C_TX_DP[9](O)	BA53	P3E_CPU0_PCIE1_1_TX_DP6
P3E_CPU0_PCIE1_1_RX_DP7	AK56	PE2C_RX_DP[8](I)	PE2C_TX_DP[8](O)	AY52	P3E_CPU0_PCIE1_1_TX_DP7
P3E_CPU0_PCIE1_1_RX_DN4	AR57	PE2C_RX_DN[11](I)	PE2C_TX_DN[11](O)	AW51	P3E_CPU0_PCIE1_1_TX_DN4
P3E_CPU0_PCIE1_1_RX_DN5	AJ57	PE2C_RX_DN[10](I)	PE2C_TX_DN[10](O)	AY54	P3E_CPU0_PCIE1_1_TX_DN5
P3E_CPU0_PCIE1_1_RX_DN6	AK58	PE2C_RX_DN[9](I)	PE2C_TX_DN[9](O)	AW53	P3E_CPU0_PCIE1_1_TX_DN6
P3E_CPU0_PCIE1_1_RX_DN7	AH56	PE2C_RX_DN[8](I)	PE2C_TX_DN[8](O)	AV52	P3E_CPU0_PCIE1_1_TX_DN7
P3E_CPU0_PCIE1_1_RX_DP8	AF58	PE2B_RX_DP[7](I)	PE2B_TX_DP[7](O)	AT54	P3E_CPU0_PCIE1_1_TX_DP8
P3E_CPU0_PCIE1_1_RX_DP9	AE55	PE2B_RX_DP[6](I)	PE2B_TX_DP[6](O)	AR53	P3E_CPU0_PCIE1_1_TX_DP9
P3E_CPU0_PCIE1_1_RX_DP10	AD56	PE2B_RX_DP[5](I)	PE2B_TX_DP[5](O)	AK94	P3E_CPU0_PCIE1_1_TX_DP10
P3E_CPU0_PCIE1_1_RX_DP11	AD54	PE2B_RX_DP[4](I)	PE2B_TX_DP[4](O)	AK53	P3E_CPU0_PCIE1_1_TX_DP11
P3E_CPU0_PCIE1_1_RX_DN8	AE57	PE2B_RX_DN[7](I)	PE2B_TX_DN[7](O)	AP54	P3E_CPU0_PCIE1_1_TX_DN8
P3E_CPU0_PCIE1_1_RX_DN9	AC55	PE2B_RX_DN[6](I)	PE2B_TX_DN[6](O)	AM53	P3E_CPU0_PCIE1_1_TX_DN9
P3E_CPU0_PCIE1_1_RX_DN10	AB56	PE2B_RX_DN[5](I)	PE2B_TX_DN[5](O)	AF54	P3E_CPU0_PCIE1_1_TX_DN10
P3E_CPU0_PCIE1_1_RX_DN11	AB54	PE2B_RX_DN[4](I)	PE2B_TX_DN[4](O)	AG53	P3E_CPU0_PCIE1_1_TX_DN11
P3E_CPU0_PCIE1_1_RX_DP12	W55	PE2A_RX_DP[3](I)	PE2A_TX_DP[3](O)	AP52	P3E_CPU0_PCIE1_1_TX_DP12
P3E_CPU0_PCIE1_1_RX_DP13	V56	PE2A_RX_DP[2](I)	PE2A_TX_DP[2](O)	AR51	P3E_CPU0_PCIE1_1_TX_DP13
P3E_CPU0_PCIE1_1_RX_DP14	V54	PE2A_RX_DP[1](I)	PE2A_TX_DP[1](O)	AP50	P3E_CPU0_PCIE1_1_TX_DP14
P3E_CPU0_PCIE1_1_RX_DP15	N55	PE2A_RX_DP[0](I)	PE2A_TX_DP[0](O)	AR49	P3E_CPU0_PCIE1_1_TX_DP15
P3E_CPU0_PCIE1_1_RX_DN12	U55	PE2A_RX_DN[3](I)	PE2A_TX_DN[3](O)	AM52	P3E_CPU0_PCIE1_1_TX_DN12
P3E_CPU0_PCIE1_1_RX_DN13	T56	PE2A_RX_DN[2](I)	PE2A_TX_DN[2](O)	AN51	P3E_CPU0_PCIE1_1_TX_DN13
P3E_CPU0_PCIE1_1_RX_DN14	T54	PE2A_RX_DN[1](I)	PE2A_TX_DN[1](O)	AM50	P3E_CPU0_PCIE1_1_TX_DN14
P3E_CPU0_PCIE1_1_RX_DN15	L55	PE2A_RX_DN[0](I)	PE2A_TX_DN[0](O)	AN49	P3E_CPU0_PCIE1_1_TX_DN15

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CPU-SK2011/S15/10SG1J02011-21R_10SG1J02011-20R

PCIEx16 SLOT1

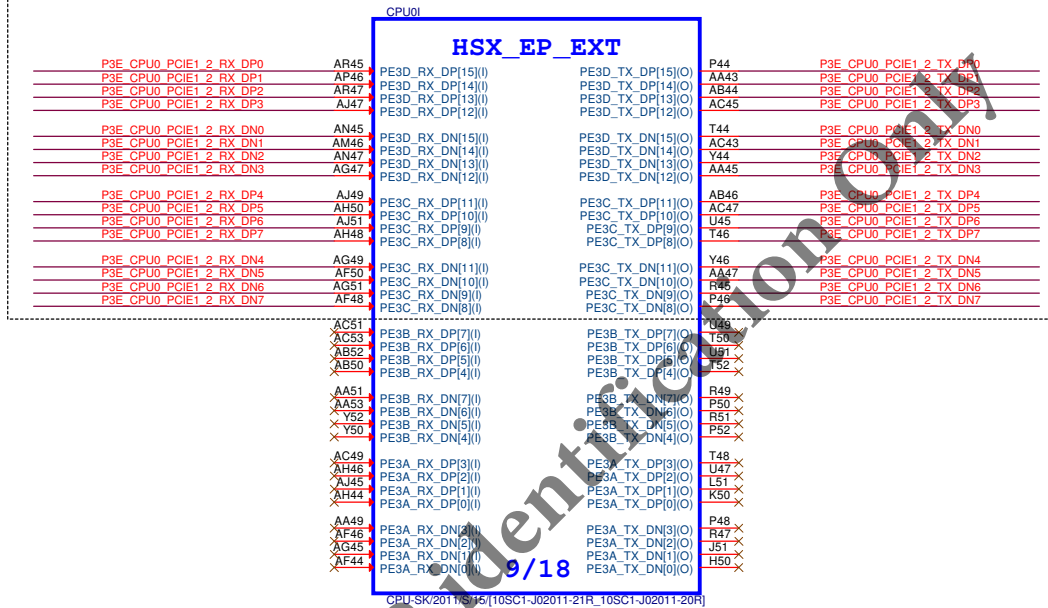
84 P3E_CPU0_PCIE1_1_RX_DP[15:0] >> P3E_CPU0_PCIE1_1_RX_DP[15:0]
84 P3E_CPU0_PCIE1_1_RX_DN[15:0] >> P3E_CPU0_PCIE1_1_RX_DN[15:0]

P3E_CPU0_PCIE1_1_TX_DP[15:0] >> P3E_CPU0_PCIE1_1_TX_DP[15:0] 84
P3E_CPU0_PCIE1_1_TX_DN[15:0] >> P3E_CPU0_PCIE1_1_TX_DN[15:0] 84

GIGABYTE™

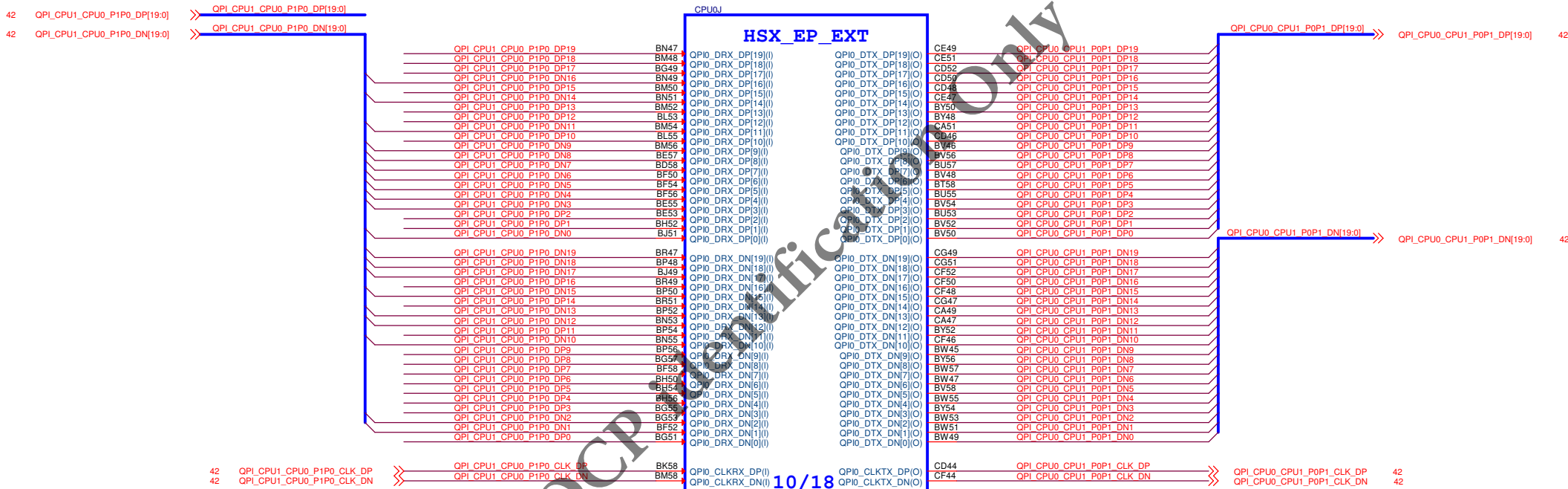
Title			CPU0_PE2 (8/14)
Size	Document Number	Rev	
Custom	MD90-FS0	1.0	
Date:	Tuesday, June 09, 2015	Sheet	25 of 231

0325 Swap Net



PCIEx8 SLOT1

84	P3E_CPU0_PCIE1_2_RX_DP[7:0]	>>	P3E_CPU0_PCIE1_2_RX_DP[7:0]		P3E_CPU0_PCIE1_2_TX_DP[7:0]	>>	P3E_CPU0_PCIE1_2_TX_DP[7:0]	84
84	P3E_CPU0_PCIE1_2_RX_DN[7:0]	>>	P3E_CPU0_PCIE1_2_RX_DN[7:0]		P3E_CPU0_PCIE1_2_TX_DN[7:0]	>>	P3E_CPU0_PCIE1_2_TX_DN[7:0]	84



41 QPI_CPU1_CPU0_P0P1_DP[19:0] >> QPI_CPU1_CPU0_P0P1_DP[19:0]
41 QPI_CPU1_CPU0_P0P1_DN[19:0] >> QPI_CPU1_CPU0_P0P1_DN[19:0]

DESIGN NOTE:
POLARITY INVERSION DONE ON THESE
PAIRS TO REDUCE CROSSTALK

41 QPI_CPU1_CPU0_P0P1_CLK_DP
41 QPI_CPU1_CPU0_P0P1_CLK_DN

QPI_CPU1_CPU0_P0P1_DN19
QPI_CPU1_CPU0_P0P1_DN18
QPI_CPU1_CPU0_P0P1_DN17
QPI_CPU1_CPU0_P0P1_DN16
QPI_CPU1_CPU0_P0P1_DP15
QPI_CPU1_CPU0_P0P1_DP14
QPI_CPU1_CPU0_P0P1_DP13
QPI_CPU1_CPU0_P0P1_DP12
QPI_CPU1_CPU0_P0P1_DP11
QPI_CPU1_CPU0_P0P1_DN10
QPI_CPU1_CPU0_P0P1_DP9
QPI_CPU1_CPU0_P0P1_DP8
QPI_CPU1_CPU0_P0P1_DP7
QPI_CPU1_CPU0_P0P1_DP6
QPI_CPU1_CPU0_P0P1_DP5
QPI_CPU1_CPU0_P0P1_DP4
QPI_CPU1_CPU0_P0P1_DP3
QPI_CPU1_CPU0_P0P1_DN2
QPI_CPU1_CPU0_P0P1_DN1
QPI_CPU1_CPU0_P0P1_DN0

QPI_CPU1_CPU0_P0P1_DP19
QPI_CPU1_CPU0_P0P1_DP18
QPI_CPU1_CPU0_P0P1_DP17
QPI_CPU1_CPU0_P0P1_DP16
QPI_CPU1_CPU0_P0P1_DN15
QPI_CPU1_CPU0_P0P1_DN14
QPI_CPU1_CPU0_P0P1_DN13
QPI_CPU1_CPU0_P0P1_DN12
QPI_CPU1_CPU0_P0P1_DN11
QPI_CPU1_CPU0_P0P1_DP10
QPI_CPU1_CPU0_P0P1_DN9
QPI_CPU1_CPU0_P0P1_DN8
QPI_CPU1_CPU0_P0P1_DN7
QPI_CPU1_CPU0_P0P1_DN6
QPI_CPU1_CPU0_P0P1_DN5
QPI_CPU1_CPU0_P0P1_DN4
QPI_CPU1_CPU0_P0P1_DN3
QPI_CPU1_CPU0_P0P1_DP2
QPI_CPU1_CPU0_P0P1_DP1
QPI_CPU1_CPU0_P0P1_DP0



QPI1_DRX_DP[19:0]
QPI1_DRX_DP[18:0]
QPI1_DRX_DP[17:0]
QPI1_DRX_DP[16:0]
QPI1_DRX_DP[15:0]
QPI1_DRX_DP[14:0]
QPI1_DRX_DP[13:0]
QPI1_DRX_DP[12:0]
QPI1_DRX_DP[11:0]
QPI1_DRX_DP[10:0]
QPI1_DRX_DP[9:0]
QPI1_DRX_DP[8:0]
QPI1_DRX_DP[7:0]
QPI1_DRX_DP[6:0]
QPI1_DRX_DP[5:0]
QPI1_DRX_DP[4:0]
QPI1_DRX_DP[3:0]
QPI1_DRX_DP[2:0]
QPI1_DRX_DP[1:0]
QPI1_DRX_DP[0:0]

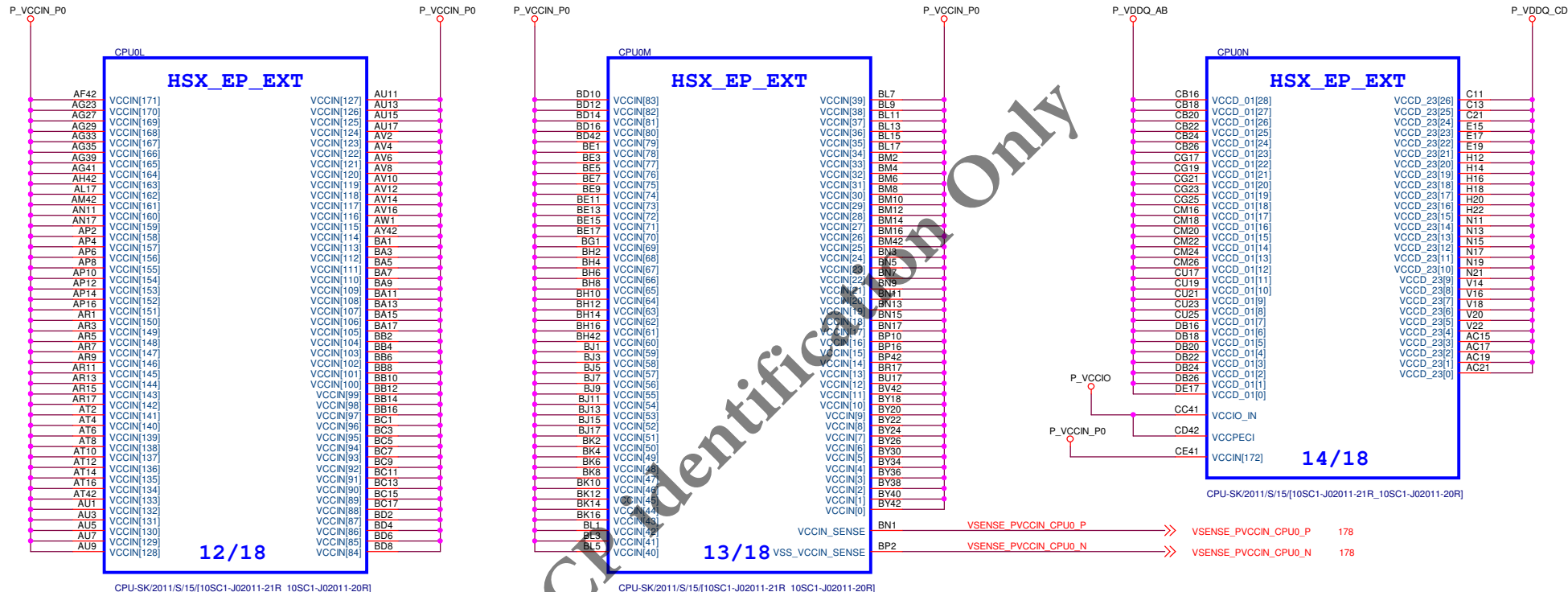
QPI1_DRX_DN[19:0]
QPI1_DRX_DN[18:0]
QPI1_DRX_DN[17:0]
QPI1_DRX_DN[16:0]
QPI1_DRX_DN[15:0]
QPI1_DRX_DN[14:0]
QPI1_DRX_DN[13:0]
QPI1_DRX_DN[12:0]
QPI1_DRX_DN[11:0]
QPI1_DRX_DN[10:0]
QPI1_DRX_DN[9:0]
QPI1_DRX_DN[8:0]
QPI1_DRX_DN[7:0]
QPI1_DRX_DN[6:0]
QPI1_DRX_DN[5:0]
QPI1_DRX_DN[4:0]
QPI1_DRX_DN[3:0]
QPI1_DRX_DN[2:0]
QPI1_DRX_DN[1:0]
QPI1_DRX_DN[0:0]

QPI1_CLKRX_DP(I)
QPI1_CLKRX_DN(I)

QPI_CPU0_CPU1_P1P0_DP[19:0] >> QPI_CPU0_CPU1_P1P0_DP[19:0] 41
QPI_CPU0_CPU1_P1P0_DP19
QPI_CPU0_CPU1_P1P0_DP18
QPI_CPU0_CPU1_P1P0_DP17
QPI_CPU0_CPU1_P1P0_DP16
QPI_CPU0_CPU1_P1P0_DP15
QPI_CPU0_CPU1_P1P0_DP14
QPI_CPU0_CPU1_P1P0_DP13
QPI_CPU0_CPU1_P1P0_DP12
QPI_CPU0_CPU1_P1P0_DP11
QPI_CPU0_CPU1_P1P0_DP10
QPI_CPU0_CPU1_P1P0_DP9
QPI_CPU0_CPU1_P1P0_DP8
QPI_CPU0_CPU1_P1P0_DP7
QPI_CPU0_CPU1_P1P0_DP6
QPI_CPU0_CPU1_P1P0_DP5
QPI_CPU0_CPU1_P1P0_DP4
QPI_CPU0_CPU1_P1P0_DP3
QPI_CPU0_CPU1_P1P0_DP2
QPI_CPU0_CPU1_P1P0_DP1
QPI_CPU0_CPU1_P1P0_DP0

QPI_CPU0_CPU1_P1P0_DN[19:0] >> QPI_CPU0_CPU1_P1P0_DN[19:0] 41
QPI_CPU0_CPU1_P1P0_DN19
QPI_CPU0_CPU1_P1P0_DN18
QPI_CPU0_CPU1_P1P0_DN17
QPI_CPU0_CPU1_P1P0_DN16
QPI_CPU0_CPU1_P1P0_DN15
QPI_CPU0_CPU1_P1P0_DN14
QPI_CPU0_CPU1_P1P0_DN13
QPI_CPU0_CPU1_P1P0_DN12
QPI_CPU0_CPU1_P1P0_DN11
QPI_CPU0_CPU1_P1P0_DN10
QPI_CPU0_CPU1_P1P0_DN9
QPI_CPU0_CPU1_P1P0_DN8
QPI_CPU0_CPU1_P1P0_DN7
QPI_CPU0_CPU1_P1P0_DN6
QPI_CPU0_CPU1_P1P0_DN5
QPI_CPU0_CPU1_P1P0_DN4
QPI_CPU0_CPU1_P1P0_DN3
QPI_CPU0_CPU1_P1P0_DN2
QPI_CPU0_CPU1_P1P0_DN1
QPI_CPU0_CPU1_P1P0_DN0

QPI_CPU0_CPU1_P1P0_CLK_DP >> QPI_CPU0_CPU1_P1P0_CLK_DP 41
QPI_CPU0_CPU1_P1P0_CLK_DN >> QPI_CPU0_CPU1_P1P0_CLK_DN 41



CPU0G

HSX_EP_EXT

A23	VSS[630]	M2	VSS[551]
A37	VSS[629]	M36	VSS[550]
A39	VSS[628]	M42	VSS[549]
A41	VSS[627]	M44	VSS[548]
A43	VSS[626]	M48	VSS[547]
A45	VSS[625]	M50	VSS[546]
A47	VSS[624]	M52	VSS[545]
A49	VSS[623]	N23	VSS[544]
A5	VSS[622]	N27	VSS[543]
A51	VSS[621]	N29	VSS[542]
A7	VSS[620]	N33	VSS[541]
B10	VSS[619]	N35	VSS[540]
B36	VSS[618]	N37	VSS[539]
B40	VSS[617]	N39	VSS[538]
B52	VSS[616]	N43	VSS[537]
B6	VSS[615]	N45	VSS[536]
C33	VSS[614]	N47	VSS[535]
C5	VSS[613]	N49	VSS[534]
C55	VSS[612]	N5	VSS[533]
D10	VSS[611]	N51	VSS[532]
D24	VSS[610]	N53	VSS[531]
D36	VSS[609]	P10	VSS[530]
D4	VSS[608]	P24	VSS[529]
D40	VSS[607]	P26	VSS[528]
E1	VSS[606]	P28	VSS[527]
E3	VSS[605]	P30	VSS[526]
E39	VSS[604]	P32	VSS[525]
E41	VSS[603]	P34	VSS[524]
F2	VSS[602]	P38	VSS[523]
F30	VSS[601]	P40	VSS[522]
F32	VSS[600]	P54	VSS[521]
F36	VSS[599]	P56	VSS[520]
F4	VSS[598]	R11	VSS[519]
F42	VSS[597]	R25	VSS[518]
F44	VSS[596]	R29	VSS[517]
F48	VSS[595]	R31	VSS[516]
F50	VSS[594]	R39	VSS[515]
G1	VSS[593]	R5	VSS[514]
G23	VSS[592]	R55	VSS[513]
G27	VSS[591]	R8	VSS[512]
G33	VSS[590]	T36	VSS[511]
G35	VSS[589]	T4	VSS[510]
G39	VSS[588]	T42	VSS[509]
G41	VSS[587]	T6	VSS[508]
G45	VSS[586]	T8	VSS[507]
G47	VSS[585]	U29	VSS[506]
G49	VSS[584]	U3	VSS[505]
G5	VSS[583]	U39	VSS[504]
G51	VSS[582]	U41	VSS[503]
G53	VSS[581]	U43	VSS[502]
G57	VSS[580]	U7	VSS[501]
G9	VSS[579]	V10	VSS[500]
H24	VSS[578]	V12	VSS[499]
H26	VSS[577]	V36	VSS[498]
H28	VSS[576]	V44	VSS[497]
H30	VSS[575]	V46	VSS[496]
H32	VSS[574]	V48	VSS[495]
H34	VSS[573]	V50	VSS[494]
H36	VSS[572]	V52	VSS[493]
H40	VSS[571]	W23	VSS[492]
H54	VSS[570]	W27	VSS[491]
H6	VSS[569]	W33	VSS[490]
H8	VSS[568]	W35	VSS[489]
J25	VSS[567]	W39	VSS[488]
J29	VSS[566]	W43	VSS[487]
J3	VSS[565]	W45	VSS[486]
J31	VSS[564]	W47	VSS[485]
J37	VSS[563]	W49	VSS[484]
J5	VSS[562]	W51	VSS[483]
J55	VSS[561]	W53	VSS[482]
J7	VSS[560]	W7	VSS[481]
K10	VSS[559]	Y24	VSS[480]
K36	VSS[558]	Y26	VSS[479]
K40	VSS[557]	Y28	VSS[478]
L29	VSS[556]	Y30	VSS[477]
L39	VSS[555]	Y32	VSS[476]
L41	VSS[554]	Y34	VSS[475]
L5	VSS[553]		
M10	VSS[552]		

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CPU-SK/2011/S/15(10SC1-J02011-21R_10SC1-J02011-20R)

CPU0P

HSX_EP_EXT

Y36	VSS[472]	VSS[393]	AH6
Y4	VSS[471]	VSS[392]	AH14
Y42	VSS[469]	VSS[391]	AH58
Y56	VSS[468]	VSS[390]	AJ11
AA3	VSS[467]	VSS[389]	AJ17
AA5	VSS[466]	VSS[388]	AK4
AA29	VSS[465]	VSS[387]	AK6
AA7	VSS[464]	VSS[386]	AK16
AA31	VSS[463]	VSS[385]	AK42
AA39	VSS[462]	VSS[384]	AK44
AA55	VSS[461]	VSS[383]	AK46
AB12	VSS[460]	VSS[382]	AK48
AB2	VSS[459]	VSS[381]	AK50
AB40	VSS[458]	VSS[380]	AK52
AB42	VSS[457]	VSS[379]	AL11
AC7	VSS[456]	VSS[378]	AL43
AC11	VSS[455]	VSS[377]	AL45
AC29	VSS[454]	VSS[376]	AL47
AD4	VSS[453]	VSS[375]	AL49
AD8	VSS[452]	VSS[374]	AL51
AD6	VSS[451]	VSS[373]	AL53
AD10	VSS[450]	VSS[372]	AM2
AD12	VSS[449]	VSS[371]	AM4
AD36	VSS[448]	VSS[370]	AM6
AD49	VSS[447]	VSS[369]	AM8
AD42	VSS[446]	VSS[368]	AM10
AD44	VSS[445]	VSS[367]	AM12
AD46	VSS[444]	VSS[366]	AM14
AD48	VSS[443]	VSS[365]	AM16
AD50	VSS[442]	VSS[364]	AM56
AD52	VSS[441]	VSS[363]	AN1
AE13	VSS[440]	VSS[362]	AN3
AE15	VSS[439]	VSS[361]	AN5
AE19	VSS[438]	VSS[360]	AN7
AE23	VSS[437]	VSS[359]	AN9
AE27	VSS[436]	VSS[358]	AN13
AE29	VSS[435]	VSS[357]	AN15
AE33	VSS[434]	VSS[356]	AN55
AE35	VSS[433]	VSS[355]	AN57
AE39	VSS[432]	VSS[354]	AP42
AE41	VSS[431]	VSS[353]	AP44
AE43	VSS[430]	VSS[352]	AP58
AE47	VSS[429]	VSS[351]	AT44
AE49	VSS[428]	VSS[350]	AT46
AF10	VSS[427]	VSS[349]	AT48
AF16	VSS[426]	VSS[348]	AT50
AF18	VSS[425]	VSS[347]	AT52
AE51	VSS[424]	VSS[346]	AU45
AE53	VSS[423]	VSS[345]	AU47
AF2	VSS[422]	VSS[344]	AU49
AF4	VSS[421]	VSS[343]	AU51
AF6	VSS[420]	VSS[342]	AU53
AF8	VSS[419]	VSS[341]	AV22
AF20	VSS[418]	VSS[340]	AV54
AF22	VSS[417]	VSS[339]	AV56
AF24	VSS[416]	VSS[338]	AW11
AF26	VSS[415]	VSS[337]	AW13
AF28	VSS[414]	VSS[336]	AW15
AF30	VSS[413]	VSS[335]	AW17
AF32	VSS[412]	VSS[334]	AW3
AF34	VSS[411]	VSS[333]	AW5
AF36	VSS[410]	VSS[332]	AW7
AF38	VSS[409]	VSS[331]	AW9
AF40	VSS[408]	VSS[330]	AW55
AF54	VSS[407]	VSS[329]	AW57
AF56	VSS[406]	VSS[328]	AY2
AG11	VSS[405]	VSS[327]	AY4
AG13	VSS[404]	VSS[326]	AY6
AG17	VSS[403]	VSS[325]	AY8
AG19	VSS[402]	VSS[324]	AY10
AG21	VSS[401]	VSS[323]	AY12
AG25	VSS[400]	VSS[322]	AY14
AG31	VSS[399]	VSS[321]	AY16
AG37	VSS[398]	VSS[320]	AY44
AG43	VSS[397]	VSS[319]	BB42
AG55	VSS[396]	VSS[318]	BB46
AG57	VSS[395]	VSS[317]	BB50
AH2	VSS[394]	VSS[316]	BB58
		VSS[315]	BC45

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CPU-SK/2011/S/15(10SC1-J02011-21R_10SC1-J02011-20R)

GIGABYTE™

Title			CPU0_GND (13/14)
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Custom	MD90-FS0		
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CPU00

HSX_EP_EXT

BC47	VSS[314]	VSS[235]	BW15
BC49	VSS[313]	VSS[234]	BW17
BC51	VSS[312]	VSS[233]	BW43
BC53	VSS[311]	VSS[232]	BY8
BC55	VSS[310]	VSS[231]	BY10
BC57	VSS[309]	VSS[230]	BY28
BD52	VSS[308]	VSS[229]	BY32
BD54	VSS[307]	VSS[228]	BY56
BD56	VSS[306]	VSS[227]	CA5
BE49	VSS[305]	VSS[226]	CA13
BE51	VSS[304]	VSS[225]	CA15
BF2	VSS[303]	VSS[224]	CA17
BF4	VSS[302]	VSS[223]	CA19
BF10	VSS[301]	VSS[222]	CA21
BF12	VSS[300]	VSS[221]	CA23
BF14	VSS[299]	VSS[220]	CA25
BF16	VSS[298]	VSS[219]	CA27
BF8	VSS[297]	VSS[218]	CA29
BF9	VSS[296]	VSS[217]	CA31
BF42	VSS[295]	VSS[216]	CA33
BG3	VSS[294]	VSS[215]	CA35
BG5	VSS[293]	VSS[214]	CA37
BG7	VSS[292]	VSS[213]	CA39
BG9	VSS[291]	VSS[212]	CA41
BG11	VSS[290]	VSS[211]	CA43
BG13	VSS[289]	VSS[210]	CA45
BG15	VSS[288]	VSS[209]	CA47
BG17	VSS[287]	VSS[208]	CB2
BG45	VSS[286]	VSS[207]	CB10
BG47	VSS[285]	VSS[206]	CB12
BH58	VSS[284]	VSS[205]	CB14
BJ55	VSS[283]	VSS[204]	CB17
BJ57	VSS[282]	VSS[203]	CB34
BK42	VSS[281]	VSS[202]	CB36
BK48	VSS[280]	VSS[201]	CB38
BK49	VSS[279]	VSS[200]	CB40
BK50	VSS[278]	VSS[199]	CB42
BK52	VSS[277]	VSS[198]	CB44
BK54	VSS[276]	VSS[197]	CB46
BL45	VSS[275]	VSS[196]	CB48
BL49	VSS[274]	VSS[195]	CB50
BL57	VSS[273]	VSS[194]	CB52
BN43	VSS[272]	VSS[193]	CB54
BN57	VSS[271]	VSS[192]	CB56
BP4	VSS[270]	VSS[191]	CC3
BP6	VSS[269]	VSS[190]	CC5
BP12	VSS[268]	VSS[189]	CC7
BP14	VSS[267]	VSS[188]	CC9
BP58	VSS[266]	VSS[187]	CC11
BR1	VSS[265]	VSS[186]	CC33
BR3	VSS[264]	VSS[185]	CC43
BR5	VSS[263]	VSS[184]	CC45
BR7	VSS[262]	VSS[183]	CC47
BR9	VSS[261]	VSS[182]	CC49
BR11	VSS[260]	VSS[181]	CD12
BR13	VSS[259]	VSS[180]	CD4
BR15	VSS[258]	VSS[179]	CD6
BR53	VSS[257]	VSS[178]	CD8
BR55	VSS[256]	VSS[177]	CD40
BR57	VSS[255]	VSS[176]	CE7
BT10	VSS[254]	VSS[175]	CE15
BT16	VSS[253]	VSS[174]	CE43
BT42	VSS[252]	VSS[173]	CE45
BT46	VSS[251]	VSS[172]	CE47
BT48	VSS[250]	VSS[171]	CE12
BT50	VSS[249]	VSS[170]	CF28
BT52	VSS[248]	VSS[169]	CF32
BT54	VSS[247]	VSS[168]	CF27
BT56	VSS[246]	VSS[167]	CG5
BU3	VSS[245]	VSS[166]	CG27
BU5	VSS[244]	VSS[165]	CG7
BU45	VSS[243]	VSS[164]	CG29
BU47	VSS[242]	VSS[163]	CG31
BV10	VSS[241]	VSS[162]	CG33
BV16	VSS[240]	VSS[161]	CG35
BW5	VSS[239]	VSS[160]	CG37
BW7	VSS[238]	VSS[159]	CG39
	VSS[237]	VSS[158]	CT2
	VSS[236]	VSS[157]	CT43
			CG45
			CG53
			CG55

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CPU-SK2011/S15[10SC1-J02011-21R_10SC1-J02011-20R]

CPU0R

HSX_EP_EXT

CH12	VSS[156]	CU1
CH30	VSS[155]	CU7
CH34	VSS[154]	CU15
CH36	VSS[153]	CU33
CH38	VSS[152]	CU6
CH40	VSS[151]	CV12
CH42	VSS[150]	CV28
CH44	VSS[149]	CV32
CH46	VSS[148]	CV40
CH48	VSS[147]	CV54
CH50	VSS[146]	CV58
CH52	VSS[145]	CW1
CH54	VSS[144]	CW5
CH56	VSS[143]	CW15
CJ3	VSS[142]	CW27
CJ7	VSS[141]	CW29
CJ15	VSS[140]	CW31
CJ33	VSS[139]	CW33
CJ41	VSS[138]	CW35
CJ43	VSS[137]	CW37
CJ45	VSS[136]	CW39
CJ47	VSS[135]	CW53
CJ49	VSS[134]	CW55
CJ57	VSS[133]	CW57
CK1	VSS[132]	CY2
CK12	VSS[131]	CY4
CK40	VSS[130]	CY8
CK52	VSS[129]	CY10
CK54	VSS[128]	CY12
CL7	VSS[127]	CY30
CL9	VSS[126]	CY34
CL11	VSS[125]	CY36
CL15	VSS[124]	CY42
CM6	VSS[123]	CY44
CM8	VSS[122]	CY46
CM10	VSS[121]	CY48
CM28	VSS[120]	CY50
CM32	VSS[119]	CY52
CM40	VSS[118]	CY54
CM52	VSS[117]	DA3
CM54	VSS[116]	DA9
CN3	VSS[115]	DA27
CN5	VSS[114]	DA35
CN7	VSS[113]	DA41
CN11	VSS[112]	DA43
CN13	VSS[111]	DA45
CN27	VSS[110]	DA47
CN29	VSS[109]	DA49
CN31	VSS[108]	DA51
CN33	VSS[107]	DA53
CN35	VSS[106]	DA55
CN37	VSS[105]	DB6
CN39	VSS[104]	DB12
CN53	VSS[103]	DB34
CN55	VSS[102]	DB40
CN57	VSS[101]	DB58
CP4	VSS[99]	DC5
CP12	VSS[98]	DC53
CP14	VSS[97]	DC55
CP30	VSS[96]	DD6
CP34	VSS[95]	DD10
CP36	VSS[94]	DD12
CP38	VSS[93]	DD34
CP42	VSS[92]	DD38
CP44	VSS[91]	DD40
CP46	VSS[90]	DE7
CP48	VSS[89]	DE15
CP50	VSS[88]	DE35
CP56	VSS[87]	DF8
CP7	VSS[86]	DF12
CR9	VSS[85]	DF40
CR33	VSS[84]	DF42
CR41	VSS[83]	DF44
CR45	VSS[82]	DF46
CR47	VSS[81]	DF48
CR49	VSS[80]	DF50
CT12	VSS[79]	DF52
CT40	VSS[78]	

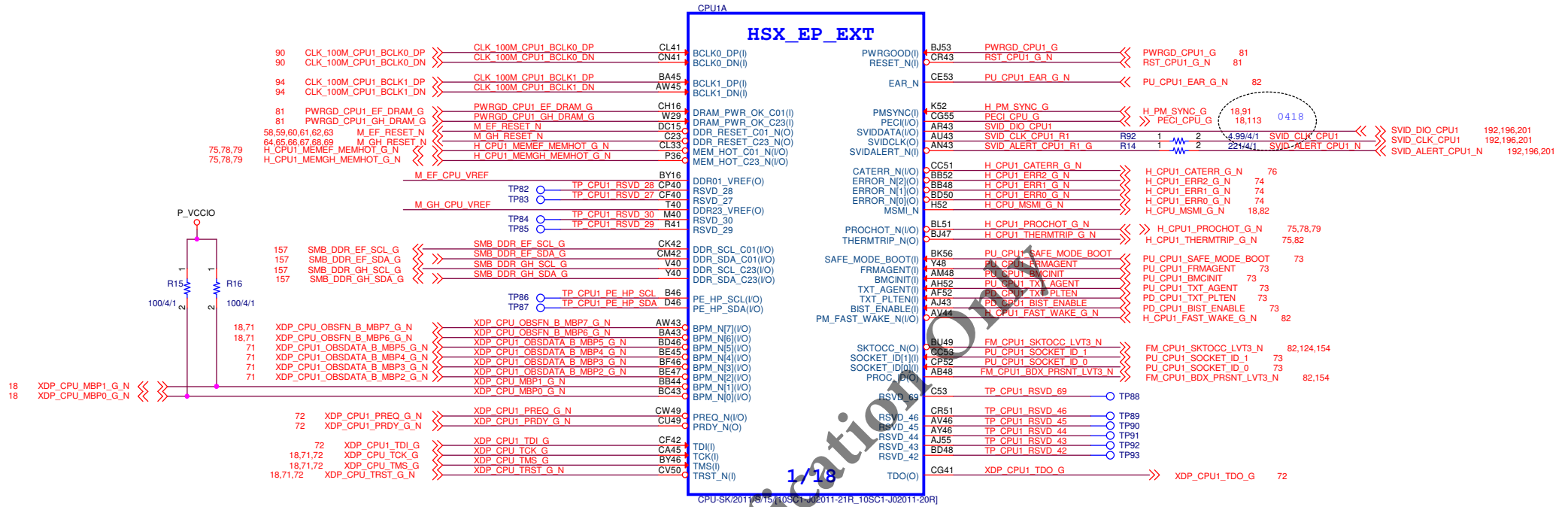
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CPU-SK2011/S15[10SC1-J02011-21R_10SC1-J02011-20R]

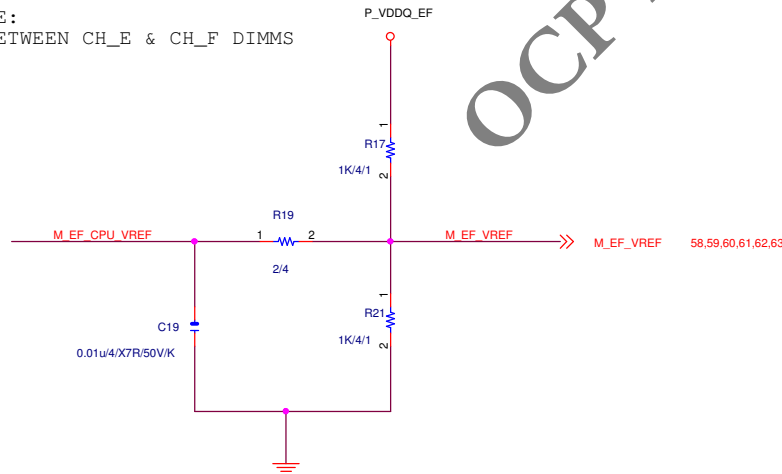
GIGABYTE™

Title				CPU0_GND (14/14)	
Size	Document Number	Rev		1.0	
Custom	MD90-FS0				
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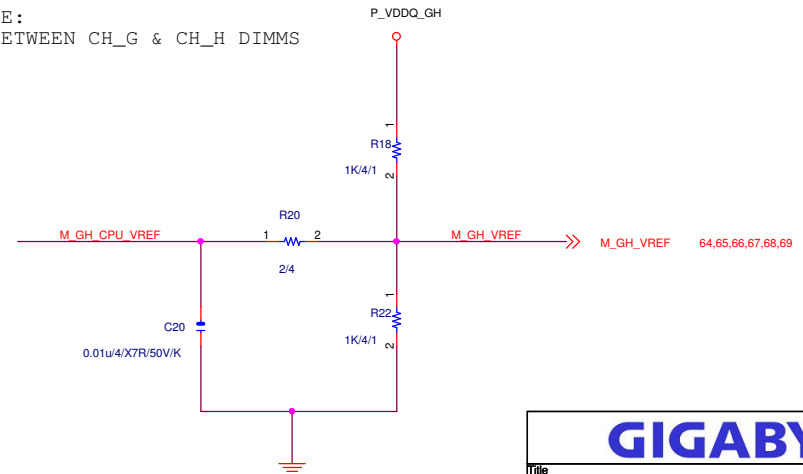
Layout NOTE:
Reduce the stub effect.



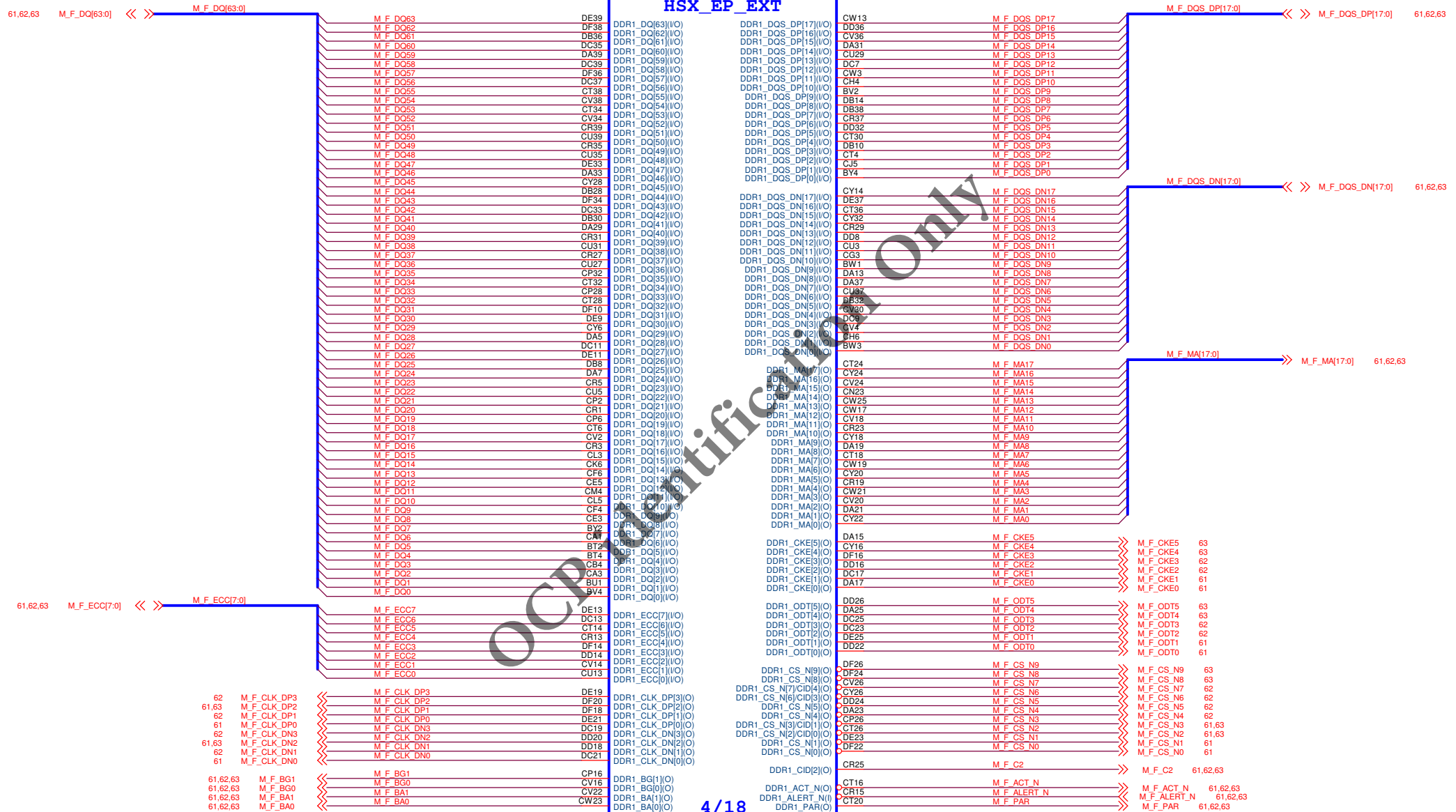
CAD NOTE:
PLACE BETWEEN CH_E & CH_F DIMMS

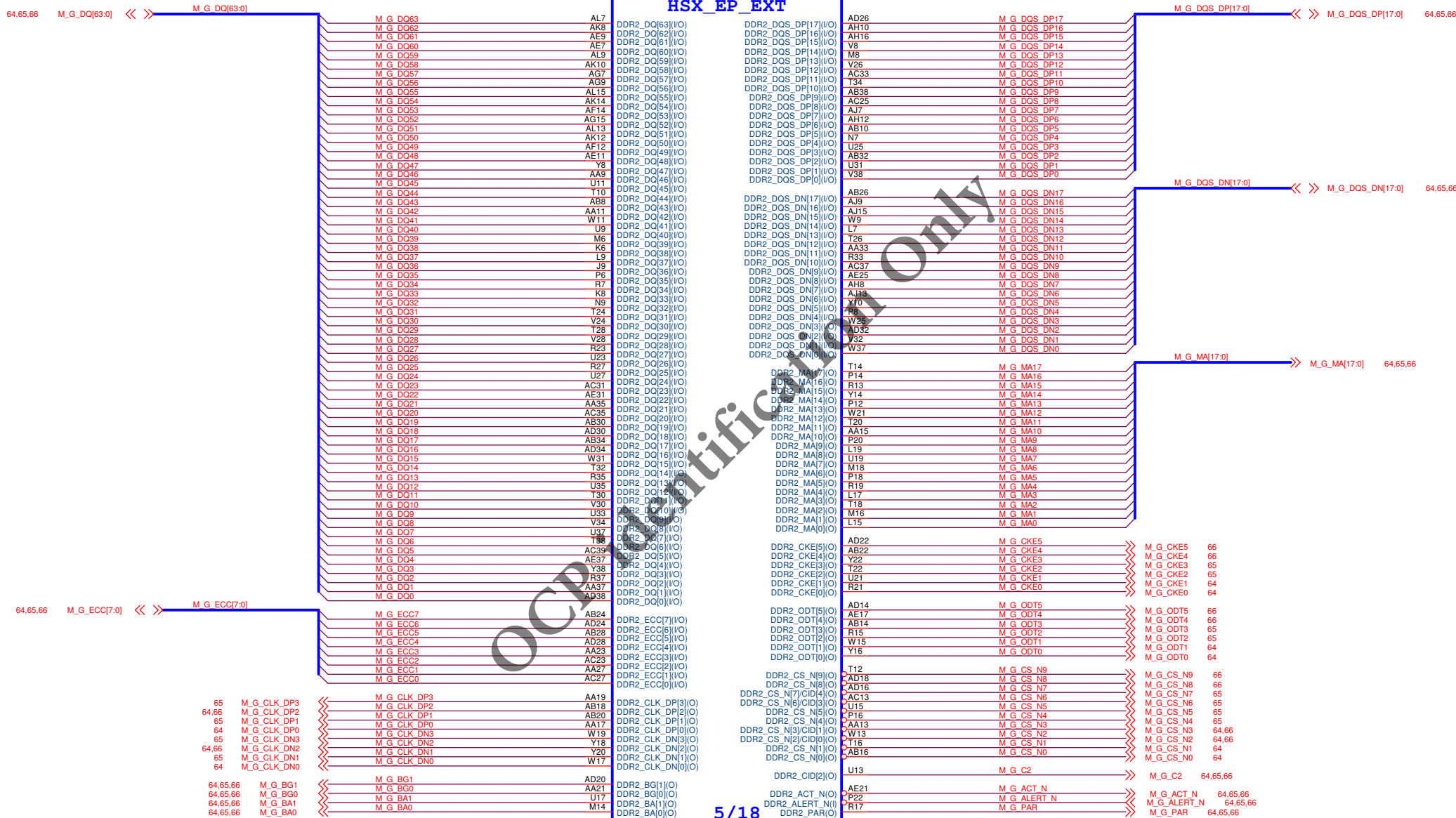


CAD NOTE:
PLACE BETWEEN CH_G & CH_H DIMMS



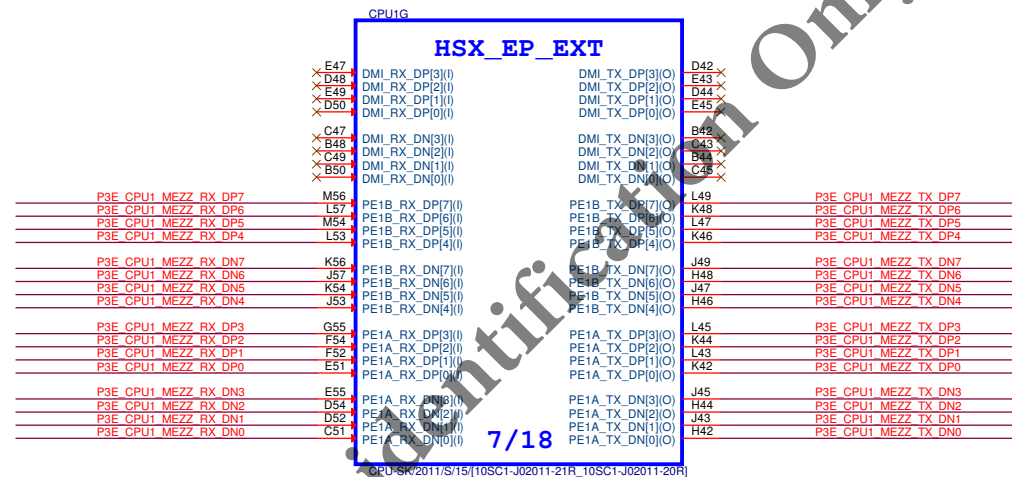
GIGABYTE™		
Title		
CPU1_SOCKET (1/14)		
Size	Document Number	Rev
Custom	MD90-FS0	1.0
Date:	Tuesday, June 09, 2015	Sheet 32 of 231





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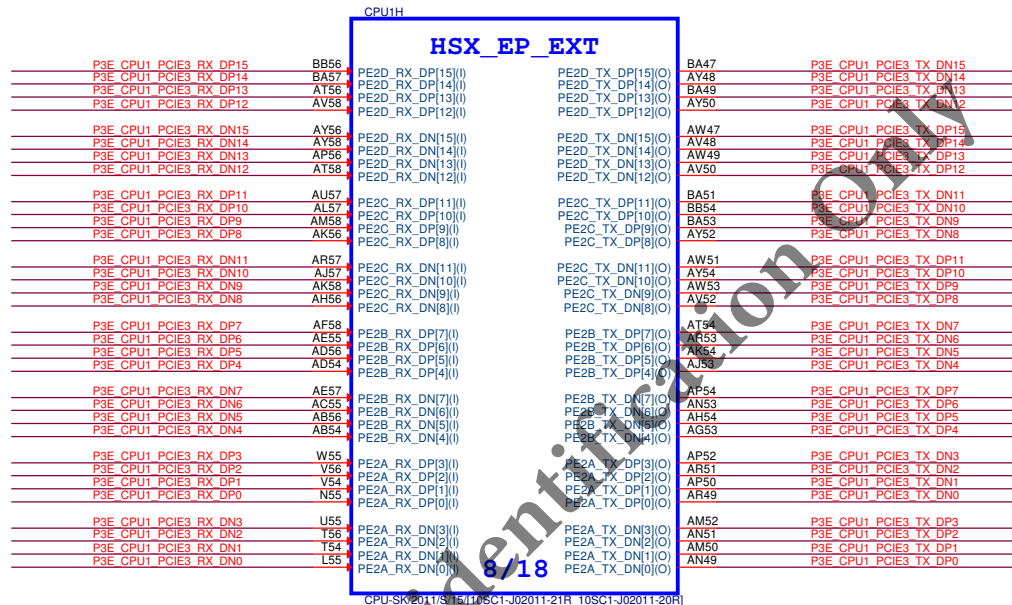
GIGABYTE™			
Title			
CPU1_MEM_CH_G (5/14)			
Size	Document Number		Rev
Custom	MD90-FS0		1.0
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87 P3E_CPU1_MEZZ_RX_DP[7:0]
87 P3E_CPU1_MEZZ_RX_DN[7:0]

>> P3E_CPU1_MEZZ_RX_DP[7:0]
>> P3E_CPU1_MEZZ_RX_DN[7:0]

P3E_CPU1_MEZZ_TX_DP[7:0] >> P3E_CPU1_MEZZ_TX_DP[7:0] 87
P3E_CPU1_MEZZ_TX_DN[7:0] >> P3E_CPU1_MEZZ_TX_DN[7:0] 87



86 P3E_CPU1_PCIE3_RX_DN[15:0] >> P3E_CPU1_PCIE3_RX_DN[15:0]

86 P3E_CPU1_PCIE3_RX_DP[15:0] >> P3E_CPU1_PCIE3_RX_DP[15:0]

P3E_CPU1_PCIE3_TX_DP[15:0] >> P3E_CPU1_PCIE3_TX_DP[15:0] 86

P3E_CPU1_PCIE3_TX_DN[15:0] >> P3E_CPU1_PCIE3_TX_DN[15:0] 86

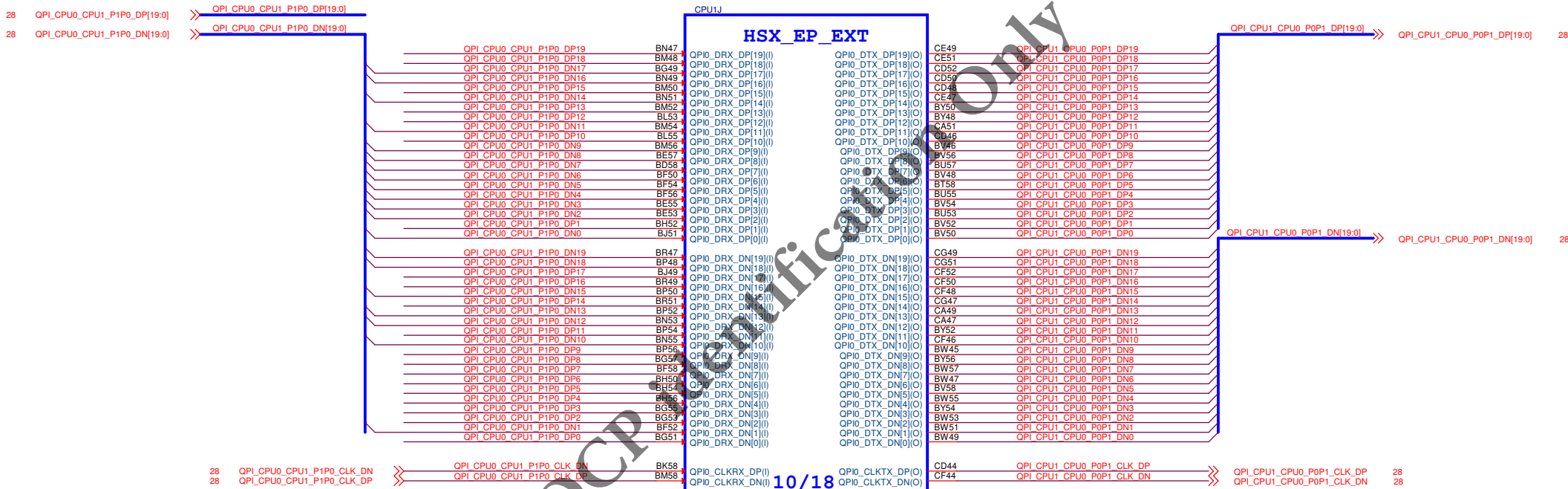
CPU11			
HSX_EP_EXT			
P3E_CPU1_PCIE2_RX_DP15	AR45	PE3D_RX_DP[15](I)	PE3D_TX_DP[15](O)
P3E_CPU1_PCIE2_RX_DP14	AP46	PE3D_RX_DP[14](I)	PE3D_TX_DP[14](O)
P3E_CPU1_PCIE2_RX_DP13	AR47	PE3D_RX_DP[13](I)	PE3D_TX_DP[13](O)
P3E_CPU1_PCIE2_RX_DP12	AJ47	PE3D_RX_DP[12](I)	PE3D_TX_DP[12](O)
P3E_CPU1_PCIE2_RX_DN15	AN45	PE3D_RX_DN[15](I)	PE3D_TX_DN[15](O)
P3E_CPU1_PCIE2_RX_DN14	AM46	PE3D_RX_DN[14](I)	PE3D_TX_DN[14](O)
P3E_CPU1_PCIE2_RX_DN13	AN47	PE3D_RX_DN[13](I)	PE3D_TX_DN[13](O)
P3E_CPU1_PCIE2_RX_DN12	AG47	PE3D_RX_DN[12](I)	PE3D_TX_DN[12](O)
P3E_CPU1_PCIE2_RX_DP11	AJ49	PE3C_RX_DP[11](I)	PE3C_TX_DP[11](O)
P3E_CPU1_PCIE2_RX_DP10	AH50	PE3C_RX_DP[10](I)	PE3C_TX_DP[10](O)
P3E_CPU1_PCIE2_RX_DP9	AJ51	PE3C_RX_DP[9](I)	PE3C_TX_DP[9](O)
P3E_CPU1_PCIE2_RX_DP8	AH48	PE3C_RX_DP[8](I)	PE3C_TX_DP[8](O)
P3E_CPU1_PCIE2_RX_DN11	AG49	PE3C_RX_DN[11](I)	PE3C_TX_DN[11](O)
P3E_CPU1_PCIE2_RX_DN10	AF50	PE3C_RX_DN[10](I)	PE3C_TX_DN[10](O)
P3E_CPU1_PCIE2_RX_DN9	AG51	PE3C_RX_DN[9](I)	PE3C_TX_DN[9](O)
P3E_CPU1_PCIE2_RX_DN8	AF48	PE3C_RX_DN[8](I)	PE3C_TX_DN[8](O)
P3E_CPU1_PCIE2_RX_DP7	AC51	PE3B_RX_DP[7](I)	PE3B_TX_DP[7](O)
P3E_CPU1_PCIE2_RX_DP6	AC53	PE3B_RX_DP[6](I)	PE3B_TX_DP[6](O)
P3E_CPU1_PCIE2_RX_DP5	AB52	PE3B_RX_DP[5](I)	PE3B_TX_DP[5](O)
P3E_CPU1_PCIE2_RX_DP4	AB50	PE3B_RX_DP[4](I)	PE3B_TX_DP[4](O)
P3E_CPU1_PCIE2_RX_DN7	AA51	PE3B_RX_DN[7](I)	PE3B_TX_DN[7](O)
P3E_CPU1_PCIE2_RX_DN6	AA53	PE3B_RX_DN[6](I)	PE3B_TX_DN[6](O)
P3E_CPU1_PCIE2_RX_DN5	Y52	PE3B_RX_DN[5](I)	PE3B_TX_DN[5](O)
P3E_CPU1_PCIE2_RX_DN4	Y50	PE3B_RX_DN[4](I)	PE3B_TX_DN[4](O)
P3E_CPU1_PCIE2_RX_DP3	AC49	PE3A_RX_DP[3](I)	PE3A_TX_DP[3](O)
P3E_CPU1_PCIE2_RX_DP2	AH46	PE3A_RX_DP[2](I)	PE3A_TX_DP[2](O)
P3E_CPU1_PCIE2_RX_DP1	AJ45	PE3A_RX_DP[1](I)	PE3A_TX_DP[1](O)
P3E_CPU1_PCIE2_RX_DP0	AH44	PE3A_RX_DP[0](I)	PE3A_TX_DP[0](O)
P3E_CPU1_PCIE2_RX_DN3	AA49	PE3A_RX_DN[3](I)	PE3A_TX_DN[3](O)
P3E_CPU1_PCIE2_RX_DN2	AF46	PE3A_RX_DN[2](I)	PE3A_TX_DN[2](O)
P3E_CPU1_PCIE2_RX_DN1	AG45	PE3A_RX_DN[1](I)	PE3A_TX_DN[1](O)
P3E_CPU1_PCIE2_RX_DN0	AF44	PE3A_RX_DN[0](I)	PE3A_TX_DN[0](O)

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85 P3E_CPU1_PCIE2_RX_DN[15:0] >> P3E_CPU1_PCIE2_RX_DN[15:0]
85 P3E_CPU1_PCIE2_RX_DP[15:0] >> P3E_CPU1_PCIE2_RX_DP[15:0]

P3E_CPU1_PCIE2_TX_DP[15:0] >> P3E_CPU1_PCIE2_TX_DP[15:0] 85
P3E_CPU1_PCIE2_TX_DN[15:0] >> P3E_CPU1_PCIE2_TX_DN[15:0] 85



CPUR-SK/2011/S/15(10SC1-J02011-21R_10SC1-J02011-20R)

27 QPI_CPU0_CPU1_P0P1_DP[19:0] >> QPI_CPU0_CPU1_P0P1_DP[19:0]
27 QPI_CPU0_CPU1_P0P1_DN[19:0] >> QPI_CPU0_CPU1_P0P1_DN[19:0]

DESIGN NOTE:
POLARITY INVERSION DONE ON THESE
PAIRS TO REDUCE CROSSTALK

27 QPI_CPU0_CPU1_P0P1_CLK_DN >> QPI_CPU0_CPU1_P0P1_CLK_DN
27 QPI_CPU0_CPU1_P0P1_CLK_DP >> QPI_CPU0_CPU1_P0P1_CLK_DP

QPI_CPU0_CPU1_P0P1_DN19
QPI_CPU0_CPU1_P0P1_DN18
QPI_CPU0_CPU1_P0P1_DN17
QPI_CPU0_CPU1_P0P1_DN16
QPI_CPU0_CPU1_P0P1_DP15
QPI_CPU0_CPU1_P0P1_DP14
QPI_CPU0_CPU1_P0P1_DP13
QPI_CPU0_CPU1_P0P1_DP12
QPI_CPU0_CPU1_P0P1_DP11
QPI_CPU0_CPU1_P0P1_DN10
QPI_CPU0_CPU1_P0P1_DP9
QPI_CPU0_CPU1_P0P1_DP8
QPI_CPU0_CPU1_P0P1_DP7
QPI_CPU0_CPU1_P0P1_DP6
QPI_CPU0_CPU1_P0P1_DP5
QPI_CPU0_CPU1_P0P1_DP4
QPI_CPU0_CPU1_P0P1_DP3
QPI_CPU0_CPU1_P0P1_DN2
QPI_CPU0_CPU1_P0P1_DN1
QPI_CPU0_CPU1_P0P1_DN0

QPI_CPU0_CPU1_P0P1_DP19
QPI_CPU0_CPU1_P0P1_DP18
QPI_CPU0_CPU1_P0P1_DP17
QPI_CPU0_CPU1_P0P1_DP16
QPI_CPU0_CPU1_P0P1_DN15
QPI_CPU0_CPU1_P0P1_DN14
QPI_CPU0_CPU1_P0P1_DN13
QPI_CPU0_CPU1_P0P1_DN12
QPI_CPU0_CPU1_P0P1_DN11
QPI_CPU0_CPU1_P0P1_DP10
QPI_CPU0_CPU1_P0P1_DN9
QPI_CPU0_CPU1_P0P1_DN8
QPI_CPU0_CPU1_P0P1_DN7
QPI_CPU0_CPU1_P0P1_DN6
QPI_CPU0_CPU1_P0P1_DN5
QPI_CPU0_CPU1_P0P1_DN4
QPI_CPU0_CPU1_P0P1_DN3
QPI_CPU0_CPU1_P0P1_DP2
QPI_CPU0_CPU1_P0P1_DP1
QPI_CPU0_CPU1_P0P1_DP0

CPU1K

HSX_EP_EXT

QPI1_DRX_DP[19:0]
QPI1_DRX_DP[18:0]
QPI1_DRX_DP[17:0]
QPI1_DRX_DP[16:0]
QPI1_DRX_DP[15:0]
QPI1_DRX_DP[14:0]
QPI1_DRX_DP[13:0]
QPI1_DRX_DP[12:0]
QPI1_DRX_DP[11:0]
QPI1_DRX_DP[10:0]
QPI1_DRX_DP[9:0]
QPI1_DRX_DP[8:0]
QPI1_DRX_DP[7:0]
QPI1_DRX_DP[6:0]
QPI1_DRX_DP[5:0]
QPI1_DRX_DP[4:0]
QPI1_DRX_DP[3:0]
QPI1_DRX_DP[2:0]
QPI1_DRX_DP[1:0]
QPI1_DRX_DP[0:0]

QPI1_DRX_DN[19:0]
QPI1_DRX_DN[18:0]
QPI1_DRX_DN[17:0]
QPI1_DRX_DN[16:0]
QPI1_DRX_DN[15:0]
QPI1_DRX_DN[14:0]
QPI1_DRX_DN[13:0]
QPI1_DRX_DN[12:0]
QPI1_DRX_DN[11:0]
QPI1_DRX_DN[10:0]
QPI1_DRX_DN[9:0]
QPI1_DRX_DN[8:0]
QPI1_DRX_DN[7:0]
QPI1_DRX_DN[6:0]
QPI1_DRX_DN[5:0]
QPI1_DRX_DN[4:0]
QPI1_DRX_DN[3:0]
QPI1_DRX_DN[2:0]
QPI1_DRX_DN[1:0]
QPI1_DRX_DN[0:0]

QPI1_CLKRX_DP(I)
QPI1_CLKRX_DN(I)

QPI1_DTX_DP[19:0]
QPI1_DTX_DP[18:0]
QPI1_DTX_DP[17:0]
QPI1_DTX_DP[16:0]
QPI1_DTX_DP[15:0]
QPI1_DTX_DP[14:0]
QPI1_DTX_DP[13:0]
QPI1_DTX_DP[12:0]
QPI1_DTX_DP[11:0]
QPI1_DTX_DP[10:0]
QPI1_DTX_DP[9:0]
QPI1_DTX_DP[8:0]
QPI1_DTX_DP[7:0]
QPI1_DTX_DP[6:0]
QPI1_DTX_DP[5:0]
QPI1_DTX_DP[4:0]
QPI1_DTX_DP[3:0]
QPI1_DTX_DP[2:0]
QPI1_DTX_DP[1:0]
QPI1_DTX_DP[0:0]

QPI1_DTX_DN[19:0]
QPI1_DTX_DN[18:0]
QPI1_DTX_DN[17:0]
QPI1_DTX_DN[16:0]
QPI1_DTX_DN[15:0]
QPI1_DTX_DN[14:0]
QPI1_DTX_DN[13:0]
QPI1_DTX_DN[12:0]
QPI1_DTX_DN[11:0]
QPI1_DTX_DN[10:0]
QPI1_DTX_DN[9:0]
QPI1_DTX_DN[8:0]
QPI1_DTX_DN[7:0]
QPI1_DTX_DN[6:0]
QPI1_DTX_DN[5:0]
QPI1_DTX_DN[4:0]
QPI1_DTX_DN[3:0]
QPI1_DTX_DN[2:0]
QPI1_DTX_DN[1:0]
QPI1_DTX_DN[0:0]

QPI1_CLKTX_DP(O)
QPI1_CLKTX_DN(O)

QPI_CPU1_CPU0_P1P0_DP19
QPI_CPU1_CPU0_P1P0_DP18
QPI_CPU1_CPU0_P1P0_DP17
QPI_CPU1_CPU0_P1P0_DP16
QPI_CPU1_CPU0_P1P0_DP15
QPI_CPU1_CPU0_P1P0_DP14
QPI_CPU1_CPU0_P1P0_DP13
QPI_CPU1_CPU0_P1P0_DP12
QPI_CPU1_CPU0_P1P0_DP11
QPI_CPU1_CPU0_P1P0_DP10
QPI_CPU1_CPU0_P1P0_DP9
QPI_CPU1_CPU0_P1P0_DP8
QPI_CPU1_CPU0_P1P0_DP7
QPI_CPU1_CPU0_P1P0_DP6
QPI_CPU1_CPU0_P1P0_DP5
QPI_CPU1_CPU0_P1P0_DP4
QPI_CPU1_CPU0_P1P0_DP3
QPI_CPU1_CPU0_P1P0_DP2
QPI_CPU1_CPU0_P1P0_DP1
QPI_CPU1_CPU0_P1P0_DP0

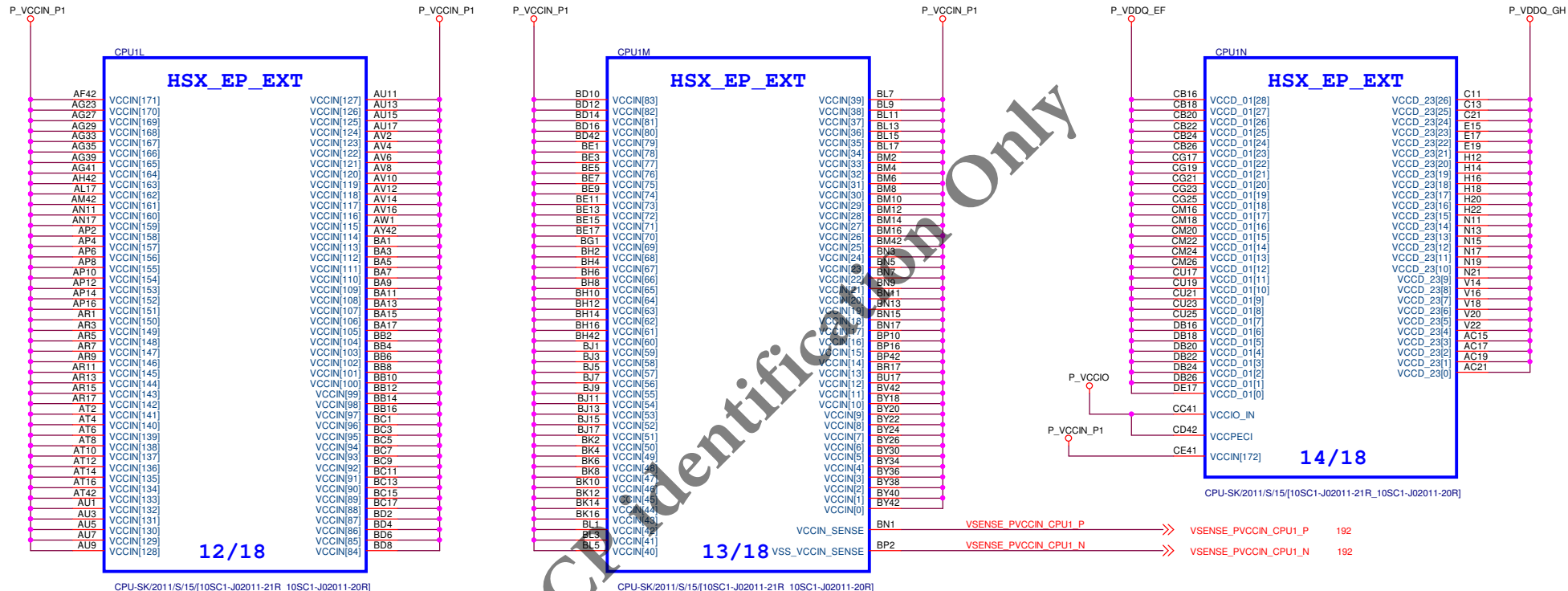
QPI_CPU1_CPU0_P1P0_DN19
QPI_CPU1_CPU0_P1P0_DN18
QPI_CPU1_CPU0_P1P0_DN17
QPI_CPU1_CPU0_P1P0_DN16
QPI_CPU1_CPU0_P1P0_DN15
QPI_CPU1_CPU0_P1P0_DN14
QPI_CPU1_CPU0_P1P0_DN13
QPI_CPU1_CPU0_P1P0_DN12
QPI_CPU1_CPU0_P1P0_DN11
QPI_CPU1_CPU0_P1P0_DN10
QPI_CPU1_CPU0_P1P0_DN9
QPI_CPU1_CPU0_P1P0_DN8
QPI_CPU1_CPU0_P1P0_DN7
QPI_CPU1_CPU0_P1P0_DN6
QPI_CPU1_CPU0_P1P0_DN5
QPI_CPU1_CPU0_P1P0_DN4
QPI_CPU1_CPU0_P1P0_DN3
QPI_CPU1_CPU0_P1P0_DN2
QPI_CPU1_CPU0_P1P0_DN1
QPI_CPU1_CPU0_P1P0_DN0

QPI_CPU1_CPU0_P1P0_CLK_DP
QPI_CPU1_CPU0_P1P0_CLK_DN

QPI_CPU1_CPU0_P1P0_DP[19:0] >> QPI_CPU1_CPU0_P1P0_DP[19:0] 27

QPI_CPU1_CPU0_P1P0_DN[19:0] >> QPI_CPU1_CPU0_P1P0_DN[19:0] 27

CPU-SK/2011/S/15(10SC1-J02011-21R_10SC1-J02011-20R)



CPU1Q

HSX_EP_EXT

A23 VSS[630]
A37 VSS[629]
A39 VSS[629]
A41 VSS[629]
A43 VSS[627]
A45 VSS[626]
A47 VSS[625]
A49 VSS[624]
A5 VSS[623]
A51 VSS[622]
A7 VSS[621]
B10 VSS[620]
B36 VSS[619]
B40 VSS[618]
B52 VSS[617]
B6 VSS[616]
C33 VSS[615]
C5 VSS[614]
C55 VSS[613]
D10 VSS[612]
D24 VSS[611]
D36 VSS[610]
D4 VSS[609]
D40 VSS[608]
E1 VSS[607]
E3 VSS[606]
E39 VSS[605]
E41 VSS[604]
F2 VSS[603]
F30 VSS[602]
F32 VSS[601]
F36 VSS[600]
F42 VSS[599]
F44 VSS[598]
F48 VSS[597]
F50 VSS[596]
F50 VSS[595]
G1 VSS[594]
G23 VSS[593]
G27 VSS[592]
G33 VSS[591]
G35 VSS[590]
G39 VSS[589]
G41 VSS[588]
G45 VSS[587]
G47 VSS[586]
G49 VSS[585]
G5 VSS[584]
G51 VSS[583]
G53 VSS[582]
G57 VSS[581]
G9 VSS[580]
H24 VSS[579]
H26 VSS[578]
H28 VSS[577]
H30 VSS[576]
H32 VSS[575]
H34 VSS[574]
H36 VSS[573]
H40 VSS[572]
H54 VSS[571]
H6 VSS[569]
H8 VSS[568]
J25 VSS[567]
J29 VSS[566]
J3 VSS[565]
J31 VSS[564]
J37 VSS[563]
J5 VSS[562]
J55 VSS[561]
J7 VSS[560]
K10 VSS[559]
K36 VSS[558]
K40 VSS[557]
L29 VSS[556]
L39 VSS[555]
L41 VSS[554]
L5 VSS[553]
M10 VSS[552]

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CPU-SK/2011/S/15(10SC1-J02011-21R_10SC1-J02011-20R)

CPU1P

HSX_EP_EXT

Y36 VSS[472]
Y4 VSS[471]
Y42 VSS[470]
Y56 VSS[469]
AA3 VSS[468]
AA5 VSS[467]
AA29 VSS[466]
AA7 VSS[465]
AA31 VSS[464]
AA39 VSS[463]
AA55 VSS[462]
AB12 VSS[461]
AB2 VSS[460]
AB40 VSS[459]
AB42 VSS[458]
AC7 VSS[457]
AC11 VSS[456]
AC29 VSS[455]
AD4 VSS[454]
AD8 VSS[453]
AD6 VSS[452]
AD10 VSS[451]
AD12 VSS[450]
AD36 VSS[449]
AD49 VSS[448]
AD42 VSS[447]
AD44 VSS[446]
AD45 VSS[445]
AD48 VSS[444]
AD50 VSS[443]
AD52 VSS[442]
AE13 VSS[441]
AE15 VSS[440]
AE19 VSS[439]
AE23 VSS[438]
AE27 VSS[437]
AE29 VSS[436]
AE33 VSS[435]
AE35 VSS[434]
AE39 VSS[433]
AE41 VSS[432]
AE43 VSS[431]
AE47 VSS[430]
AE49 VSS[429]
AF10 VSS[428]
AF16 VSS[427]
AF18 VSS[426]
AE51 VSS[425]
AE53 VSS[424]
AF2 VSS[423]
AF4 VSS[422]
AF6 VSS[421]
AF8 VSS[420]
AF20 VSS[419]
AF22 VSS[418]
AF24 VSS[417]
AF26 VSS[416]
AF28 VSS[415]
AF30 VSS[414]
AF32 VSS[413]
AF34 VSS[412]
AF36 VSS[411]
AF38 VSS[410]
AF40 VSS[409]
AF54 VSS[408]
AF56 VSS[407]
AG11 VSS[406]
AG13 VSS[405]
AG17 VSS[404]
AG19 VSS[403]
AG21 VSS[402]
AG25 VSS[401]
AG31 VSS[400]
AG37 VSS[399]
AG43 VSS[398]
AG55 VSS[397]
AG57 VSS[396]
AH2 VSS[395]
AH3 VSS[394]

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CPU-SK/2011/S/15(10SC1-J02011-21R_10SC1-J02011-20R)

AH6 VSS[393]
AH14 VSS[392]
AH58 VSS[391]
AJ11 VSS[390]
AJ17 VSS[389]
AK4 VSS[388]
AK6 VSS[387]
AK16 VSS[386]
AK42 VSS[385]
AK44 VSS[384]
AK46 VSS[383]
AK48 VSS[382]
AK50 VSS[381]
AK52 VSS[380]
AL11 VSS[379]
AL43 VSS[378]
AL45 VSS[377]
AL47 VSS[376]
AL49 VSS[375]
AL51 VSS[374]
AL53 VSS[373]
AM2 VSS[372]
AM4 VSS[371]
AM6 VSS[370]
AM8 VSS[369]
AM10 VSS[368]
AM12 VSS[367]
AM14 VSS[366]
AM16 VSS[365]
AM56 VSS[364]
AN1 VSS[363]
AN3 VSS[362]
AN5 VSS[361]
AN7 VSS[360]
AN9 VSS[359]
AN13 VSS[358]
AN15 VSS[357]
AN55 VSS[356]
AN57 VSS[355]
AP42 VSS[354]
AP44 VSS[353]
AP58 VSS[352]
AT44 VSS[351]
AT46 VSS[350]
AT48 VSS[349]
AT50 VSS[348]
AT52 VSS[347]
AU45 VSS[346]
AU47 VSS[345]
AU49 VSS[344]
AU51 VSS[343]
AU53 VSS[342]
AV42 VSS[341]
AV54 VSS[340]
AV56 VSS[339]
AW11 VSS[338]
AW13 VSS[337]
AW15 VSS[336]
AW17 VSS[335]
AW3 VSS[334]
AW7 VSS[333]
AW9 VSS[332]
AW55 VSS[331]
AW57 VSS[330]
AY2 VSS[329]
AY4 VSS[328]
AY6 VSS[327]
AY8 VSS[326]
AY10 VSS[325]
AY12 VSS[324]
AY14 VSS[323]
AY16 VSS[322]
AY44 VSS[321]
BB42 VSS[320]
BB46 VSS[319]
BB50 VSS[318]
BB58 VSS[317]
BC45 VSS[316]
BC45 VSS[315]

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Title			
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CPU1Q

HSX_EP_EXT

BC47	VSS[314]	VSS[235]	BW15
BC49	VSS[313]	VSS[234]	BW17
BC51	VSS[312]	VSS[233]	BW43
BC53	VSS[311]	VSS[232]	BY8
BC55	VSS[310]	VSS[231]	BY10
BC57	VSS[309]	VSS[230]	BY28
BD52	VSS[308]	VSS[229]	BY32
BD54	VSS[307]	VSS[228]	BY56
BD56	VSS[306]	VSS[227]	CA5
BE49	VSS[305]	VSS[226]	CA13
BE51	VSS[304]	VSS[225]	CA15
BF2	VSS[303]	VSS[224]	CA17
BF4	VSS[302]	VSS[223]	CA19
BF10	VSS[301]	VSS[222]	CA21
BF12	VSS[300]	VSS[221]	CA23
BF14	VSS[299]	VSS[220]	CA25
BF16	VSS[298]	VSS[219]	CA27
BF8	VSS[297]	VSS[218]	CA29
BF9	VSS[296]	VSS[217]	CA31
BF42	VSS[295]	VSS[216]	CA33
BG3	VSS[294]	VSS[215]	CA35
BG5	VSS[293]	VSS[214]	CA37
BG7	VSS[292]	VSS[213]	CA39
BG9	VSS[291]	VSS[212]	CA41
BG11	VSS[290]	VSS[211]	CA43
BG13	VSS[289]	VSS[210]	CA45
BG15	VSS[288]	VSS[209]	CA57
BG17	VSS[287]	VSS[208]	CB2
BG45	VSS[286]	VSS[207]	CB10
BG47	VSS[285]	VSS[206]	CB12
BH58	VSS[284]	VSS[205]	CB14
BJ55	VSS[283]	VSS[204]	CB17
BJ57	VSS[282]	VSS[203]	CB34
BK42	VSS[281]	VSS[202]	CB36
BK48	VSS[280]	VSS[201]	CB38
BK49	VSS[279]	VSS[200]	CB40
BK50	VSS[278]	VSS[199]	CB42
BK52	VSS[277]	VSS[198]	CB44
BK54	VSS[276]	VSS[197]	CB46
BL45	VSS[275]	VSS[196]	CB48
BL49	VSS[274]	VSS[195]	CB50
BN43	VSS[273]	VSS[194]	CB52
BN57	VSS[272]	VSS[193]	CB54
BP4	VSS[271]	VSS[192]	CB56
BP6	VSS[270]	VSS[191]	CC3
BP8	VSS[269]	VSS[190]	CC5
BP12	VSS[268]	VSS[189]	CC7
BP14	VSS[267]	VSS[188]	CC9
BP58	VSS[266]	VSS[187]	CC11
BR1	VSS[265]	VSS[186]	CC33
BR3	VSS[264]	VSS[185]	CC43
BR5	VSS[263]	VSS[184]	CC45
BR7	VSS[262]	VSS[183]	CC47
BR9	VSS[261]	VSS[182]	CC49
BR11	VSS[260]	VSS[181]	CD12
BR13	VSS[259]	VSS[180]	CD4
BR15	VSS[258]	VSS[179]	CD6
BR53	VSS[257]	VSS[178]	CD8
BR55	VSS[256]	VSS[177]	CD40
BR57	VSS[255]	VSS[176]	CE7
BT10	VSS[254]	VSS[175]	CE15
BT16	VSS[253]	VSS[174]	CE43
BT42	VSS[252]	VSS[173]	CE45
BT46	VSS[251]	VSS[172]	CE47
BT48	VSS[250]	VSS[171]	CE12
BT50	VSS[249]	VSS[170]	CF28
BT52	VSS[248]	VSS[169]	CF32
BT54	VSS[247]	VSS[168]	CF27
BT56	VSS[246]	VSS[167]	CG5
BU3	VSS[245]	VSS[166]	CG27
BU5	VSS[244]	VSS[165]	CG7
BU45	VSS[243]	VSS[164]	CG29
BU47	VSS[242]	VSS[163]	CG31
BV10	VSS[241]	VSS[162]	CG33
BV16	VSS[240]	VSS[161]	CG35
BW5	VSS[239]	VSS[160]	CG37
BW7	VSS[238]	VSS[159]	CG39
	VSS[237]	VSS[158]	CT2
	VSS[236]	VSS[157]	CT43
			CG45
			CG53
			CG55

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CPU-SK/2011/S/15[10SC1-J02011-21R_10SC1-J02011-20R]

CPU1R

HSX_EP_EXT

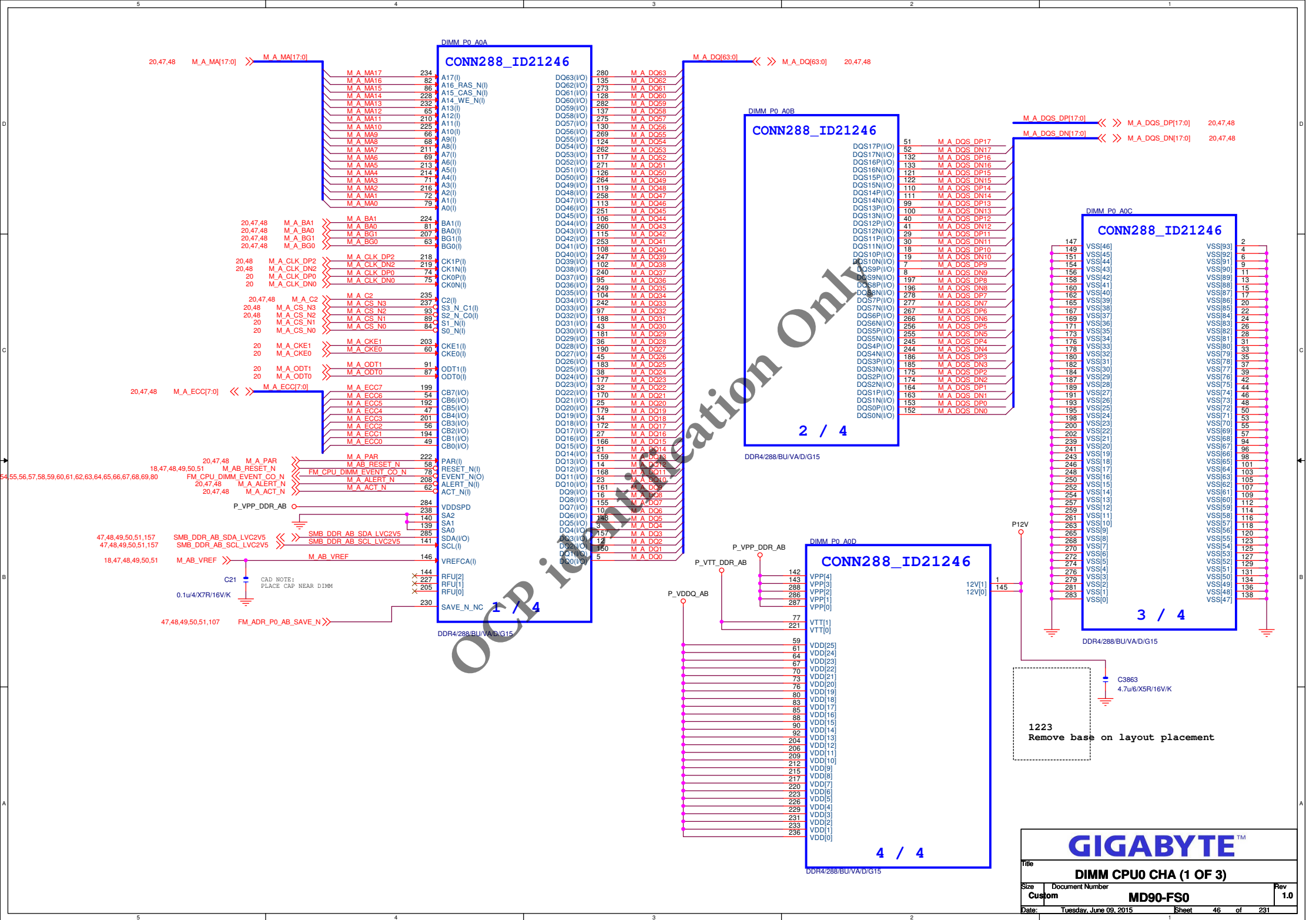
CH12	VSS[156]	CU1
CH30	VSS[155]	CU7
CH34	VSS[154]	CU15
CH36	VSS[153]	CU33
CH38	VSS[152]	CV6
CH40	VSS[151]	CV12
CH42	VSS[150]	CV28
CH44	VSS[149]	CV32
CH46	VSS[148]	CV40
CH48	VSS[147]	CV54
CH50	VSS[146]	CV58
CH52	VSS[145]	CW1
CH54	VSS[144]	CW5
CH56	VSS[143]	CW15
CJ3	VSS[142]	CW27
CJ7	VSS[141]	CW29
CJ15	VSS[140]	CW31
CJ33	VSS[139]	CW33
CJ41	VSS[138]	CW35
CJ43	VSS[137]	CW37
CJ45	VSS[136]	CW39
CJ47	VSS[135]	CW53
CJ49	VSS[134]	CW55
CJ57	VSS[133]	CW57
CK1	VSS[132]	CY2
CK12	VSS[131]	CY4
CK40	VSS[130]	CY8
CK52	VSS[129]	CY10
CK54	VSS[128]	CY12
CL7	VSS[127]	CY30
CL9	VSS[126]	CY34
CL11	VSS[125]	CY36
CL15	VSS[124]	CY42
CM6	VSS[123]	CY44
CM8	VSS[122]	CY46
CM10	VSS[121]	CY48
CM28	VSS[120]	CY50
CM32	VSS[119]	CY52
CM40	VSS[118]	DA3
CM52	VSS[117]	DA9
CM54	VSS[116]	DA27
CN3	VSS[115]	DA35
CN5	VSS[114]	DA41
CN7	VSS[113]	DA43
CN11	VSS[112]	DA45
CN13	VSS[111]	DA47
CN27	VSS[110]	DA49
CN29	VSS[109]	DA51
CN31	VSS[108]	DA53
CN33	VSS[107]	DA55
CN35	VSS[106]	DB6
CN37	VSS[105]	DB12
CN39	VSS[104]	DB34
CN53	VSS[103]	DB40
CN55	VSS[102]	DB58
CN57	VSS[101]	DC5
CP4	VSS[99]	DC53
CP12	VSS[98]	DC55
CP14	VSS[97]	DD6
CP30	VSS[96]	DD10
CP34	VSS[95]	DD12
CP36	VSS[94]	DD34
CP38	VSS[93]	DD38
CP42	VSS[92]	DD40
CP44	VSS[91]	DE7
CP46	VSS[90]	DE15
CP48	VSS[89]	DE35
CP50	VSS[88]	DF8
CP56	VSS[87]	DF12
CP7	VSS[86]	DF40
CR9	VSS[85]	DF42
CR33	VSS[84]	DF44
CR41	VSS[83]	DF46
CR45	VSS[82]	DF48
CR47	VSS[81]	DF50
CR49	VSS[80]	DF52
CT12	VSS[79]	
CT40	VSS[78]	

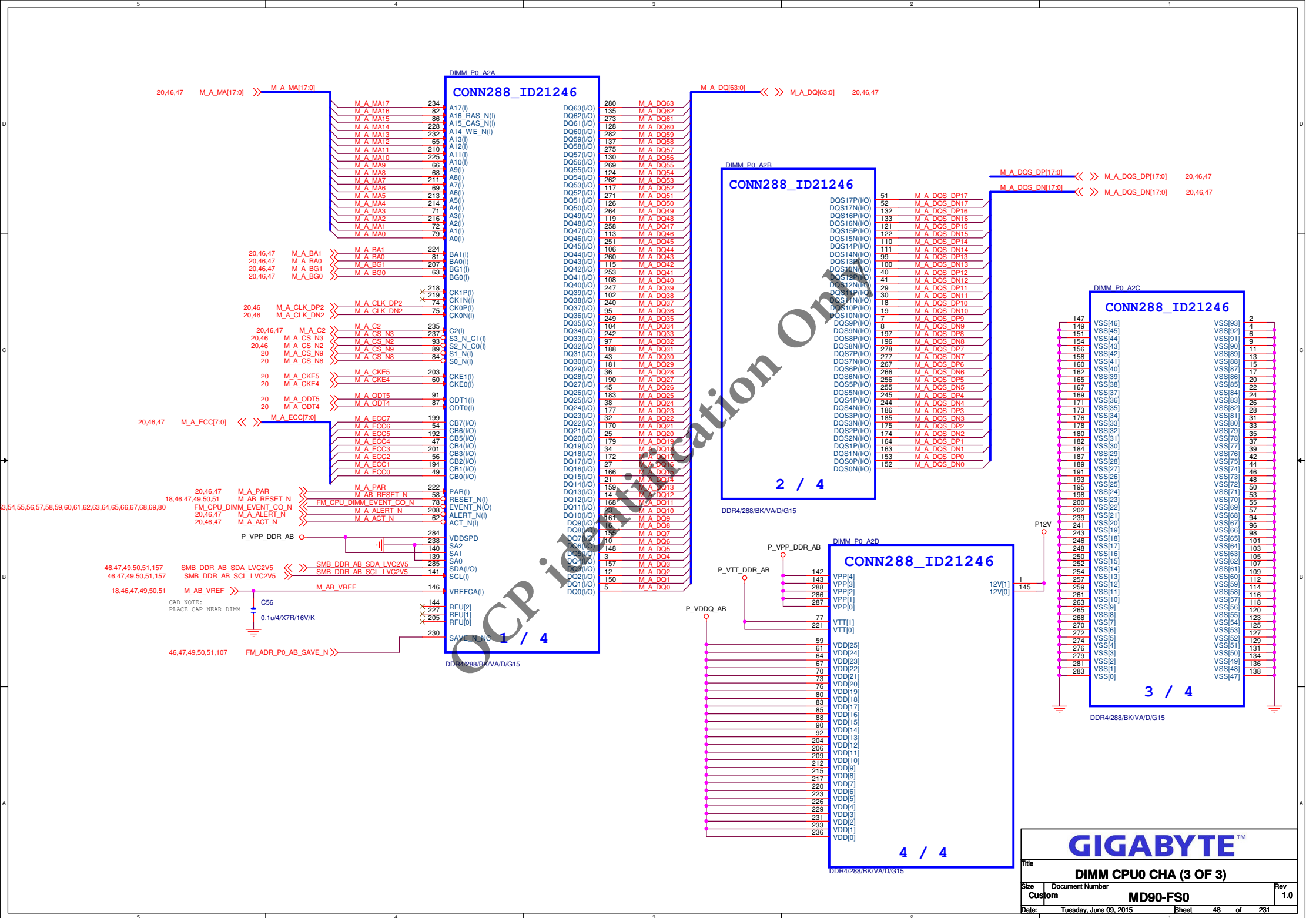
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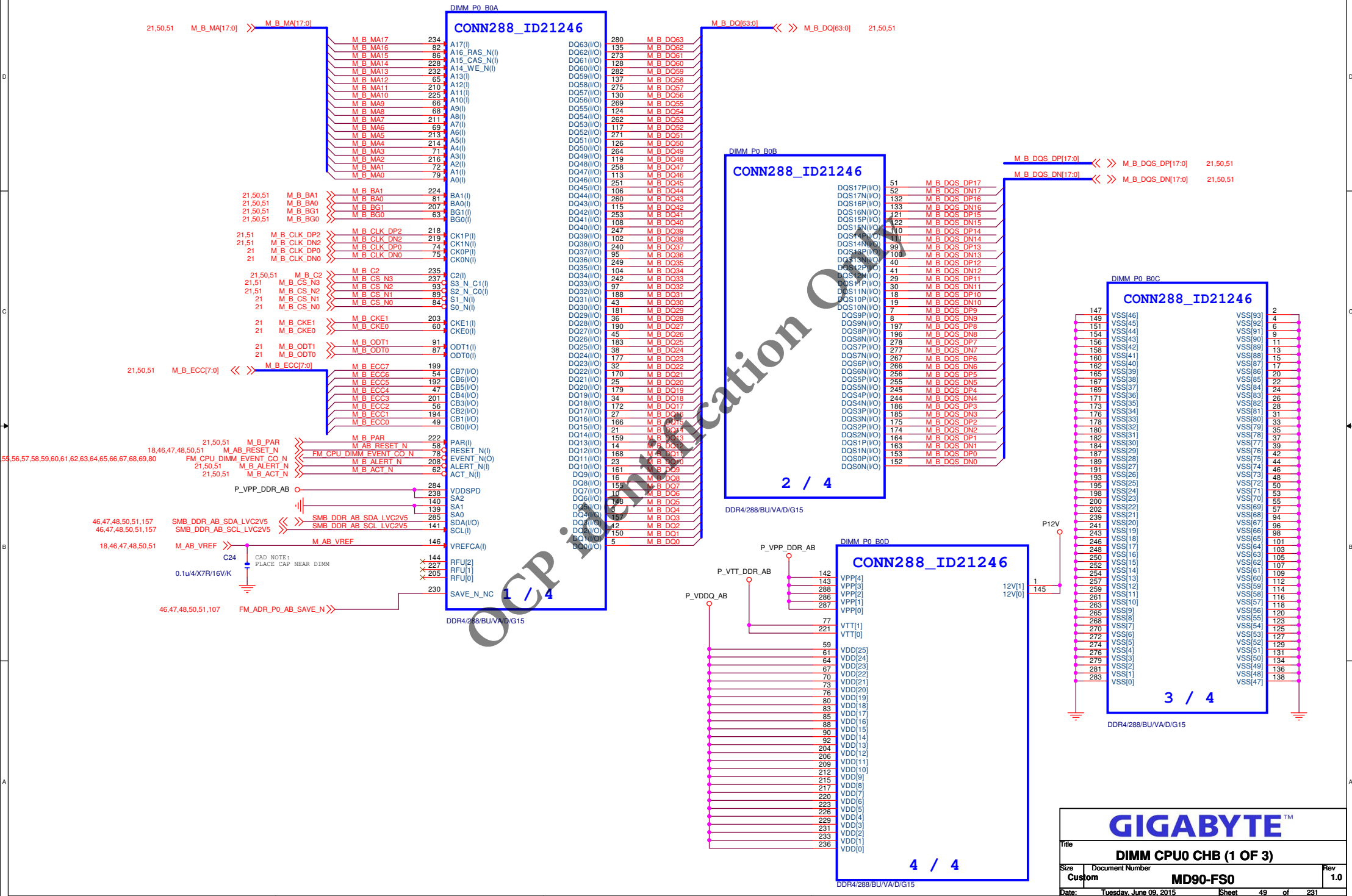
CPU-SK/2011/S/15[10SC1-J02011-21R_10SC1-J02011-20R]

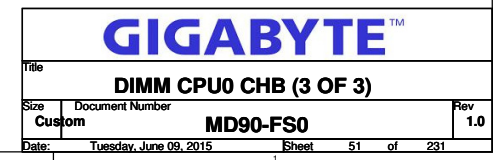
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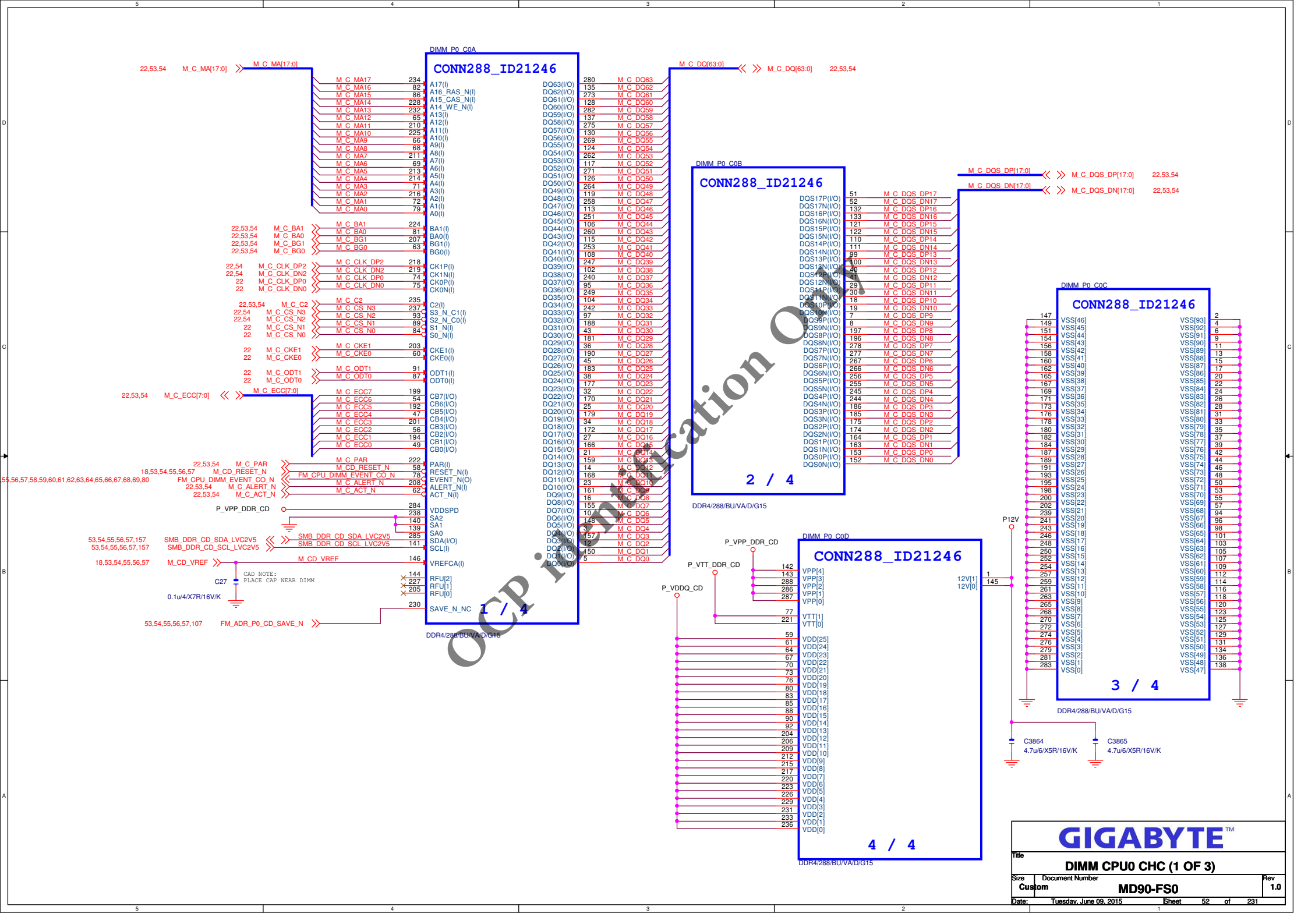
Title				CPU1_GND (14/14)	
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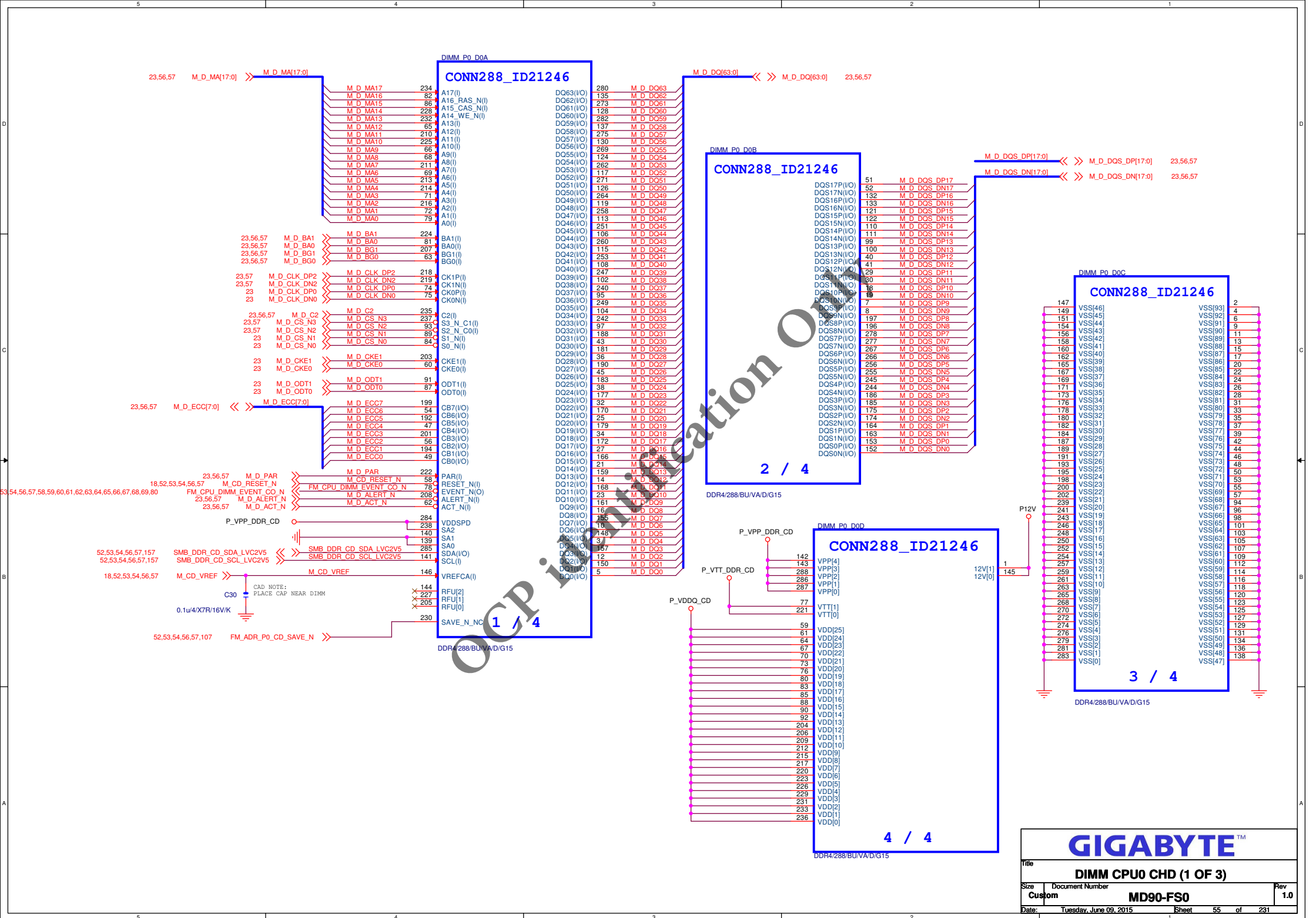


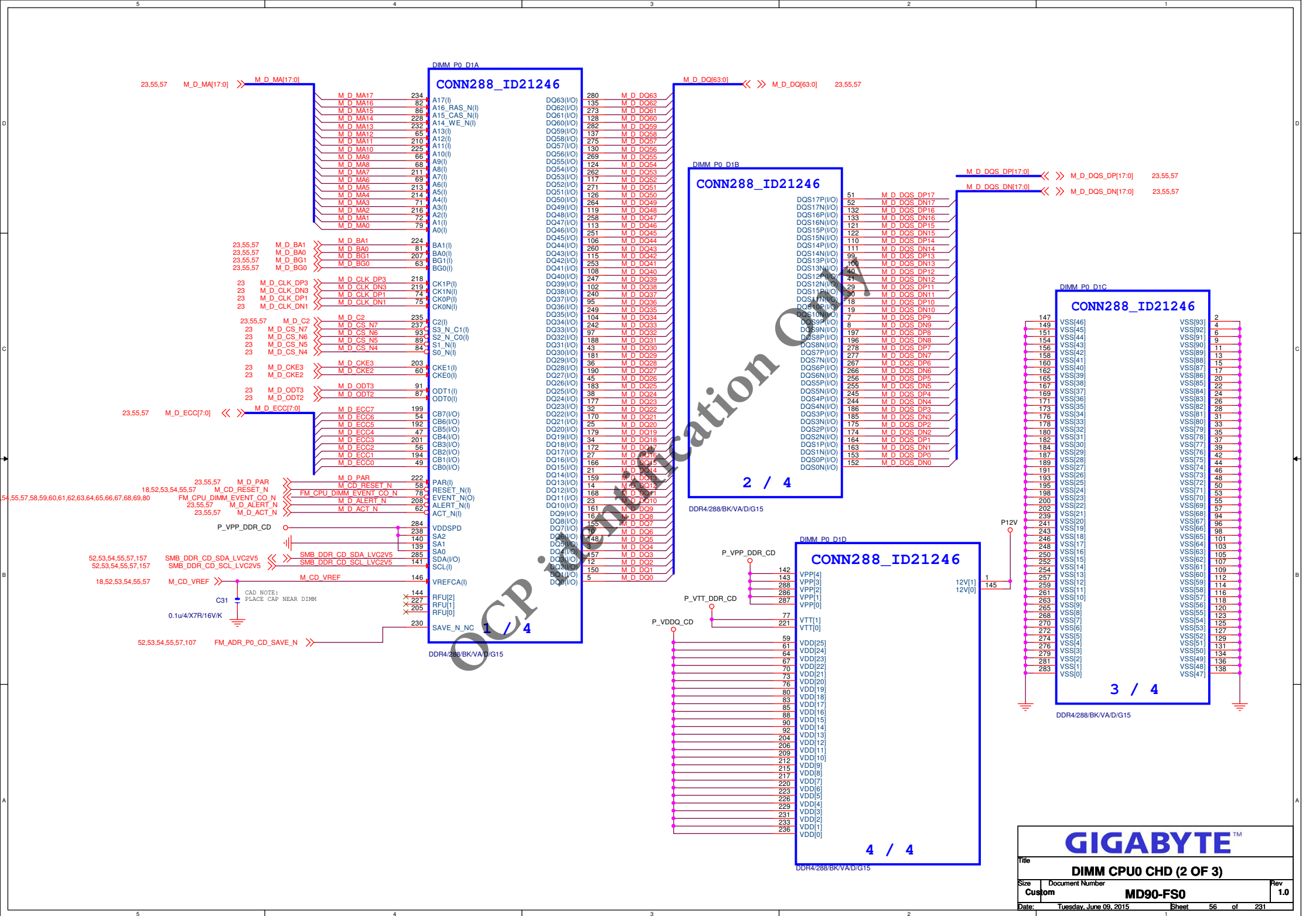


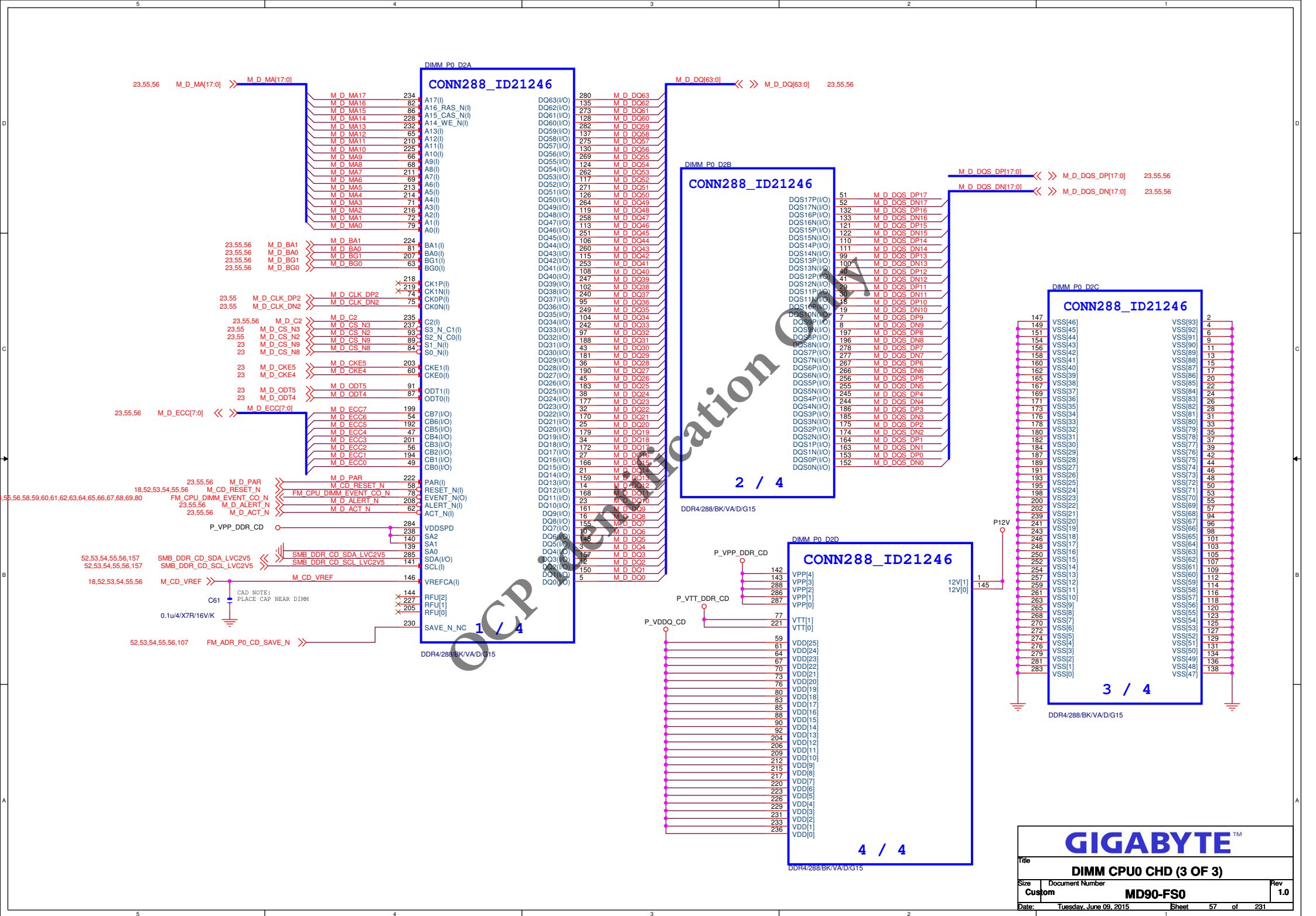


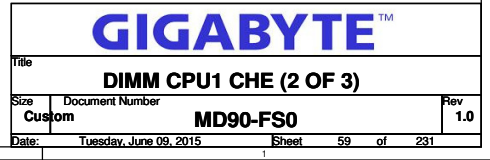


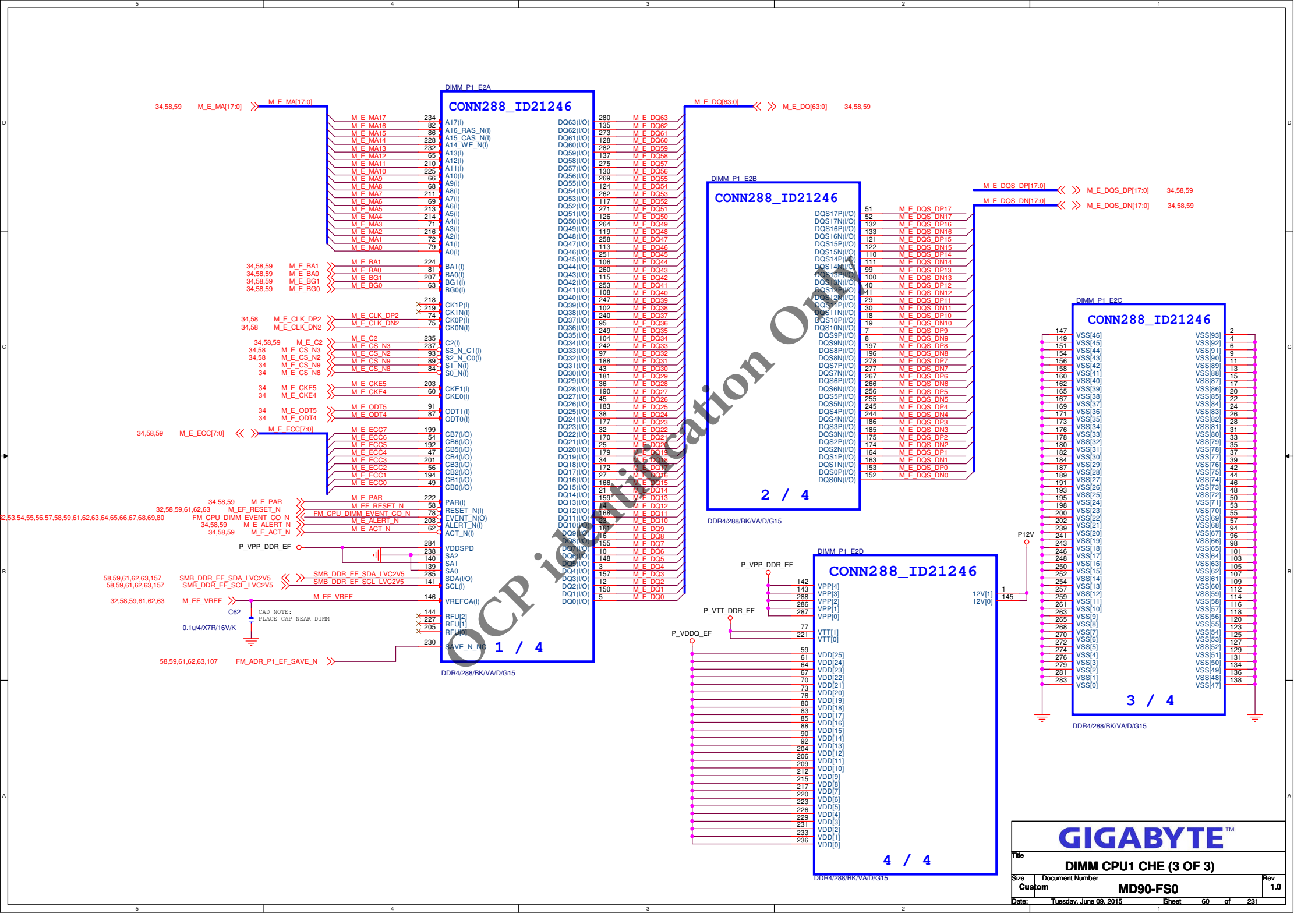


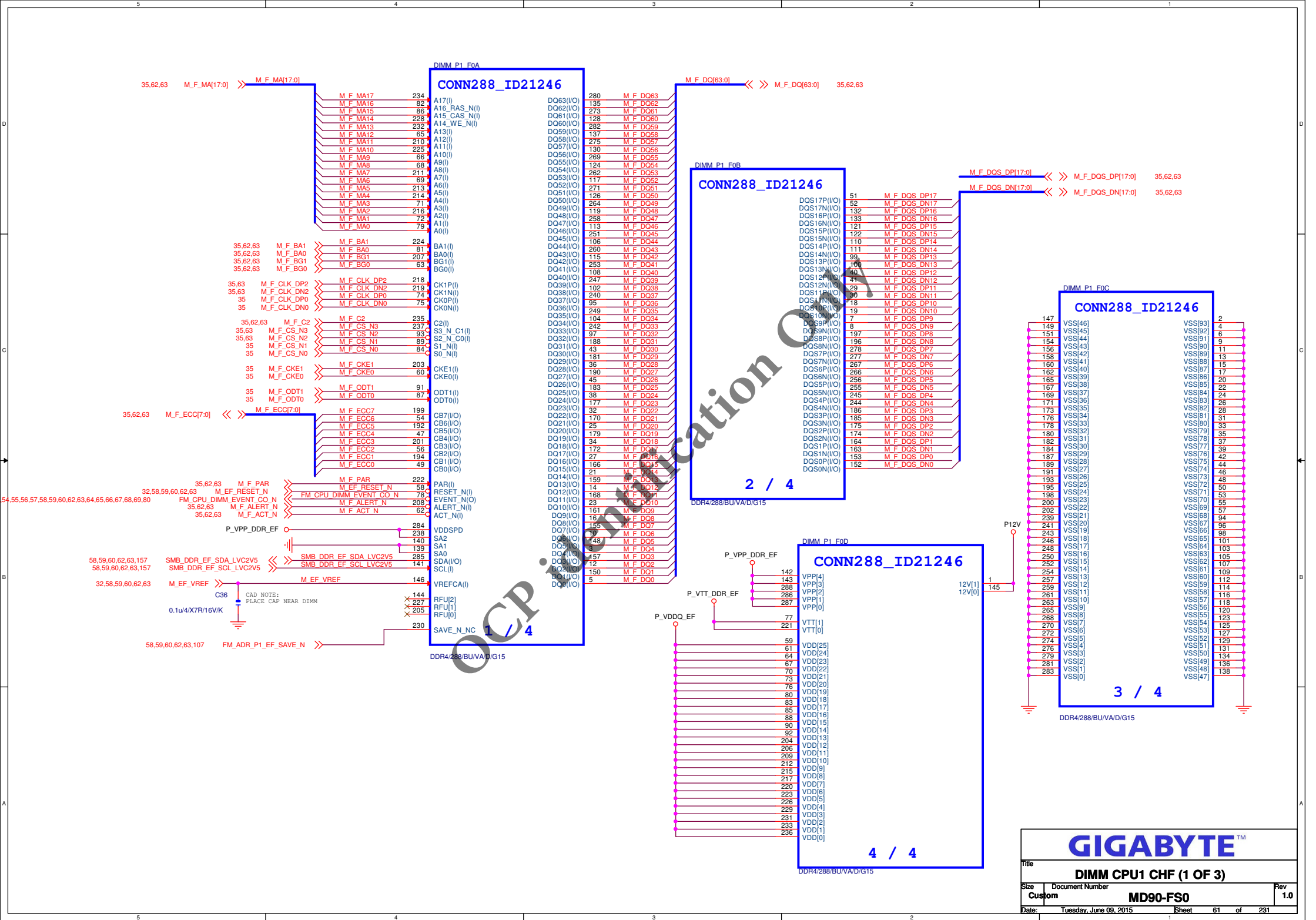


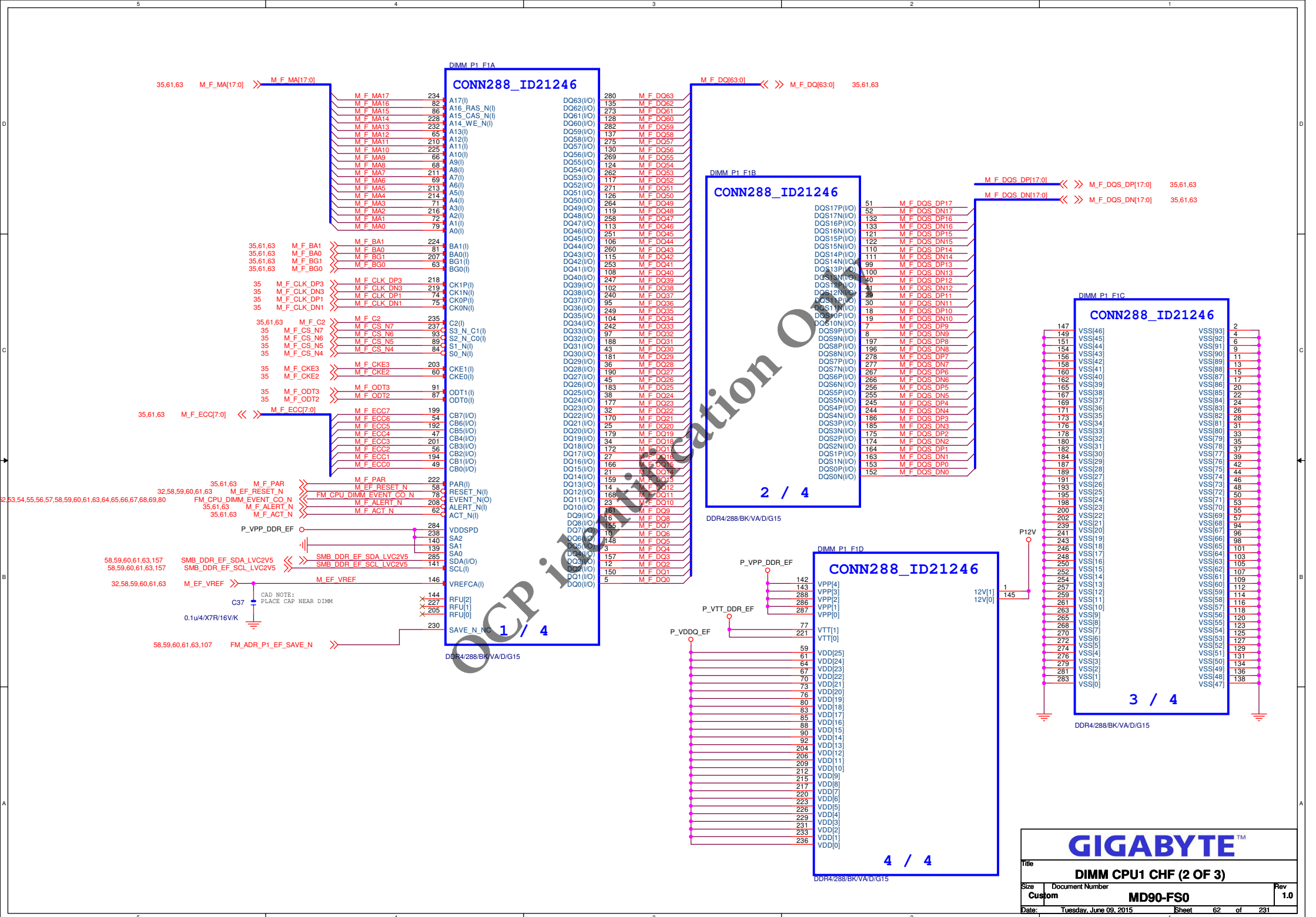


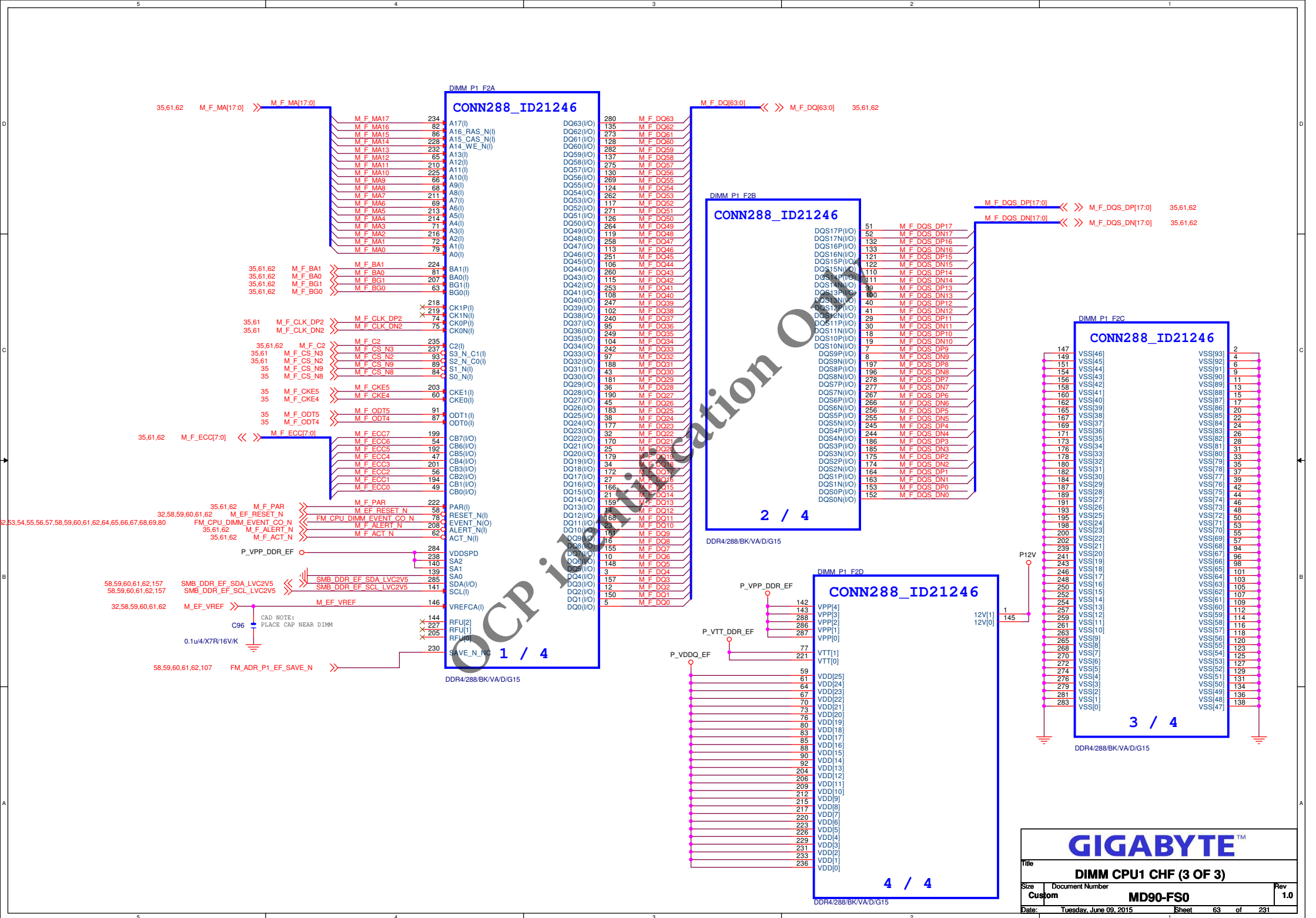


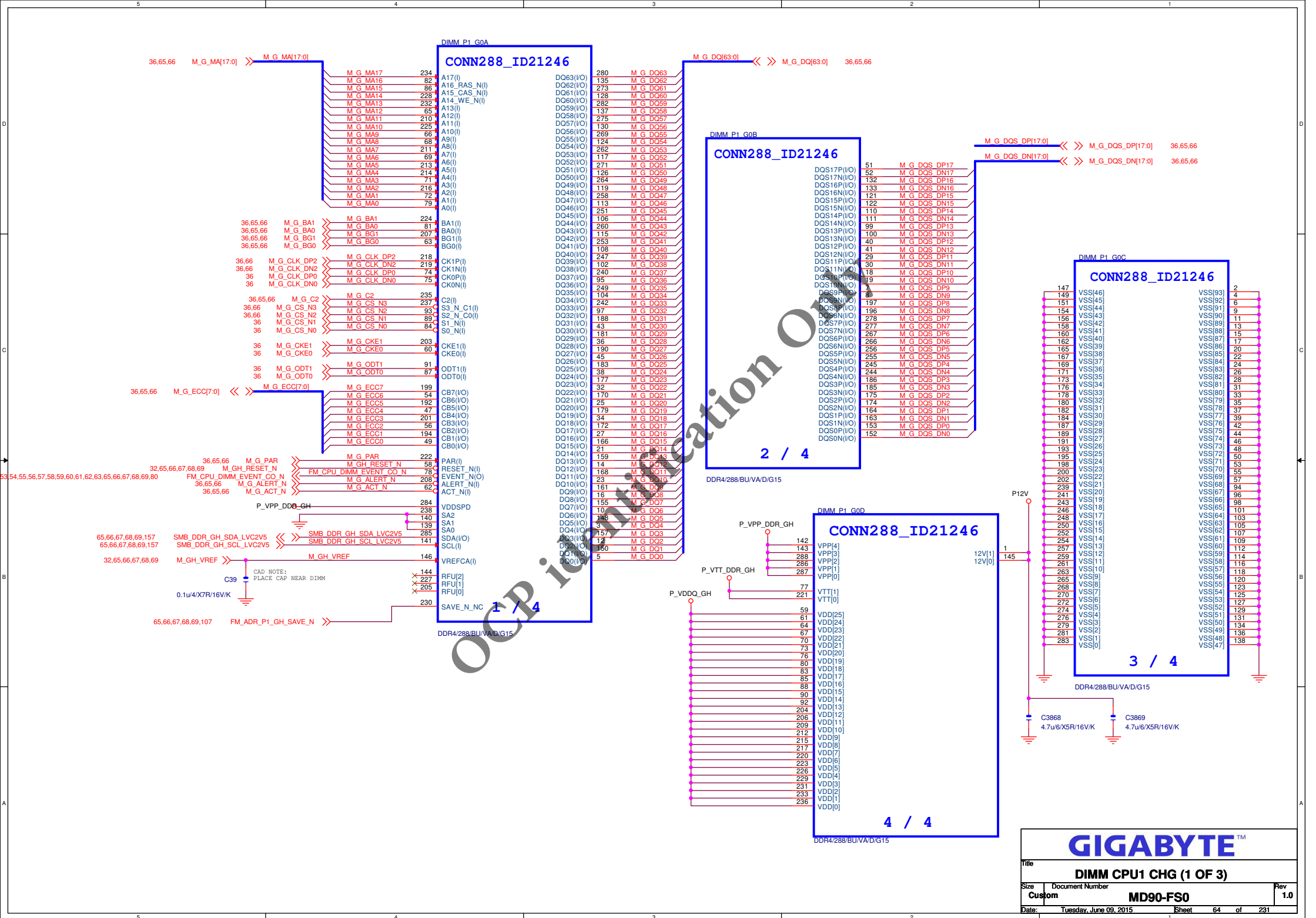


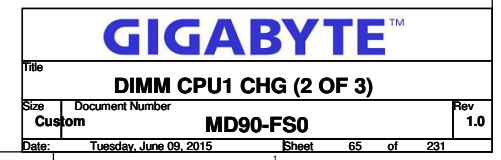


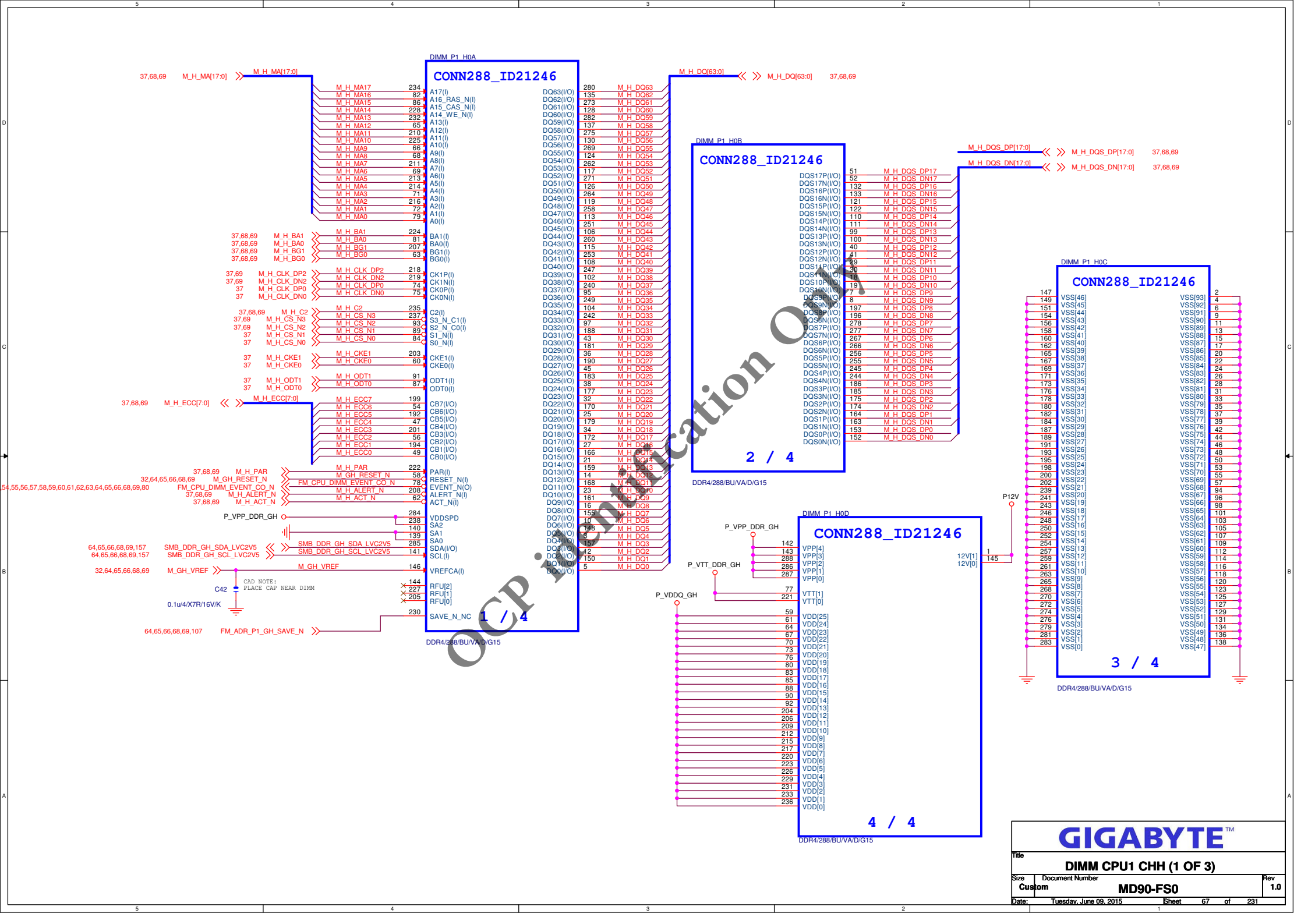


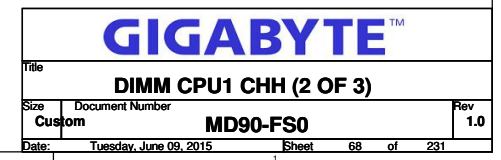


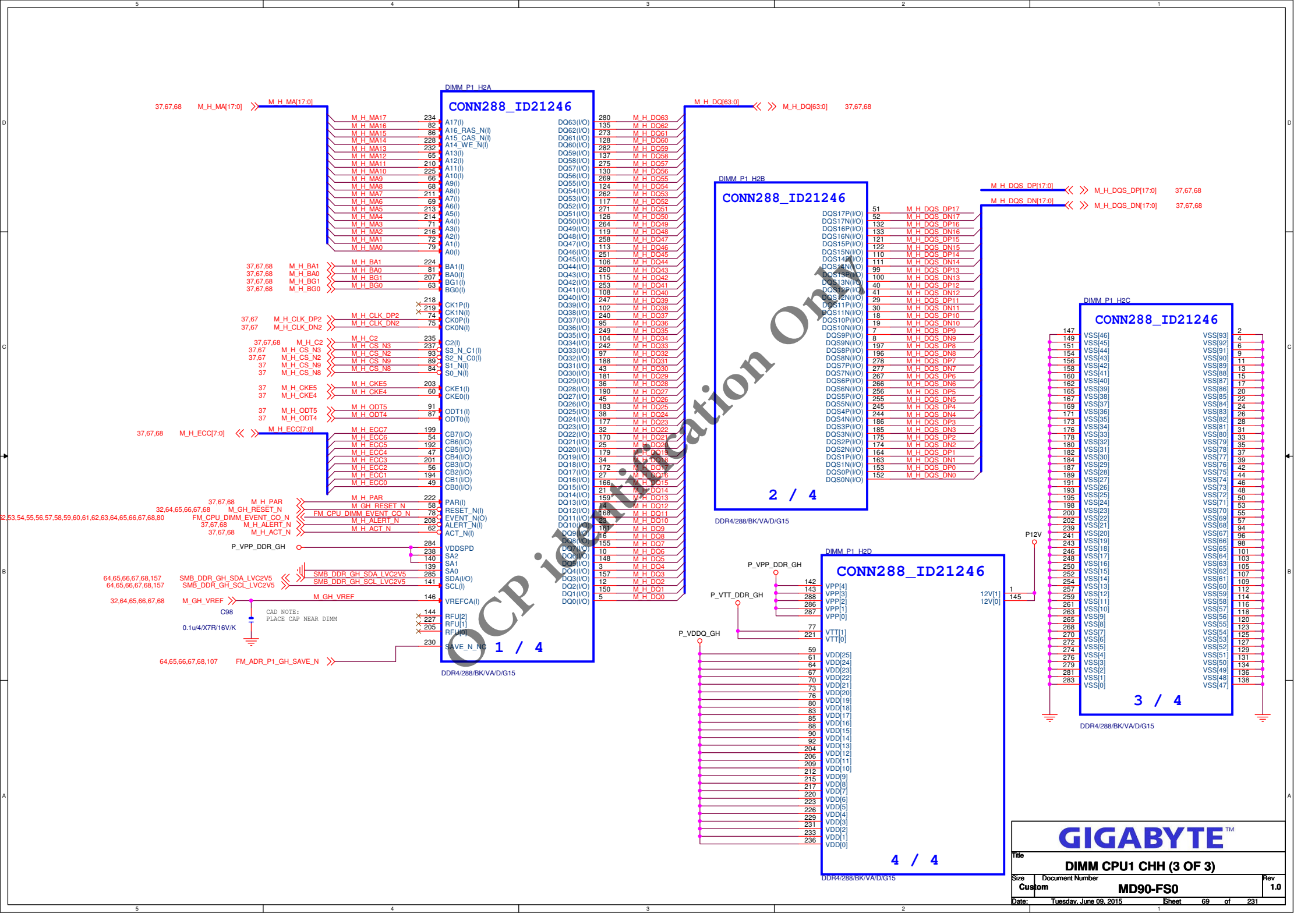






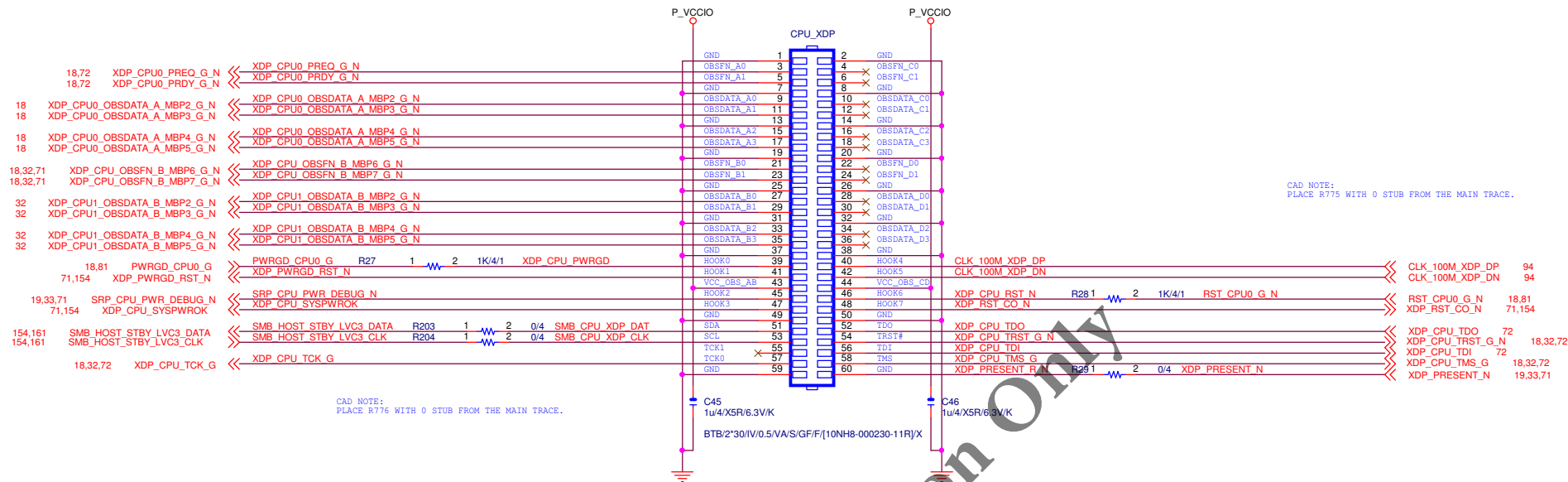


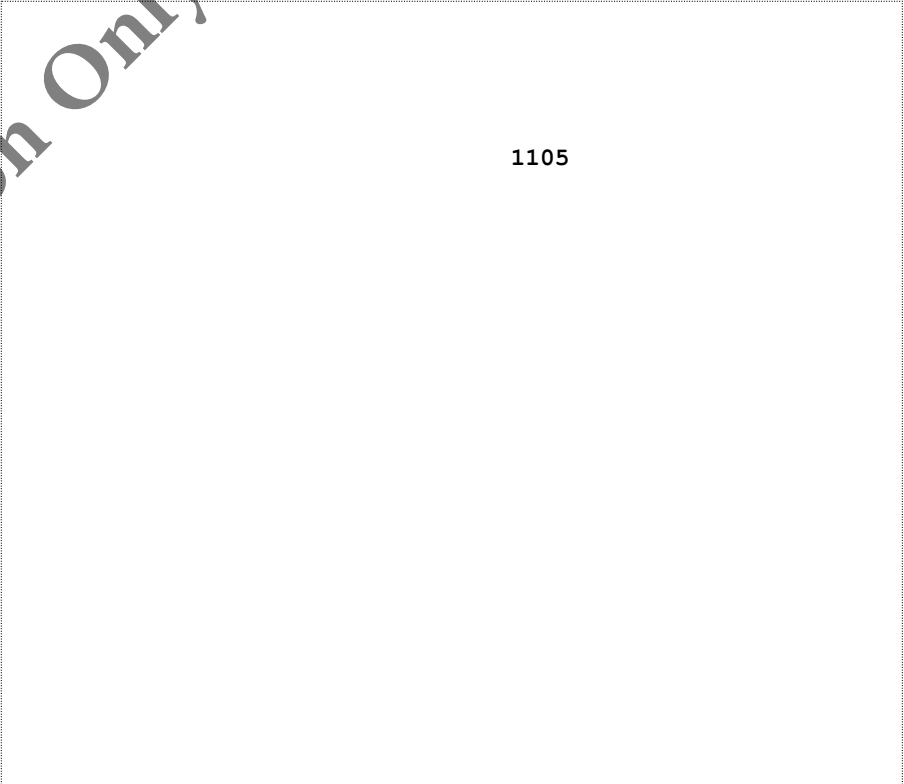
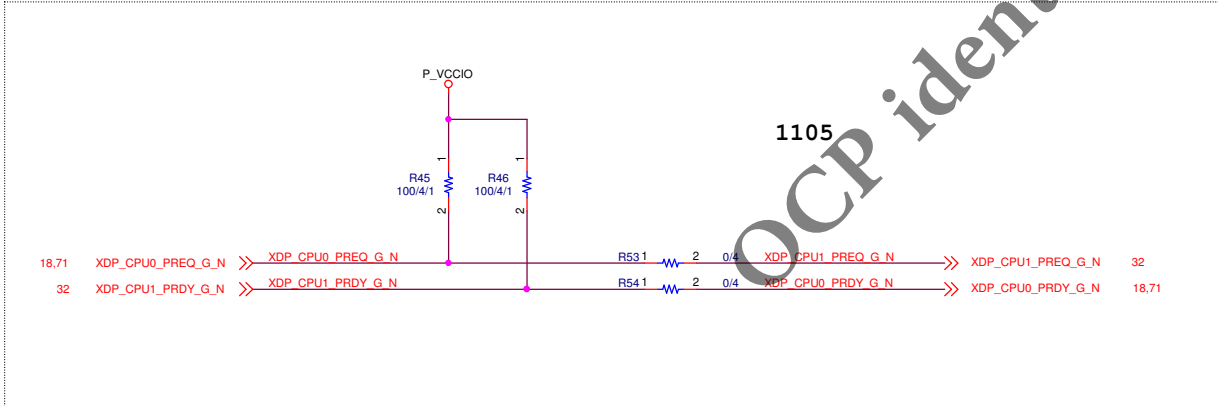
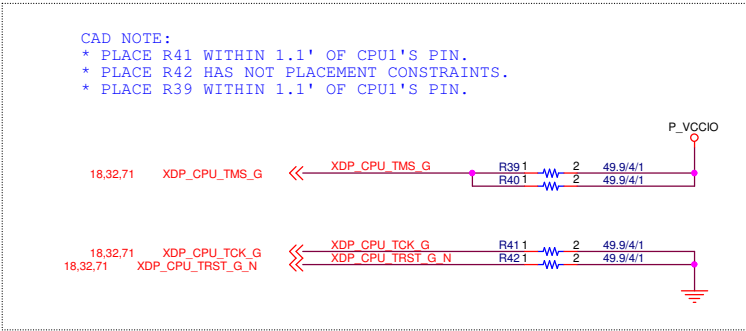
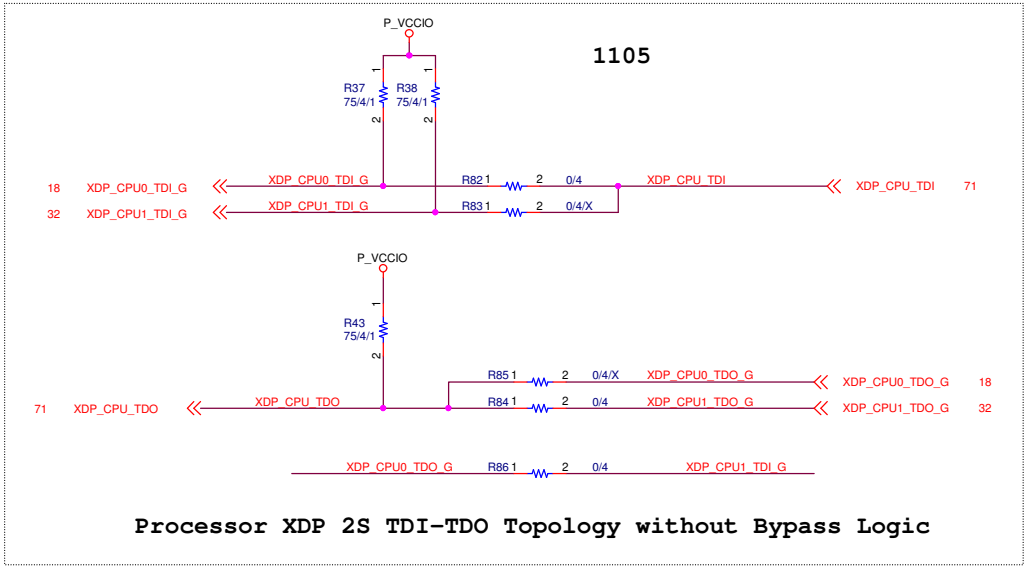




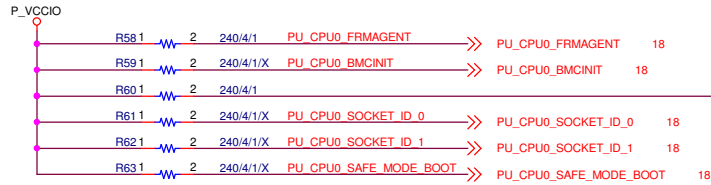
OCP identification Only

GIGABYTE™		
Title		
DECOUPLING CPU0 & CPU1		
Size	Document Number	Rev
Custom	MD90-FS0	1.0
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STRAPS (CPU0)

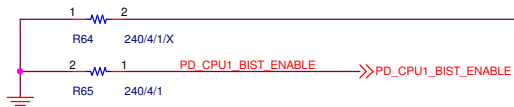
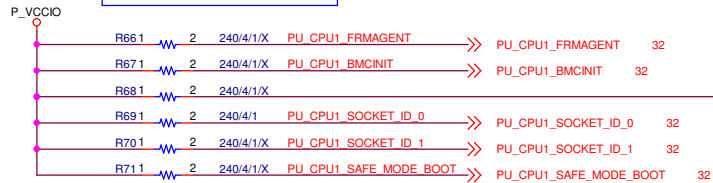


PD_CPU0_TXT_PLTEN >> PD_CPU0_TXT_PLTEN 18

PU_CPU0_TXT_AGENT >> PU_CPU0_TXT_AGENT 18

	HSX Pin Name	When Sampled	Internal PUPD	CPU0 (Default)	CPU1 (Default)	Description	SRP1 (Mayan City)	
							CPU0	CPU1
1	BIST_ENABLE	RESET_N deassertion	PU	1	1	Built-In Self Test (BIST): - 1 = BIST enabled - 0 = BIST disabled	STUFFED 240 ohms Pull-Down	STUFFED 240 ohms Pull-Down
2	BMCINIT	PwRGD assertion	PD	0	0	Service Processor boot mode: - 1 = CPU halts until BMC releases boot flow - 0 = Normal boot flow	EMPTY 240 ohms Pull-up	EMPTY 240 ohms Pull-up
3	FRMAGENT	PwRGD assertion	PD	1	0	Bootable Firmware Agent Strap: For Socket_ID[10] = 00 - 1 = Boot Flash Present, DMI Mode = DMI2 - 0 = Boot Flash Not Present, DMI Mode = DMI2 For Socket_ID[10] = 00 - 1 = Boot Flash NOT Present, DMI Mode = PCIE - 0 = Boot Flash NOT Present, DMI Mode = DMI2 NOTES: - For Grand legacy CPU (Socket ID = 00) must have FRMAGENT = 1	STUFFED 240 ohms Pull-up	EMPTY 240 ohms Pull-up
4	SAFE_MODE_BOOT	PwRGD assertion	PD	0	0	Safe Mode Boot (Disables clock gating): - 1 = Safe Mode Boot enabled - 0 = Safe Mode Boot disabled	EMPTY 240 ohms Pull-up	EMPTY 240 ohms Pull-up
5	SOCKET_ID<0>	PwRGD assertion	PD	0	0	Socket Identifier: Legacy CPU = 00 Non-legacy CPUs = 01,10,11	SOCKET_ID<0>: EMPTY 240 ohms Pull-up	SOCKET_ID<0>: STUFFED 240 ohms Pull-up
6	SOCKET_ID<1>	PwRGD assertion	PD	0	0		SOCKET_ID<1>: EMPTY 240 ohms Pull-up	SOCKET_ID<1>: EMPTY 240 ohms Pull-up
7	TXT_AGENT	PwRGD assertion	PD	0	0	TXT Agent (Drives TXT Transactions): - 1 = CPU is TXT_AGENT - 0 = CPU is not a TXT_AGENT NOTES: - Legacy CPU (Socket ID = 00) needs to be configured as TXT_AGENT if TXT_PLTEN = 1	DIP Switch connected to 240 ohms Pull-up. - DIP Switch Default OFF	DIP Switch connected to 240 ohms Pull-up. - DIP Switch Default OFF
8	TXT_PLTEN	PwRGD assertion	PU	1	1	TXT Enable: - 1 = TXT enabled - 0 = TXT disabled NOTE: All CPUs should be strapped to same value	DIP Switch connected to 240 ohms Pull-down. - DIP Switch Default ON	DIP Switch connected to 240 ohms Pull-down. - DIP Switch Default ON
10	DEBUG_EN_N	CPU_RESET	PU	1	1	In Debug Mode, enables DFX hooks: - 1 = Normal Mode - 0 = Debug Mode	Connected to XDP Pin 60 and to 475 ohms Pull-up	

STRAPS (CPU1)

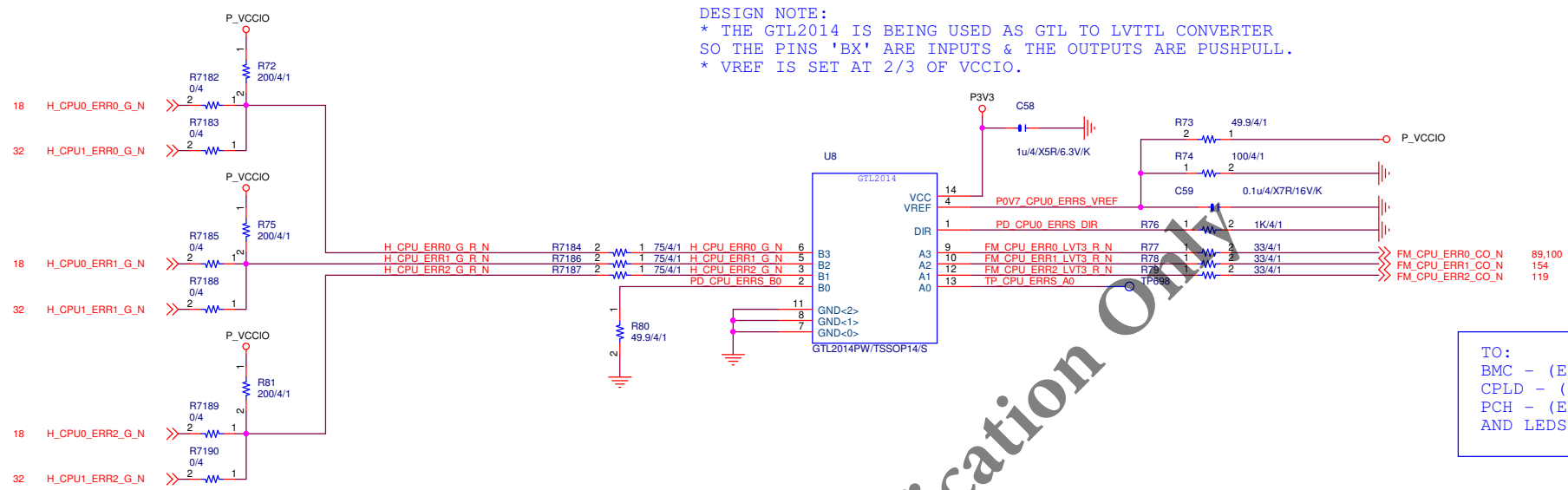


PD_CPU1_TXT_PLTEN >> PD_CPU1_TXT_PLTEN 32

PU_CPU1_TXT_AGENT >> PU_CPU1_TXT_AGENT 32

GIGABYTE™

Title				CPU SIDE BAND: HW STRAPS	
Size	Document Number	Custom		MD90-FS0	Rev 1.0
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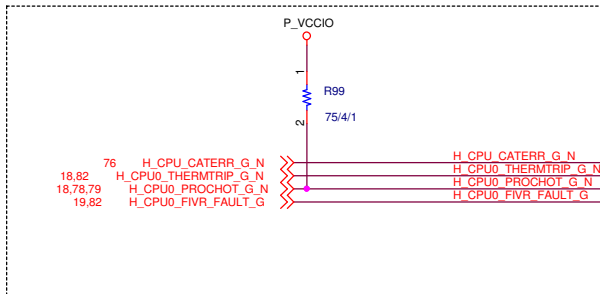


DESIGN NOTE:
* THE GTL2014 IS BEING USED AS GTL TO LVTTTL CONVERTER
SO THE PINS 'BX' ARE INPUTS & THE OUTPUTS ARE PUSH/PULL.
* VREF IS SET AT 2/3 OF VCCIO.

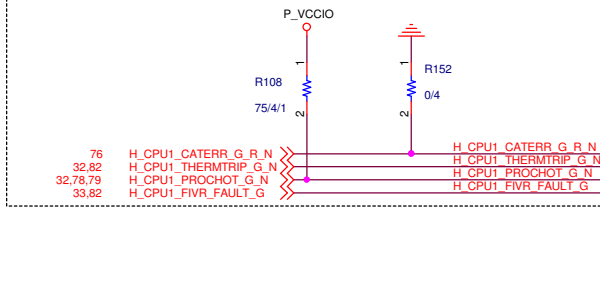
TO:
BMC - (ERR2)
CPLD - (ERR1)
PCH - (ERR0)
AND LEDS

CAD NOTE:
* PLACE CLOSE TO VOLTAGE TRANSLATOR.
* X6S USED TO MEET THERMAL REQUIREMENT.

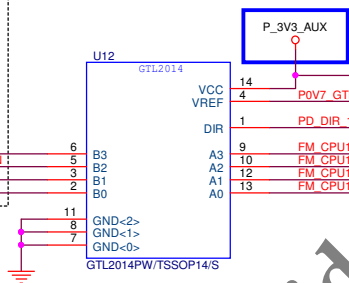
CAD NOTE:
 * PLACE CLOSE TO VOLTAGE TRANSLATOR.
 * X6S USED TO MEET THERMAL REQUIREMENT.



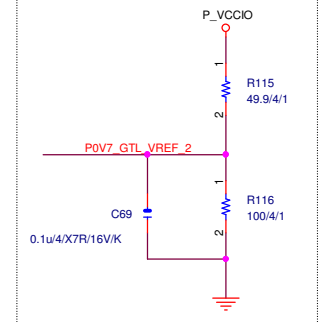
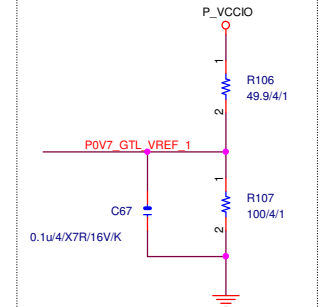
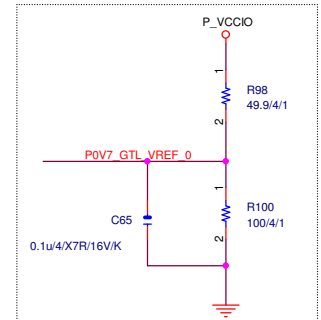
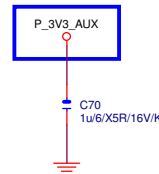
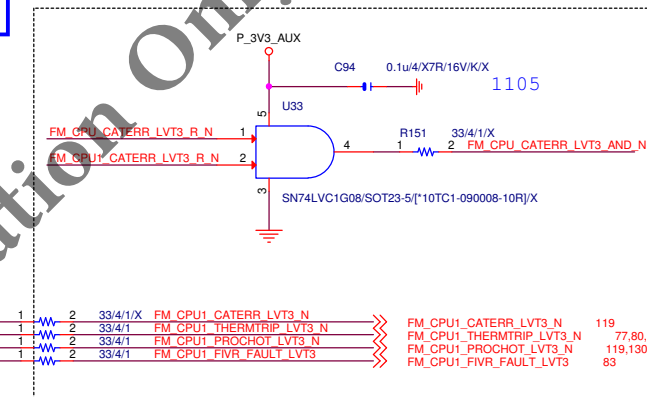
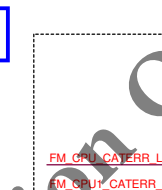
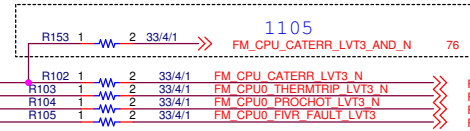
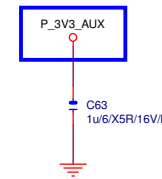
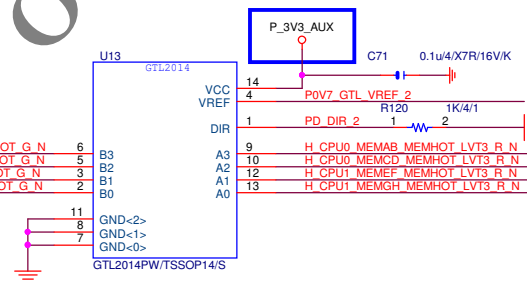
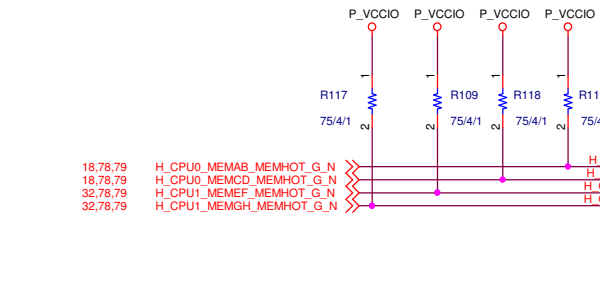
1105

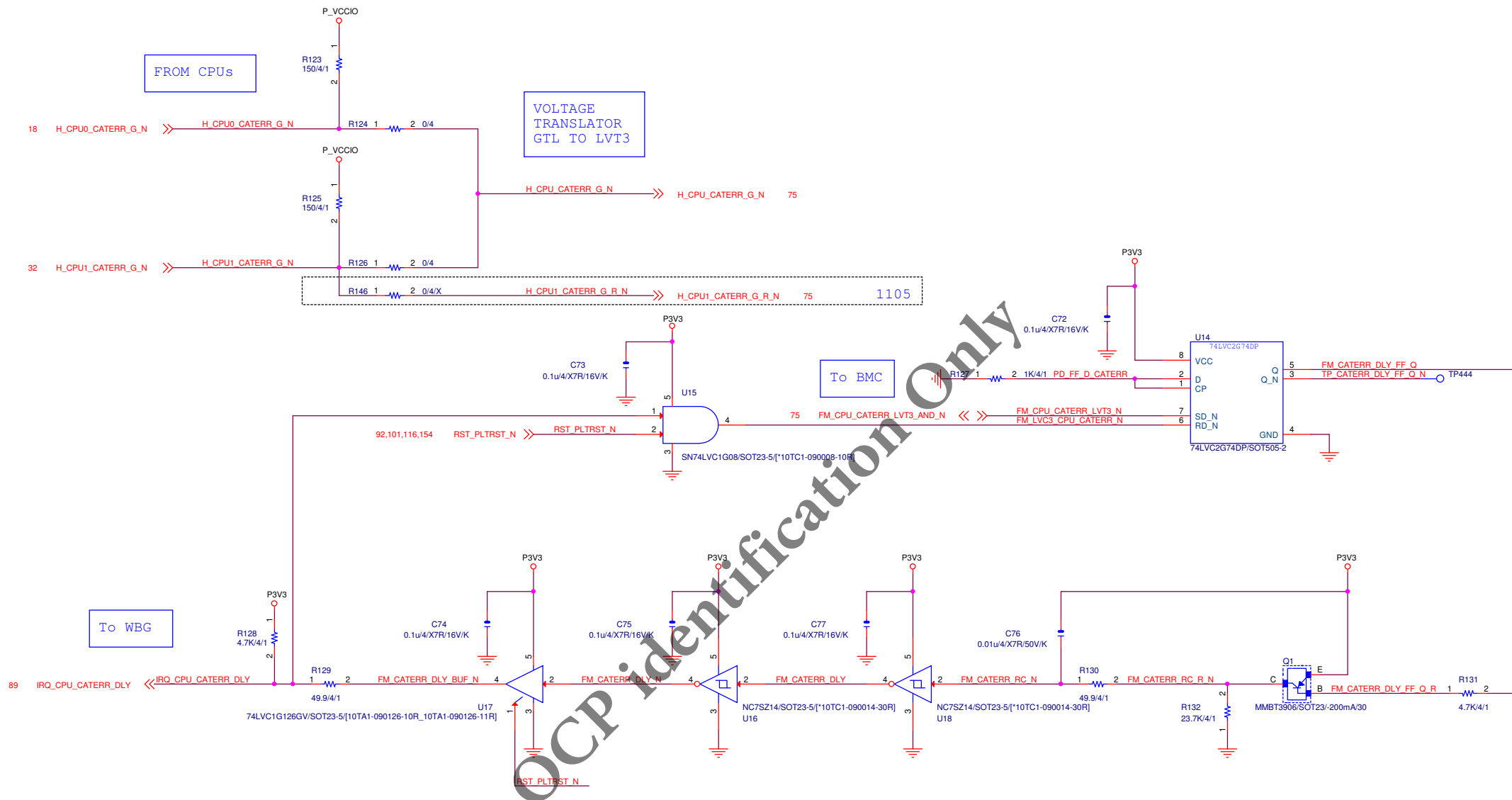


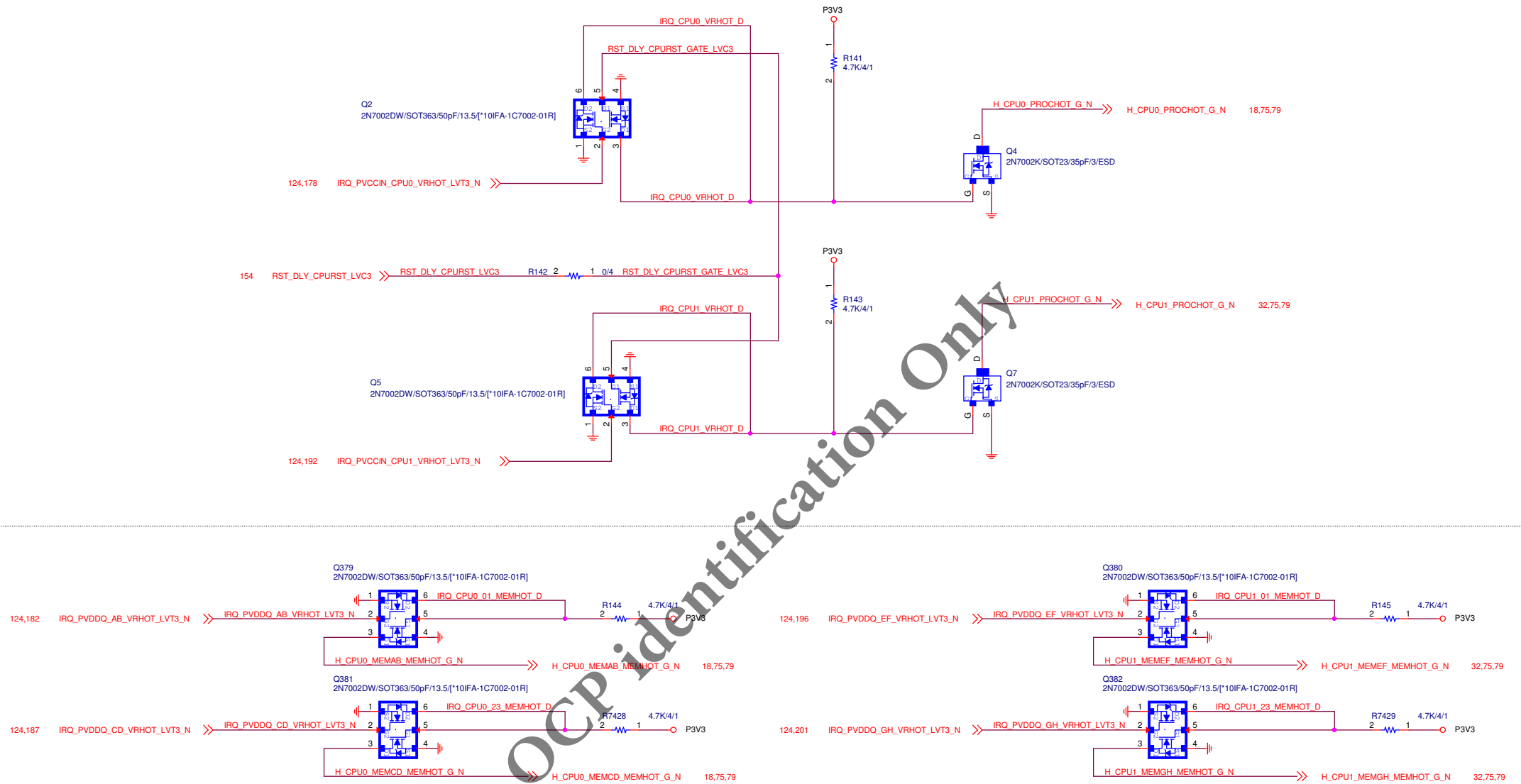
CAD NOTE:
 * PLACE CLOSE TO VOLTAGE TRANSLATOR.
 * X6S USED TO MEET THERMAL REQUIREMENT.

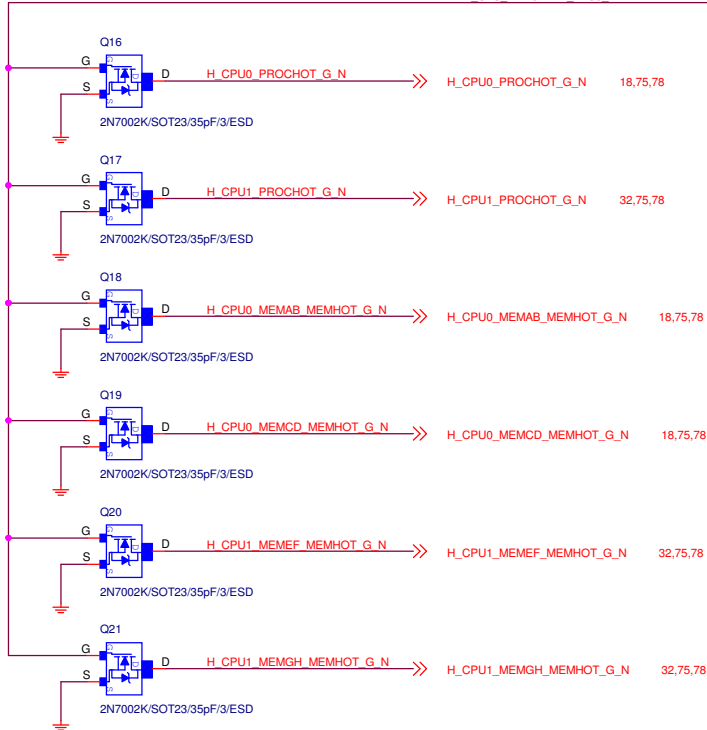
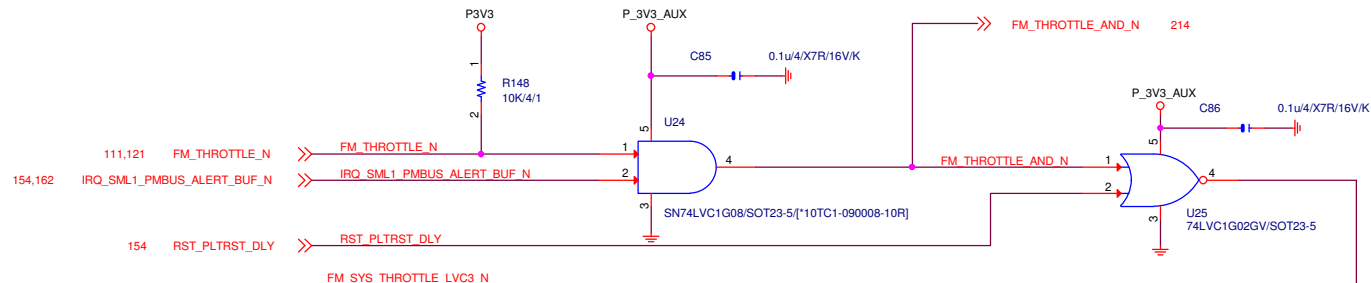


CAD NOTE:
 * PLACE CLOSE TO VOLTAGE TRANSLATOR.
 * X6S USED TO MEET THERMAL REQUIREMENT.

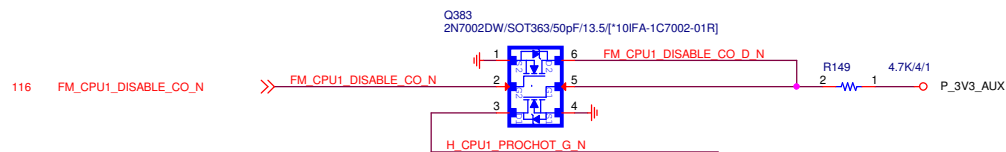


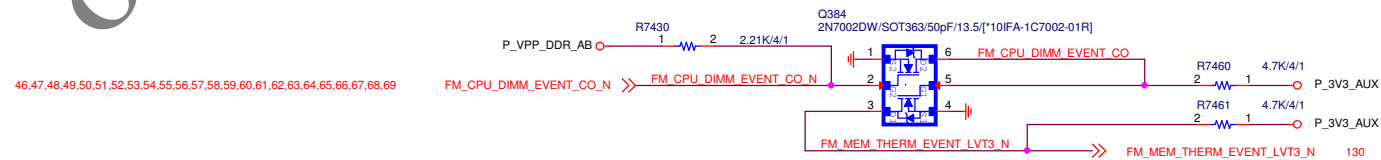
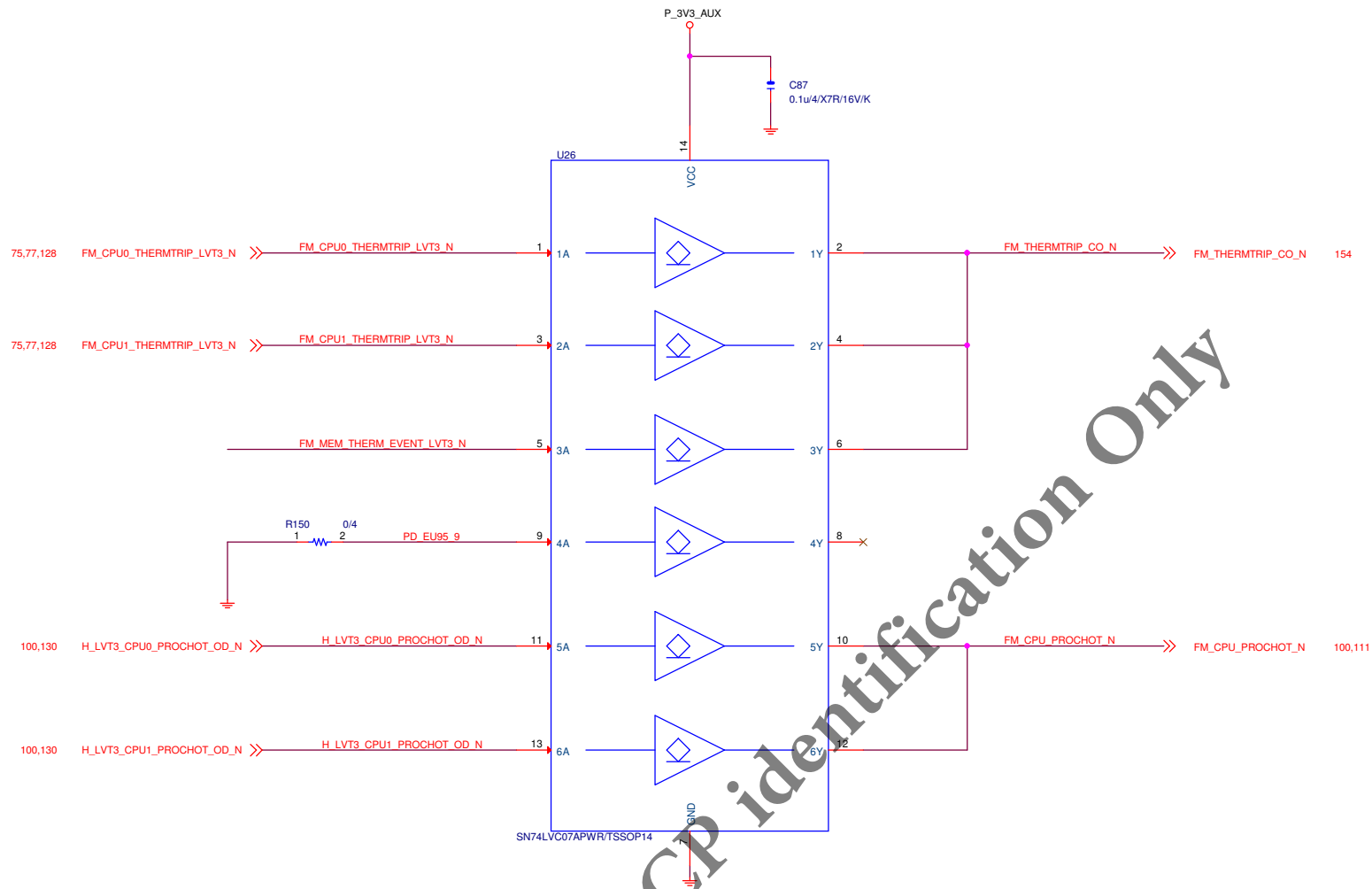


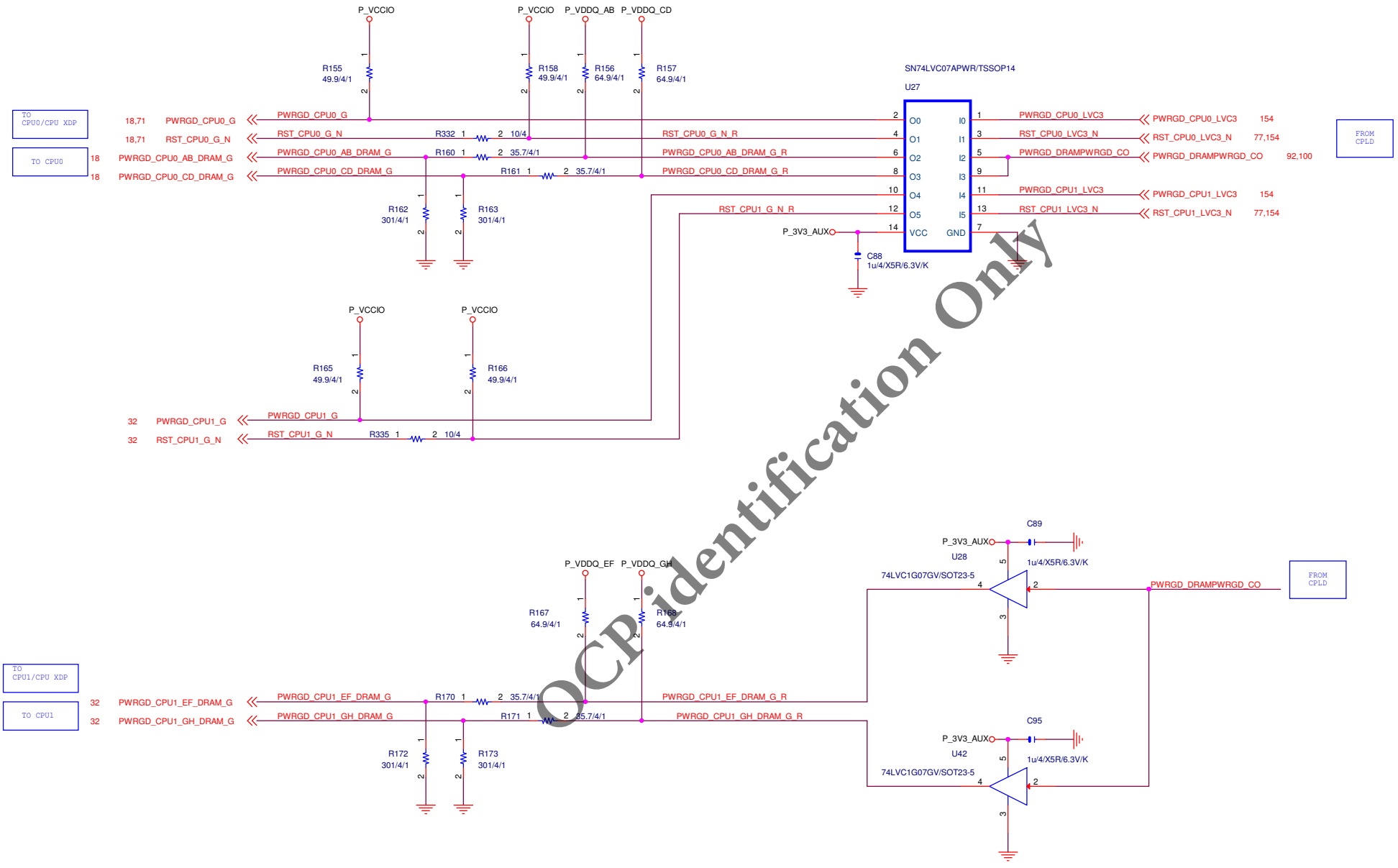




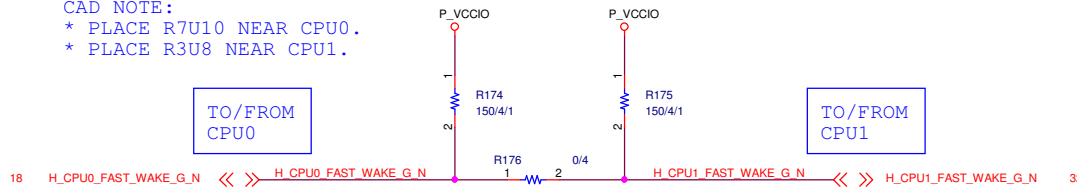
OCP identification Only







CAD NOTE:
 * PLACE R7U10 NEAR CPU0.
 * PLACE R3U8 NEAR CPU1.

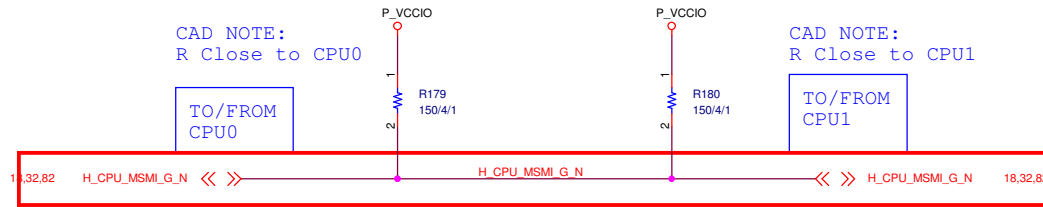


CAD NOTE:
 R Close to CPU0

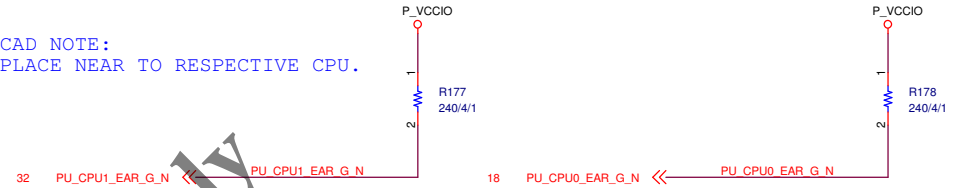
TO/FROM CPU0

CAD NOTE:
 R Close to CPU1

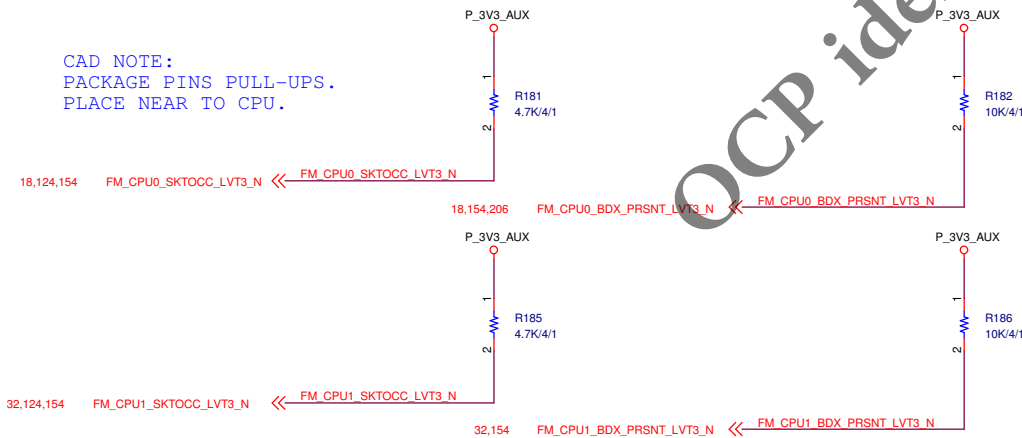
TO/FROM CPU1



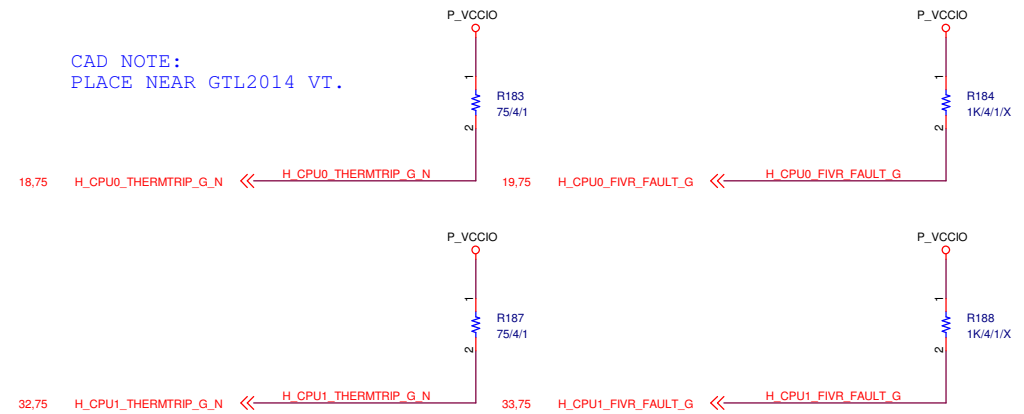
CAD NOTE:
 PLACE NEAR TO RESPECTIVE CPU.

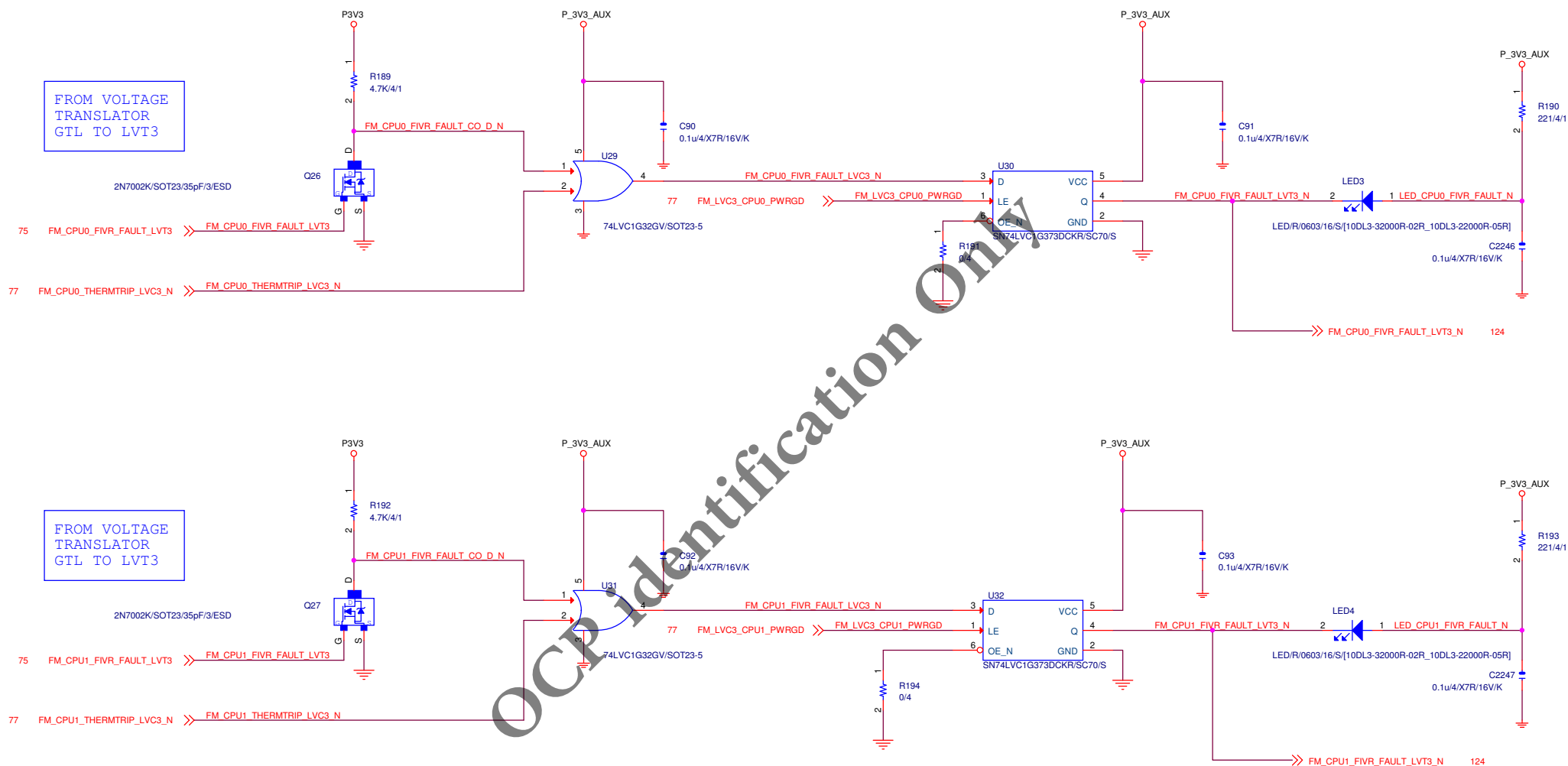


CAD NOTE:
 PACKAGE PINS PULL-UPS.
 PLACE NEAR TO CPU.

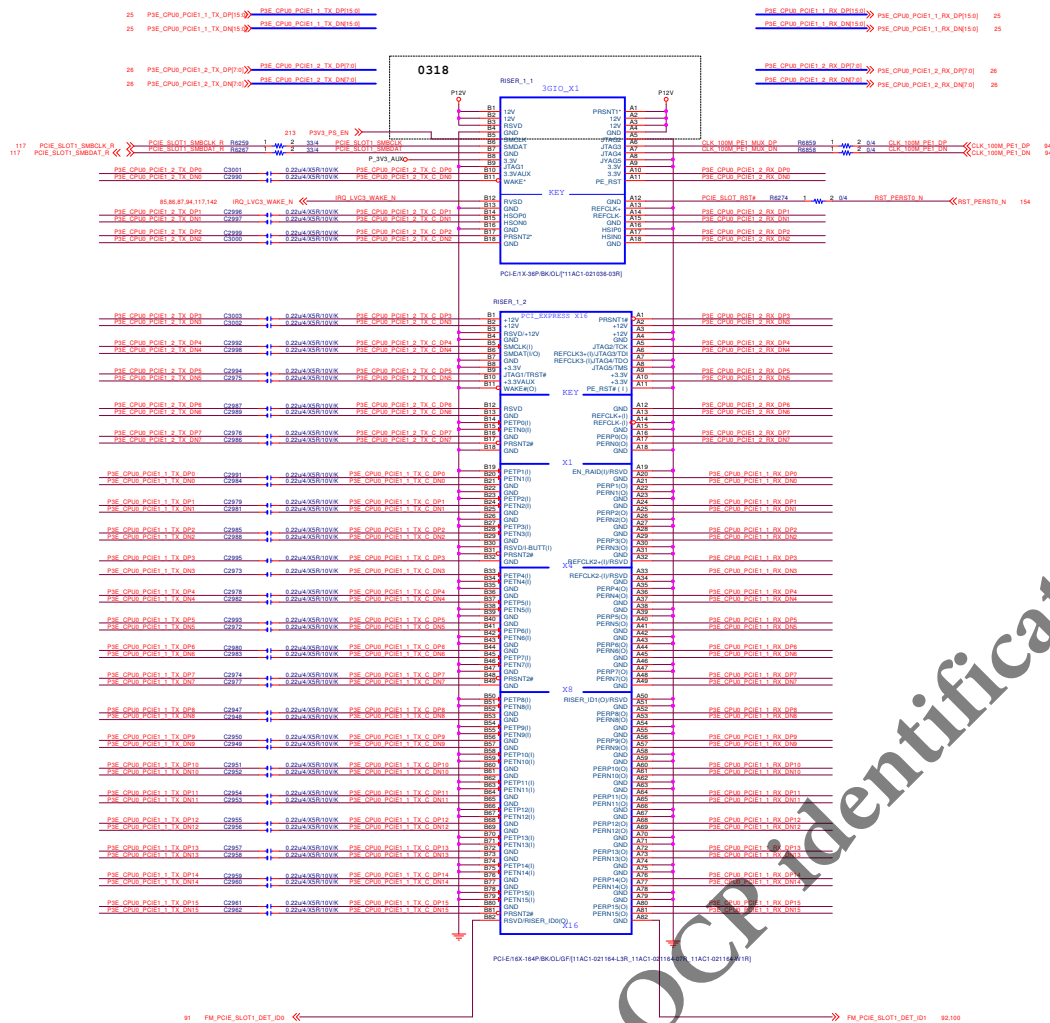


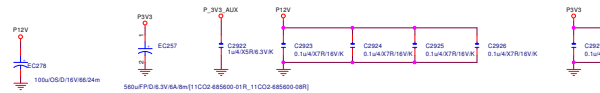
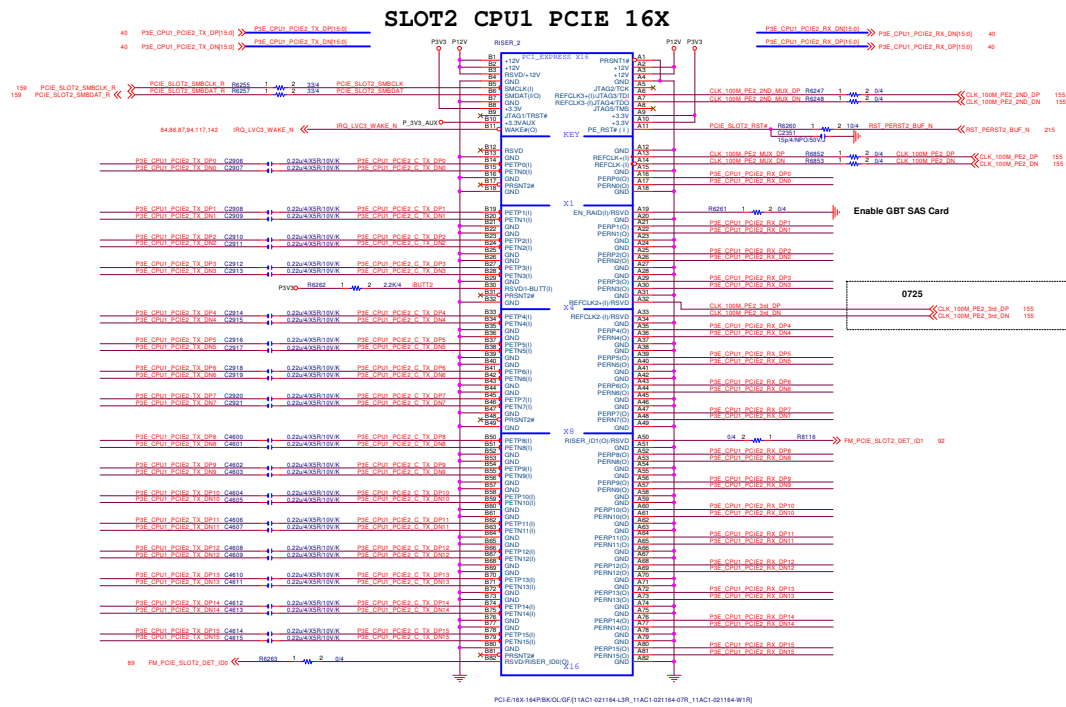
CAD NOTE:
 PLACE NEAR GTL2014 VT.



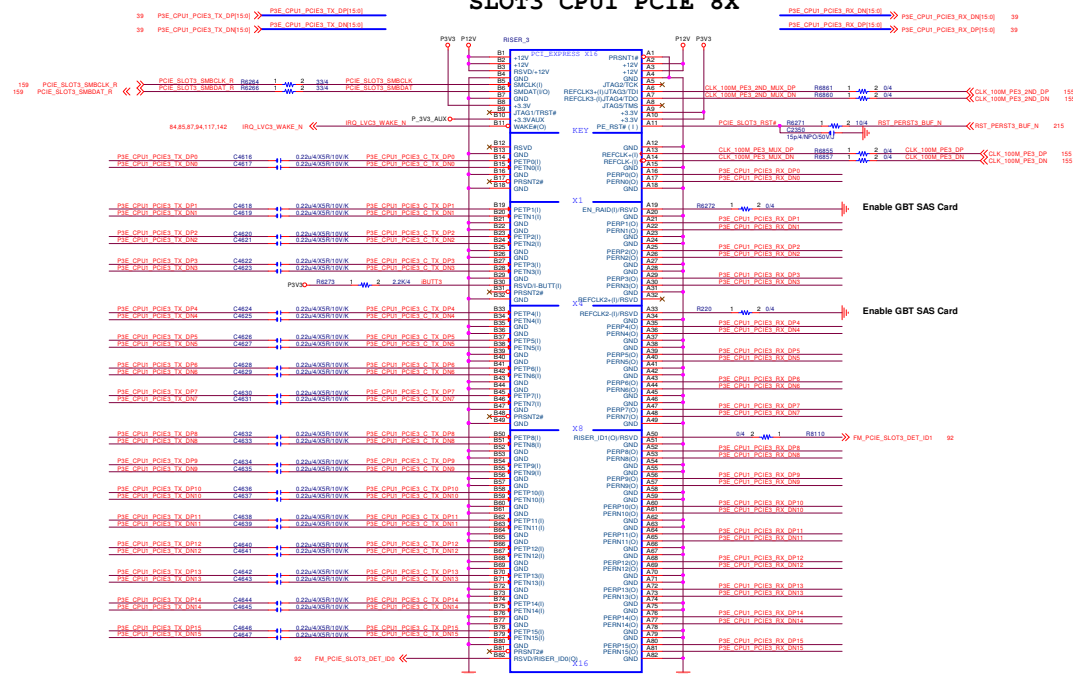


SLOT1 CPU0 PCIE 16X+8X

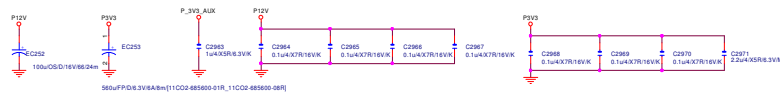




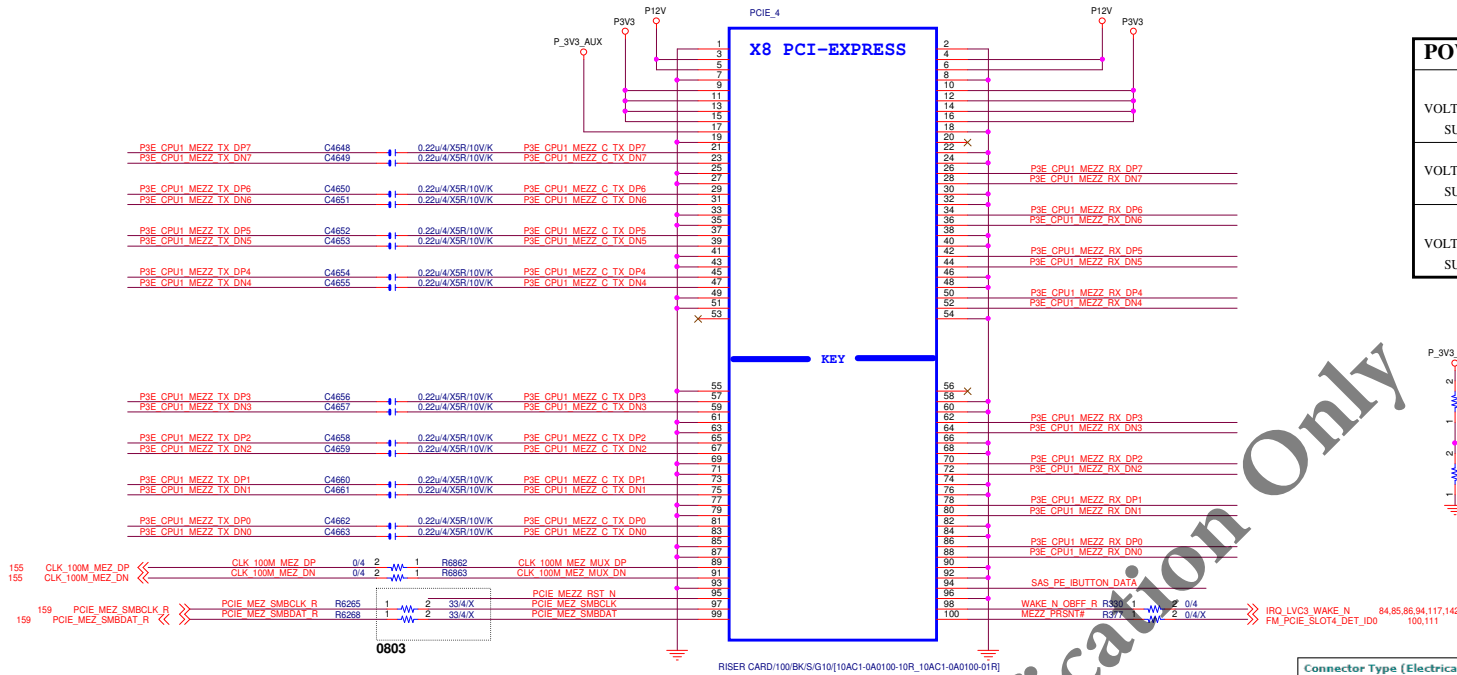
SLOT3 CPU1 PCIE 8X



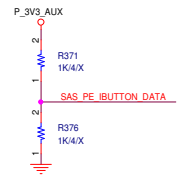
PCIE16X-16APBOLDF(1AC1-021164-L3R, 11AC1-021164-07R, 11AC1-021164-W1R)



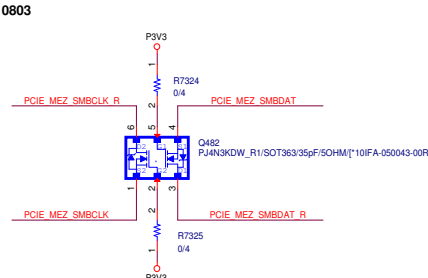
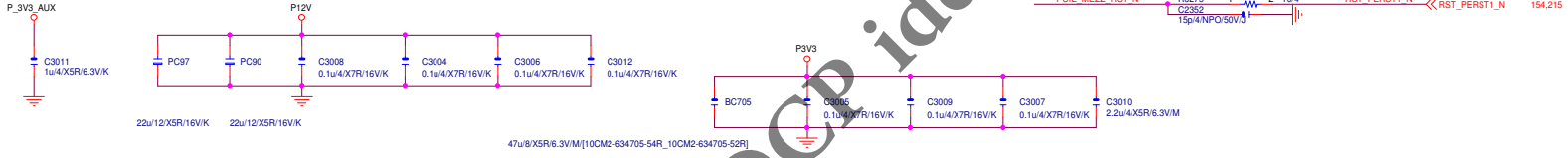
OCP identification Only



POWER RAIL	X4/X8/X16
+3.3V VOLTAGE TOLERANCE SUPPLY CURRENT	+/- 9% 3.0A (MAX)
+12V VOLTAGE TOLERANCE SUPPLY CURRENT	+/- 8% 5.5A (MAX)
+3.3VAUX VOLTAGE TOLERANCE SUPPLY CURRENT	+/- 9% 375mA (MAX)

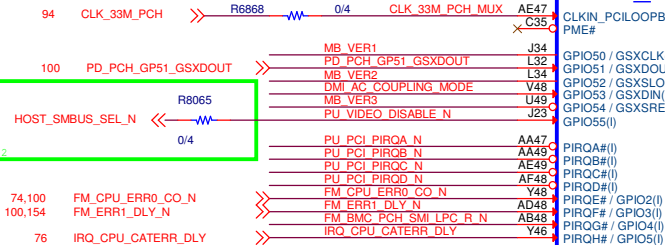
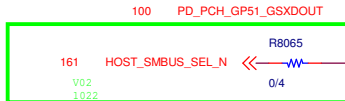
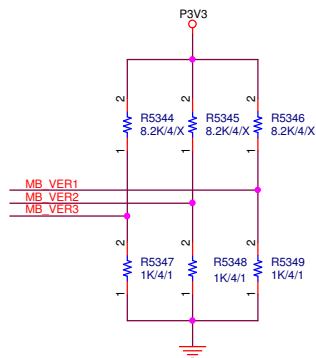


Connector Type (Electrical)	Pins That Should Use Un-plated Vias
x1	B12, B17***
X4	B12, B30, A32, A19, B17***
X8	B12, B30, A32, A33, A19, B17***, B31***, B48***
X16	B12, B30, A32, A33, A50, A19, B17***, B31***, B48***, B81***

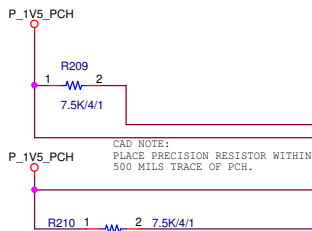


OCP identification Only

GIGABYTE™		
Title ===== PCH_Wellsburg =====		
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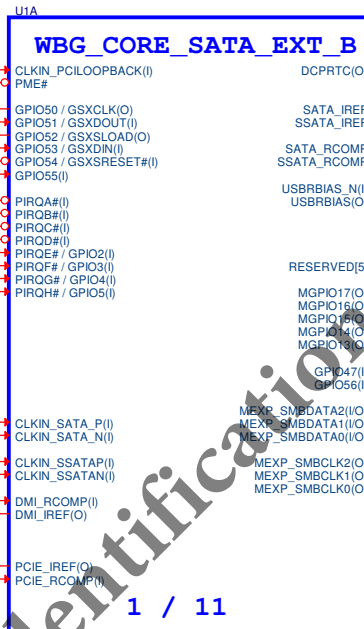


DESIGN NOTE:
Unused as Native isCLK Mode or Hybrid Mode
tied each signal to GND through a 10 KΩ
resistor.



CAD NOTE:
PLACE PRECISION RESISTOR WITHIN
500 MILS TRACE OF PCH.

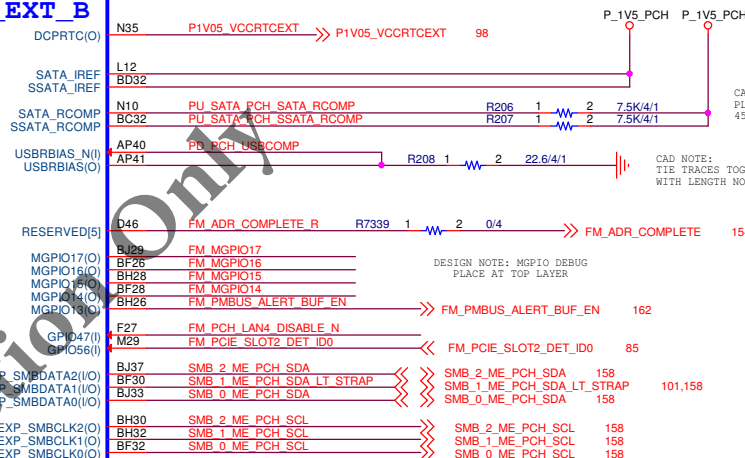
CAD NOTE:
MAX LENGTH ALLOWED FOR RCOMP/USBCOMP/TDIREF/BIASREF TRACES IS 280MILS.
TRACE WIDTH EXPECTED IS 10MILS.



1 / 11

920728 BGA0336 S110HB1-030612-00R_10HB1-030612-03R

DESIGN NOTE:
VCCRTCEXT_NCTF NEEDS TO BE SHORTED DIRECTLY TO VCCRTCEXT PIN.

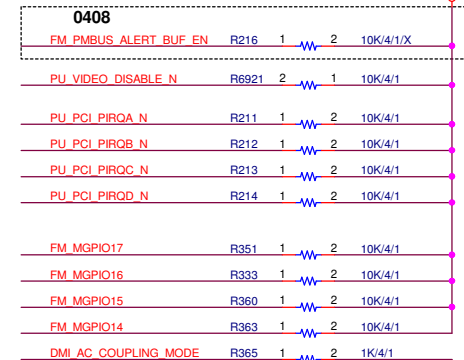


CAD NOTE:
PLACE PRECISION RESISTOR WITHIN
450 MILS TRACE OF PCH.

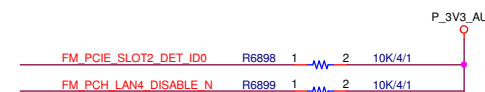
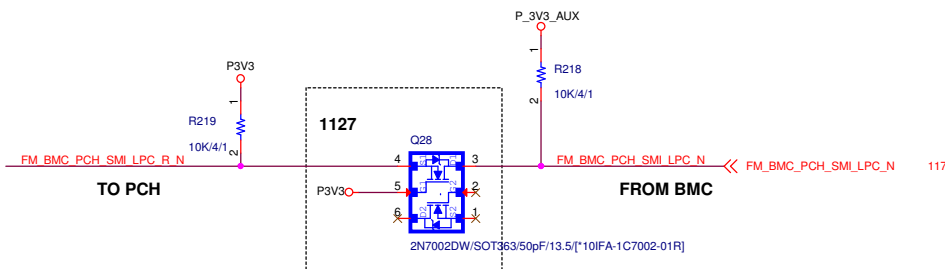
CAD NOTE:
TIE TRACES TOGETHER CLOSE TO PINS
WITH LENGTH NO LONGER THAN 1" TO RESISTOR.

DESIGN NOTE: MGPIO DEBUG
PLACE AT TOP LAYER

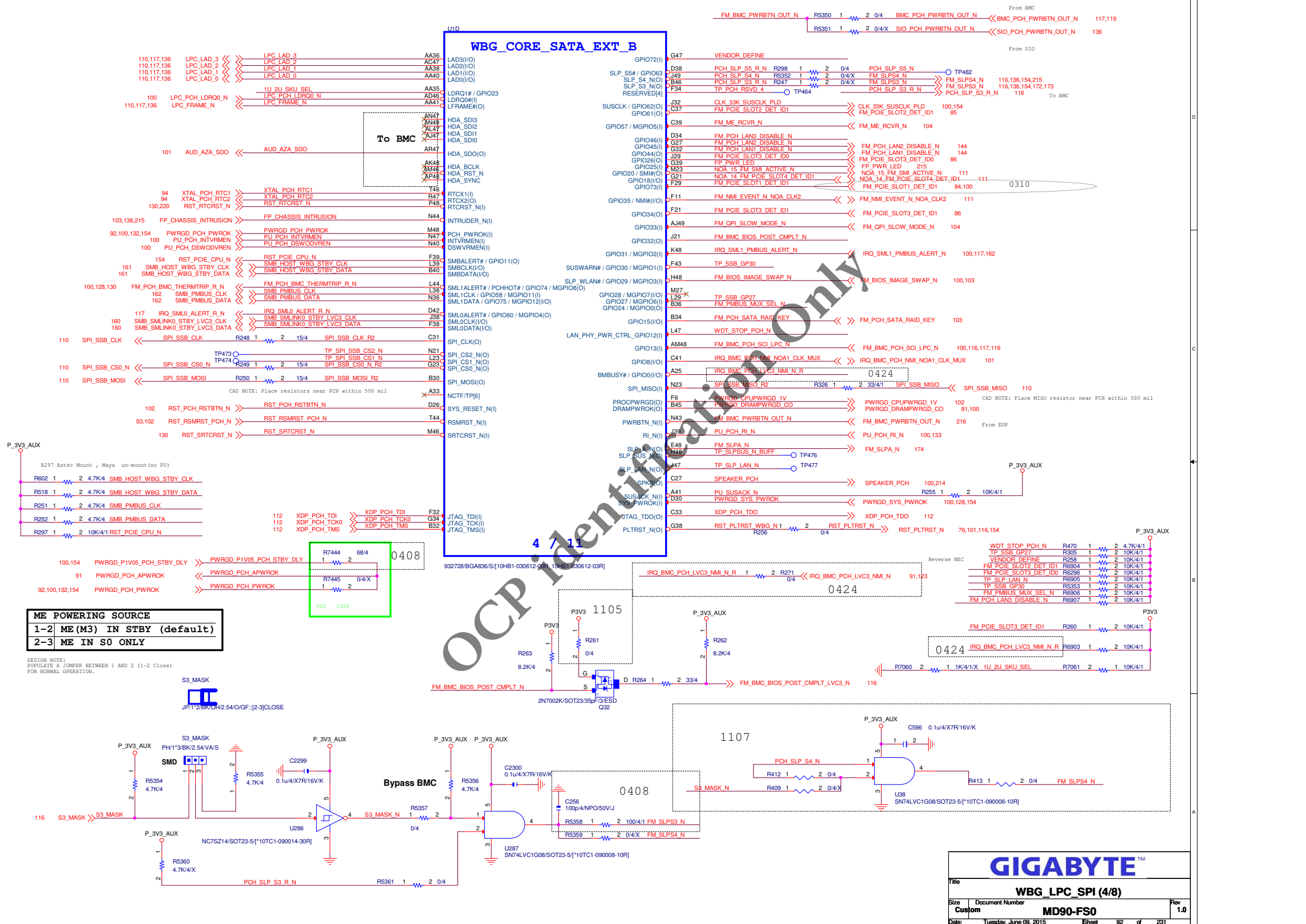
DESIGN NOTE:
MEXP_SMB DATA / CLK ; External pull-up
to P3V3 is required even if no used.



ISOLATION FORM BMC TO PCH



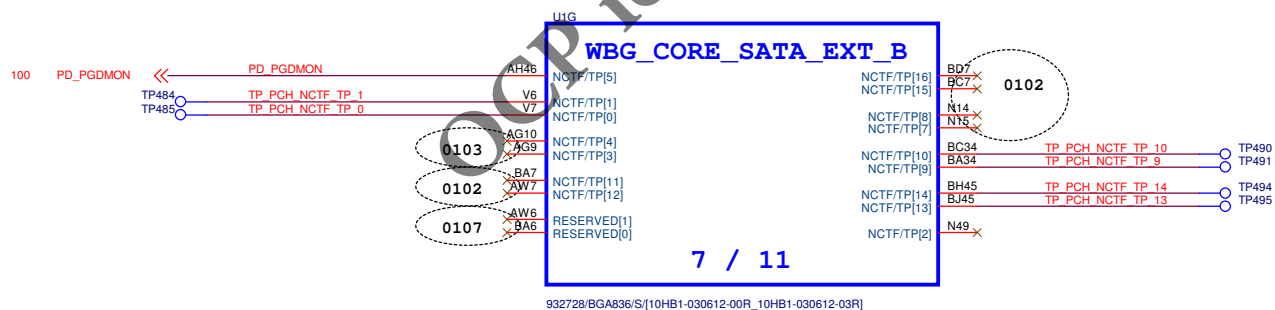
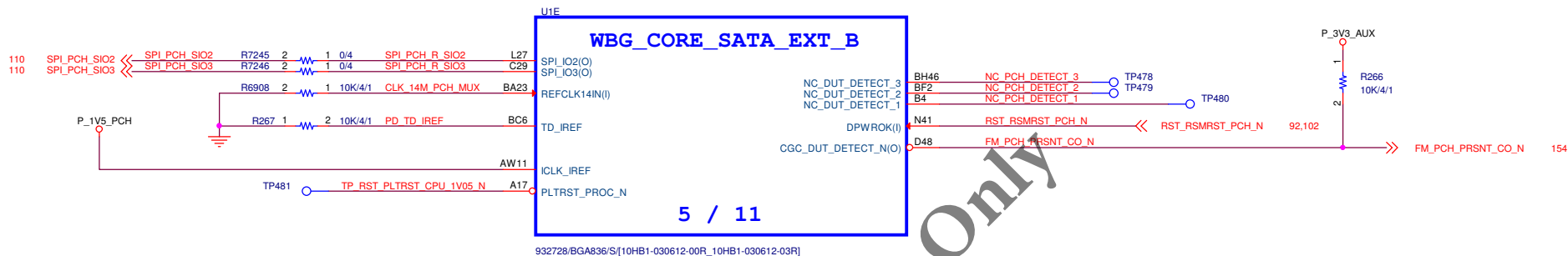
GIGABYTE™			
Title WBG_CLK_MEXP (1/8)			
Size	Document Number		Rev
Custom	MD90-FS0		1.0
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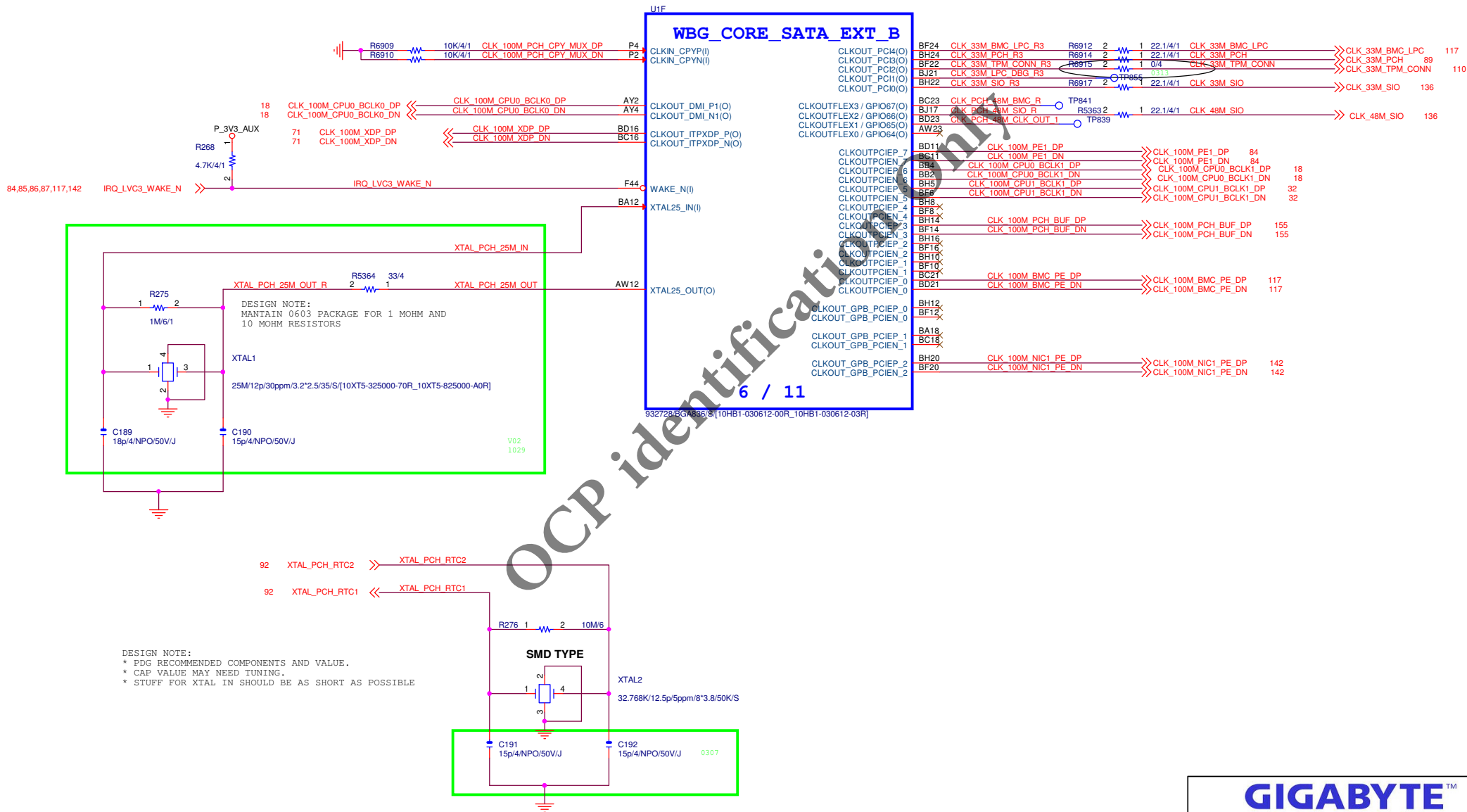


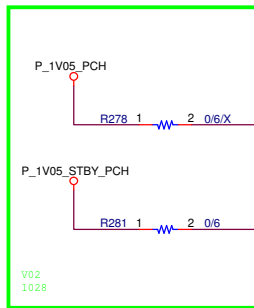
OCP Identification Only

ME POWERING SOURCE
1-2 ME (M3) IN STBY (default)
2-3 ME IN S0 ONLY

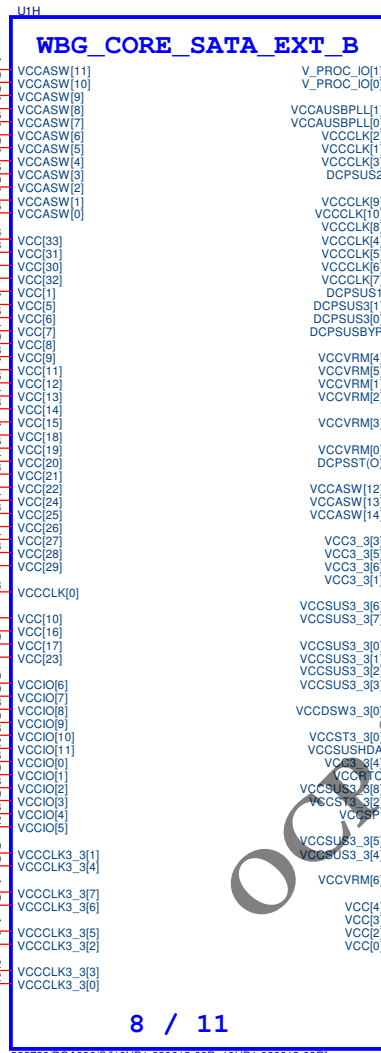
DESIGN NOTE:
POPULATE A JUMPER BETWEEN 1 AND 2 (1-2 Close)
FOR NORMAL OPERATION.







DESIGN NOTE:
1.0V OR 1.05V (NOMINAL) SUPPLY.
NOT FILTERED:
STUFF: RB / DO NOT STUFF: RA
FILTERED (DEFAULT):
STUFF: RA / DO NOT STUFF: RB

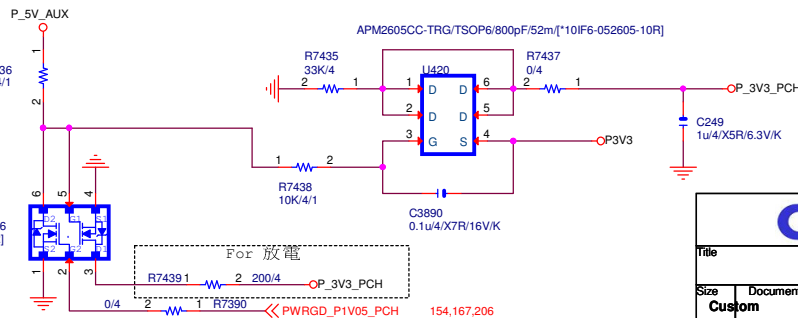


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932728/BGA836/S/[10]HB1-030612-00R_10HB1-030612-03R]

DESIGN NOTE:
<1> 1.5V WHEN USING INTERNAL VRM, NO FILTERING REQUIRED (DEFAULT)
STUFF: VRM_R1 ~ R4
DO NOT STUFF: VRM BYPASS_R1 ~ R4
<2> 1.05 FOR VRM BYPASS MODE
STUFF: VRM BYPASS_R1 ~ R4
DO NOT STUFF: VRM_R1 ~ R4

2N7002DW/SOT363/50pF/13.5/[*10]FA-1C7002-01R]



GIGABYTE™		
Title: WBG_VCC (7/8)		
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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U1I

WBG_CORE_SATA_EXT_B

A11	VSS[239]	P6
A15	VSS[238]	P9
A19	VSS[237]	P12
A23	VSS[236]	P15
A27	VSS[235]	P38
A29	VSS[234]	P41
A31	VSS[233]	P44
A35	VSS[232]	P46
A39	VSS[231]	R1
A43	VSS[230]	R3
B22	VSS[229]	R49
C7	VSS[228]	T10
C9	VSS[227]	T6
C11	VSS[226]	T48
C13	VSS[225]	U1
C15	VSS[224]	U3
C17	VSS[223]	U47
C19	VSS[222]	V14
C21	VSS[221]	V46
C23	VSS[220]	W1
D22	VSS[219]	W3
D24	VSS[218]	W18
D28	VSS[217]	W19
D32	VSS[216]	W23
D36	VSS[215]	W24
D40	VSS[214]	W26
D44	VSS[213]	W27
F9	VSS[212]	W31
F14	VSS[211]	W32
F16	VSS[210]	W47
F20	VSS[209]	W49
F23	VSS[208]	Y6
F25	VSS[207]	Y12
F36	VSS[206]	Y15
F41	VSS[205]	Y38
F46	VSS[204]	Y41
G3	VSS[203]	Y44
G16	VSS[202]	Y44
G49	VSS[201]	AA1
J1	VSS[200]	AA3
J3	VSS[199]	AA10
J9	VSS[198]	AA43
J14	VSS[197]	AA44
J20	VSS[196]	AB46
J30	VSS[195]	AC3
J36	VSS[194]	AC6
J41	VSS[193]	AC10
K46	VSS[192]	AC49
L1	VSS[191]	AD18
L7	VSS[190]	AD19
L3	VSS[189]	AD21
L49	VSS[188]	AD23
M20	VSS[187]	AD24
M25	VSS[186]	AD26
M30	VSS[185]	AD27
M32	VSS[184]	AD29
N1	VSS[183]	AD31
N3	VSS[182]	AD32
N32	VSS[181]	AE1
	VSS[180]	

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932728/BGA836/S/[10HB1-030612-00R_10HB1-030612-03R]

U1J

WBG_CORE_SATA_EXT_B

AE3	VSS[179]	AP35
AE6	VSS[178]	AP38
AE9	VSS[177]	AP46
AE12	VSS[176]	AR1
AE15	VSS[175]	AR3
AE35	VSS[174]	AR49
AE38	VSS[173]	AT6
AE41	VSS[172]	AT9
AE44	VSS[171]	AT12
AP46	VSS[170]	AT15
AG1	VSS[169]	AT35
AG3	VSS[168]	AT38
AG47	VSS[167]	AT41
AG49	VSS[166]	AT44
AH48	VSS[165]	AT49
AJ1	VSS[164]	BD30
AJ3	VSS[163]	BD34
AJ6	VSS[162]	BD36
AJ7	VSS[161]	BD39
AJ9	VSS[160]	BD41
AJ10	VSS[159]	BD44
AJ12	VSS[158]	BF18
AJ14	VSS[157]	BF4
AJ19	VSS[156]	BF44
AJ21	VSS[155]	BF46
AJ23	VSS[154]	BF48
AJ24	VSS[153]	BG7
AJ26	VSS[152]	BG9
AJ27	VSS[151]	BG11
AJ31	VSS[150]	BG13
AJ38	VSS[149]	BG15
AK6	VSS[148]	BG17
AK9	VSS[147]	BG19
AK12	VSS[146]	BG21
AK15	VSS[145]	BG23
AK35	VSS[144]	BG25
AK38	VSS[143]	BG27
AK41	VSS[142]	BG29
AK44	VSS[141]	BG31
AK46	VSS[140]	BG33
AL1	VSS[139]	BG35
AL3	VSS[138]	BG37
AL48	VSS[137]	BG39
AM9	VSS[136]	BG41
AM14	VSS[135]	BG43
AM15	VSS[134]	BH4
AM18	VSS[133]	BH18
AM19	VSS[132]	BJ7
AM21	VSS[131]	BJ9
AM22	VSS[130]	BJ11
AM29	VSS[129]	BJ13
AM31	VSS[128]	BJ15
AM32	VSS[127]	BJ19
AM38	VSS[126]	BJ23
AN1	VSS[125]	BJ25
AN3	VSS[124]	BJ31
AP6	VSS[123]	BJ35
AP10	VSS[122]	BJ39
AP15	VSS[121]	BJ41
AP31	VSS[120]	BJ43
		VSS[60]

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932728/BGA836/S/[10HB1-030612-00R_10HB1-030612-03R]

U1K

WBG_CORE_SATA_EXT_B

BC12	VSS[59]	VSS[301]	A4
BC27	VSS[58]	VSS[302]	A5
BC3	VSS[57]	VSS[303]	A7
BC39	VSS[56]	VSS[304]	A45
BC44	VSS[55]	VSS[305]	A46
BC47	VSS[54]	VSS[306]	A48
BC49	VSS[53]	VSS[307]	B2
BD6	VSS[52]	VSS[308]	B48
BD9	VSS[51]	VSS[309]	B49
BD12	VSS[50]	VSS[310]	D1
BD14	VSS[49]	VSS[311]	D2
BD18	VSS[48]	VSS[312]	D49
BD20	VSS[47]	VSS[313]	E1
BD25	VSS[46]	VSS[314]	E49
BD27	VSS[45]	VSS[315]	G1
BD30	VSS[44]	VSS[316]	BE1
BD34	VSS[43]	VSS[317]	BE49
BD36	VSS[42]	VSS[318]	BF1
BD39	VSS[41]	VSS[319]	BF49
BD41	VSS[40]	VSS[320]	BH1
BD44	VSS[39]	VSS[321]	BH2
BF18	VSS[38]	VSS[322]	BH48
BF4	VSS[37]	VSS[323]	BH49
BF44	VSS[36]	VSS[324]	BJ2
BF46	VSS[35]	VSS[325]	BJ4
BF48	VSS[34]	VSS[326]	BJ5
BG7	VSS[33]	VSS[327]	BJ48
BG9	VSS[32]	VSS[328]	BJ48
BG11	VSS[31]	VSS[329]	
BG13	VSS[30]		
BG15	VSS[29]		
BG17	VSS[28]		
BG19	VSS[27]		
BG21	VSS[26]		
BG23	VSS[25]		
BG25	VSS[24]		
BG27	VSS[23]		
BG29	VSS[22]		
BG31	VSS[21]		
BG33	VSS[20]		
BG35	VSS[19]		
BG37	VSS[18]		
BG39	VSS[17]		
BG41	VSS[16]		
BG43	VSS[15]		
BH4	VSS[14]		
BH18	VSS[13]		
BJ7	VSS[12]		
BJ9	VSS[11]		
BJ11	VSS[10]		
BJ13	VSS[9]		
BJ15	VSS[8]		
BJ19	VSS[7]		
BJ23	VSS[6]		
BJ25	VSS[5]		
BJ31	VSS[4]		
BJ35	VSS[3]		
BJ39	VSS[2]		
BJ41	VSS[1]		
BJ43	VSS[0]		
		VSS[300]	AU47

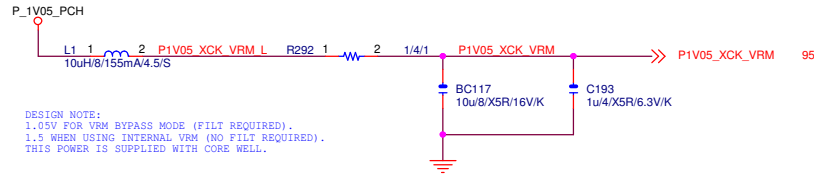
11 / 11

932728/BGA836/S/[10HB1-030612-00R_10HB1-030612-03R]

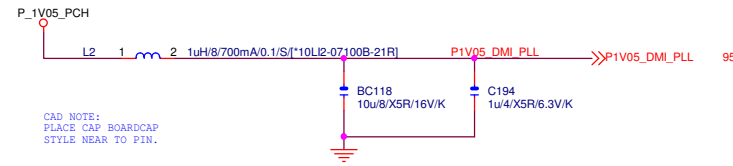
GIGABYTE™

Title				
WBG_GND (8/8)				
Size	Document Number			Rev
Custom	MD90-FS0			1.0
Date:	Tuesday, June 09, 2015	Sheet	96 of	231

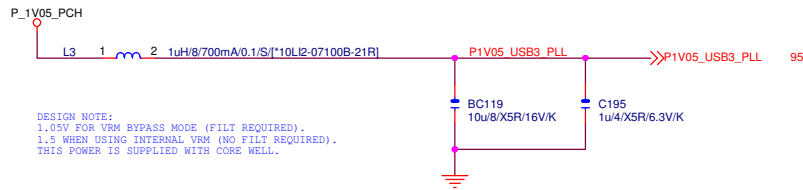
P1V05_XCK_VRM - CLOCK INTEGRATION



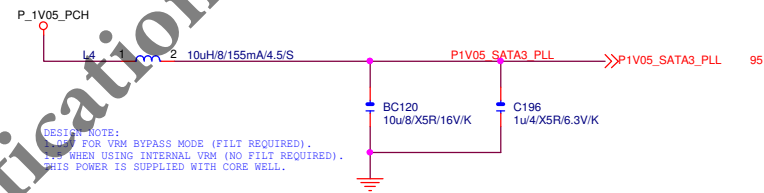
DMI PLL FILTER 1.05V PCIE/DMI SECTION



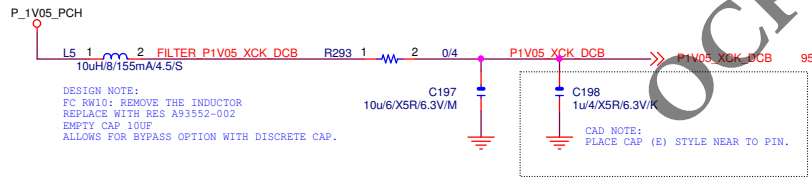
USB3 PLL FILTER



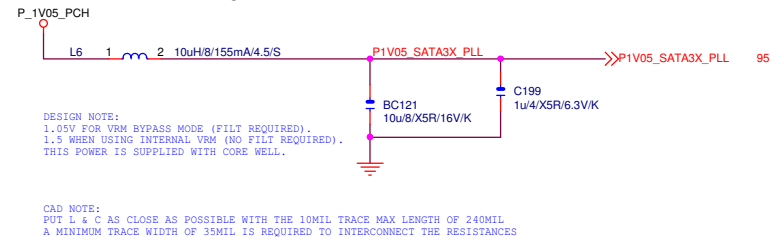
SATA PLL FILTER



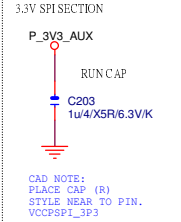
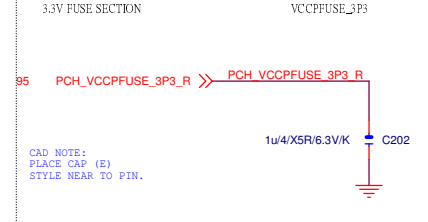
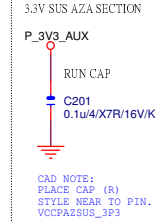
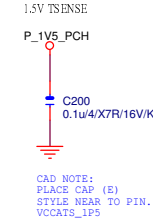
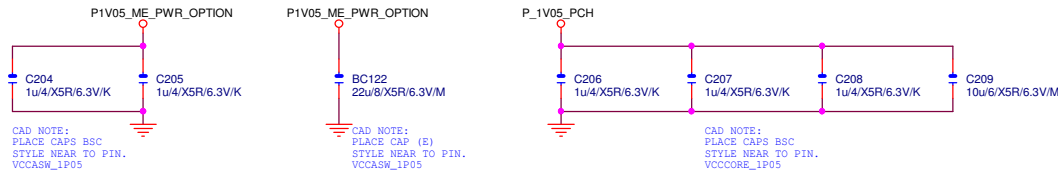
P1V05_XCK_DCB - CLOCK INTEGRATION



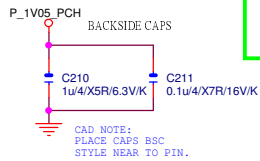
SATA3X PLL FILTER



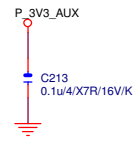
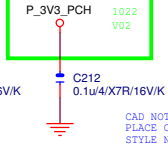
1.05V CORE/ASW/SUS FOR CORE SECTION



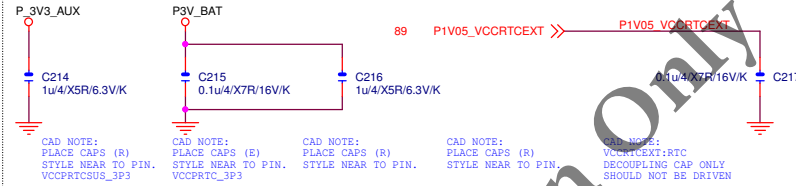
1.05V CORE USB2 SECTION



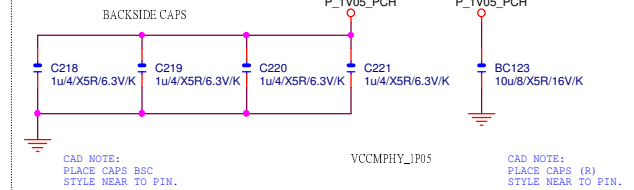
3.3V CORE/SUS USB2 SECTION



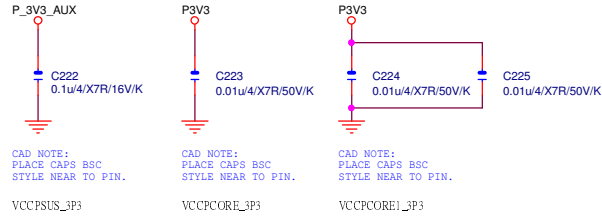
3.3V DSW/RTC FOR RTC SECTION



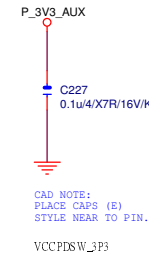
1.05V PCIE/DMI/SATA SECTION



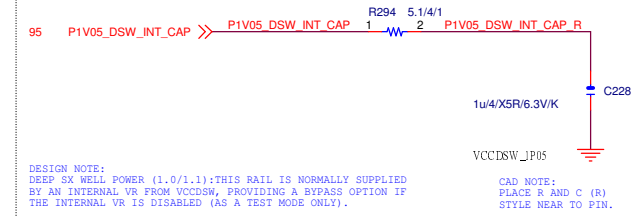
3.3V SUS/DSW/CORE FOR GPIO/LPC SECTION



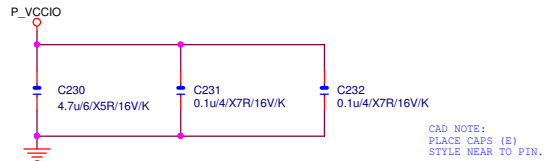
GPIO/LPC SECTION



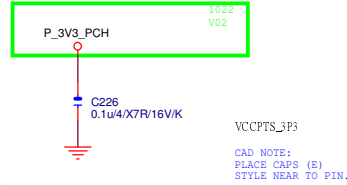
GPIO/LPC SECTION



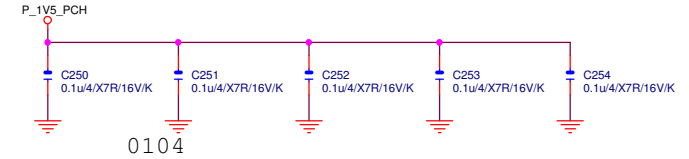
VCCIO2PCH FOR CPU SECTION



3.3V CORE THERMAL SENSOR

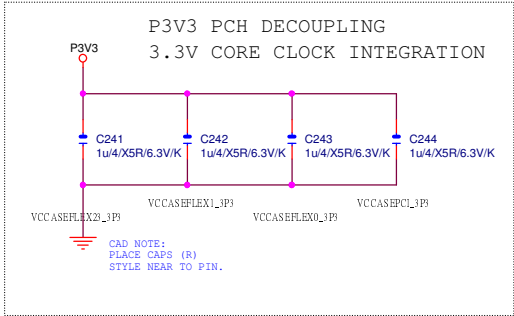
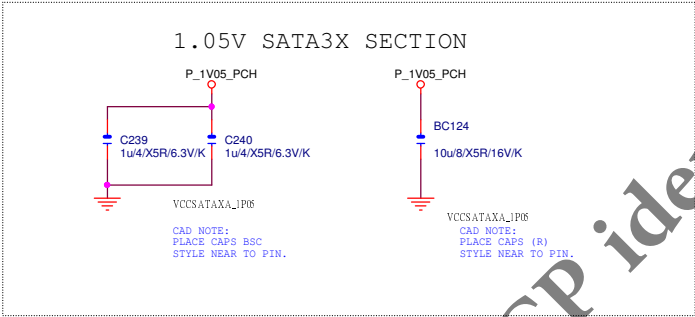
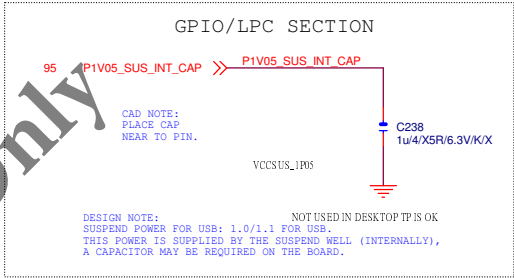
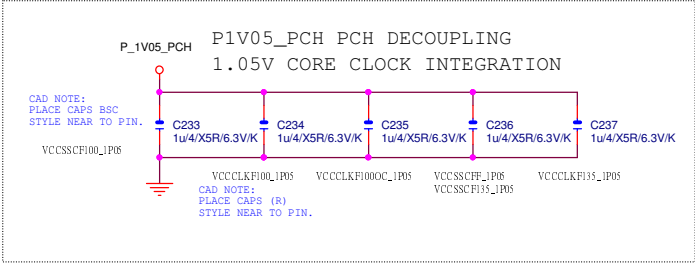


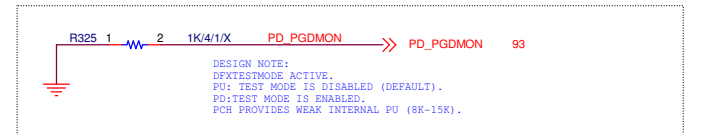
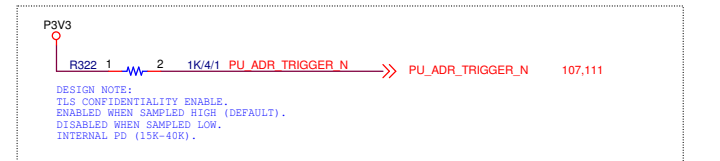
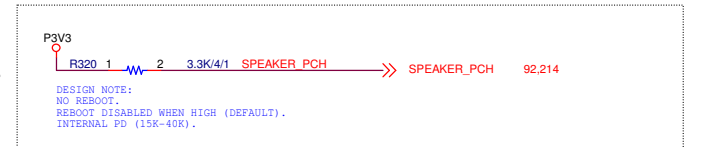
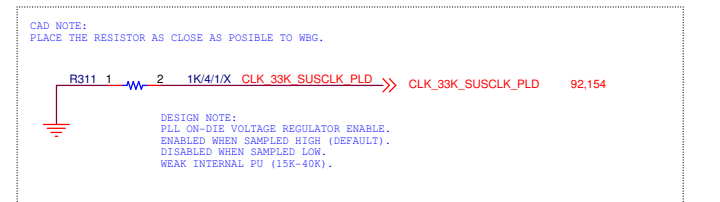
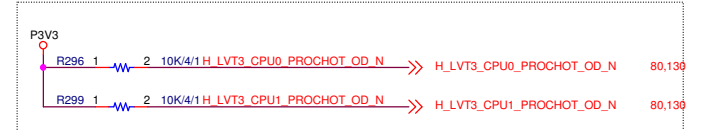
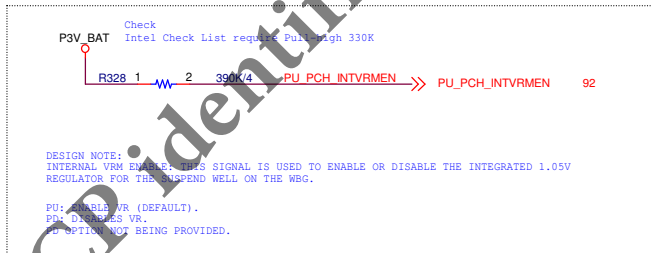
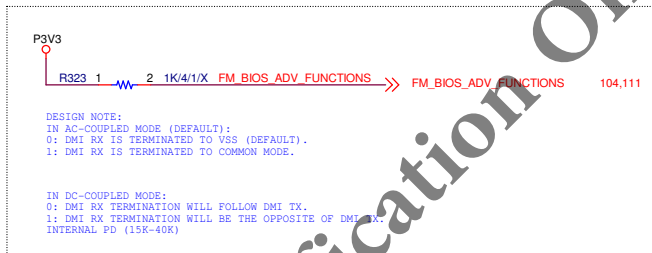
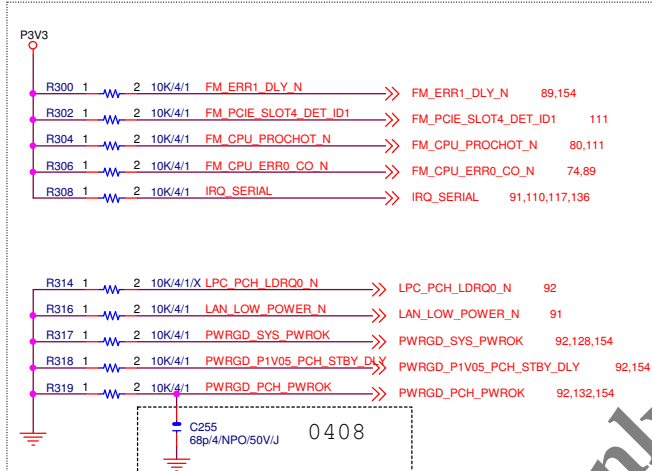
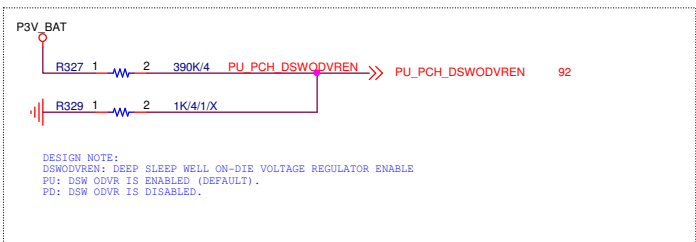
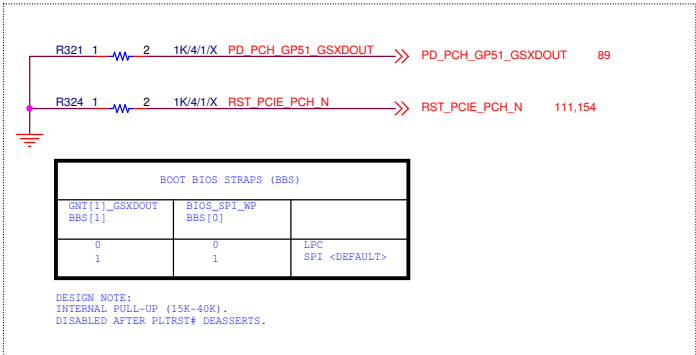
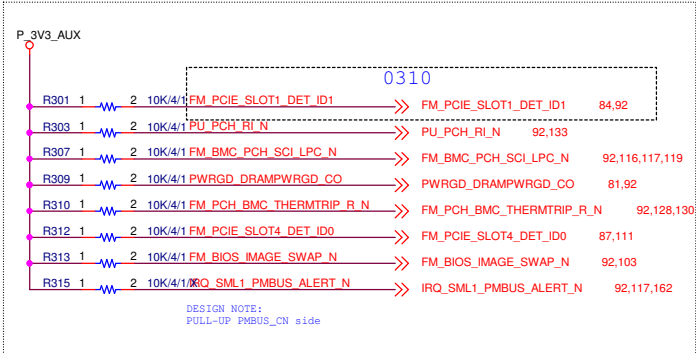
CAD NOTE:
BSC: BACK SIDE COMPONENT
E: EDGE
R: RUN

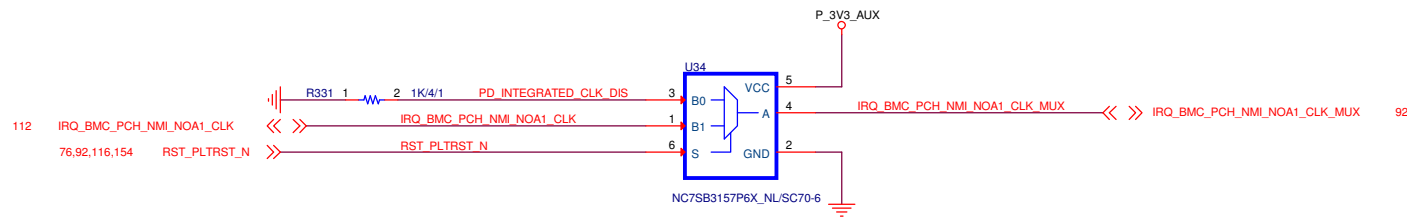


GIGABYTE™

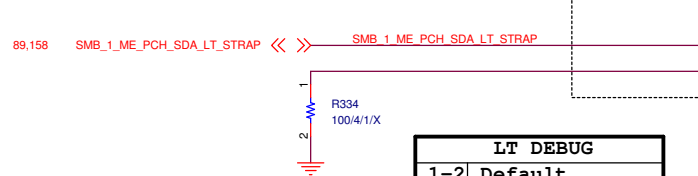
Title	WBG DECOUPLING (1/2)		
Size	Document Number	Rev	1.0
Custom	MD90-FS0		
Date:	Tuesday, June 09, 2015	Sheet	98 of 231





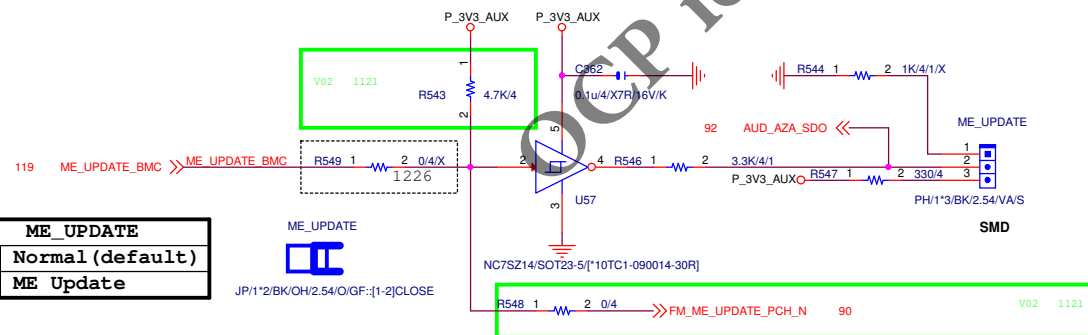


DESIGN NOTE:
 INTEGRATED CLOCK CHIP DISABLE.
 INTERNAL PULL-UP (15K-40K).
 ENABLED WHEN SAMPLED LOW.
 INTERATED CLOCK CHIP ENABLED FOR PPO AND PO.



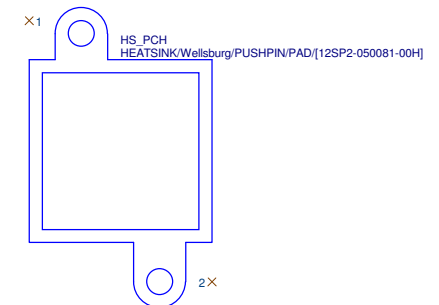
LT DEBUG	
1-2	Default
2-3	DEBUG MODE

DESIGN NOTE:
 LT KEY DOWNGRADE.
 P/U (1-2): LT DEBUG MODE IS DISABLED WHEN PULLED HIGH (DEFAULT).
 P/D (2-3): LT DEBUG MODE IS ENABLED WHEN PULLED LOW.
 THIS PIN IS SHARED WITH MEXP_BMBDATA1. IF THIS FEATURE NEEDS TO BE ENABLED.
 PLEASE SET THE JUMPER TO 2-3 BEFORE PLTRST# AND THEN RETURN TO 1-2 FOR SMBUS FUNCTIONALITY.

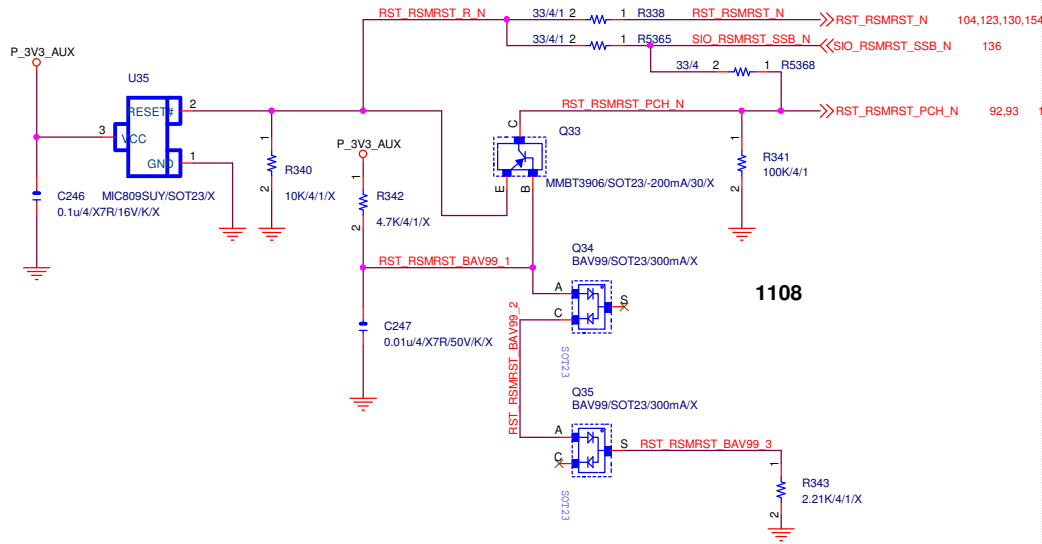


ME_UPDATE	
1-2	Normal (default)
2-3	ME Update

DESIGN NOTE:
 FLASH DESCRIPTOR SECURITY OVERRIDE.
 * FLASH DESCRIPTOR SECURITY OVERRIDE WHEN HIGH SET JUMPER.
 * FLASH DESCRIPTOR SECURITY NO OVERRIDE WHEN LOW (DEFAULT, NO JUMPER).
 INTERNAL PD (9K-50K). MANUFACTURING JUMPER ALSO CAN BE USED TO SET THIS STRAP.



RTC Power-WELL ISOLATION

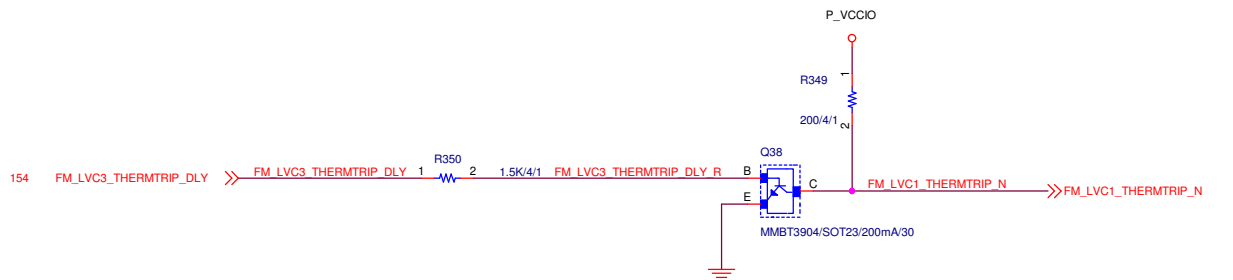
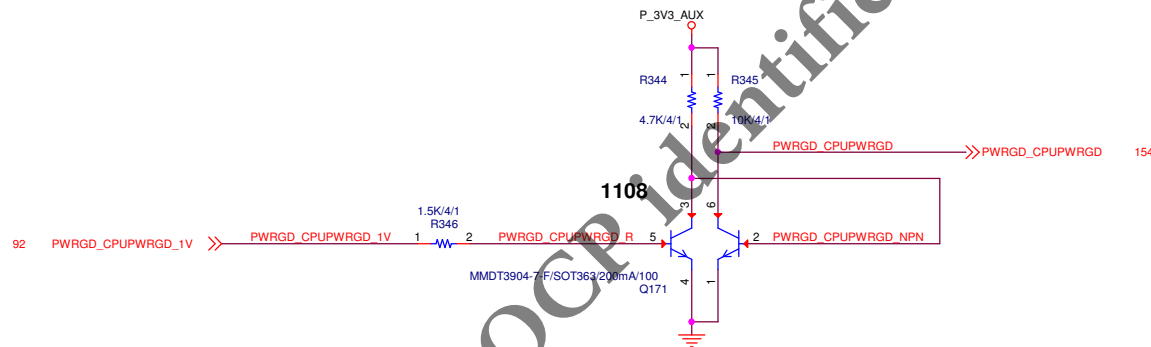
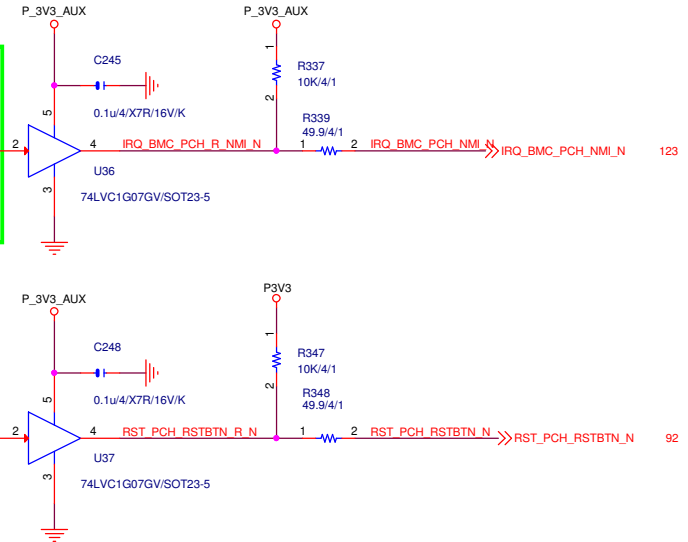


From BMC Passthrough

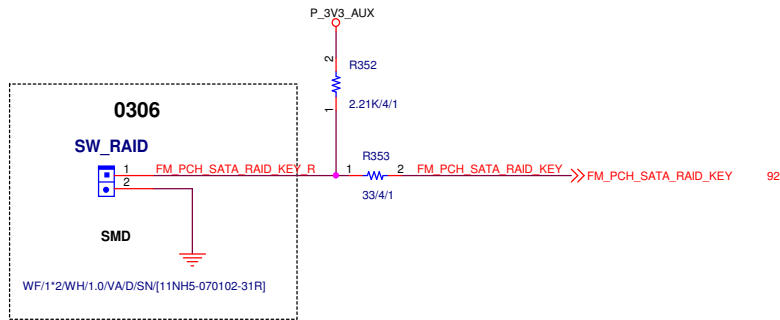
Bypass BMC

From BMC Passthrough

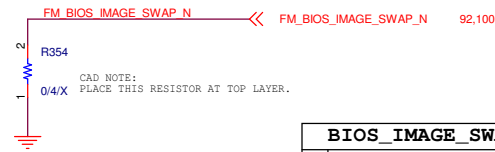
Bypass BMC



SATA RAID KEY

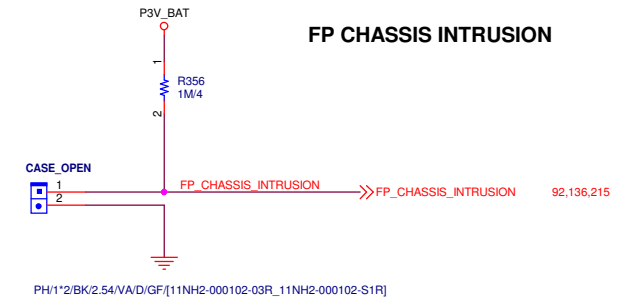


BIOS IMAGE SWAP JUMPER



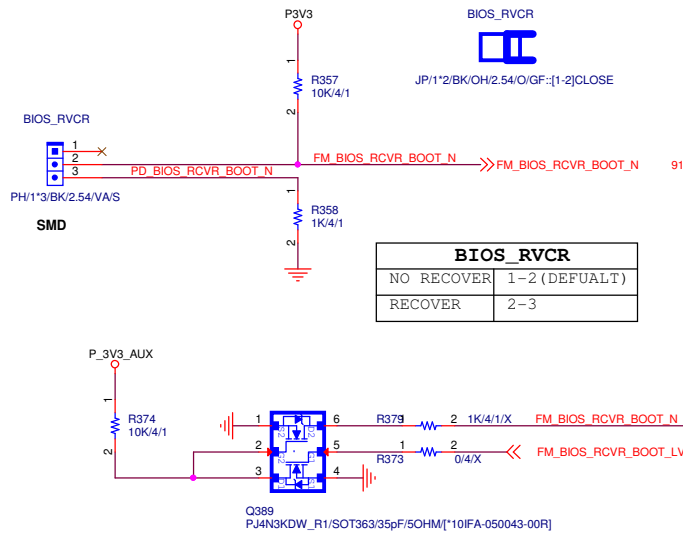
BIOS_IMAGE_SWAP	
H	(DEFAULT)
L	IMAGE SWAP

FP CHASSIS INTRUSION



FP CHASSIS INTRUSION	
CHASSIS CLOSE	1-2 CLOSED
CHASSIS OPEN	1-2 OPEN

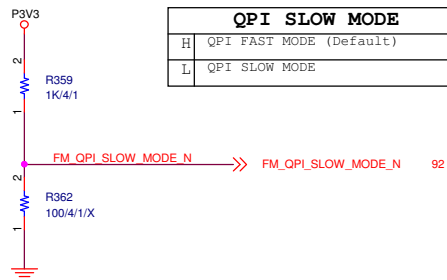
BIOS RECOVERY



BIOS_RVCR	
NO RECOVER	1-2 (DEFAULT)
RECOVER	2-3

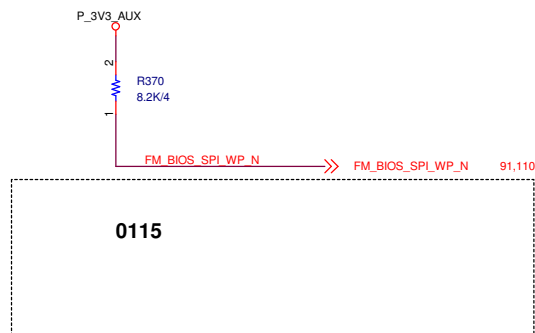
QPI SLOW MODE SELECT

CAD NOTE: PLACE THESE RESISTORS AT TOP LAYER.



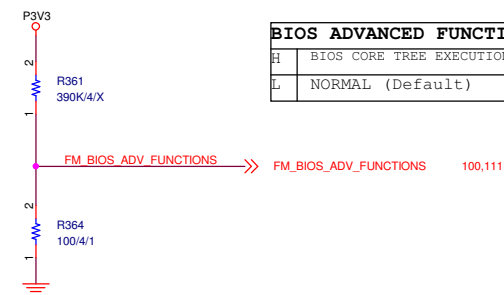
QPI SLOW MODE	
H	QPI FAST MODE (Default)
L	QPI SLOW MODE

BIOS WRITE PROTECT



BIOS ADVANCED FUNCTIONS

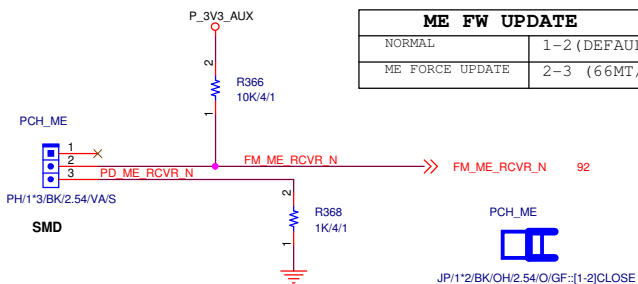
CAD NOTE: PLACE THESE RESISTORS AT TOP LAYER.



BIOS ADVANCED FUNCTION	
H	BIOS CORE TREE EXECUTION
L	NORMAL (Default)

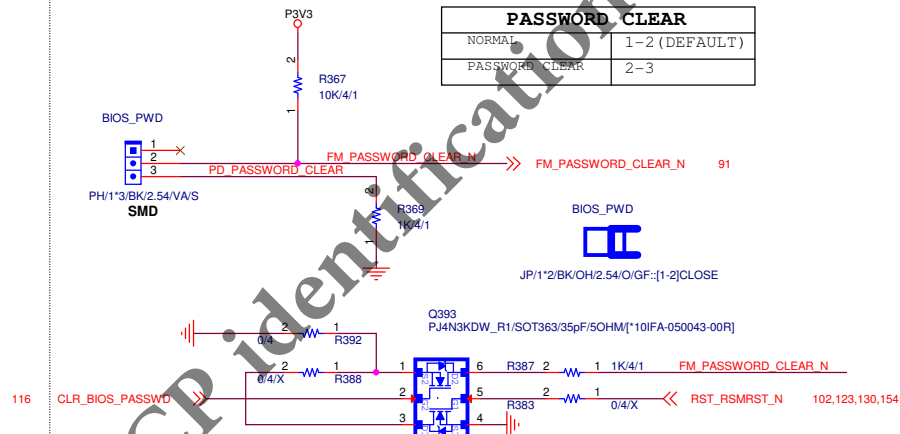
ME FIRMWARE UPDATE

ME FW UPDATE	
NORMAL	1-2 (DEFAULT)
ME FORCE UPDATE	2-3 (66MT/S)



PASSWORD CLEAR JUMPER

PASSWORD CLEAR	
NORMAL	1-2 (DEFAULT)
PASSWORD CLEAR	2-3

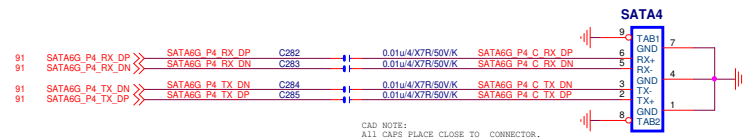
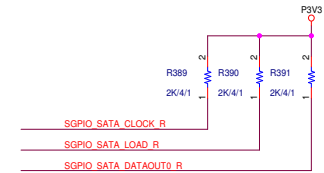
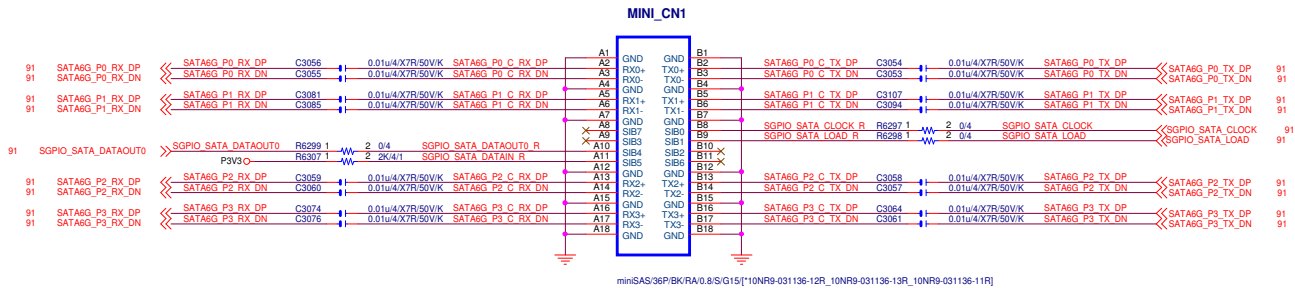


GIGABYTE™

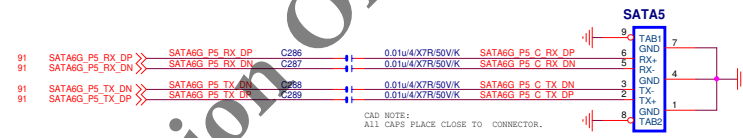
Title	WBG HEADERS (2/2)		
Size	Document Number	Rev	1.0
Custom	MD90-FS0		
Date:	Tuesday, June 09, 2015	Sheet	104 of 231

OCP identification Only

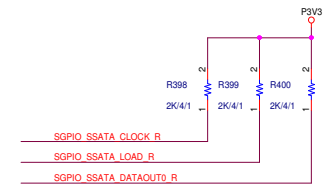
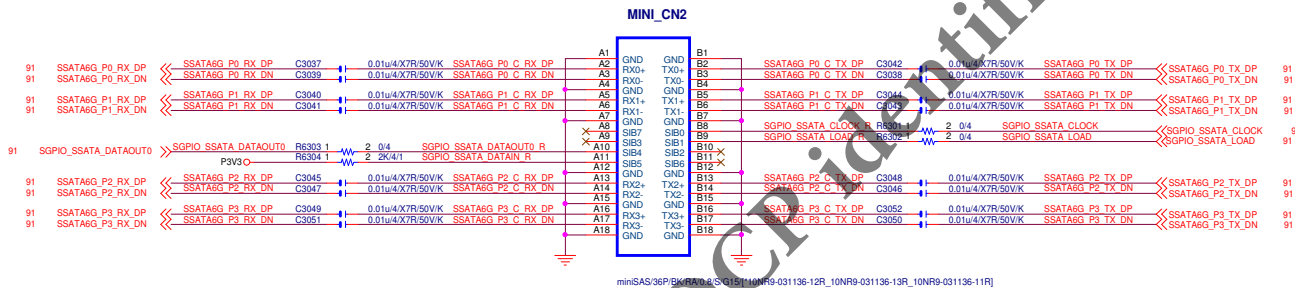
GIGABYTE™		
Title		
WBG SATA SGPIO		
Size	Document Number	Rev
Custom	MD90-FS0	1.0
Date:	Tuesday, June 09, 2015	Sheet 105 of 231



SATA3/17/RE/H/OP/VA/D/1/B/G15
PCB Footprint = 11NH_SATA3-B90_7_000-GB

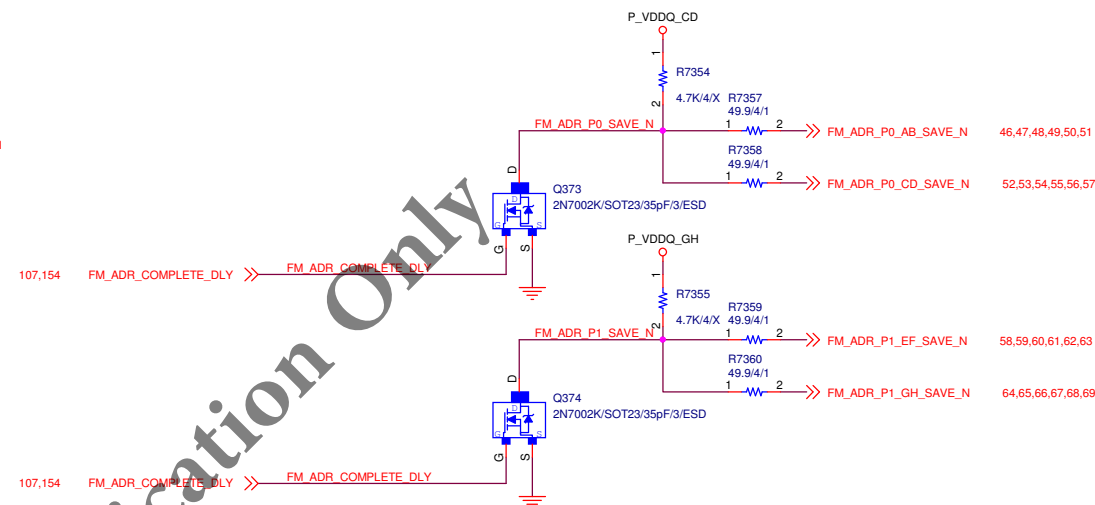
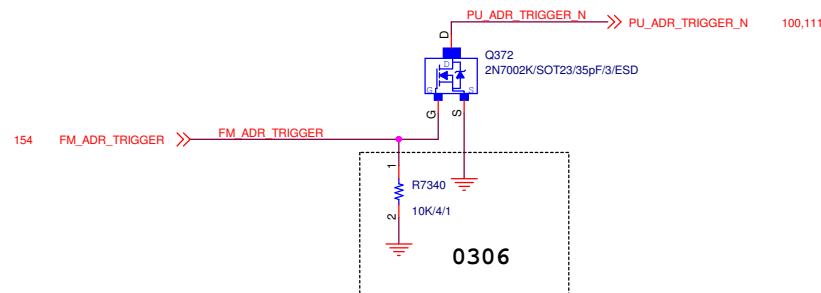


SATA3/17/RE/H/OP/VA/D/1/B/G15
PCB Footprint = 11NH_SATA3-B90_7_000-GB



FM_ADR_COMPLETE_DLY FROM CPLD TO DIMM

ADR Trigger FROM CPLD TO PCH

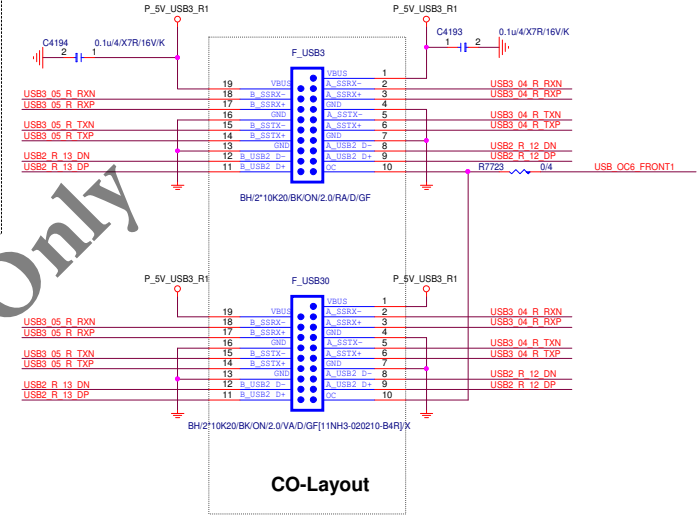
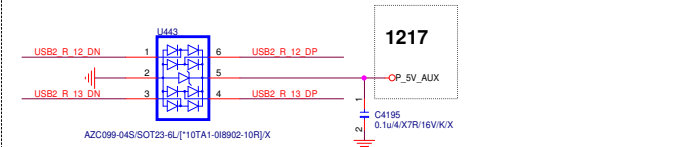
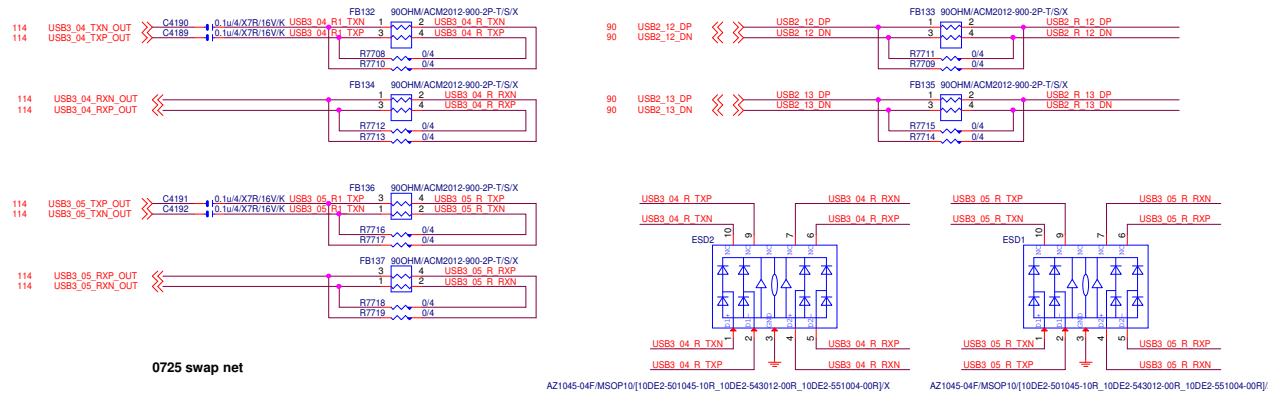


OCP identification Only

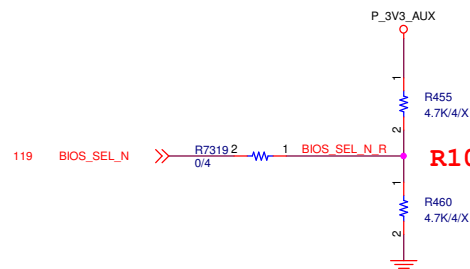
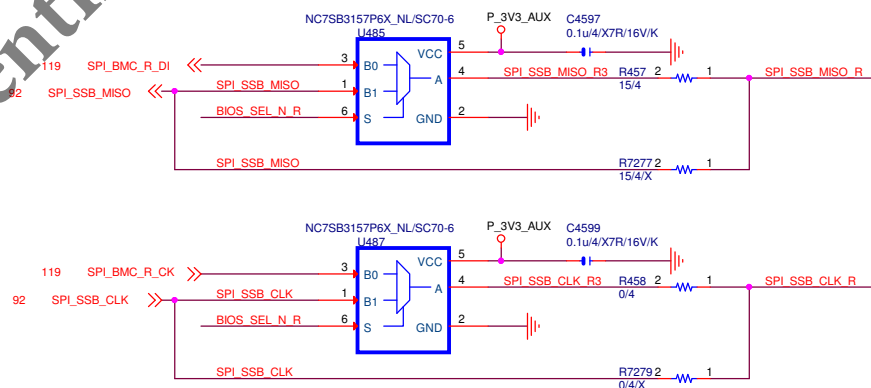
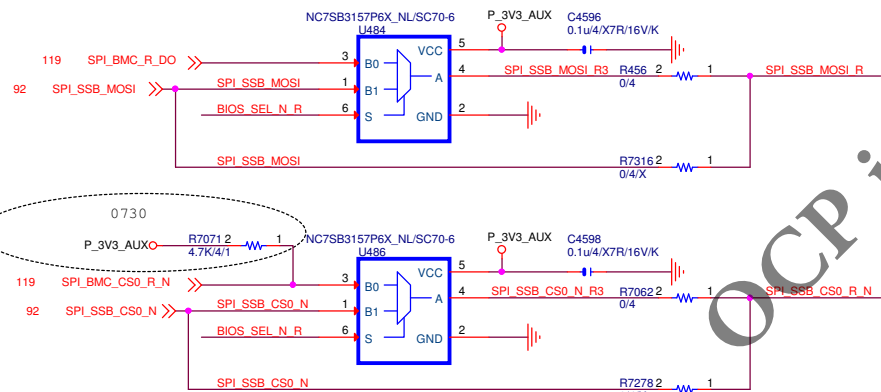
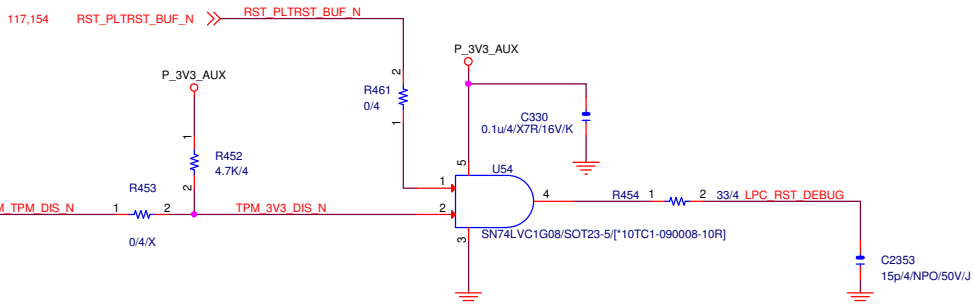
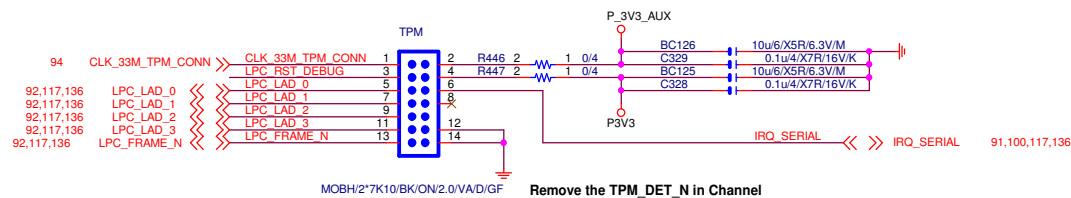
OCP identification Only

GIGABYTE™		
Title USB CONNECTORS_REAR1		
Size	Document Number	Rev
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Front USB3.0 [04:05] USB2.0[12:13]; OC6 FOR Front USB3



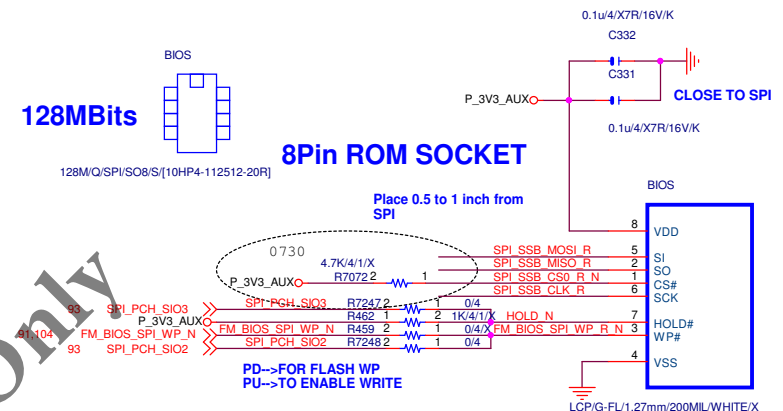
TPM



R10: Stuff R7319.

SPI BIOS

NOTE : SPI_CLK & SPI_MOSI must be length matched to within 500mils
SPI_CLK & SPI_CS0# must be length matched to within 500mils



CAD NOTE:
PLACE ALL SERIES RESISTORS EXCEPT MISO R NEAR WBG<0.5 AND MISO R NEAR
SPI <0.5.

NOA_0_FM_USB_OC_0_N
OC0 USB3_FRONT1

NOA_1_FM_USB_OC_1_N
OC1 F_USB2

NOA_2_FM_USB_OC_2_N

90 NOA_3_FM_USB_OC_3_N >> R471 1 2 10K/4/1 P_3V3_AUX
OC3

90 NOA_4_FM_USB_OC_4_N >> R473 1 2 10K/4/1 P_3V3_AUX
OC4

NOA_5_FM_USB_OC_5_N
OC5 USB3_REAR1_2

NOA_6_FM_USB_OC_6_N
OC6 USB3_FRONT1

90 NOA_7_FM_PCIE_SLOT4_DET_ID0 >> R517 1 2 0/4 << FM_PCIE_SLOT4_DET_ID0 87,100
OC7

NOA_8_GP21_PD

91,112 NOA_9_RST_PCIE_PCH_N >> R465 1 2 0/4 RST_PCIE_PCH_N >> RST_PCIE_PCH_N 100,154

91,111,112 NOA_10_FM_BIOS_ADV_FUNCTIONS >> NOA_10_FM_BIOS_ADV_FUNCTIONS >> NOA_10_FM_BIOS_ADV_FUNCTIONS 91,111,112
R467 1 2 0/4 FM_BIOS_ADV_FUNCTIONS << FM_BIOS_ADV_FUNCTIONS 100,104

91,111,112 NOA_11_FM_ADR_TRIGGER_N >> NOA_11_FM_ADR_TRIGGER_N >> NOA_11_FM_ADR_TRIGGER_N 91,111,112
R469 1 2 0/4 >> PU_ADR_TRIGGER_N 100,107

91 NOA_12_FM_NM_THROTTLE_N >> R472 1 2 0/4 FM_THROTTLE_N >> FM_THROTTLE_N 79,121

91 NOA_13_FM_CPU_PROCHOT_N >> R474 1 2 0/4 << FM_CPU_PROCHOT_N 80,100

92 NOA_14_FM_PCIE_SLOT4_DET_ID1 >> R476 1 2 0/4 << FM_PCIE_SLOT4_DET_ID1 100

92 NOA_15_FM_SMI_ACTIVE_N >> R478 1 2 0/4 FM_SMI_ACTIVE_N >> FM_SMI_ACTIVE_N 123

101,111,112 IRQ_BMC_PCH_NMI_NOA1_CLK << >> IRQ_BMC_PCH_NMI_NOA1_CLK >> IRQ_BMC_PCH_NMI_NOA1_CLK 101,111,112

92,111 FM_NMI_EVENT_N_NOA_CLK2 >> R498 1 2 4.7K/4/1 P3V3 >> FM_NMI_EVENT_N_NOA_CLK2 92,111
R5372 1 2 0/4 FM_NMI_EVENT_N >> FM_NMI_EVENT_N 123

GIGABYTE™

Title

WBG NOA

Size

Custom

Date:

Tuesday, June 09, 2015

Document Number

MD90-FS0

Rev

1.0

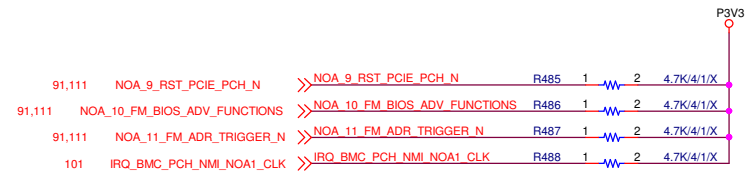
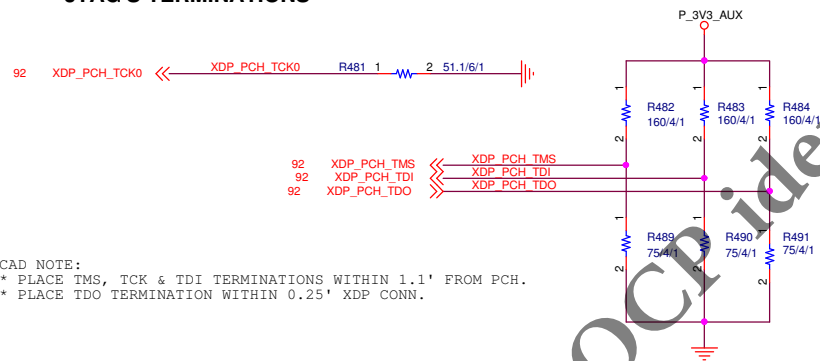
Sheet

111

of

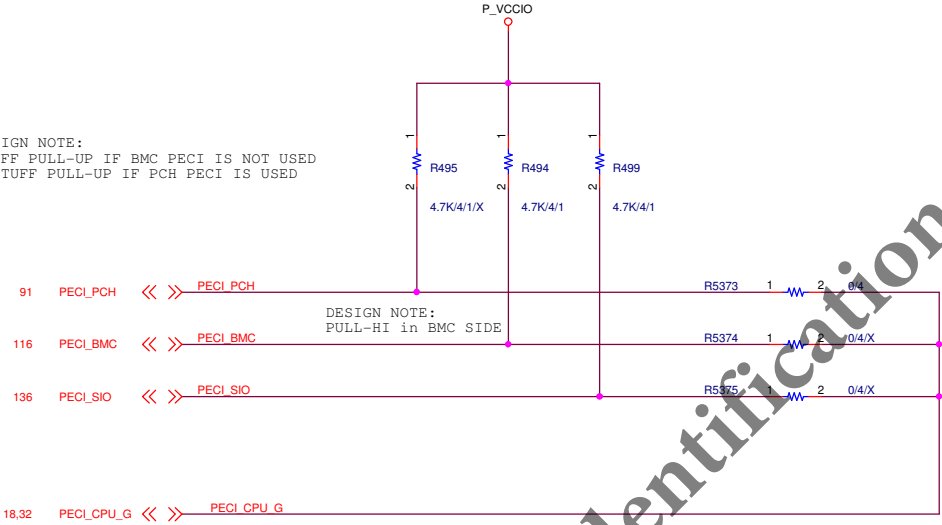
231

JTAG'S TERMINATIONS



DESIGN NOTE:
* THESE PULL UPS RESISTORS SHOULD BE PLACED
WHEN NOA INTERFACE IS USED TO AVOID HW STRAP
CORRUPTION.

DESIGN NOTE:
STUFF PULL-UP IF BMC Peci IS NOT USED
UNSTUFF PULL-UP IF PCH Peci IS USED



OCP identification Only

GIGABYTE™

Title

PAGE INDEX AND TITLE

Size
A

Document Number

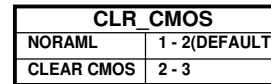
MD90-FS0

Rev
1.0

Date: Tuesday, June 09, 2015

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Don't place RB under socket of battery and bottom layer



128 FM_PCH_THERMTRIP_N >> R725 1 2 0/4 >> FM_PCH_THERMTRIP_N 128

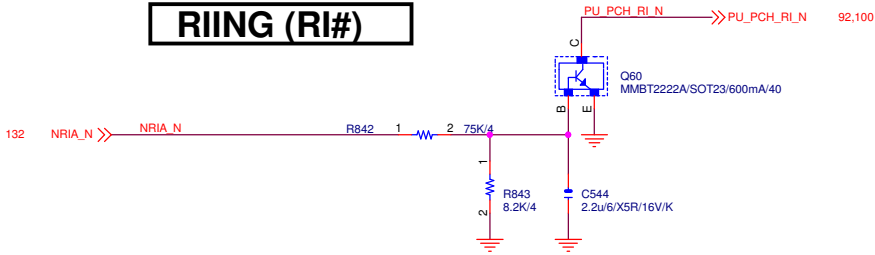
92,100,128 FM_PCH_BMC_THERMTRIP_R_N >> R713 1 2 0/4 >> FM_PCH_BMC_THERMTRIP_N 119

75,119 FM_CPU0_PROCHOT_LVT3_N >> R715 1 2 0/4 >> H_LVT3_CPU0_PROCHOT_OD_N 80,100

75,119 FM_CPU1_PROCHOT_LVT3_N >> R716 1 2 0/4 >> H_LVT3_CPU1_PROCHOT_OD_N 80,100

80 FM_MEM_THERM_EVENT_LVT3_N >> R718 1 2 0/4 >> FM_MEM_THERM_EVENT_BMC_N 119

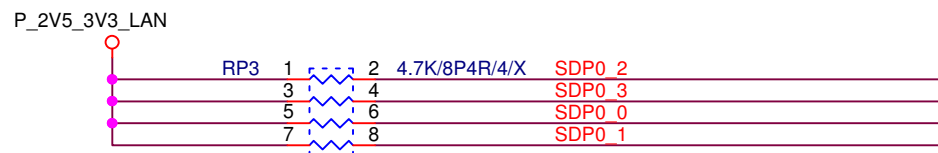
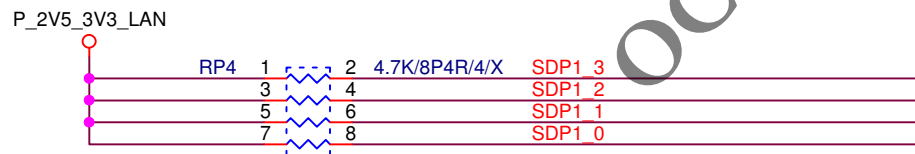
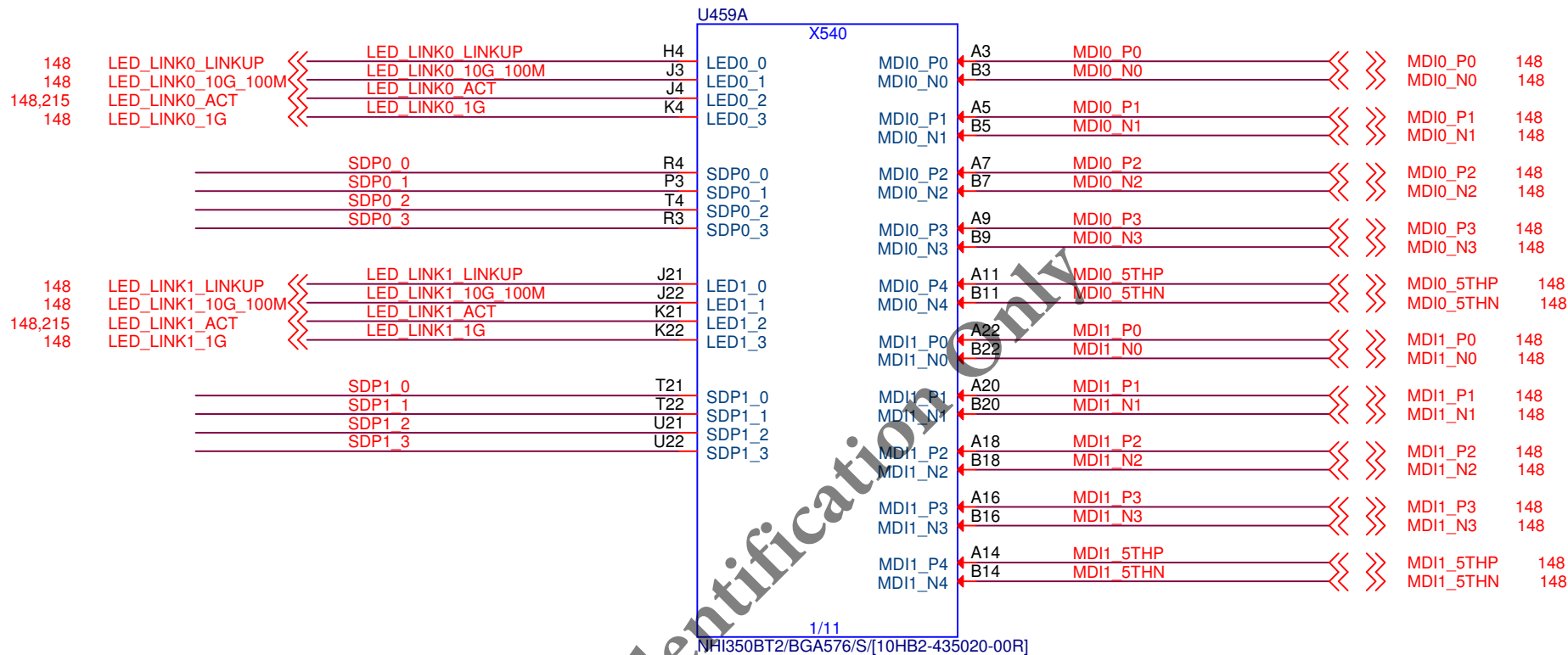
RIING (RI#)



OCP identification Only

OCP identification Only

GIGA-BYTE TECHNOLOGY CO., LTD			
Title			
=====LAN & PHY=====			
Size	Document Number		Rev
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GIGABYTE™

Title

X540 PCIE

Size
A

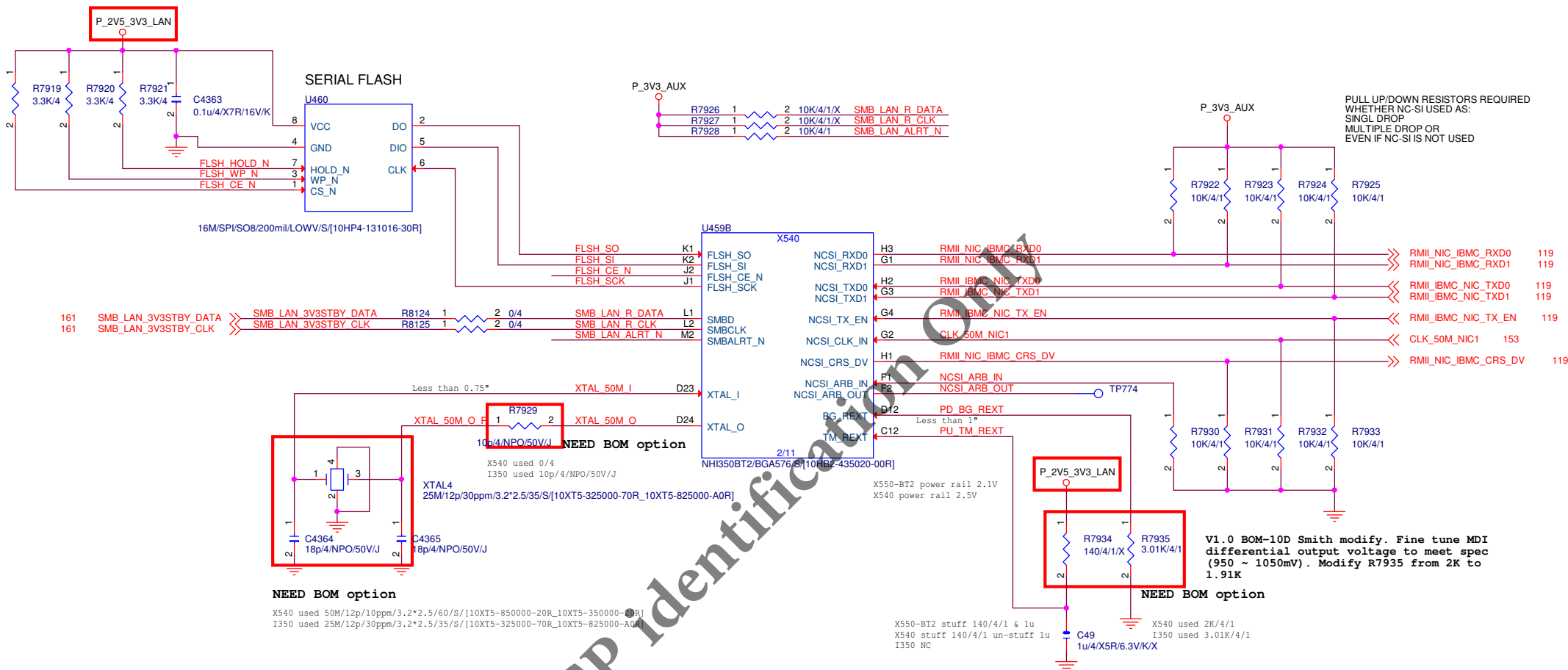
Document Number

MD90-FS0

Rev
1.0

Date: Tuesday, June 09, 2015

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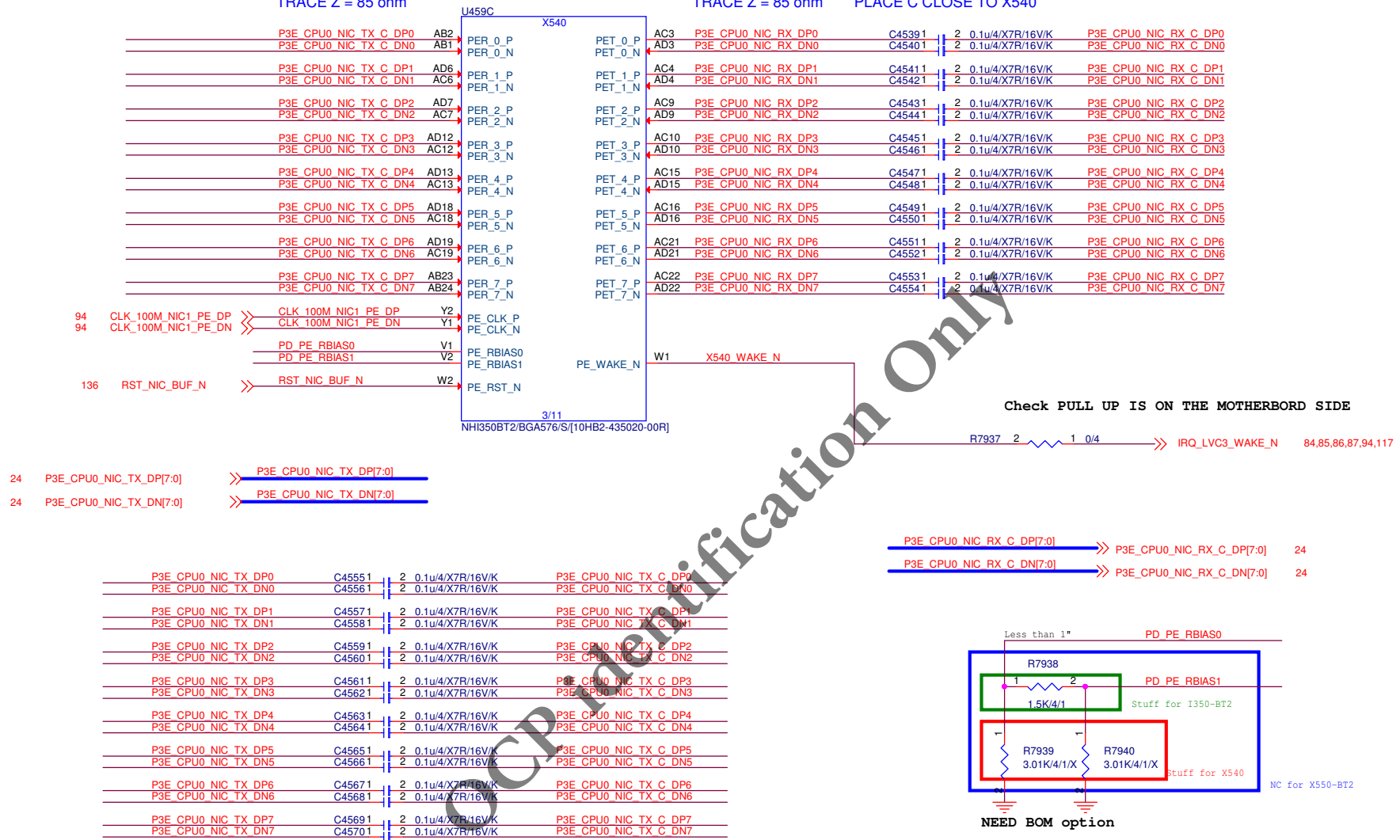
GIGABYTE™

Title			
X540 RSVD PINS			
Size	Document Number	Rev	
B	MD90-FS0	1.0	
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TRACE Z = 85 ohm

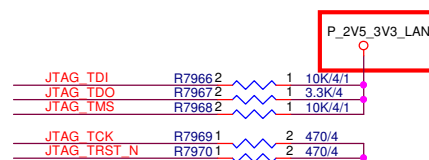
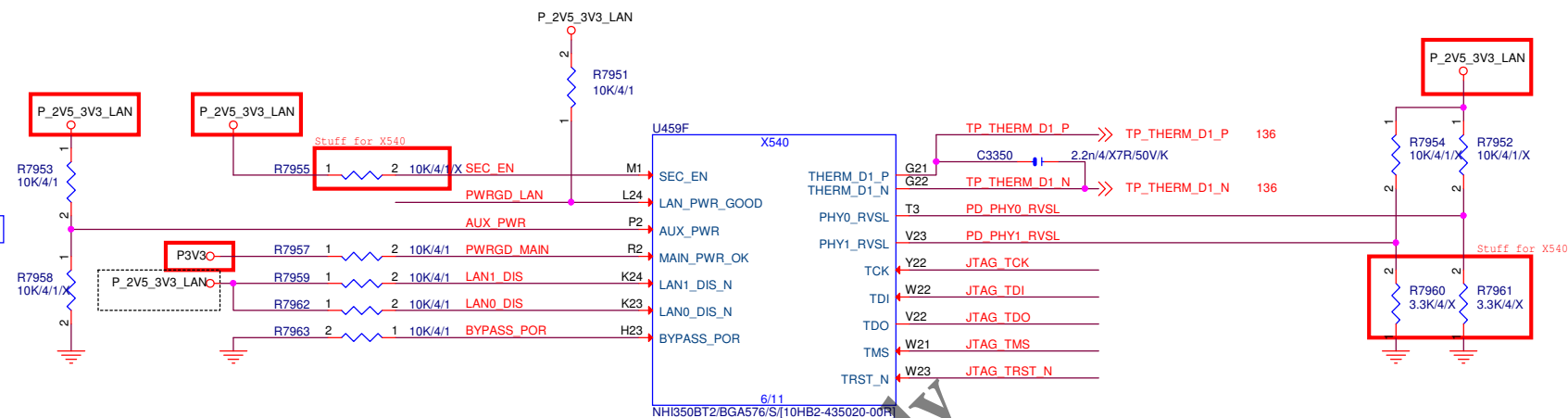
TRACE Z = 85 ohm

PLACE C CLOSE TO X540

**GIGABYTE™**

Title				
X540 MISC				
Size	Document Number			Rev
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AUX_PWR	FUNCTION
HI	AUX POWER IS AVAILABLE X540 SUPPORT D3 COLD POWER STATE
LOW	AUX POWER IS NOT AVAILABLE

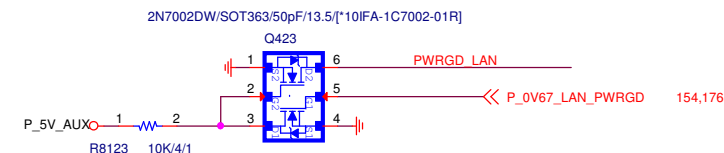
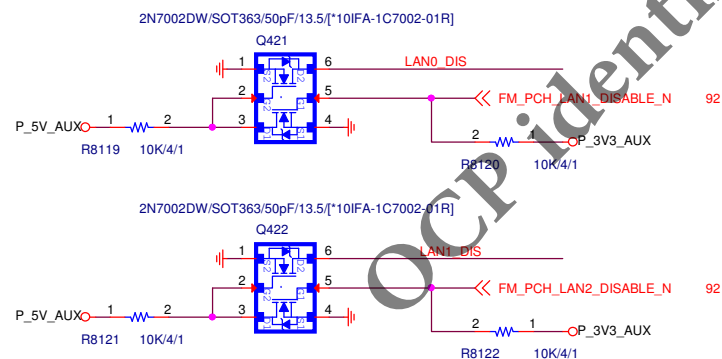


IF THE JTAG INTERFACE IS NOT CONNECTED TO THE SYSTEM JTRST_N SHOULD BE CONNECTED TO PD.

PHY0_RVSL	PHY MDI LANE REVERSAL
HI	MDI LANE ORDER: 3,2,1,0-->A,B,C,D
LOW	MDI LANE ORDER: 0,1,2,3-->A,B,C,D

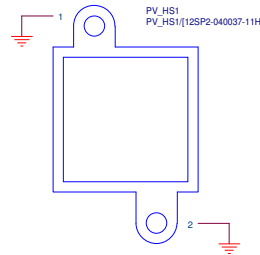
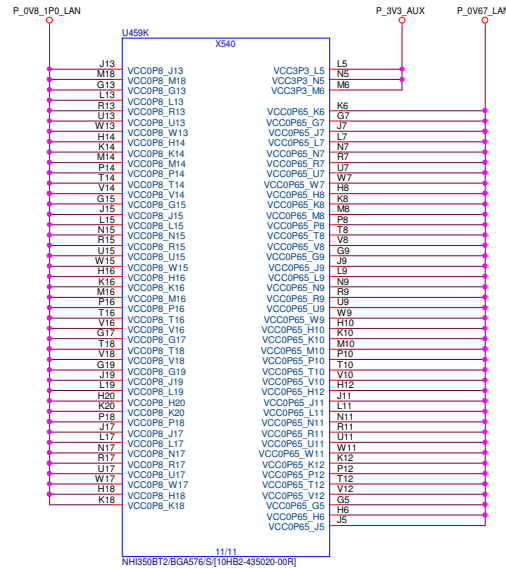
5th channel swap not supported.

FOR I350-BT2: PHY MDI LANE REVERSAL CONFIGURATION USE EEPROM SETTING

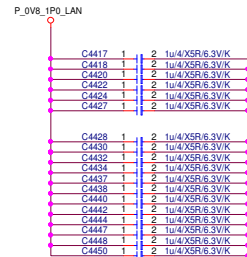


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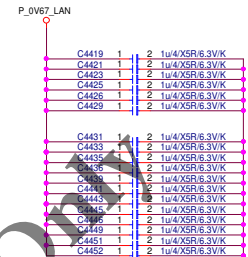
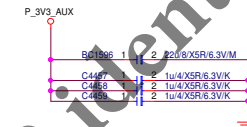
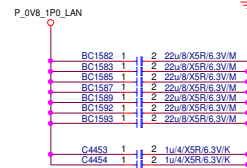
Title		
X540 POWER		
Size	Document Number	Rev
B	MD90-FS0	1.0
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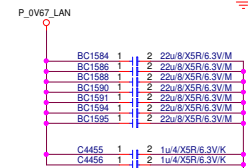
PCB Footprint = 12SP_60X16X10M7_2_100-GB



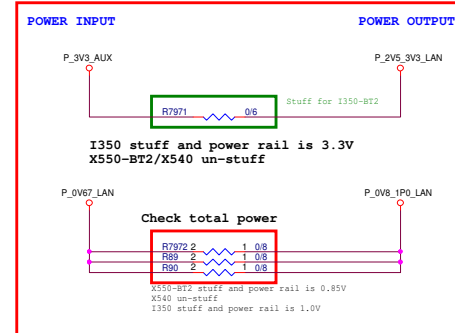
PLACE 6 BULK UNDER THE BGA



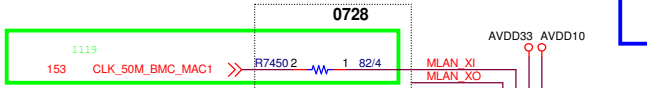
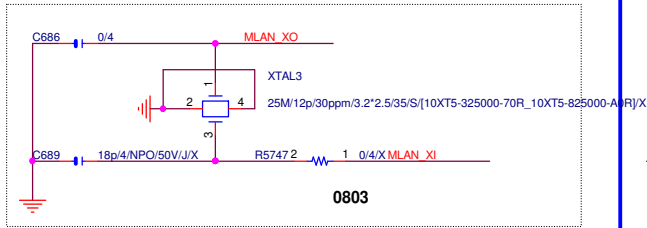
PLACE 6 BULK UNDER THE BGA



Power rail option

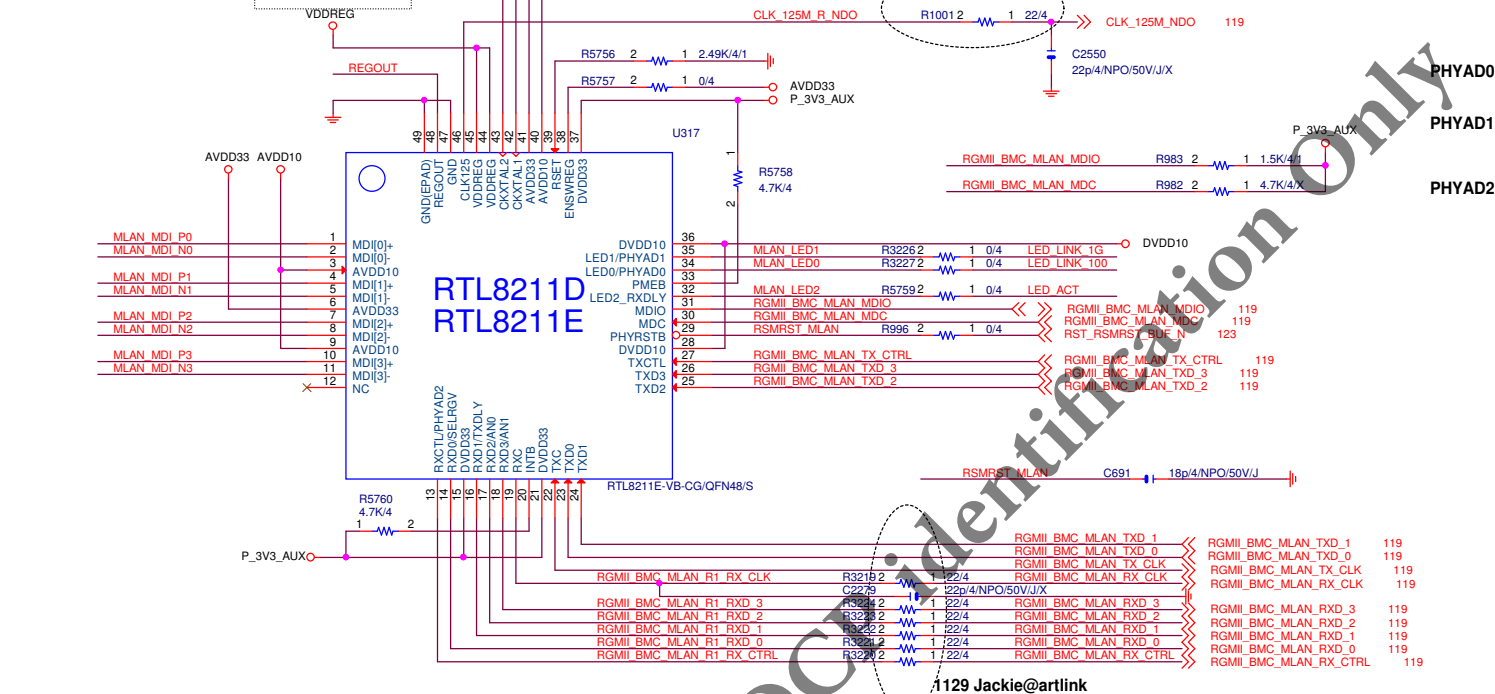
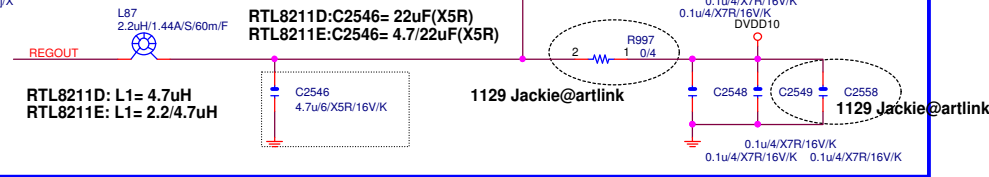


RTL8211E

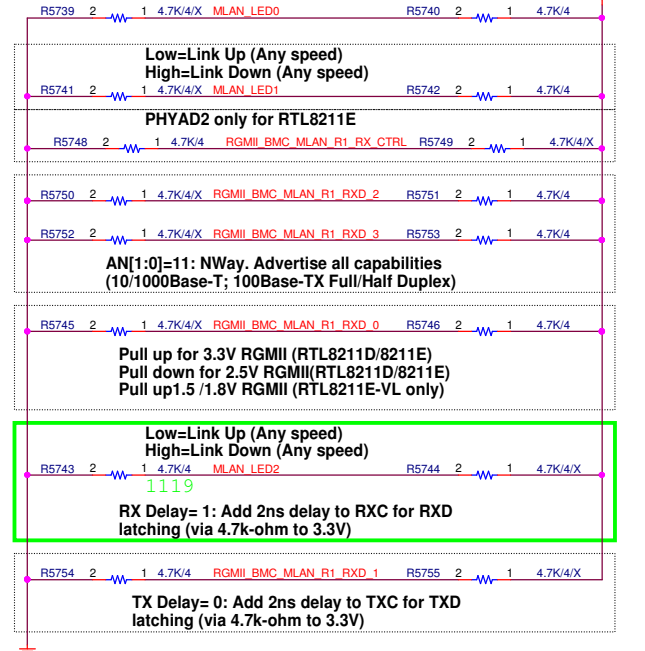


1.05V Power

Note 1: The Trace length between L87 and PHY's Pin48 must be within 0.5 cm. C2546 and C2547 to L87 must be within 0.5cm.

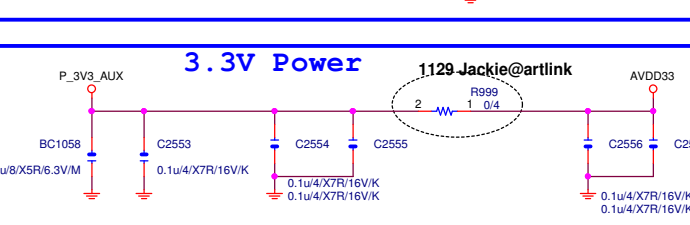


Configuration Setting

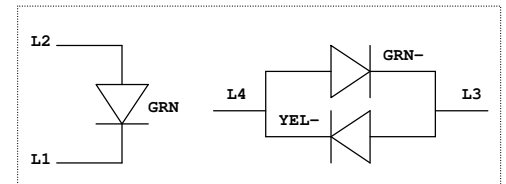
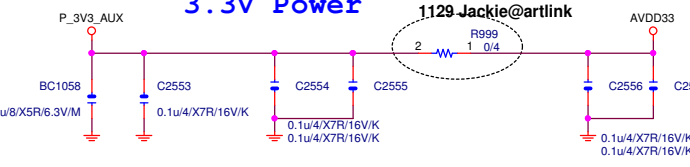


VDDREG

Note 2: The Trace length from C2251, C2252 to Pin 44,45(VDDREG) must be within 0.5 cm. The trace width from AVDD33 to Pin 44,45 should=40mils



3.3V Power



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Title	MLAN_PHY_RTL8211E
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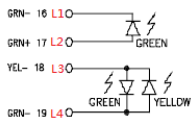
Name	Color	Condition	What it describes
Link/Activity	Green	ON	LAN link / No access
	Green	BLINK	LAN access
	-	OFF	Idle
	-	BLINK	Port identification (Base on Lan)
SPEED/Link	-	BLINK	Port identification (Base on Lan)
	-	OFF	10Mbps connection
10/100 Speed	Green	ON	100Mbps connection
	-	OFF	10Mbps connection
	-	OFF	10Mbps connection
	-	OFF	10Mbps connection
1GbE Speed	Yellow	ON	1Gbps connection
	Green	ON	100Mbps connection
	-	OFF	10Mbps connection
	-	OFF	10Mbps connection
10GbE Speed	Green	ON	10Gbps connection
	Yellow	ON	1Gbps connection
	-	OFF	100Mbps connection
	-	OFF	100Mbps connection
40GbE Speed Need check	Green	ON	40Gbps connection
	Yellow	ON	10Gbps connection
	-	OFF	10Gbps connection

PLACE AND ROUTED AS BALANCED DIFFERENTIALLY
LOCATE CLOSE TO X540

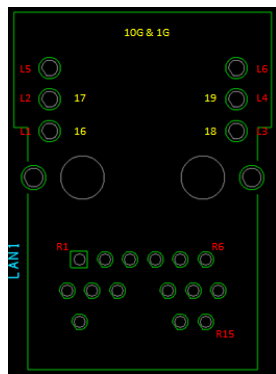
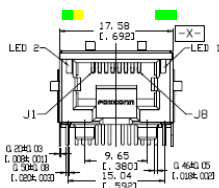
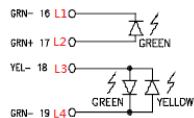


X550-BT2 un-stuff inductors & cap but stuff 0 OHM
X540 stuff inductors & cap
1350 NC

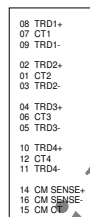
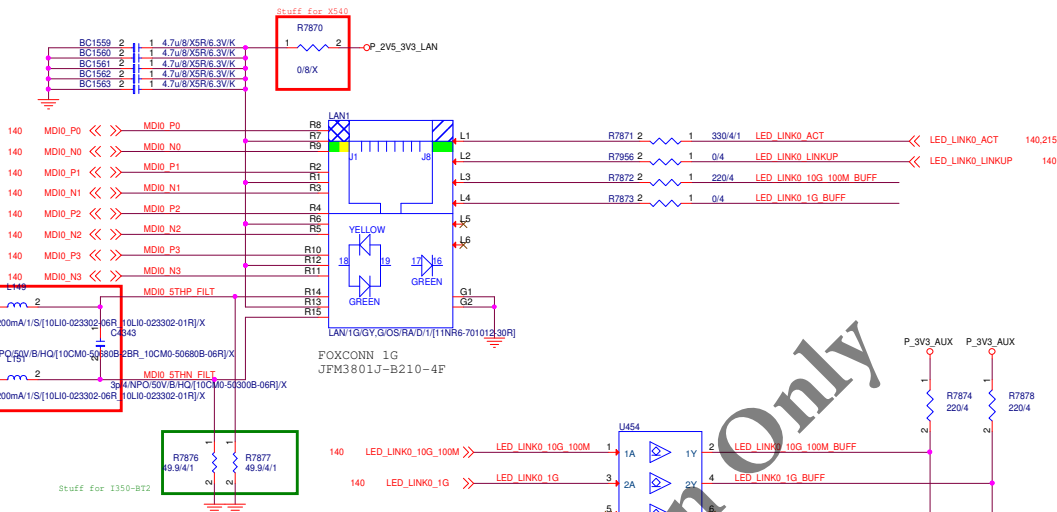
10G LAN LED



1G LAN LED

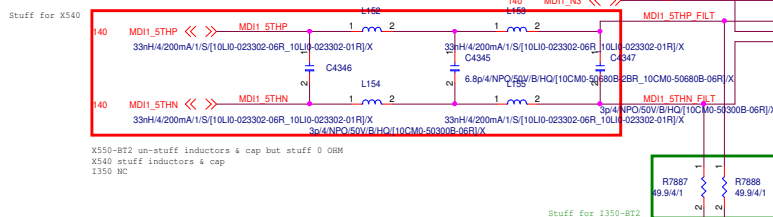


Co-Layout Footprint
11NR_RJ45E0_21_C00-GB



LINK/ACTIVITY	COLOR	LIGHT	ACTION
LAN	GREEN	ON	LAN LINK / NO ACCESS
	Green	BLINK	LAN ACCESS
	-	OFF	IDLE
	-	BLINK	Port identification (Base on Lan)
10 GbE	Green	ON	10 Gbps CONNECTION
	Green	BLINK	IDENTIFICAT 10 Gbps CONN.
	Yellow	ON	1 Gbps CONNECTION
	Yellow	BLINK	IDENTIFICAT 1 Gbps CONN.
10 Mbps	Green	ON	10 Mbps CONNECTION
	-	OFF	10 Mbps OR 100 Mbps CONNECTION

PLACE AND ROUTED AS BALANCED DIFFERENTIALLY
LOCATE CLOSE TO X540



X550-BT2 un-stuff inductors & cap but stuff 0 OHM
X540 stuff inductors & cap
1350 NC

