PROJECT NAME : MD90-FS0
PROJECT CODE : S14043-0
Major Chipsets : Haswell EP Processor + Wellsburg (PCH)
I/O Chipsets : I350 + ASPEED AST2400

Team Member List :

Members	Name	TEL Ext.	Email
PM			
HW Engineer			
Project Leader			
ME Engineer			
SI Engineer			
SW Engineer			
Layout Engineer			
FW Engineer			
DQA Engineer			
Thermal			
Validation Engineer			
CPE			
FAE Engineer			
Sales			

PCB part number

PCB1

PCB/[10PMD90FS0-TN-S10B_10PMD90FS0-TX-S10B]

EC Key 入 *1 SMT 階

MAC Label part number

MAC_LB1

MAC/[12LB4-016006-2AR_12LB4-016006-20R]

MAC_LB2

MAC/[12LB4-016006-2AR_12LB4-016006-20R]

DED_MAC

MAC/[12LB4-016006-2AR_12LB4-016006-20R]

SHA_MAC

MAC/[12LB4-016006-2AR_12LB4-016006-20R]

EC Key 入 *6 DIP階

SERIAL Number part number

SFIS1

SFIS/[12LB4-020004-0AR_12LB4-020004-00R]

EC Key 入 *1 SMT 階

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Title: COVER		
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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Title: PAGE INDEX AND TITLE		
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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Title	MECHANICAL DRAWING	
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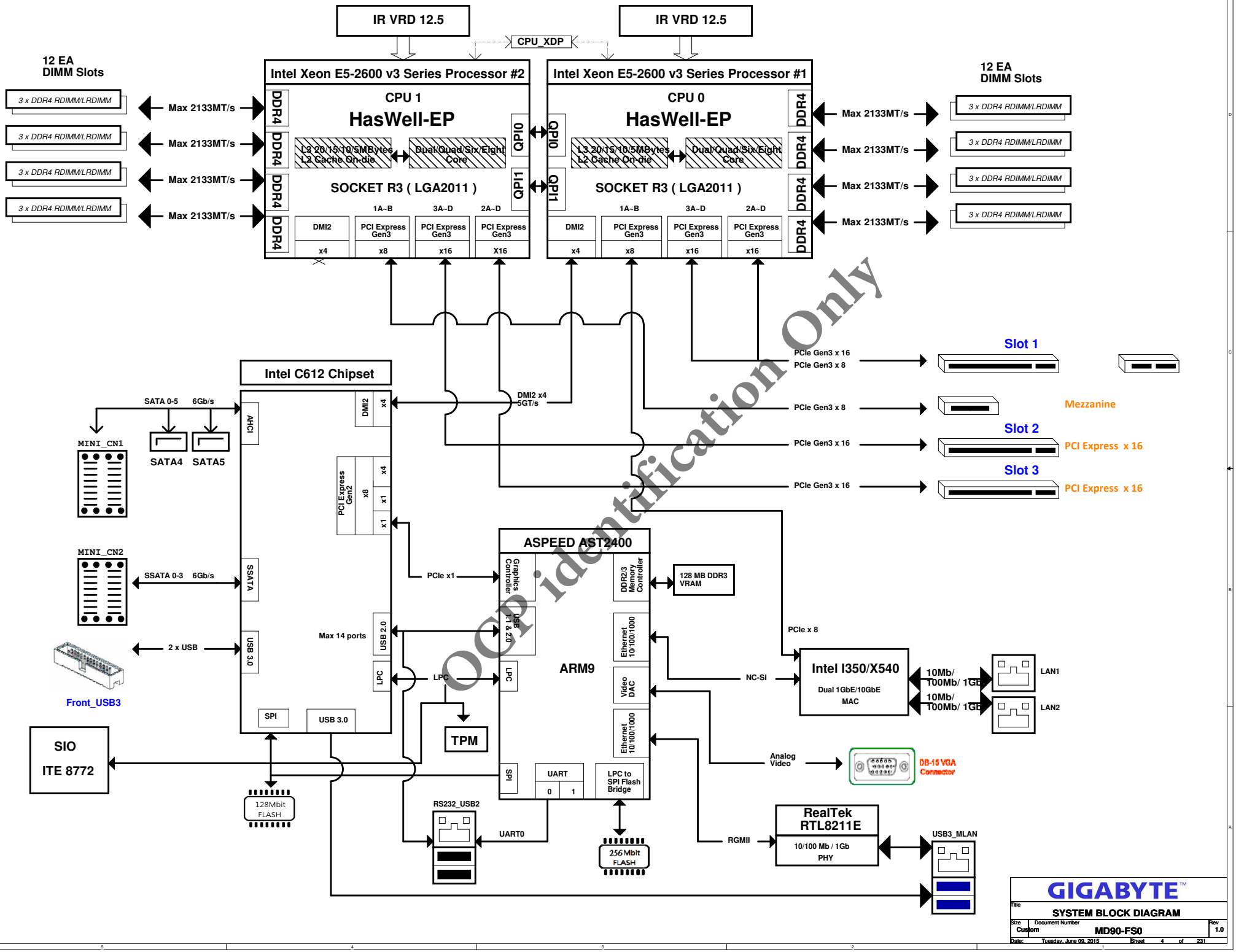
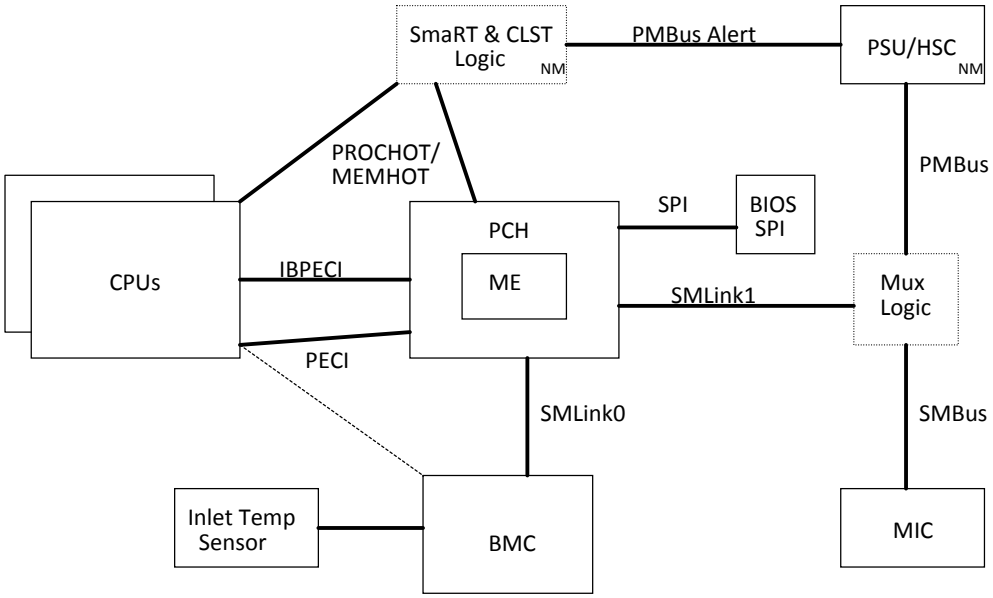
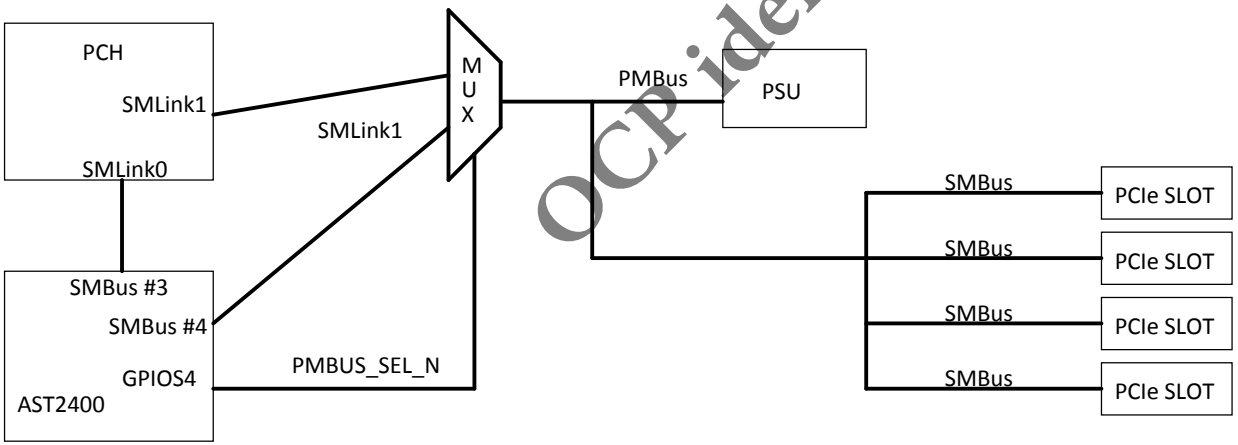

IR VRD 12.5
IR VRD 12.5
CPU_XDP
12 EA DIMM Slots
Intel Xeon E5-2600 v3 Series Processor #2
CPU 1
HasWell-EP
SOCKET R3 (LGA2011)
Intel Xeon E5-2600 v3 Series Processor #1
CPU 0
HasWell-EP
SOCKET R3 (LGA2011)
3 x DDR4 RDIMM/LRDIMM
Max 2133MT/s
DDR4
L3 20/15/10/5MBytes L2 Cache On-die
Dual/Quad/Six/Eight Core
QPI0
QPI1
DMI2
PCI Express Gen3
1A~B
3A~D
2A~D
x4
x8
x16
X16
Intel C612 Chipset
DMI2 x4 5GT/s
SATA 0-5 6Gb/s
AHCI
MINI_CN1
SATA4
SATA5
PCI Express Gen2
MINI_CN2
SSATA 0-3 6Gb/s
SSATA
2 x USB
USB 3.0
Front_USB3
Max 14 ports
USB 2.0
LPC
SPI
USB 3.0
SIO
ITE 8772
128Mbit FLASH
TPM
PCIe x1
ASPEED AST2400
Graphics Controller
DDR2/3 Memory Controller
128 MB DDR3 VRAM
USB 1.1 & 2.0
Ethernet 10/100/1000
Video DAC
ARM9
SPI
UART
0
1
LPC to SPI Flash Bridge
RS232_USB2
UART0
256 Mbit FLASH
PCIe x 8
Intel I350/X540
Dual 1GbE/10GbE MAC
NC-SI
10Mb/ 100Mb/ 1GB
LAN1
LAN2
Analog Video
DB-15 VGA Connector
RealTek RTL8211E
10/100 Mb / 1Gb PHY
RGMII
USB3_MLAN
PCIe Gen3 x 16
PCIe Gen3 x 8
Slot 1
Mezzanine
Slot 2
PCI Express x 16
Slot 3
PCI Express x 16
OCP identification Only
GIGABYTE
SYSTEM BLOCK DIAGRAM
Size Custom
Document Number MD90-FS0
Rev 1.0
Date: Tuesday, June 09, 2015
Sheet 4 of 231



Mux Logic



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Title: NM HW Topology		
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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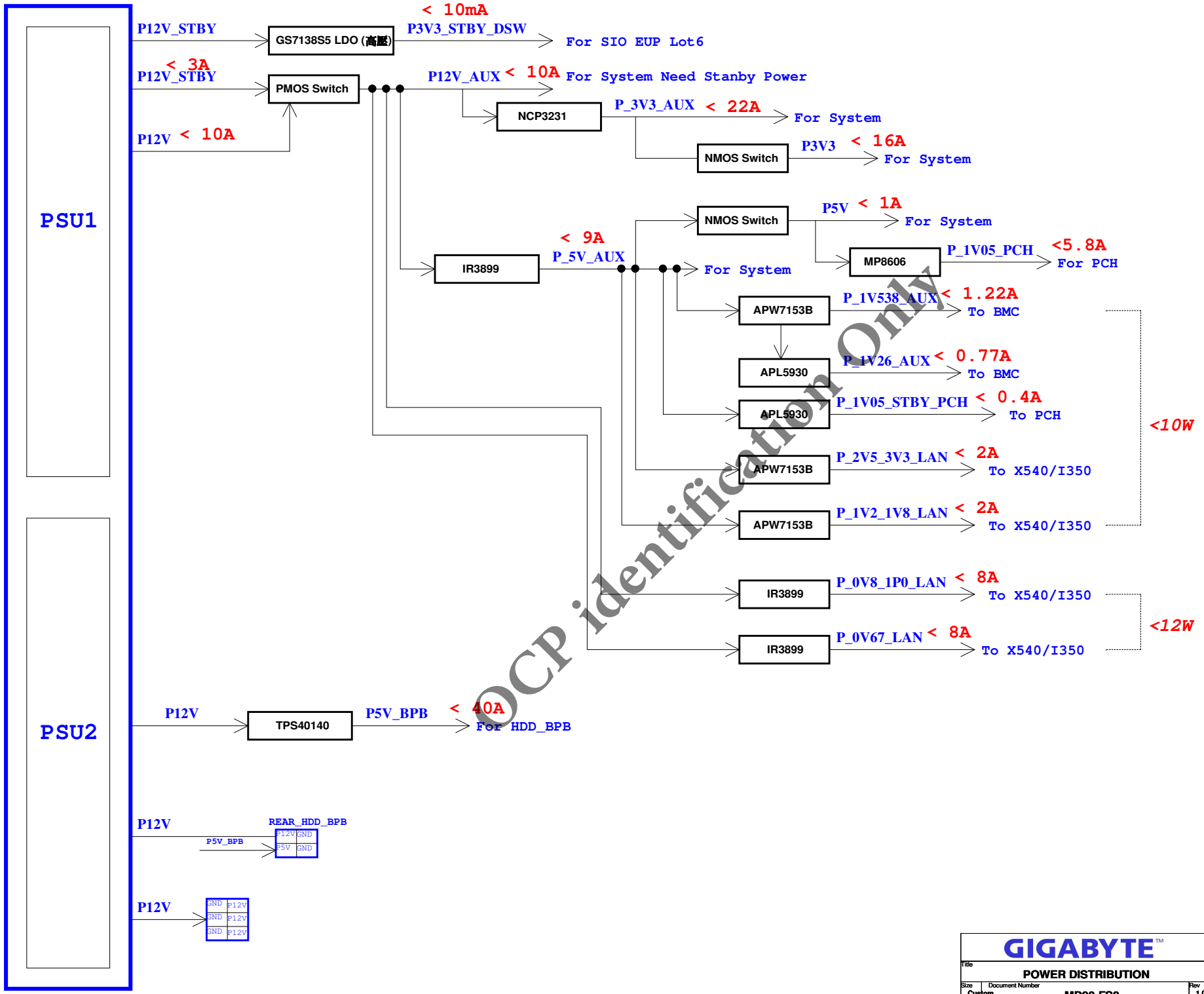

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Title: POWER DISTRIBUTION

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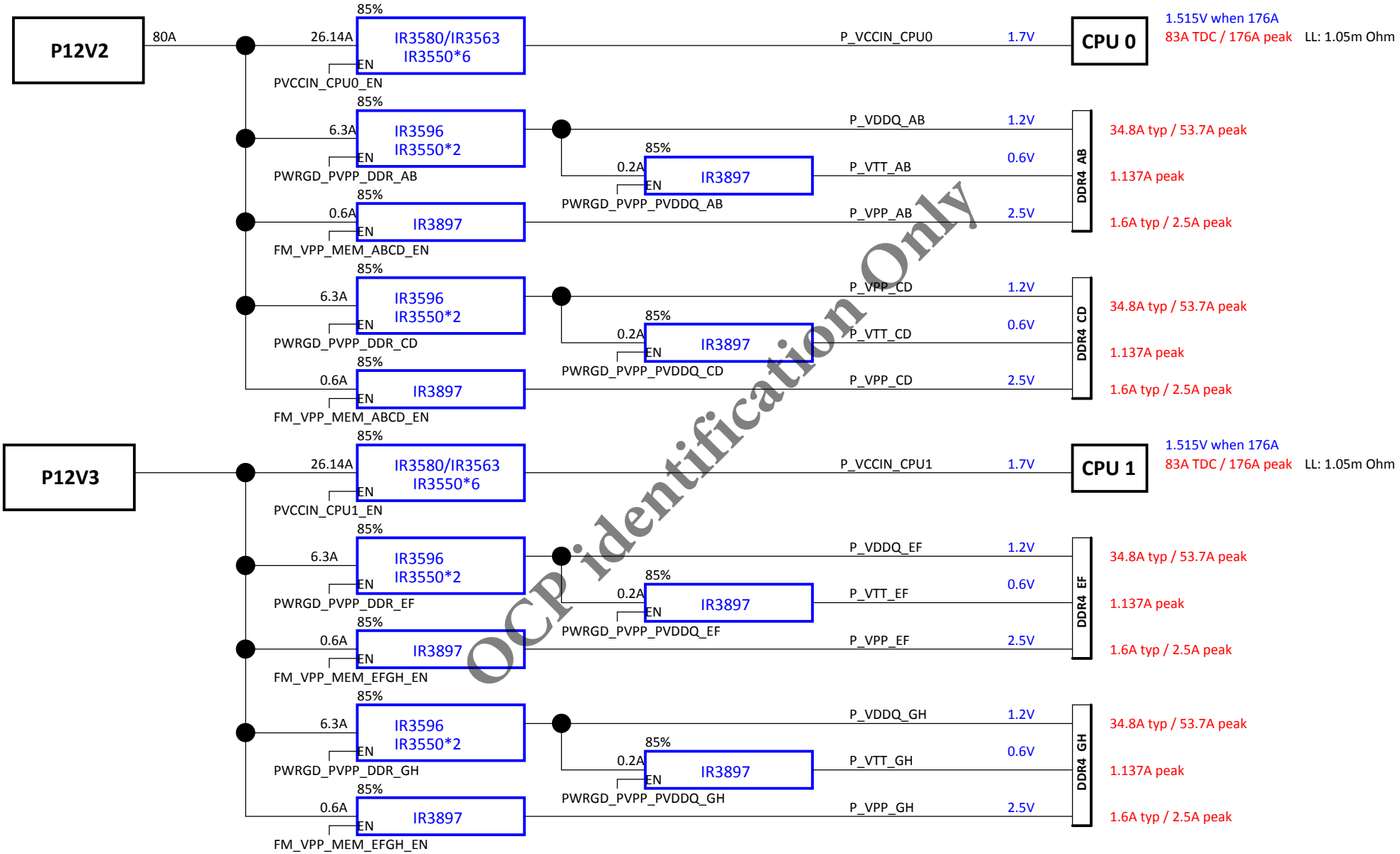
VR BLOCK DIAGRAM-1



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Title	VR BOLOCK DIAGRAM1	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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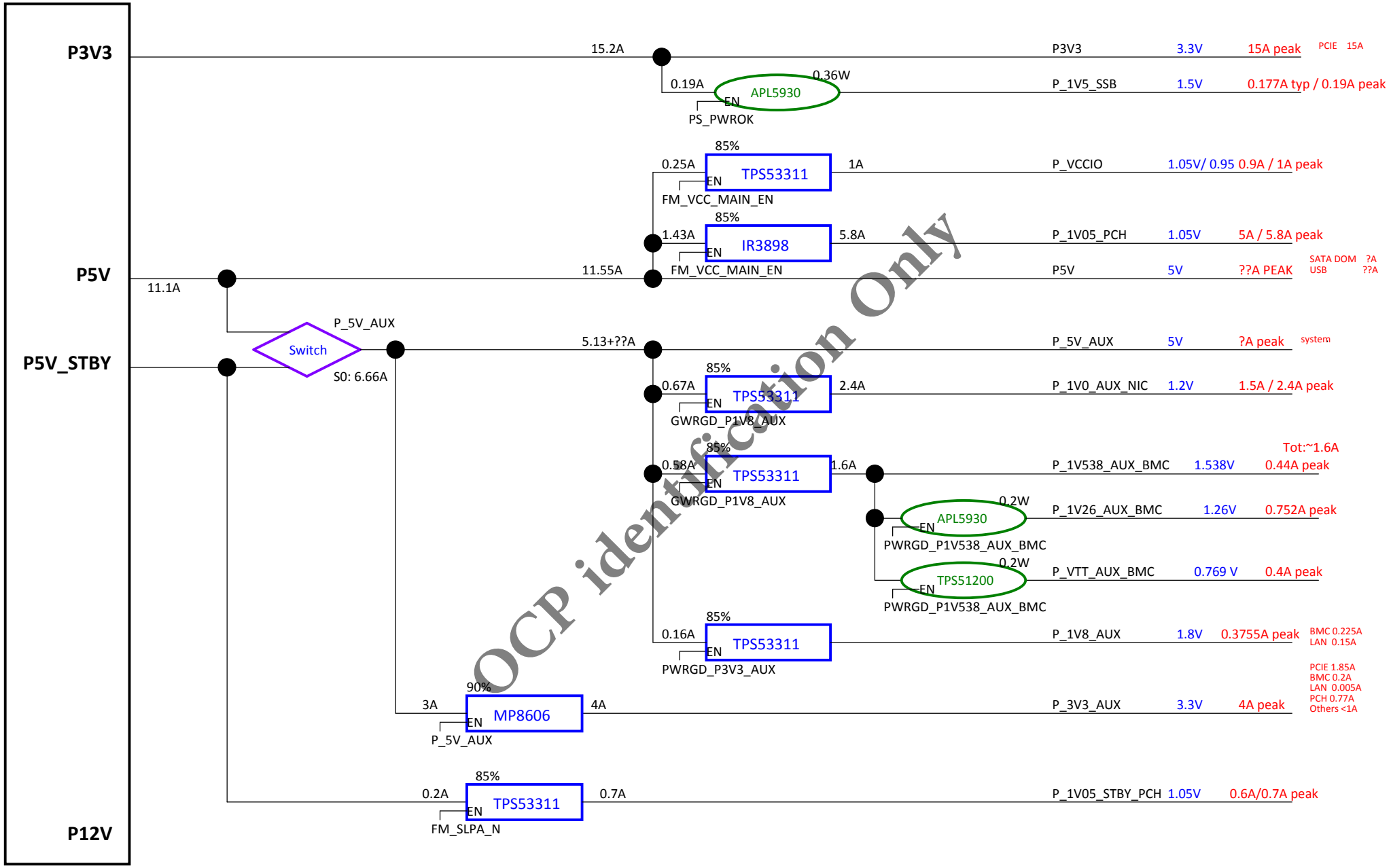
VR BLOCK DIAGRAM-2



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Title	VR BLOCKDIAGRAM2	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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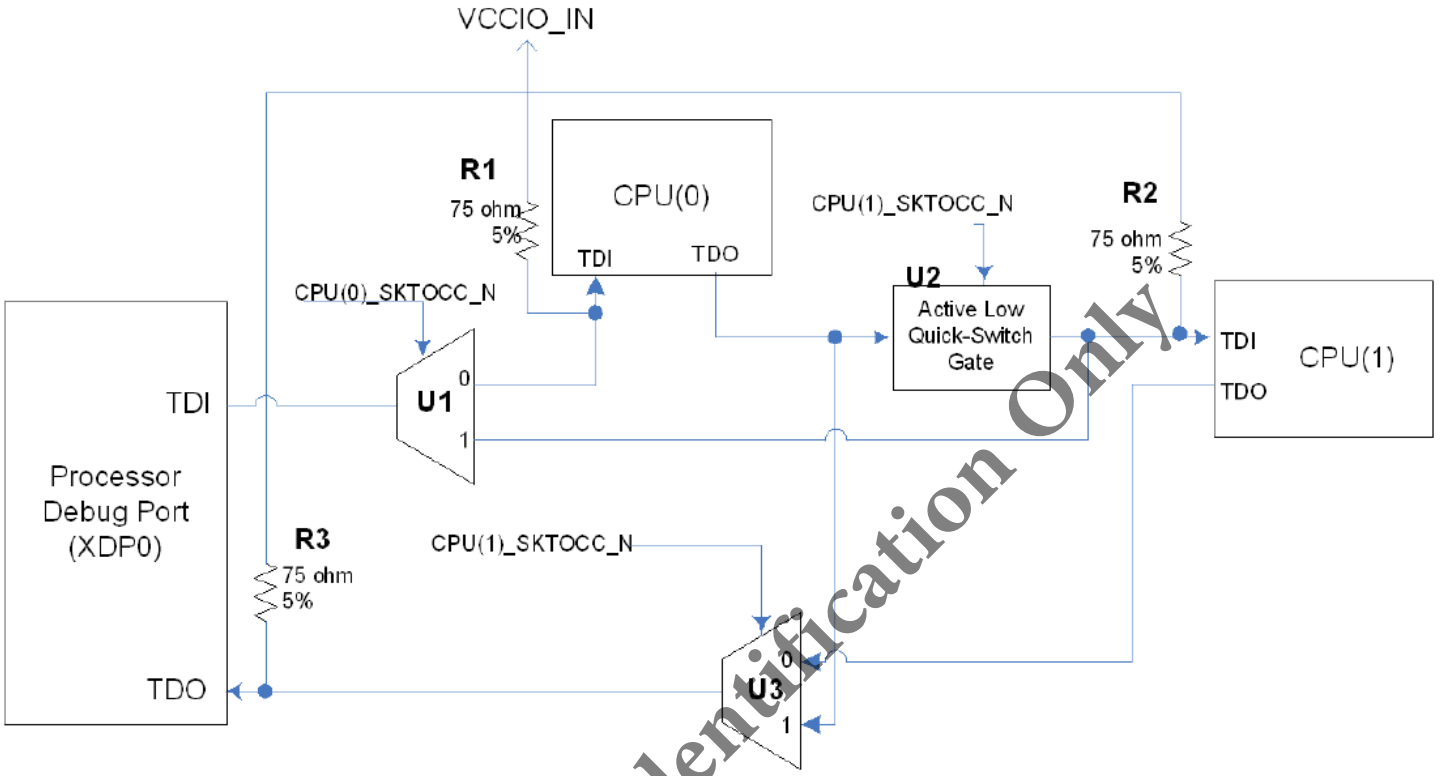
Figure 378. Processor XDP 2S TDI-TDO Topology with Automatic Bypass Quick Switches



CAD Notes:
- Place R1 and R2 to within 200ps of the CPU(0) and CPU(1)TDI pin respectively
- Place R3 to within 50ps of XDP TDO pin
- Place U1 to within 1.1" of both U2 and U3.
- Stub length on TDI and TDO is 200ps.
- No trace length constraint for TDO and TDI traces

U1 and U3 = 2:1 Mux/Demux with Max Ron of 20ohm, Max Capitance of 20pF (ex. NC7SB3157 or NC7SB3257)
U2 = Active LOW enable 1-bit Bus Switch with Max Ron of 6 ohm, Max Capacitance of 20 pF (ex. 74CBTLV1G125)

Note: it is acceptable to replace R1 and R3 with 51ohm 5% resistor.

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Title: XDP/JTAG BLOCK DIAGRAM(PCH)

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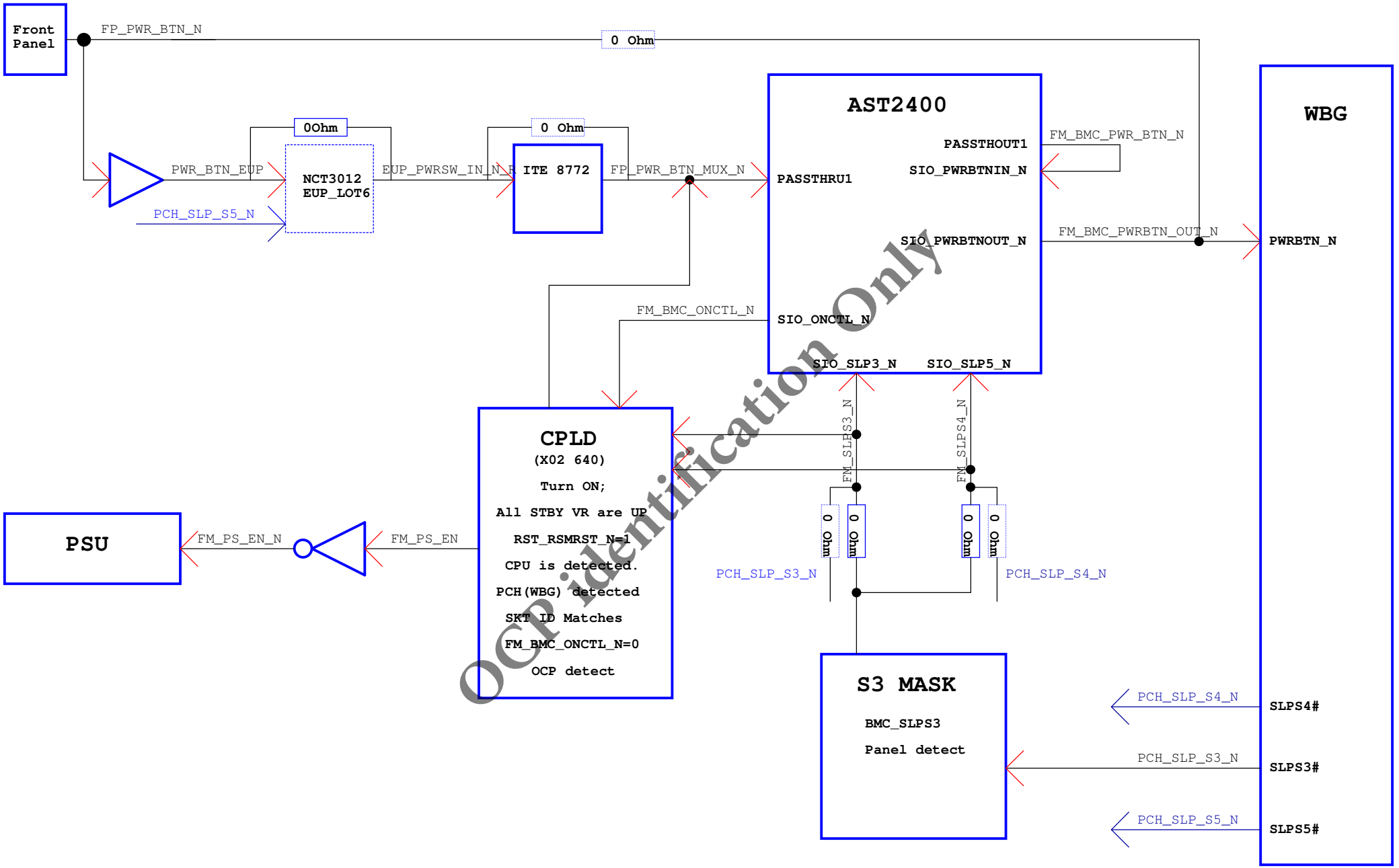

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Title: POWER BUTTON PATH LOOP

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Title: PWR GOOD/ RST DIAGRAM

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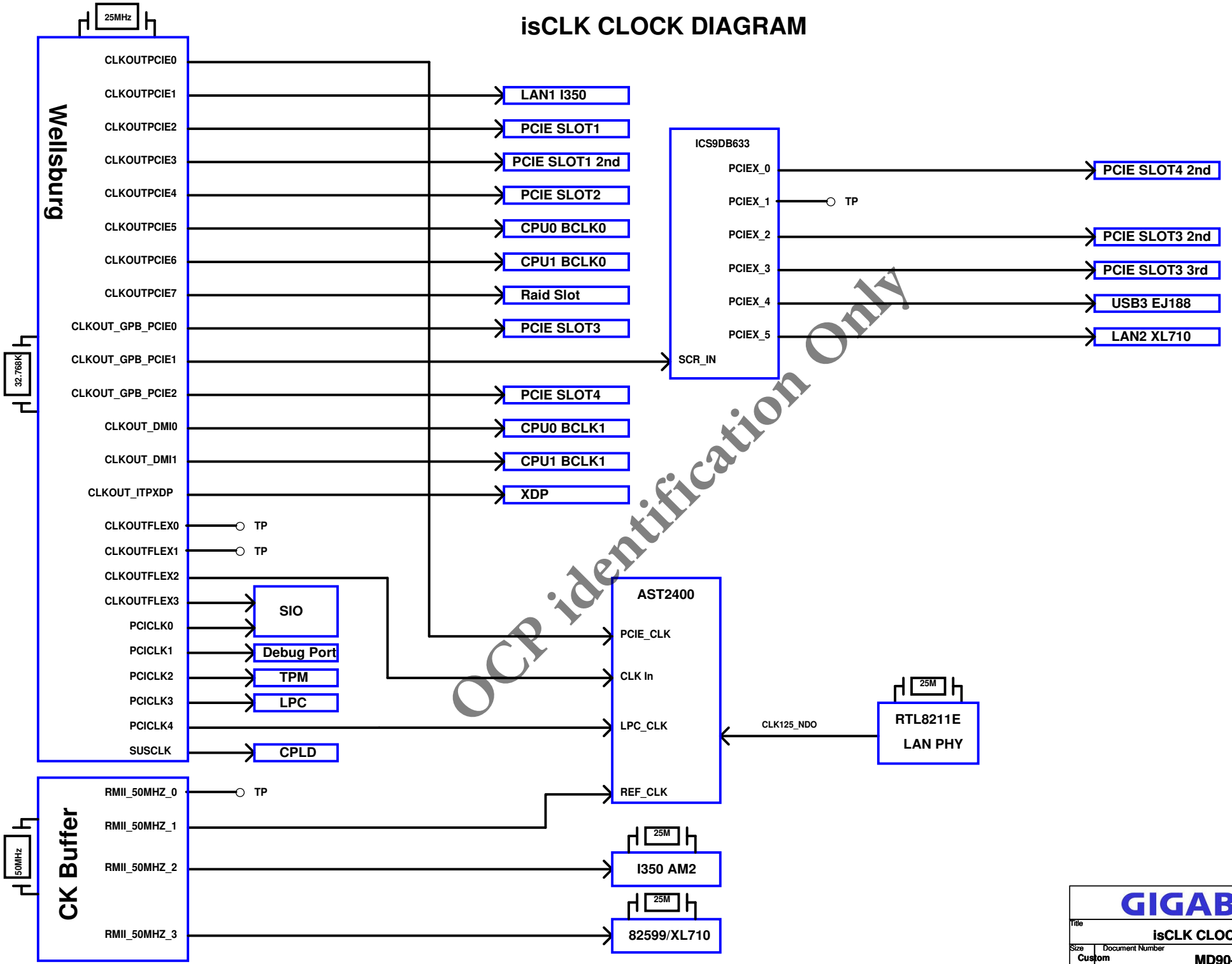
isCLK CLOCK DIAGRAM



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Title	isCLK CLOCK DIAGRAM	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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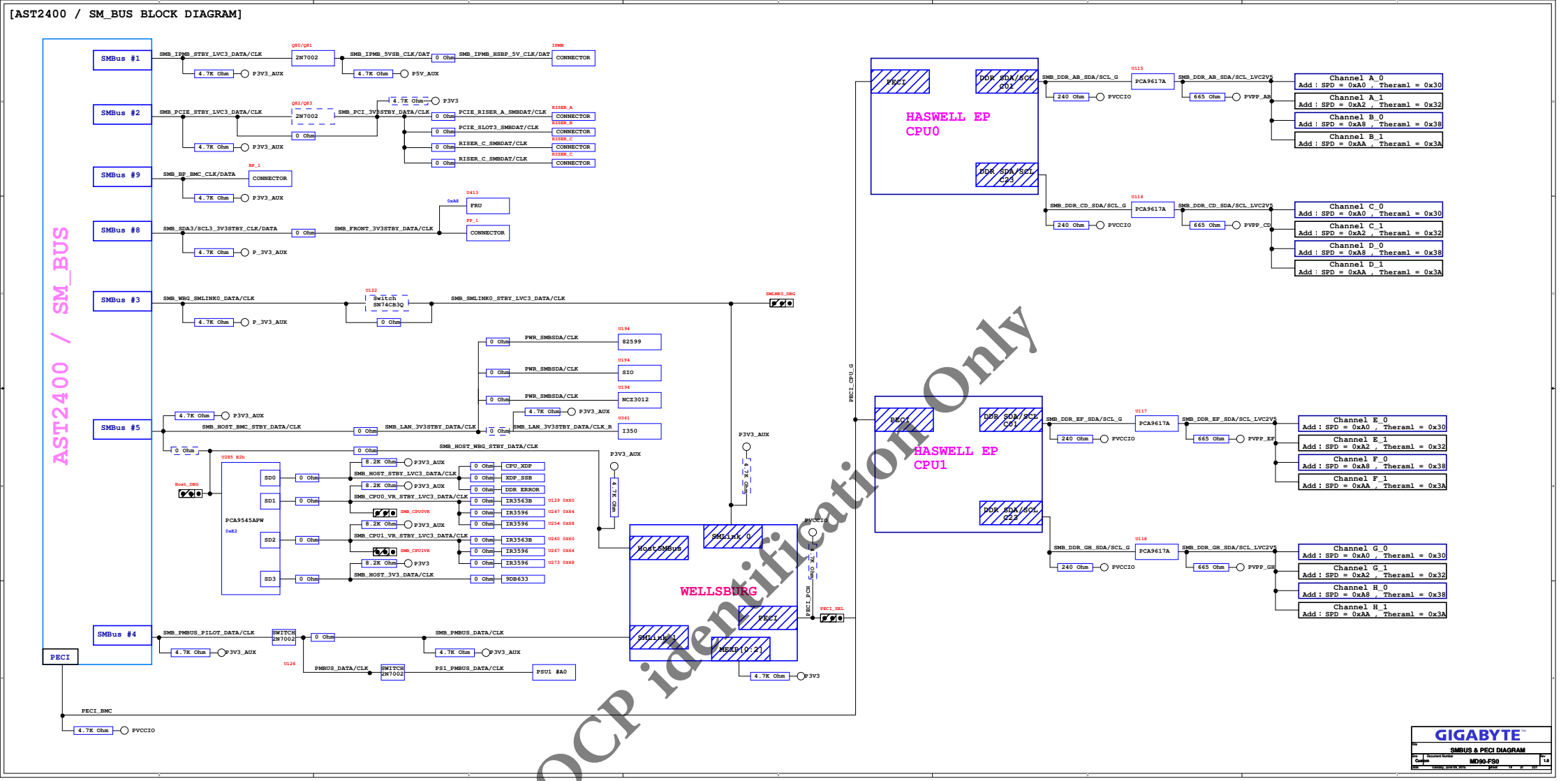
[AST2400 / SM_BUS BLOCK DIAGRAM]
AST2400 / SM_BUS
SMBus #1
SMBus #2
SMBus #9
SMBus #8
SMBus #3
SMBus #5
SMBus #4
PECI
SMB_IPMB_STBY_LVC3_DATA/CLK
2N7002
SMB_IPMB_5VSB_CLK/DAT
SMB_IPMB_HSBP_5V_CLK/DAT
CONNECTOR
SMB_PCIE_STBY_LVC3_DATA/CLK
SMB_PCI_3V3STBY_DATA/CLK
PCIE_RISER_A_SMBDAT/CLK
PCIE_SLOT3_SMBDAT/CLK
RISER_C_SMBDAT/CLK
SMB_BP_BMC_CLK/DATA
SMB_SDA3/SCL3_3V3STBY_CLK/DATA
SMB_FRONT_3V3STBY_DATA/CLK
FRU
SMB_WBG_SMLINK0_DATA/CLK
Switch SN74CB3Q
SMB_SMLINK0_STBY_LVC3_DATA/CLK
SMB_HOST_BMC_STBY_DATA/CLK
SMB_LAN_3V3STBY_DATA/CLK
SMB_LAN_3V3STBY_DATA/CLK_R
SMB_HOST_WBG_STBY_DATA/CLK
PWR_SMBSDA/CLK
82599
SIO
NCZ3012
I350
PCA9545APW
SD0
SD1
SD2
SD3
SMB_HOST_STBY_LVC3_DATA/CLK
SMB_CPU0_VR_STBY_LVC3_DATA/CLK
SMB_CPU1_VR_STBY_LVC3_DATA/CLK
SMB_HOST_3V3_DATA/CLK
CPU_XDP
XDP_SSB
DDR_ERROR
IR3563B
IR3596
9DB633
SMB_PMBUS_PILOT_DATA/CLK
SWITCH 2N7002
SMB_PMBUS_DATA/CLK
PMBUS_DATA/CLK
PS1_PMBUS_DATA/CLK
PSU1 #A0
PECI_BMC
P3V3_AUX
P5V_AUX
PVCCIO
WELLSBURG
HostSMBus
SMLink_0
SMLink_1
MEXP[0:2]
PECI_PCH
PECI_SEL
PECI_CPU_G
HASWELL EP CPU0
HASWELL EP CPU1
DDR_SDA/SCL C01
DDR_SDA/SCL C23
DDR_SDA/SCL C01
DDR_SDA/SCL C23
SMB_DDR_AB_SDA/SCL_G
SMB_DDR_CD_SDA/SCL_G
SMB_DDR_EF_SDA/SCL_G
SMB_DDR_GH_SDA/SCL_G
PCA9617A
SMB_DDR_AB_SDA/SCL_LVC2V5
SMB_DDR_CD_SDA/SCL_LVC2V5
SMB_DDR_EF_SDA/SCL_LVC2V5
SMB_DDR_GH_SDA/SCL_LVC2V5
PVPP_AB
PVPP_CD
PVPP_EF
PVPP_GH
Channel A_0 Add : SPD = 0xA0 , Theram1 = 0x30
Channel A_1 Add : SPD = 0xA2 , Theram1 = 0x32
Channel B_0 Add : SPD = 0xA8 , Theram1 = 0x38
Channel B_1 Add : SPD = 0xAA , Theram1 = 0x3A
Channel C_0 Add : SPD = 0xA0 , Theram1 = 0x30
Channel C_1 Add : SPD = 0xA2 , Theram1 = 0x32
Channel D_0 Add : SPD = 0xA8 , Theram1 = 0x38
Channel D_1 Add : SPD = 0xAA , Theram1 = 0x3A
Channel E_0 Add : SPD = 0xA0 , Theram1 = 0x30
Channel E_1 Add : SPD = 0xA2 , Theram1 = 0x32
Channel F_0 Add : SPD = 0xA8 , Theram1 = 0x38
Channel F_1 Add : SPD = 0xAA , Theram1 = 0x3A
Channel G_0 Add : SPD = 0xA0 , Theram1 = 0x30
Channel G_1 Add : SPD = 0xA2 , Theram1 = 0x32
Channel H_0 Add : SPD = 0xA8 , Theram1 = 0x38
Channel H_1 Add : SPD = 0xAA , Theram1 = 0x3A
GIGABYTE
SMBUS & PECI DIAGRAM
MD90-FS0
OCP identification Only

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Title

POWER SEQUENCE DIAGRAM

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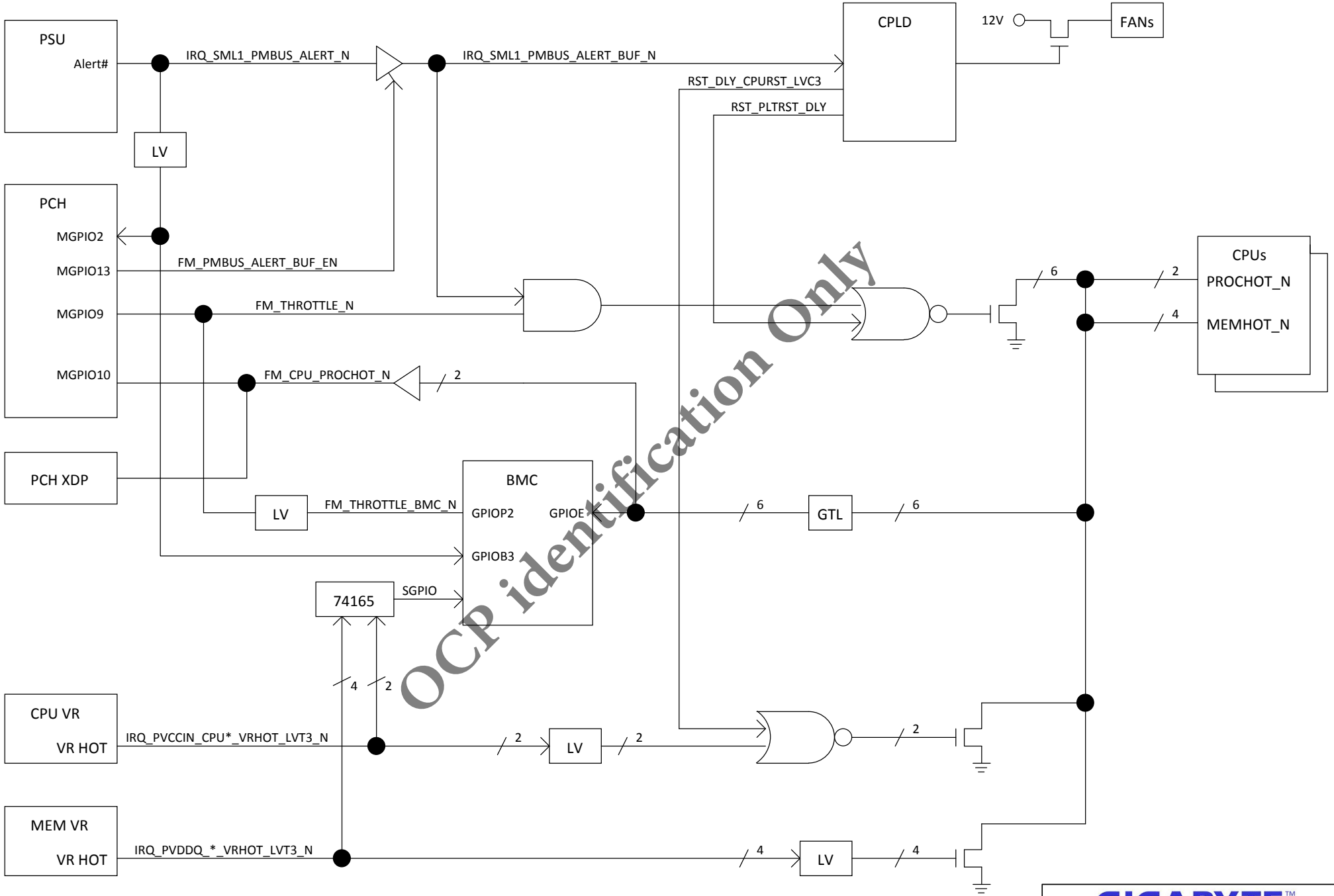

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Title: SmaRT&CLST		
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Title

========CPU0, CPU1========

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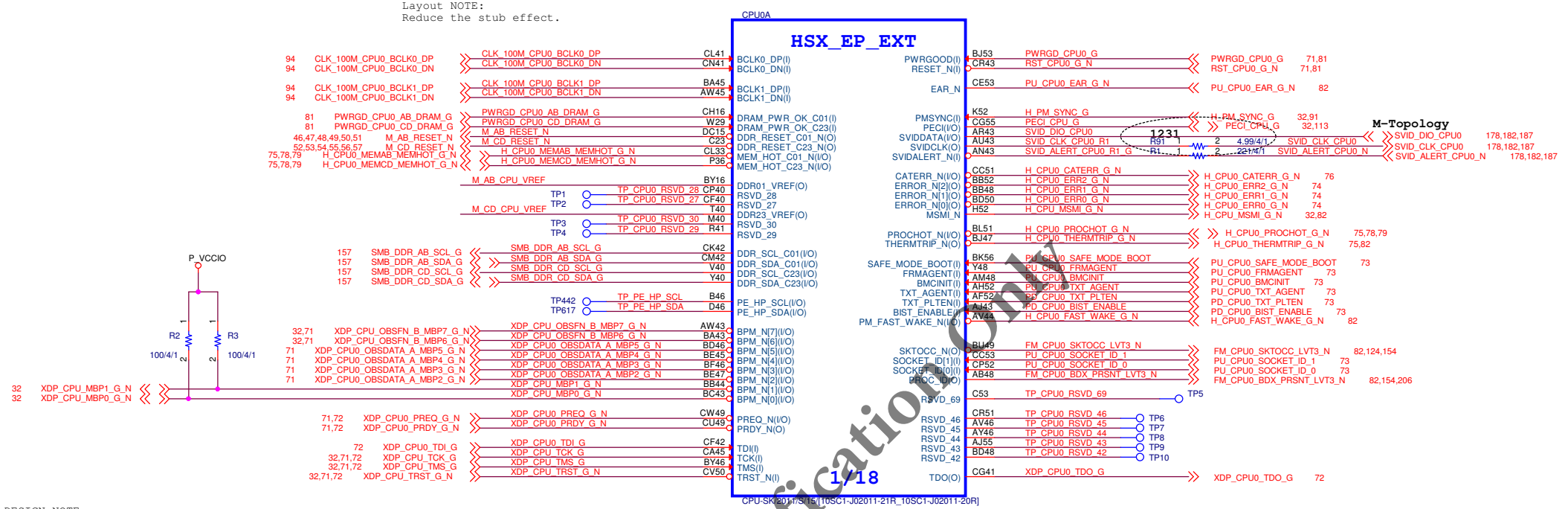
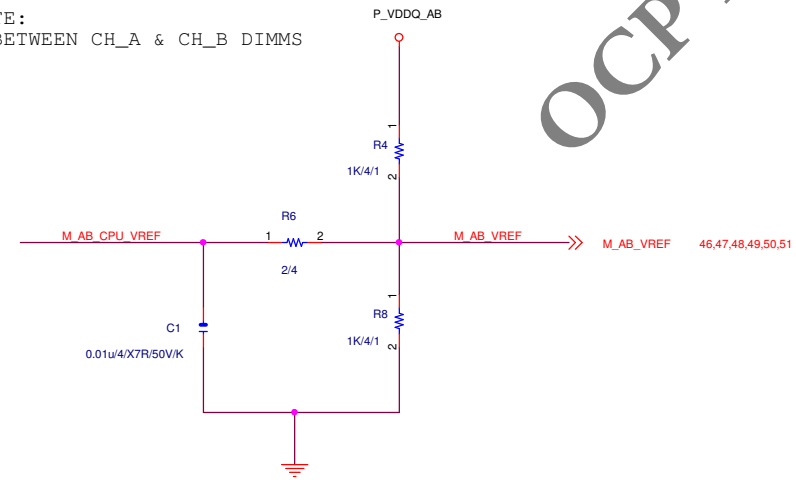
Layout NOTE:
Reduce the stub effect.

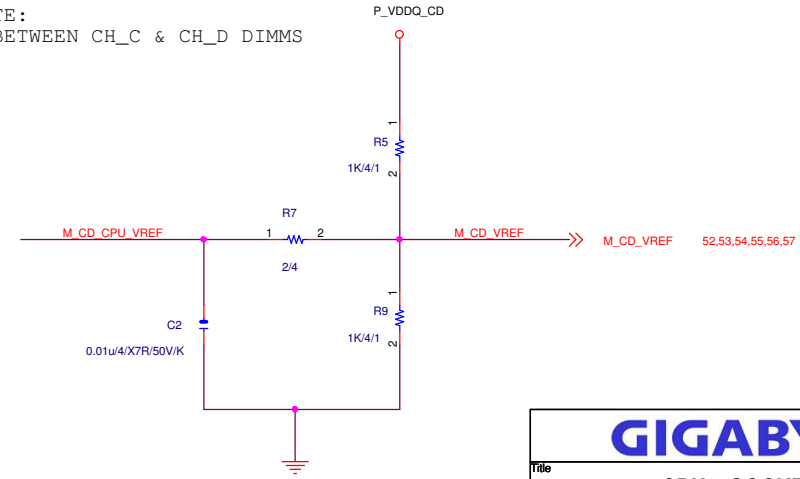


DESIGN NOTE:
If PEHPSCL and PEHPSDA are not used leave them unconnected.

CAD NOTE:
PLACE BETWEEN CH_A & CH_B DIMMS



CAD NOTE:
PLACE BETWEEN CH_C & CH_D DIMMS



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Title	CPU0_SOCKET(1/14)	
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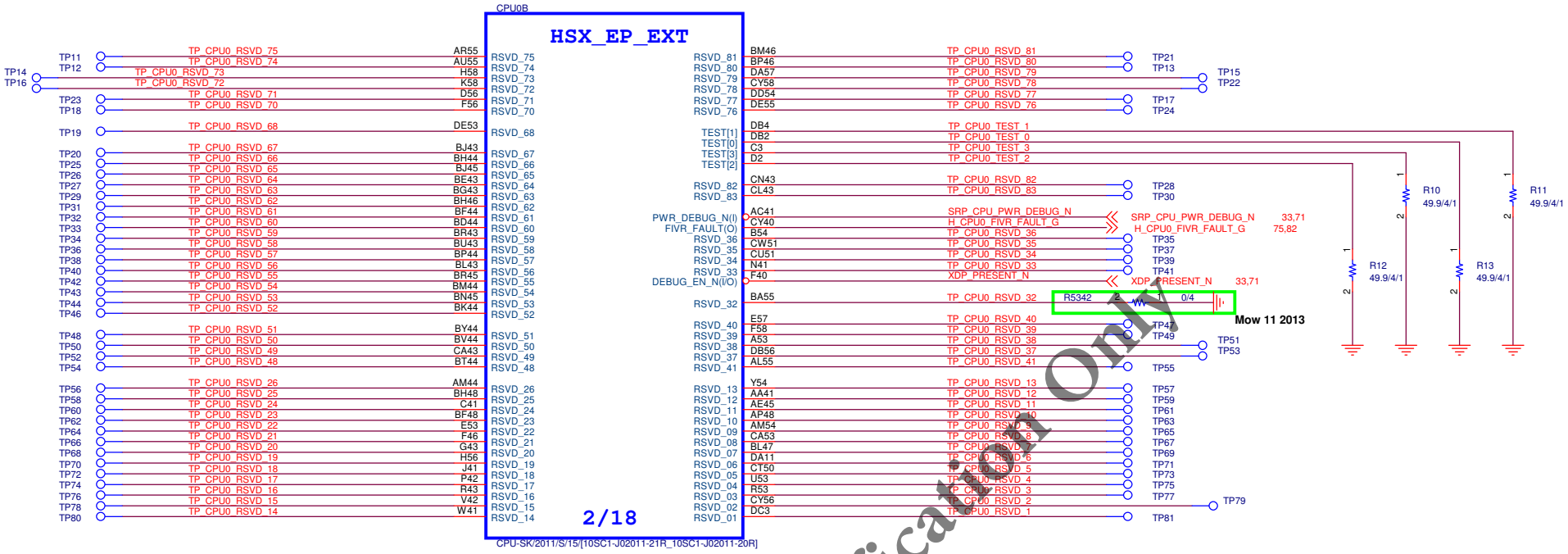
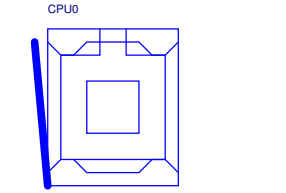
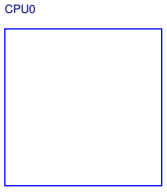
Date: Tuesday, June 09, 2015	Sheet 18 of 231	







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Title: CPU0_SOCKET(2/14)		
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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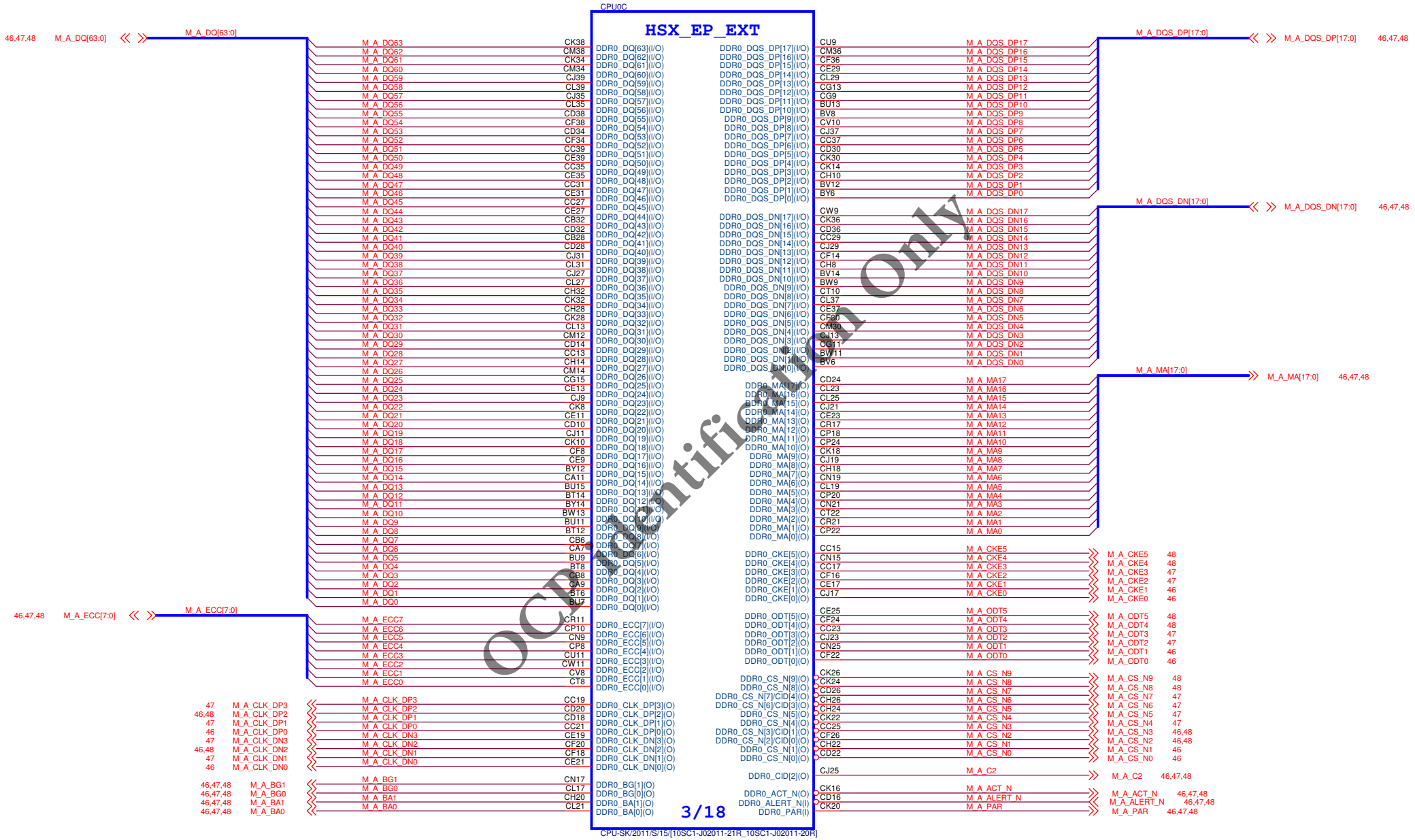

Title	CPU0_MEM_CH_A (3/14)
Size	Custom
Document Number	MD90-FS0
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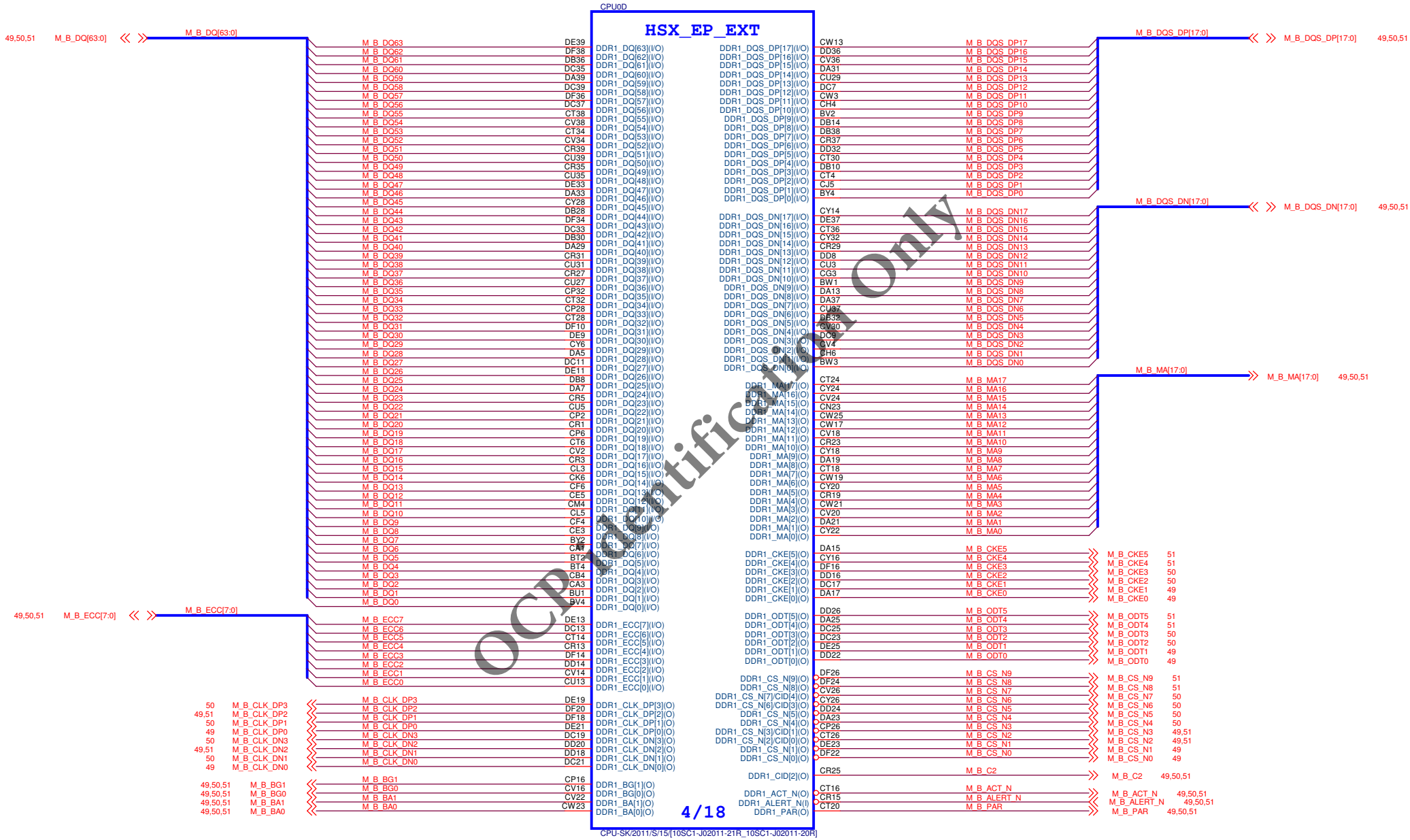

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Title	CPU0_MEM_CH_B (4/14)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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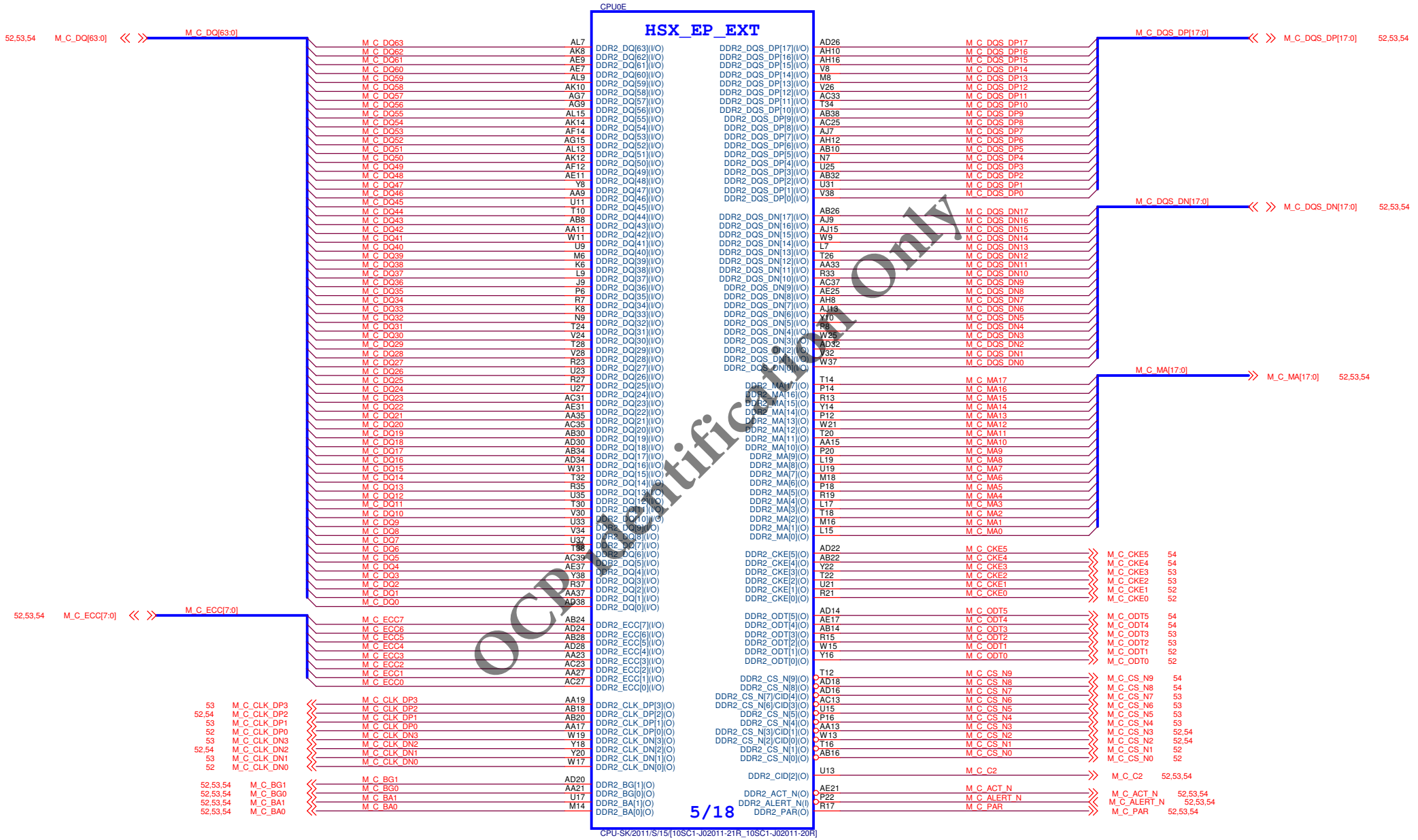

Title	CPU0_MEM_CH_C
Size	Custom
Document Number	MD90-FS0
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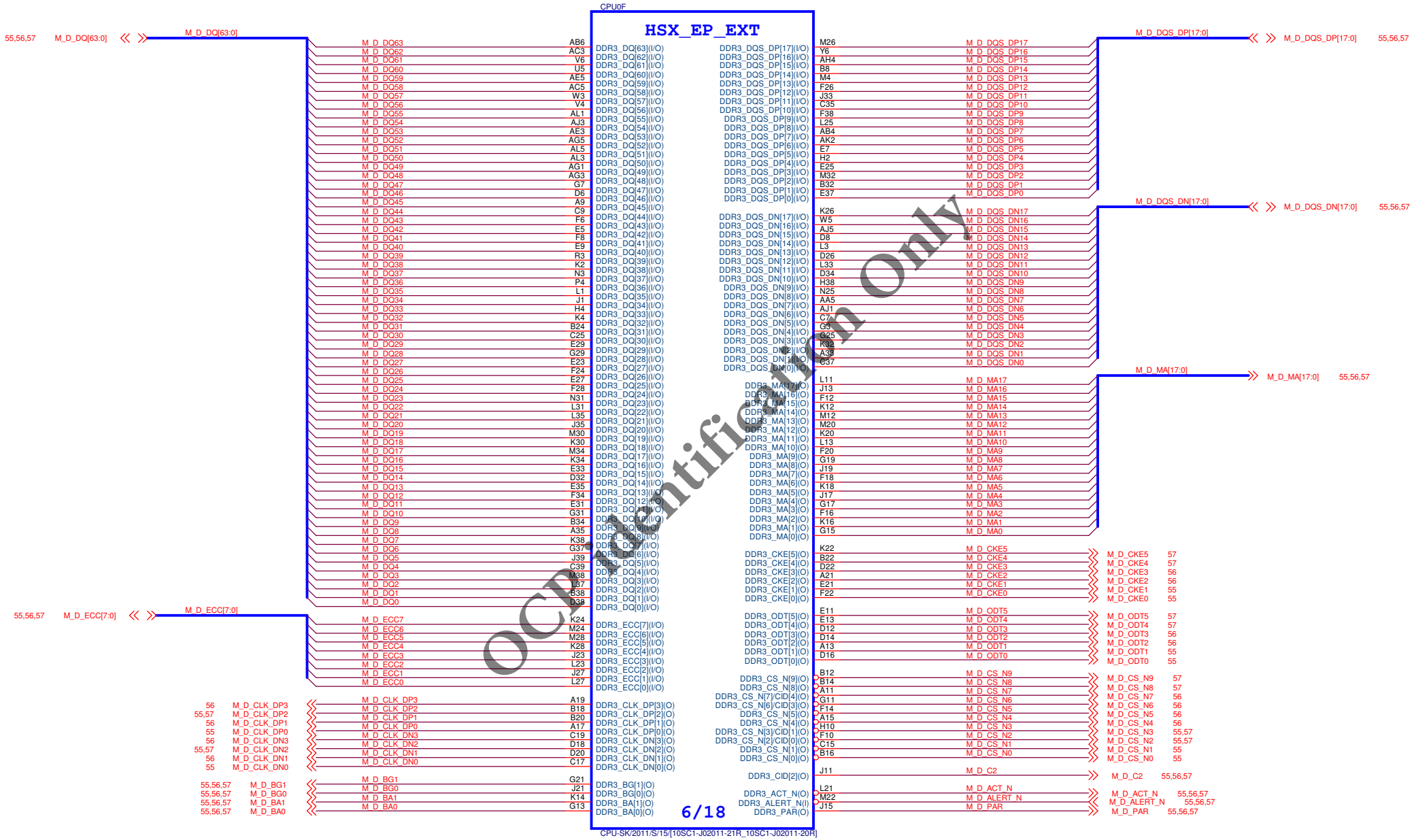

Title	CPU0_MEM_CH_D
Size	Custom
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90 DMI_CPU0_PCH_RX_C_DP[3:0] DMI_CPU0_PCH_RX_C_DP[3:0]

90 DMI_CPU0_PCH_RX_C_DN[3:0] DMI_CPU0_PCH_RX_C_DN[3:0]

DMI_CPU0_PCH_TX_C_DP[3:0] DMI_CPU0_PCH_TX_C_DP[3:0] 90

DMI_CPU0_PCH_TX_C_DN[3:0] DMI_CPU0_PCH_TX_C_DN[3:0] 90

Place AC CAP Close to CPU

Place AC CAP Close to CPU

CPU0G

HSX_EP_EXT

DMI_CPU0_PCH_RX_C_DP3	E47	DMI_RX_DP[3](I)	DMI_TX_DP[3](O)	D42	DMI_CPU0_PCH_TX_DP3	C4	0.1u/4/X7R/16V/K	DMI_CPU0_PCH_TX_C_DP3
DMI_CPU0_PCH_RX_C_DP2	D48	DMI_RX_DP[2](I)	DMI_TX_DP[2](O)	E43	DMI_CPU0_PCH_TX_DP2	C6	0.1u/4/X7R/16V/K	DMI_CPU0_PCH_TX_C_DP2
DMI_CPU0_PCH_RX_C_DP1	E49	DMI_RX_DP[1](I)	DMI_TX_DP[1](O)	D44	DMI_CPU0_PCH_TX_DP1	C8	0.1u/4/X7R/16V/K	DMI_CPU0_PCH_TX_C_DP1
DMI_CPU0_PCH_RX_C_DP0	D50	DMI_RX_DP[0](I)	DMI_TX_DP[0](O)	E45	DMI_CPU0_PCH_TX_DP0	C10	0.1u/4/X7R/16V/K	DMI_CPU0_PCH_TX_C_DP0
DMI_CPU0_PCH_RX_C_DN3	C47	DMI_RX_DN[3](I)	DMI_TX_DN[3](O)	B42	DMI_CPU0_PCH_TX_DN3	C12	0.1u/4/X7R/16V/K	DMI_CPU0_PCH_TX_C_DN3
DMI_CPU0_PCH_RX_C_DN2	B48	DMI_RX_DN[2](I)	DMI_TX_DN[2](O)	C43	DMI_CPU0_PCH_TX_DN2	C14	0.1u/4/X7R/16V/K	DMI_CPU0_PCH_TX_C_DN2
DMI_CPU0_PCH_RX_C_DN1	C49	DMI_RX_DN[1](I)	DMI_TX_DN[1](O)	B44	DMI_CPU0_PCH_TX_DN1	C16	0.1u/4/X7R/16V/K	DMI_CPU0_PCH_TX_C_DN1
DMI_CPU0_PCH_RX_C_DN0	B50	DMI_RX_DN[0](I)	DMI_TX_DN[0](O)	C45	DMI_CPU0_PCH_TX_DN0	C18	0.1u/4/X7R/16V/K	DMI_CPU0_PCH_TX_C_DN0
P3E_CPU0_NIC_RX_C_DP7	M56	PE1B_RX_DP[7](I)	PE1B_TX_DP[7](O)	L49	P3E_CPU0_NIC_TX_DP7			
P3E_CPU0_NIC_RX_C_DP6	L57	PE1B_RX_DP[6](I)	PE1B_TX_DP[6](O)	K48	P3E_CPU0_NIC_TX_DP6			
P3E_CPU0_NIC_RX_C_DP5	M54	PE1B_RX_DP[5](I)	PE1B_TX_DP[5](O)	L47	P3E_CPU0_NIC_TX_DP5			
P3E_CPU0_NIC_RX_C_DP4	L53	PE1B_RX_DP[4](I)	PE1B_TX_DP[4](O)	K46	P3E_CPU0_NIC_TX_DP4			
P3E_CPU0_NIC_RX_C_DN7	K56	PE1B_RX_DN[7](I)	PE1B_TX_DN[7](O)	J49	P3E_CPU0_NIC_TX_DN7			
P3E_CPU0_NIC_RX_C_DN6	J57	PE1B_RX_DN[6](I)	PE1B_TX_DN[6](O)	H48	P3E_CPU0_NIC_TX_DN6			
P3E_CPU0_NIC_RX_C_DN5	K54	PE1B_RX_DN[5](I)	PE1B_TX_DN[5](O)	J47	P3E_CPU0_NIC_TX_DN5			
P3E_CPU0_NIC_RX_C_DN4	J53	PE1B_RX_DN[4](I)	PE1B_TX_DN[4](O)	H46	P3E_CPU0_NIC_TX_DN4			
P3E_CPU0_NIC_RX_C_DP3	G55	PE1A_RX_DP[3](I)	PE1A_TX_DP[3](O)	L45	P3E_CPU0_NIC_TX_DP3			
P3E_CPU0_NIC_RX_C_DP2	F54	PE1A_RX_DP[2](I)	PE1A_TX_DP[2](O)	K44	P3E_CPU0_NIC_TX_DP2			
P3E_CPU0_NIC_RX_C_DP1	F52	PE1A_RX_DP[1](I)	PE1A_TX_DP[1](O)	L43	P3E_CPU0_NIC_TX_DP1			
P3E_CPU0_NIC_RX_C_DP0	E51	PE1A_RX_DP[0](I)	PE1A_TX_DP[0](O)	K42	P3E_CPU0_NIC_TX_DP0			
P3E_CPU0_NIC_RX_C_DN3	E55	PE1A_RX_DN[3](I)	PE1A_TX_DN[3](O)	J45	P3E_CPU0_NIC_TX_DN3			
P3E_CPU0_NIC_RX_C_DN2	D54	PE1A_RX_DN[2](I)	PE1A_TX_DN[2](O)	H44	P3E_CPU0_NIC_TX_DN2			
P3E_CPU0_NIC_RX_C_DN1	D52	PE1A_RX_DN[1](I)	PE1A_TX_DN[1](O)	J43	P3E_CPU0_NIC_TX_DN1			
P3E_CPU0_NIC_RX_C_DN0	C51	PE1A_RX_DN[0](I)	PE1A_TX_DN[0](O)	H42	P3E_CPU0_NIC_TX_DN0			

7/18

CPU-SK/2011/S/15/[10SC1-J02011-21R_10SC1-J02011-20R]

X540

142 P3E_CPU0_NIC_RX_C_DP[7:0] P3E_CPU0_NIC_RX_C_DP[7:0]

142 P3E_CPU0_NIC_RX_C_DN[7:0] P3E_CPU0_NIC_RX_C_DN[7:0]

P3E_CPU0_NIC_TX_DP[7:0] P3E_CPU0_NIC_TX_DP[7:0] 142

P3E_CPU0_NIC_TX_DN[7:0] P3E_CPU0_NIC_TX_DN[7:0] 142

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Title: CPU0_DMI_PE1 (7/14)

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PCIEx16 SLOT1

84 P3E_CPU0_PCIE1_1_RX_DP[15:0] >> P3E_CPU0_PCIE1_1_RX_DP[15:0]

84 P3E_CPU0_PCIE1_1_RX_DN[15:0] >> P3E_CPU0_PCIE1_1_RX_DN[15:0]

P3E_CPU0_PCIE1_1_TX_DP[15:0] >> P3E_CPU0_PCIE1_1_TX_DP[15:0] 84

P3E_CPU0_PCIE1_1_TX_DN[15:0] >> P3E_CPU0_PCIE1_1_TX_DN[15:0] 84

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Title	CPU0_PE2 (8/14)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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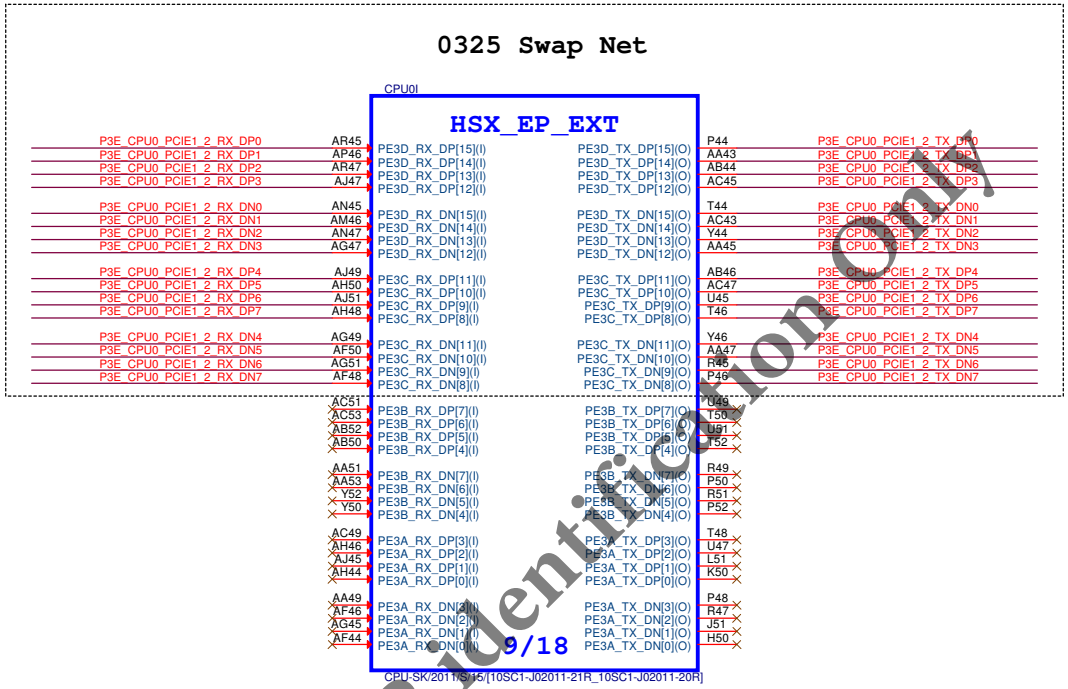

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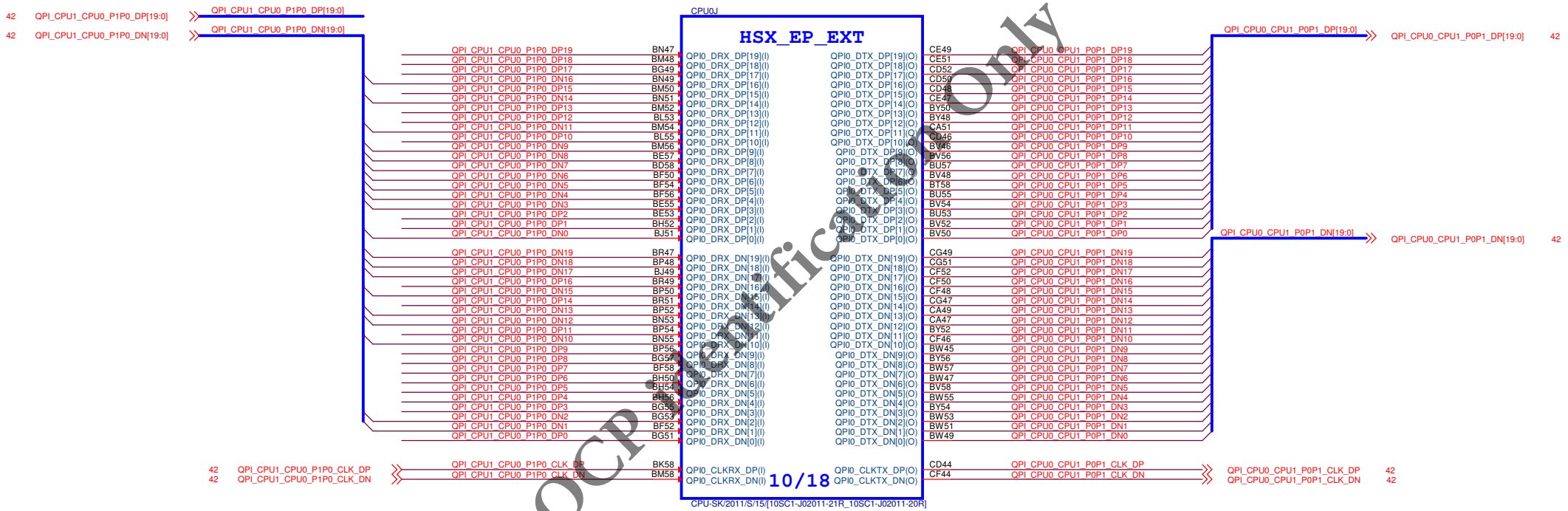
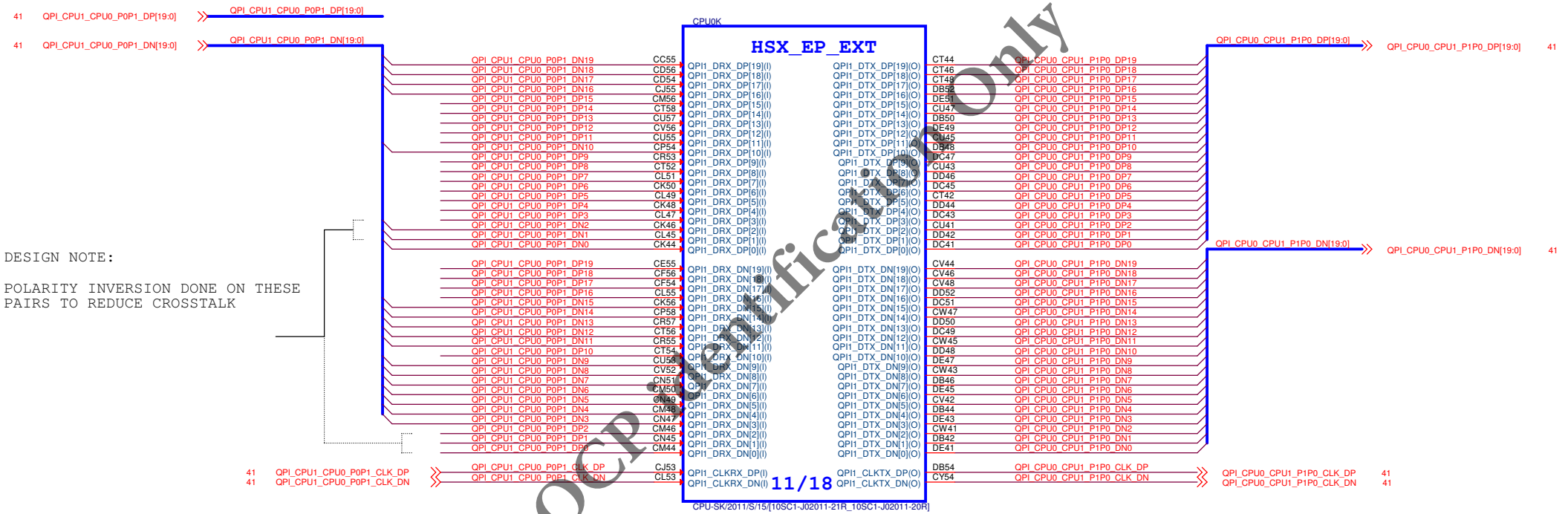
Title	CPU0_PE3 (9/14)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 26 of 231	

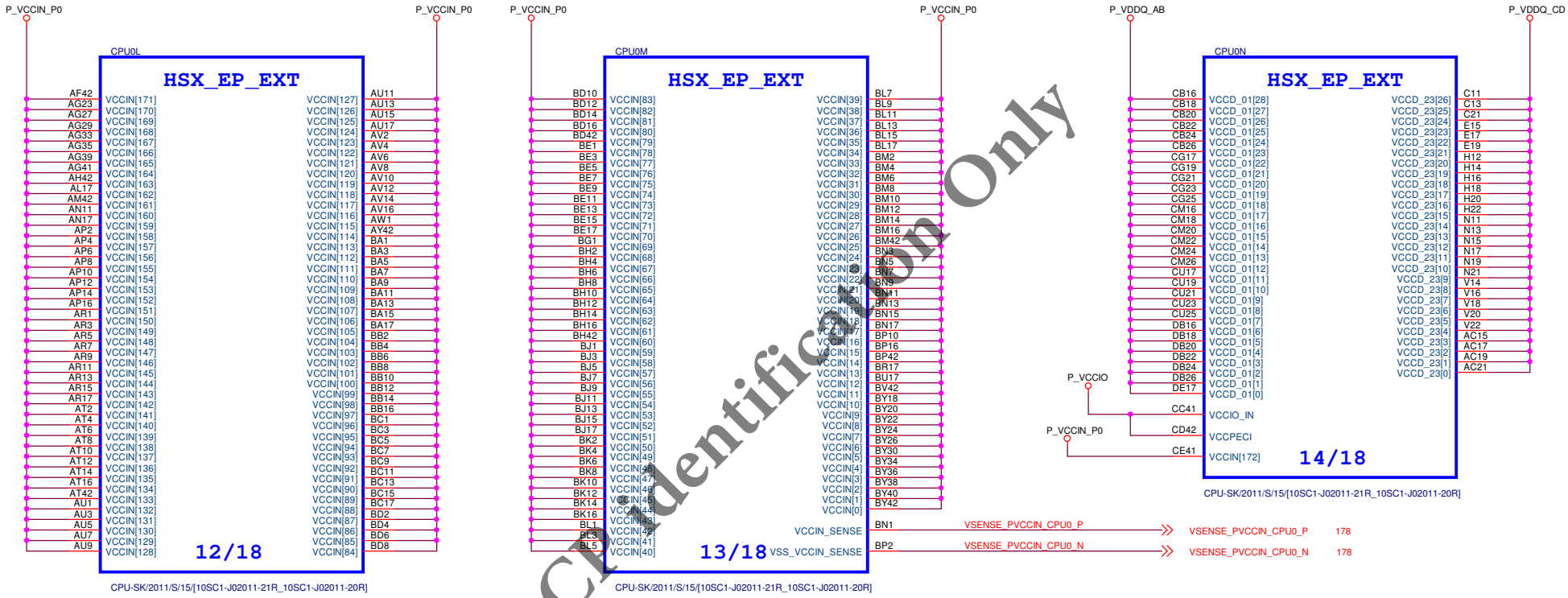


GIGABYTE™

Title	CPU0_QPI (10/14)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 27 of 231	



Title	CPU0_QPI (11/14)		
Size: Custom	Document Number: MD90-FS0		Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 28 of 231		



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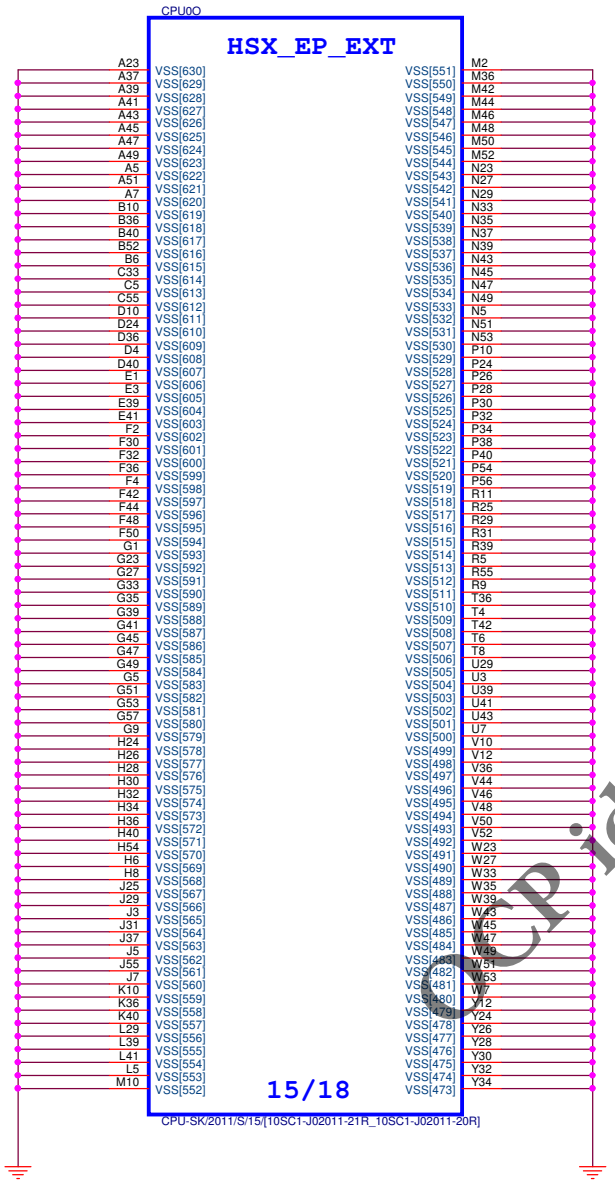
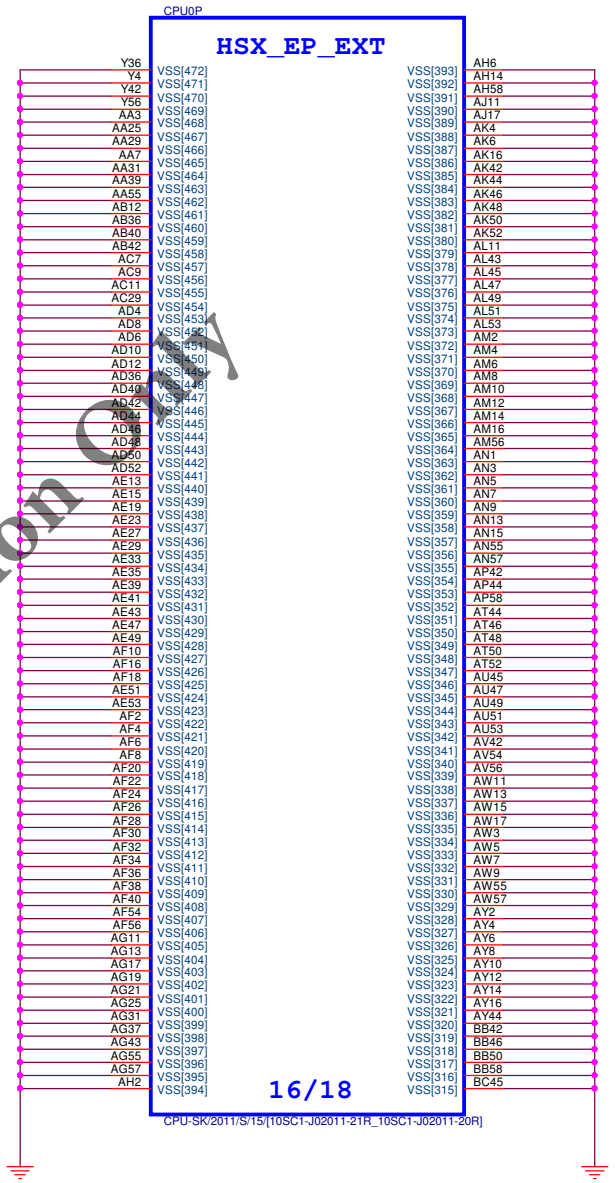
Title: CPU0_POWER (12/14)

Size: Custom | Document Number: MD90-FS0 | Rev: 1.0

Date: Tuesday, June 09, 2015 | Sheet 29 of 231





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Title: CPU0_GND (13/14)

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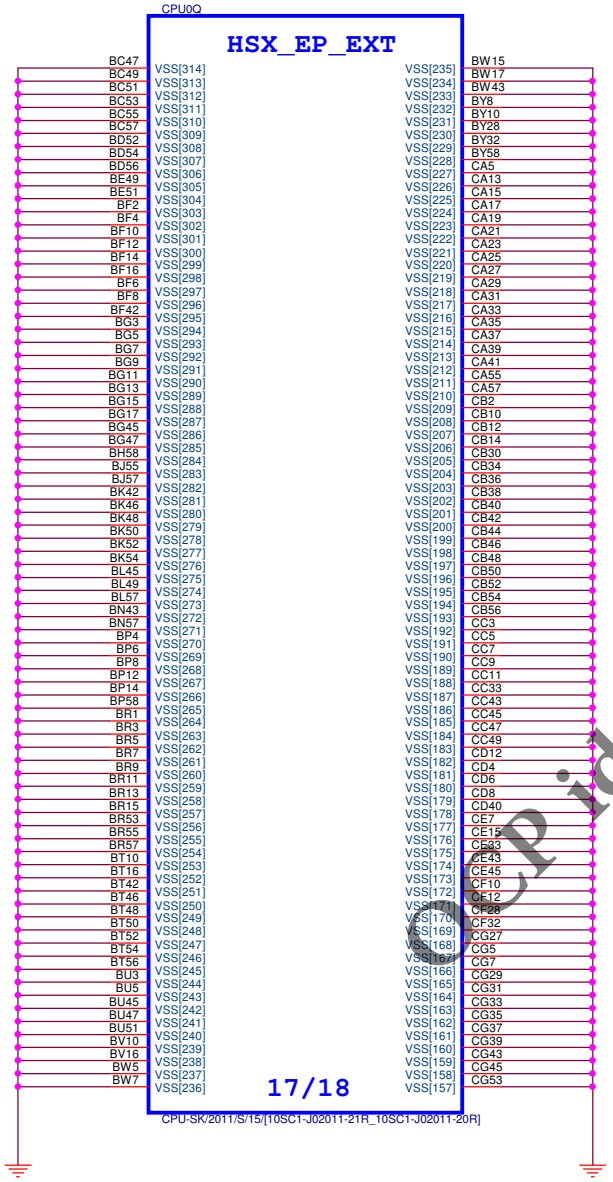

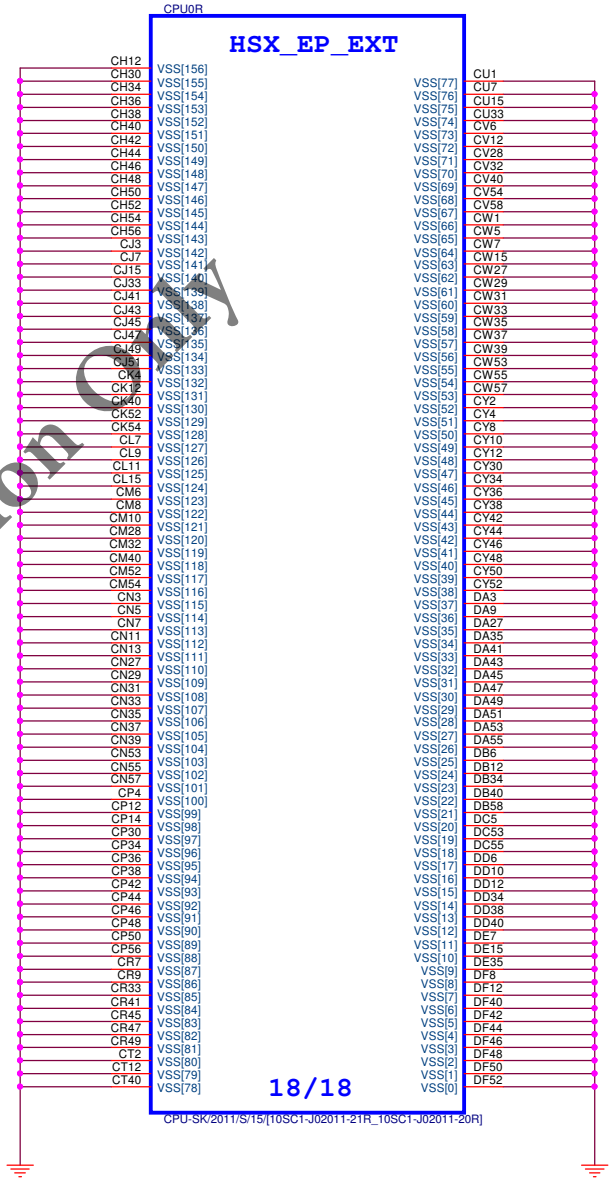

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Title	CPU0_GND (14/14)	
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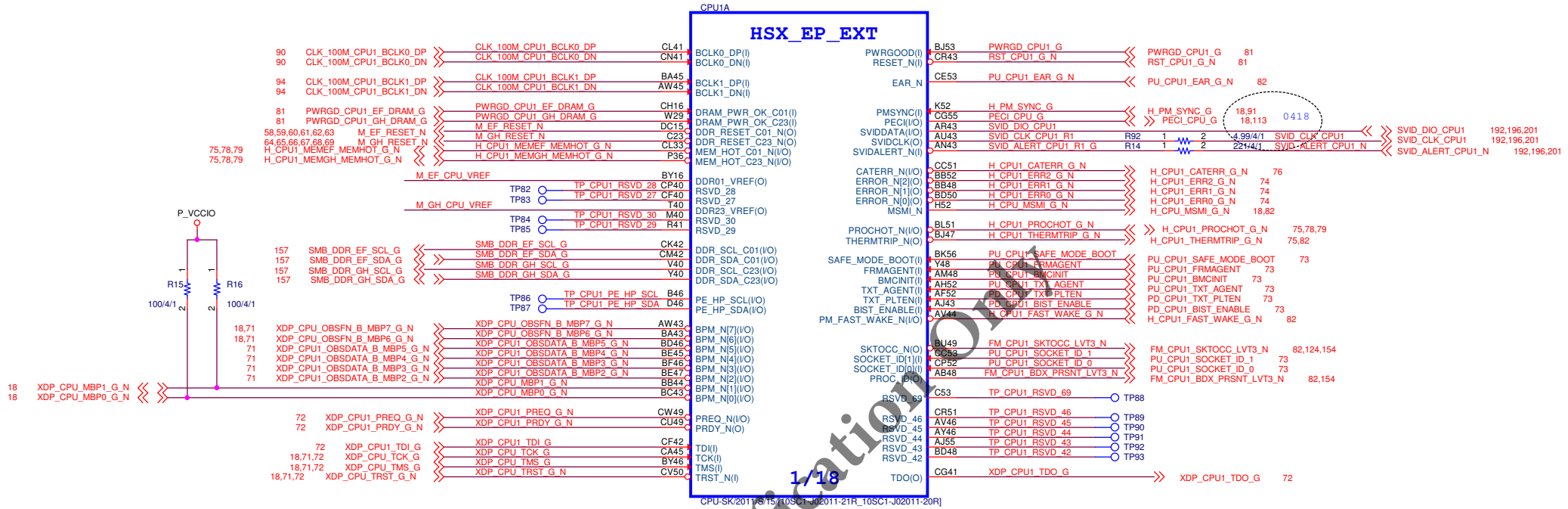
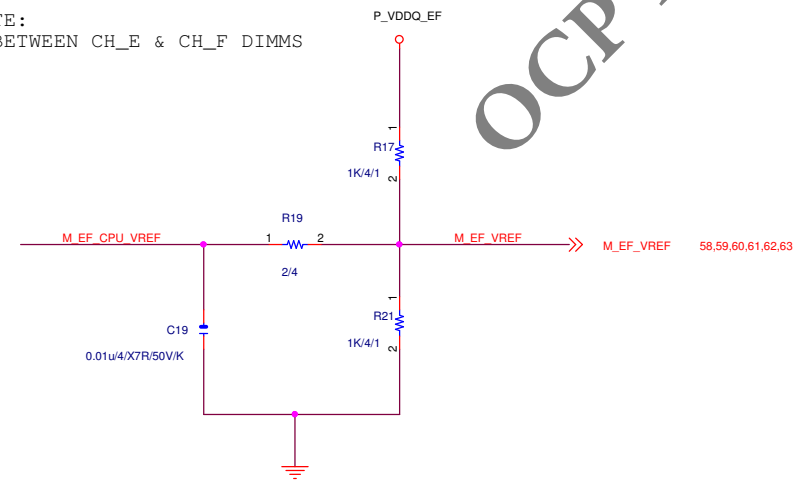
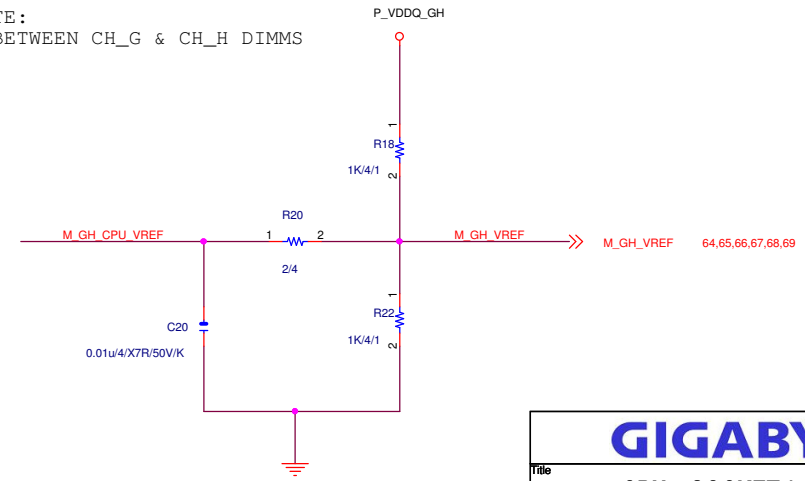
Layout NOTE:
Reduce the stub effect.



CAD NOTE:
PLACE BETWEEN CH_E & CH_F DIMMS



CAD NOTE:
PLACE BETWEEN CH_G & CH_H DIMMS



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Title: CPU1_SOCKET (1/14)

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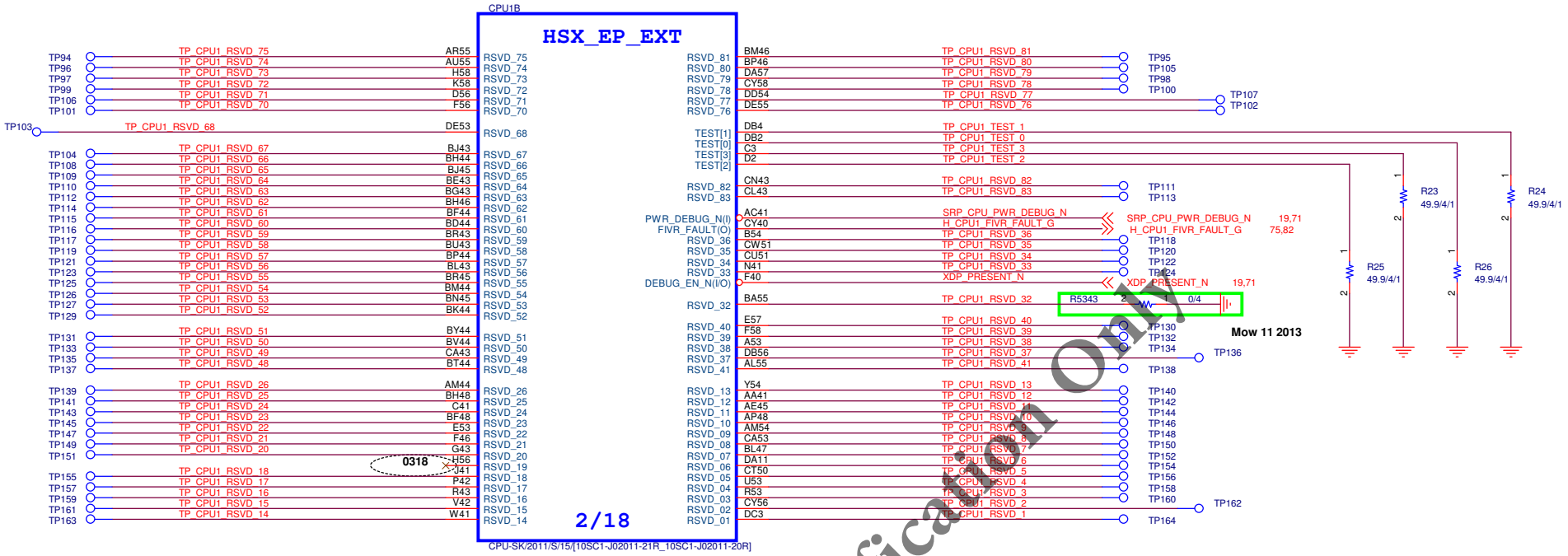

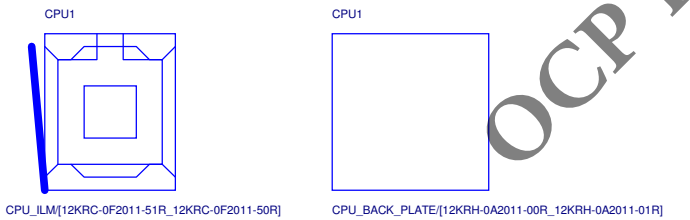

GIGABYTE™

Title: CPU1_SOCKET (2/14)		
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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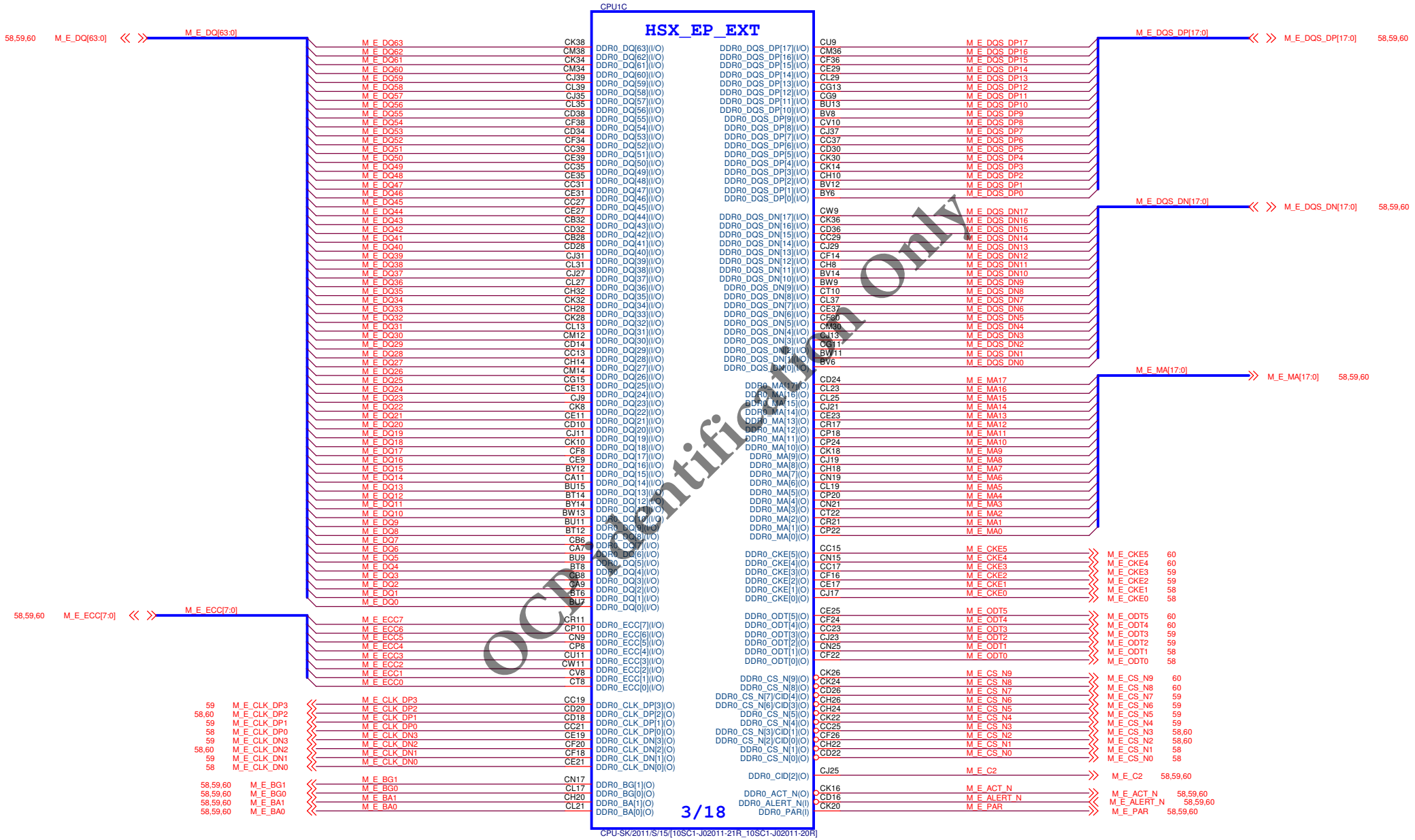

Title	CPU1_MEM_CH_E (3/14)
Size	Custom
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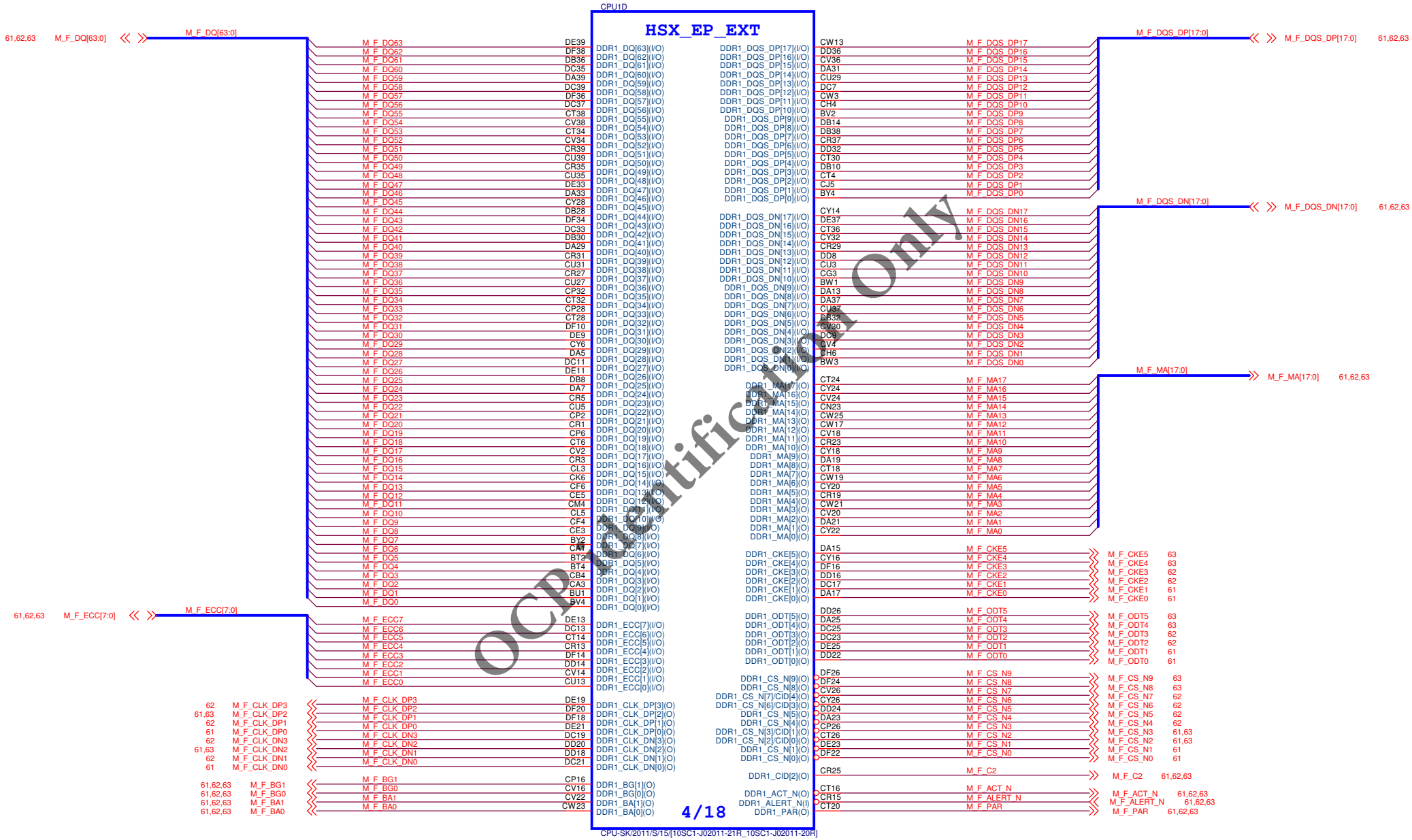

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Title	CPU1_MEM_CH_F (4/14)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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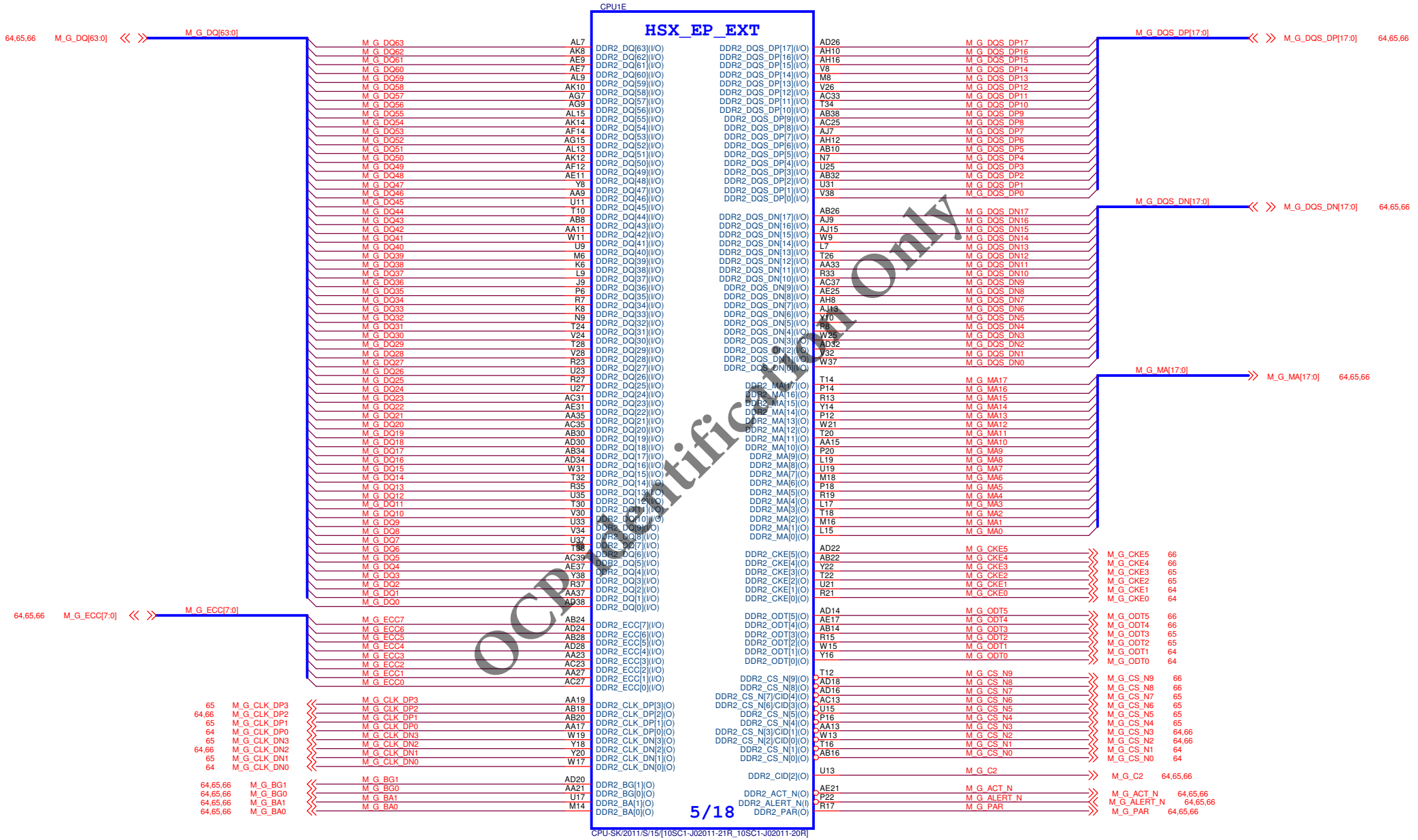

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Title	CPU1_MEM_CH_G (5/14)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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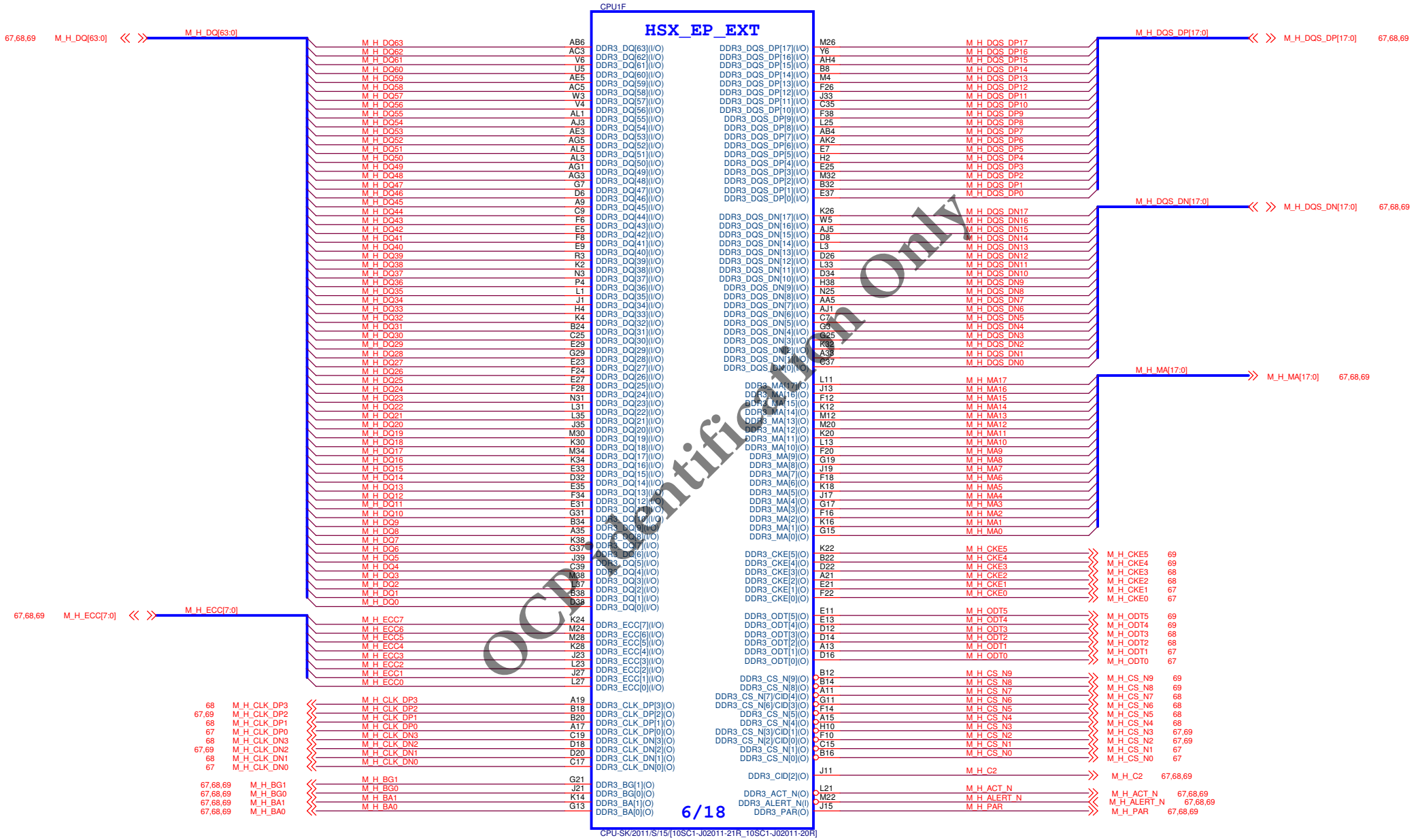

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Title: CPU1_MEM_CH_H (6/14)

Size: Custom | Document Number: MD90-FS0 | Rev: 1.0

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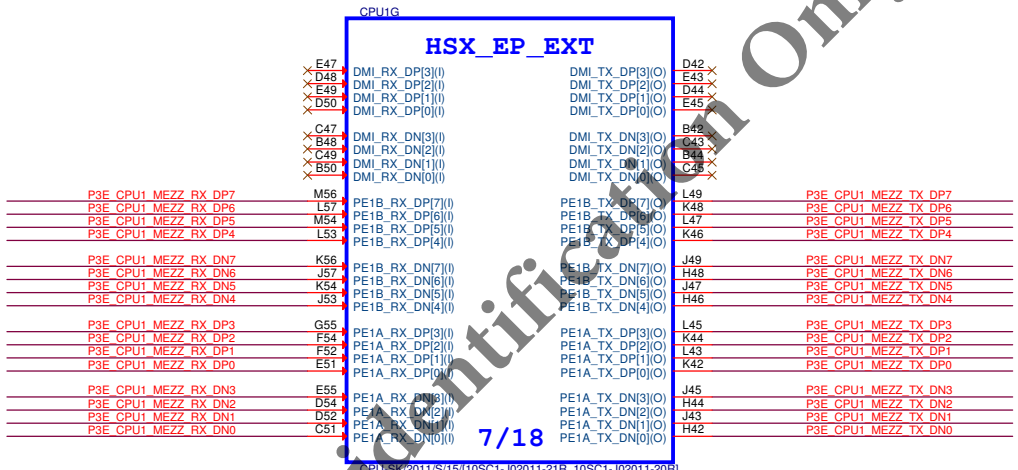

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Title: CPU1_DMI_PE1 (7/14)

Size: Custom | Document Number: MD90-FS0 | Rev: 1.0

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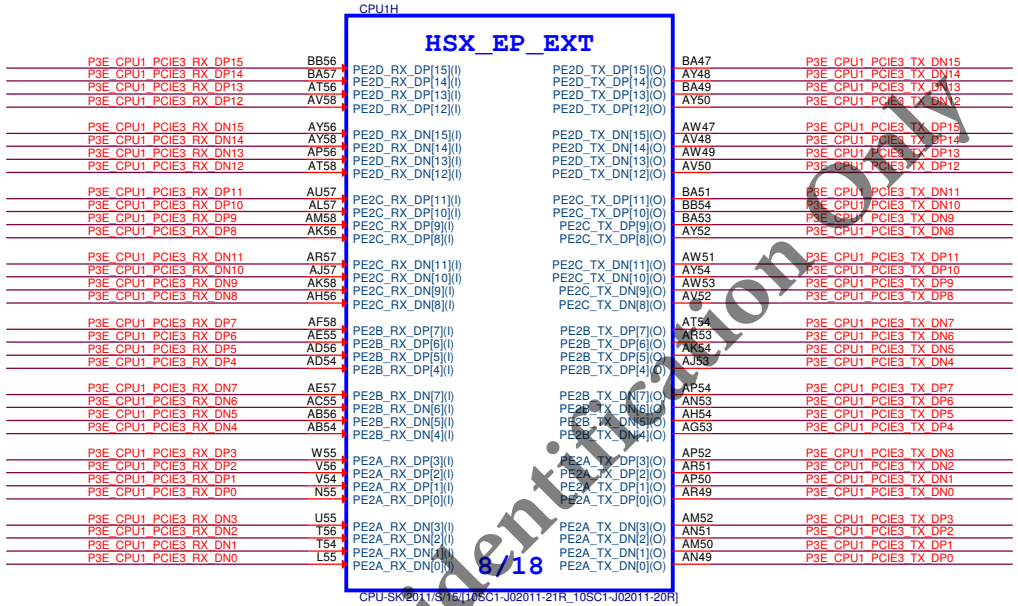

86 P3E_CPU1_PCIE3_RX_DN[15:0] >> P3E_CPU1_PCIE3_RX_DN[15:0]

86 P3E_CPU1_PCIE3_RX_DP[15:0] >> P3E_CPU1_PCIE3_RX_DP[15:0]

P3E_CPU1_PCIE3_TX_DP[15:0] >> P3E_CPU1_PCIE3_TX_DP[15:0] 86

P3E_CPU1_PCIE3_TX_DN[15:0] >> P3E_CPU1_PCIE3_TX_DN[15:0] 86

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Title	CPU1_PE2 (8/14)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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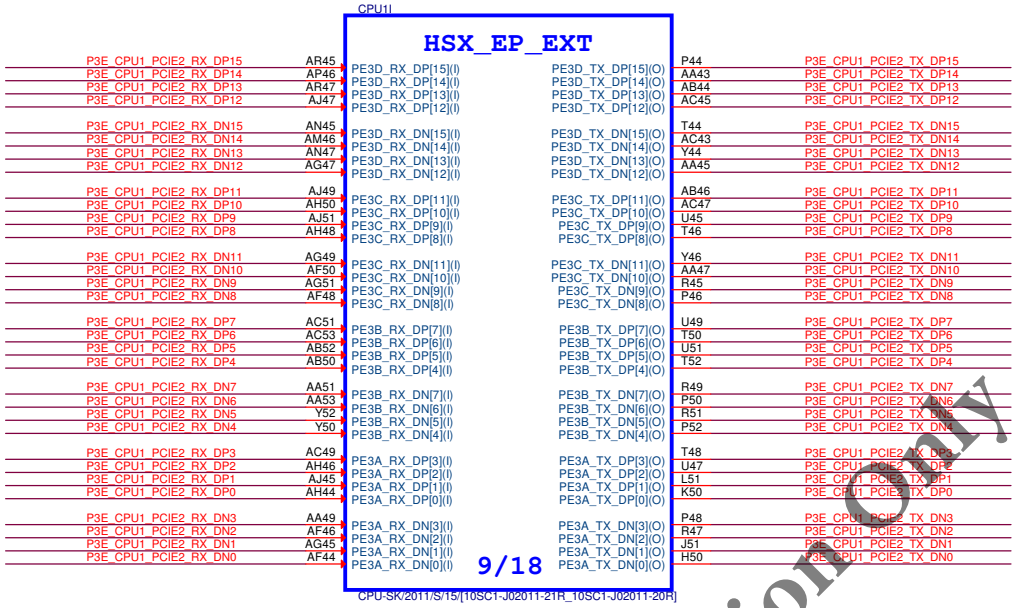

85 P3E_CPU1_PCIE2_RX_DN[15:0] >> P3E_CPU1_PCIE2_RX_DN[15:0]

85 P3E_CPU1_PCIE2_RX_DP[15:0] >> P3E_CPU1_PCIE2_RX_DP[15:0]

P3E_CPU1_PCIE2_TX_DP[15:0] >> P3E_CPU1_PCIE2_TX_DP[15:0] 85

P3E_CPU1_PCIE2_TX_DN[15:0] >> P3E_CPU1_PCIE2_TX_DN[15:0] 85

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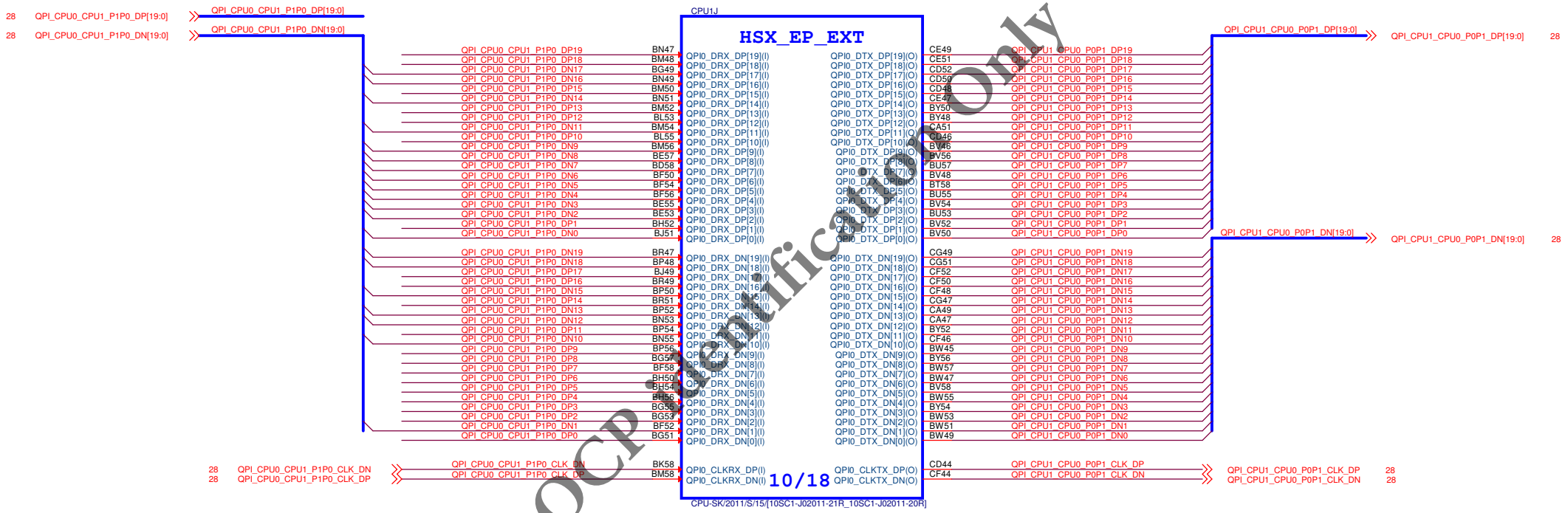
Title	CPU1_PE3 (9/14)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 40 of 231	



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Title	CPU1_QPI (10/14)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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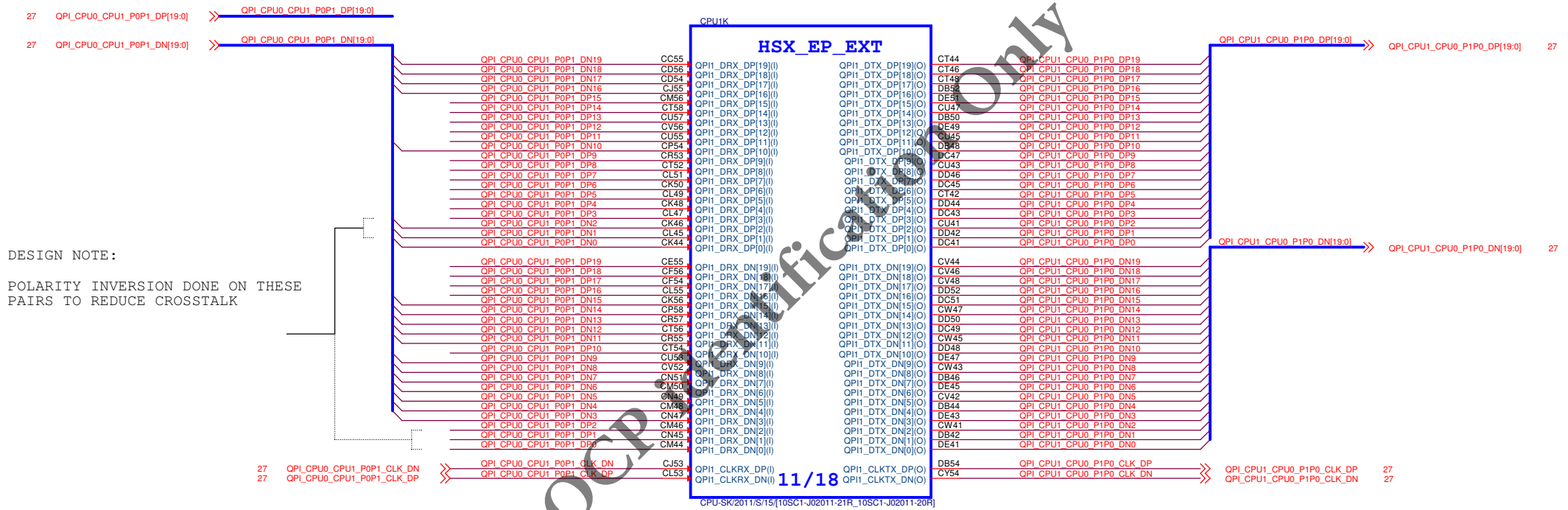

GIGABYTE™		
Title: CPU1_QPI (11/14)		
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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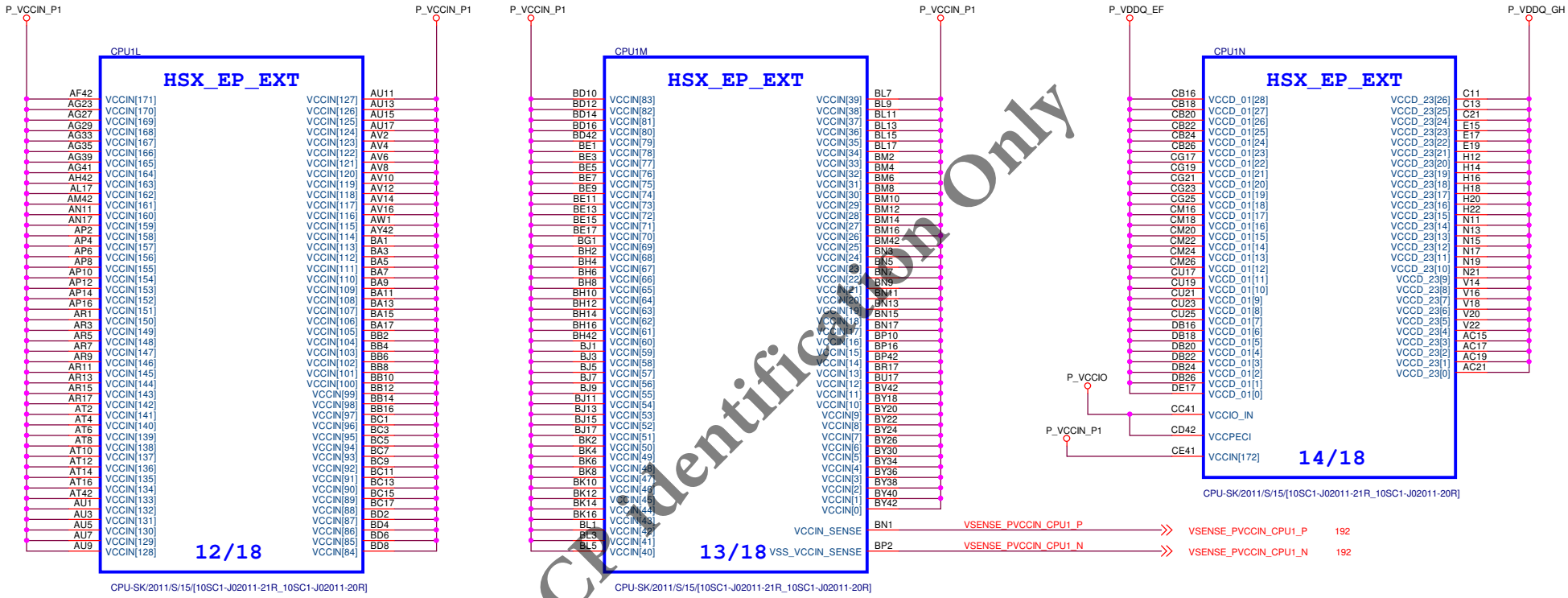

GIGABYTE™

Title: CPU1_POWER (12/14)

Size: Custom | Document Number: MD90-FS0 | Rev: 1.0

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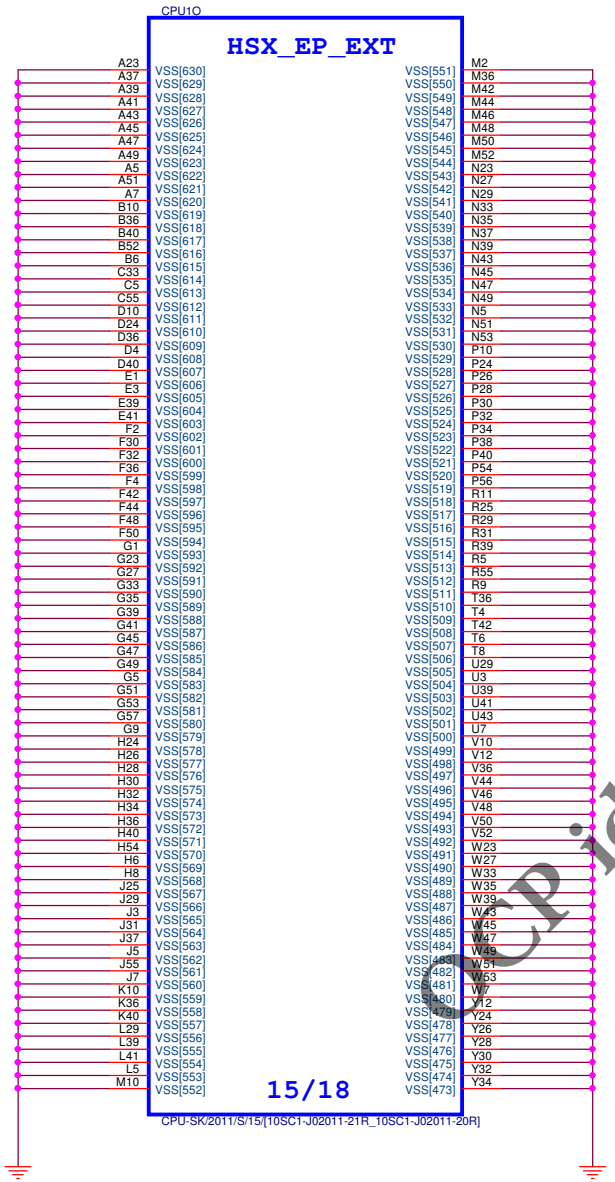

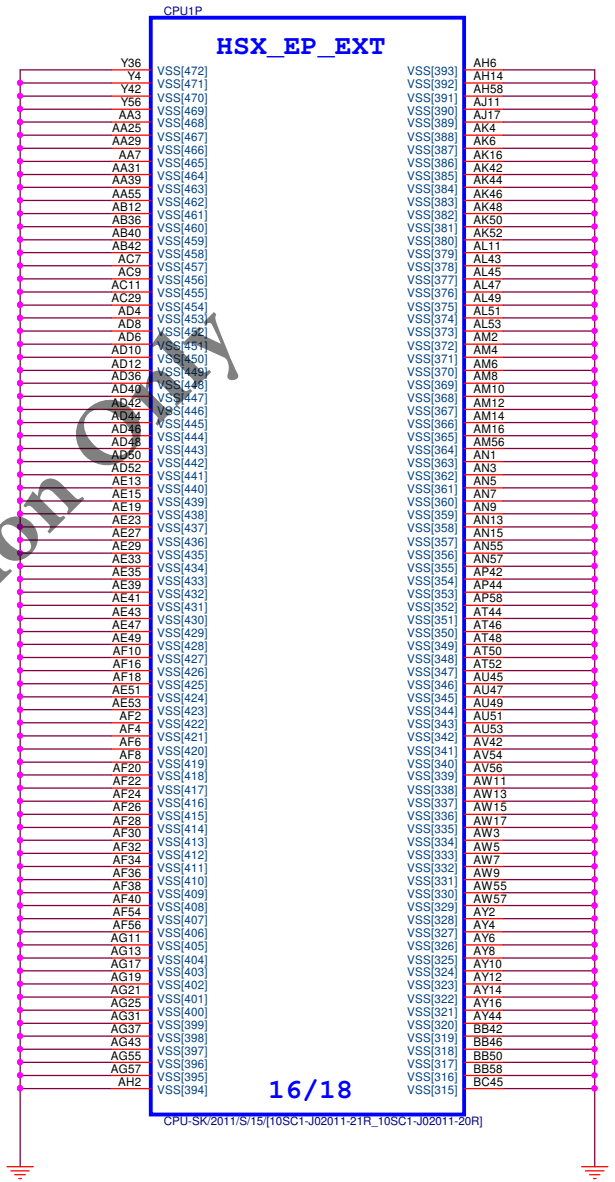

GIGABYTE™

Title	CPU1_GND (13/14)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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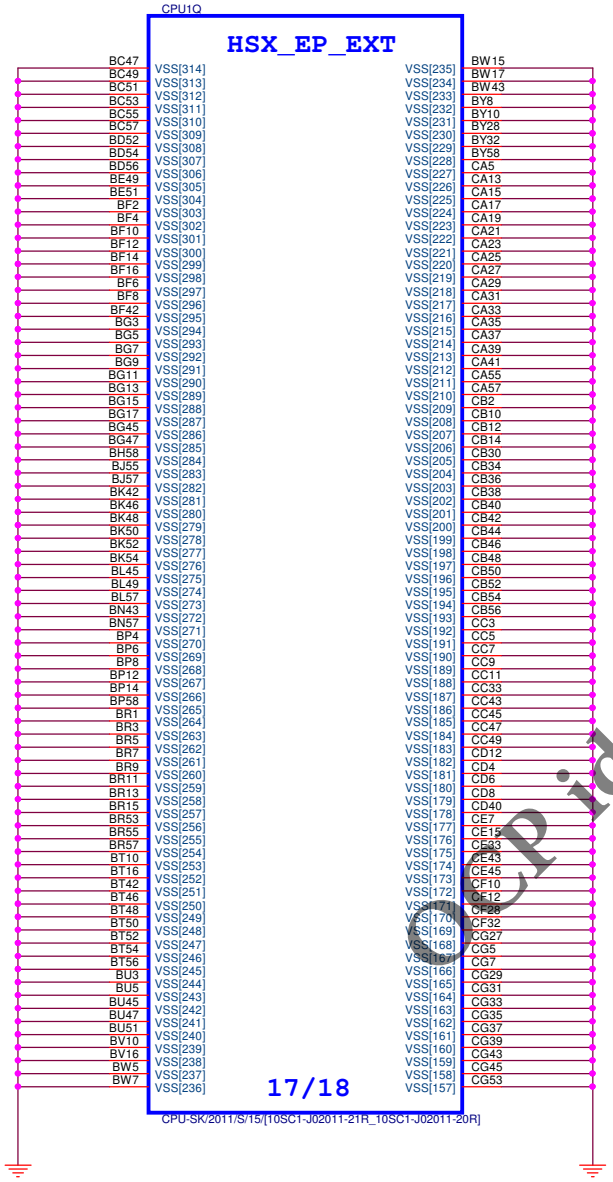

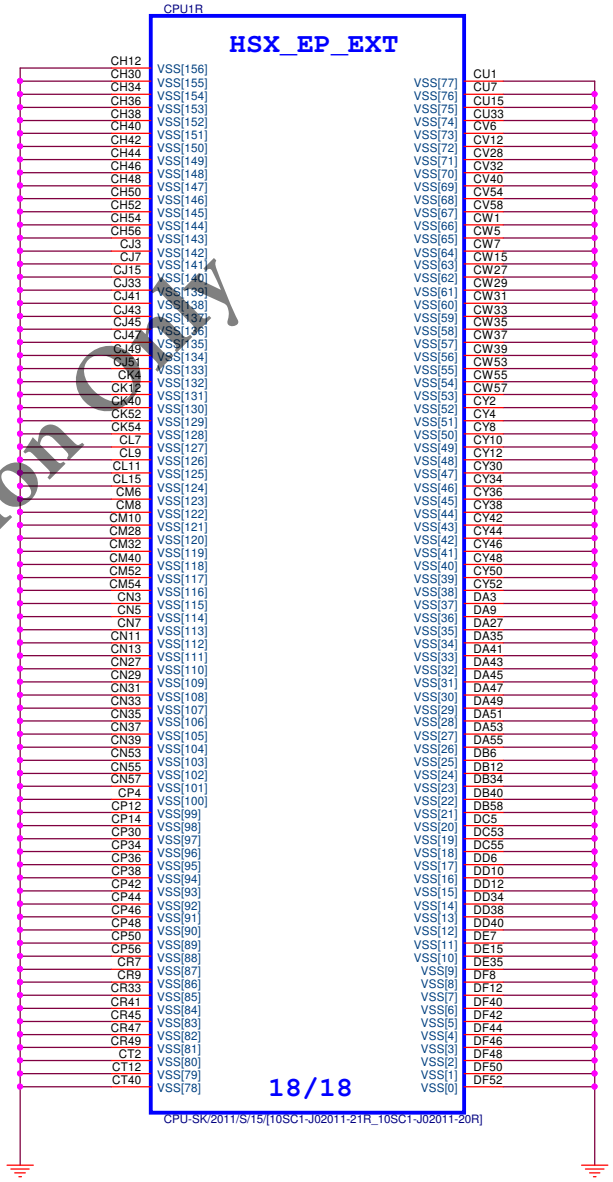

GIGABYTE™

Title	CPU1_GND (14/14)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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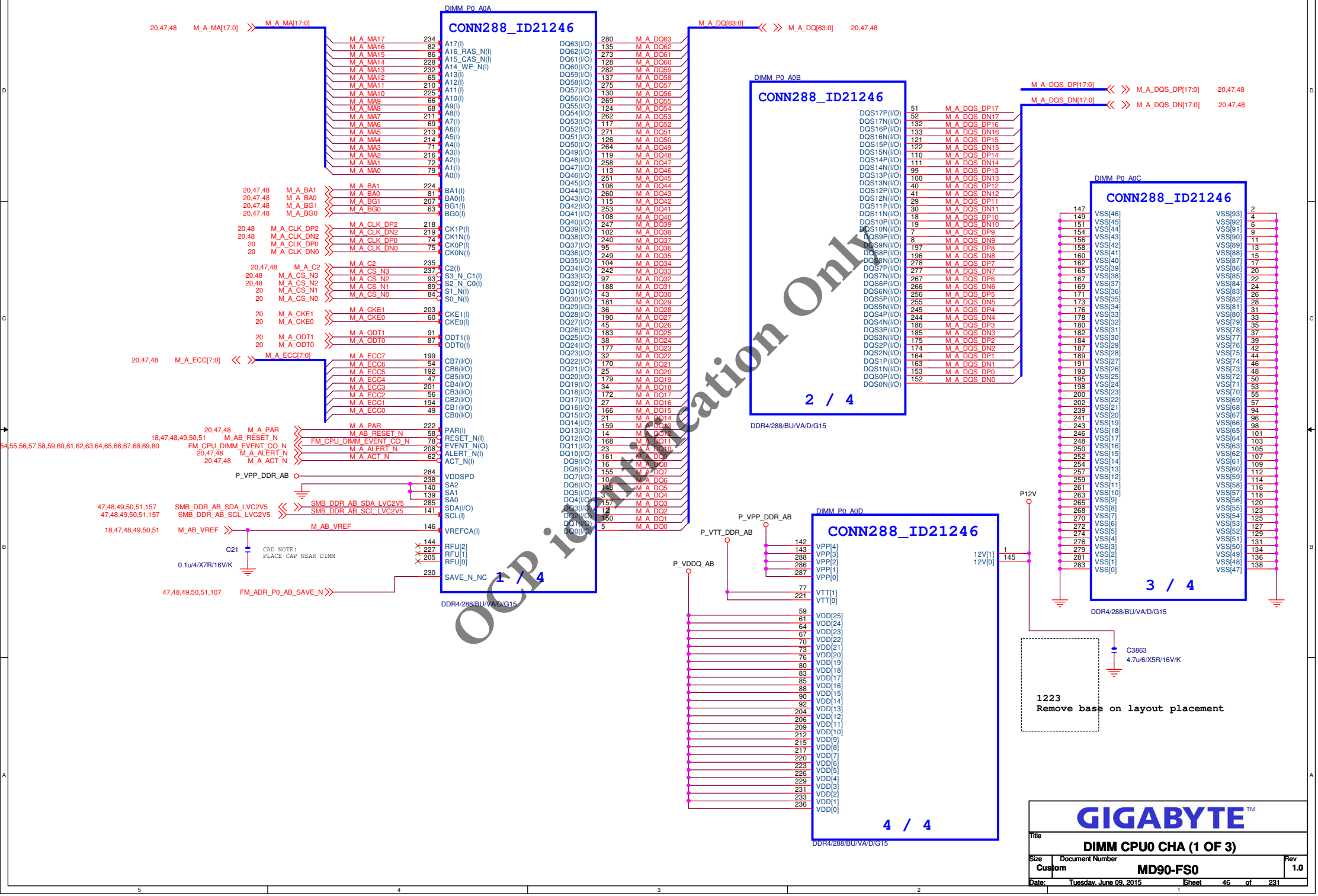

GIGABYTE™

Title	DIMM CPU0 CHA (1 OF 3)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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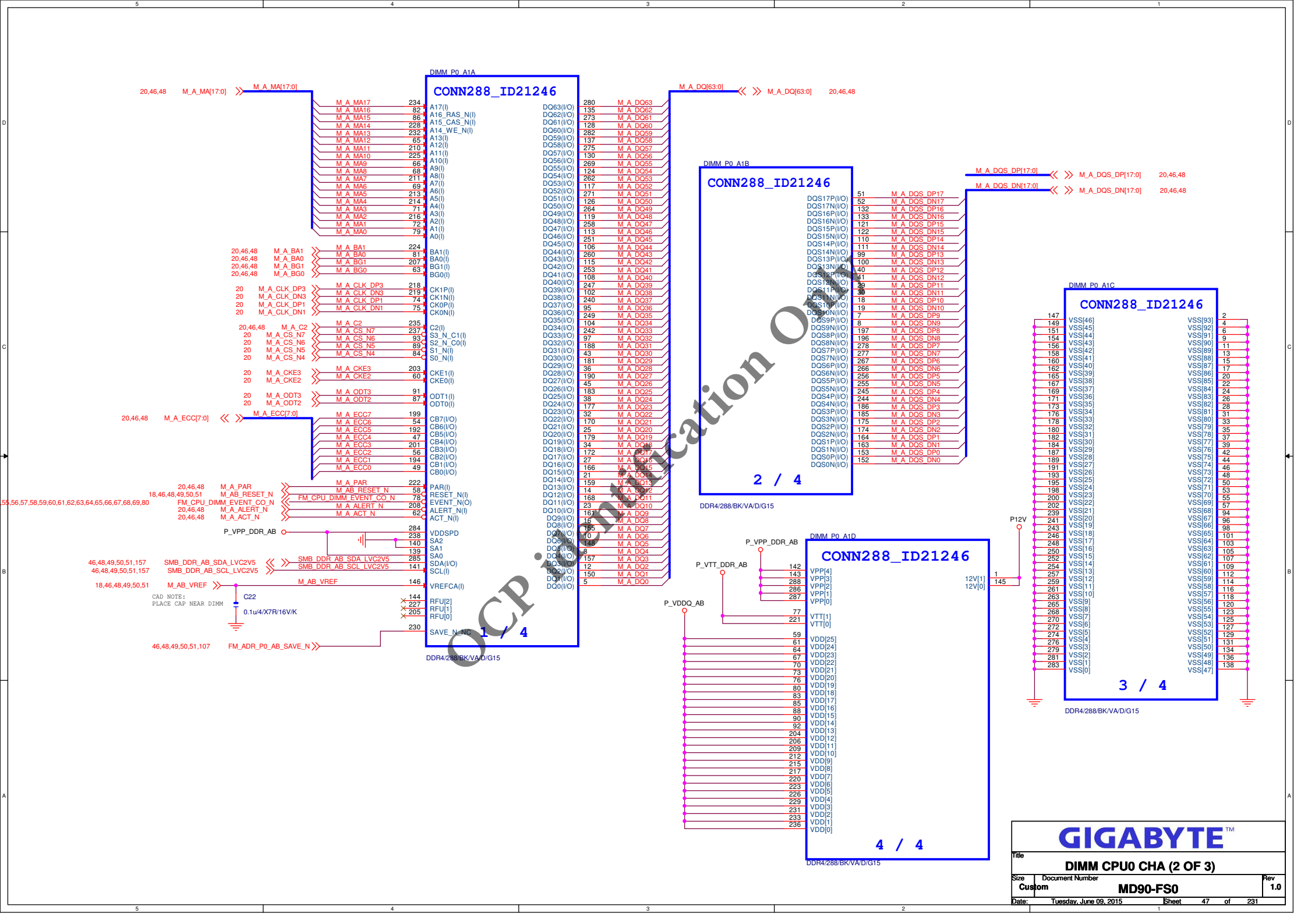
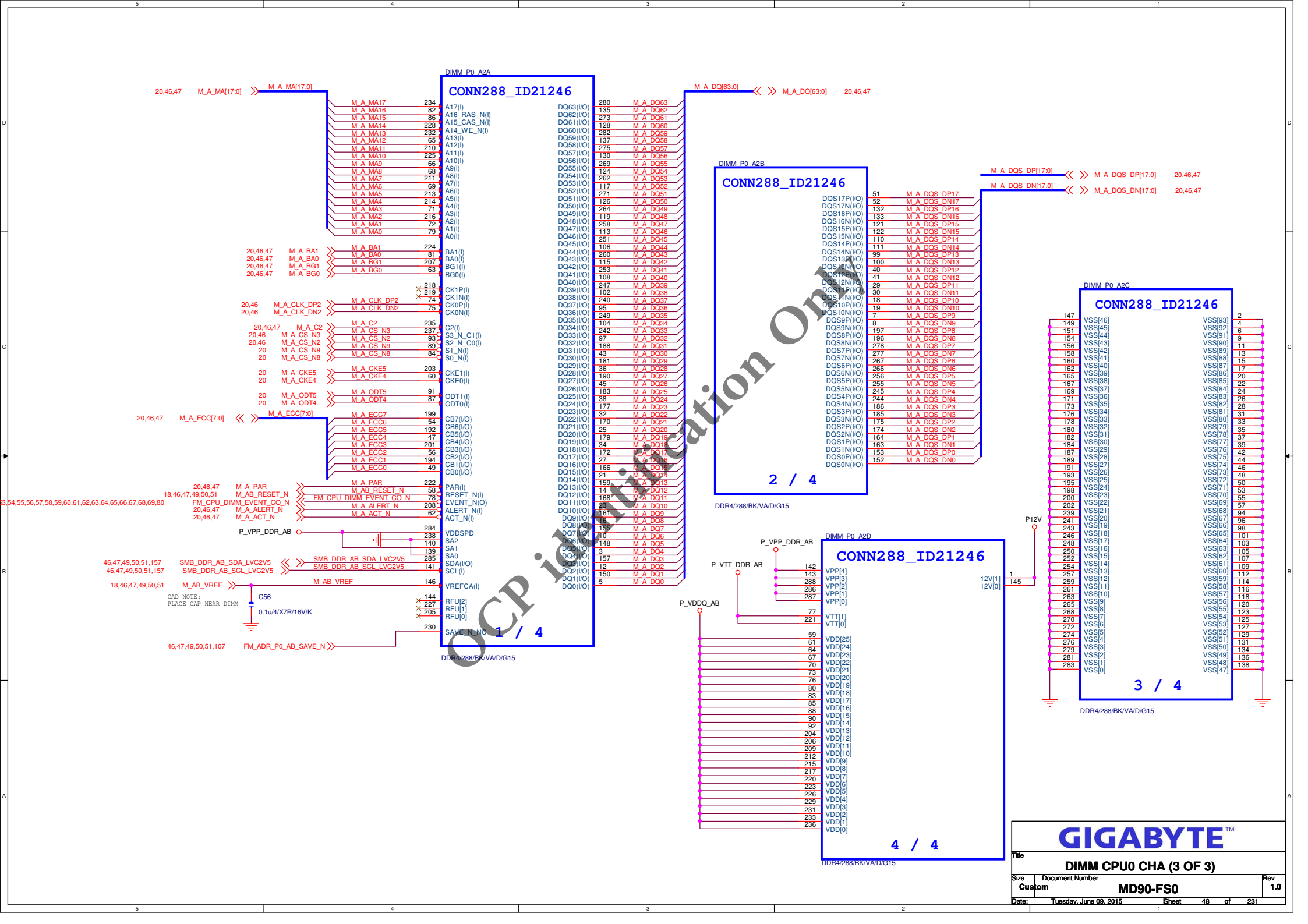


GIGABYTE™

Title	DIMM CPU0 CHA (2 OF 3)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 47 of 231	



Title	DIMM CPU0 CHA (3 OF 3)
Size	Custom
Document Number	MD90-FS0
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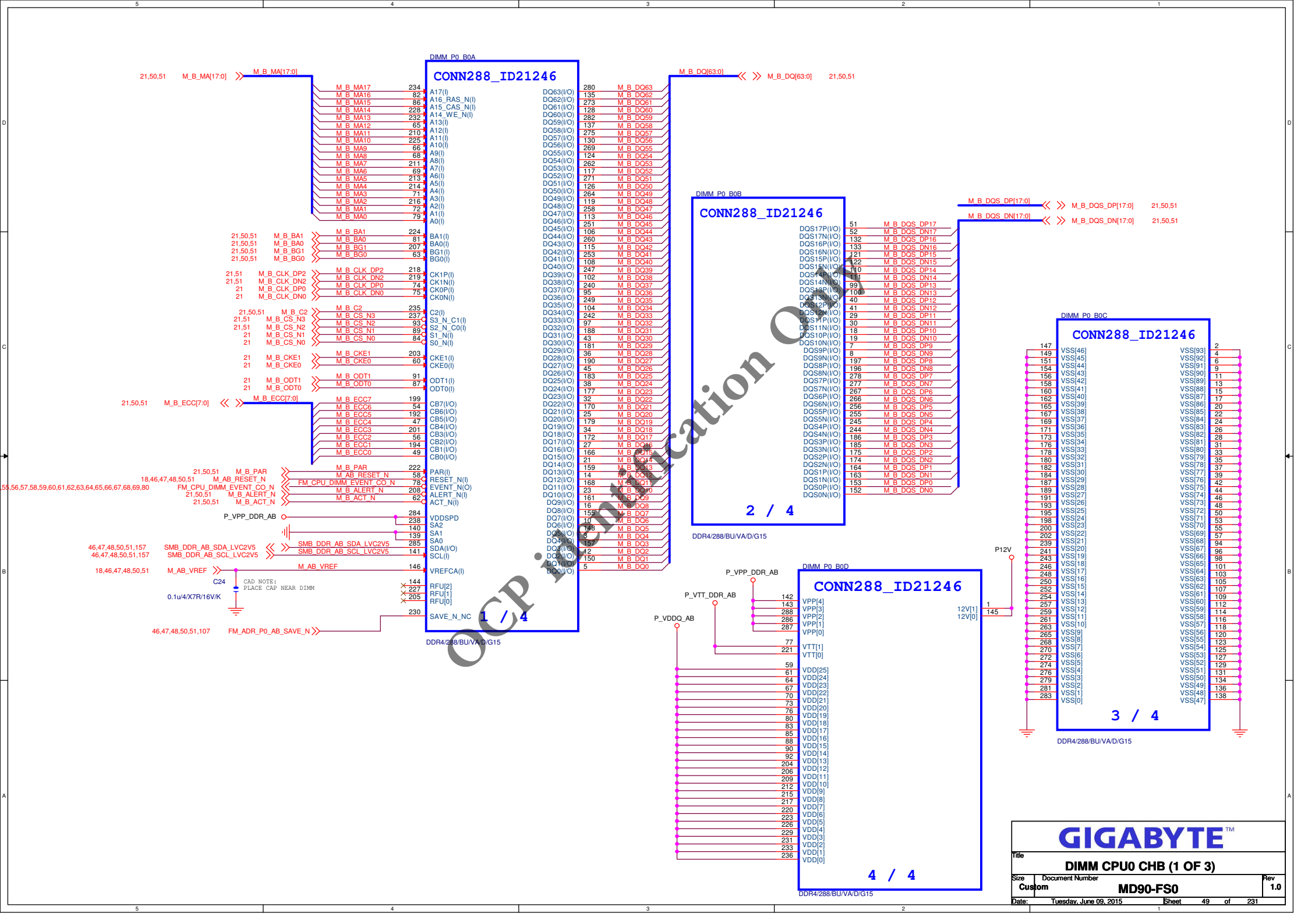

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Title: DIMM CPU0 CHB (1 OF 3)

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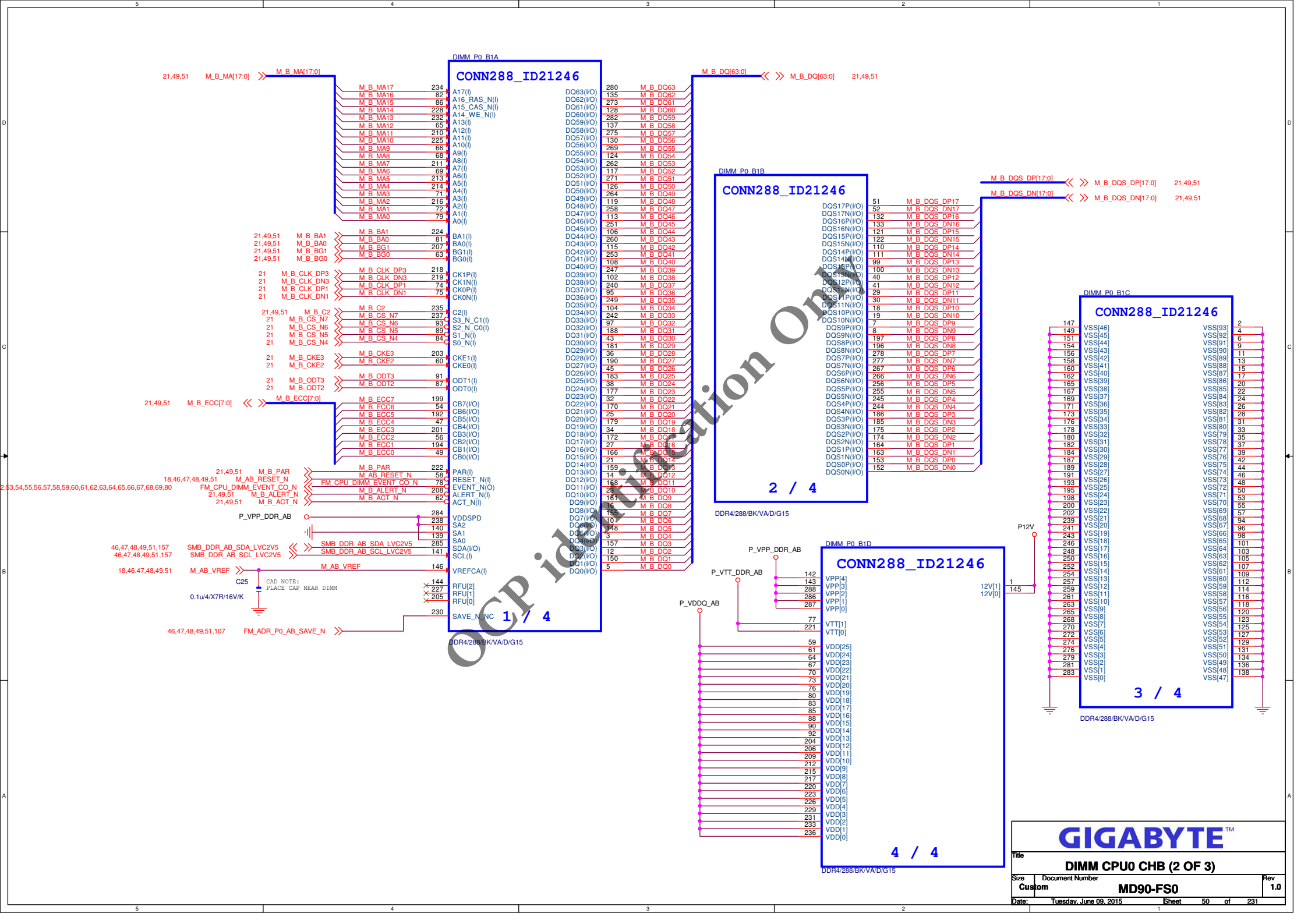
DIMM_P0_B1A
CONN288_ID21246
1 / 4
DDR4/288/BK/VA/D/G15
DIMM_P0_B1B
CONN288_ID21246
2 / 4
DDR4/288/BK/VA/D/G15
DIMM_P0_B1C
CONN288_ID21246
3 / 4
DDR4/288/BK/VA/D/G15
DIMM_P0_B1D
CONN288_ID21246
4 / 4
DDR4/288/BK/VA/D/G15
M_B_MA[17:0]
M_B_DQ[63:0]
M_B_ECC[7:0]
M_B_DQS_DP[17:0]
M_B_DQS_DN[17:0]
P_VPP_DDR_AB
P_VTT_DDR_AB
P_VDDQ_AB
P12V
C25
CAD NOTE: PLACE CAP NEAR DIMM
0.1u/4/X7R/16V/K
OCP identification Only
GIGABYTE
Title
DIMM CPU0 CHB (2 OF 3)
Size Custom
Document Number MD90-FS0
Rev 1.0
Date: Tuesday, June 09, 2015
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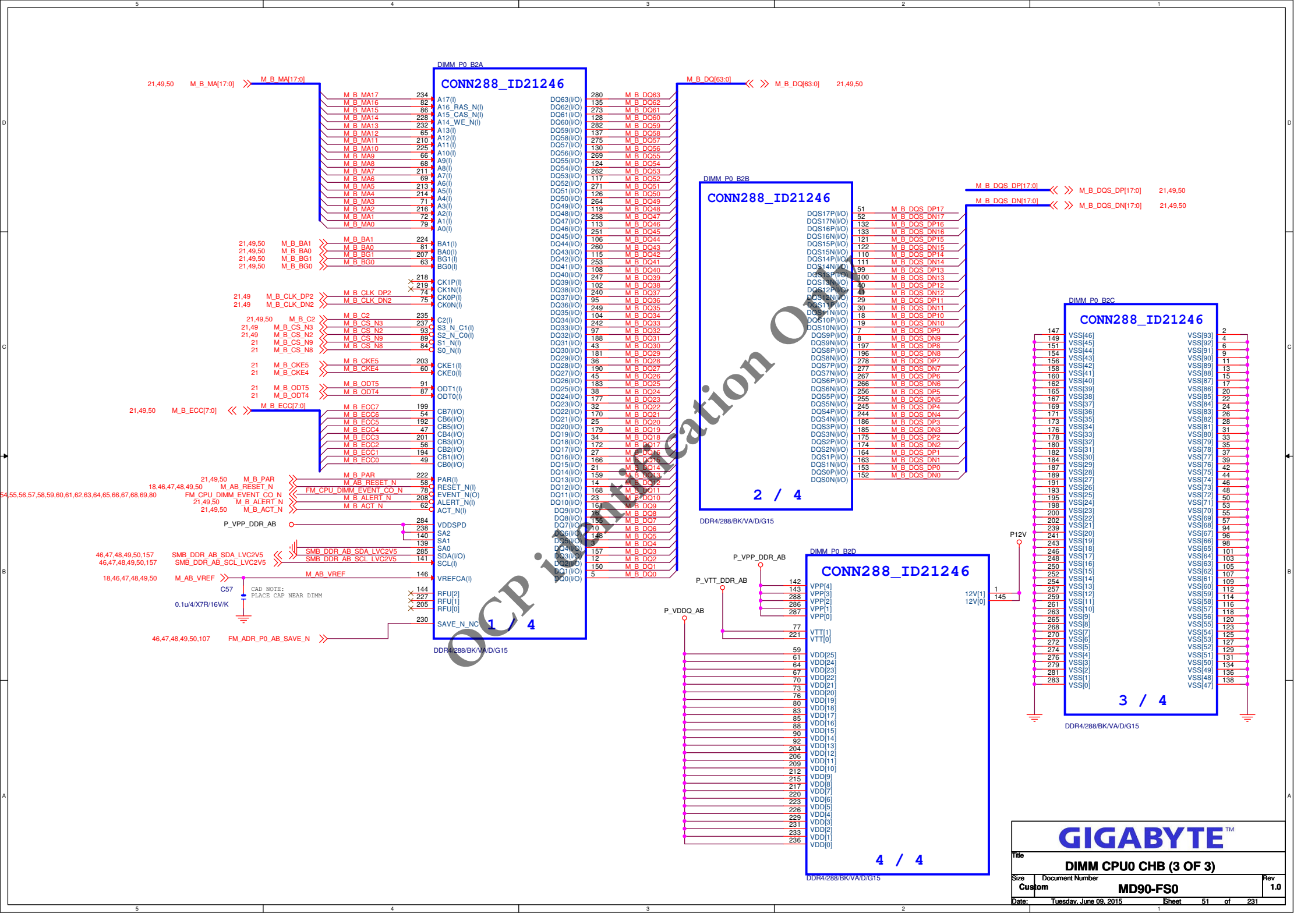

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Title	DIMM CPU0 CHB (3 OF 3)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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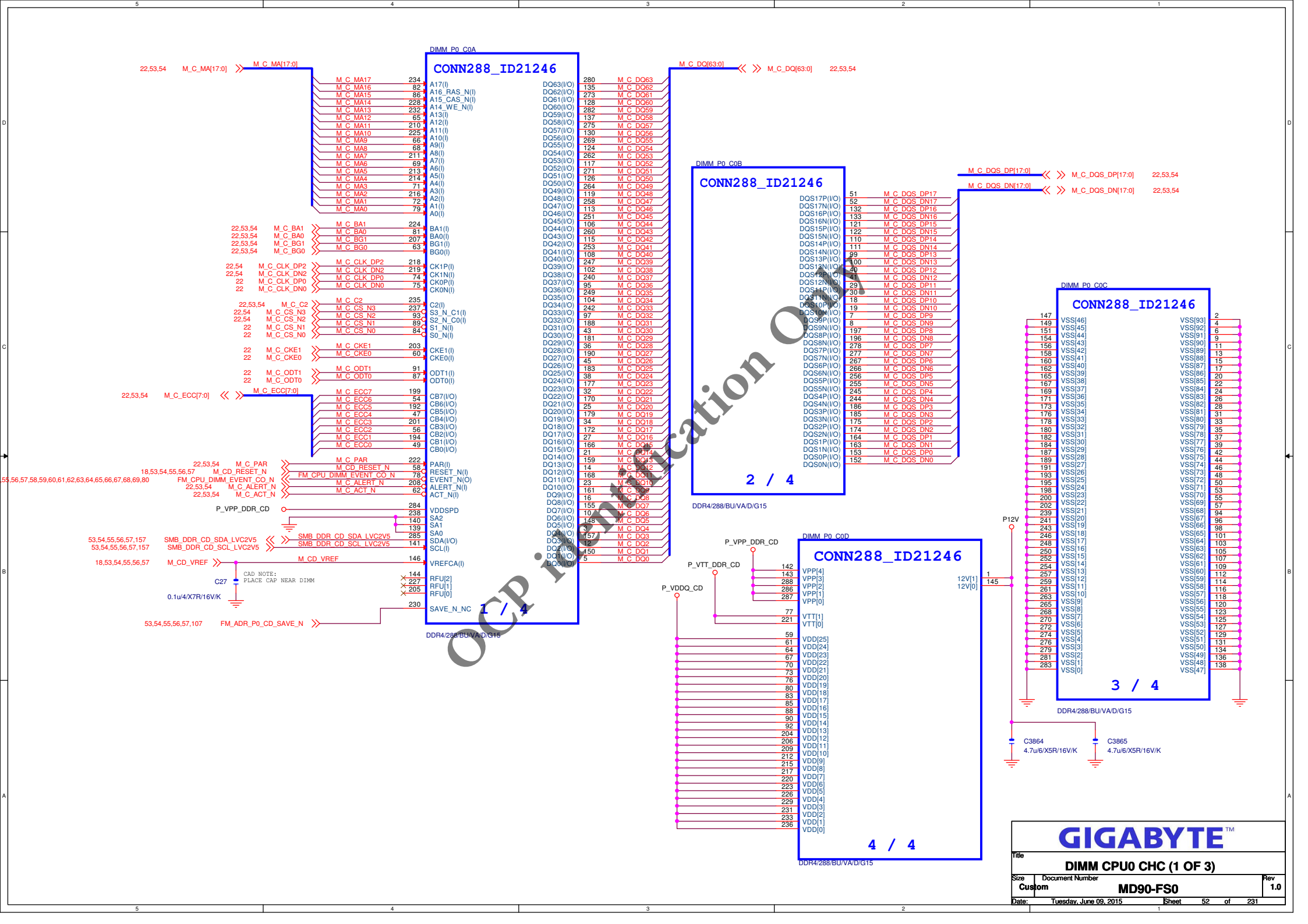

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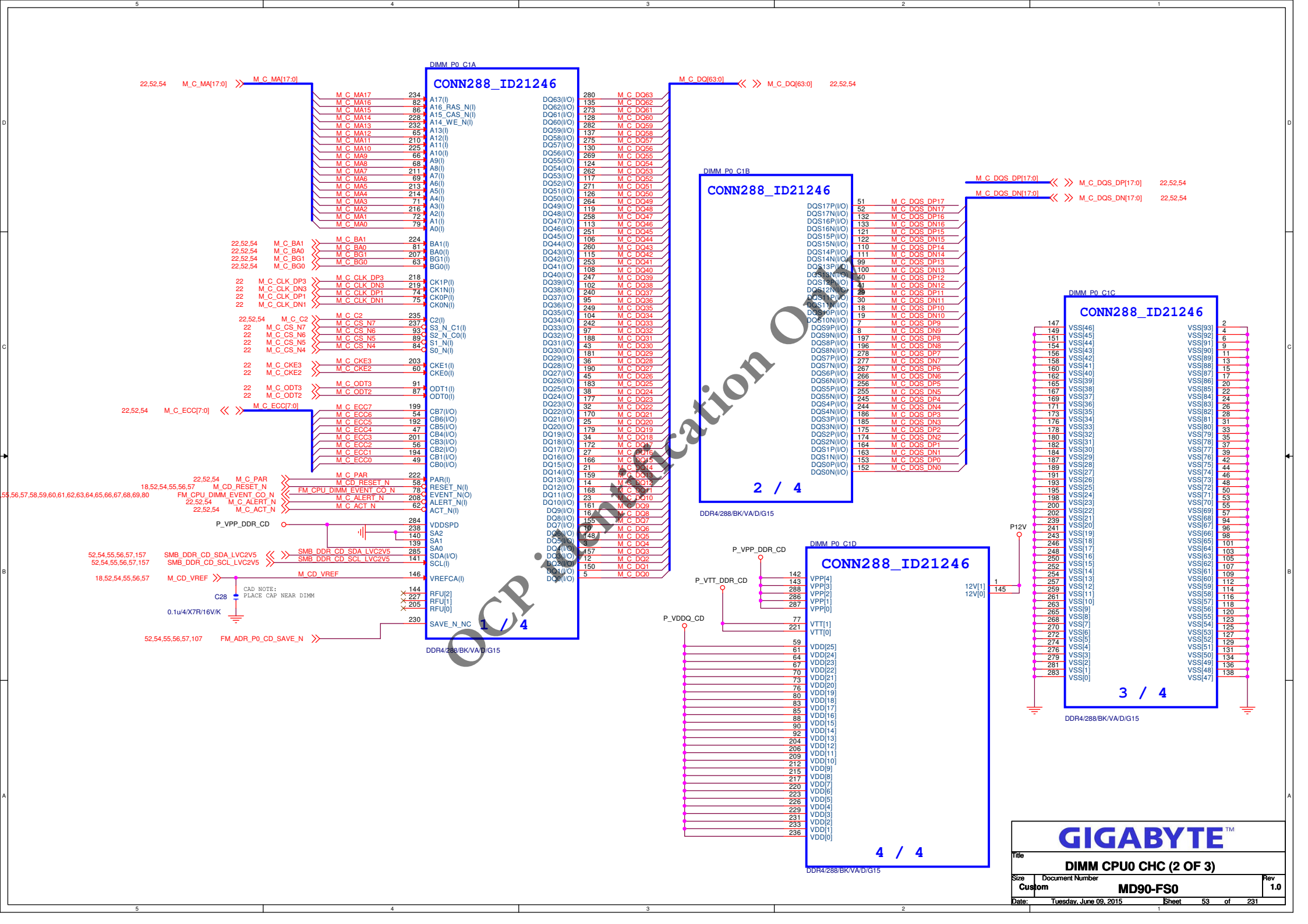
Title: DIMM CPU0 CHC (1 OF 3)

Size	Document Number	Rev
Custom	MD90-FS0	1.0

Date: Tuesday, June 09, 2015 Sheet 52 of 231



GIGABYTE™

Title: DIMM CPU0 CHC (2 OF 3)

Size: Custom | Document Number: MD90-FS0 | Rev: 1.0

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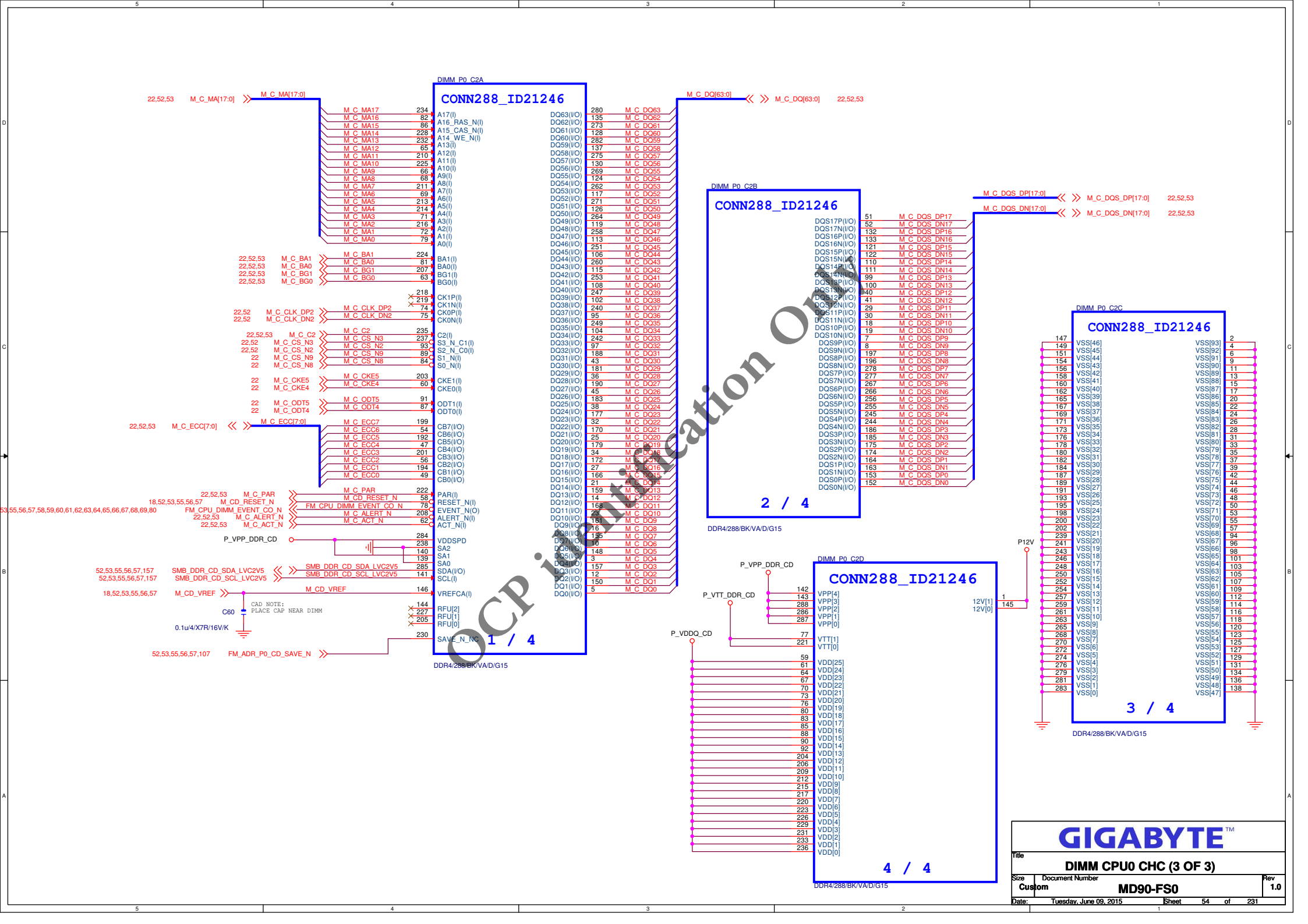

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Title: DIMM CPU0 CHC (3 OF 3)

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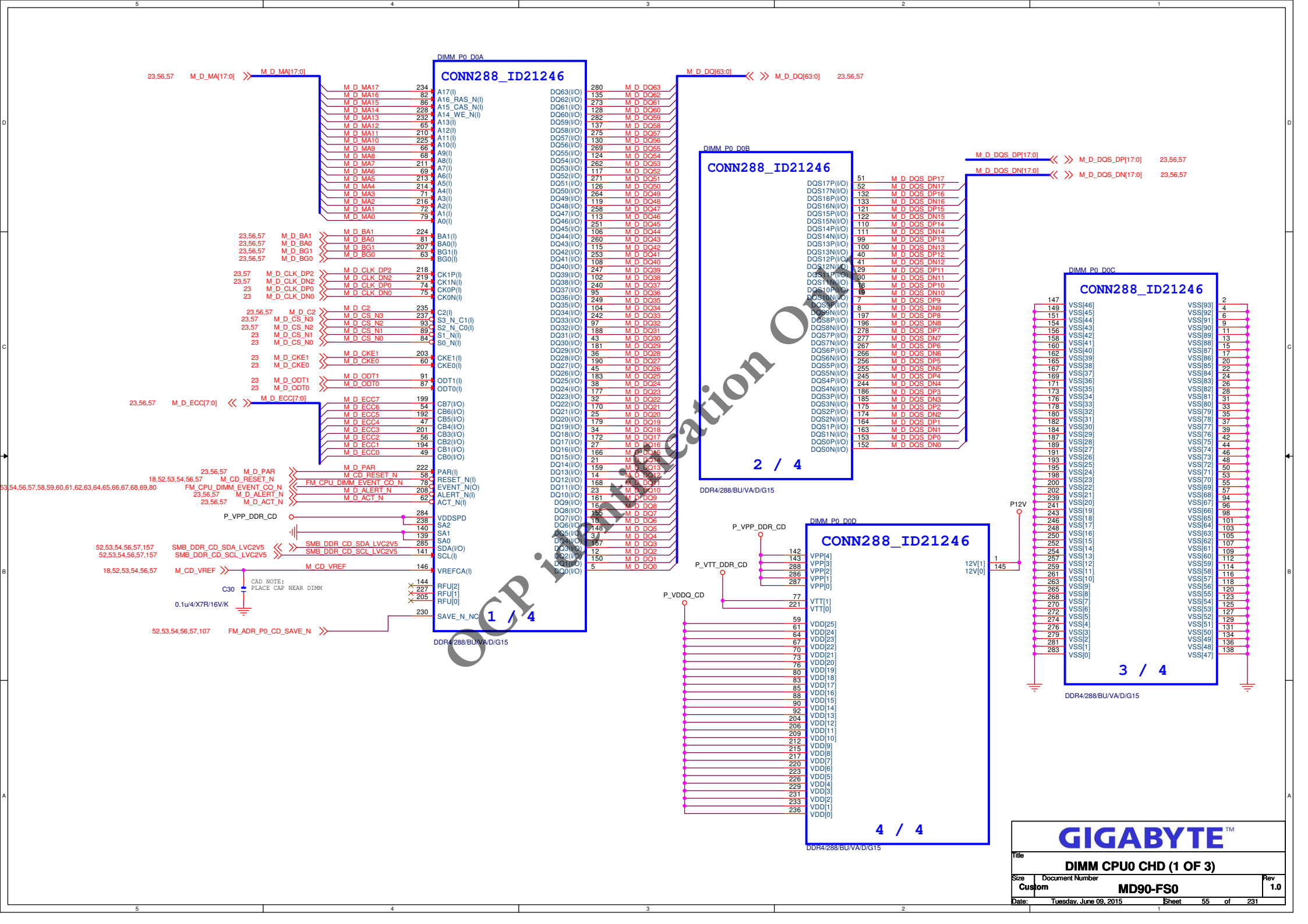
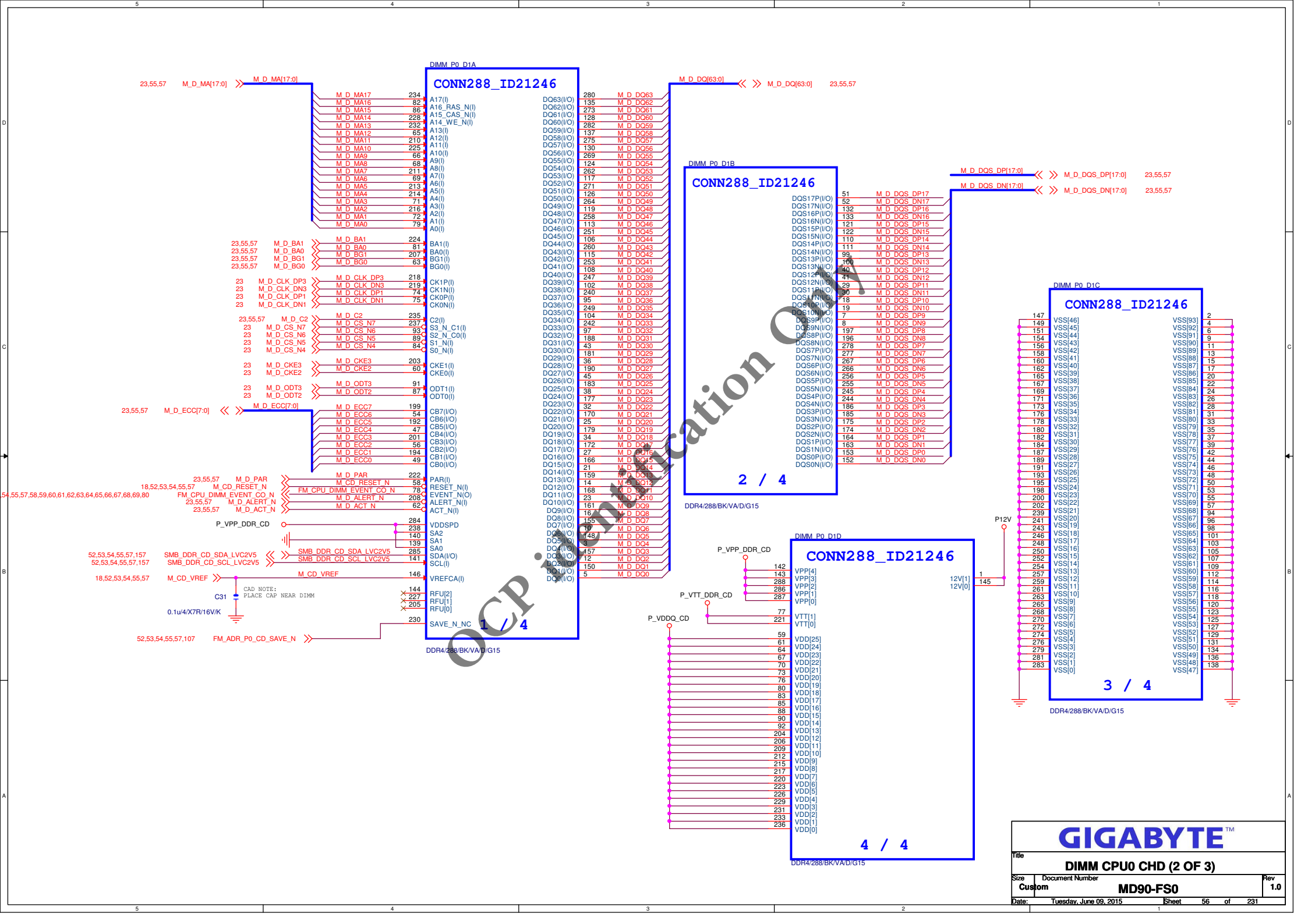


GIGABYTE™

Title: DIMM CPU0 CHD (1 OF 3)

Size: Custom | Document Number: MD90-FS0 | Rev: 1.0

Date: Tuesday, June 09, 2015 | Sheet 55 of 231



Title	DIMM CPU0 CHD (2 OF 3)
Size	Custom
Document Number	MD90-FS0
Rev	1.0
Date:	Tuesday, June 09, 2015
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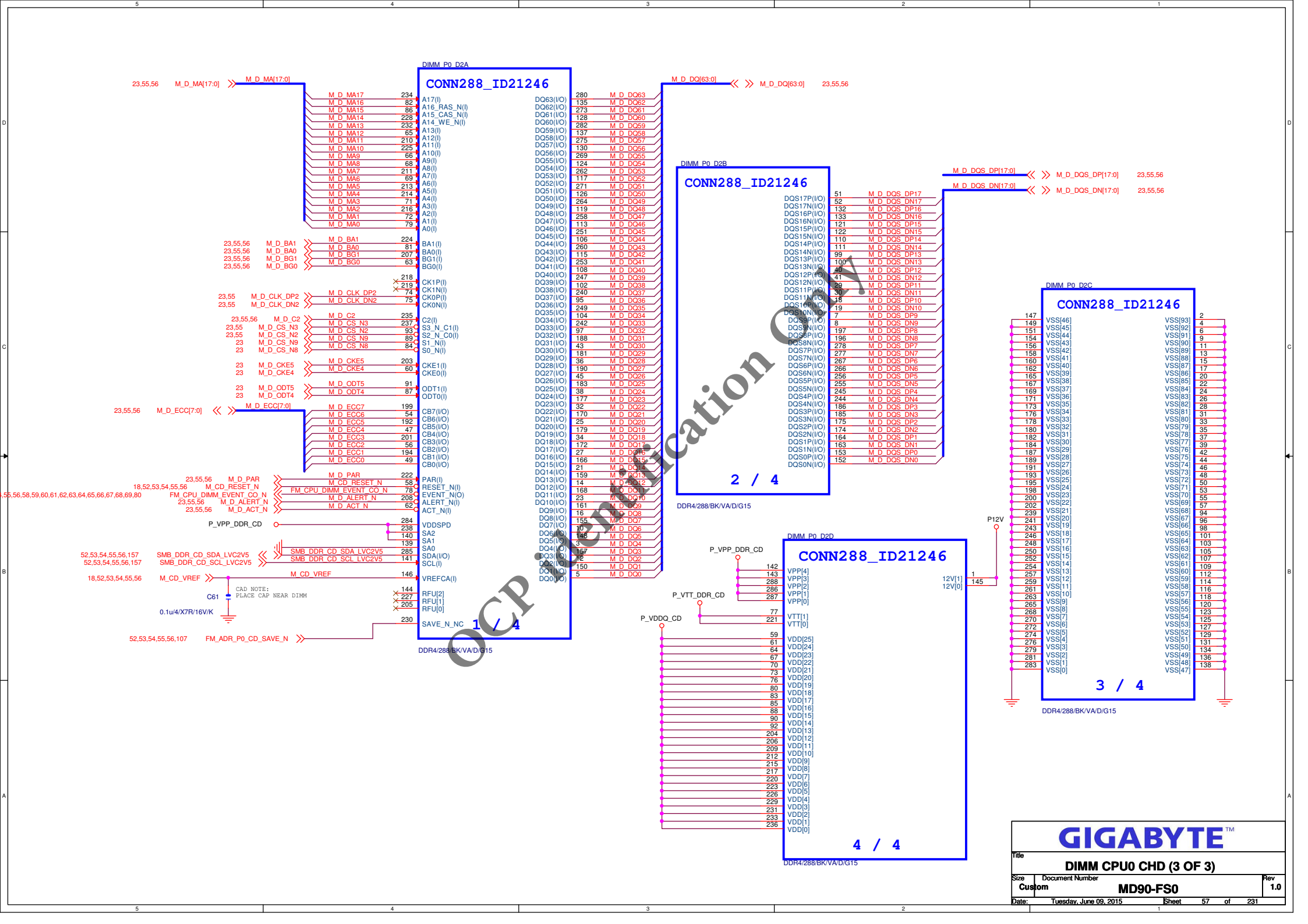
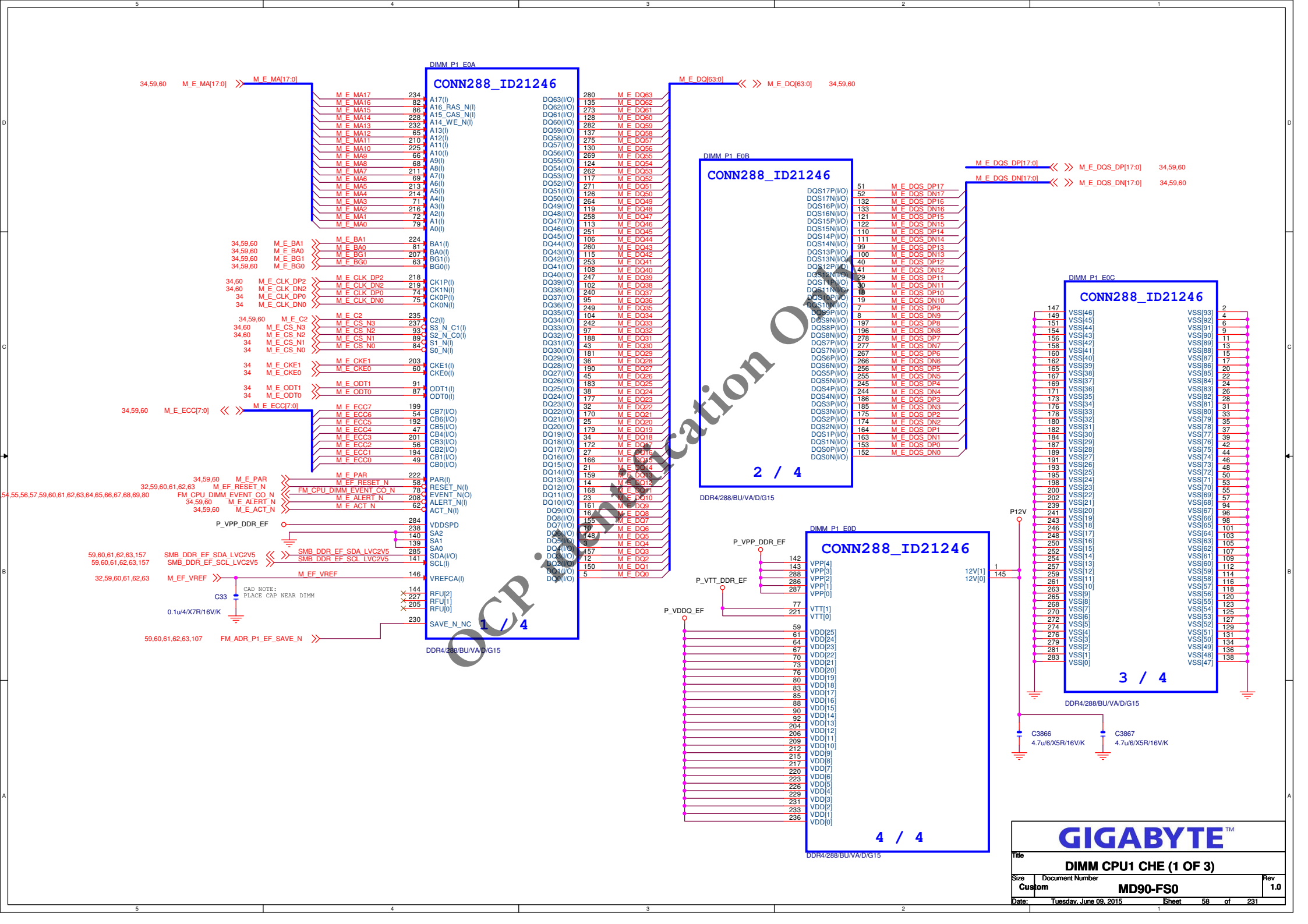


GIGABYTE™			
Title: DIMM CPU0 CHD (3 OF 3)			
Size: Custom	Document Number: MD90-FS0		Rev: 1.0
Date: Tuesday, June 09, 2015		Sheet 57 of 231	

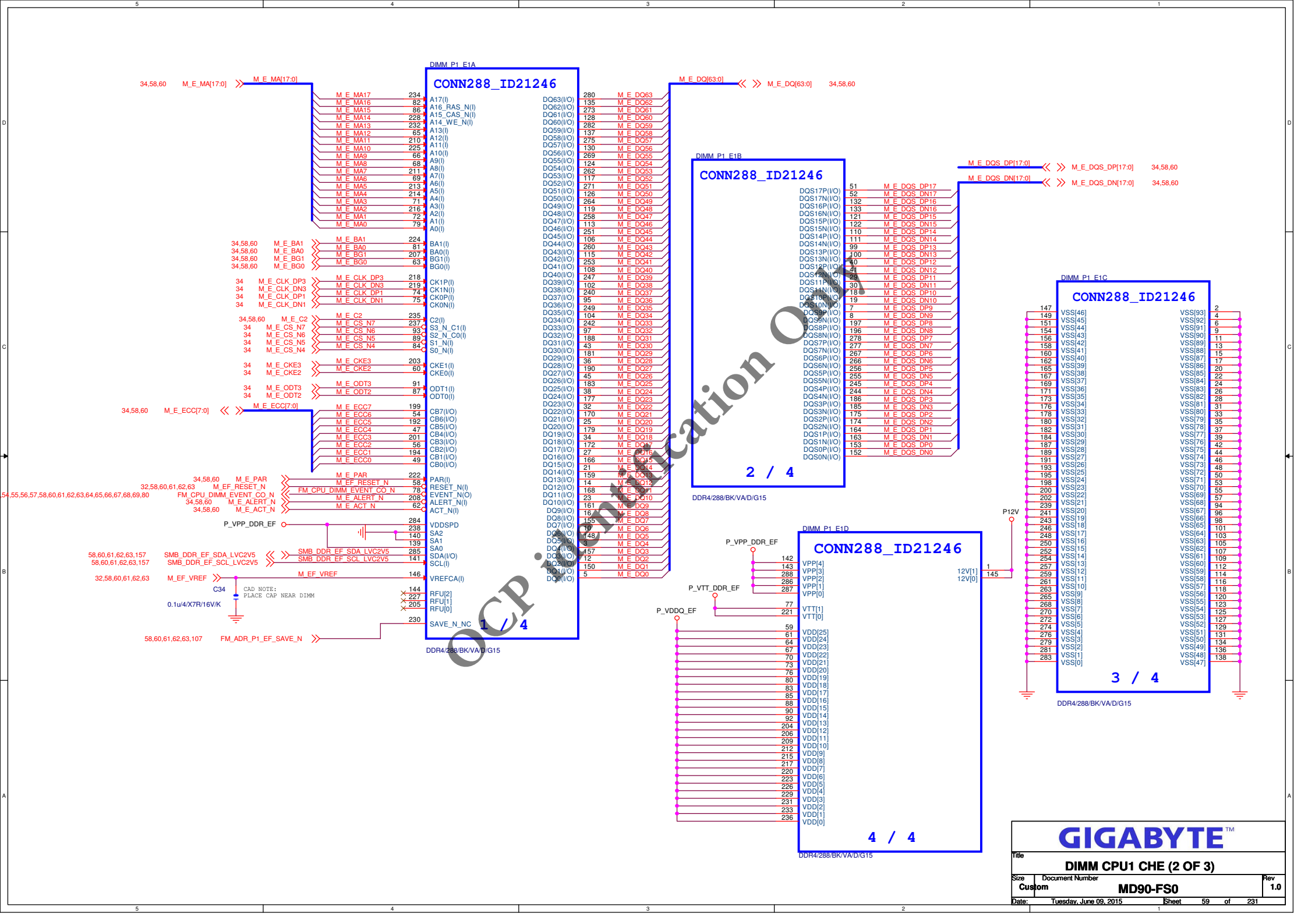


GIGABYTE™

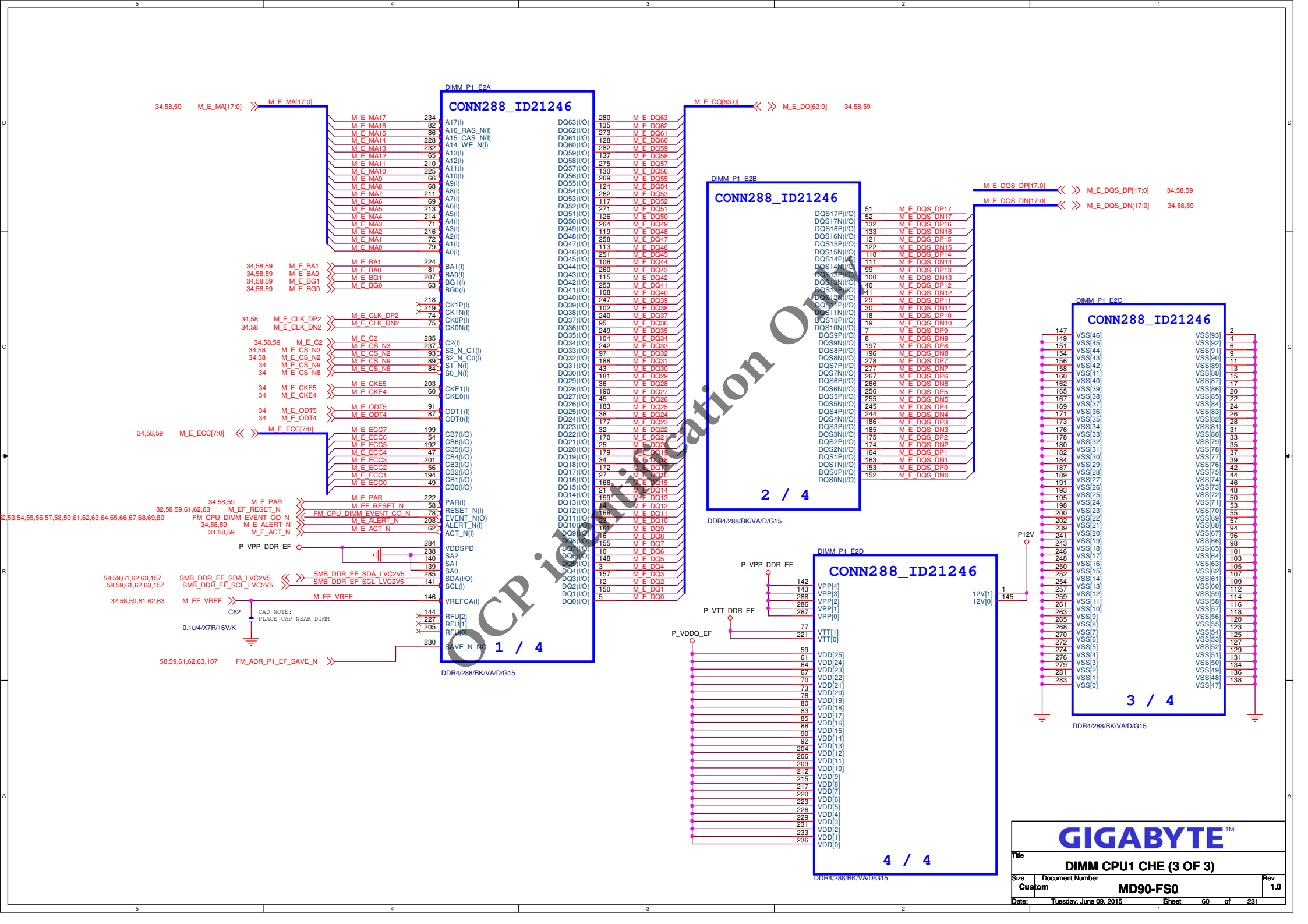
Title: DIMM CPU1 CHE (1 OF 3)

Size	Document Number	Rev
Custom	MD90-FS0	1.0

Date: Tuesday, June 09, 2015 Sheet 58 of 231

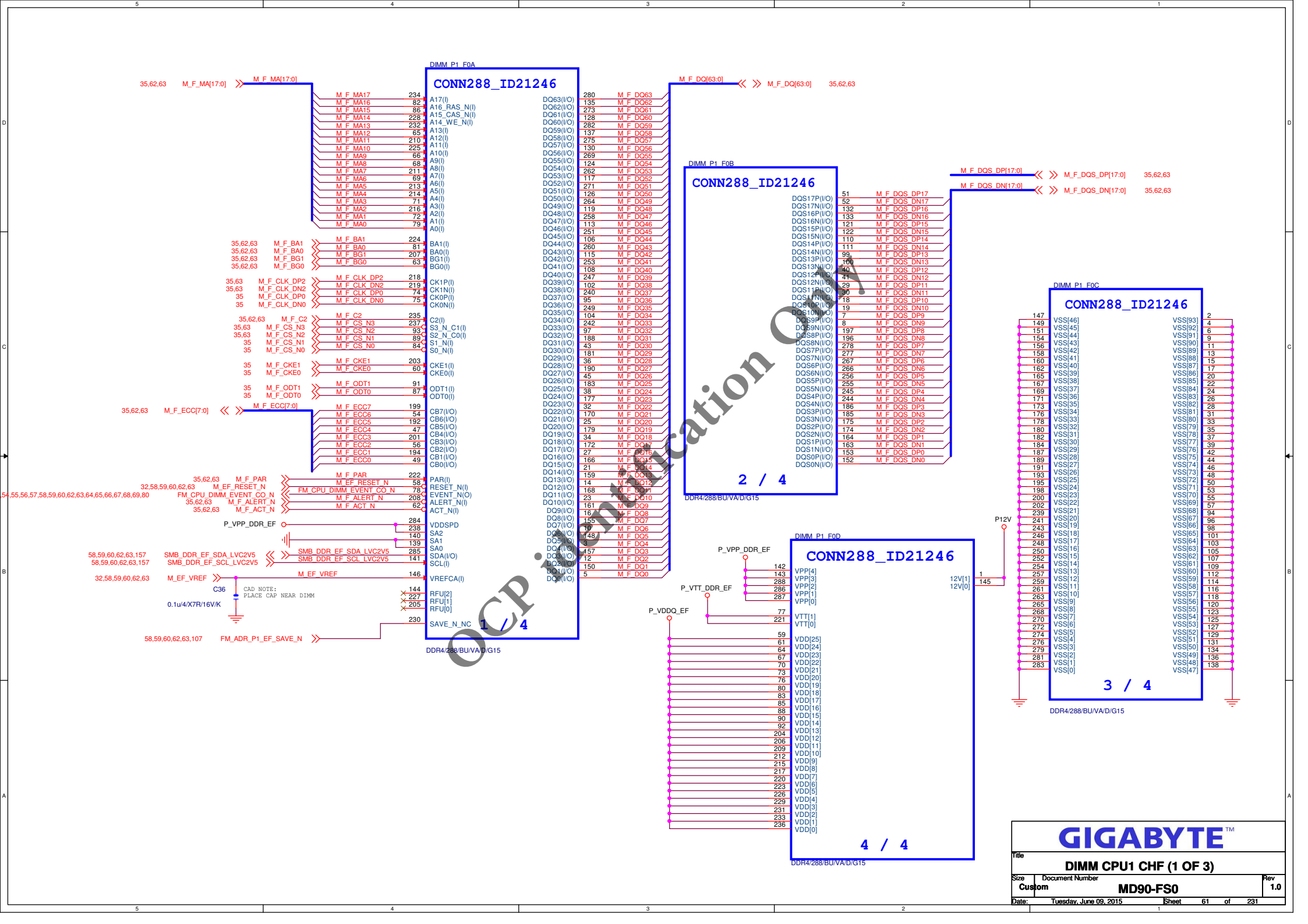


Title	DIMM CPU1 CHE (2 OF 3)		
Size	Document Number		Rev
Custom	MD90-FS0		1.0
Date:	Tuesday, June 09, 2015	Sheet	59 of 231

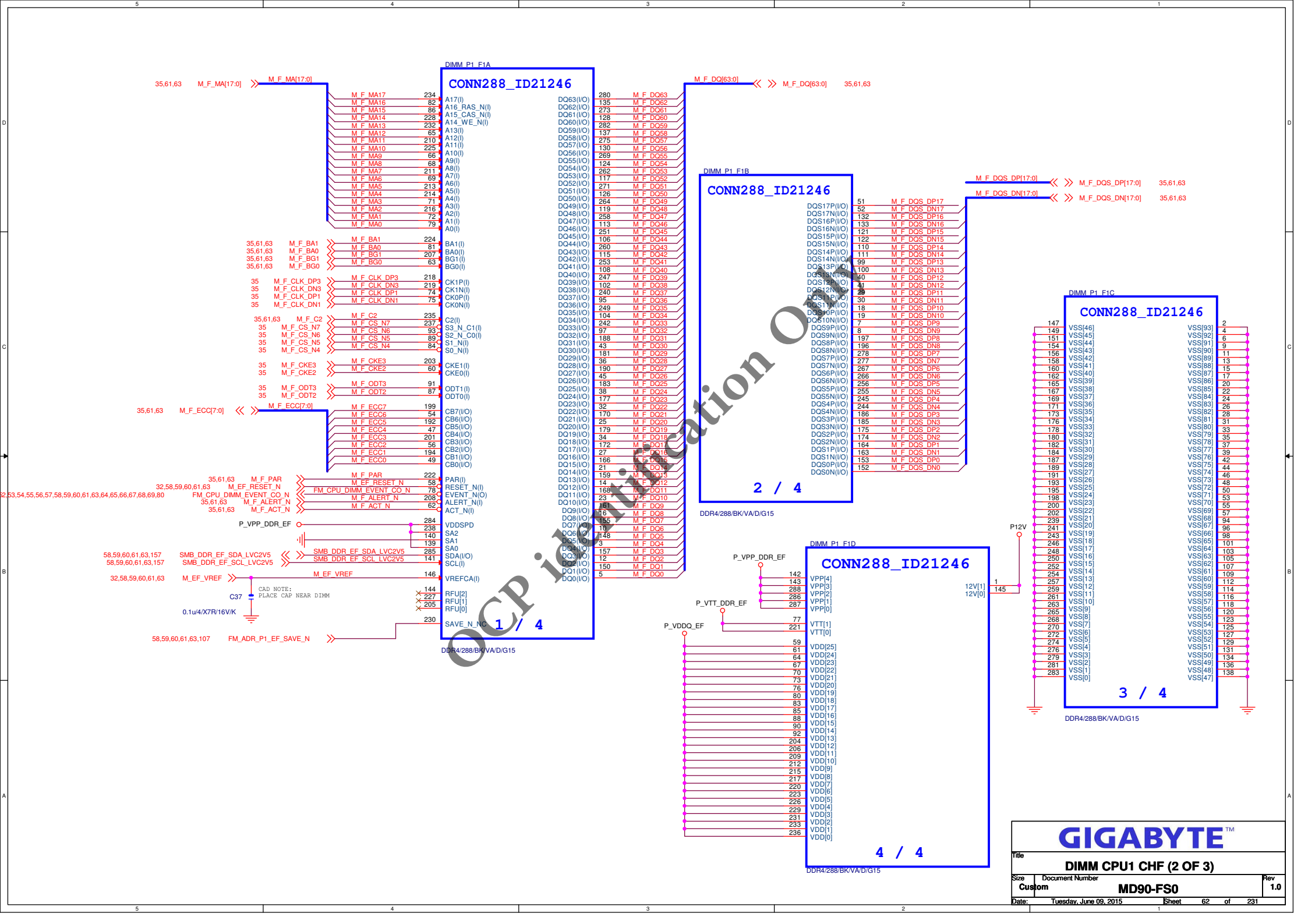


GIGABYTE™

Title	DIMM CPU1 CHE (3 OF 3)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 60 of 231	



Title	DIMM CPU1 CHF (1 OF 3)
Size	Custom
Document Number	MD90-FS0
Rev	1.0
Date:	Tuesday, June 09, 2015
Sheet	61 of 231

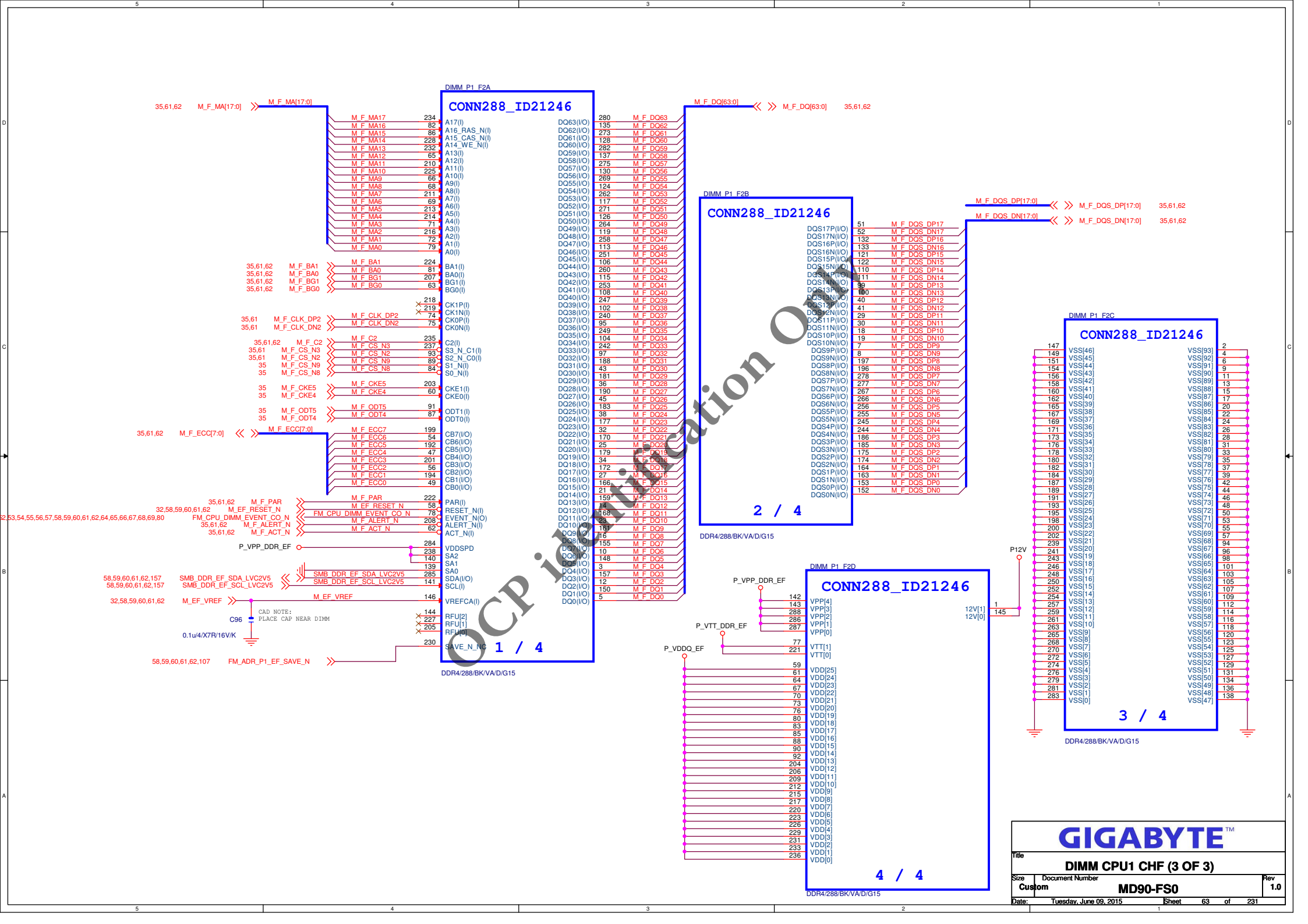


GIGABYTE™

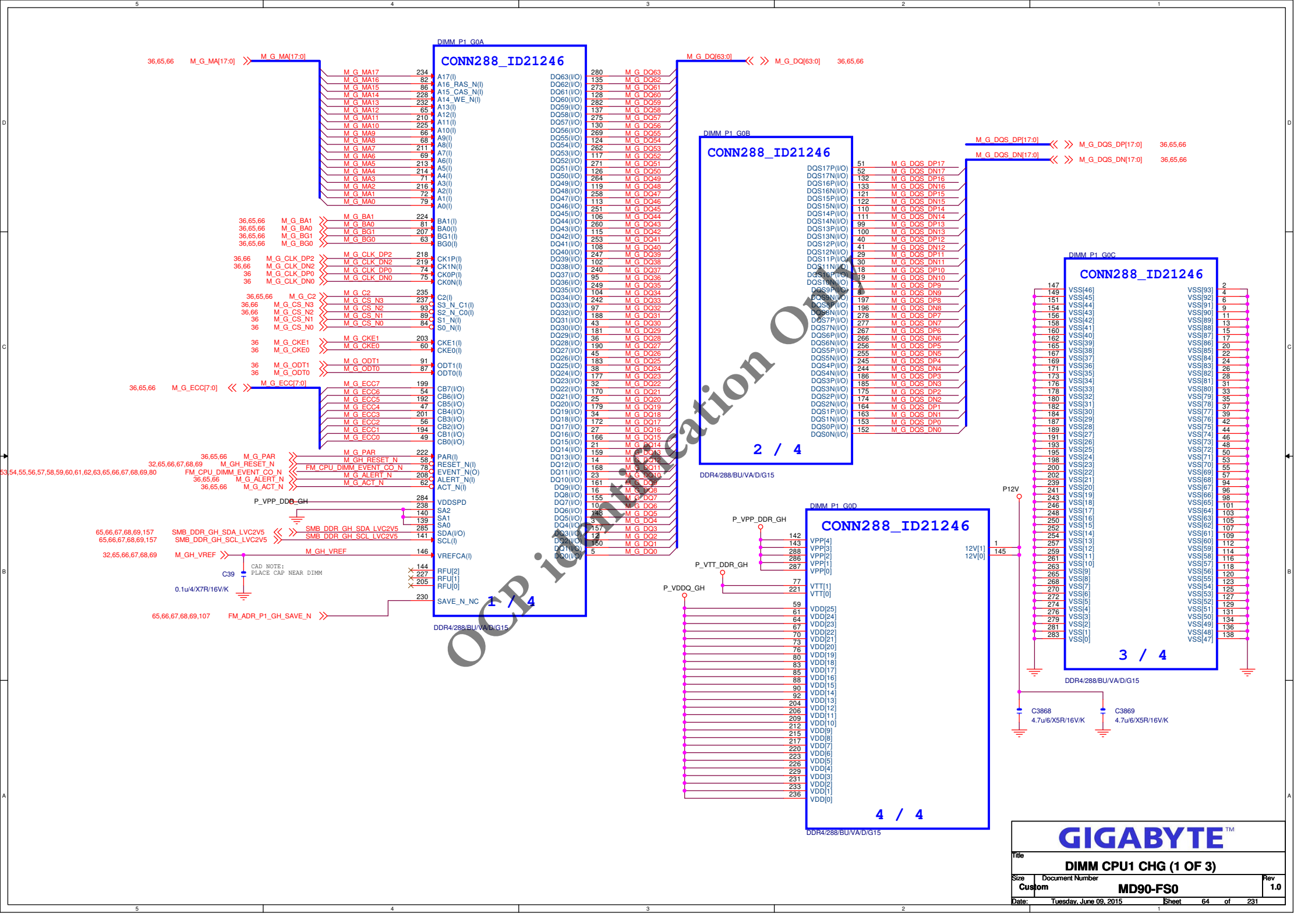
Title: DIMM CPU1 CHF (2 OF 3)

Size	Document Number	Rev
Custom	MD90-FS0	1.0

Date: Tuesday, June 09, 2015 Sheet 62 of 231



Title	DIMM CPU1 CHF (3 OF 3)		
Size	Document Number		Rev
Custom	MD90-FS0		1.0
Date:	Tuesday, June 09, 2015	Sheet	63 of 231

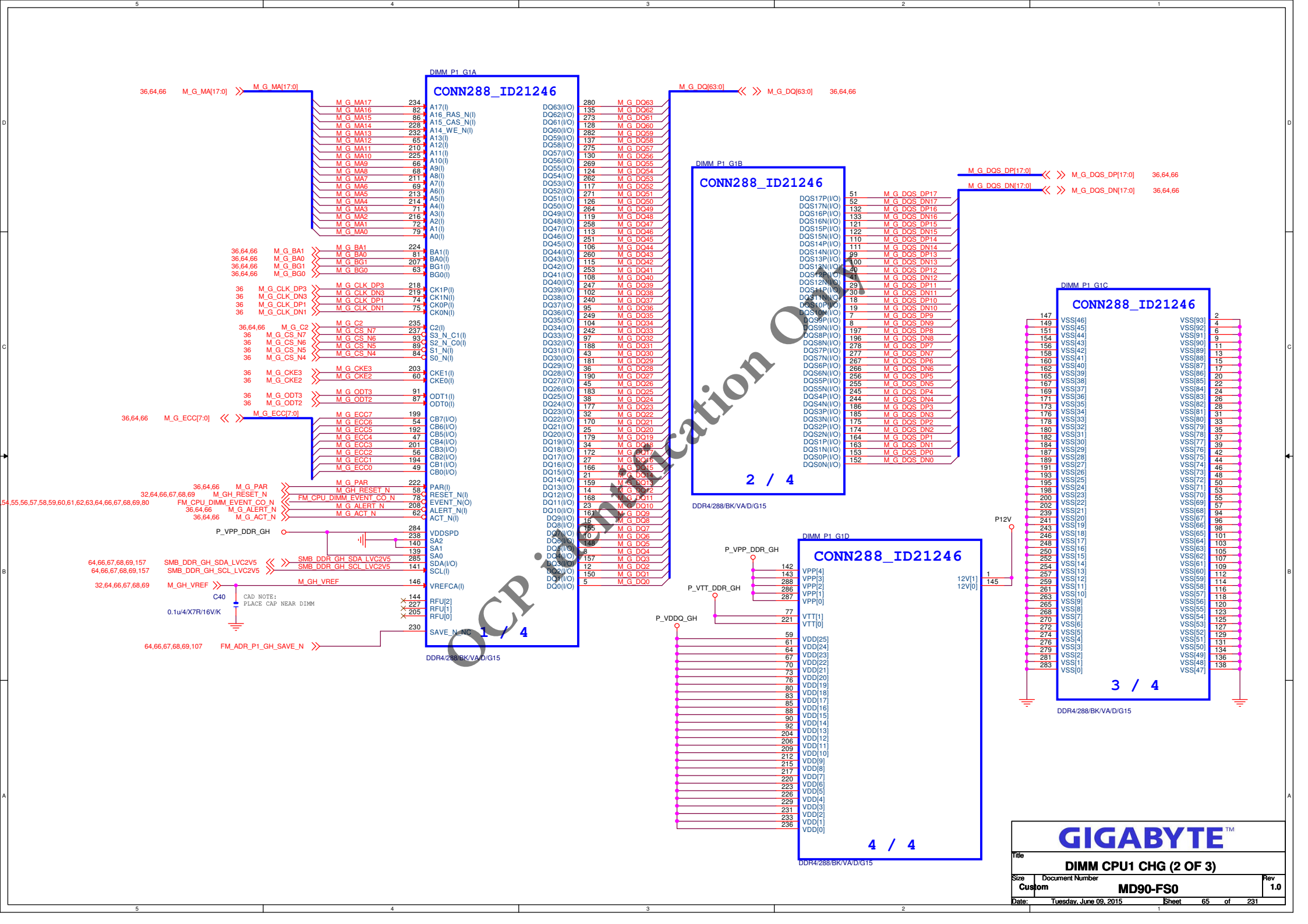


GIGABYTE™

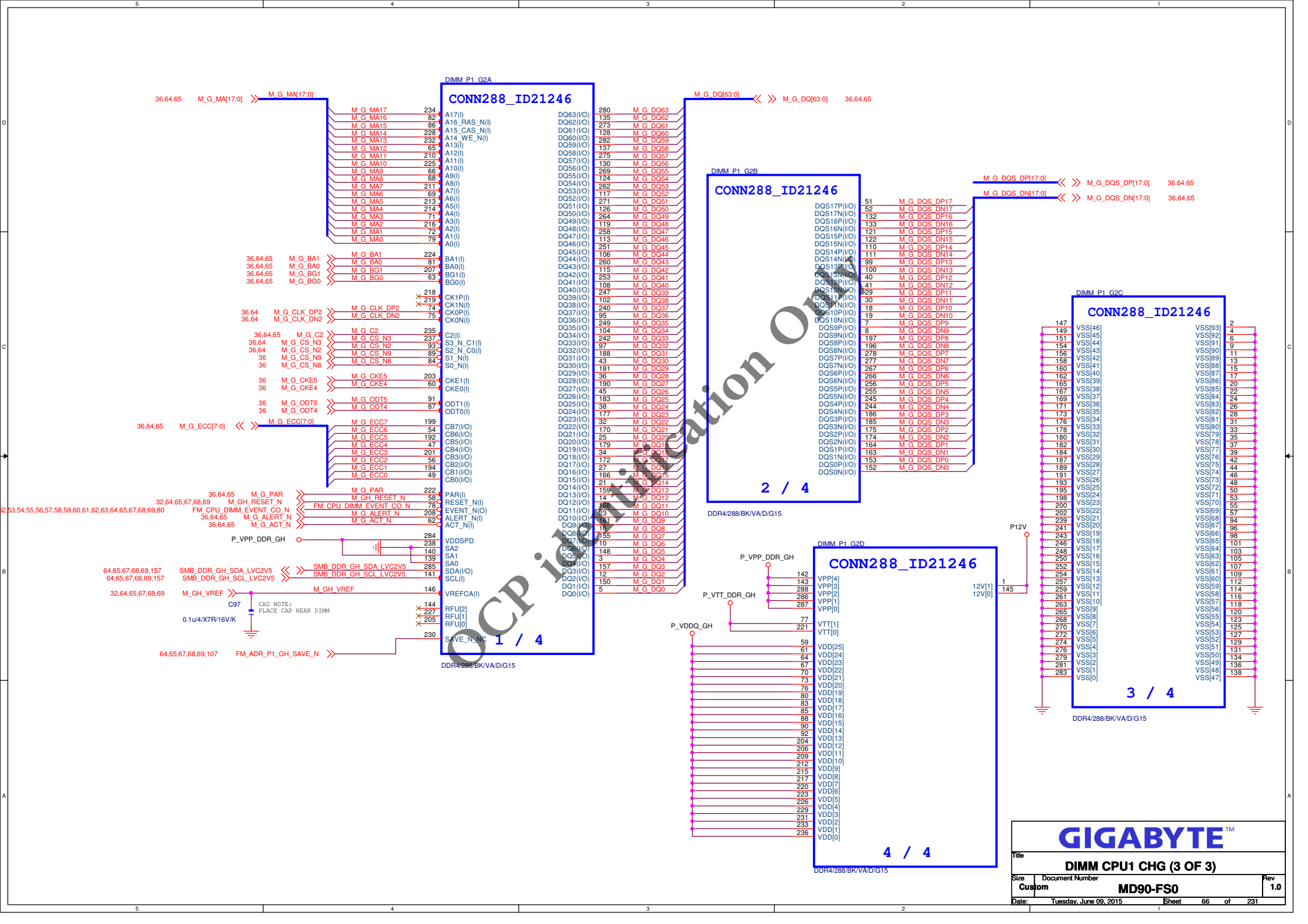
Title: DIMM CPU1 CHG (1 OF 3)

Size	Document Number	Rev
Custom	MD90-FS0	1.0

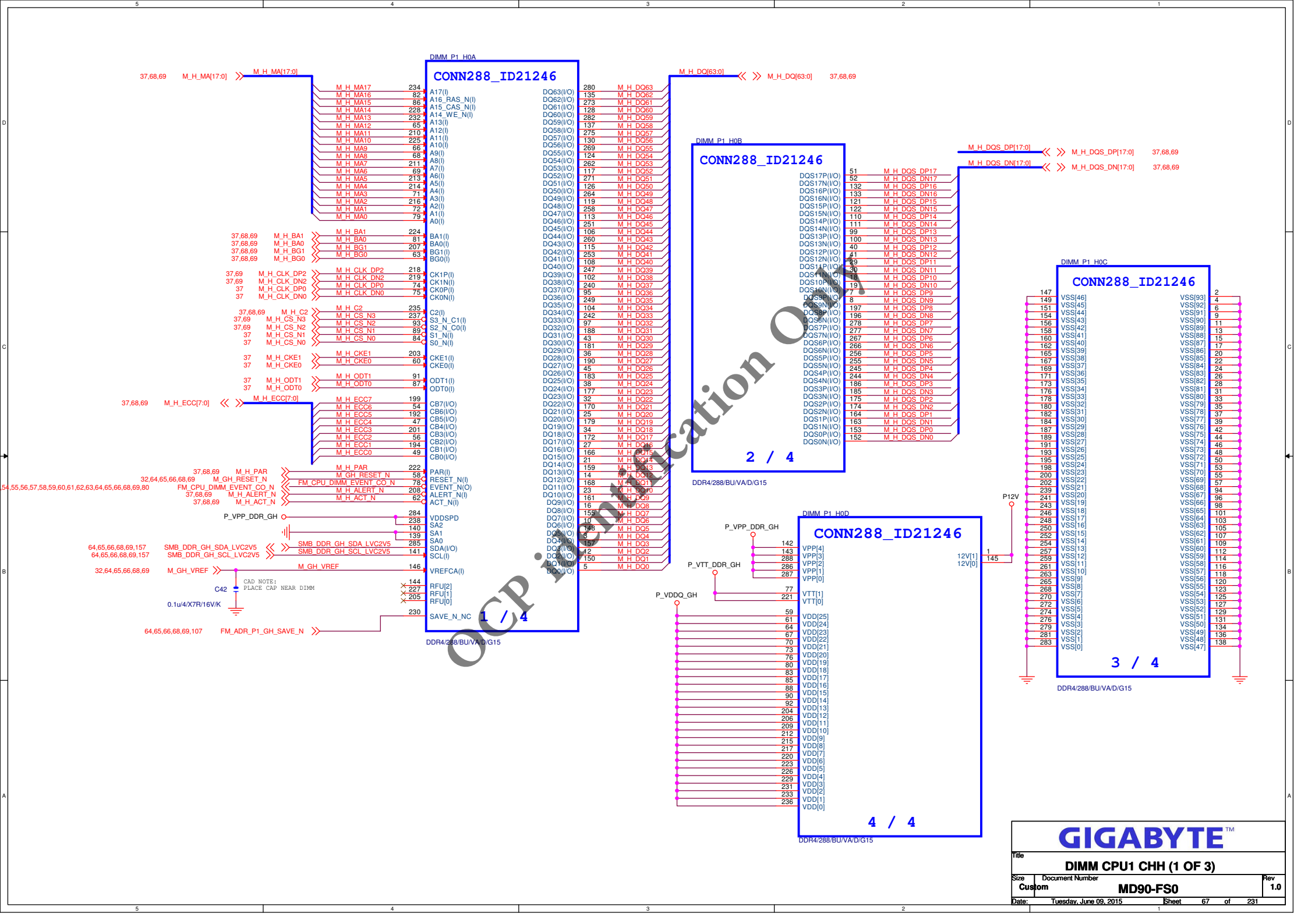
Date: Tuesday, June 09, 2015 Sheet 64 of 231



GIGABYTE		
Title	DIMM CPU1 CHG (2 OF 3)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 65 of 231	



GIGABYTE™		
Title	DIMM CPU1 CHG (3 OF 3)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 66 of 231	

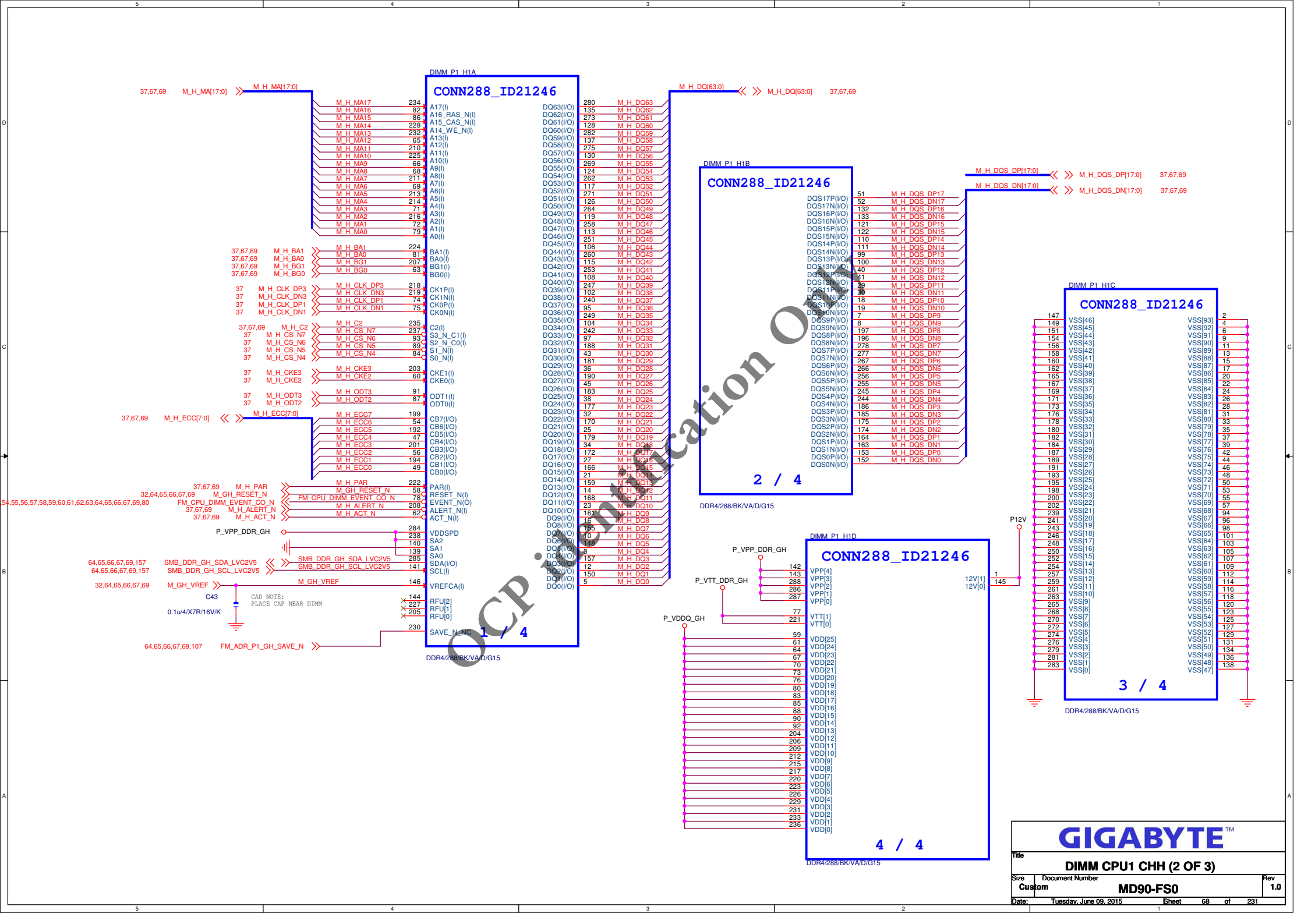


GIGABYTE™

Title: DIMM CPU1 CHH (1 OF 3)

Size	Document Number	Rev
Custom	MD90-FS0	1.0

Date: Tuesday, June 09, 2015 Sheet 67 of 231



Title	DIMM CPU1 CHH (2 OF 3)
Size	Custom
Document Number	MD90-FS0
Rev	1.0
Date:	Tuesday, June 09, 2015
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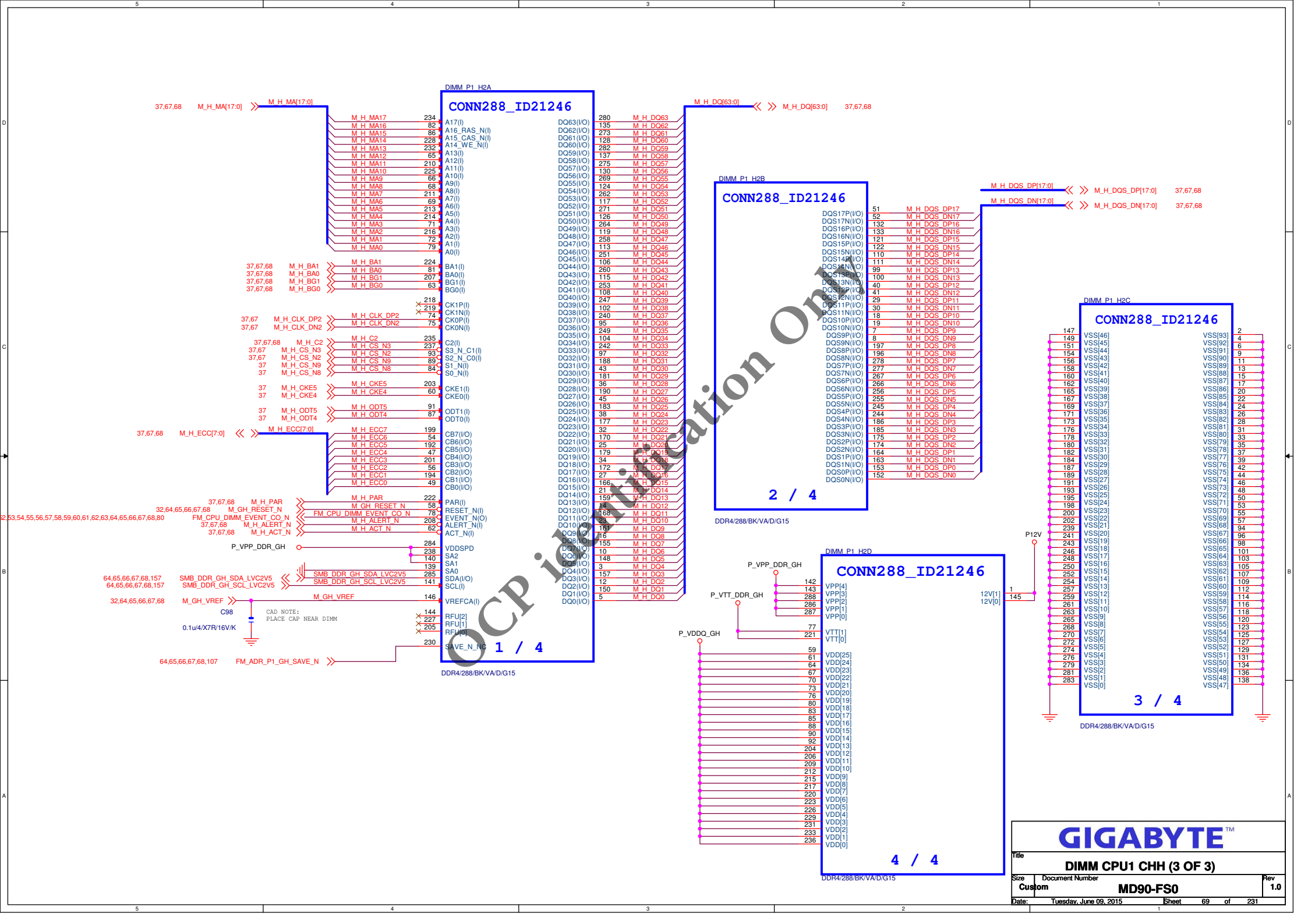

Title	DIMM CPU1 CHH (3 OF 3)
Size	Custom
Document Number	MD90-FS0
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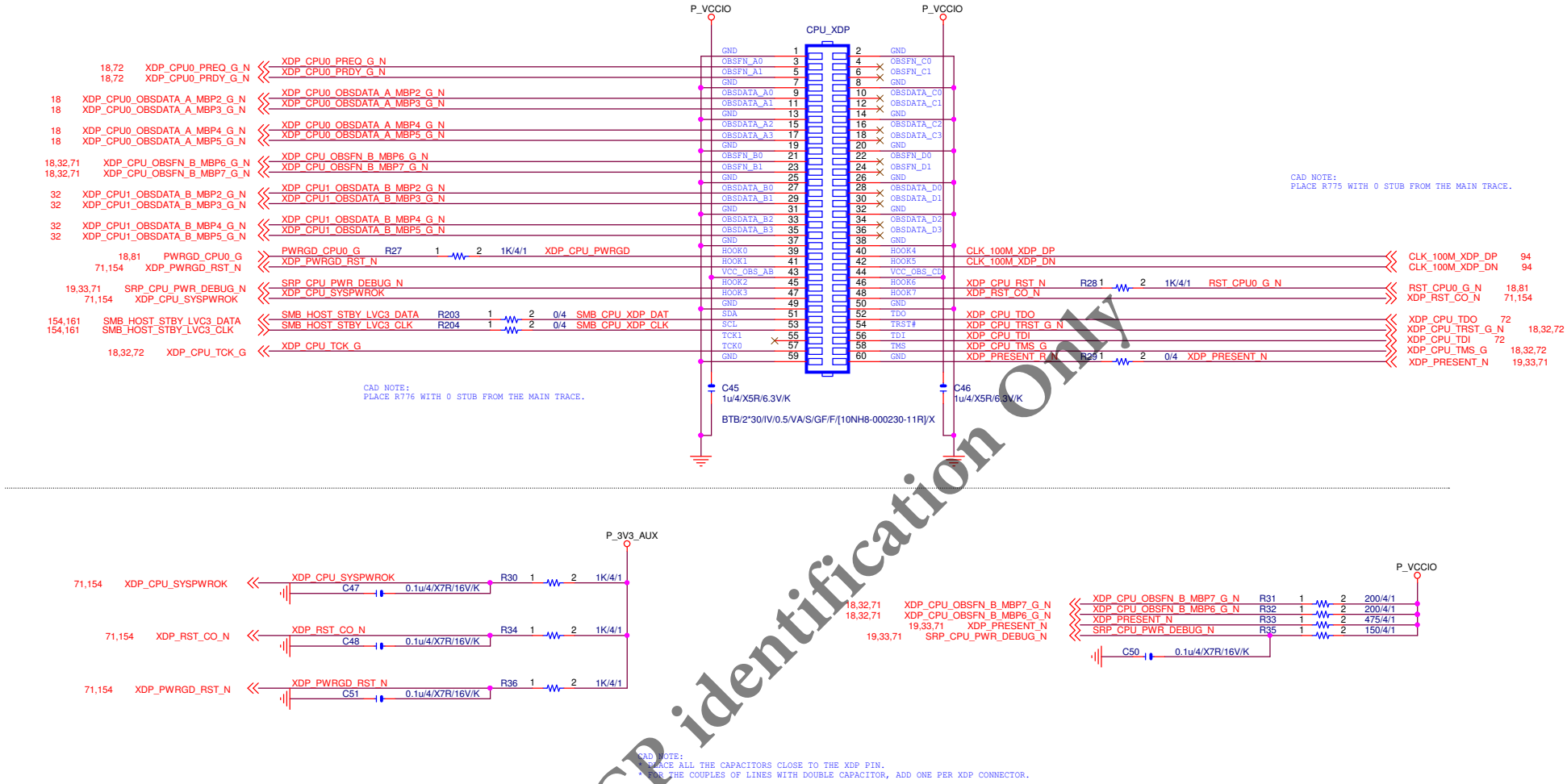
GIGABYTE™

Title: DECOUPLING CPU0 & CPU1

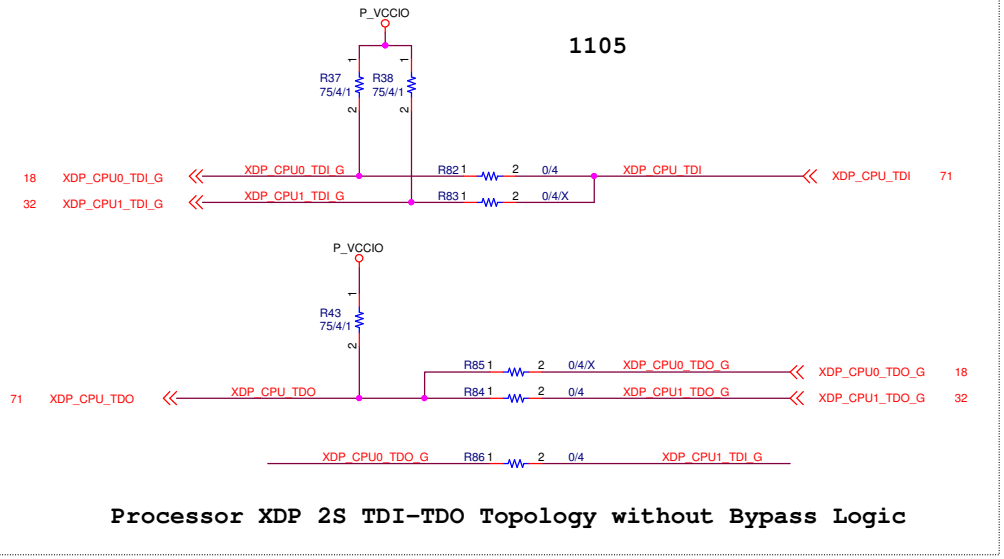
Size	Document Number	Rev
Custom	MD90-FS0	1.0

Date: Tuesday, June 09, 2015 Sheet 70 of 231



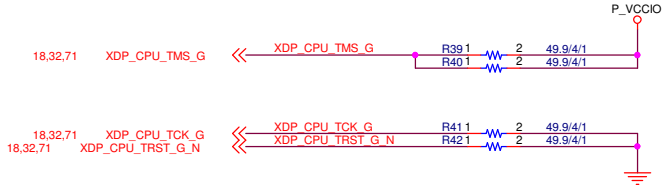
GIGABYTE™

Title	CPU_XDP	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 71 of 231	

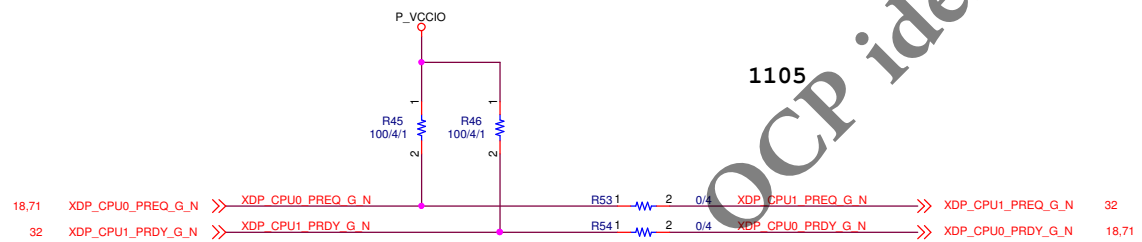


Processor XDP 2S TDI-TDO Topology without Bypass Logic

```
CAD NOTE:
* PLACE R41 WITHIN 1.1' OF CPU1'S PIN.
* PLACE R42 HAS NOT PLACEMENT CONSTRAINTS.
* PLACE R39 WITHIN 1.1' OF CPU1'S PIN.
```



1105

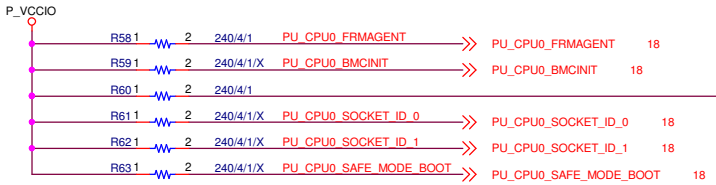


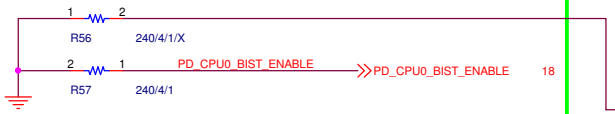
1105

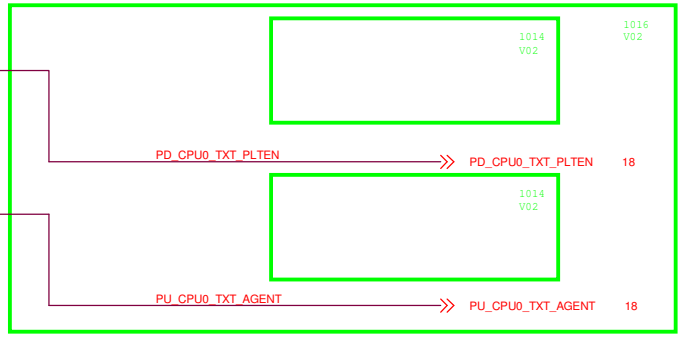
GIGABYTE™

Title: CPU JTAG		
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 72 of 231	

STRAPS (CPU0)

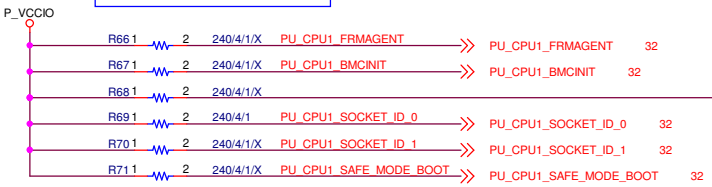


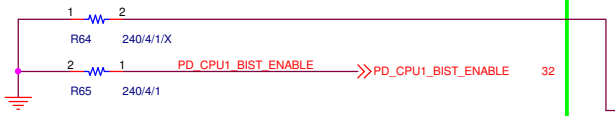


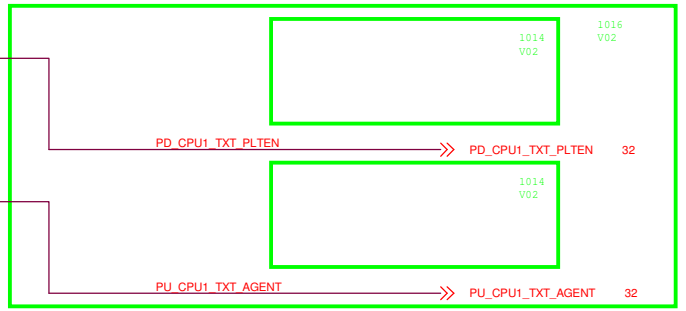


	HSX Pin Name	When Sampled	Internal PU/PD	CPU0 (Default)	CPU1 (Default)	Description	SRP1 (Mayan City) CPU0	SRP1 (Mayan City) CPU1
1	BIST_ENABLE	RESET_N deassertion	PU	1	1	Built-In Self Test (BIST): - 1 = BIST enabled - 0 = BIST disabled	STUFFED 240 ohms Pull-Down	STUFFED 240 ohms Pull-Down
2	BMCINIT	PWRGD assertion	PD	0	0	Service Processor boot mode: - 1 = CPU halts until BMC releases boot flow - 0 = Normal boot flow	EMPTY 240 ohms Pull-up	EMPTY 240 ohms Pull-up
3	FRMAGENT	PWRGD assertion	PD	1	0	Bootable Firmware Agent Strap: For Socket_ID[1:0] = 00 - 1 = Boot Flash Present, DMI Mode = DMI2 - 0 = Boot Flash Not Present, DMI Mode = DMI2 For Socket_ID[1:0] != 00 - 1 = Boot Flash NOT Present, DMI Mode = PCIE - 0 = Boot Flash NOT Present, DMI Mode = DMI2 NOTES: - For Grandly legacy CPU (Socket ID = 00) must have FRMAGENT = 1	STUFFED 240 ohms Pull-up	EMPTY 240 ohms Pull-up
4	SAFE_MODE_BOOT	PWRGD assertion	PD	0	0	Safe Mode Boot (Disables clock gating): - 1 = Safe Mode Boot enabled - 0 = Safe Mode Boot disabled	EMPTY 240 ohms Pull-up	EMPTY 240 ohms Pull-up
5	SOCKET_ID<0>	PWRGD assertion	PD	0	1	Socket Identifier: - Legacy CPU = 00 - Non-legacy CPUs = 01,10,11	SOCKET_ID<0>: EMPTY 240 ohms Pull-up SOCKET_ID<1>: EMPTY 240 ohms Pull-up	SOCKET_ID<0>: STUFFED 240 ohms Pull-up SOCKET_ID<1>: EMPTY 240 ohms Pull-up
6	SOCKET_ID<1>	PWRGD assertion	PD	0	0			
7	TXT_AGENT	PWRGD assertion	PD	1	0	TXT Agent (Drives TXT Transactions): - 1 = CPU is TXT_AGENT - 0 = CPU is not a TXT_AGENT NOTES: - Legacy CPU (Socket ID = 00) needs to be configured as TXT_AGENT if TXT_PLT_EN= 1	DIP Switch connected to 240 ohms Pull-up. - DIP Switch Default OFF	DIP Switch connected to 240 ohms Pull-up. - DIP Switch Default OFF
8	TXT_PLT_EN	PWRGD assertion	PU	1	1	TXT Enable: - 1= TXT enabled - 0= TXT disabled NOTE: All CPUs should be strapped to same value	DIP Switch connected to 240 ohms Pull-down. - DIP Switch Default ON	DIP Switch connected to 240 ohms Pull-down. - DIP Switch Default ON
10	DEBUG_EN_N	CPU_RESET	PU	1	1	In Debug Mode, enables DFX hooks: - 1 = Normal Mode - 0 = Debug Mode	Connected to XDP Pin 60 and to 475 ohms Pull-up	

STRAPS (CPU1)







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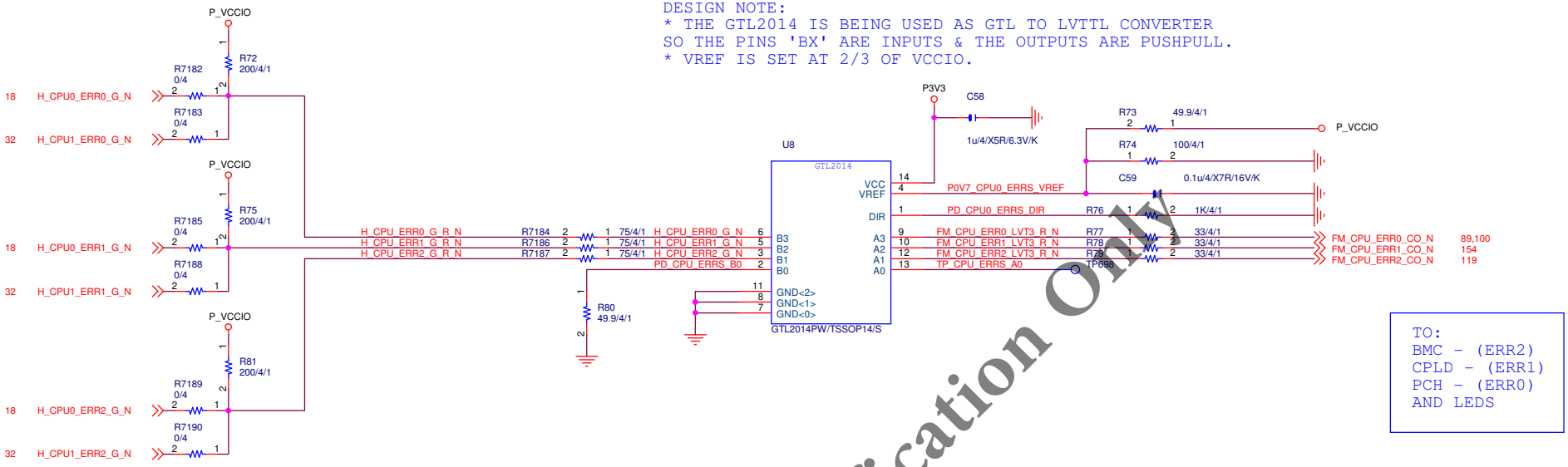
Title: CPU SIDE BAND: HW STRAPS

Size	Document Number	Rev
Custom	MD90-FS0	1.0

Date: Tuesday, June 09, 2015 Sheet 73 of 231

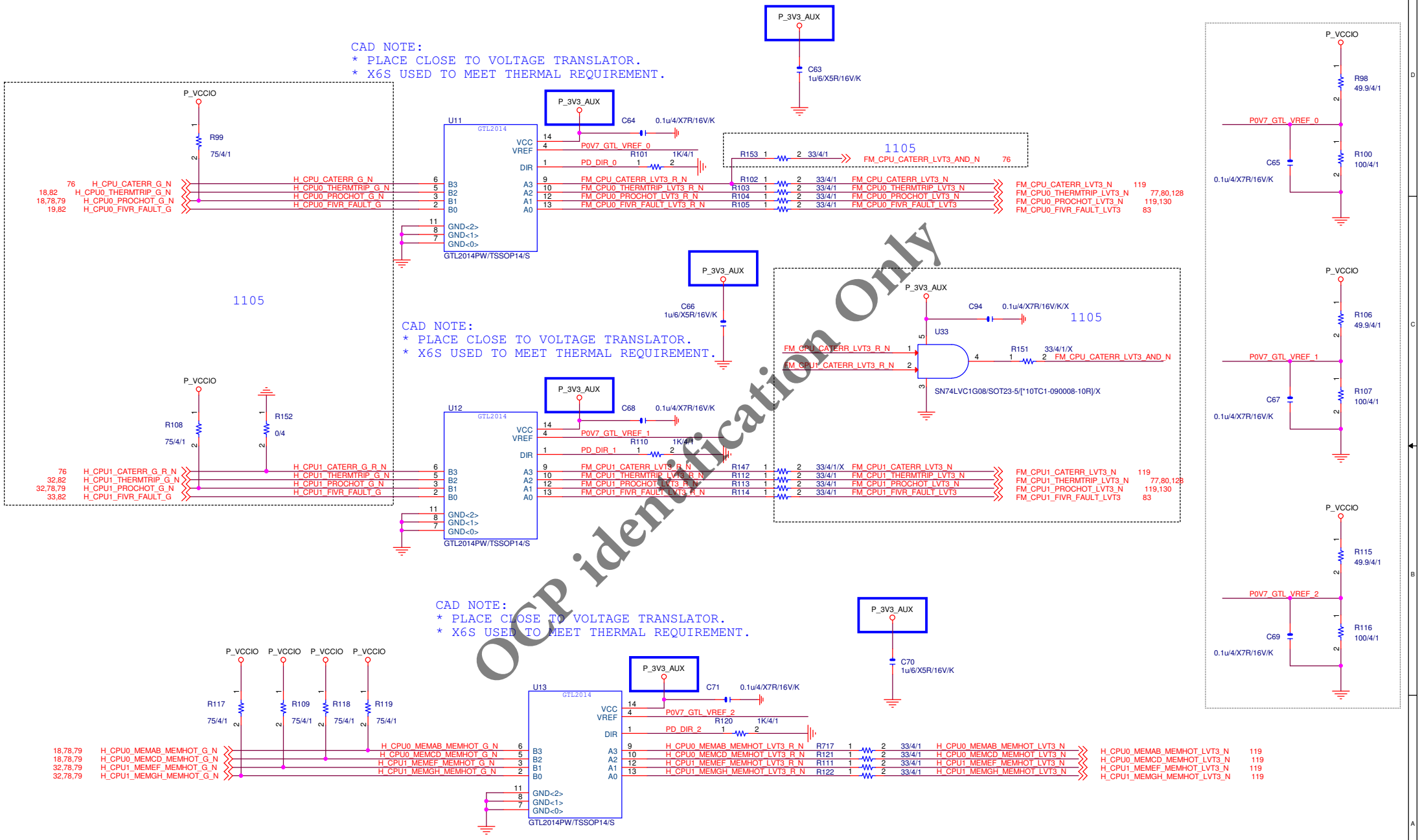


GIGABYTE™

Title: CPU SIDE BAND:ERROR CIRCUIT

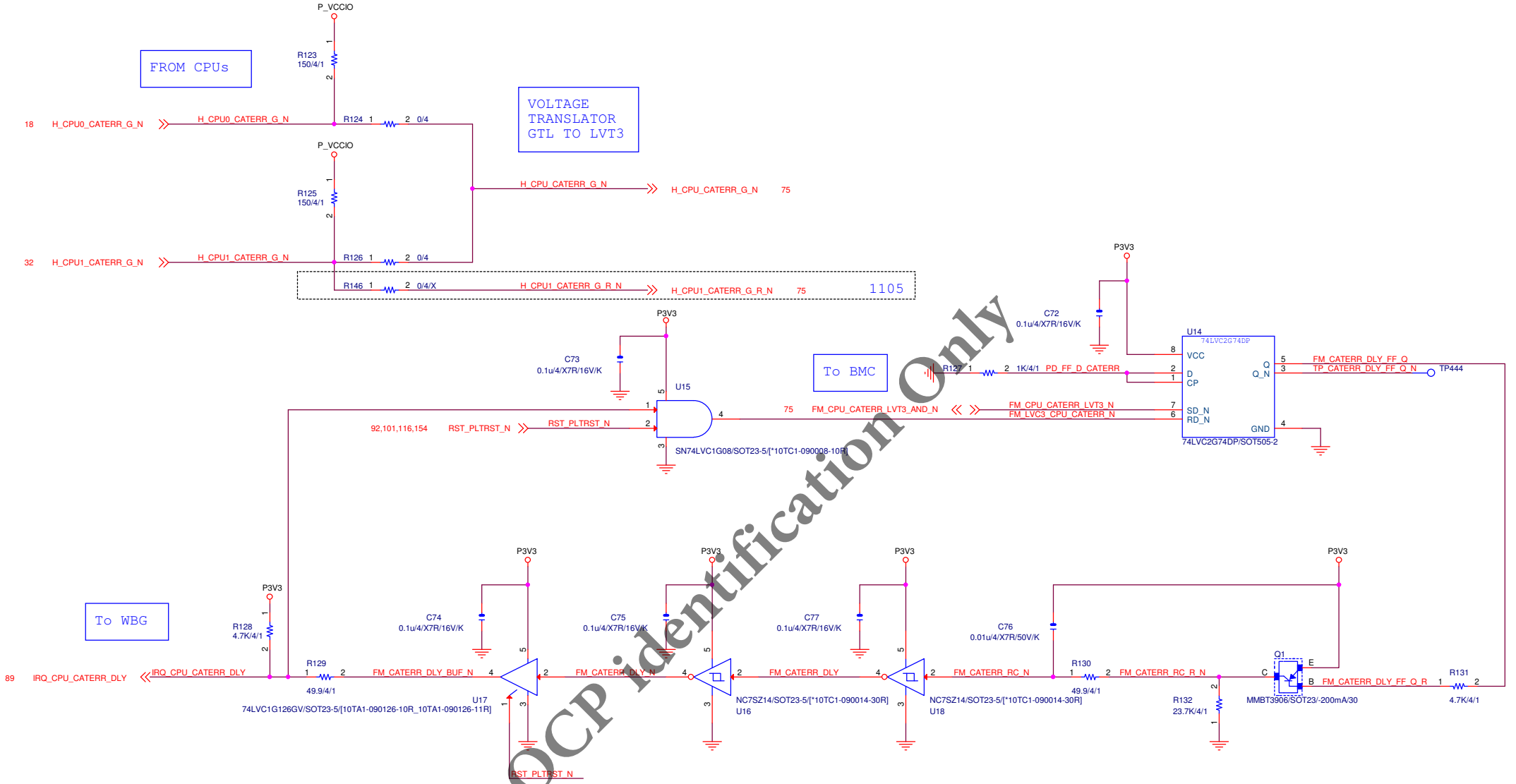
Size	Document Number	Rev
Custom	MD90-FS0	1.0

Date: Tuesday, June 09, 2015 Sheet 74 of 231



GIGABYTE™

Title	CPU SIDE BAND: VOLTAGE TRAN	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 75 of 231	

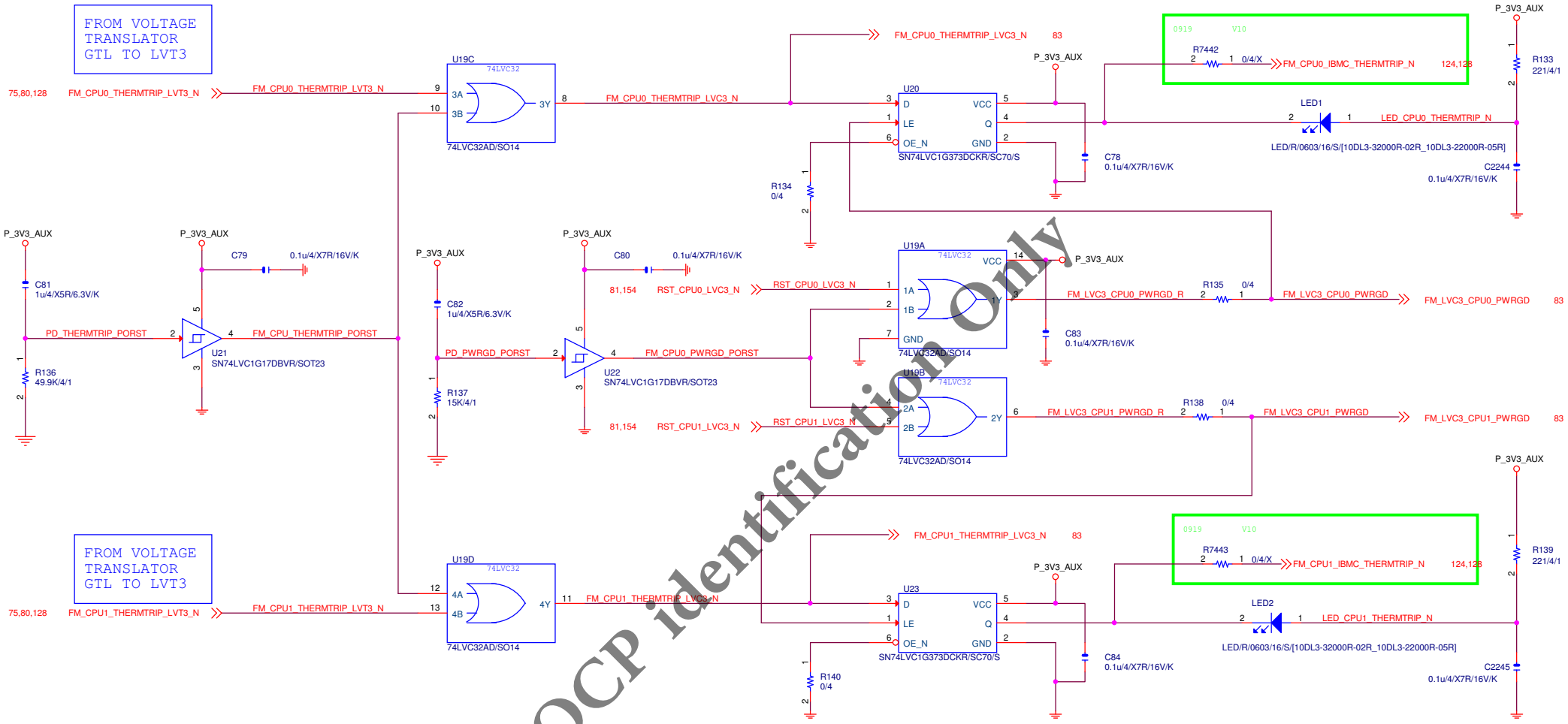


GIGABYTE™

Title: CPU SIDE BAND: CATASTROPHIC

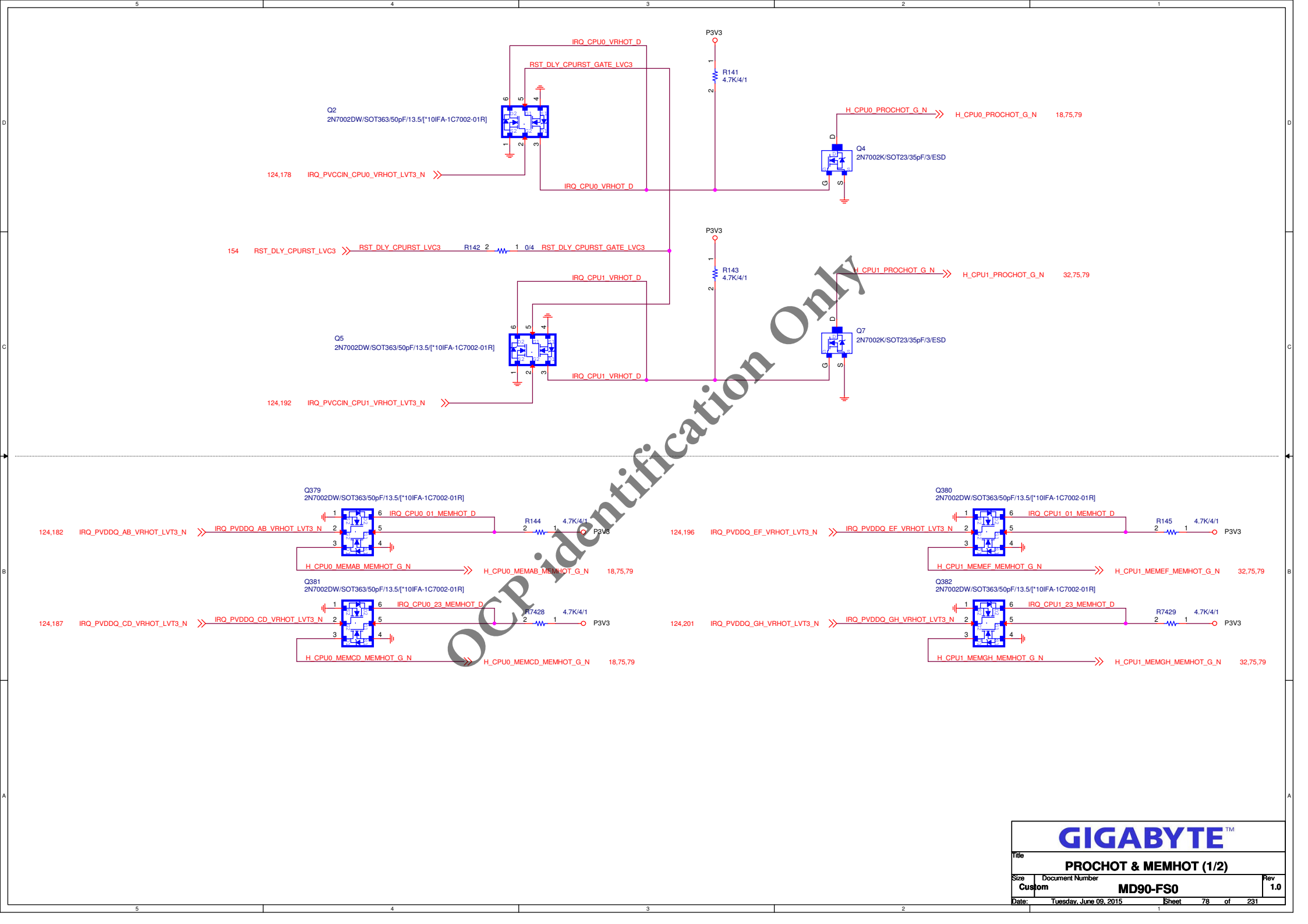
Size	Document Number	Rev
Custom	MD90-FS0	1.0

Date: Tuesday, June 09, 2015 Sheet 76 of 231



GIGABYTE™

Title	CPU SIDE BAND: THERMTRIP LA	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 77 of 231	

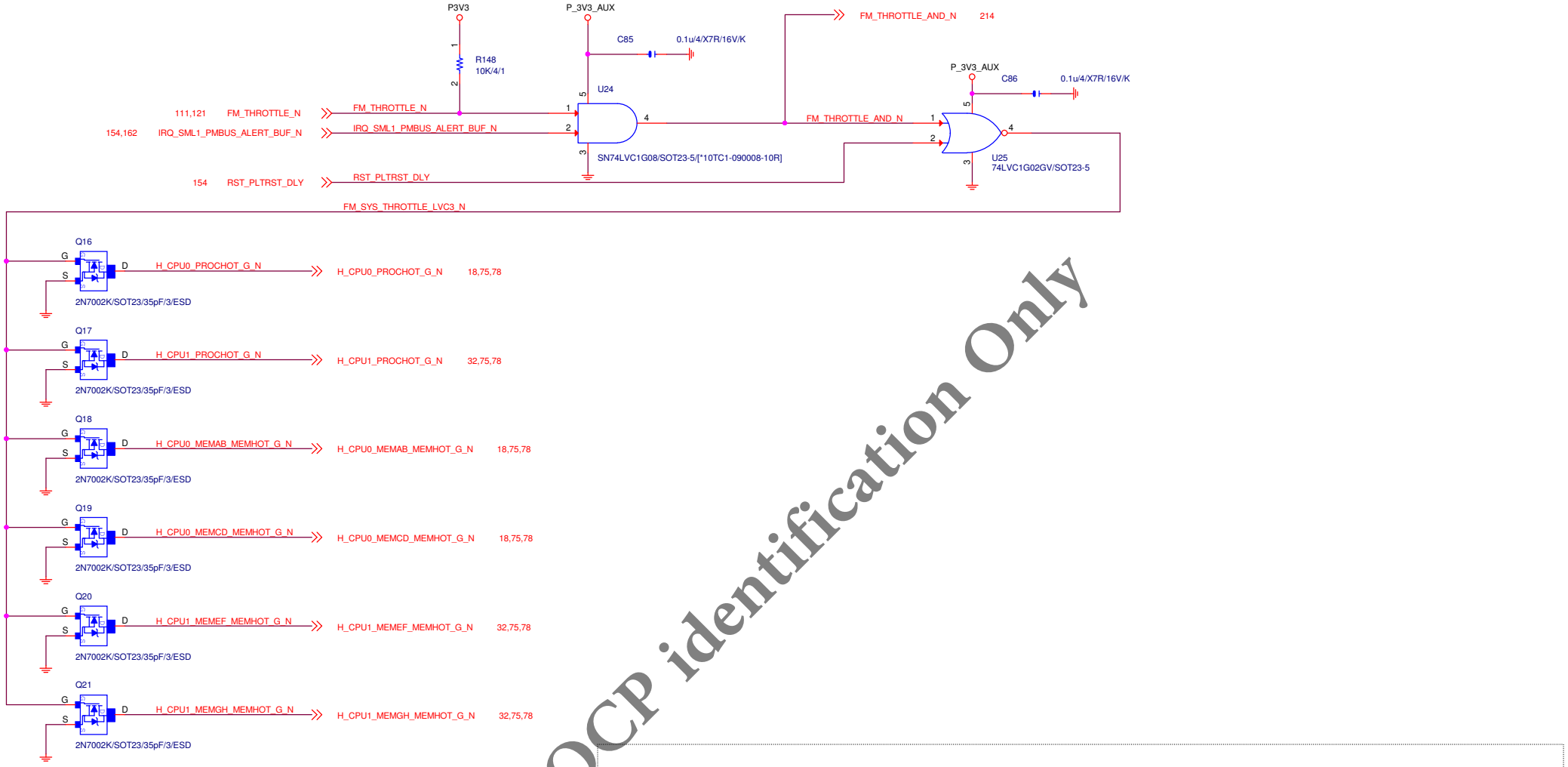


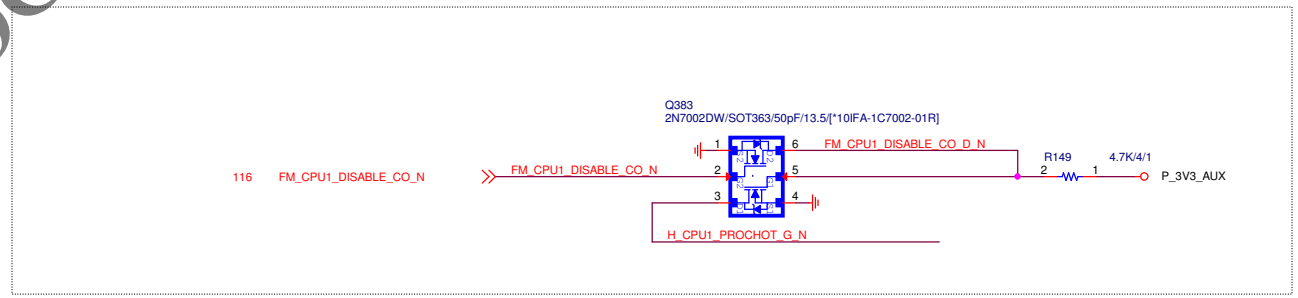
GIGABYTE™

Title: PROCHOT & MEMHOT (1/2)

Size	Document Number	Rev
Custom	MD90-FS0	1.0

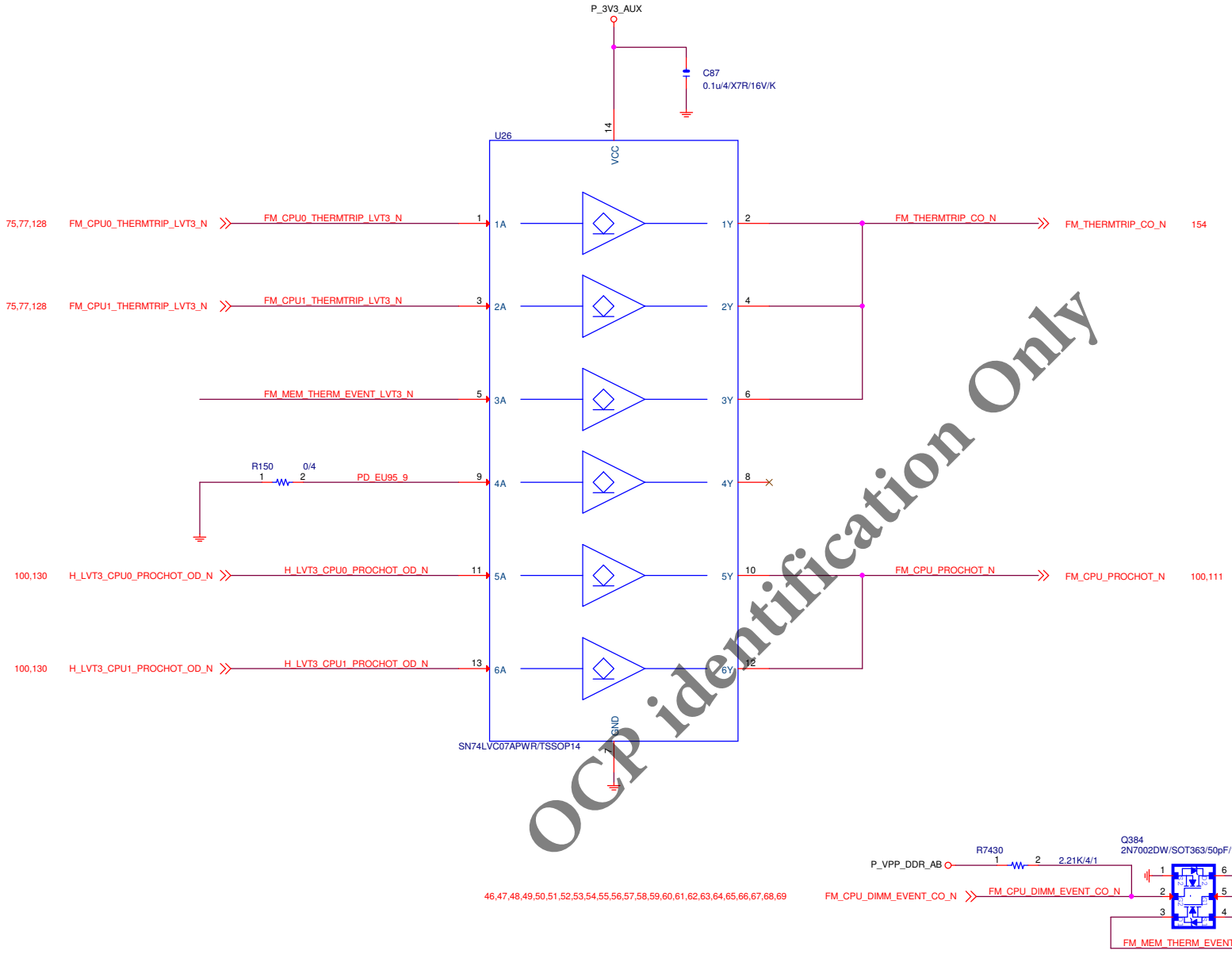
Date: Tuesday, June 09, 2015 Sheet 78 of 231





GIGABYTE™

Title	PROCHOT & MEMHOT (2/2)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 79 of 231	

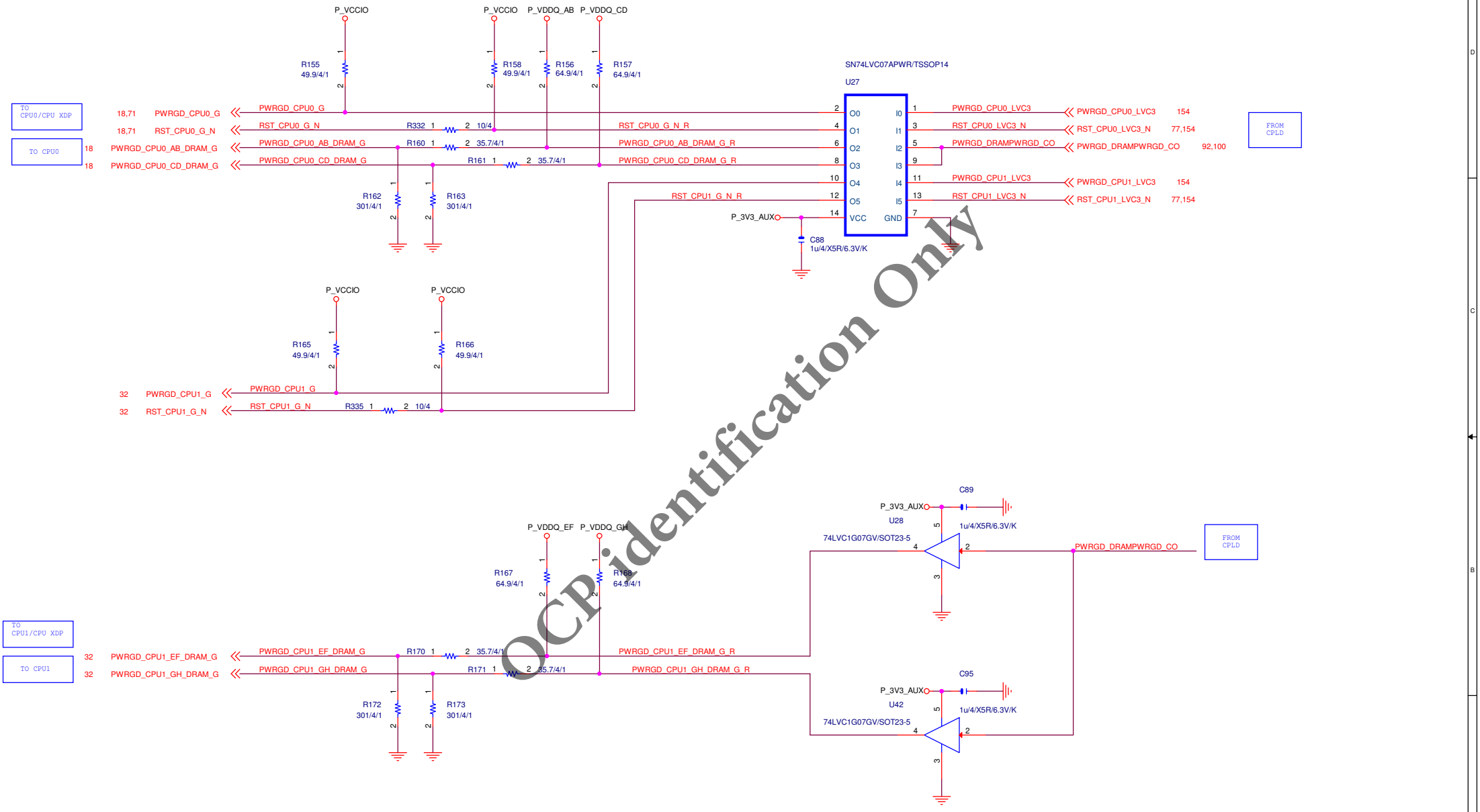


GIGABYTE™

Title: CPU SIDE BAND: DIMM EVENT

Size	Document Number	Rev
Custom	MD90-FS0	1.0

Date: Tuesday, June 09, 2015 Sheet 80 of 231



GIGABYTE™

Title: CPU SIDE BAND: RESET & PWR

Size	Document Number	Rev
Custom	MD90-FS0	1.0

Date: Tuesday, June 09, 2015 Sheet 81 of 231

CAD NOTE:
* PLACE R7U10 NEAR CPU0.
* PLACE R3U8 NEAR CPU1.

TO/FROM CPU0

TO/FROM CPU1

P_VCCIO

R174 150/4/1

R175 150/4/1

R176 0/4

18 H_CPU0_FAST_WAKE_G_N << >> H_CPU0_FAST_WAKE_G_N — H_CPU1_FAST_WAKE_G_N << >> H_CPU1_FAST_WAKE_G_N 32

CAD NOTE:
R Close to CPU0

CAD NOTE:
R Close to CPU1

TO/FROM CPU0

TO/FROM CPU1

P_VCCIO

R179 150/4/1

R180 150/4/1

18,32,82 H_CPU_MSMI_G_N << >> H_CPU_MSMI_G_N — H_CPU_MSMI_G_N << >> H_CPU_MSMI_G_N 18,32,82

CAD NOTE:
PLACE NEAR TO RESPECTIVE CPU.

P_VCCIO

R177 240/4/1

R178 240/4/1

32 PU_CPU1_EAR_G_N << PU_CPU1_EAR_G_N

18 PU_CPU0_EAR_G_N << PU_CPU0_EAR_G_N

CAD NOTE:
PACKAGE PINS PULL-UPS.
PLACE NEAR TO CPU.

P_3V3_AUX

R181 4.7K/4/1

R182 10K/4/1

18,124,154 FM_CPU0_SKTOCC_LVT3_N << FM_CPU0_SKTOCC_LVT3_N

18,154,206 FM_CPU0_BDX_PRSNT_LVT3_N << FM_CPU0_BDX_PRSNT_LVT3_N

R185 4.7K/4/1

R186 10K/4/1

32,124,154 FM_CPU1_SKTOCC_LVT3_N << FM_CPU1_SKTOCC_LVT3_N

32,154 FM_CPU1_BDX_PRSNT_LVT3_N << FM_CPU1_BDX_PRSNT_LVT3_N

CAD NOTE:
PLACE NEAR GTL2014 VT.

P_VCCIO

R183 75/4/1

R184 1K/4/1/X

18,75 H_CPU0_THERMTRIP_G_N << H_CPU0_THERMTRIP_G_N

19,75 H_CPU0_FIVR_FAULT_G << H_CPU0_FIVR_FAULT_G

R187 75/4/1

R188 1K/4/1/X

32,75 H_CPU1_THERMTRIP_G_N << H_CPU1_THERMTRIP_G_N

33,75 H_CPU1_FIVR_FAULT_G << H_CPU1_FIVR_FAULT_G

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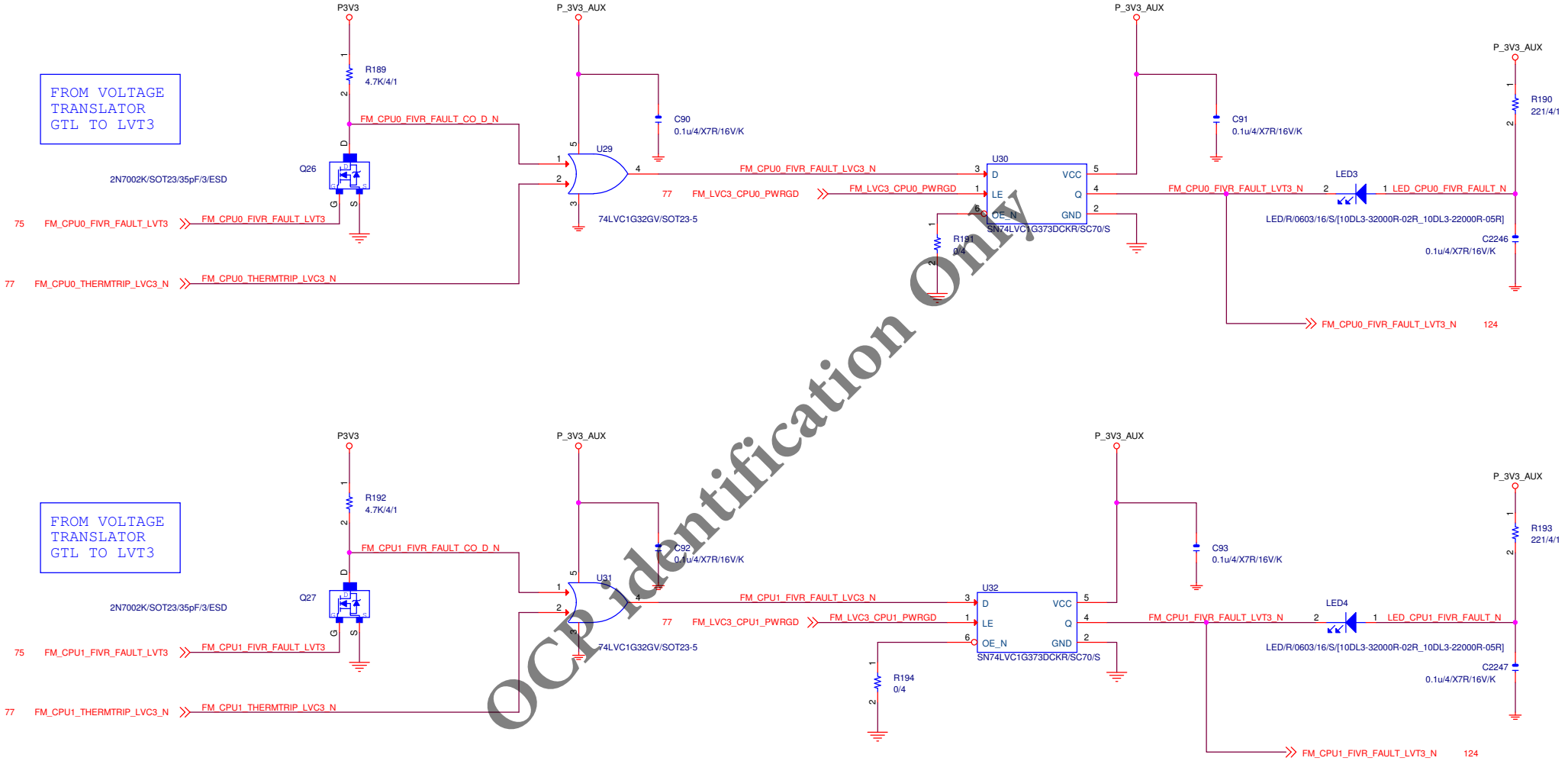
Title: CPU SIDE BAND: PULL UPS/DOWNS

Size: Custom | Document Number: MD90-FS0 | Rev: 1.0

Date: Tuesday, June 09, 2015 | Sheet 82 of 231



GIGABYTE™

Title: CPU SIDE BAND:FIVR FAULT

Size	Document Number	Rev
Custom	MD90-FS0	1.0

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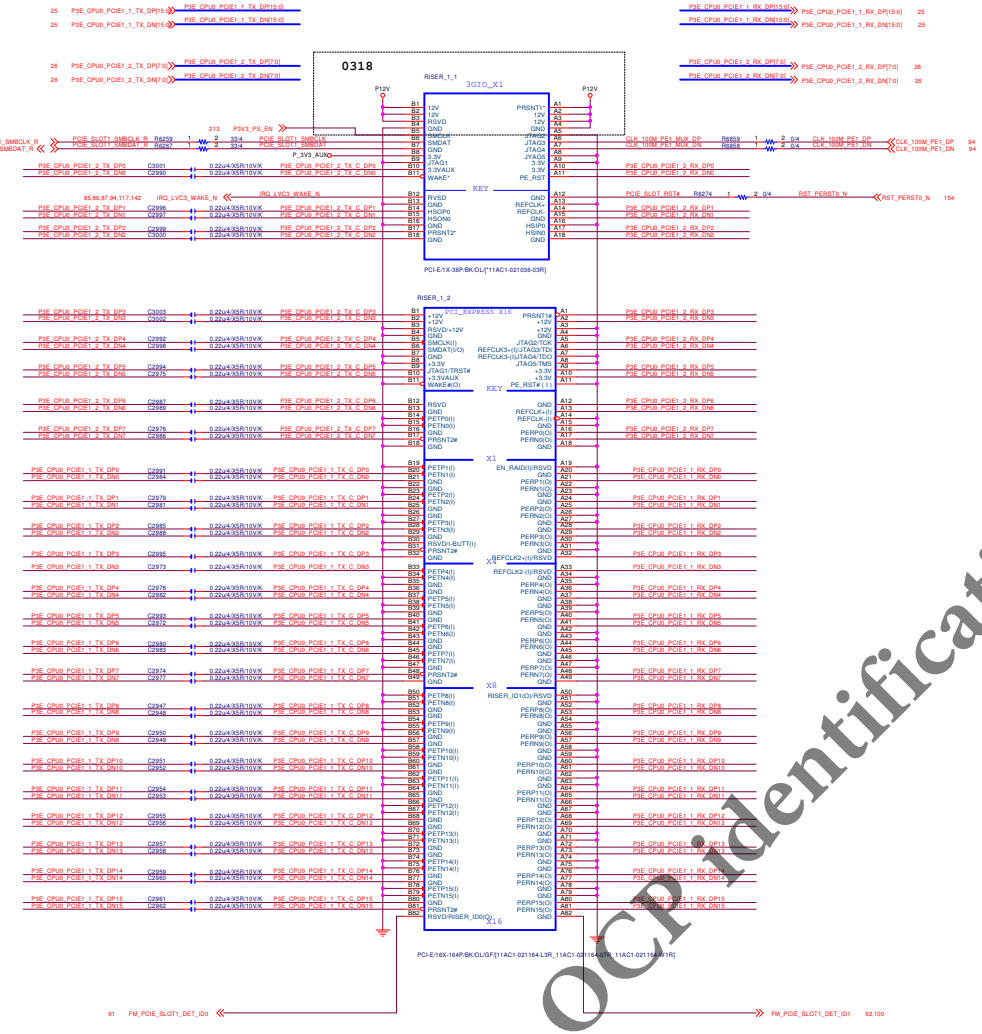
SLOT1 CPU0 PCIE 16X+8X



GIGABYTE				
Title: RISER_A (P0_Gen3x8)				
Size: D	Document Number: MD90-FS0			Rev: 1.0
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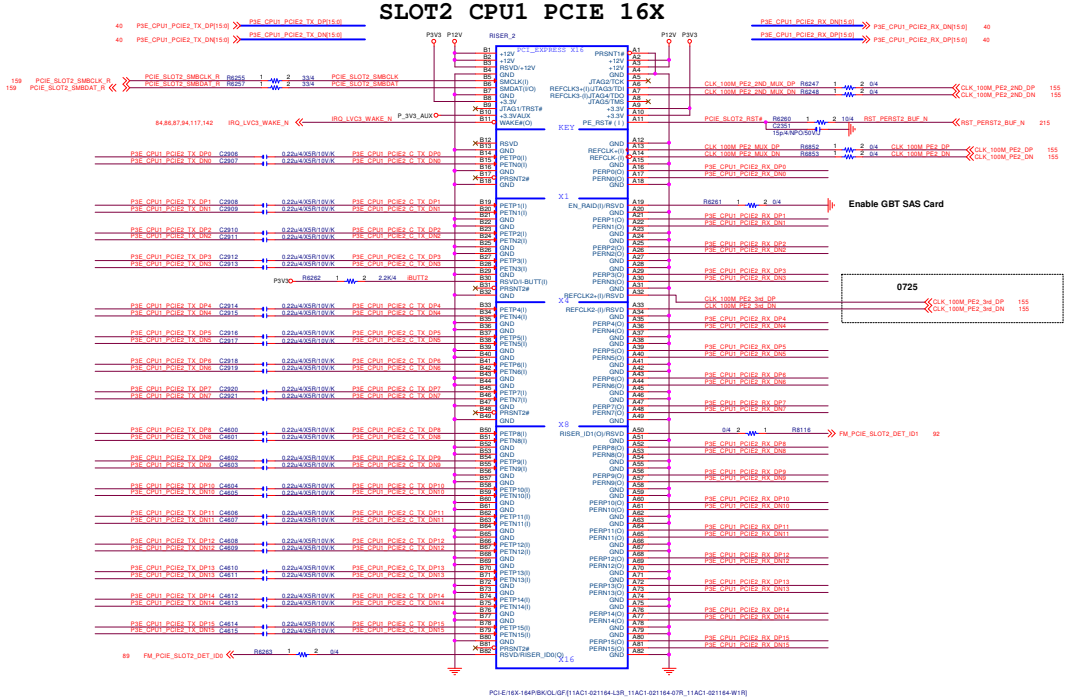
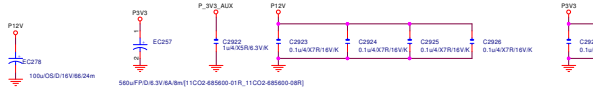
SLOT2 CPU1 PCIE 16X



PCI-E/16X-164P/BK/OL/GF[11AC1-021164-L3R_11AC1-021164-07R_11AC1-021164-W1R]



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Title	RISER_B (P0_Gen3 x4x4x8)	
Size: D	Document Number: MD90-FS0	Rev: 1.0
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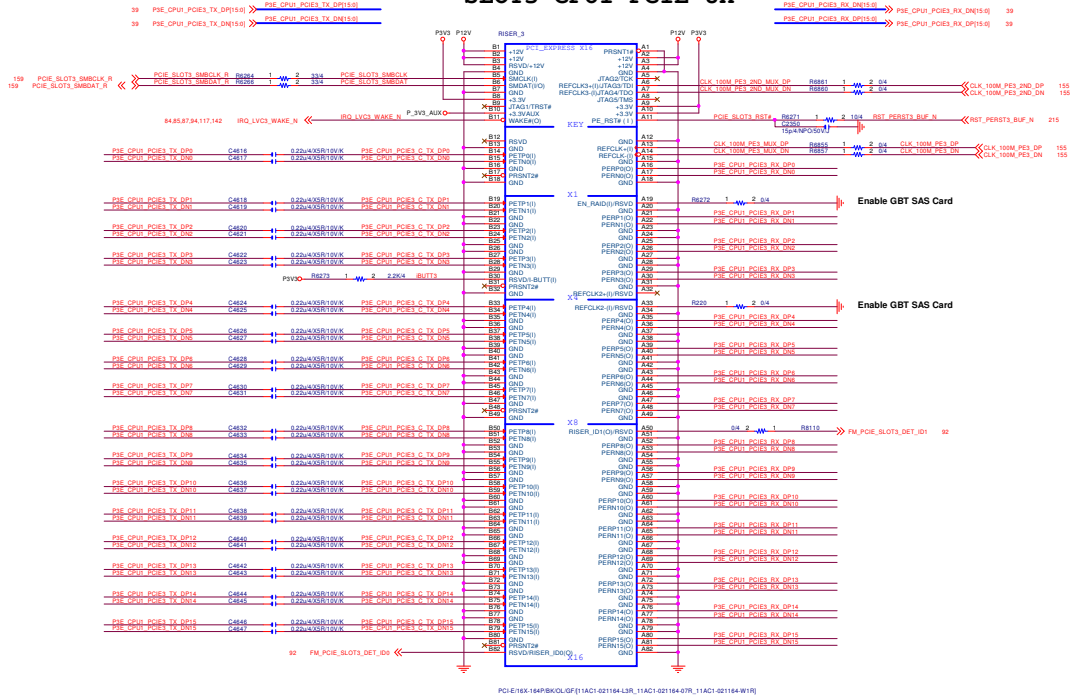
SLOT3 CPU1 PCIE 8X



GIGABYTE

Title	RISER_C (P1_Gen3 x4x4x8)	
Size: D	Document Number: MD90-FS0	Rev: 1.0
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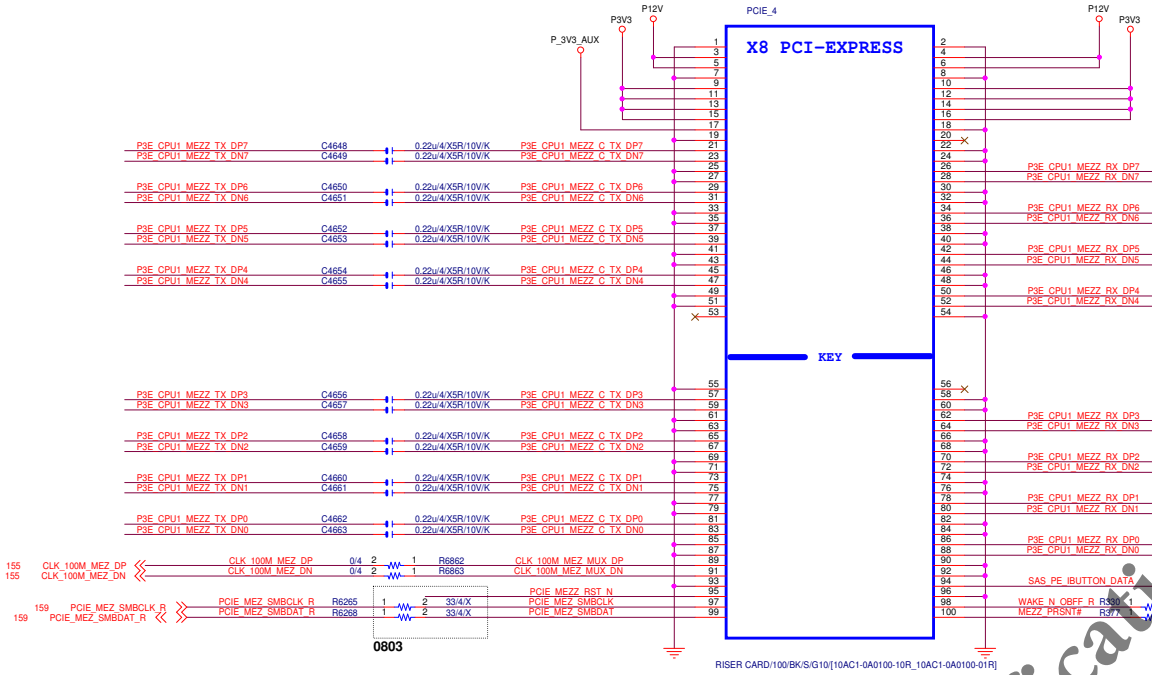
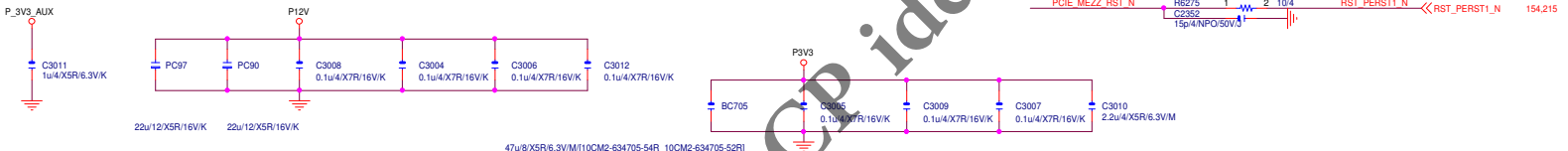
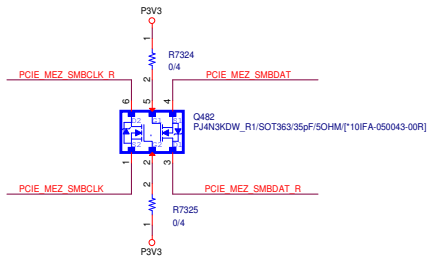


POWER RAIL	X4/X8/X16
+3.3V VOLTAGE TOLERANCE SUPPLY CURRENT	+/- 9% 3.0A (MAX)
+12V VOLTAGE TOLERANCE SUPPLY CURRENT	+/- 8% 5.5A (MAX)
+3.3VAUX VOLTAGE TOLERANCE SUPPLY CURRENT	+/- 9% 375mA (MAX)

Connector Type (Electrical)	Pins That Should Use Un-plated Vias
x1	B12, B17***
X4	B12, B30, A32, A19, B17***
X8	B12, B30, A32, A33, A19, B17***, B31***, B48***
X16	B12, B30, A32, A33, A50, A19, B17***, B31***, B48***, B81***





Title	BLANK		
Size C	Document Number MD90-FS0		Rev 1.0
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Title

====== PCH_Wellsburg ======

Size	Document Number	Rev
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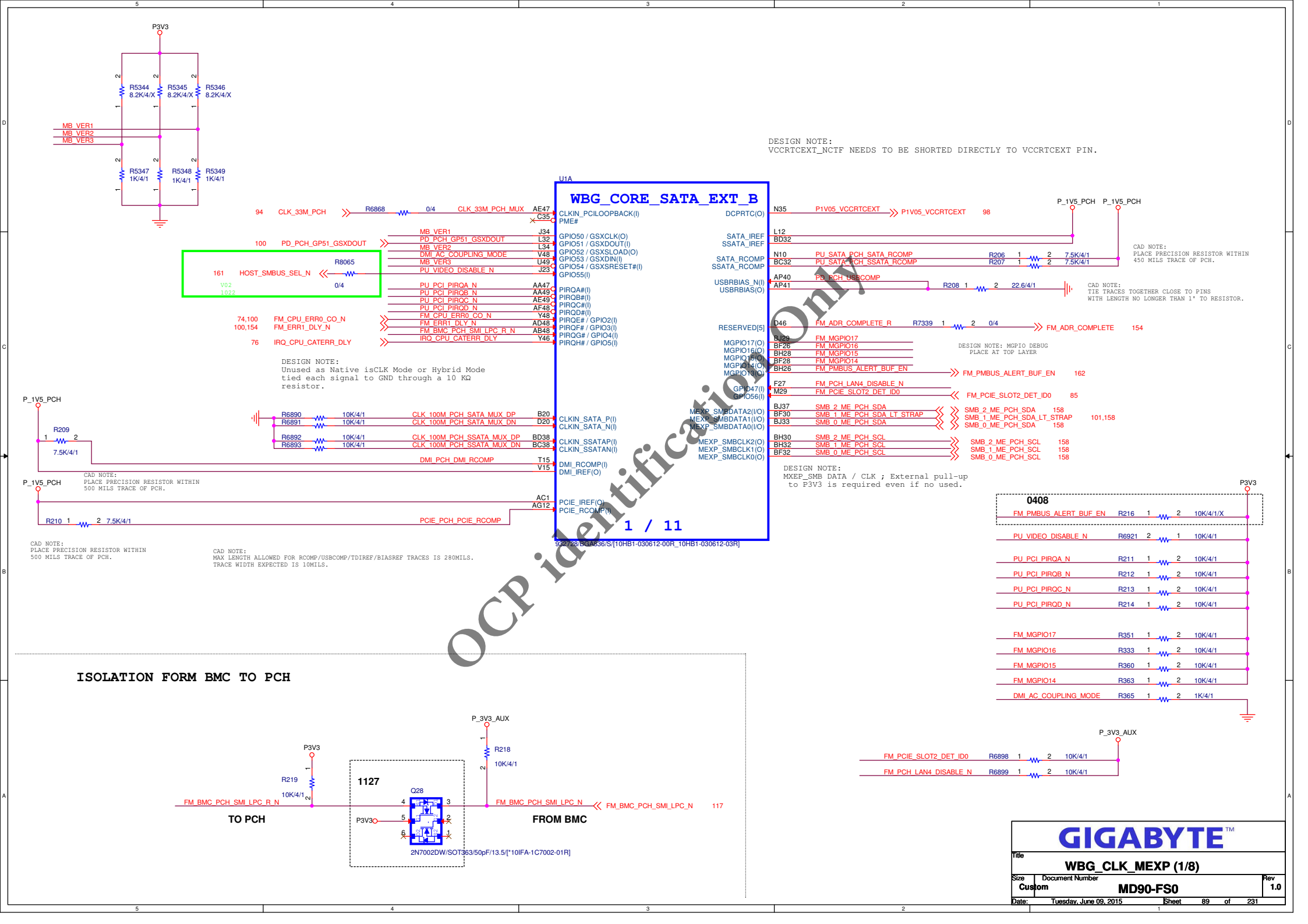

Title	WBG_CLK_MEXP (1/8)
Size	Custom
Document Number	MD90-FS0
Rev	1.0
Date:	Tuesday, June 09, 2015
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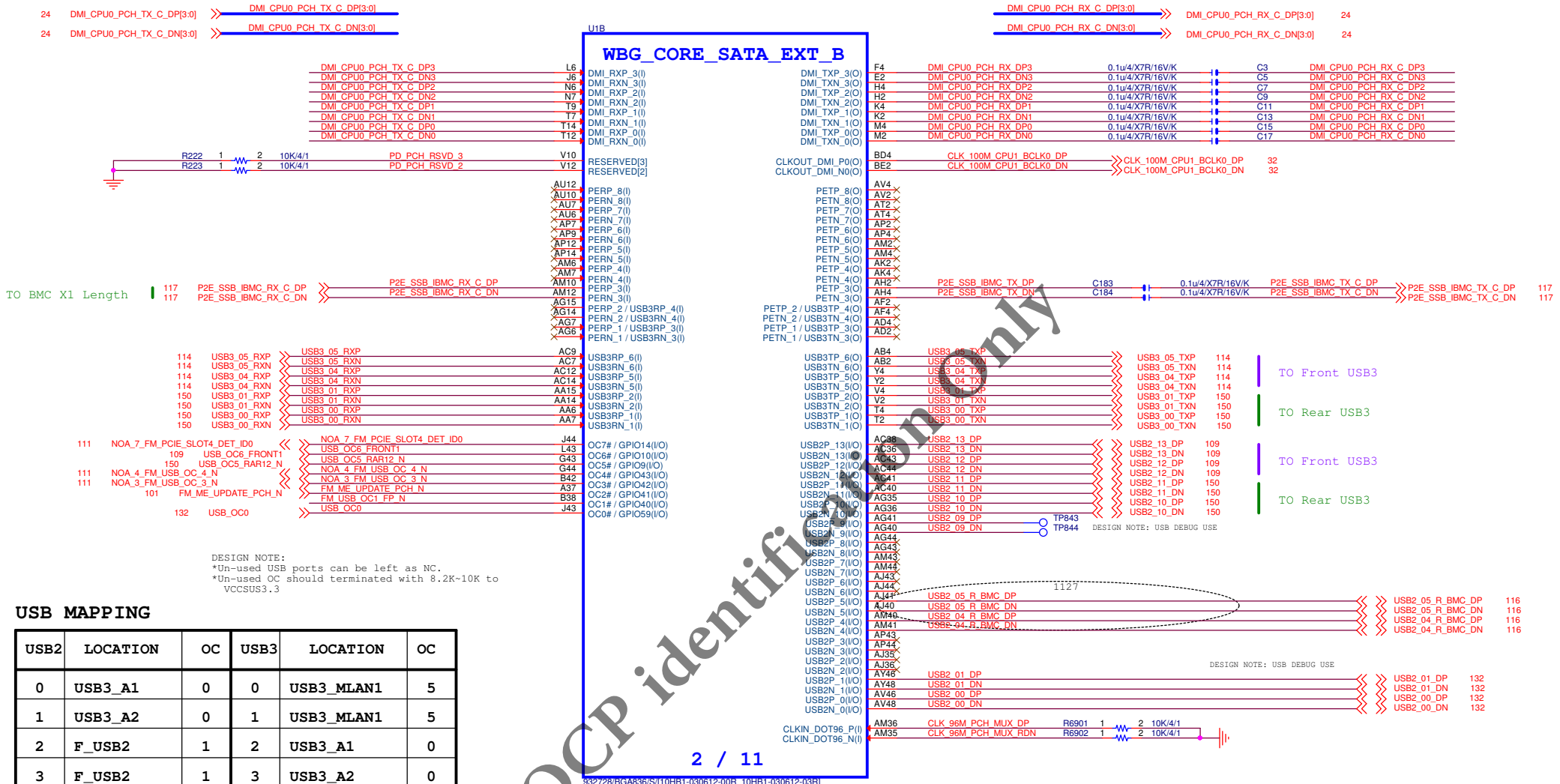

DESIGN NOTE:
*Un-used USB ports can be left as NC.
*Un-used OC should terminated with 8.2K~10K to VCCSUS3.3

USB MAPPING

USB2	LOCATION	OC	USB3	LOCATION	OC
0	USB3_A1	0	0	USB3_MLAN1	5
1	USB3_A2	0	1	USB3_MLAN1	5
2	F_USB2	1	2	USB3_A1	0
3	F_USB2	1	3	USB3_A2	0
4	To BMC	N/A	4	F_USB1	6
5	To BMC	N/A	5	F_USB1	6
6	NC	N/A			
7	NC	N/A			
8	NC	4			
9	USB Debug	4			
10	USB3_MLAN1	5			
11	USB3_MLAN1	5			
12	F_USB1	6			
13	F_USB1	6			

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Title: WBG_DMI_PCIE_USBOC (2/8)

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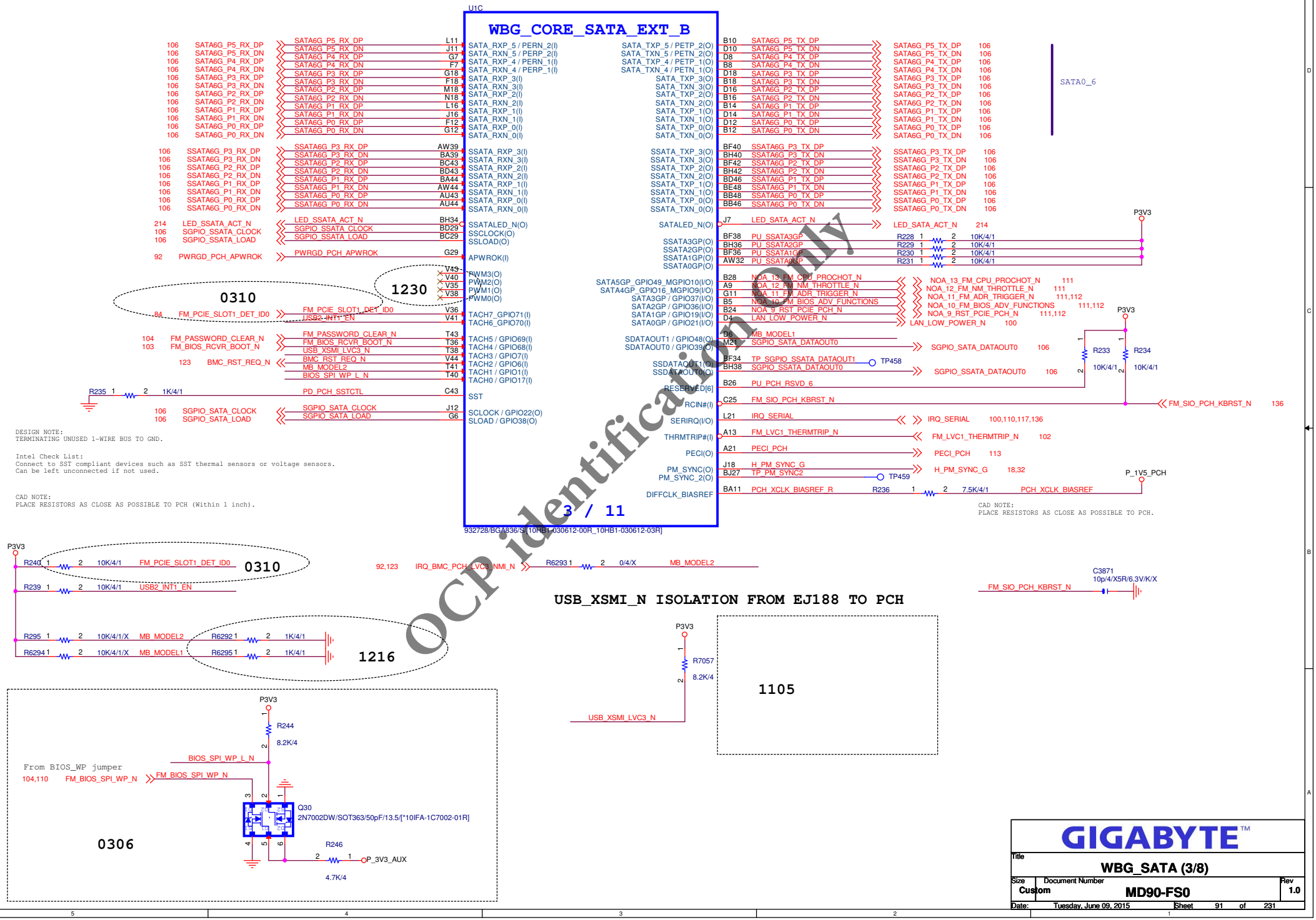
U1C
WBG_CORE_SATA_EXT_B
3 / 11
932728/BGA836/S/[10HB1-030612-00R_10HB1-030612-03R]
SATA0_6
0310
1230
1216
1105
USB_XSMI_N ISOLATION FROM EJ188 TO PCH
DESIGN NOTE:
TERMINATING UNUSED 1-WIRE BUS TO GND.
Intel Check List:
Connect to SST compliant devices such as SST thermal sensors or voltage sensors.
Can be left unconnected if not used.
CAD NOTE:
PLACE RESISTORS AS CLOSE AS POSSIBLE TO PCH (Within 1 inch).
CAD NOTE:
PLACE RESISTORS AS CLOSE AS POSSIBLE TO PCH.
From BIOS_WP jumper
Q30
2N7002DW/SOT363/50pF/13.5/[*10IFA-1C7002-01R]
OCP identification only
GIGABYTE
Title
WBG_SATA (3/8)
Size
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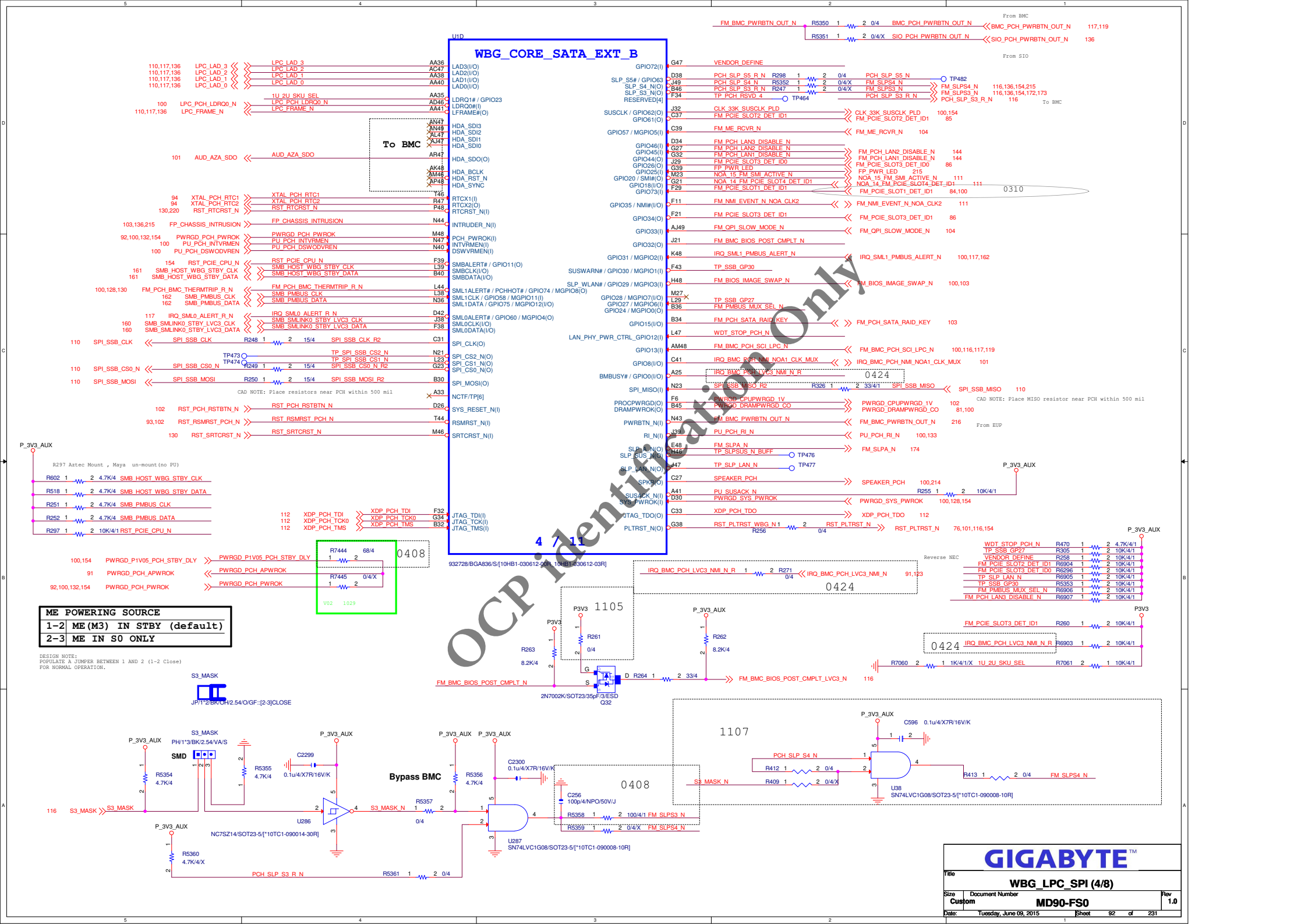
WBG_CORE_SATA_EXT_B
U1D
To BMC
From BMC
From SIO
From EUP
To BMC
OCP identification Only
4 7 11
932728/BGA836/S/[10HB1-030612-00R, 10HB1-030612-03R]
ME POWERING SOURCE
1-2 ME(M3) IN STBY (default)
2-3 ME IN S0 ONLY
DESIGN NOTE:
POPULATE A JUMPER BETWEEN 1 AND 2 (1-2 Close)
FOR NORMAL OPERATION.
R297 Aztec Mount , Maya un-mount(no PU)
CAD NOTE: Place resistors near PCH within 500 mil
CAD NOTE: Place MISO resistor near PCH within 500 mil
Reverse NEC
Bypass BMC
SMD
0310
0424
0408
1105
1107
GIGABYTE
Title
WBG_LPC_SPI (4/8)
Size Custom
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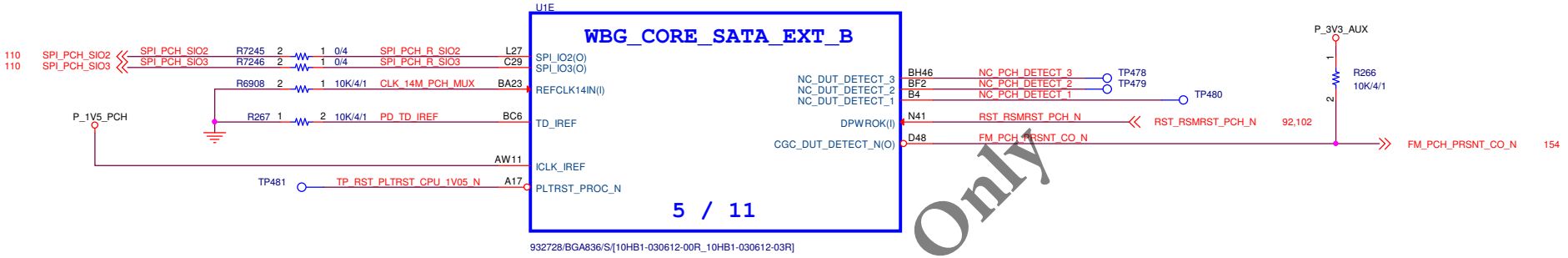

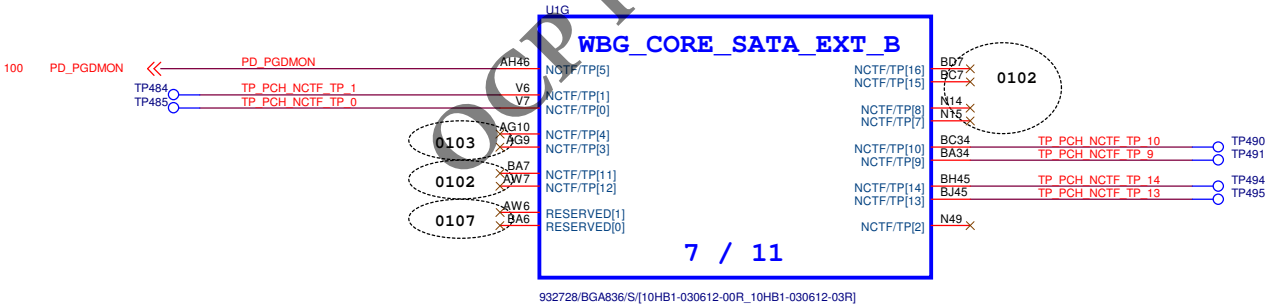

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Title	WBG (5/8)	
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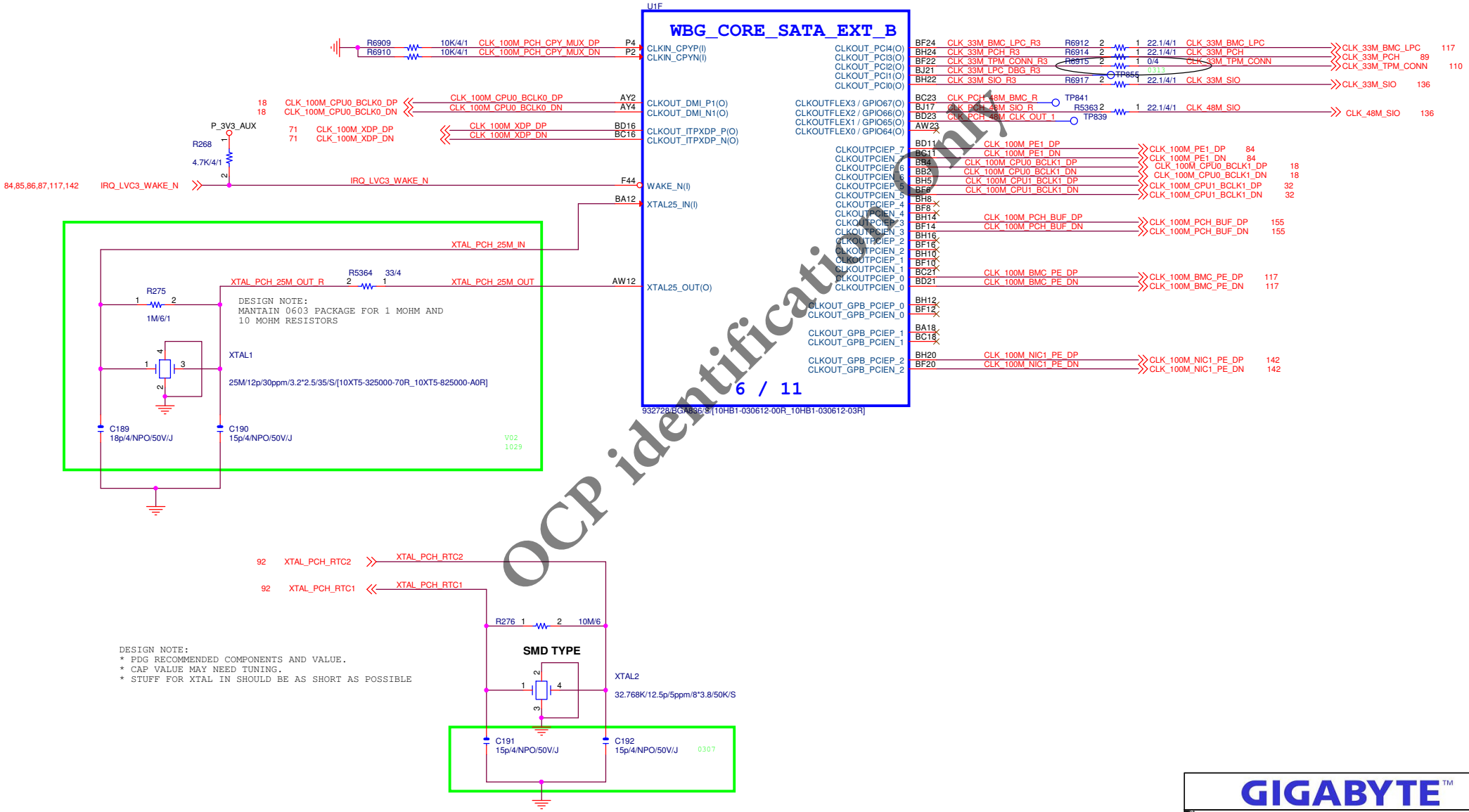

GIGABYTE™

Title: WBG_ISCLK (6/8)

Size: Custom | Document Number: MD90-FS0 | Rev: 1.0

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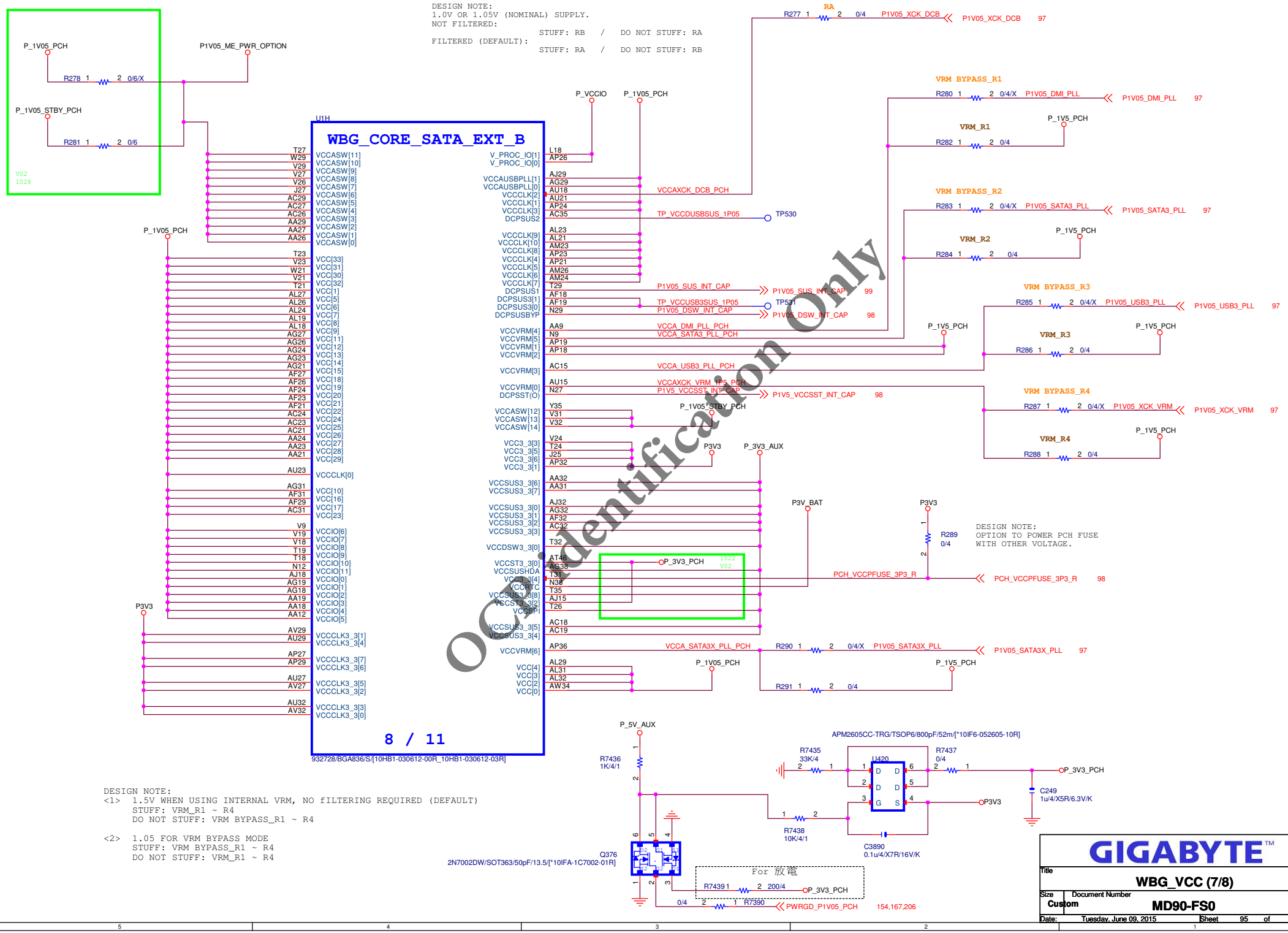

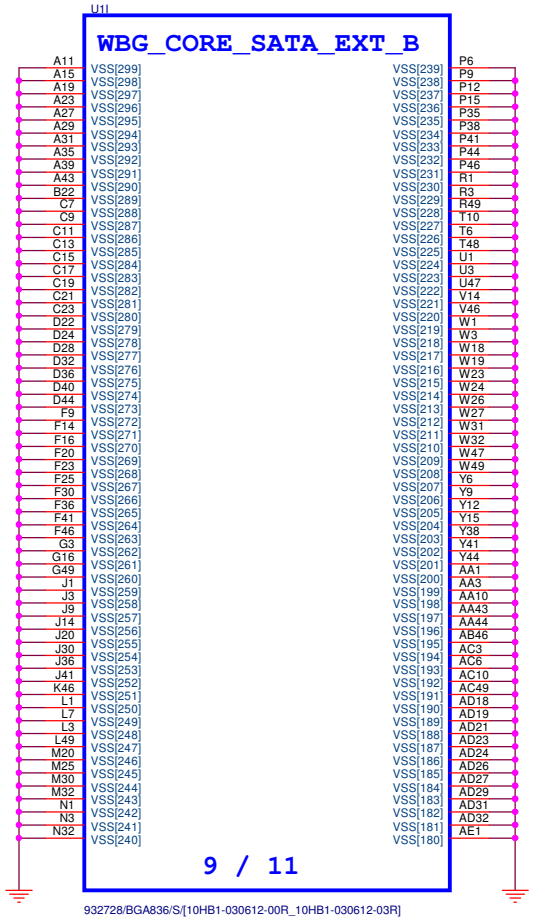

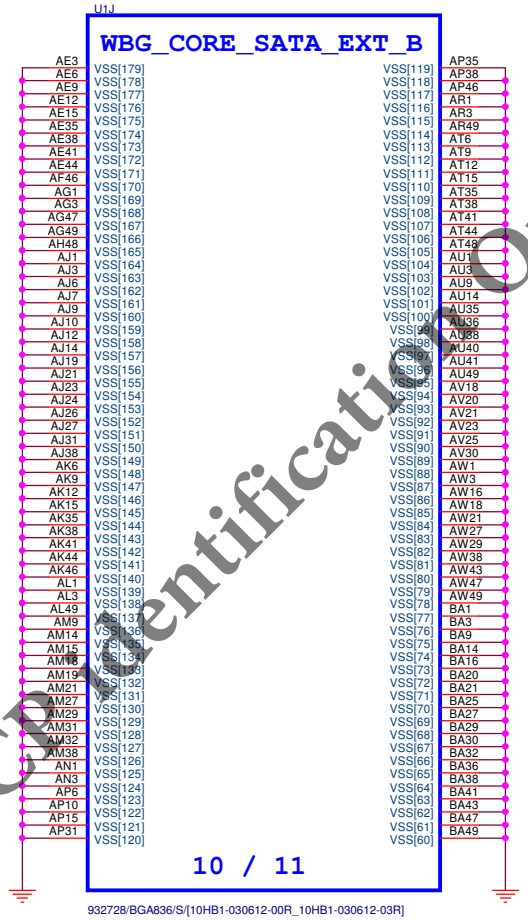

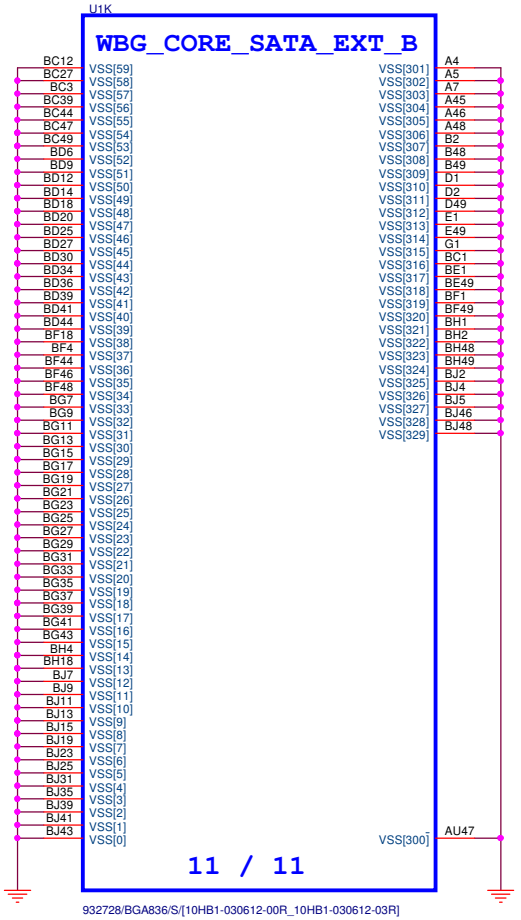

GIGABYTE™

Title: WBG_GND (8/8)		
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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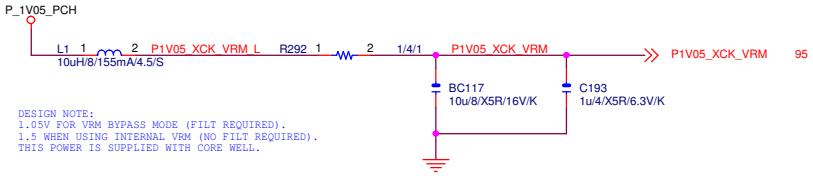
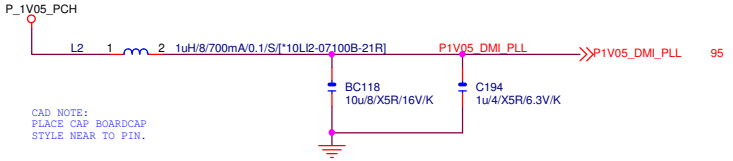
P1V05_XCK_VRM - CLOCK INTEGRATION

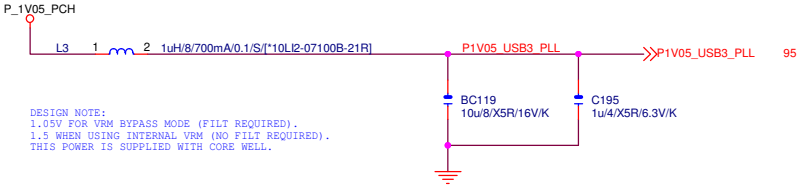


DMI PLL FILTER

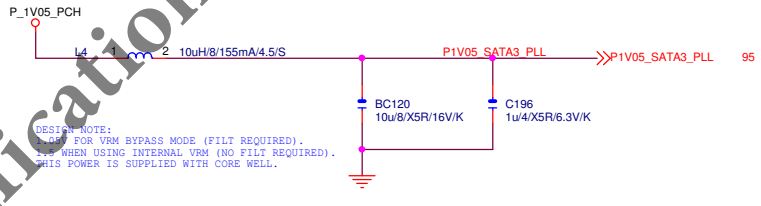
1.05V PCIE/DMI SECTION



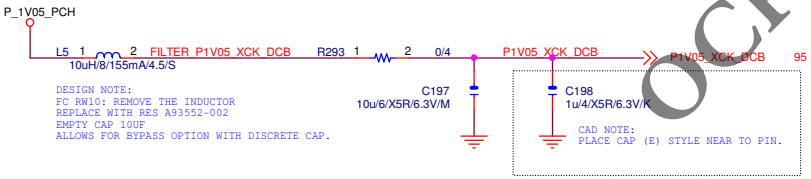
USB3 PLL FILTER



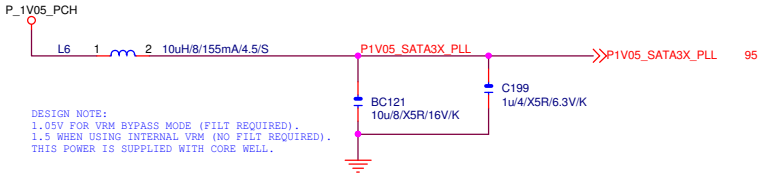
SATA PLL FILTER



P1V05_XCK_DCB - CLOCK INTEGRATION



SATAX PLL FILTER



CAD NOTE:
PUT L & C AS CLOSE AS POSSIBLE WITH THE 10MIL TRACE MAX LENGTH OF 240MIL
A MINIMUM TRACE WIDTH OF 35MIL IS REQUIRED TO INTERCONNECT THE RESISTANCES

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Title	WBG_FILTERING (1/2)	
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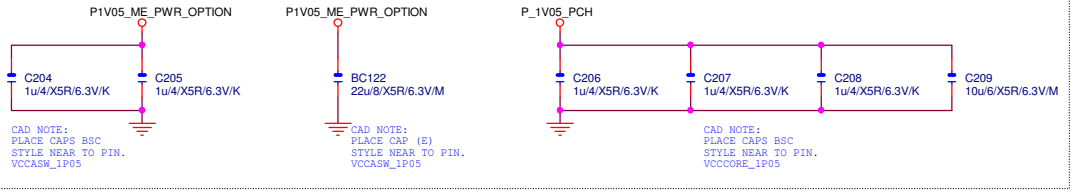
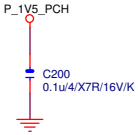
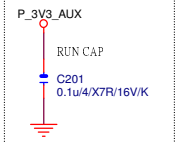
1.05V CORE/ASW/SUS FOR CORE SECTION



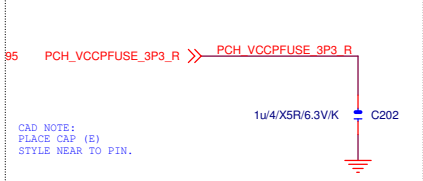
1.5V TSENSE



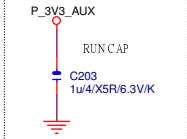
3.3V SUS AZA SECTION



3.3V FUSE SECTION

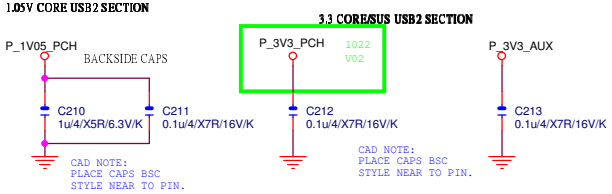


3.3V SPI SECTION

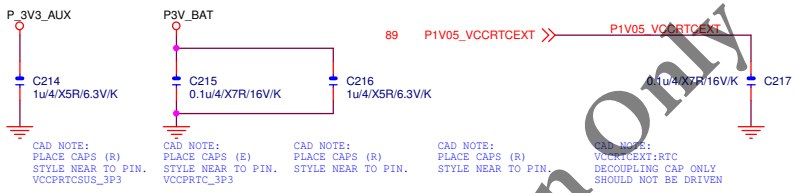


1.05V CORE USB2 SECTION

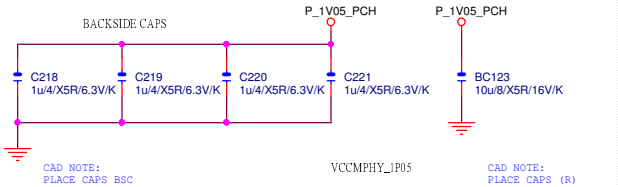
3.3 CORE/SUS USB2 SECTION



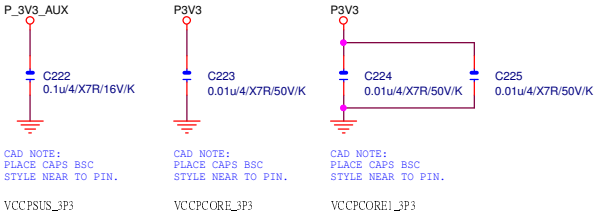
3.3V DSW/RTC FOR RTC SECTION



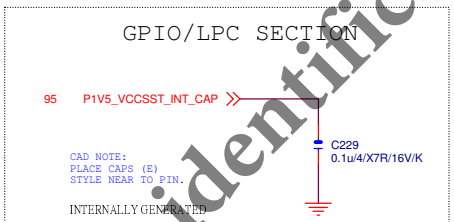
1.05V PCIE/DMI/SATA SECTION

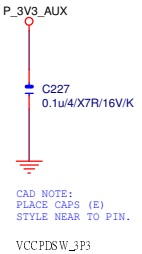


3.3V SUS/DSW/CORE FOR GPIO/LPC SECTION

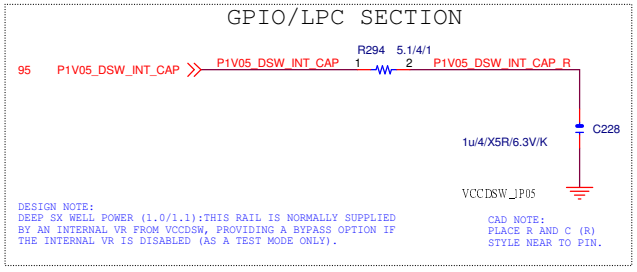


GPIO/LPC SECTION

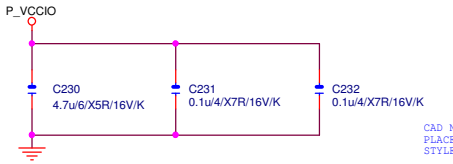




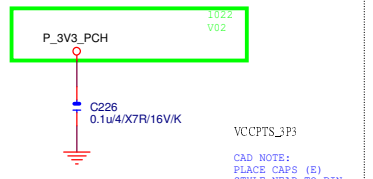
GPIO/LPC SECTION



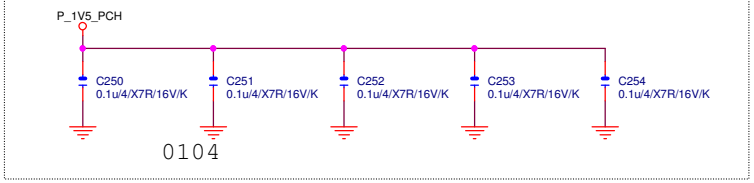
VCCIO2PCH FOR CPU SECTION



3.3V CORE THERMAL SENSOR



CAD NOTE: BSD: BACK SIDE COMPONENT E: EDGE R: RUN



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Title: WBG DECOUPLING (1/2)

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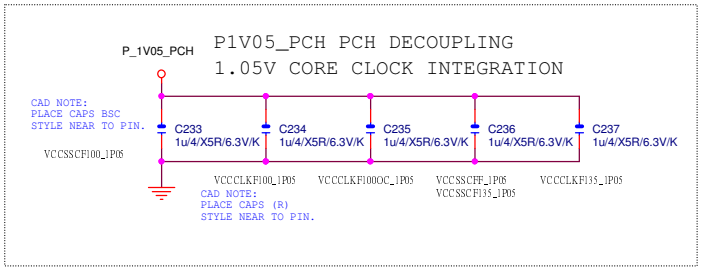

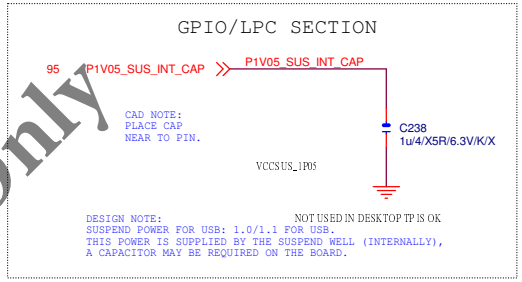

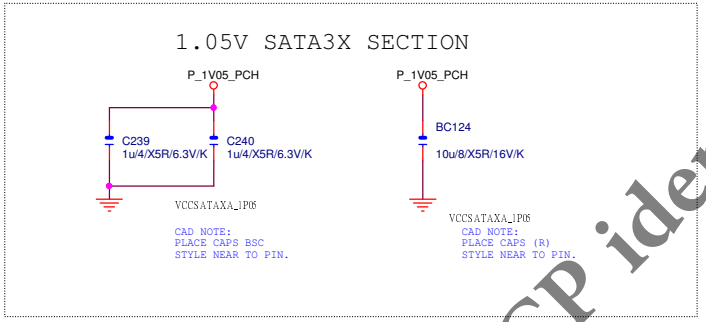

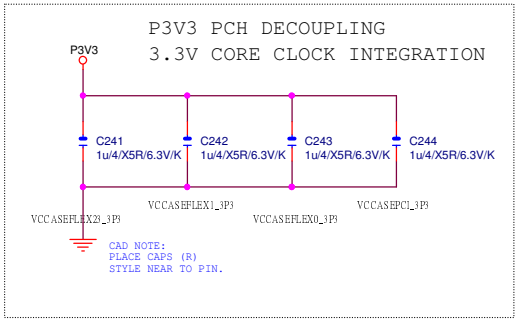

GIGABYTE™

Title	WBG DECOUPLING (2/2)	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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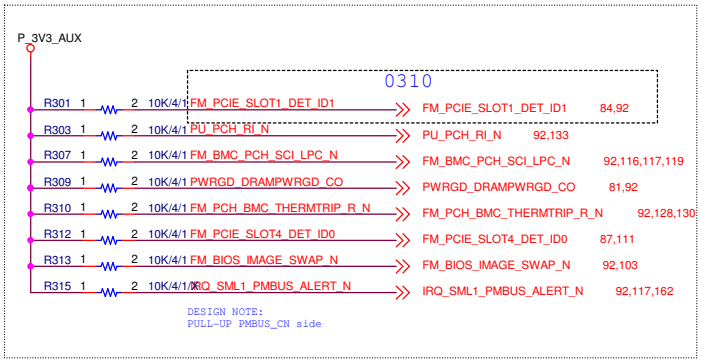

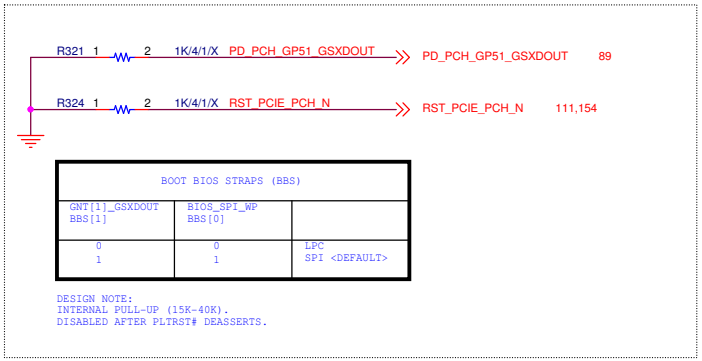

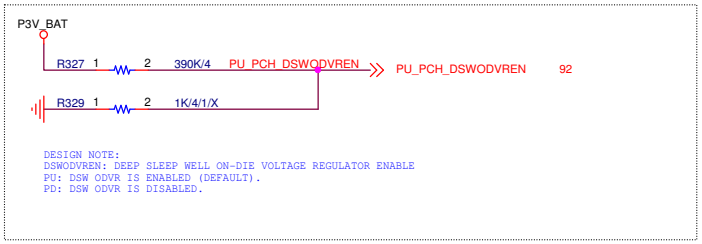

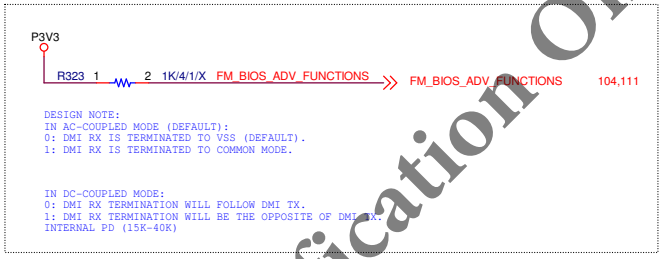

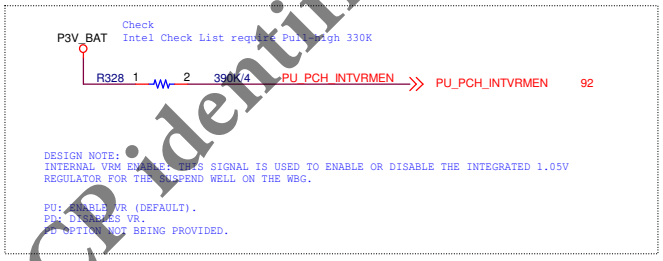

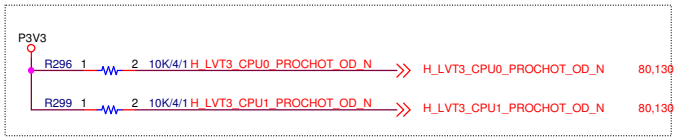

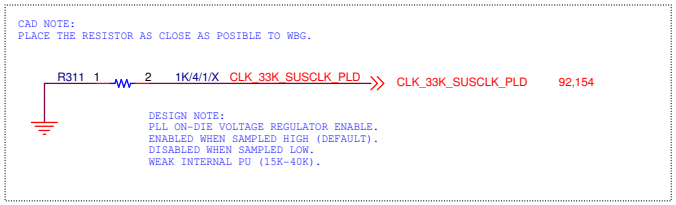

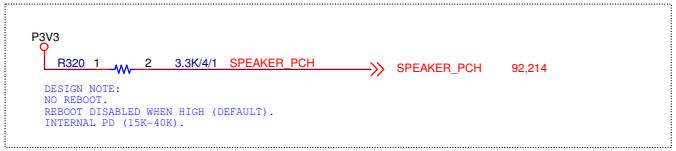

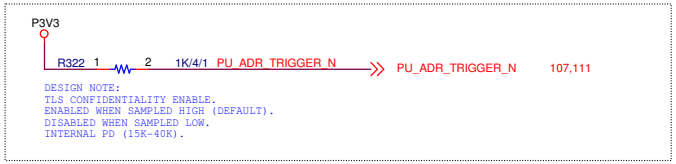

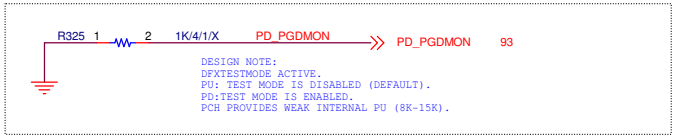

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Title	WBG STRAPPING/MISC (1/2)	
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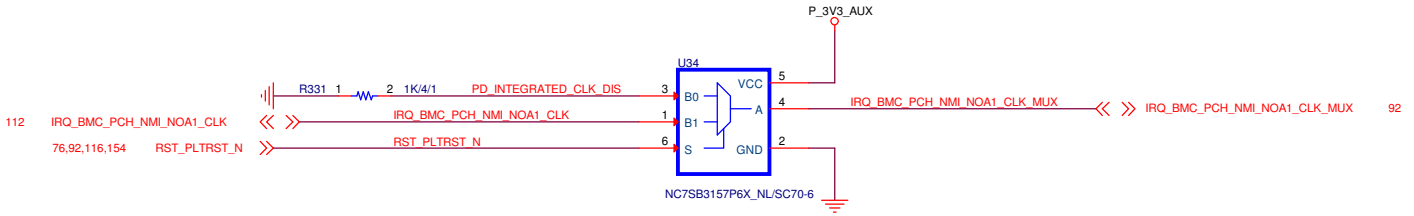
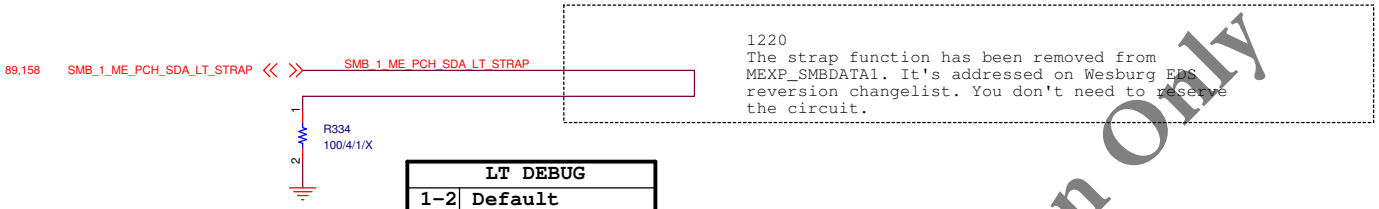
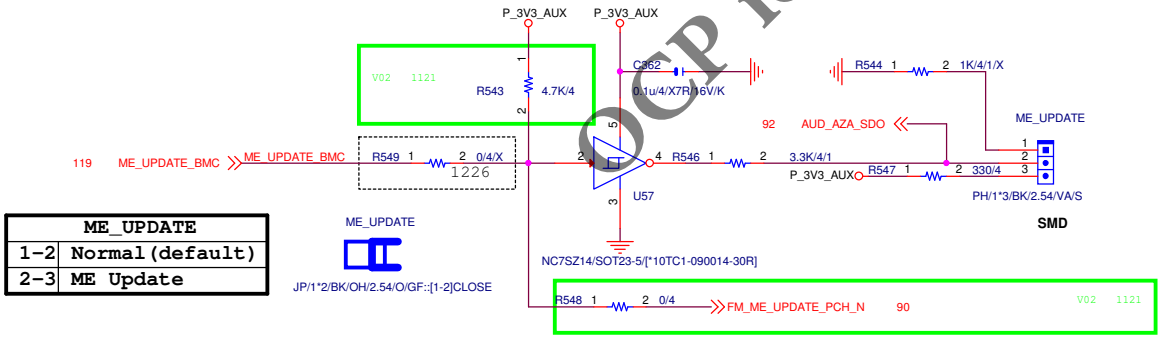


DESIGN NOTE:
INTEGRATED CLOCK CHIP DISABLE.
INTERNAL PULL-UP (15K-40K).
ENABLED WHEN SAMPLED LOW.
INTERATED CLOCK CHIP ENABLED FOR PPO AND PO.

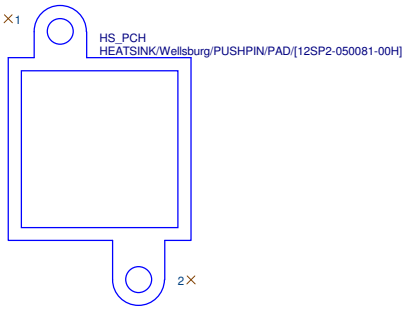


LT DEBUG	
1-2	Default
2-3	DEBUG MODE

DESIGN NOTE:
LT KEY DOWNGRADE.
P/U (1-2): LT DEBUG MODE IS DISABLED WHEN PULLED HIGH (DEFAULT).
P/D (2-3): LT DEBUG MODE IS ENABLED WHEN PULLED LOW.
THIS PIN IS SHARED WITH MEXP_BMBDATA1. IF THIS FEATURE NEEDS TO BE ENABLED.
PLEASE SET THE JUMPER TO 2-3 BEFORE PLTRST# AND THEN RETURN TO 1-2 FOR SMBUS FUNCTIONALITY.



ME_UPDATE	
1-2	Normal(default)
2-3	ME Update



DESIGN NOTE:
FLASH DESCRIPTOR SECURITY OVERRIDE.
* FLASH DESCRIPTOR SECURITY OVERRIDE WHEN HIGH SET JUMPER.
* FLASH DESCRIPTOR SECURITY NO OVERRIDE WHEN LOW (DEFAULT, NO JUMPER).

INTERNAL PD (9K-50K). MANUFACTURING JUMPER ALSO CAN BE USED TO SET THIS STRAP.

GIGABYTE™

Title: WBG STRAPPING/MISC (2/2)

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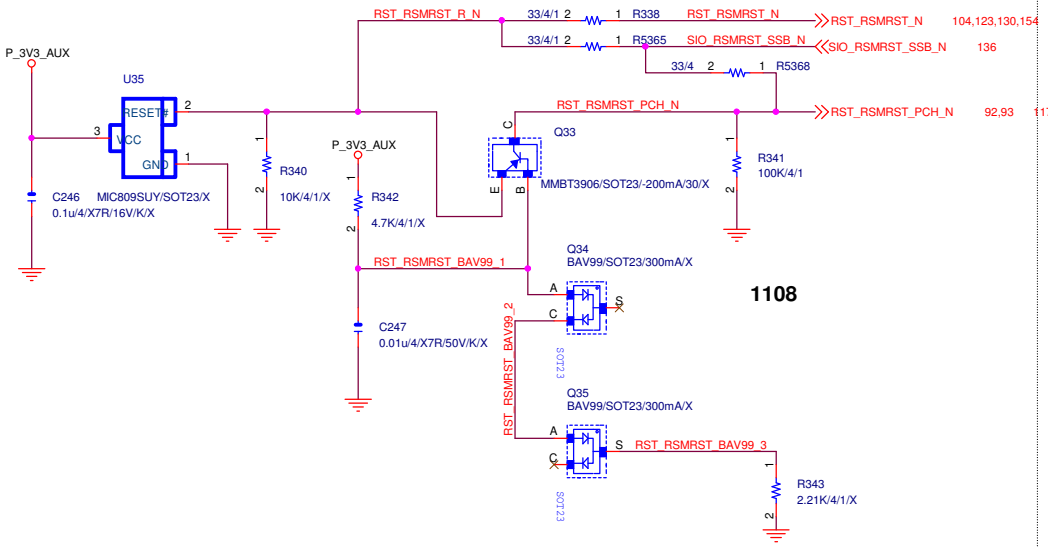
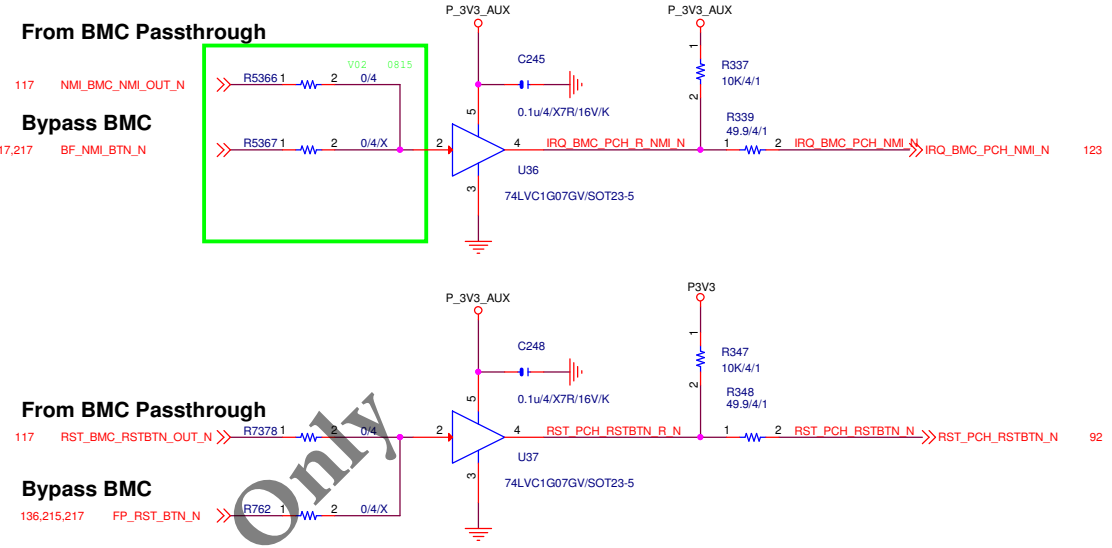
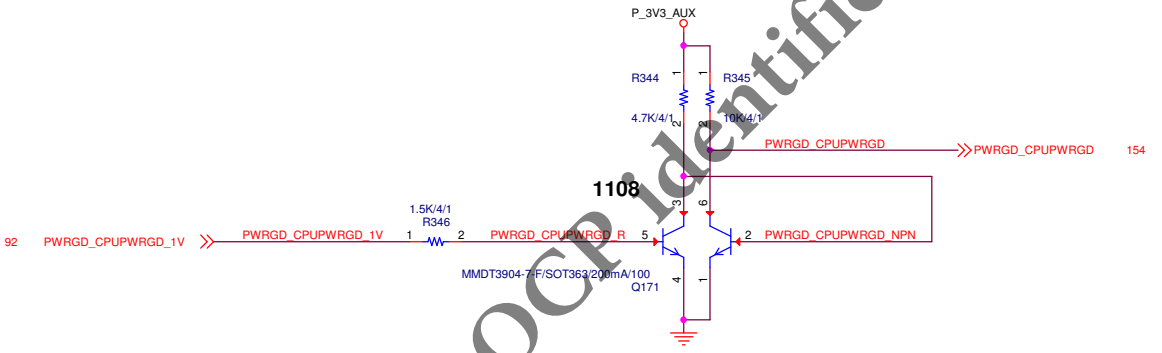
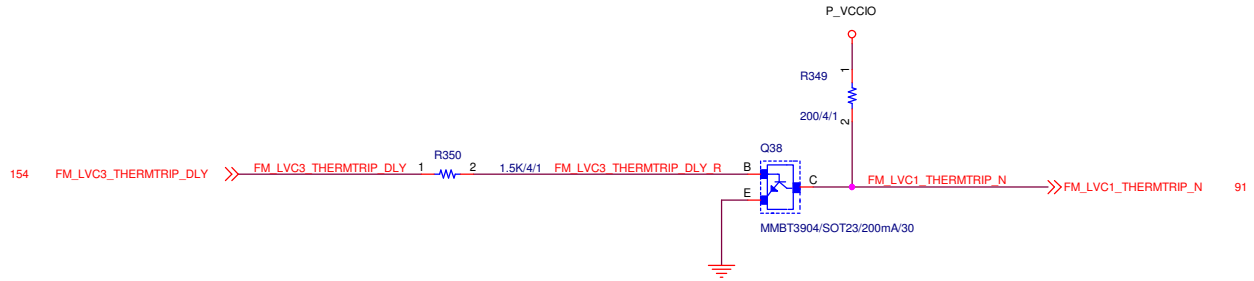
RTC Power-WELL ISOLATION









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Title: WBG ISOLATION/TERMINATION

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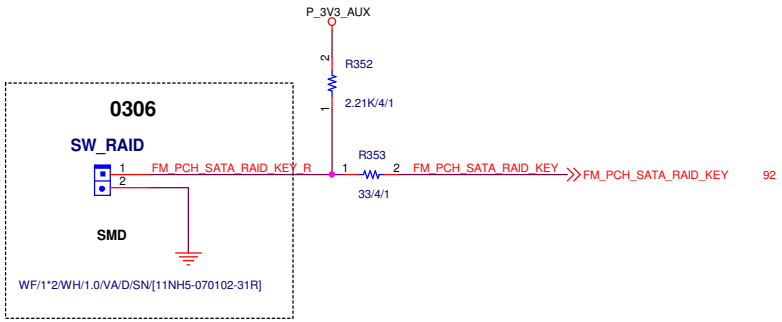
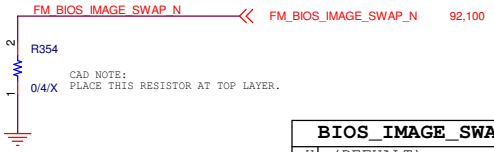
SATA RAID KEY

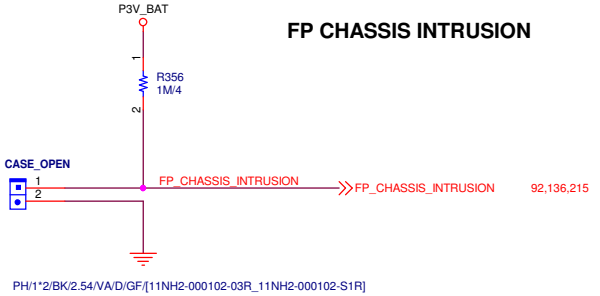


BIOS IMAGE SWAP JUMPER



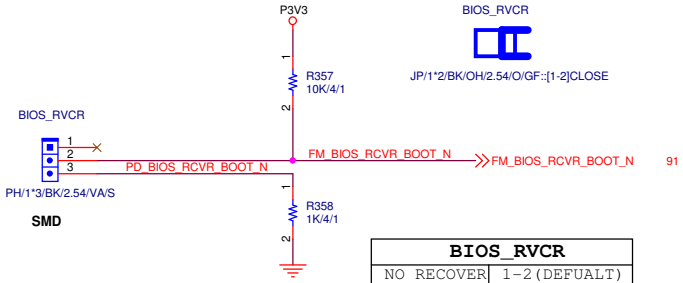
BIOS_IMAGE_SWAP	
H	(DEFUALT)
L	IMAGE SWAP

FP CHASSIS INTRUSION

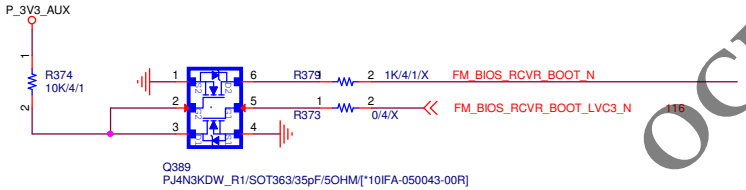


FP CHASSIS INTRUSION	
CHASSIS CLOSE	1-2 CLOSED
CHASSIS OPEN	1-2 OPEN

BIOS RECOVERY



BIOS_RVCR	
NO RECOVER	1-2(DEFUALT)
RECOVER	2-3



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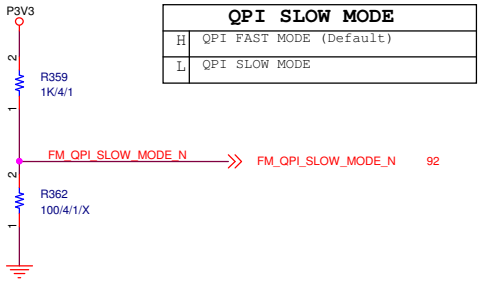
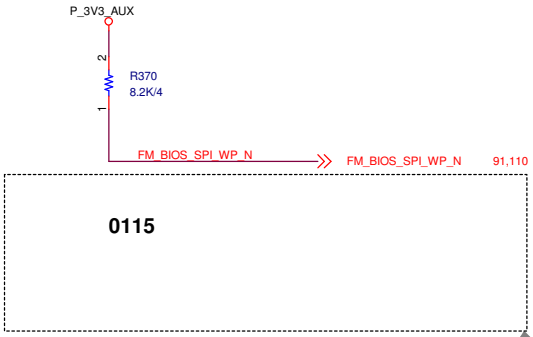
QPI SLOW MODE SELECT

CAD NOTE: PLACE THESE RESISTORS AT TOP LAYER.



QPI SLOW MODE	
H	QPI FAST MODE (Default)
L	QPI SLOW MODE

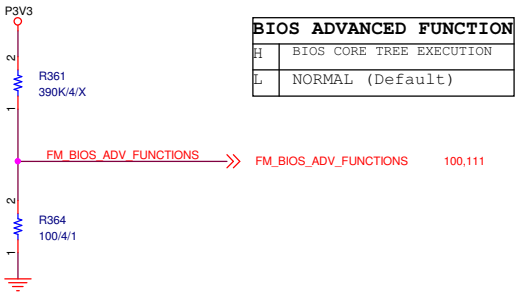
BIOS WRITE PROTECT



0115

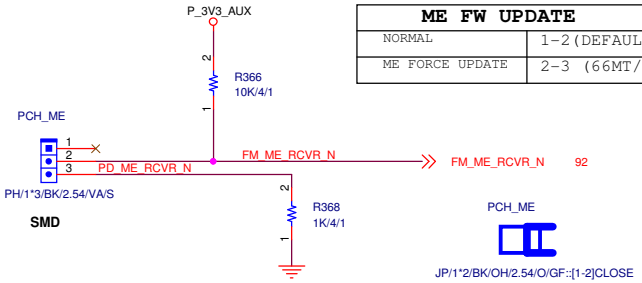
BIOS ADVANCED FUNCTIONS

CAD NOTE: PLACE THESE RESISTORS AT TOP LAYER.



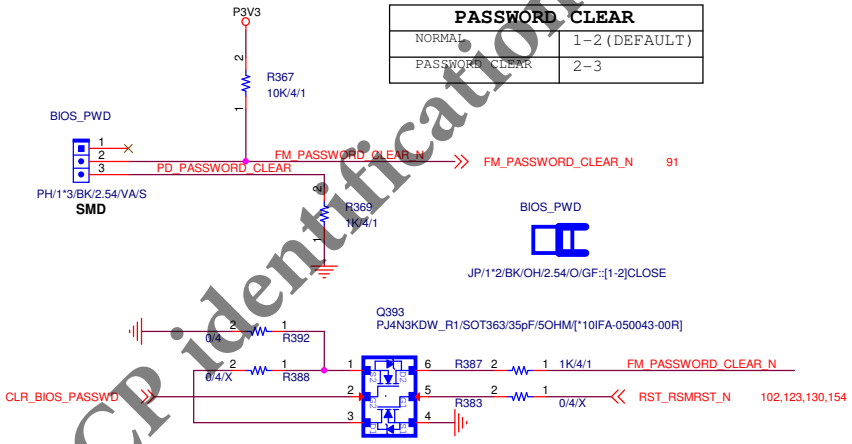
BIOS ADVANCED FUNCTION	
H	BIOS CORE TREE EXECUTION
L	NORMAL (Default)

ME FIRMWARE UPDATE



ME FW UPDATE	
NORMAL	1-2 (DEFAULT)
ME FORCE UPDATE	2-3 (66MT/S)

PASSWORD CLEAR JUMPER



PASSWORD CLEAR	
NORMAL	1-2 (DEFAULT)
PASSWORD CLEAR	2-3

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Title: WBG HEADERS (2/2)

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GIGABYTE™

Title: WBG SATA SGPIO

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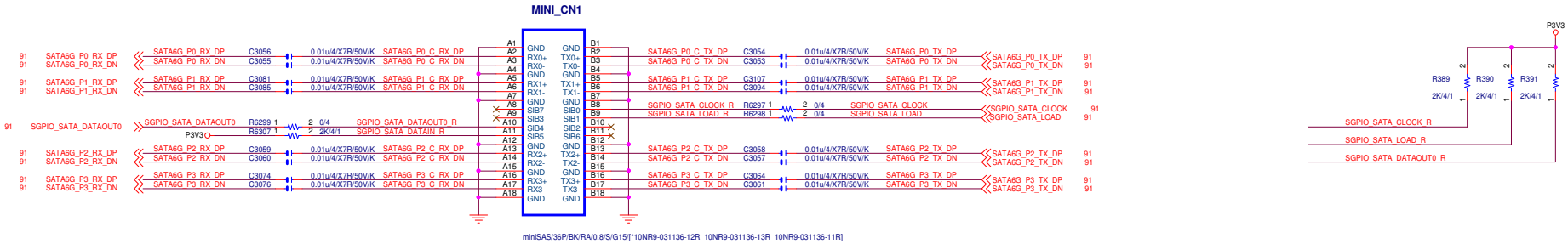
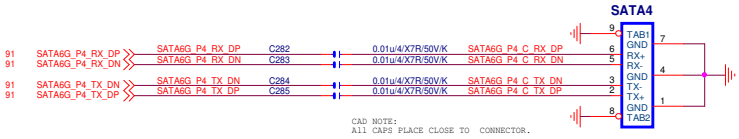
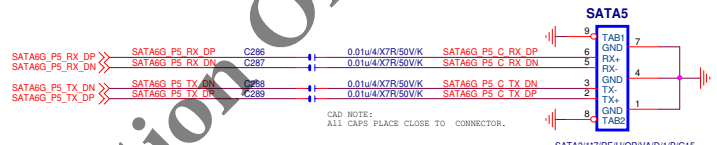
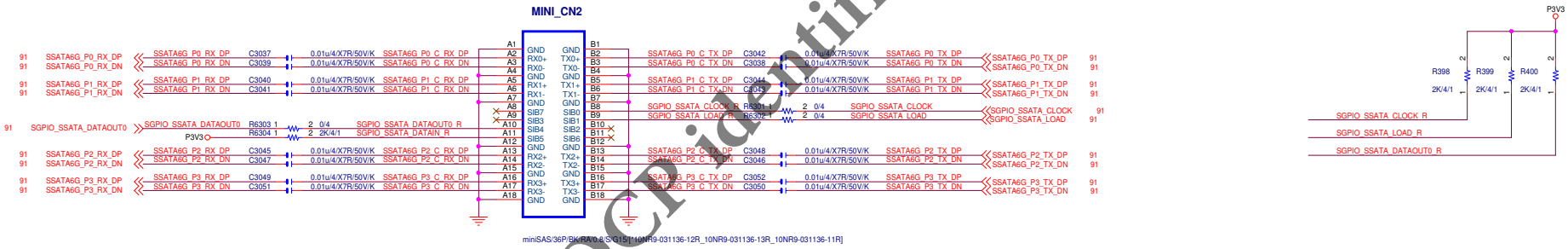




PCB Footprint = 11NH_SATA3-B90_7_000-GB



PCB Footprint = 11NH_SATA3-B90_7_000-GB



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Title: SAS & SATA SGPIO CONNECTORS

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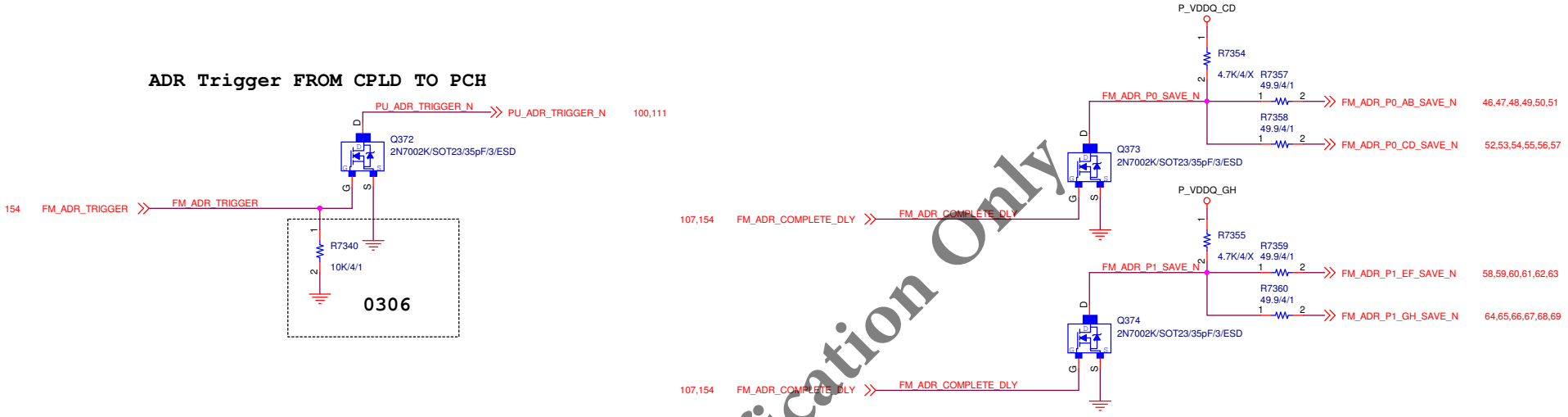
FM_ADR_COMPLETE_DLY FROM CPLD TO DIMM

ADR Trigger FROM CPLD TO PCH



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Title	USB CONNECTORS_INTERNAL	
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GIGABYTE™

Title: USB CONNECTORS_REAR1

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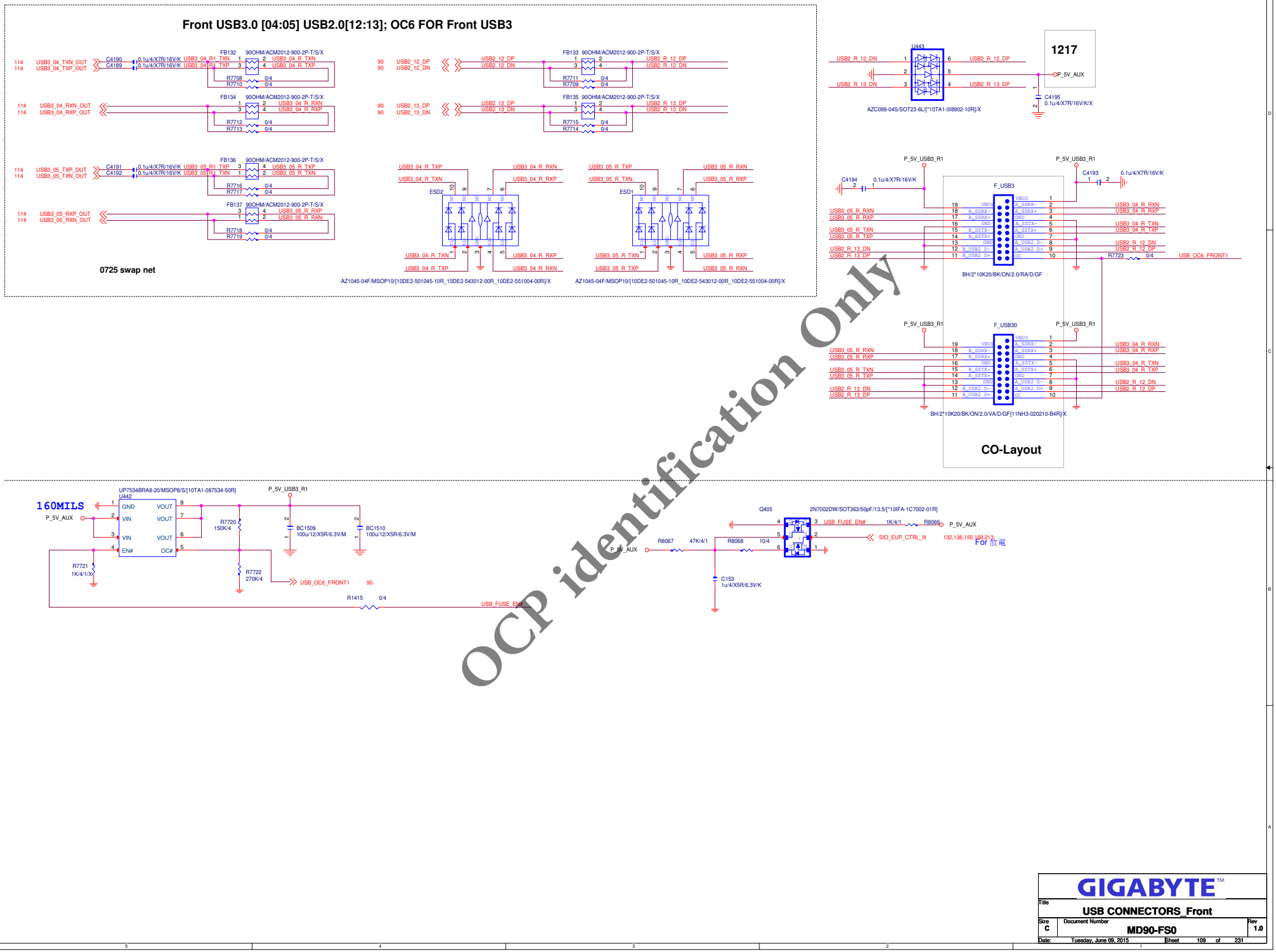

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Title	USB CONNECTORS_Front	
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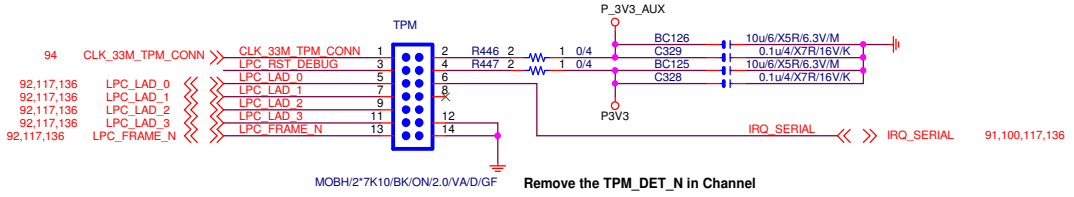
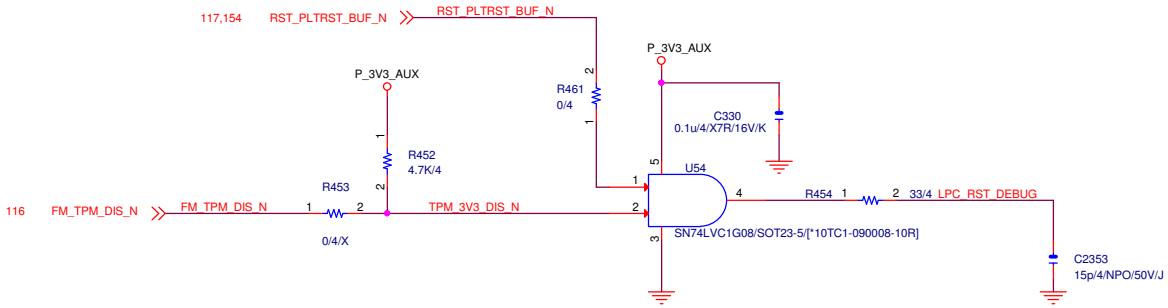
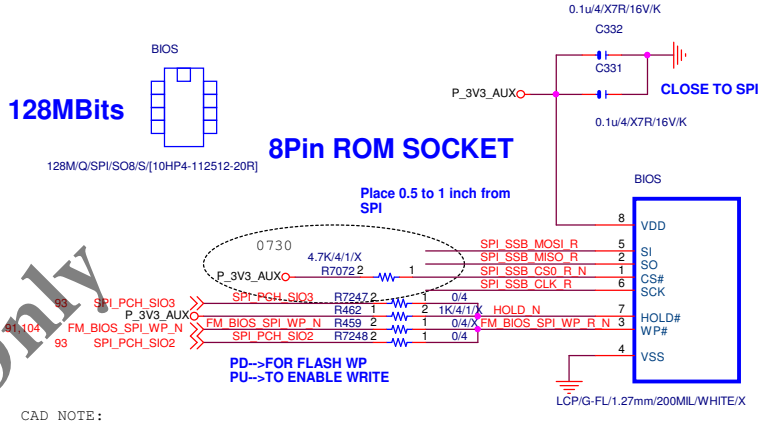
TPM



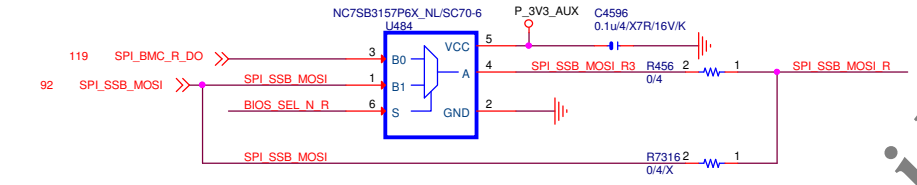


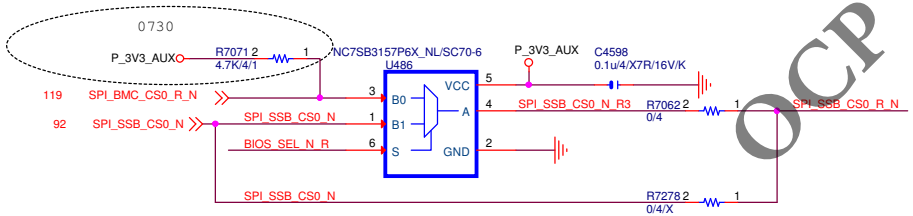
SPI BIOS

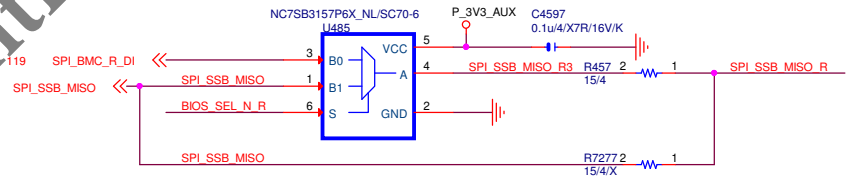
NOTE : SPI_CLK & SPI_MOSI must be length matched to within 500mils
SPI_CLK & SPI_CS0# must be length matched to within 500mils

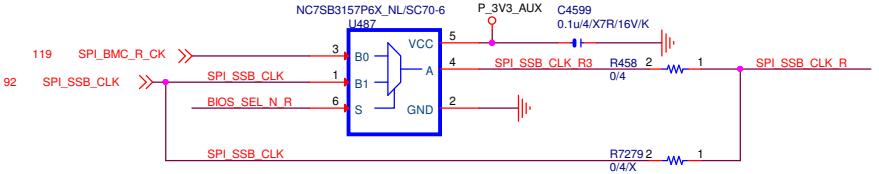


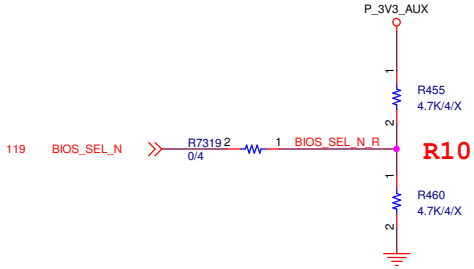
CAD NOTE:
PLACE ALL SERIES RESISTORS EXCEPT MISO R NEAR WBG<0.5 AND MISO R NEAR SPI <0.5.











R10: Stuff R7319.

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Title	WBG_SPI_BIOS_TPM	
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NOA_0_FM_USB_OC_0_N

OC0 USB3_FRONT1

NOA_1_FM_USB_OC_1_N

OC1 F_USB2

NOA_2_FM_USB_OC_2_N

P_3V3_AUX

90 NOA_3_FM_USB_OC_3_N — R471 1 2 10K/4/1

OC3

P_3V3_AUX

90 NOA_4_FM_USB_OC_4_N — R473 1 2 10K/4/1

OC4

NOA_5_FM_USB_OC_5_N

OC5 USB3_REAR1_2

NOA_6_FM_USB_OC_6_N

OC6 USB3_FRONT1

90 NOA_7_FM_PCIE_SLOT4_DET_ID0 — R517 1 2 0/4 — FM_PCIE_SLOT4_DET_ID0 87,100

OC7

NOA_8_GP21_PD

91,112 NOA_9_RST_PCIE_PCH_N — R465 1 2 0/4 RST_PCIE_PCH_N — RST_PCIE_PCH_N 100,154

91,111,112 NOA_10_FM_BIOS_ADV_FUNCTIONS — NOA_10_FM_BIOS_ADV_FUNCTIONS — NOA_10_FM_BIOS_ADV_FUNCTIONS 91,111,112

R467 1 2 0/4 FM_BIOS_ADV_FUNCTIONS — FM_BIOS_ADV_FUNCTIONS 100,104

91,111,112 NOA_11_FM_ADR_TRIGGER_N — NOA_11_FM_ADR_TRIGGER_N — NOA_11_FM_ADR_TRIGGER_N 91,111,112

R469 1 2 0/4 — PU_ADR_TRIGGER_N 100,107

91 NOA_12_FM_NM_THROTTLE_N

R472 1 2 0/4 FM_THROTTLE_N — FM_THROTTLE_N 79,121

91 NOA_13_FM_CPU_PROCHOT_N

R474 1 2 0/4 — FM_CPU_PROCHOT_N 80,100

92 NOA_14_FM_PCIE_SLOT4_DET_ID1

R476 1 2 0/4 — FM_PCIE_SLOT4_DET_ID1 100

92 NOA_15_FM_SMI_ACTIVE_N

R478 1 2 0/4 FM_SMI_ACTIVE_N — FM_SMI_ACTIVE_N 123

101,111,112 IRQ_BMC_PCH_NMI_NOA1_CLK — IRQ_BMC_PCH_NMI_NOA1_CLK — IRQ_BMC_PCH_NMI_NOA1_CLK 101,111,112

R498 1 2 4.7K/4/1 P3V3

92,111 FM_NMI_EVENT_N_NOA_CLK2 — FM_NMI_EVENT_N_NOA_CLK2 92,111

R5372 1 2 0/4 FM_NMI_EVENT_N — FM_NMI_EVENT_N 123

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Title	WBG NOA	
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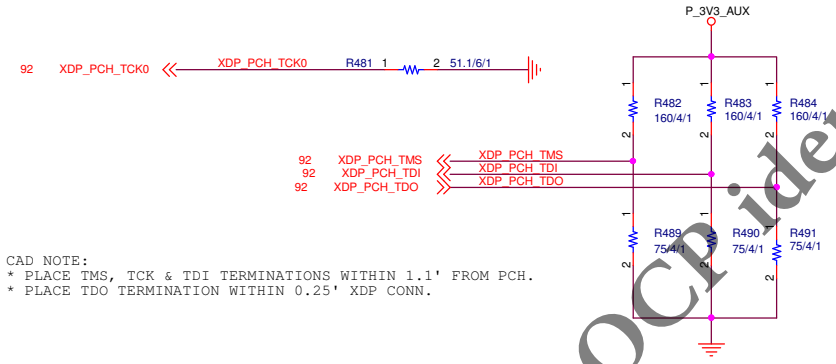
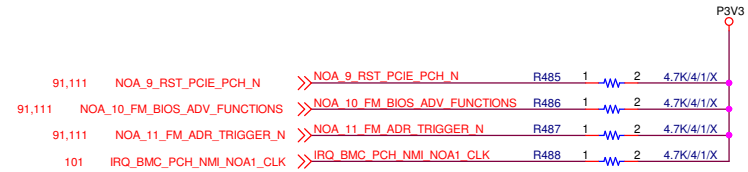
JTAG'S TERMINATIONS



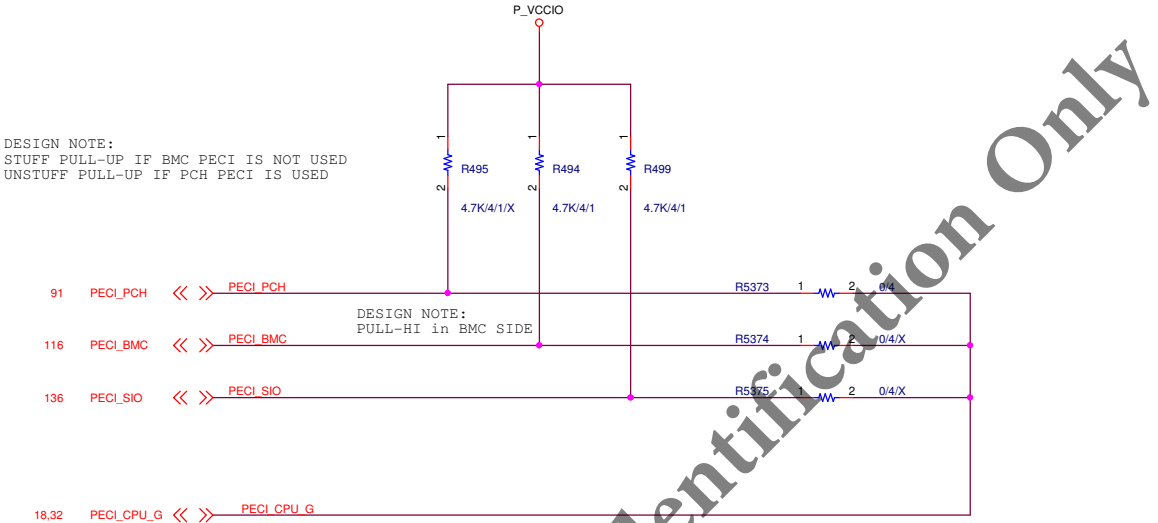
CAD NOTE:
* PLACE TMS, TCK & TDI TERMINATIONS WITHIN 1.1' FROM PCH.
* PLACE TDO TERMINATION WITHIN 0.25' XDP CONN.



DESIGN NOTE:
* THESE PULL UPS RESISTORS SHOULD BE PLACED WHEN NOA INTERFACE IS USED TO AVOID HW STRAP CORRUPTION.

GIGABYTE™

Title: WBG XDP		
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 112 of 231	



GIGABYTE™

Title: PECI		
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
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GIGABYTE™

Title

PAGE INDEX AND TITLE

Size	Document Number	Rev
A	MD90-FS0	1.0

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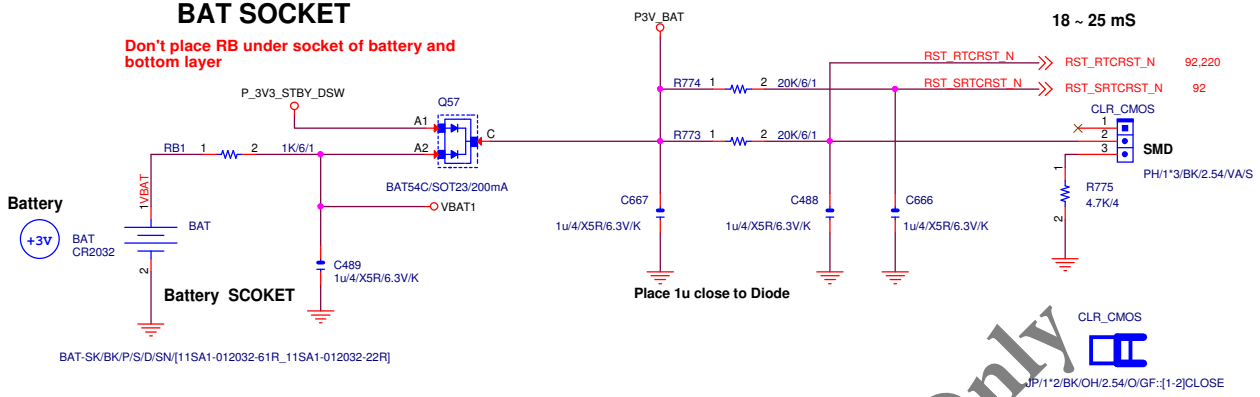
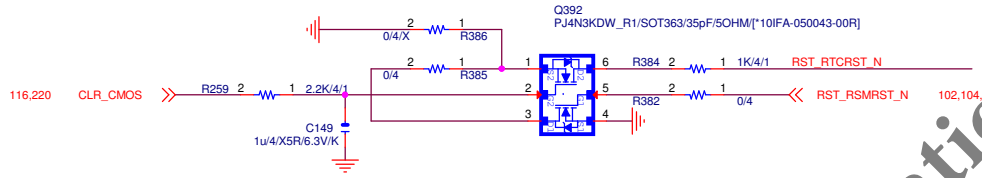
BAT SOCKET

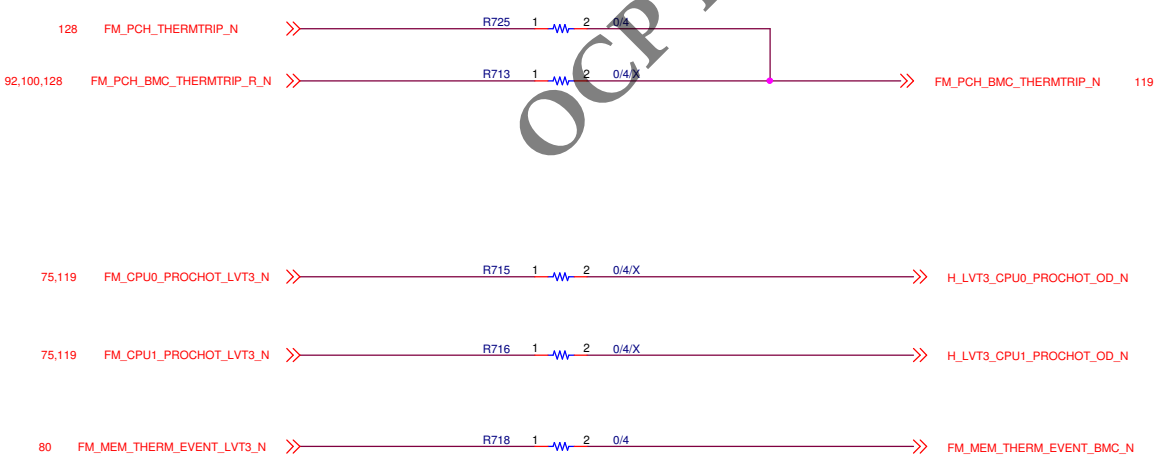
Don't place RB under socket of battery and bottom layer





CLR_CMOS	
NORAML	1 - 2(DEFAULT)
CLEAR CMOS	2 - 3

PCH-RELATED MISC SIGNALS



GIGABYTE™

Title	IBMC_SPI_FLASH & BAT SOCKET	
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V1 : RED	V6 : RED_RTN	V11 : N/C (ID0)
V2 : GREEN	V7 : GREEN_RTN	V12 : SDA
V3 : BLUE	V8 : BLUE_RTN	V13 : HSync
V4 : NC	V9 : SENSE	V14 : VSync
V5 : GND	V10 : GND/SYNC RETURN	V15 : SCL

VGA & COM

Use this cable to configure a Cisco router through the Console port at the router.
This cable is also suitable to be used with Sun T2000.

9 PIN D-SUB FEMALE to the Computer

RJ45 MALE CONNECTOR to the Cisco router

RJ45		DB9
RTS	1 8	CTS
DTR	2 6	DSR
TXD	3 2	RXD
GND	4 5	GND
GND	5 5	GND
RXD	6 3	TXD
DSR	7 4	DTR
CTS	8 7	RTS

GIGABYTE

Title: VGA_&_COM_PORT

Size: Custom | Document Number: MD90-FS0 | Rev: 1.0

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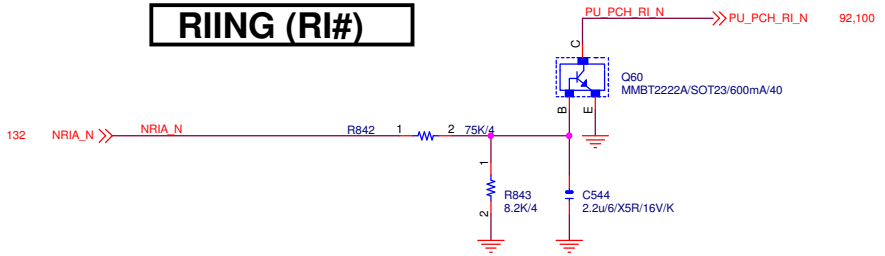
RIING (RI#)



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Title	IBMC_REAR_COM2	
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GIGA-BYTE TECHNOLOGY CO., LTD

Title

=========LAN & PHY=========

Size	Document Number	Rev
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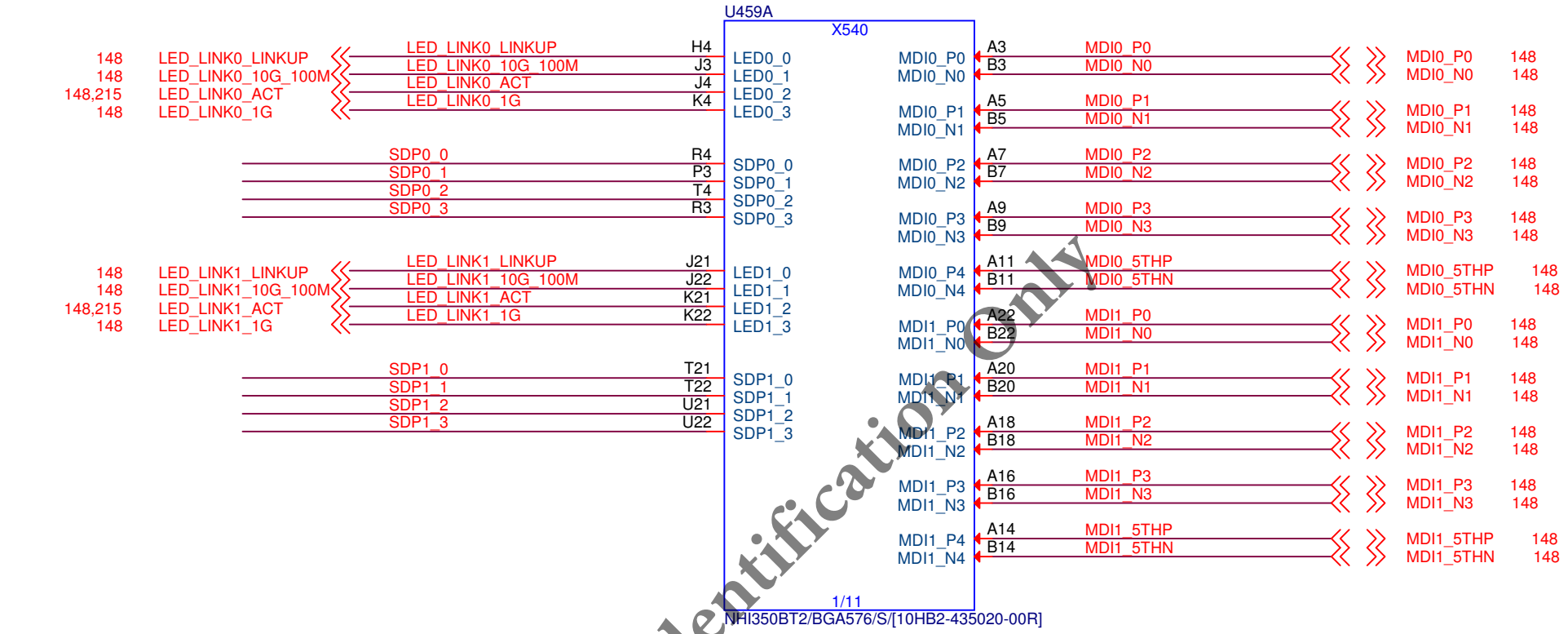
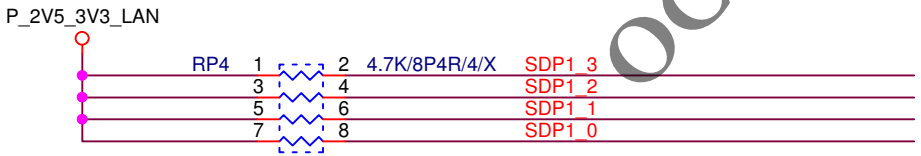
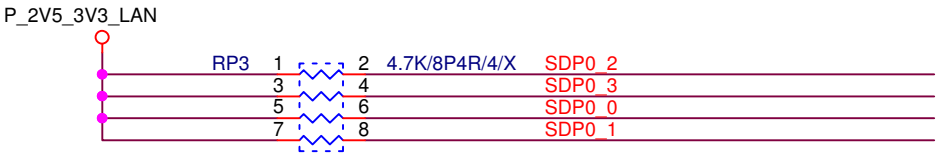
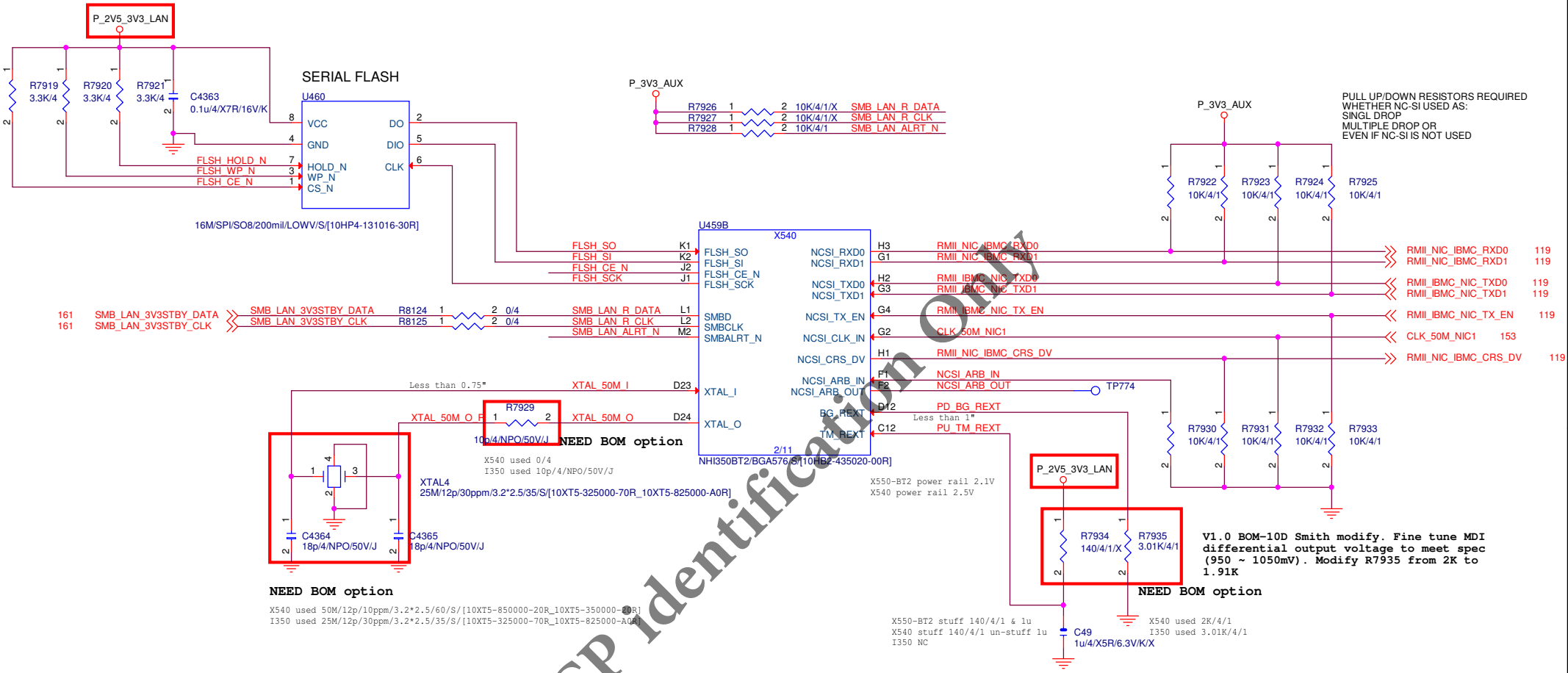






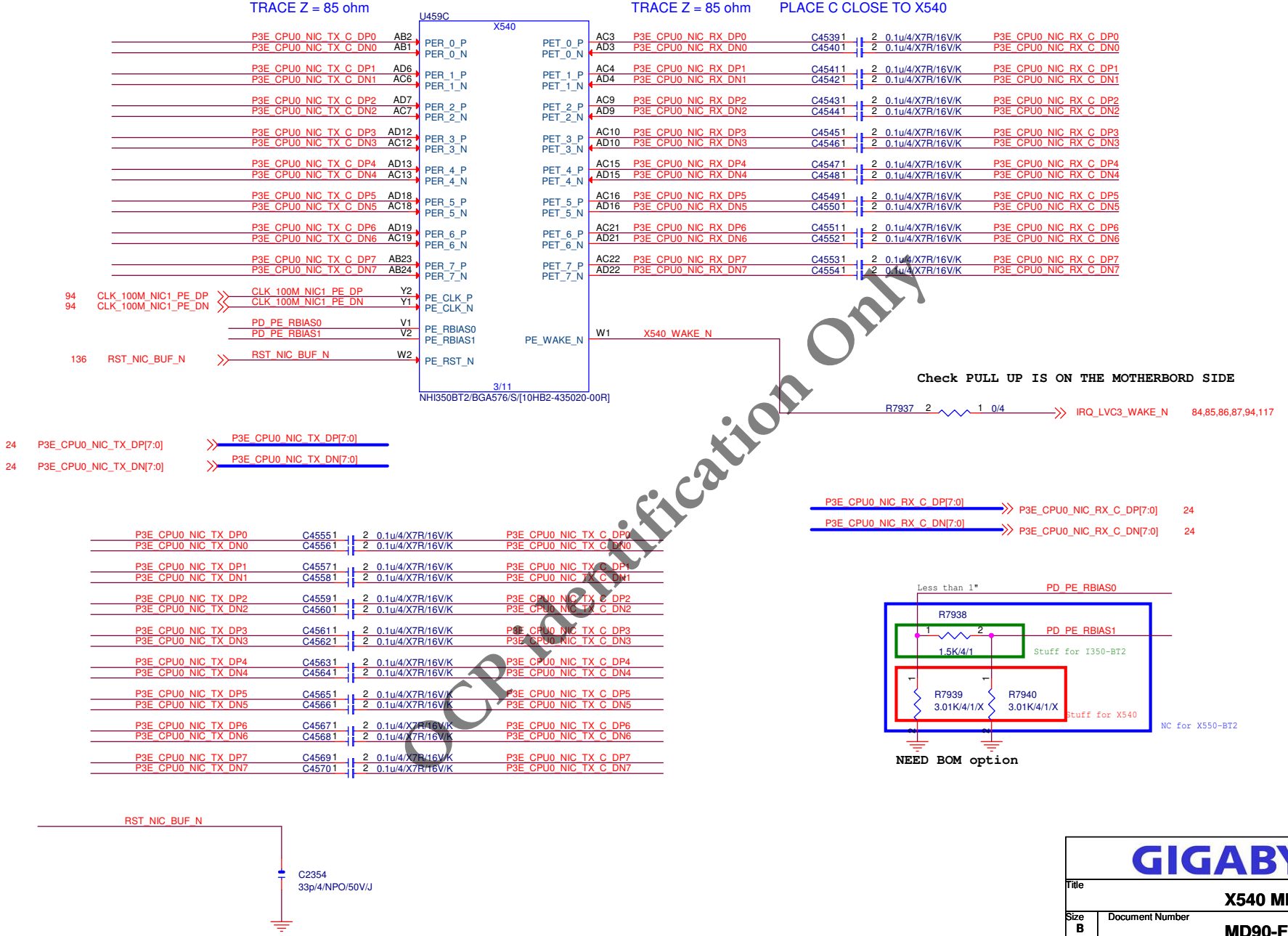
GIGABYTE™

Title: X540 PCIE		
Size: A	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 140 of 231	

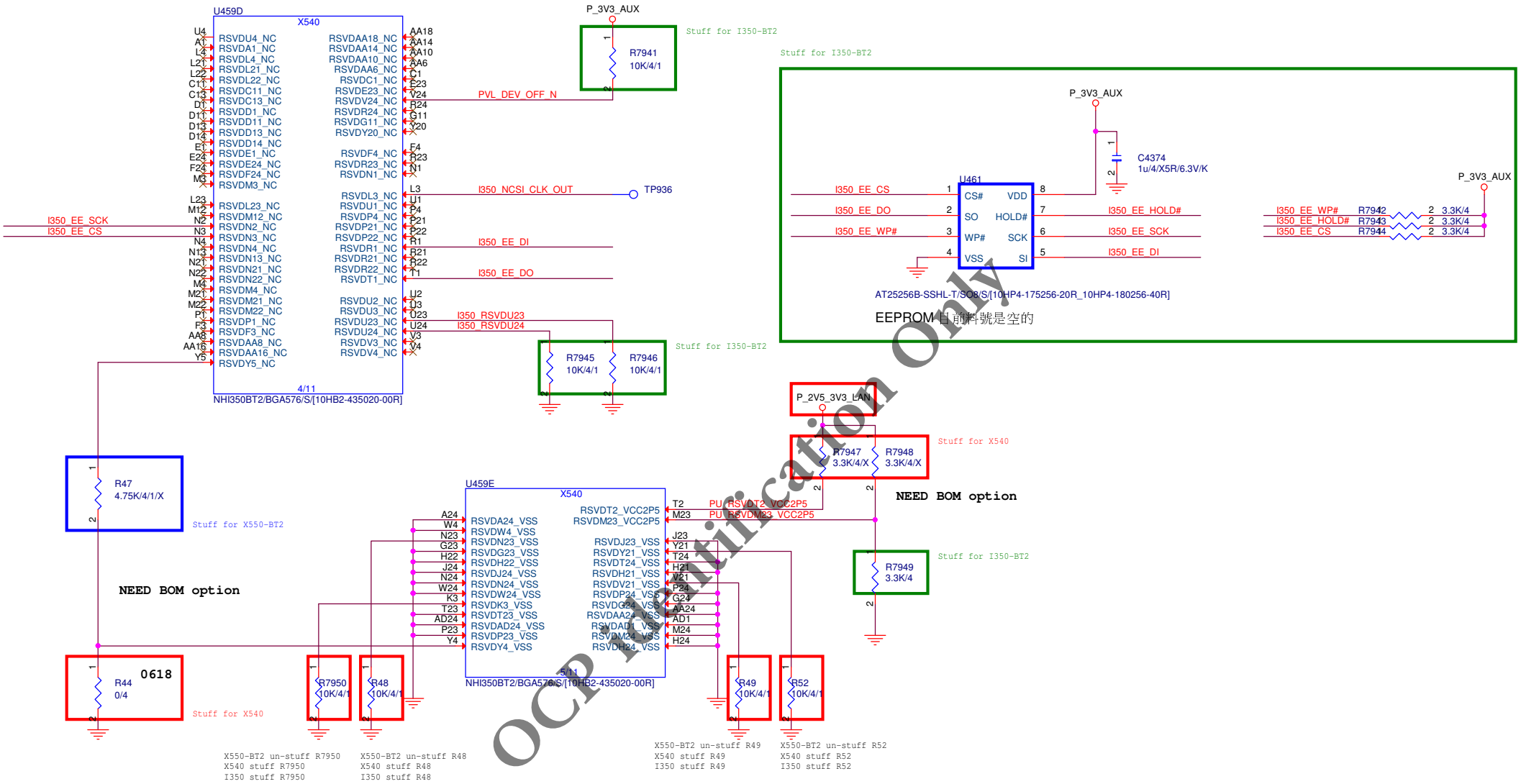


GIGABYTE™

Title	X540 RSVD PINS	
Size B	Document Number MD90-FS0	Rev 1.0
Date: Tuesday, June 09, 2015	Sheet 141 of 231	

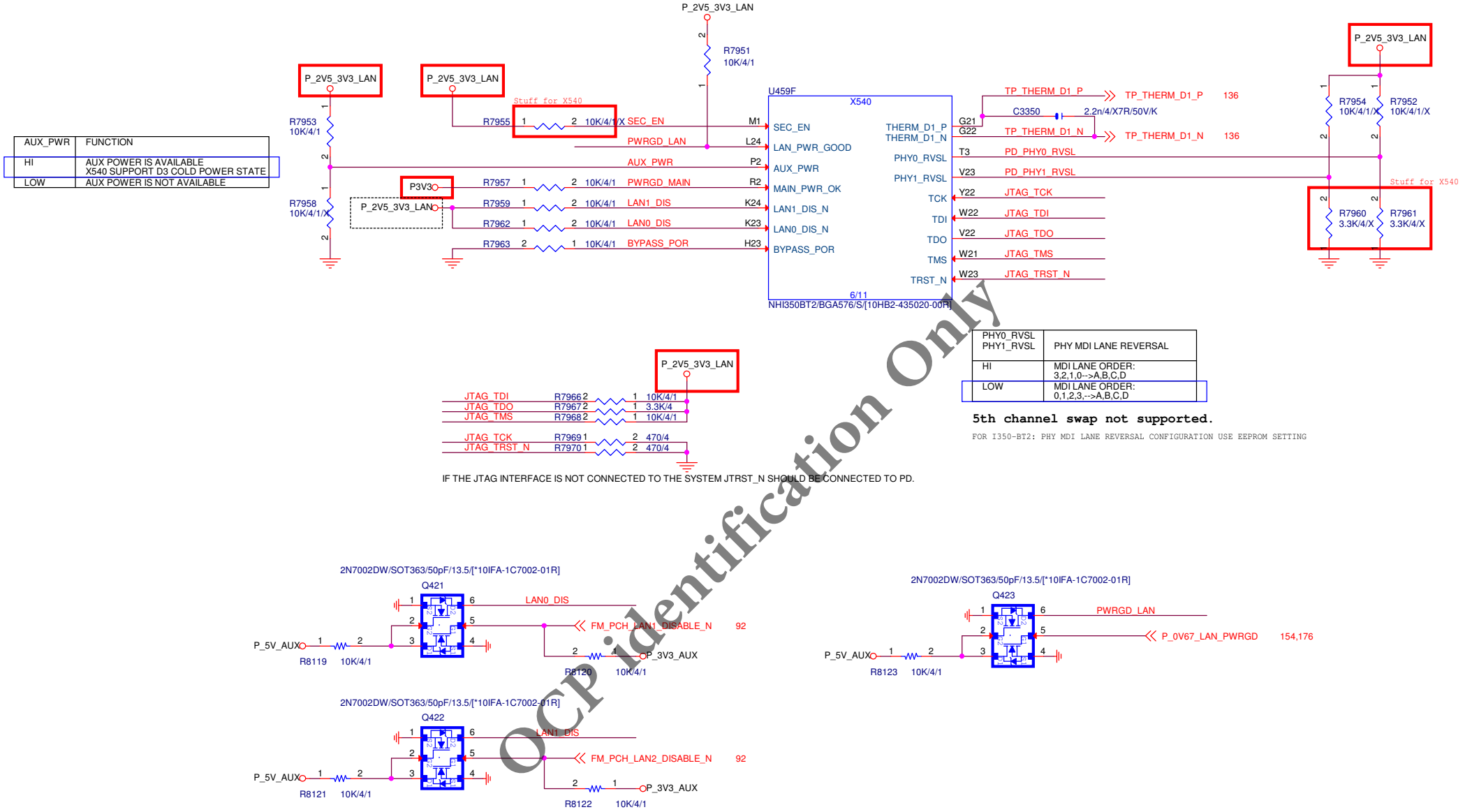


Title	X540 MISC		
Size B	Document Number MD90-FS0		Rev 1.0
Date: Tuesday, June 09, 2015	Sheet 142 of 231		



GIGABYTE™

Title	X540 POWER, VSS	
Size B	Document Number MD90-FS0	Rev 1.0
Date: Tuesday, June 09, 2015	Sheet 143 of 231	



AUX_PWR	FUNCTION
HI	AUX POWER IS AVAILABLE X540 SUPPORT D3 COLD POWER STATE
LOW	AUX POWER IS NOT AVAILABLE

PHY0_RVSL PHY1_RVSL	PHY MDI LANE REVERSAL
HI	MDI LANE ORDER: 3,2,1,0-->A,B,C,D
LOW	MDI LANE ORDER: 0,1,2,3,-->A,B,C,D

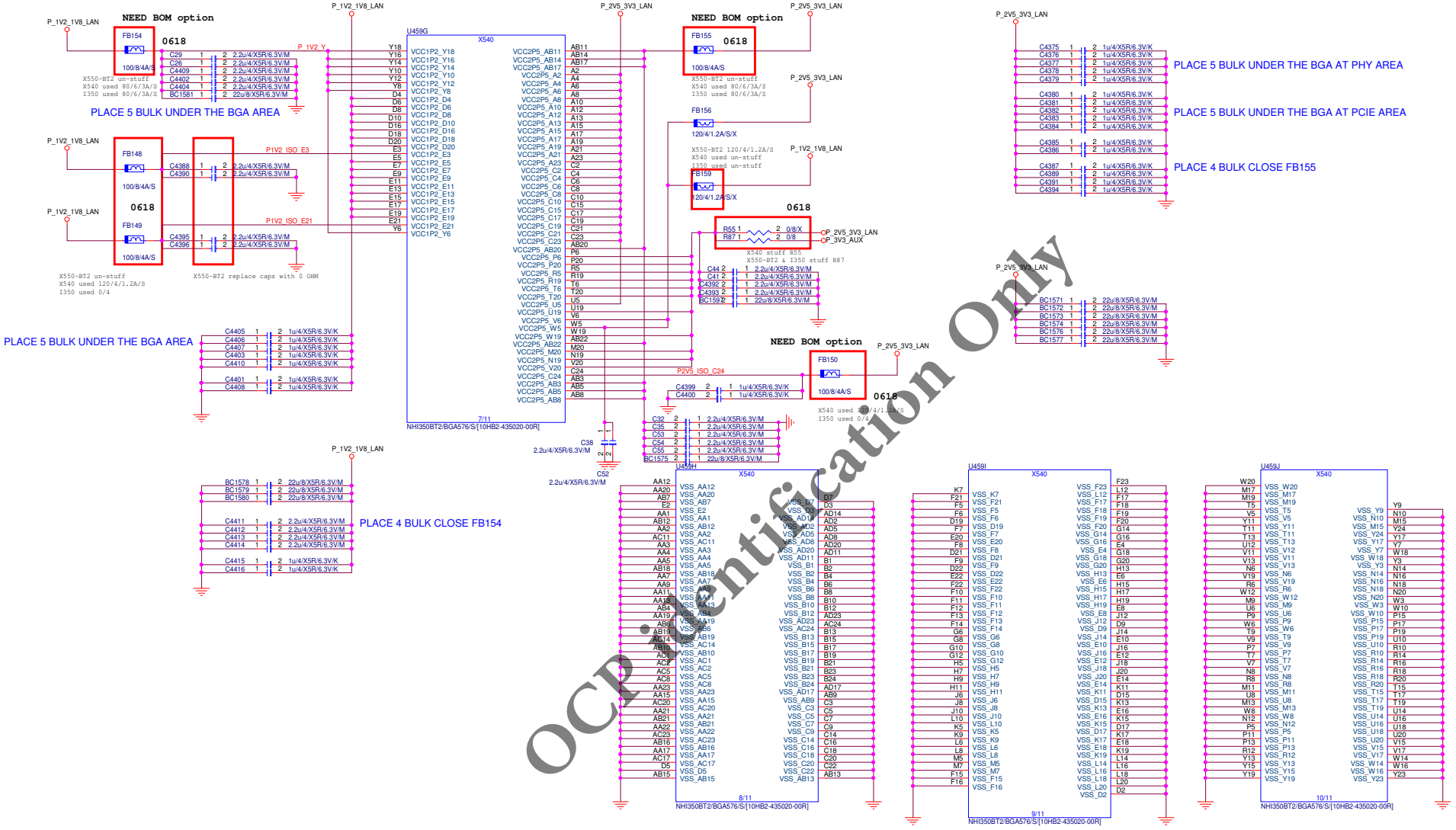
5th channel swap not supported.

FOR I350-BT2: PHY MDI LANE REVERSAL CONFIGURATION USE EEPROM SETTING

IF THE JTAG INTERFACE IS NOT CONNECTED TO THE SYSTEM JTRST_N SHOULD BE CONNECTED TO PD.

GIGABYTE™

Title: X540 POWER		
Size: B	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 144 of 231	



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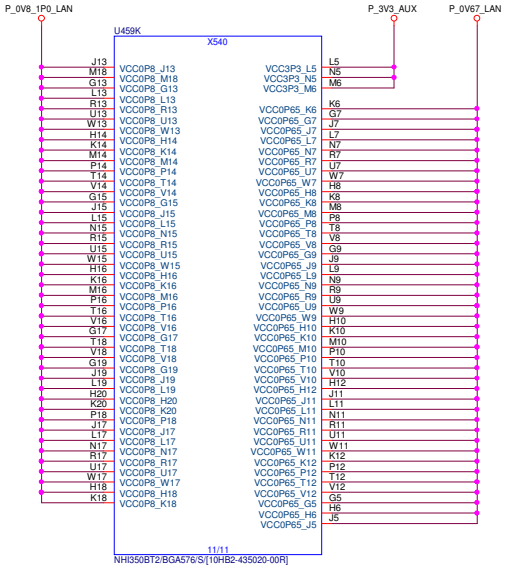
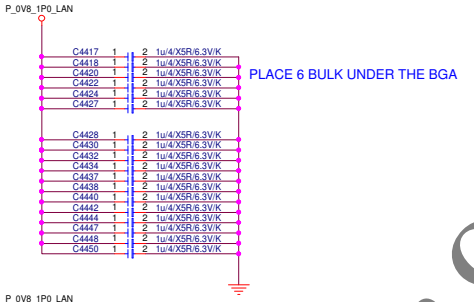
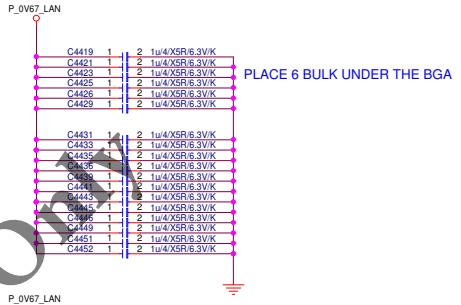
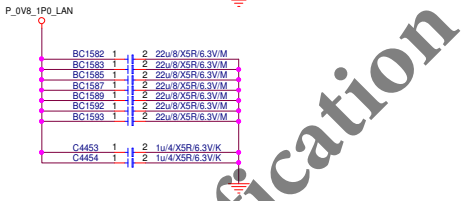
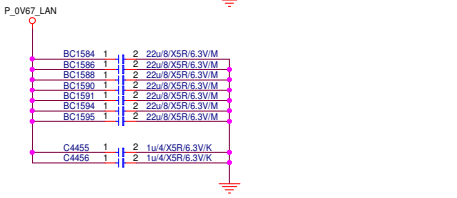
Title	10G_LAN CONNECTOR	
Size: C	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 145 of 231	

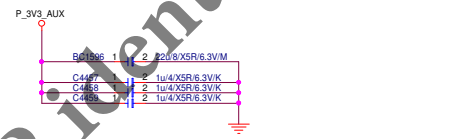


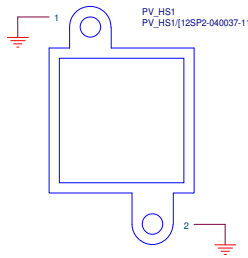




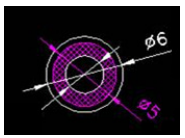




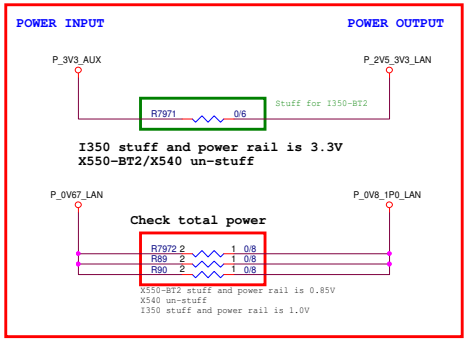




PCB Footprint = 12SP_60X16X10M7_2_100-GB



Power rail option



GIGABYTE™

Title	P_1V2_AUX_LAN	
Size C	Document Number MD90-FS0	Rev 1.0
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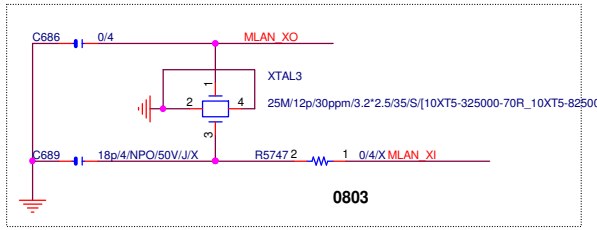
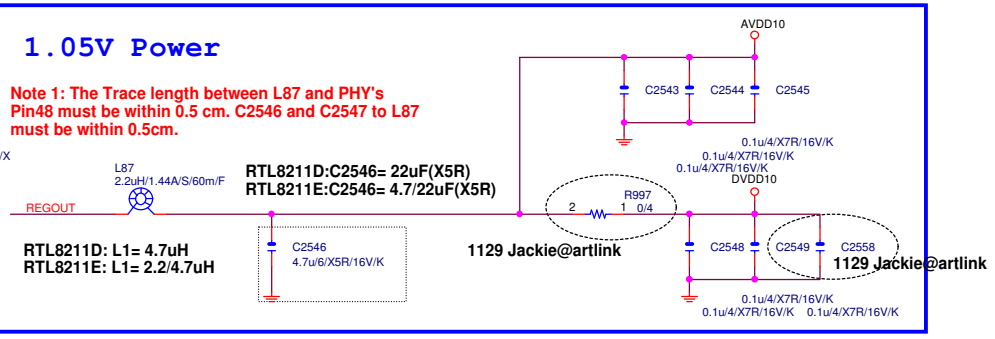
RTL8211E



1.05V Power

Note 1: The Trace length between L87 and PHY's Pin48 must be within 0.5 cm. C2546 and C2547 to L87 must be within 0.5cm.



0728

1119

153 CLK_50M_BMC_MAC1 R7450 2 1 82/4 MLAN_XI MLAN_XO

AVDD33 AVDD10

VDDREG

REGOUT

0313

CLK_125M_R_NDO R1001 2 1 22/4 CLK_125M_NDO 119

C2550 22p/4/NPO/50V/J/X

R5756 2 1 2.49K/4/1

R5757 2 1 0/4 AVDD33 P_3V3_AUX

U317

R5758 4.7K/4

RTL8211D
RTL8211E

GND(EPAD) REGOUT GND CLK125 VDDREG CKXTAL2 CKXTAL1 AVDD33 AVDD10 RSET ENSWREG DVDD33

MDI[0]+ MDI[0]- AVDD10 MDI[1]+ MDI[1]- AVDD33 MDI[2]+ MDI[2]- AVDD10 MDI[3]+ MDI[3]- NC

DVDD10 LED1/PHYAD1 LED0/PHYAD0 PMEB LED2_RXDLY MDIO MDC PHYRSTB DVDD10 TXCTL TXD3 TXD2

RXCTL/PHYAD2 RXD0/SELRGV DVDD33 RXD1/TXDLY RXD2/AN0 RXD3/AN1 RXC INTB DVDD33 TXC TXD0 TXD1

RTL8211E-VB-CG/QFN48/S

MLAN_MDI_P0 MLAN_MDI_N0 MLAN_MDI_P1 MLAN_MDI_N1 MLAN_MDI_P2 MLAN_MDI_N2 MLAN_MDI_P3 MLAN_MDI_N3

MLAN_LED1 R3226 2 1 0/4 LED_LINK_1G
MLAN_LED0 R3227 2 1 0/4 LED_LINK_100
MLAN_LED2 R5759 2 1 0/4 LED_ACT
RGMII_BMC_MLAN_MDIO
RGMII_BMC_MLAN_MDC
RSMRST_MLAN R996 2 1 0/4 RST_RSMRST_BUF_N 123
RGMII_BMC_MLAN_TX_CTRL
RGMII_BMC_MLAN_TXD_3
RGMII_BMC_MLAN_TXD_2

RGMII_BMC_MLAN_MDIO R983 2 1 1.5K/4/1
RGMII_BMC_MLAN_MDC R982 2 1 4.7K/4/X
P_3V3_AUX

RSMRST_MLAN C691 18p/4/NPO/50V/J

R5760 4.7K/4 P_3V3_AUX

RGMII_BMC_MLAN_R1_RX_CLK R3219 2 1 22/4 C2279 22p/4/NPO/50V/J/X
RGMII_BMC_MLAN_R1_RXD_3 R3244 2 1 22/4
RGMII_BMC_MLAN_R1_RXD_2 R3233 2 1 22/4
RGMII_BMC_MLAN_R1_RXD_1 R3232 2 1 22/4
RGMII_BMC_MLAN_R1_RXD_0 R3231 2 1 22/4
RGMII_BMC_MLAN_R1_RX_CTRL R3220 2 1 22/4

RGMII_BMC_MLAN_TXD_1 119
RGMII_BMC_MLAN_TXD_0 119
RGMII_BMC_MLAN_TX_CLK 119
RGMII_BMC_MLAN_RX_CLK 119
RGMII_BMC_MLAN_RXD_3 119
RGMII_BMC_MLAN_RXD_2 119
RGMII_BMC_MLAN_RXD_1 119
RGMII_BMC_MLAN_RXD_0 119
RGMII_BMC_MLAN_RX_CTRL 119

1129 Jackie@artlink

Configuration Setting

PHYAD0 PHYAD1 PHYAD2

P_3V3_AUX

R5739 2 1 4.7K/4/X MLAN_LED0 R5740 2 1 4.7K/4

Low=Link Up (Any speed)
High=Link Down (Any speed)

R5741 2 1 4.7K/4/X MLAN_LED1 R5742 2 1 4.7K/4

PHYAD2 only for RTL8211E

R5748 2 1 4.7K/4 RGMII_BMC_MLAN_R1_RX_CTRL R5749 2 1 4.7K/4/X

R5750 2 1 4.7K/4/X RGMII_BMC_MLAN_R1_RXD_2 R5751 2 1 4.7K/4

R5752 2 1 4.7K/4/X RGMII_BMC_MLAN_R1_RXD_3 R5753 2 1 4.7K/4

AN[1:0]=11: NWay. Advertise all capabilities
(10/1000Base-T; 100Base-TX Full/Half Duplex)

R5745 2 1 4.7K/4/X RGMII_BMC_MLAN_R1_RXD_0 R5746 2 1 4.7K/4

Pull up for 3.3V RGMII (RTL8211D/8211E)
Pull down for 2.5V RGMII(RTL8211D/8211E)
Pull up1.5 /1.8V RGMII (RTL8211E-VL only)

Low=Link Up (Any speed)
High=Link Down (Any speed)

R5743 2 1 4.7K/4 MLAN_LED2 R5744 2 1 4.7K/4/X

1119

RX Delay= 1: Add 2ns delay to RXC for RXD latching (via 4.7k-ohm to 3.3V)

R5754 2 1 4.7K/4 RGMII_BMC_MLAN_R1_RXD_1 R5755 2 1 4.7K/4/X

TX Delay= 0: Add 2ns delay to TXC for TXD latching (via 4.7k-ohm to 3.3V)

VDDREG

Note 2: The Trace length from C2251, C2252 to Pin 44,45(VDDREG) must be within 0.5 cm. The trace width from AVDD33 to Pin 44,45 should>40mils

P_3V3_AUX 1129 Jackie@artlink R998 2 1 0/4 VDDREG

C2551 4.7u/6/X5R/16V/K C2552 0.1u/4/X7R/16V/K

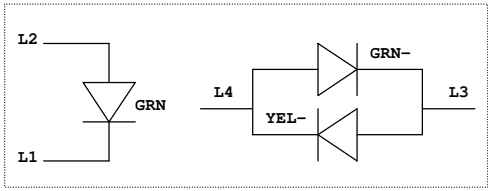
MLAN_MDI_P0 150
MLAN_MDI_N0 150
MLAN_MDI_P1 150
MLAN_MDI_N1 150
MLAN_MDI_P2 150
MLAN_MDI_N2 150
MLAN_MDI_P3 150
MLAN_MDI_N3 150

LED_ACT 150
LED_LINK_1G 150
LED_LINK_100 150

3.3V Power

P_3V3_AUX 1129 Jackie@artlink R999 2 1 0/4 AVDD33

BC1058 22u/8/X5R/6.3V/M
C2553 0.1u/4/X7R/16V/K
C2554 C2555 0.1u/4/X7R/16V/K 0.1u/4/X7R/16V/K
C2556 C2557 0.1u/4/X7R/16V/K 0.1u/4/X7R/16V/K



GIGABYTE™

Title	MLAN_PHY_RTL8211E	
Size: Custom	Document Number: MD90-FS0	Rev: 1.0
Date: Tuesday, June 09, 2015	Sheet 147 of 231	

	Name	Color	Condition	What it describes
LAN	Link/Activity	Green	ON	LAN link / No access
		Green	BLINK	LAN access
		-	OFF	Idle
	SPEED/Link	-	BLINK	Port identification (Base on Lan
	10/100 Speed	Green	ON	100Mbps connection
		-	OFF	10Mbps connection
	1GbE Speed	Yellow	ON	1Gbps connection
		Green	ON	100Mbps connection
		-	OFF	10Mbps connection
	10GbE Speed	Green	ON	10Gbps connection
		Yellow	ON	1Gbps connection
		-	OFF	100Mbps connection
	40GbE Speed Need check	Green	ON	40Gbps connection
		Yellow	ON	10Gbps connection
			OFF	1Gbps connection

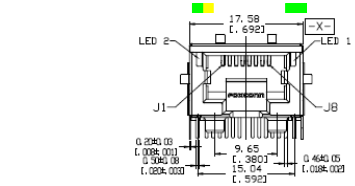
PLACE AND ROUTED AS BALANCED DIFFERENTIALLY
LOCATE CLOSE TO X540

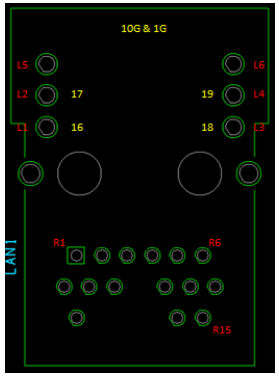
FOXCONN 1G
JFM3801J-B210-4F

X550-BT2 un-stuff inductors & cap but stuff 0 OHM
X540 stuff inductors & cap
1350 NC

10G LAN LED

1G LAN LED





Co-Layout Footprint
11NR_RJ45E0_21_C00-GB

	COLOR	LIGHT	ACTION
LINK/ACTIVITY	GREEN	ON	LAN LINK / NO ACCESS
	GREEN	BLINK	LAN ACCESS
	-	OFF	IDLE
10 GbE	GREEN	ON	10 Gbps CONNECTION
	GREEN	BLINK	IDENTIFICAT 10 Gbps CONN.
	YELLOW	ON	1 Gbps CONNECTION
	YELLOW	BLINK	IDENTIFICAT 1 Gbps CONN.
	-	OFF	10 Mbps OR 100 Mbps CONNECTION

Title	10G CONNECTOR
Size	C
Document Number	MD90-FS0
Rev	1.0
Date	Tuesday, June 09, 2015
Sheet	148 of 231